Design and Qualification of a High-Speed Low-Power Comparator in 40 nm CMOS Technology

Mohammad Zaki, Alireza ; Du, Yutong; Nihtianova, Stoyan

DOI
10.1109/ET59121.2023.10278935

Publication date
2023

Document Version
Final published version

Published in
2023 32nd International Scientific Conference Electronics, ET 2023 - Proceedings

2023 XXXII International Scientific Conference Electronics (ET) | 979-8-3503-0200-4/23/$31.00 ©2023 IEEE | DOI: 10.1109/ET59121.2023.10278935

Design and Qualification of a High-Speed Low-Power Comparator in 40 nm CMOS Technology

Alireza Mohammad Zaki, Yutong Du, and Stoyan Nihtianov
Department of Microelectronics, Faculty of Electrical Engineering, Mathematics, and Computer Science
Delft University of Technology
Mekelweg 5, 2628 CD Delft, The Netherlands
A.R.Mohammadzaki@tudelft.nl, Y.Du-10@student.tudelft.nl, S.Nihtianov@tudelft.nl

Abstract – **This paper presents the design methodology, test setup and experimental qualification results of a high-speed low-power threshold comparator in 40 nm CMOS technology intended for the registry of particles landing on a PIN-detector surface in particle detector readout electronics. The operation of the designed comparator is experimentally qualified for ideal digital pulses and analog signals generated by the preceding stages in a targeted potential application.**

Keywords – **high-speed; low-power; readout interface; voltage comparator; temperature sensor**

I. Introduction

Sensing fast and low-energy physical phenomena requires high-precision sensors as well as high-speed and low-noise readout electronics. The readout electronics comprise an analog frontend for signal extraction from the sensor and a digital backend for data processing which are interfaced through a multi-bit analog-to-digital converter, or a threshold comparator operating as one bit analog-to-digital converter, in the case of event registration [1 – 6]. Located at the very end of the analog frontend chain, the threshold comparator can perform a few different tasks depending on the information the detector is expected to supply, including: indicating the occurrence of an event, enabling the time measurement unit, and activating amplitude measurement [7]. As an illustration, in particle detector readout electronics, the signal of the comparator, besides indicating the arrival of a hit, can be used as a latch signal for a time stamp register or as a gate signal for a counter in a time-over-threshold amplitude measurement system [1], [7].

The threshold comparators must satisfy specific application requirements such as: signal processing speed, power consumption, noise, and offset, with a reasonable deviation over the commercial temperature range (0 to 70 degrees Celsius). Since a large part of the power budget is consumed in the frontend stages, the remainder of the available power may impose constraints on designing a cogent high-speed comparator that complies with the desired performance [8]. Thus, simple circuit architectures with small size transistor devices are preferred. Although the choice of small transistor devices provides benefits in processing speed by minimizing the parasitic capacitive loads and occupying less silicon area, it would negatively impact the noise and offset dispersion, which could potentially result in degradation of its operation accuracy. Feeding the comparator by an amplified and properly shaped signal in time domain, the input referred noise and offset of the threshold comparator would play a less significant role in the overall operation of the readout electronics.

The target is to design a high-speed and low-power threshold comparator for the PIN-detector readout electronics proposed in [9 – 11] to register the arrival time of the particles landing on the detector surface. The comparator should digitize the analog signal provided by the preceding stage, labeled as the signal shaper block, with a propagation delay shorter than 0.5 ns, an input referred offset of less than 1 mV, and power consumption of less than 70 µW over the commercial temperature range.

Section II presents the operation principle and architecture of the designed comparator. In Section III, the test setup for qualification of the comparator performance over the commercial temperature range as well as the calibrations are presented. Section IV provides the experimentally qualified performance results of the comparator driven by both the ideal digital pulses and analog voltage signals provided by the signal shaper block. The paper ends with conclusions.

II. Architecture and Design Methodology

To achieve an optimum tradeoff between speed, power consumption, and offset dispersion, the comparator was designed with a simple circuit architecture. As shown in Fig. 1, the comparator comprises a differential operational transimpedance amplifier (OTA) to compare the input signal with the threshold voltage V_{Th} and a few cascading inverters to both consolidate the logic levels at the output and minimize the delay time.

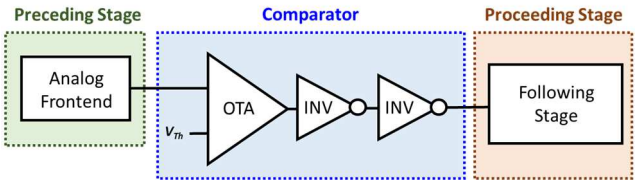

Fig. 1. Comparator block diagram.

The differential OTA (Fig. 2), in its simplest form, is a five-transistor amplifier with an NMOS differential input pair and PMOS mirrored load. The input differential pair was realized with NMOS transistors to comply with the 450 mV base line of the preceding stage (signal shaper). The transistors were sized to comply with the input referred offset dispersion. The choice of the OTA tail current I_{tail} sets the power consumption of the comparator; and has an impact on main performance parameters such as: noise and propagation delay. Table 1 summarizes the simulated

979-8-3503-0200-4/23/$31.00 ©2023 IEEE

operation metrics of the differential OTA as a function of the tail current I_{tail}. Concerning the presented simulation results, the differential OTA can fulfill the desired requirements in terms of speed, input referred noise, offset, and power consumption with a tail current of $I_{tail} = 40$ µA. Table 2 presents the size of the transistors in the differential OTA for $I_{tail} = 40$ µA.

The cascading inverters following the differential amplifier (Fig. 2) were optimally sized to minimize the propagation delay for driving a load capacitance C_L which comprises the equivalent capacitance of the digital backend network and the corresponding signal transmission line.

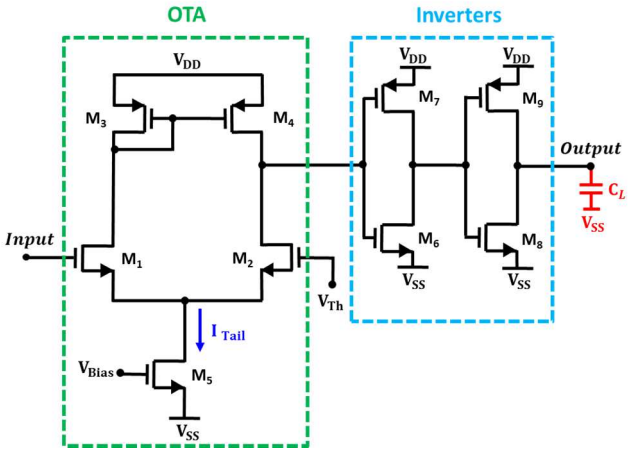

Fig. 2. Schematic of the differential OTA and the inverters.

TABLE 1. SIMULATED OPERATION METRICS OF THE DIFFERENTIAL OTA AS A FUNCTION OF THE TAIL CURRENT I_{tail}

Tail Current I_{Tail}	20 [µA]	30 [µA]	40 [µA]	50 [µA]
Gain [dB]	25.14	25.52	24.57	24.29
Bandwidth [GHz]	0.811	0.891	1.075	1.137
Rise Time [ps]	19.6	18.9	18.1	17.8
Noise [µV_{rms}]	290.3	246.2	228.9	209.7
Offset [mV]	0.64	0.57	0.52	0.48
Power [µW]	28.9	37.53	52.17	63.74

TABLE 2. DIFFERENTIAL OTA TRANSISTOR SIZES FOR $I_{tail} = 40\ \mu A$

Transistors	W [µm]	L [µm]
M_1, M_2	1.44	0.3
M_3, M_4	7.2	0.48
M_5	2.2	0.1

III. QUALIFICATION TEST SETUP

For the experimental verification of the performance of the comparator, a qualified and cogent test setup, as well as high precision lab equipment, was used. A few auxiliary blocks were implemented on the chip to facilitate the qualification of the comparator performance.

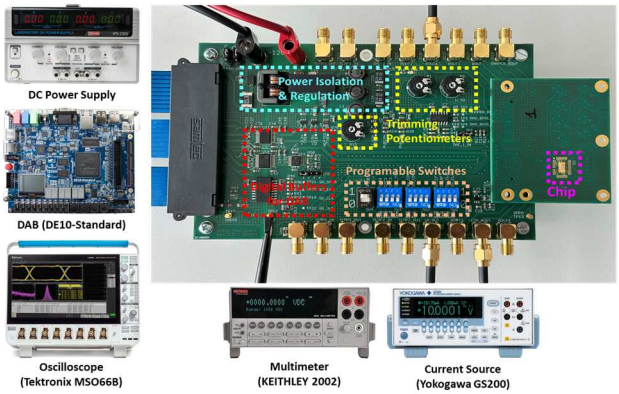

Fig. 3. Qualification test setup.

A. Discriminator Testbench

Figure 3 illustrates the test setup. Figure 4 presents the chip block diagram including the discriminator and the auxiliary blocks implemented to facilitate the qualifications. To evaluate the operation speed and the delay of the comparator, it must be driven by a sharp rising edge and high amplitude voltage signals, representing the output signal of the previous stage in the targeted application: the signal shaper block. For this purpose, a digital buffer including four cascaded inverters was implemented for driving the comparator input node. The comparator reacts to the given input signal and generates a digital pulse with a propagation delay of t_p indicating the moment the input signal passes the threshold level V_{Th}. An FPGA-based data acquisition board (DAB) was used in this test to trigger the digital buffer and collect the pulses generated by the comparator. The DAB communicates with the chip through low voltage differential signal (LVDS) interfaces. Both the DAB trigger pulse and the comparator digital pulse were monitored by a 1 GHz oscilloscope (Tektronix MSO66B) through active probes to calculate the comparator propagation delay t_p.

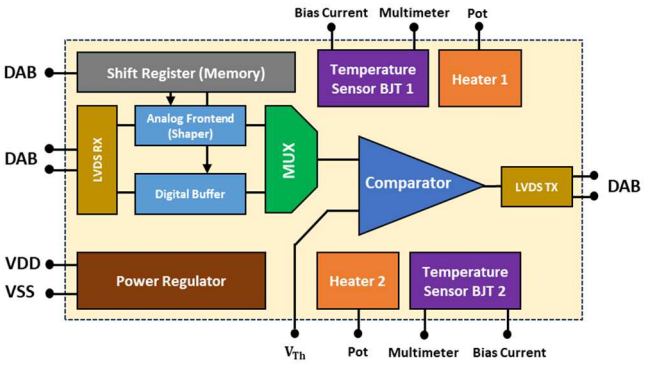

Fig. 4. Chip block diagram for experimental comparator qualification.

B. Temperature Measurement

To qualify the comparator operation over the commercial temperature range, two resistive-based thermal heaters and two temperature sensors were implemented on-chip in close vicinity of the comparator. The thermal heaters were two polysilicon resistors with $R = 100\ \Omega$, which were warming up the chip through self-heating as a function of their power dissipation. Thus, the power of these resistors could simply be controlled by tuning the applied voltage through a

potentiometer on the test PCB. On the other hand, the cooling was done by a Peltier plate glued onto the test PCB under the chip.

The temperature sensors were implemented with bipolar junction transistors (BJT) available in the CMOS process, using their $I_C - V_{BE}$ characteristics as a function of temperature. There are two general requirements for implementing a temperature sensor: a temperature-dependent signal and a temperature-independent reference. A proportional-to-absolute-temperature (PTAT) signal can be obtained by measuring the difference of the base-emitter voltages ΔV_{BE} of a diode-connected BJT transistor for two different collector currents I_{C_1} and I_{C_2}:

$$\Delta V_{BE} = V_{BE_1} - V_{BE_2} = \frac{KT}{q} ln\left(\frac{I_{C_1}}{I_{C_2}}\right) \quad (1)$$

where, q is the electron charge, K is the Boltzmann constant, and T is the absolute temperature in Kelvin.

Accurate temperature measurement requires bias currents of the BJT transistors to fall within a specific margin. The biasing current must be much larger than the saturation current I_S to avoid BJT operation in the low injection region. On the other hand, the maximum bias current must be set to avoid BJT operation in the high injection region as well as to keep the transistor current gain β independent of the biasing current [12]. Concerning the above-mentioned criteria and probing the operation of the BJT transistor through simulation results, the margins of the bias currents were set at $I_{C_{min}} = 50$ µA and $I_{C_{max}} = 890$ µA. In addition, the voltage drop over the parasitic series resistance of the BJT transistor can give rise to inaccuracy in the temperature measurement, which can be simply eliminated by using three different currents to bias the BJT transistor [12], [13]. Thus, the three bias currents were set to $I_{C_1} = 50$ µA, $I_{C_2} = 500$ µA, and $I_{C_3} = 800$ µA. Using three biasing currents, it is shown in [12] that the PTAT ΔV_{BE} can be calculated as:

$$\Delta V_{BE} = -\frac{2}{45} V_{BE}|_{I_{C_1}} - \frac{1}{15} V_{BE}|_{I_{C_2}} + \frac{1}{9} V_{BE}|_{I_{C_3}} \quad (2)$$

where $V_{BE}|_{I_1}$ is the base-emitter voltage for the bias current I_{C_1}. The bias currents are provided by an external high precision current generator (Yokogawa GS200) to make their value chip-temperature independent, while their V_{BE} voltage is measured by an external multimeter (KEITHLEY 2002).

IV. Experimental Results

The goal of the following experimental tests was to evaluate the propagation delay of the proposed comparator t_p for different threshold levels as well as to qualify the operation over the commercial temperature range.

First, an attempt was made to verify experimentally the performance of the integrated BJT-based temperature sensors through a calibrated 10 KΩ external NTC thermistor, glued on top of the chip, the resistance of which is read through the four-wire method by the same high precision multimeter.

A. Temperature Sensor Validation

The chip temperature was measured by an external NTC thermistor while the temperature was varied by means of the aforementioned heating and cooling mechanisms. The chip and the NTC thermistor were covered by a plastic cap to isolate them from environmental temperature variations. Figure 5 illustrates the temperature validation setup. It is worth mentioning that, for each temperature level, the setup was settled for 40 minutes to reach the thermal equilibrium between the NTC thermistor and the chip (including the BJT-based temperature sensors). The minimum obtainable temperature through this setup was 25^oC due to: the limited cooling power of the Peltier plate; the non-ideal thermal isolation of the testbench; and the self-heating of the chip even when the heaters were completely switched off.

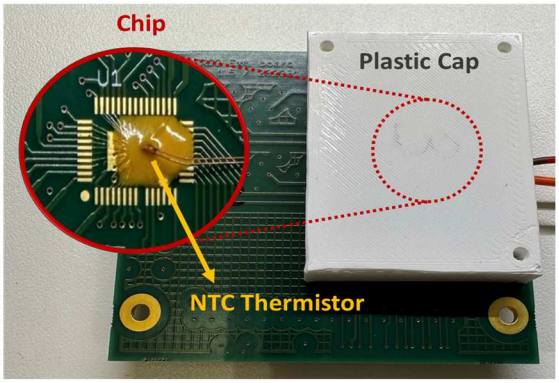

Fig. 5. Temperature calibration setup: (a) the NTC thermistor glued onto the chip; (b) the plastic cap.

For each calibration point, the BJT-based temperature sensors were biased in turn with the external currents (I_{C_1}, I_{C_2}, and I_{C_3}), their base-emitter voltages V_{BE} were recorded by the external multimeter, and their PTAT voltage ΔV_{BE} was calculated using Eq. 2. For mapping the experimentally obtained ΔV_{BE} to the temperature, the post-layout simulation results were exerted. Table 3 presents the measured temperature using the NTC thermistor and the BJT-based temperature sensors. By deactivating the cooling and heating mechanisms, the chip operated at 40^oC (according to the built in BJT-based temperature sensors), due to its self-heating through power dissipation.

Results indicated that there was a varying offset between the average temperature measured by the BJT-based temperature sensors and the NTC thermistor. Such an offset was probably due to the thermal gradient of the medium between the chip and the NTC thermistor (i.e., chip passivation layer, thermo conductive glue, and NTC thermistor cover). For temperature levels higher than 40^oC, the BJT-based sensors reported a larger temperature than what the NTC thermistor senses on its surface. On the other hand, for temperature levels lower than 40^oC, the BJT-based temperature sensors reported a lower temperature as the cooling mechanism was implemented under the chip, while the NTC thermistor was mounted on top of the chip. Unfortunately, this offset could not be eliminated even by letting the test setup settle the temperature for a longer time, due to the thermal resistance between the chip and the NTC thermistor leading to the existing thermal gradients.

TABLE 3. MEASURED CHIP TEMPERATURE USING THE NTC THERMISTOR AND THE BJT-BASED SENSORS

Sensors	NTC	BJT 1	BJT 2
Temperature Value	25	23.4	23.8
	30	28.6	29.3
	40	40.7	41.2
	50	51.1	51.8
	60	60.9	61.5
	70	71.3	72.1
	80	81.4	82.3

Despite the fact that we could not accurately calibrate the integrated temperature sensors with our setup, the results showed that using an external temperature senor always carries the risk to measure temperatures different from that of the device under test. The existing offset between the two integrated temperature sensors was most probably due to their different location on the chip and orientation. It is very common, after dicing and mounting of the die, due to stress, the variation between identical temperature sensors on one and the same die to increase up to a few tens of degree. Another factor could be the existing internal thermal gradient, although silicon is a very good thermal conductor. For the comparator characterization we used the average value of the two integrated temperature sensors.

B. Comparator Characterization

The comparator should discriminate the input signal concerning the threshold level V_{Th} with a propagation delay of $t_p < 0.5$ ns. Measuring accurately sub-nanoseconds time intervals is not a trivial task which requires wide bandwidth equipment. Moreover, it is crucial to apply the trigger pulse and monitor the generated signal directly at the input and output of the comparator, respectively. However, this was not feasible in the test setup illustrated in Fig 3. The challenge was the LVDS form of the DAB trigger signals which had to be converted to single-ended form by a digital buffer. Furthermore, on the test PCB, additional blocks had to be added in the signal loop to provide isolation between the DAB and the chip. Each of the aforementioned blocks and buffers added a delay in the signal propagation path that was comparable or even larger than the delay of the comparator itself. Figure 6 shows all functional blocks on the signal propagation path.

Using the oscilloscope, the intrinsic delay of all off-chip functional blocks $t_{int} = 29.67$ ns was measured by shorting the chip inputs on the test PCB (Fig. 6) and probing the trigger signal at the output of the DAB and the end of the signal propagation path. The rising edge of the probed signal was approximately 1 ns (10 – 90 % amplitude). The same measurement was done with the chip in the signal propagation path to measure the total delay t_{total}. The delay of the on-chip blocks (LVDS Rx, digital buffer, MUX, comparator, and LVDS Tx) t_{chip} was calculated by subtracting the total and intrinsic delays:

$$t_{chip} = t_{total} - t_{int} \quad (3)$$

With the help of post-layout simulations, the delay of each of the on-chip blocks was defined. As the measured delay of the on-chip blocks was larger than the one defined by the post-layout simulations, the following expression was used to calculate the comparator delay t_p:

$$t_p|_{measurement} = \frac{t_p|_{simulation}}{t_{chip}|_{simulation}} \times t_{chip}|_{measurement} \quad (4)$$

Table 4 presents the comparator propagation delay t_p obtained through post-layout simulations and experimental qualifications as well as the associated error rate for different threshold levels V_{Th} and a fixed amplitude of the input signal, at 40°C. The propagation delay t_p rises at higher threshold levels, as the input signal was not an ideal step pulse. Nevertheless, the error rate among the simulation and measurement results was reasonable.

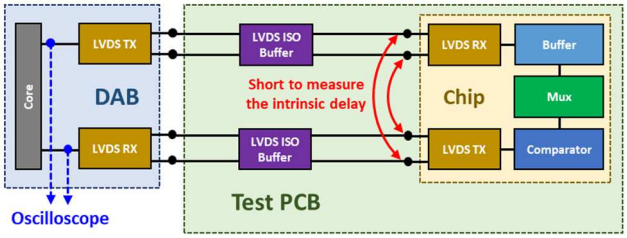

Fig. 6. Functional blocks on the signal propagation path.

TABLE 4. THE COMPARATOR PROPAGATION DELAY t_p AT 40°C

Threshold Voltage V_{Th} [mV]	Propagation Delay t_p [ps]		Error [%]
	Post-Layout	Measurement	
360	186.9	203.6	8.2
420	180.6	197.3	8.5
480	185.3	199.8	7.2
540	191.9	210.5	8.8
600	212.3	245.6	13.5
660	243.5	273.1	10.8
720	302.4	325.5	7.1
780	362.4	394.6	8.2

Figure 7 illustrates the experimentally obtained comparator propagation delay t_p as a function of the temperature for different threshold levels V_{Th}. Results indicate that the propagation delay t_p increases for higher chip temperatures.

The measured power consumption of the comparator, including the differential OTA, inverters, and the associated biasing branch, was 60 µW.

In the readout frontend, the comparator's function is to digitize the analog signals provided by the signal shaper block. The signal shaper block generates voltage signals with an amplitude of $V_{Amp} = 220.4$ mV and a width at their base of $t_{Width} = 2.91$ ns [11]. Figure 8 illustrates the measured propagation delay t_p of the comparator driven by the signal shaper block (blue line), which was the previous stage in the targeted application, as function of the threshold voltage V_{Th} at 40°C. Results indicate that the comparator can generate digital pulses with a propagation delay of less than 0.5 ns.

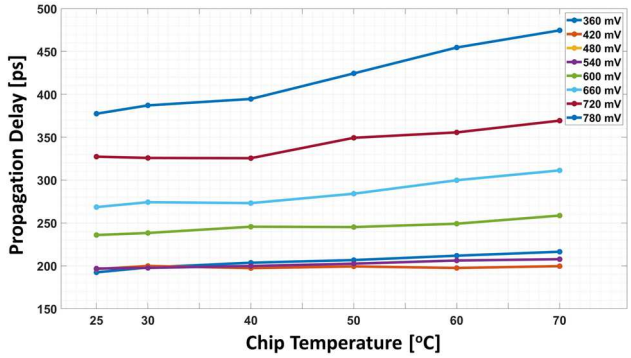

Fig. 7. Experimentally measured comparator propagation delay t_p as a function of the temperature for different threshold levels V_{Th}.

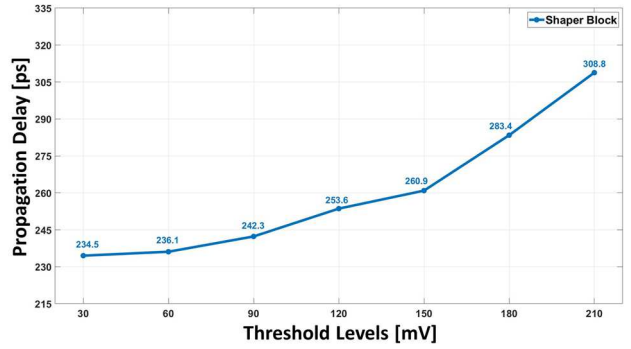

Fig. 8. Measured propagation delay t_p of the comparator driven by the signal shaper block as function of the threshold voltage V_{Th} at 40^{o}C.

V. Conclusion

The designed comparator is intended to digitize the analog signal provided by a preceding stage, labeled as the signal shaper block, in order to register the arrival time of particles landing on the detector surface. In this paper, the operation of the proposed comparator was experimentally qualified over the commercial temperature range (0 to 70 degrees Celsius) to verify its operation accuracy. High-precision lab devices and a dedicated test setup, including the heating and cooling systems, were utilized for experimental tests. Two internal BJT-based temperature sensors and an external NTC thermistor were employed to measure the chip temperature.

The comparator was driven by both ideal digital pulses and analog voltage signals provided by the signal shaper block) which is the previous stage in the targeted application. Experimental qualifications indicated that the designed comparator can discriminate the input signal concerning the threshold level V_{Th} with a propagation delay of t_p less than 0.5 ns while consuming 60 µw of power. The operation of the comparator over the commercial temperature range was verified.

References

[1] M. Nakhostin, "Pulses from Ionization Detectors," in Signal Processing for Radiation Detectors, New York: John Wiley & Sons, 2017.

[2] I. Fleck, M. Titov, C. Grupen, and I. Buvat, "Handbook of Particle Detection and Imaging," 2nd ed., Cham: Springer, 2021.

[3] I. S. McLean, "Electronic Imaging in Astronomy, Detectors and Instrumentation," 2nd ed., Berlin: Springer Praxis Books, 2008.

[4] K. Iniewski, "Medical Imaging, Principles, Detectors, and Electronics," John Wiley & Sons, 2009.

[5] J. Goldstein, D. E.Newbury, J. R. Michael, N. Ritchie, J. Scott, and D. Joy, "Scanning Electron Microscopy and X-Ray Microanalysis," 4th ed., New York: Springer, 2018.

[6] M. A. Disi, A. Mohammad Zaki, Q. Fan and S. Nihtianov, "High-count rate, low power and low noise single electron readout ASIC in 65nm CMOS technology," 2021 XXX International Scientific Conference Electronics (ET), pp. 1-5, 2021.

[7] L. Ratti, M. Manghisoni, V. Re and G. Traversi, "Discriminators in 65 nm CMOS process for high granularity, high time resolution pixel detectors," 2013 IEEE Nuclear Science Symposium and Medical Imaging Conference (2013 NSS/MIC), Seoul, Korea (South), pp. 1-6, 2013.

[8] A. Mohammad Zaki and S. Nihtianov, "Characterization Challenges of a Low Noise Charge Detection ROIC," in IEEE Transactions on Instrumentation and Measurement, vol. 71, pp. 1-8, 2022.

[9] A. Mohammad Zaki and S. Nihtianov, "High Time Resolution, Low-Noise, Power-Efficient, Charge-Sensitive Amplifier in 40 nm Technology," 2022 XXXI International Scientific Conference Electronics (ET), pp. 1-6, 2022.

[10] A. Mohammad Zaki and S. Nihtianov, "Experimental Qualification of a Low-Noise Charge-Sensitive ROIC with Very High Time Resolution," 2023 IEEE 32st International Symposium on Industrial Electronics (ISIE), Helsinki-Espoo, Finland, 2023. (Accepted for publication)

[11] A. Mohammad Zaki and S. Nihtianov, "Low-Offset Band-Pass Signal Shaper with High Time Resolution in 40nm CMOS Technology," the 49th Annual Conference of the IEEE Industrial Electronics Society, Singapore, 16–19 October 2023. (Accepted for publication)

[12] Michiel A.P. Pertijs, Johan H. Huijsing, "Precision Temperature Sensors in CMOS Technology," 1st ed., Dordrecht, The Netherlands: Springer, 2006.

[13] K. Souri, K.A.A. Makinwa, 'Energy-Efficient Smart Temperature Sensors in CMOS Technology." 1st ed., The Netherlands: Springer, 2018.