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## Exploiting Non-50 Ω Antenna Impedance and Phase-Only Quantization

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# Analysis and Design of Low-Power Receivers: Exploiting Non-50 Ω Antenna Impedance and Phase-Only Quantization

Yao Liu

# Analysis and Design of Low-Power Receivers: Exploiting Non-50 Ω Antenna Impedance and Phase-Only Quantization

Proefschrift

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*To my family*

# Summary

Reducing the power consumption of low-power short-range receivers is of critical importance for biomedical and Internet-of-Things applications. Two interesting degrees of freedom (or properties) that have not been fully exploited in the pursuit of low power consumption are the antenna impedance and the phase-only modulation property of FSK/PSK signals. This dissertation explores the possibility of reducing the power consumption of the receiver by utilizing these two degrees of freedom.

The feasibility of using a non-50 Ω antenna impedance in an active receiver front-end is first studied. A general antenna-electronics interface analysis is carried out, suggesting that power transfer is not the only design objective in the interface, but that the impedances of antenna and load need to be optimized for either voltage or current, depending on which is more favorable to measure with the electronics. This principle has been applied to a co-design example of an inductive antenna impedance and a low-noise amplifier (LNA). A passive voltage gain can be achieved by using the proposed principle, and hence the noise figure (NF) can be reduced without sacrificing power consumption.

The concept of a non-50 Ω antenna impedance is also exploited in the context of passive front-ends (PFEs). An inductive antenna impedance proves beneficial for increasing the passive voltage gain of an antenna-LNA interface. The study of the PFE aims for the same voltage-boosting effect by incorporating the inductive antenna impedance in the PFE. An analysis reveals that the inductive antenna impedance introduces two extra degrees of freedom to increase the downconverted voltage of the front-end for a given antenna available power. In order to well maintain the passive voltage gain offered by the inductive antenna impedance together with its resonant load,

the passive mixer should present a high-quality-factor capacitive input. This is achieved by incorporating an intermediate inductance in the passive network. The proposed front-end and a baseband LNA are implemented to verify the voltage-boosting effect. The implementation has a passive voltage gain of 11.6 dB, which is close to the state-of-the-art of 12 dB.

A promising concept which can fully utilize the phase-only modulation property of FSK/PSK signals is that of phase-domain analog-to-digital converters (PhADCs). This dissertation also deals with the analysis and design of PhADCs. First of all, analytical methods are proposed to comprehensively compare the PhADC and an (in-phase and quadrature) IQ ADC. Phase signal-to-noise ratio (SNR) expressions of the two ADC types are formulated analytically to facilitate a quantitative comparison of the ADCs. In comparison with the IQ ADC, the PhADC, due to its embedded demodulation attribute, is a more compact quantization and demodulation solution when interference accommodation is not required. Moreover, considering a flash ADC as an example of the low resolution (3-4 bit) IQ ADC, the PhADC has a lower theoretical energy limit than the flash IQ ADC for a given phase effective number of bits (ENOB) due to the immunity to magnitude variations and the phase-only quantization, thereby showing the great room for energy efficiency improvement that the PhADC has. Second, having discussed the interesting attributes of the PhADC, an IQ-assisted conversion algorithm and a corresponding circuit topology to improve the energy efficiency of the PhADC are proposed. Thanks to the successive approximation (SAR)-like algorithm and charge-domain operation, the prototype achieves a FoM of 1.2 pJ/step, which is better than the state-of-the-art of 8.3 pJ/step. Finally, the explicit relationship between the input amplitude SNR and the output phase SNR of the PhADC has been formulated. This relationship facilitates the system analysis of a receiver using a PhADC.

Using the proposed PFE and charge-redistribution PhADC, a receiver system is constructed. Based on the measured performance of the PFE and the PhADC, the simulated performance of a PGA and a $2^{\text{nd}}$-order filter and the analysis outcomes of the PhADC presented in Chapter 4, the benefit of using the PhADC for a receiver system is quantified. For the proposed PFE and the IEEE 802.15.6 application, two ADCs (for I and Q paths) with a SNR of 30.4 dB are

needed if an amplitude ADC is used, while a PhADC with a phase SNR of 24.5 dB (when the input amplitude is -11.9 dBm) is sufficient if a PhADC is used. For an antenna input level of -83.6 dBm (which corresponds to the minimum input level that has been specified for the PhADC), the presented receiver system demonstrates a sufficient overall SNR for the IEEE 802.15.6 standard, thereby paving the way to fully-integrated low-power receivers for the standard.

# Samenvatting

Het verminderen van het energieverbruik van laagvermogens- korte-afstands-ontvangers is van cruciaal belang voor biomedische en Internet-of-Things (IoT) toepassingen. Twee interessante vrijheidsgraden (of eigenschappen) die niet ten volle zijn benut in het streven naar een laag energieverbruik zijn de antenne-impedantie en de alleen-fase modulatie-eigenschap van FSK/PSK-signalen. Dit proefschrift onderzoekt de mogelijkheid van het verminderen van het energieverbruik van de ontvanger met behulp van deze twee graden van vrijheid.

De haalbaarheid van het gebruik van een niet-50Ω antenne-impedantie in een actief ontvanger-frontend wordt eerst bestudeerd. Een algemene antenne-elektronica koppeling-analyse wordt uitgevoerd, waarvan het resultaat suggereert dat vermogensoverdracht niet de enige ontwerp-doelstelling is in de koppeling, maar dat de impedanties van de antenne en de belasting moeten worden geoptimaliseerd voor ofwel spanning of stroom, afhankelijk van wat gunstiger te meten of aan te sturen is met de elektronica. Dit principe is toegepast op een co-ontwerp-voorbeeld van een inductieve antenne-impedantie en een ruisarme voorversterker (Engels: low-noise amplifier, LNA). Passieve spannings-versterking kan worden bereikt met behulp van het voorgestelde beginsel, en derhalve kan het ruisgetal (Engels: noise figure, NF) worden gereduceerd zonder in te boeten aan energieverbruik.

Het begrip van een niet-50 Ω antenne-impedantie is ook benut in de context van passieve front-ends (PFE's). Een inductieve antenne-impedantie blijkt gunstig voor het verhogen van de passieve spanningsversterking van een antenne-LNA koppeling. De studie van het PFE beoogt hetzelfde spanningsverhogings-effect door het opnemen van de inductieve antenne-impedantie in het PFE. Uit de analyse blijkt dat de inductieve antenne-impedantie twee extra graden van vrijheid introduceert voor het verhogen van de omlaag geconverteerde

spanning van het front-end voor een bepaald beschikbaar antennevermogen. Om de passieve spannings-versterking, aangeboden door de inductieve antenne-impedantie samen met zijn resonante belasting, goed te handhaven, dient de passieve mixer een capacitieve input met een hoge kwaliteits-factor te laten zien. Dit wordt bereikt door het opnemen van een tussenliggende inductantie in het passieve netwerk. Het voorgestelde front-end en een basisband LNA zijn geïmplementeerd om het spanningsverhogingseffect te verifiëren. De realisatie heeft een passieve spannings-versterking van 11,6 dB, hetgeen de state-of-the-art van 12 dB benadert.

Een veelbelovend concept dat volledig gebruik kan maken van de eigenschap van alleen-fase modulatie van FSK/PSK signalen is dat van fase-domein analoog-naar-digitaal-omzetters (Engels: phase-domain analog-to-digital converters, PhADCs). Dit proefschrift houdt zich ook bezig met de analyse en het ontwerp van PhADCs. Bovenal worden analysemethoden voorgesteld voor een volledige vergelijking van de PhADC en een (in-fase en kwadratuur) IQ ADC. Uitdrukkingen voor de fase-signaal-ruis-verhouding (Engels: signal-to-noise-ratio, SNR) van de twee ADC types zijn analytisch geformuleerd voor een kwantitatieve vergelijking van de ADC's. In vergelijking met de IQ ADC is de PhADC, als gevolg van de ingebouwde demodulatie-eigenschap, een compactere kwantisatie- en demodulatie-oplossing wanneer interferentie-accommodatie niet vereist is. Bovendien, bijvoorbeeld in het geval van een flits- (Engels: flash) ADC als lage-resolutie (3-4 bits) IQ ADC, heeft de PhADC een lagere theoretische energielimiet dan de flits IQ ADC voor een gegeven effectief aantal bits (Engels: effective number of bits, ENOB) van de fase, vanwege de immuniteit voor sterkte-variaties en de alleen-fase kwantisatie, waarmee de grote potentie voor verbetering van de energie-efficiëntie middels de PhADC wordt aangetoont. Ten tweede, na de interessante eigenschappen van de PhADC te hebben besproken, wordt een IQ-ondersteund conversie-algoritme en een bijbehorende circuit-topologie om de energie-efficiëntie van de PhADC te verbeteren voorgesteld. Dankzij het opeenvolgende-benaderings- (Engels: successive approximation, SAR) achtige algoritme en de werking in het ladingsdomein behaalt het prototype een maat van verdienste (Engels: figure of merit, FoM) van 1,2 pJ/conversie-stap, hetgeen beter is dan de stand van de techniek van 8,3 pJ/conversie-stap. Ten slotte wordt de expliciete relatie tussen

de ingangs-amplitude SNR en de uitgangs-fase SNR van de PhADC geformuleerd. Deze relatie vergemakkelijkt de systeemanalyse van een ontvanger die gebruik maakt van een PhADC.

Met het voorgestelde PFE en ladings-herverdelings-PhADC is een ontvanger-systeem gebouwd. Gebaseerd op de gemeten performatie van het PFE en van de PhADC, de gesimuleerde prestaties van een instelbare versterker (Engels: programmable gain amplifier, PGA) en een 2e-orde filter en de resultaten na analyse van de PhADC die beschreven in hoofdstuk 4, zijn de voordelen van de PhADC voor een ontvanger gekwantificeerd. Voor de voorgestelde PFE en de IEEE 802.15.6 toepassing zijn twee ADC's (voor het I- en het Q- pad) met een SNR van 30.4 dB nodig als een amplitude ADC wordt gebruikt, terwijl een PhADC met een fase-SNR van 24.5 dB (wanneer het ingangs-niveau -11.9 dBm is) voldoet. Voor een antenne met een ingangsniveau van -83.6 dBm (wat overeenkomt met het gedefinieerde minimum ingangsniveau voor de PhADC), toont de voorgestelde ontvanger een voldoende totale SNR voor de IEEE 802.15.6 standaard. Dit stelt de weg open tot volledig geïntegreerde ontvangers met een laag vermogensverbruik voor de standaard.

# Contents

# Chapter 1

# Introduction

The markets of wearable and implantable healthcare, fitness monitors and Internet of Things have been growing tremendously recently. Short-range radios are widely employed in these applications to connect various devices. Form factor and battery life are critical for these applications. Since the radio is often one of the most power-hungry blocks in small sensing nodes, improving the energy efficiency of the radio is of significant interest for both academic and industry communities. Reducing the power consumption of the radios can be challenging, however, as with every electronic system there is always a trade-off between power consumption and performance parameters of interest, which should be wisely dealt with to improve the energy efficiency of the radios. A low-power short-range receiver usually requires very loose specifications of sensitivity, frequency selectivity and data rate, which could be exploited in the pursuit of low overall power consumption. This principle has led to a number of low power architectural and circuit techniques that are briefly summarized below.

Owing to the low data rate requirement, simple amplitude modulation schemes such as on-off keying (OOK) and amplitude shift keying (ASK) can be used for the low-power receiver. These signals can be demodulated by an energy/envelope detector [1], a super-regenerative receiver [2–4], or an uncertain-IF receiver [5], all of which are extremely low power thanks to the absence of an accurate but power hungry frequency reference. One important challenge of the OOK/ASK low power receivers is their poor interference robustness. Several techniques such as "2-tone architecture" [6], "transmitted ref-

erence + shifted limiter" [7], and "dual-IF multi-stage N-path architecture" [8] have been proposed to enhance the interference resilience. Nevertheless, the low spectral efficiency of the OOK and ASK modulation schemes and the low data rate of the above receivers often limit their applications to a wake-up receiver, rather than the main data receiver of a receiving system. The modulation schemes employed for the main communication link are usually frequency shift keying (FSK) or phase shift keying (PSK), such as gaussian minimum shift keying (GMSK), gaussian frequency shift keying (GFSK), differential quadrature phase shift keying (DQPSK) and Offset-QPSK [9–11]. A number of efforts have been made to improve the energy efficiency of the receivers for these modulation schemes. The power consumption of the PLL and its buffers can be significantly reduced by employing an off-chip high-quality bulk acoustic wave (BAW) resonator [12], an optimum frequency translation plan (e.g., sliding-IF downconversion in [13, 14]), low-power all-digital PLL [15] and the sub-sampling technique [16, 17]. In order to achieve a compact and efficient receiver front-end, the functionalities of a low-noise amplifier (LNA), a mixer and a voltage-controlled oscillator (VCO) can be merged together as one unit and its bias current can even be shared with baseband stages [18]. Another approach to save the power of the front-end is replacing the active LNA with a passive amplification network such as a step-up transformer [19, 20] or an LC resonant matching network [21]. Also, the phase-only modulation property of the FSK/PSK signals can be utilized to implement a phase-domain analog-to-digital converter (PhADC) [20, 22] or a PLL-based receiver [23, 24]. Both the PhADC-based receiver and the PLL-based receiver simplify the standard Cartesian analog signal conditioning, exhibiting impressive energy efficiency.

However, an interesting degree of freedom that has not been fully exploited for a low-power receiver is the antenna impedance. This dissertation explores the possibility of reducing the power consumption of the receiver by utilizing this freedom. Also, the phase-only-modulation property of the FSK/PSK signals is further exercised.

# 1.1 Motivation

## 1.1.1 Non-50 Ω antenna impedance

During the design process of a wireless receiver system, the antenna and electronic circuit designers sometimes are operating independently from each other and considered to belong to separate disciplines. Both designers agree upon a common characteristic impedance of the antenna-electronics interface and subsequently optimize their part of the receiver system. The electronic circuit often requires an impedance transformation network while the antenna usually is directly matched to the characteristic impedance of a transmission line to avoid propagation effects at the interface, as shown in Fig. 1.1(a). Traditionally, this characteristic impedance is commonly assumed to be 50 Ω and the interface is impedance matched (50Ω-50Ω matching). However, it's important to note that 50 Ω is only a traditional value originally meant to offer a reasonable compromise between loss and power-handling capability for a coaxial cable with an air dielectric [25]. Also, if the length L between the antenna and the electronic circuit is electrically short ($L<\lambda/10$, $\lambda$ being the wavelength), then the propagation effects in the interface can be neglected as the voltage and current can be considered constant along the connection [26], and hence there is no fundamental reason to use a transmission line in the interface. This, for example, may be the case for integrated circuits (ICs) with on-chip antennas [27] and ICs that are close enough to an off-chip antenna [28–30], especially at low frequencies (e.g., $\lambda$ is as large as 300 mm at 1 GHz in the air). For the electrically-short interface, if the maximum power delivery is not the objective of interest, the impedance matching is no longer necessary. This opens up the possibility to directly match the antenna to the electronic circuitry as illustrated in Fig. 1.1(b). The freedom of antenna impedance could and should be fully exercised to optimize the performance of interest for a given application, rather than simply complying with the comfortable 50 Ω standard.

The reader may wonder if the above principle applies to a wireless system with more practical constraints imposed by blocks such as band-selection filters and transmitters. We make the following observations. (1) The band-selection filter is usually an off-chip component interposed between an antenna and a receiver IC, and is typically

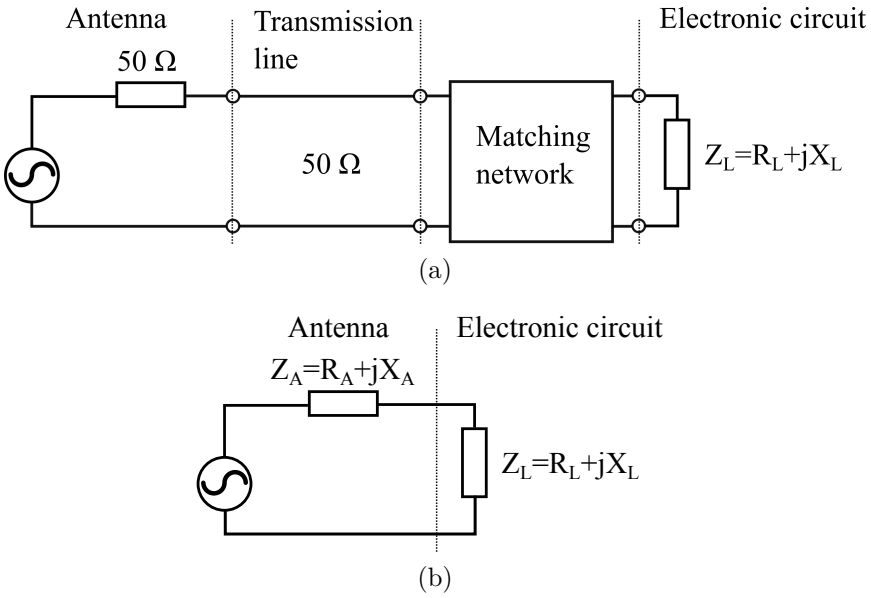



Figure 1.1: (a) Conventional 50 Ω antenna-electronics interface. (b) Electrically short antenna-electronics interface with a non-50 Ω antenna impedance.

designed for a standard 50 Ω termination. If the input or output termination deviates from 50 Ω, then the passband and stopband characteristics of the filter may exhibit loss and ripple [31]. Fortunately, for a single-band low-power short-range receiver, the off-chip band-selection filter can be omitted [24, 32], due to the relaxed frequency selectivity of standards such as Bluetooth Low Energy. Furthermore, even in the presence of the on-chip band-selection filter, the above principle still holds for the interfaces of antenna-filter and filter-circuitry respectively, although they may require more overall compromises than the antenna-circuitry interface does. (2) In a modern wireless system, a stand-alone receiver rarely exists, and hence the transmitter must also be taken into account when selecting the antenna impedance. From the transmitter point of view, it appears that the antenna impedance should contain a negligible reactive part so that it maximally radiates the signal power [31]. However, in practice, the optimum load impedance for the maximum efficiency of the transmitter heavily depends on the specifications of maximum power, supply voltage, power amplifier (PA) topology, matching network and parasitics, thereby

being unnecessarily equal to 50 Ω or any other resistive value. Thus, there is no fundamental reason for keeping a 50 Ω antenna impedance.

In Section 1.2, we address the design challenges of a receiver based on the non-50 Ω antenna impedance, as well as our objectives.

### 1.1.2 Phase-only quantization and demodulation

In a typical receiver system, downconverted FSK/PSK signals are commonly digitized by a pair of in-phase and quadrature (I and Q) amplitude ADCs (IQ ADC) before subsequent phase demodulation in the digital domain, as shown in Fig. 1.2(a). The complex IQ plane is uniformly segmented by amplitude into several discrete levels. Alternatively, modulation-specific quantization and demodulation approaches can be used by exploiting the unique properties of the modulation schemes at hand. The fact that in the FSK and PSK modulation schemes data information is encoded in the signal phase alone is utilized by a PhADC by only quantizing phase information as opposed to I and Q amplitude information, and hence the IQ plane is uniformly segmented by phase rather than amplitude, as shown in Fig. 1.2(b). Several benefits can be expected from the phase-only quantization. (1) While the IQ ADC needs subsequent digital demodulation, the PhADC embeds most of the demodulation process in the quantization, thereby saving the power and area otherwise needed for the demodulation. (2) Since phase is the only signal of interest, the power consumption of the PhADC can be considerably reduced with respect to that of the IQ ADC if they have the same energy efficiency.

A number of analysis and silicon implementations of the PhADC have been reported. PhADC-based demodulators have proven to have bit-error-rate (BER) characteristics close to an ideal coherent GFSK demodulator [33]. PhADCs based on a zero-crossing (ZC) conversion algorithm have been realized in silicon by a resistor-bridge-based approach [34, 35] as well as a current-mirror-based approach [20, 22]. The benefits of robustness to circuit nonidealities and noise and large amplitude dynamic range of the resistor-bridge-based ZC PhADC has been addressed in [36]. It is also interesting to mention the polar quantizer proposed in [37, 38]. The phase quantization path of the polar quantizer can be considered as a type of PhADC. Compared to

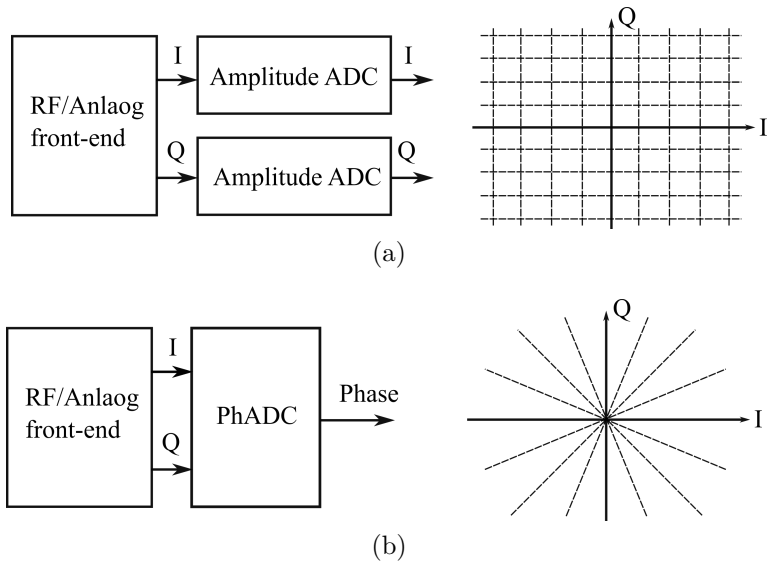



Figure 1.2: I and Q signals are digitized by (a) a pair of amplitude ADCs, and (b) a PhADC, respectively.

a traditional Cartesian quantizer, the polar quantizer can boost the signal to quantization noise ratio (SQNR) of a receiver.

In the following section, the limitations of the circuit topologies and analytical techniques presented in the above publications are examined, and hence the objectives of this dissertation can be addressed.

## 1.2 Challenges and objectives

### 1.2.1 Active and passive receiver front-ends with non-50 Ω antenna impedances

This thesis explores the feasibility of using a non-50 Ω antenna impedance for both an active and a passive receiver front-end. For the former case, the focus is on the antenna impedance and the first stage of the active front-end, which often is an LNA. Several questions arise when the design process no longer begins from the 50 Ω impedance matching. First of all, the input of an antenna is a power quantity, while the quantity of interest from the LNA point of view is usually either voltage or current. So which choice of the antenna impedance maximizes

the voltage or current for a given antenna power? Second, with both freedom of the antenna impedance and the input impedance of the LNA, how do we begin the co-design? Moreover, apart from signal, noise is also of critical importance for the LNA. Can noise metrics (e.g., noise figure (NF) ) be optimized together with signal metrics (e.g., voltage or current gain) by co-designing the antenna and the LNA? These questions are answered in Chapter 2.

A passive front-end (PFE) (or mixer-first front-end) avoids active LNAs or low-noise transconductance amplifiers (LNTAs), and active mixers, and hence can potentially reduce the power consumption of a receiver. Although the PFE features high linearity, flexible frequency programability and baseband impedance upconversion [39–42], it suffers from a tight trade-off between power consumption and noise figure (NF). This is because the NF of a passive mixer is often improved by lowering the on resistance of the switches or increasing the number of non-overlapping phases [43], which are both directly paid by a larger power consumption of the local oscillator (LO) buffers. This tight trade-off might not always be affordable for a low-power short-range receiver with a power budget of only a few milliwatts or even below one milliwatt. A passive amplification network such as a step-up transformer [19, 20] or an LC resonant matching network [21] prior to the passive mixer can effectively relax the power-NF trade-off.

The passive network is often designed under the a constraint of a 50 Ω antenna impedance, or even 50 Ω impedance matching. The concept of a non-50 Ω antenna impedance is also exploited in the context of PFEs in this thesis. We consider the topology of a direct-conversion quadrature passive mixer in this study. Owing to the time-variant and bidirectional nature of the passive mixer, the input impedance of the mixer is strongly dependent on its source impedance. Also, both the signal and noise in the passive mixer experience frequency translation, which does not occur in the LNA. These two reasons make interfacing the antenna and the passive mixer very different from co-designing the antenna and the LNA. Consequently, the questions addressed for the active front-end still hold but need to be studied and answered differently, which are presented in Chapter 3.

### 1.2.2 Phase-domain ADC

As described in Section 1.1.2, a PhADC is a promising alternative to an IQ ADC for low power wireless receivers. However, there is a lack of thorough and accurate analysis of the fundamental benefits and limitations of the PhADC over the IQ ADC in the literature. The difficulty primarily arises from the fact that the two ADCs process signals in different domains, i.e., the phase and the amplitude domain, respectively. Thus, a connection between these two domains must be established to facilitate the comparison between the two ADCs. Also, the relationship between the amplitude and phase of the PhADC is necessary for the system analysis of a receiver using the PhADC, because amplitude is a more familiar quantity for analog circuitry. Finally, the influence of amplitude nonidealities on the phase quality of the PhADC needs to be quantified as well.

From an implementation perspective, the reported PhADCs [20, 22, 33, 35] have several limitations. The principle of the conversion algorithm employed in these PhADCs is to detect the zero-crossings of rotated I and Q projections, i.e., a zero-crossing algorithm. This algorithm relies on the accurate linear combinations of I and Q signals with various scaling factors, thereby limiting the efficiency and the simplicity of the hardware implementation. Besides, the amplitude nonidealities arising from the linear combination circuitry also degrade the performance of the zero-crossing PhADCs. For example, the 4 bit resistor-bridge-based zero-crossing PhADC in [35] needs at least two power-hungry fully differential chopped operational transconductance amplifier (OTAs) to convert I and Q voltages into currents, which are subsequently converted into several phase-rotated voltages with the aid of a resistor bridge. The nonlinearities and the noise of the OTAs as well as the mismatch and the noise of the resistor bridge can introduce significant errors to the phase signal. In [20,22], similar amplitude nonidealities also occur during the voltage to current conversion in the current-mirror-based PhADC. Furthermore, both the resistor-bridge-based and the current-mirror-based PhADCs operate in a flash-like fashion, thus consuming static power in either the resistor bridge or the current mirrors. The polar quantizer proposed in [37, 38] uses a time-to-digital converter (TDC) to quantize the phase information. Though being a very interesting phase quantization technique, the

proposed TDC is very power-hungry (~7 mW), since it targets LTE applications and hence needs to operate at a speed of 40 MHz speed with a resolution of 12 bit.

In order to fulfill the potential of the PhADC mentioned in Section 1.1.2, we need to develop a new conversion algorithm which can avoid the above issues, and implement the algorithm in an efficient fashion. These are the objectives of Chapter 3.

## 1.3 Thesis organization

The remainder of this thesis is organized as follows.

Chapter 2 first presents a co-design principle for electrically-short antenna-LNA interfaces. The principle is then verified by a design example of a 900 MHz LNA using an inductive antenna impedance.

Chapter 3 presents a PFE using a non-50 Ω (inductive) antenna impedance. A passive network based on the inductive antenna impedance is proposed to provide a passive voltage gain in front of a passive mixer. Analytical methods for the desired signal transfer and noise behavior of the proposed PFE are also presented to facilitate the design. The proposed PFE together with a baseband low-noise amplifier are implemented to verify the voltage-boosting effect.

Chapter 4 deals with the analysis and design of a PhADC. Analytical methods to compare a PhADC with an IQ ADC are presented. The principal merits and drawbacks of the PhADC are then accurately formulated or addressed with the aid of several implementation examples of the PhADC and the IQ ADC. Moreover, a new conversion algorithm and a corresponding circuit implementation are proposed to improve the energy efficiency of the PhADC. Finally, the influence of amplitude nonidealities on the phase is quantified for the PhADC.

A system integration of the PFE and the PhADC is demonstrated in Chapter 5. The system aims to comply with the specifications of the 402-405 MHz band of the IEEE 802.15.6 WBAN standard.

Finally, a summary of the main contributions of this work, together with some recommendations for future work, are given in Chapter 6.

# Chapter 2

# Co-design of low-noise amplifiers and non-50 Ω antennas

## 2.1 Introduction

By designing a proper interface between the antenna and the electronics, both disciplines share a common optimization target and can agree on a non-50Ω interface impedance to optimize the overall system performance for a specific application. The choice of interface impedance plays a crucial role in the performance optimization. In this chapter, a general co-design principle is addressed, followed by a co-design example of an LNA with an inductive antenna impedance to demonstrate the benefits of the proposed principle for low power receivers.

## 2.2 Co-design principle

As addressed in Chapter 1, if an IC is directly connected to an off-chip antenna and the connection between them is electrically short, the antenna and the circuitry can be directly matched without any intermediate stages, as modeled by Fig. 2.1. An optimum choice of antenna impedance $Z_A$ and load impedance $Z_L$ allows us to increase the voltage or current at the antenna load for the same available power

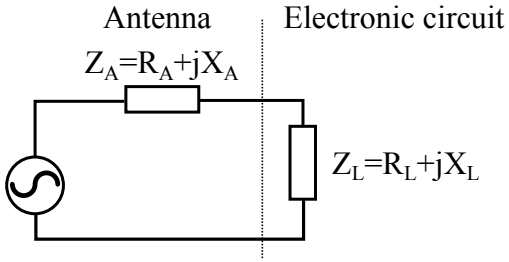



Figure 2.1: Input impedance of the electronic circuitry is directly matched to that of a non-50Ω antenna impedance.

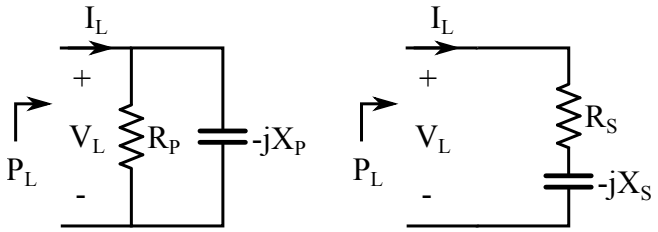



Figure 2.2: Antenna load impedance equivalent models.

at the antenna.

Optimizing the interface for maximum voltage or current is a matter of first optimizing the antenna load impedance. In many cases, the load for a given frequency range can be modeled as either a series or parallel combination of a resistance and a reactance (Fig. 2.2). Depending on preference and application, one might be more convenient to use than the other, but both provide the same characteristics. An antenna load impedance with a capacitive reactance is assumed hereafter, which holds for the majority of integrated circuits.

Without making any assumptions about the source, the power in the load can be expressed as:

$$P_L = \left(1 - |\Gamma|^2\right) P_{av} \tag{2.1}$$

where $\Gamma = \left(\mathrm{Z_L} - \mathrm{Z_A^*}\right) / \left(\mathrm{Z_L} + \mathrm{Z_A}\right)$ is the power wave reflection coefficient [26], $\mathrm{Z_A}$ is the antenna impedance, $\mathrm{Z_L}$ is the antenna load impedance and $\mathrm{P_{av}}$ denotes the power available to the antenna. The root-mean-squared (RMS) current magnitude through the load then equals:

$$|I_L| = \sqrt{\frac{2\left(1 - |\Gamma|^2\right) P_{av}}{R_S}} \tag{2.2}$$

while the RMS voltage magnitude across the load is:

$$|V_L| = \sqrt{2\left(1 - |\Gamma|^2\right) P_{av} R_P} \tag{2.3}$$

In both cases, a conjugate matched interface ($Z_A$=$Z_L^*$) produces the maximum voltage and current at a given antenna load, which is the first condition to optimize the desired signal quantity. Although this condition relates the relative impedance between the antenna and the electronic circuit, the key point is that an additional increase in voltage or current can be achieved by correctly choosing at which impedance level conjugate matching occurs.

When assuming an ideal conjugate matched interface, the RMS voltage across the parallel load terminals is given by:

$$|V_L| = \sqrt{2 P_{av} R_P} \tag{2.4}$$

The voltage across the load of the equivalent series impedance is calculated using the resistance parallel-to-series conversion equation:

$$R_P = \left(1 + Q^2\right) R_S \tag{2.5}$$

where Q=($X_S$/$R_S$)=($R_P$/$X_P$). Note that this impedance conversion is only valid around the resonance frequency. The RMS voltage in terms of the series load is then expressed as:

$$|V_L| = \sqrt{2 P_{av} R_S}\sqrt{1 + Q^2} \tag{2.6}$$

Equation (2.6) indicates that the output voltage can be 'boosted' by increasing the Q-factor of the interface. It should be noted that this also requires a larger parallel load resistance $R_P$ due to the equivalence of (2.4) and (2.6). Hence, when the available power and antenna load are fixed, one cannot increase the load voltage to higher levels by means of antenna design. The designer therefore needs to design the electronic circuit for the largest $R_P$ possible and subsequently co-design the antenna impedance for conjugate matching. This conclusion is a key point that needs to be considered during the design procedure.

The RMS load current can similarly be found by writing:

$$|I_L| = \sqrt{\frac{2P_{av}}{R_S}} \tag{2.7}$$

and hence can only be maximized by minimizing $R_S$. This is equivalent to the following expression in terms of the parallel load:

$$|I_L| = \sqrt{\frac{2P_{av}}{R_P}}\sqrt{1+Q^2} \tag{2.8}$$

Thus, the maximum voltage and current at the interface is set only by the antenna load impedance and the available power. The series and parallel load representations are tools to help the designer to analyze and find the required impedance.

The antenna impedance ($Z_A$=$R_A$+j$X_A$) is found by determining the required ratio of the resistive and reactive part of the load impedance. When considering voltage to be the signal quantity to maximize and assuming a conjugate matched interface ($X_A$=$X_S$ and $R_A$=$R_S$), Equation (2.6) can be rewritten as:

$$|V_L| = \sqrt{2P_{av}\left(\frac{R_A^2+X_A^2}{R_A}\right)} \tag{2.9}$$

Equation (2.9) is plotted in Figure 2.3 together with the Q-factor and shows the antenna load voltage as a function of antenna resistance for a given $P_{av}$ and non-zero $X_A$. Note that the voltage can be maximized by either decreasing or increasing $R_A$ and is at its minimum when $R_A$=$X_A$. Two different regions therefore can be identified, i.e., Region 1 for $R_A$<$X_A$ and Region 2 for $R_A$>$X_A$.

When assuming $R_A \ll X_A$ in Region 1, (2.9) simplifies to

$$V_L|_{R_A \ll X_A} \approx \sqrt{2P_{av}}\frac{X_A}{\sqrt{R_A}} \tag{2.10}$$

In this region, the output voltage is passively boosted by the presence of the antenna reactance, which forms an LC resonator with the load. Significant improvement for large values of Q can be achieved at the expense of bandwidth. This property is exploited in [28], where the input voltage at the RF energy harvester is effectively increased

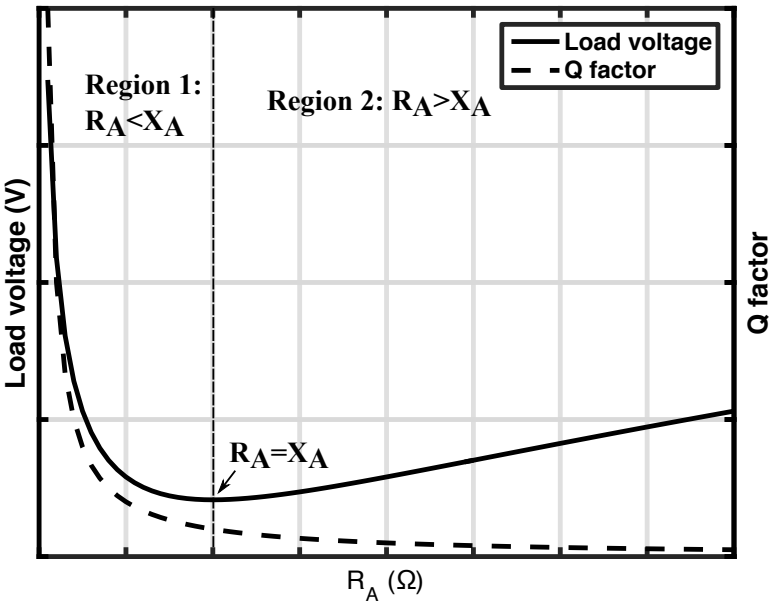



Figure 2.3: Antenna load voltage as a function of antenna resistance for non-zero antenna reactance.

using a high-Q loop antenna ($Z_A$=4.4+j328 Ω at 868 MHz). The voltage boost improves the rectifier sensitivity, meaning that a wireless sensor node with an RF energy harvester can be operated at a larger distance from the RF energy source.

When assuming $R_A \gg X_A$ in Region 2, (2.9) simplifies to

$$V_L|_{R_A \gg X_A} \approx \sqrt{2P_{av}R_A} \tag{2.11}$$

In this region, the antenna impedance can be considered to be purely resistive. The load voltage is simply determined by the resistive voltage division between the antenna and its load. But since the equivalent Thévenin antenna voltage itself depends on the antenna resistance by $V_A = \sqrt{8P_{av}R_A}$ [44] ($V_A$ is the peak value), the load voltage increases, although at a slower rate compared to Region 1. On the other hand, Region 2 has a fundamentally wideband characteristic, which can be exploited in the design of wideband LNA, where relatively large antenna resistances of 150 Ω [30] have been reported in the literature.

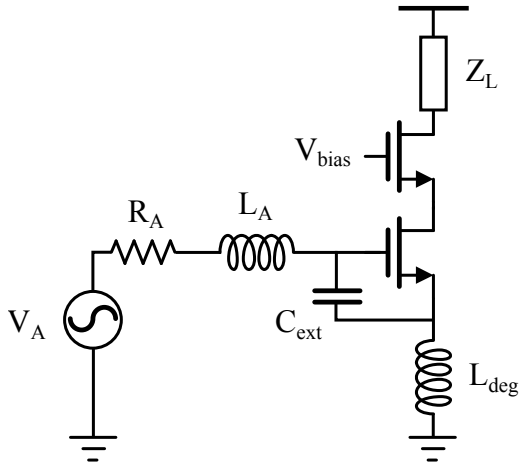



Figure 2.4: Interface model of an inductively degenerated CMOS LNA directly connected to an inductive antenna impedance including relevant noise sources.

## 2.3 A co-design example: a 900 MHz LNA with an inductive antenna impedance

The co-design of any antenna-electronics interface starts by optimizing the antenna load impedance, which in this example is a 900 MHz narrowband LNA. The well-known inductively degenerated CMOS cascode LNA topology [45] is used as it provides an easy way of adjusting the LNA input impedance. The LNA is directly connected to an inductive antenna as depicted in Fig. 2.4. The information is sensed with a CMOS gate, meaning that voltage is the preferred signal quantity to maximize.

Along with the desired signal $V_A$, the antenna picks up noise from all points within its directivity radiation pattern and thus depends on how the antenna is directed towards its environment. However, at radio frequencies it is usually assumed that the random noise of an antenna is as low or lower than the thermal noise corresponding to room temperature [46]. The antenna noise can thus be modeled as $\overline{V_{n,A}^2}$=4kTR$_A\Delta$f, where $k = 1.38 \cdot 10^{-23}$ J/K is Boltzmann's constant, T=300 K, and $\Delta$f denotes the unit bandwidth. Other relevant sources of noise are the channel noise of the transistor $\overline{i_{n,d}^2}$=4kT$\gamma$g$_m\Delta$f, the gate

resistance $\overline{v_{n,g}^2}$=4kT$\gamma$R$_g\Delta$f and the LNA load noise $\overline{i_{n,L}^2}$=4kT$\Delta$f/R$_L$. Here, g$_m$ denotes the transconductance of the MOS transistor, R$_g$ is the transistor gate resistance and R$_L$ is the equivalent thermal noise resistance of the LNA's load and subsequent stages. The coefficient $\gamma$ is often between 2/3 and 2, depending on the transistor size and the technology.

The performance of the LNA is evaluated using the Noise Factor (F), which is a measure of how much noise is relatively added by the LNA compared to the noise generated by the source. It is worth to emphasize that the noise factor therefore is defined for a specific antenna resistance and thus can be improved by co-design. A larger antenna resistance for example generates more noise, but also equally scales the desired antenna voltage as $V_A = \sqrt{8P_{av}R_A}$. The input signal-to-noise ratio (SNR) therefore does not change. However, the noise of the LNA now appears relatively smaller compared to the antenna noise, resulting in a lower noise factor and therefore better SNR at the output.

For this particular LNA implementation, the interface impedance is defined as Z$_{int}$=R$_A$+j$\omega$(L$_A$+L$_{deg}$)=R$_A$+jX$_A$ as the total inductance in the interface is the sum of the antenna and the degeneration inductors. As the narrowband LNA operates in Region 1, the antenna load voltage is thus approximated by (2.10) for large values of Q. When assuming the interface to be at the resonance frequency with conjugate matching, the minimum noise factor for low and medium frequencies is approximated as:

$$F_{min} \approx 1 + \delta\frac{R_g}{R_A} + \underbrace{\frac{R_A}{X_A^2}}_{co-design}\underbrace{\left(\frac{\gamma}{g_m} + \frac{4}{g_m^2 R_L}\right)}_{LNA} \tag{2.12}$$

Notice that the 'LNA' term in (2.12) only depends on the LNA circuit parameters and can be minimized by increasing the MOS transistor's bias current and gate area. The 'co-design' term allows to reduce the noise factor without additional power consumption by using a high-Q impedance interface. By contrast, for an LNA with the same circuit topology but a 50 $\Omega$ power-matching interface, R$_A$ and X$_A$ cannot be selected freely, and hence the noise factor can only be reduced by sacrificing power. Reducing the power consumption is the main benefit offered by the proposed co-design principle. The input-

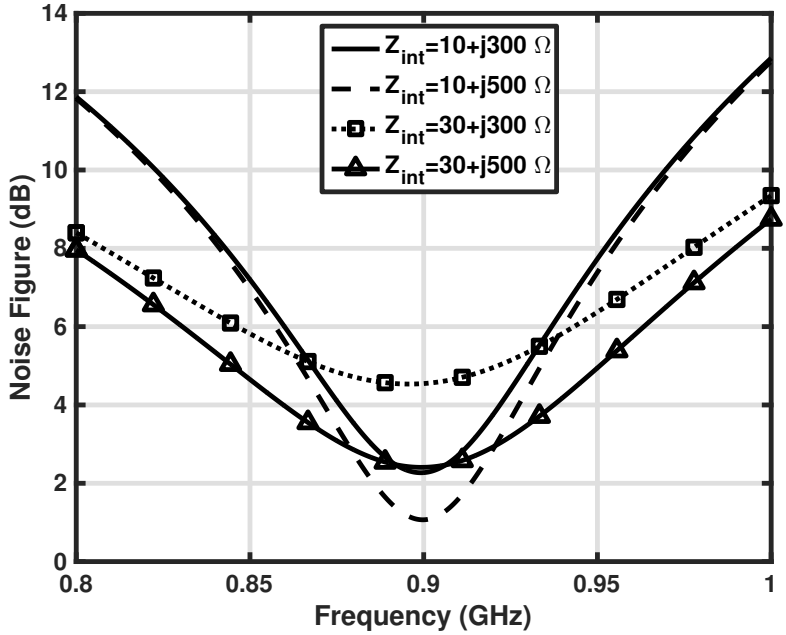



Figure 2.5: Simulated narrowband LNA noise figure for various interface impedances.

referred noise of $R_g$ is suppressed by the interface gain due to the presence of the external capacitor $C_{ext}$. This is indicated by $\delta$, which scales with $1/Q^2$ when $C_{ext} \gg C_{gs}$.

The LNA is designed in AMS 0.18 um technology and its design parameters are kept constant during the following circuit simulations ($g_m$=366 uS, $C_{gs}$=4 fF, $R_g$=18 Ω, $R_L$=10 kΩ, $\gamma$ = 1.1). The LNA input impedance is varied by tuning $L_{deg}$ and $C_{ext}$ while the antenna impedance is subsequently conjugate matched to the LNA input for each case. The inductive antenna impedance is modeled as an inductor $L_A$ in series with a power port with resistance $R_A$. The difference in noise factor is thus only determined by the difference in interface impedance. As a proof of concept, the antenna impedance and matching components are considered lossless.

The impact of the 'co-design' term can be confirmed by the simulated noise figure (NF, in dB) for various interface impedances, as shown in Fig. 2.5. Note that, in order to clearly demonstrate the impact of the interface impedance $Z_{int}$, some of $Z_{int}$ in Fig. 2.5 have a

big reactance and hence require an impractical value of $L_{deg}$ (e.g., 50 nH). In practice, the feasibility of the required $L_{deg}$ and other design constraints may result in interface impedances that are different from those in Fig. 2.5. (2.12) and Fig. 2.5 suggest that $R_A$ should be as low and $X_A$ as high as possible to reduce NF. In practice however, this will cause the antenna radiation efficiency to drop considerably when the antenna conduction loss resistance becomes comparable to $R_A$ [44]. In this case, a minimum $R_A$ should be selected during the optimization process. The LNA input however, can be designed for maximum parallel resistance (i.e., purely capacitive input impedance) and therefore would increase the load voltage by 6 dB when keeping $R_A$ fixed at the minimum value [30]. It is important to point out that a conjugate matched interface in theory would increase the voltage even further, but in this case would require a purely inductive antenna with infinitely small antenna radiation resistance and conduction loss resistance, which of course is not realizable.

## 2.4 Conclusions

In this chapter, the feasibility of using a non-50 Ω antenna impedance for an active receiver front-end is studied. A general co-design principle is first presented for electrically-short antenna-electronics interfaces. It is argued that power transfer is not the only design objective in these interfaces, but that the impedances of antenna and load need to be optimized for either voltage or current, depending on which is more favorable to measure with the electronics.

The first condition is to conjugate match the antenna-electronics interface as this maximizes both the voltage and current at the load. The second condition is to determine at which impedance level conjugate matching should occur in order to further increase the load voltage or current. This is demonstrated with a co-design example of an inductive antenna impedance and an LNA. A passive voltage gain can be achieved by using the proposed principle, and hence NF can be reduced without sacrificing power consumption. These are useful properties that can be applied to low power receivers.

# Chapter 3

# Passive receiver front-ends with non-50 Ω antennas

## 3.1 Introduction

As described in Chapter 2, an inductive antenna impedance together with a resonant interface proves beneficial for increasing the passive voltage gain into an active low-noise amplifier (LNA), and hence reducing its noise figure (NF) as well. This chapter explores the feasibility of incorporating an inductive antenna impedance in a passive receiver front-end to obtain the same voltage-boosting effect.

For the study of a passive front-end (PFE), we consider the topology of a direct-conversion quadrature passive mixer. Owing to the time-variant and bidirectional nature of a passive mixer, interfacing an inductive antenna impedance and a passive mixer proves critical and challenging. Moreover, the frequency-dependent impedances preceding the mixer complicate the analysis of voltage gain and noise of the entire front-end. This chapter proposes an interfacing technique to improve the passive voltage gain as well as NF of the front-end, which is discussed in Section 3.2. Also, the analytical methods for the voltage gain and noise behavior of the proposed topology is presented to facilitate the design.

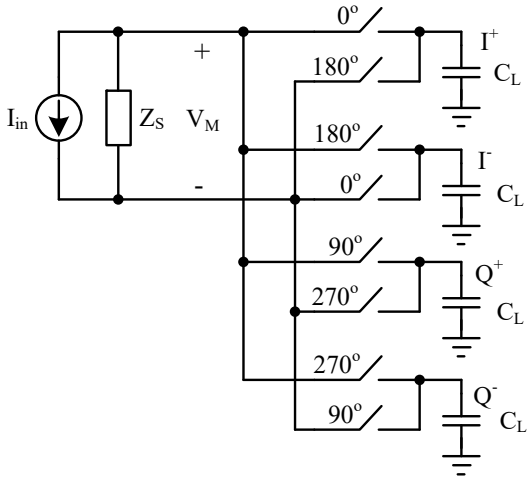
The proposed PFE together with a baseband LNA is implemented in 0.18 $\mu$m CMOS technology to verify the voltage-boosting effect. The circuit implementation details are described in Section 3.3, while the measurement results of the design are presented and compared to

prior art in Section 3.4.

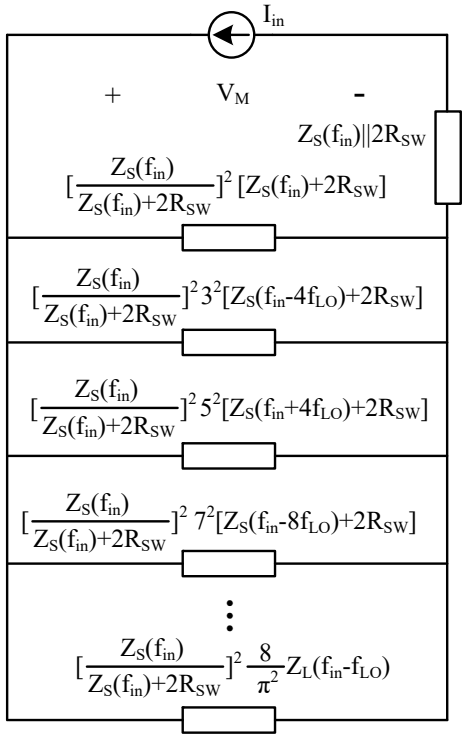
## 3.2 A passive front-end with an inductive antenna impedance

In this study, a 25% duty cycle (as opposed to 50%) quadrature passive mixer is used in the PFE due to its superior voltage gain, NF and linearity [47]. A 25% duty cycle quadrature passive mixer with an arbitrary source impedance, as shown in Fig. 3.1(a), can be modeled by the circuitry in Fig. 3.1(b) in the vicinity of switching frequency $f_{LO}$ [19]. $I_{in}$ and $Z_S$ represent the Norton equivalent of the source. $C_L$ is the baseband capacitor, $Z_L$ is its impedance, $R_{SW}$ is the on-resistance of the switches, and $f_{in}$ is the input RF frequency. This model is utilized to develop analytical methods for our proposed PFE in this section and subsequent sections.

Given an inductive antenna impedance, the simplest approach to extract the maximum voltage is loading the antenna with a resonating capacitance, which usually consists of the intrinsic capacitive input impedance of most circuits (e.g., an energy harvester or an LNA) and an extra capacitor [28, 48]. Considering a quadrature passive mixer as the load of the inductive antenna in Fig. 3.2(a), owing to its bidirectional and time-variant nature, the mixer presents rather different input properties from most linear time-invariant circuits, thereby significantly degrading the voltage gain at the interface. This can be explained with the aid of the model in Fig. 3.1(b) as follows. First, the complexity of the mixer input impedance demands a few assumptions and conditions before more insight can be given: (1) The inductive antenna is resonant with a capacitor $C_R$ at $f_{LO}$, and hence $Z_S(f_{LO})$ is a relatively high impedance. (2) If we assume $R_{SW} \ll Z_S(f_{LO})$, $(1+2R_{SW}/Z_S(f_{LO})) = 1$ and $Z_S(f_{in})||2R_{SW} = 2R_{SW}$. (3) Baseband capacitor $C_L$ presents an infinite impedance at DC. After transforming the Thevenin equivalent into its Norton counterpart as illustrated in Fig. 3.2(a), a simplified model can be given, as shown in Fig. 3.2(b). $Z_1$ is the parallel combination of $(4M+1)^2[Z_S((4M+1)f_{LO})+2R_{SW}]$ $(M \neq 0)$, where 4M+1 is the harmonic index. In order to maximize the input voltage of the mixer $V_M$, $Z_1$ must be sufficiently greater than $Z_S(f_{LO})$. While the bandpass-shaping $Z_S(f)$ presents a large value at $f_{LO}$, the




(a)




(b)

Figure 3.1: (a) A 25% duty cycle quadrature passive mixer and (b) its equivalent model in the vicinity of switching frequency $f_{LO}$ [19].

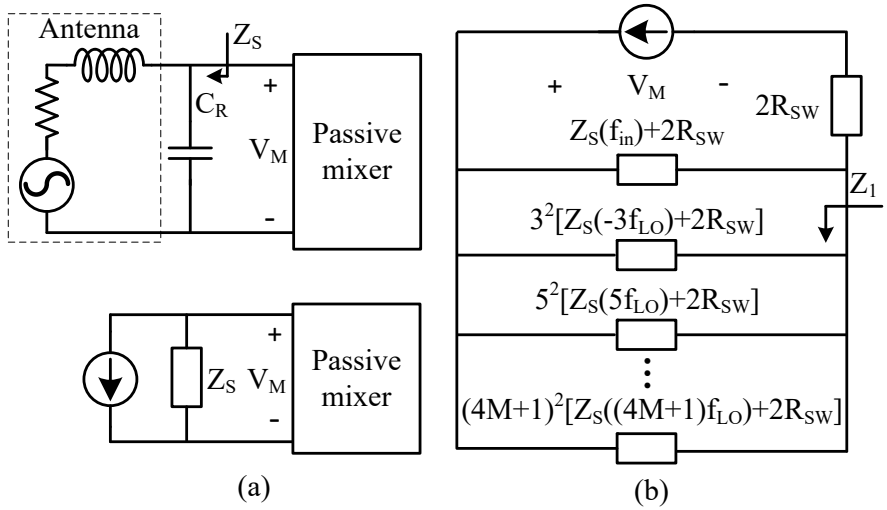



Figure 3.2: (a) A front-end consisting of a passive amplification network and a subsequent passive mixer (b) Equivalent circuit of the front-end at $f_{LO}$.

impedance decreases rapidly as the frequency moves away from $f_{LO}$ (i.e., as |M| increases). $Z_S((4M+1)f_{LO})+2R_{SW}$ is therefore dominated by the $2R_{SW}$ for large value of |M|. Thus, the overall effect of the parallel impedances results in a rather low quality factor complex $Z_1$, thereby considerably reducing the voltage gain at the interface.

The proposed PFE is shown in Fig. 3.3(a). A series inductance is inserted between the inductive antenna and the mixer to boost the source impedance at harmonics of $f_{LO}$, thereby presenting a large impedance at the mixer input and maintaining the voltage-boosting effect offered by the antenna and $C_R$. To explain this more quantitatively, the voltage gain from the antenna to the baseband output of the mixer is analyzed in this section. Furthermore, the noise behavior of the proposed PFE is also analyzed, revealing an improved NF.

### 3.2.1 Voltage gain

We first make the following assumptions:

1. The inductive antenna impedance is resonant with $C_R$ at $f_{LO}$, their impedances at $f_{LO}$ being $R_A+jX_A$and $-jX_A$, respectively.

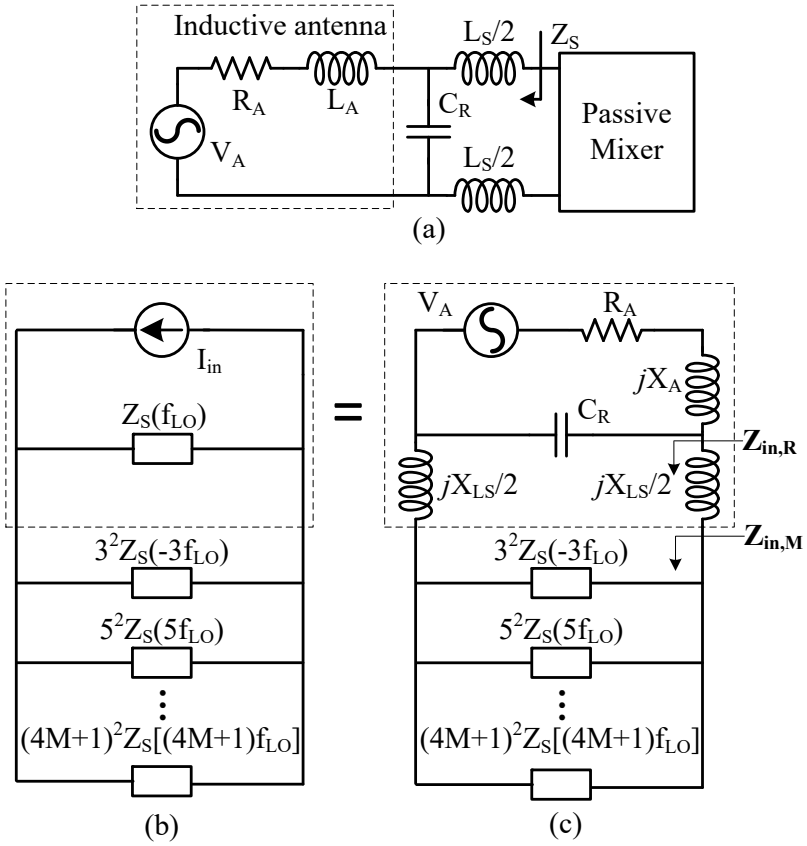



Figure 3.3: (a) Proposed PFE, (b) its equivalent model at $f_{LO}$with a Norton source, and (c) a physical source.

The quality factor of the antenna is $Q_A$=$X_A/R_A$.

2. $R_{SW}$ is assumed to be zero for now, so $(1+2R_{SW}/Z_S(f_{LO}))$ =1 and $Z_S(f_{in})||2R_{SW}$=0. Also, the voltage gain from the mixer input to the differential baseband output is simply $\sqrt{2}\pi/4$ due to the absence of the on-resistance [19]. Thus, the analysis of the voltage gain from the antenna to the baseband boils down to that of the voltage amplification at the mixer input, which is determined by the input impedance of the mixer near $f_{LO}$.

3. We focus on the voltage gain of the zero-IF product. $f_{in}$ is therefore assumed to be equal to $f_{LO}$.

4. Baseband capacitor $C_L$ presents an infinite impedance at DC.

Under these assumptions, the model in Fig. 3.1(b) can be simplified into the one shown in Fig. 3.3(b). Furthermore, $I_{in}$ and $Z_S(f_{LO})$ are transformed back into their physical model to facilitate analysis, as shown in Fig 3.3(c). The source impedance at $f_{LO}$ and its harmonics can be expressed as:

$$Z_S(Nf_{LO}) = (\frac{X_A}{Q_A} + jNX_A)||(-j\frac{X_A}{N}) + jNX_{LS}, \tag{3.1}$$

where N is the harmonics index, and $X_{LS}$ is the impedance magnitude of $L_S$ at $f_{LO}$. The impedance of this $R_A$-$L_A$-$C_R$ resonant network becomes dominated by $C_R$ as |N| increases, thus the first term in (3.1) can be approximated as $-jX_A/N$ for |N| greater or equal to 3. This also suggests that $Q_A$ has little impact on $Zs(Nf_{LO})$ for |N| greater or equal to 3. Furthermore, we can define the input impedance of the mixer at $f_{LO}$ as:

$$Z_{in,M} = \frac{1}{\sum\limits_{M=-\infty}^{\infty} \frac{1}{(4M+1)^2 Z_S[(4M+1)f_{LO}]}}, \ (M \neq 0), \tag{3.2}$$

which is a parallel combination of impedances, as shown in Fig. 3.3(c). Note that the harmonics index N in (3.1) is now replaced by 4M+1. $Z_{in,R}$ is the series combination of $Z_{in,M}$ and $jX_{LS}$. For large values of |4M+1|, impedance term $(4M+1)^2Z_S[(4M+1)f_{LO}]$ can be approximated as:

$$(4M+1)^2 Z_S[(4M+1)f_{LO}] \approx -j(4M+1)X_A + j(4M+1)^3 X_{LS}, \tag{3.3}$$

which increases approximately proportionally to $(4M+1)^3$. In contrast, in the absence of $L_S$, (3.3) is only proportional to (4M+1). More importantly, with $R_{SW}$ taken into account, (3.3) can be rewritten as:

$$(4M+1)^2 Z_S[(4M+1)f_{LO}] \approx -j(4M+1)X_A + (4M+1)^2 2R_{SW}, \tag{3.4}$$

indicating that the impedance becomes resistive as |4M+1| increases. Consequently, the total effect presented by the mixer is a low quality

factor impedance. The above observation exhibits the main benefit of $L_S$, i.e., boosting the source impedance at $f_{L0}$ harmonics and hence increasing the mixer input impedance at $f_{LO}$.

$Z_{in,M}$ can be approximated by a few impedance terms for small values of |4M+1|. We use only the terms of M=-1 and M=1 to approximate the input impedance for developing insight, then more terms will be taken into account to provide more precise results. We thus have:

$$\begin{aligned} Z_{in,M} &\approx 3^2 Z_S(-3f_{LO}) || 5^2 Z_S(5f_{LO}) \\ &= -j11.43 X_A \frac{(1-8\alpha)(26\alpha-1)}{1-69\alpha}, \end{aligned} \tag{3.5}$$

where $\alpha = X_{LS}/X_A$ is also the inductance ratio of $L_S$ and $L_A$. We make the following observations here:

1. With improper values of $X_A$ and $X_{LS}$, one of the parallel impedances in Fig. 3.3(c) could be zero (or very small). To avoid this, $3^2Z_S(-3f_{LO})$ should be capacitive, i.e., $X_{LS}>0.125X_A$. In such a condition, terms $3^2Z_S(-3f_{LO})$, $7^2Z_S(-7f_{LO})$... are all capacitive with their magnitudes increasing with harmonic index |4M+1|, while terms $5^2Z_S(5f_{LO})$, $9^2Z_S(9f_{LO})$... are all inductive with their magnitudes increasing with |4M+1|, and the total impedance $Z_{in,M}$ is capacitive.

2. $Z_{in,M}$ increases proportionally to $\alpha$ as indicated by (3.5). This can be further illustrated by the precisely calculated relationship shown in Fig. 3.4, with all of the parallel impedances shown in Fig. 3.3(c) taken into account. Also, due to the high quality nature of the source impedance, the mixer input impedance is mainly capacitive. The approximated $Z_{in,M}$ and $Z_{in,R}$ using Equation (3.5) are plotted together with the precisely-calculated counterparts of Fig. 3.3(c) in Fig. 3.4 as well, suggesting a good approximation accuracy of Equation (3.5).

As the combined capacitive impedance of $C_R$ and $Z_{in,R}$ must be resonant with $L_A$, the question arises how the total desired capacitive impedance should be partitioned between $Z_{in,R}$ and the impedance of $C_R$, i.e., $Z_{CR}=-jX_{CR}$. Since $Z_{in,R}$ is strongly dependent on the value of $L_S$, it is desirable to make $Z_{in,R}$ dominate the total impedance,

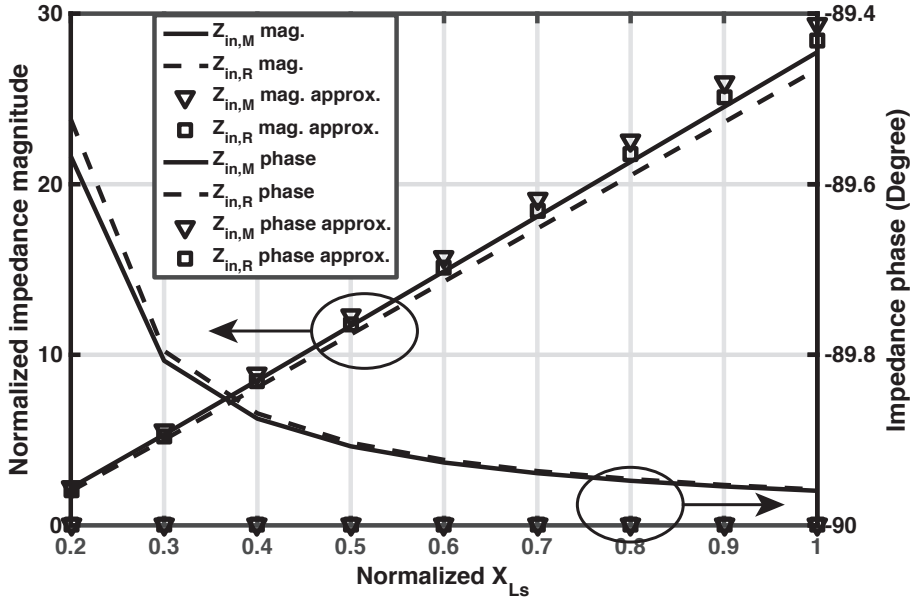



Figure 3.4: Precisely-calculated (Equation (3.2)) and approximated (Equation (3.5)) $Z_{in,M}$, as well as $Z_{in,R}$, as a function of $X_{LS}$, with all the magnitudes normalized to $X_A$. These results are approximately the same for different values of quality factor $Q_A$, though $Q_A$=10 ($R_A$=10 Ω, $X_A$=100 Ω, at 403.5 MHz) has been taken as an example. This is because $Z_S(Nf_{LO})$ has little dependence on $Q_A$ as addressed by Eq. (3.1), and hence so do $Z_{in,M}$ and $Z_{in,R}$.

thereby fully utilizing the effect of $L_S$. However, the following example shows that the strong dependence of $Z_{in,M}$ upon $Z_S$ renders this infeasible. Suppose $X_{CR}$ is much greater than $X_A$, e.g., $X_{CR}$=10$X_A$, and $L_S$=0.2$L_A$. We repeat (3.1) and (3.5), resulting in the following impedances:

$$\begin{aligned} Z_{in,R} &\approx 3^2 Z_S(-3f_{LO})||5^2 Z_S(5f_{LO}) + j0.2X_A \\ &= -X_A(3.5 - 48.2j), \end{aligned} \tag{3.6}$$

$$Z_{CR}||Z_{in,R} = (0.1 - 8.4j)X_A. \tag{3.7}$$

(3.6) suggests that $Z_{in,R}$ is a complex high impedance (magnitude is around 5 times $X_{CR}$), rather than a purely capacitive low impedance (magnitude is much smaller than $X_{CR}$) as we wished. $Z_{CR}||Z_{in,R}$ is

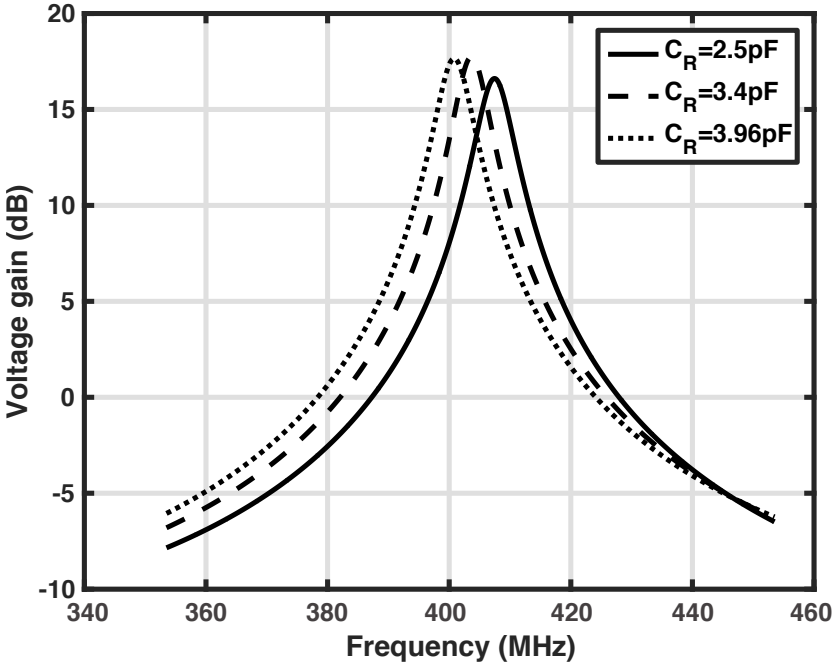



Figure 3.5: Voltage transfer function from the antenna source to the mixer input (voltage gain) in the vicinity of $f_{LO}$. Resonant frequency offset can be compensated for by tuning $C_R$. We assume the following simulation settings hereafter unless otherwise noted: $R_A$=10 Ω, $X_A$=100 Ω ($L_A$=39.6 nH), $X_{LS}$=0.5 $X_A$, $C_R$=3.4 pF, $C_L$=50 pF, $f_{LO}$=403.5 MHz, with ideal non-overlapping 25% duty-cycle quadrature signals, and the switch can switch instantaneously between on and off states with a on-resistance of $R_{SW}$=10 Ω.

therefore dominated by $X_{CR}$ as shown by (3.7), yielding an impedance much higher than the required value of $-jX_A$ for resonance at $f_{LO}$.

The above example suggests that $-jX_{CR}$ should be chosen around the desired resonance impedance $-jX_A$, and $L_S$ should be sufficient to make $Z_{in,R}$ much greater than $-jX_{CR}$. A practical method to determine the component values is as follows. (1) Choose a sufficient $L_S$ value according to Fig. 3.4. For example, $L_S$=0.5$L_A$ offers a $|Z_{in,R}|$ of 11.2$X_A$. (2) Reduce $C_R$ to compensate for the resonance frequency shift, as illustrated by Fig. 3.5.

Having developed a good understanding of the mixer's impedance at the switching frequency, we now formulate the voltage conversion

gain. $Z_{CR}||Z_{in,R}$ should be designed to resonate with the antenna impedance $R_A$+j$X_A$, as discussed above. Since $Z_{CR}||Z_{in,R}$ is a capacitive load with a negligible resistive part if $R_{SW}$ is assumed to be zero, the resonant voltage across $C_R$ is:

$$V_R = Q_A V_A. \tag{3.8}$$

Considering the impedance ratio of j$X_{LS}$ and $Z_{in,M}$, we get the voltage at the mixer's input:

$$V_{in,M} = \frac{Z_{in,M}}{Z_{in,M} + jX_{LS}} V_R. \tag{3.9}$$

As indicated by Fig. 3.4, $Z_{in,M}$ is much greater than j$X_{LS}$, i.e., the ratio $Z_{in,M}/(Z_{in,M}$+j$X_{LS})$ only varies from 1.1 to 1.04 if α varies from 0.2 to 1. So the voltage drop across $L_S$ is negligible. The voltage gain from mixer input to mixer output $V_{OUT}$ is $\sqrt{2}\pi/4$, assuming Rsw=0 [19], and hence the conversion gain from $V_A$ to $V_{OUT}$ is:

$$G = \frac{V_{OUT}}{V_A} = Q_A \frac{\sqrt{2}\pi}{4}. \tag{3.10}$$

Although voltage is a more familiar quantity, the input of an antenna is actually a power quantity. The antenna input power can be transformed into a Thevenin equivalent peak voltage as [28]:

$$V_A = \sqrt{8 R_A P_{av}}, \tag{3.11}$$

where $P_{av}$ is the available power of the antenna. Substituting (3.11) into (3.10) and expressing $Q_A$ as $X_A/R_A$, we get the mixer's output peak voltage as a function of the input power:

$$V_{OUT} = \sqrt{8 P_{av}} \frac{X_A}{\sqrt{R_A}} \frac{\sqrt{2}\pi}{4}. \tag{3.12}$$

The effect of $R_A$ on $V_{OUT}$ is a point of interest. For a given power $P_{av}$, although reducing $R_A$ decreases $V_A$, $Q_A$ is increased to a greater extent, thereby increasing $V_{OUT}$. It is also instructive to contrast (3.12) with the same quantity of a PFE with the same passive mixer but with a standard 50 Ω antenna impedance (50 Ω-based counterpart). Assuming $R_{SW}$=0, the voltage at the input of the mixer can

be calculated with the aid of the model shown in Fig. 3.1(b), yielding $V_{in,M}=8V_A/\pi^2$. Incorporating a voltage gain of $\sqrt{2}\pi/4$ from the input of the mixer to its output and (3.11), the output peak voltage is:

$$V_{OUT} = \sqrt{8 \cdot 50 P_{av}} \frac{2\sqrt{2}}{\pi}. \tag{3.13}$$

The contrast between (3.12) and (3.13) summarizes the benefits of the proposed PFE: (1) using an inductive antenna impedance, two extra degrees of freedom, i.e., $R_A$ and $X_A$ are introduced to increase $V_{OUT}$ for a given antenna available power; (2) the intermediate inductance $L_S$ increases the input impedance of the mixer considerably, thereby well maintaining the passive voltage gain offered by the passive network, i.e., $Q_A$. Considering a PFE with an antenna impedance of (10+j100) Ω, $L_S=0.5L_A$ and $R_{SW}=10$ Ω, Fig. 3.6 demonstrates that the PFE offers 12 dB higher peak RF voltage than its 50 Ω-based counterpart does for the same antenna available power. Note that the simulated 12 dB is smaller than the 14.8 dB difference between the calculated RF voltages using Equation (3.12) and (3.13) (excluding the conversion gain of $\sqrt{2}\pi/4$ from the switch input to switch output for both), which are marked as "X" in Fig. 3.6. This discrepancy primarily arises from the presence of the 10 Ω switch resistance. We elaborate on the effect of the switch resistance in the following section.

### 3.2.2 Effects of switch on-resistance

If $R_{SW}$ is assumed to be zero, $Z_{in,M}$ is almost capacitive with a very high quality factor as shown by Fig. 3.4. The presence of the on-resistance gives rise to the addition of a resistive part to each of the parallel impedances shown in Fig. 3.3(c) and Equation (3.2), thereby reducing the quality factor of $Z_{in,M}$. Consequently, the RF voltage gain offered by the passive network is reduced due to the limited quality factor of $Z_{in,M}$. Considering $R_A=10$ Ω, $L_A=39.6$ nH ($X_A=100$ Ω at 403.5 MHz), $L_S=0.5L_A$ and $C_R=3.4$ pF (to resonate at 403.5 MHz as indicated by Fig. 3.5), the calculated $Z_{in,M}$ using Equation (3.2) and the resulting $Z_{in,R}$ and $Z_{in,R}||Z_{CR}$ are shown in Table 3.1 for several $R_{SW}$ values. The quality factor of the resonance impedance $Z_{in,R}||Z_{CR}$ decreases with increasing $R_{SW}$, thereby reducing the passive voltage gain, as shown by the simulation results depicted in Fig. 3.7. Note that, as $R_{SW}$

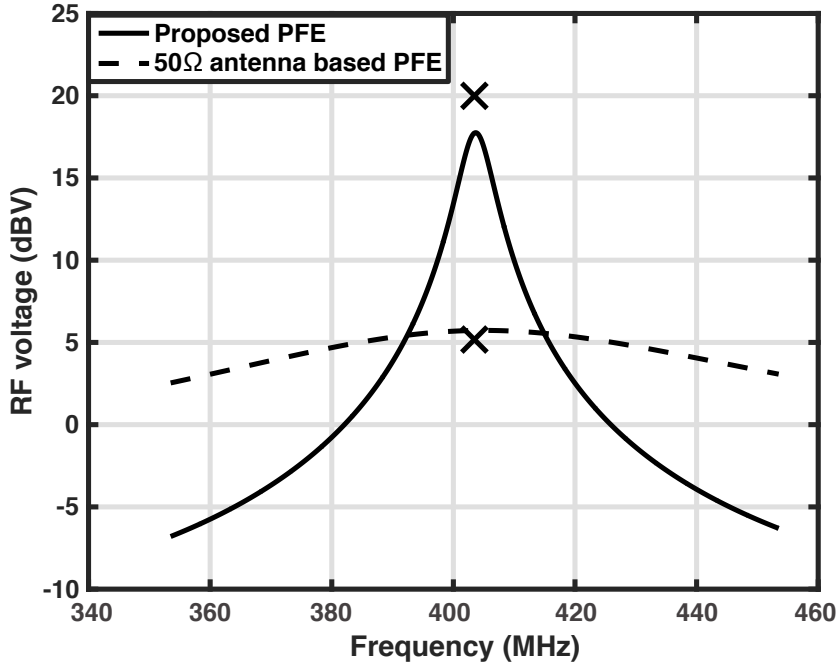



Figure 3.6: RF voltage at the mixer input of the proposed PFE and its 50 Ω-based counterpart for a given antenna available power. $P_{av}$=10.98 dBm. The approximated RF voltages using Equation (3.12) and (3.13) (excluding the conversion gain of $\sqrt{2}\pi/4$ from the switch input to switch output for both) are marked by "X".

increases, the discrepancy between the simulated gain and calculated gain shown in Fig. 3.7 increases, suggesting the model of Fig. 3.3(c) becomes less accurate. This is because the source models (dashed blocks) in Fig. 3.3(b) and (c) ignore the impedance term $Z_S(f_{in})||2R_{SW}$ (of the original model shown in Fig. 3.1(b)) due to the assumption of $R_{SW}$=0 Ω, and this impedance term becomes more pronounced as $R_{SW}$ increases, thereby causing the discrepancy. Nevertheless, the model shown in Fig. 3.3(c) incorporates the physical model of the passive network and hence is easier than the mathematical model (shown in Fig. 3.1(b)) to develop design insight.

This impact of $R_{SW}$ can be compensated for by increasing the quality factor of each parallel element in Fig. 3.3(c), i.e., increasing $L_S$. The conversion gain from the input of the mixer to its output is also reduced because of the voltage drop over the switch [19]. However,

Table 3.1: Calculated $Z_{in,M}$, $Z_{in,R}$ and $Z_{in,R}||Z_{CR}$ at LO frequency (403.5 MHz) as a function of $R_{SW}$.

| $R_{SW}$ ($\Omega$) | 10 | 20 | 40 |
|---|---|---|---|
| $Z_{in,M}(\Omega)$ | 303-j1027 | 559-j905 | 909-j590 |
| $Z_{in,R}(\Omega)$ | 303-j976 | 559-j854 | 909-j539 |
| $Z_{in,R}\|\|Z_{CR}(\Omega)$ | 3-j105 | 6-j106 | 10-j109 |

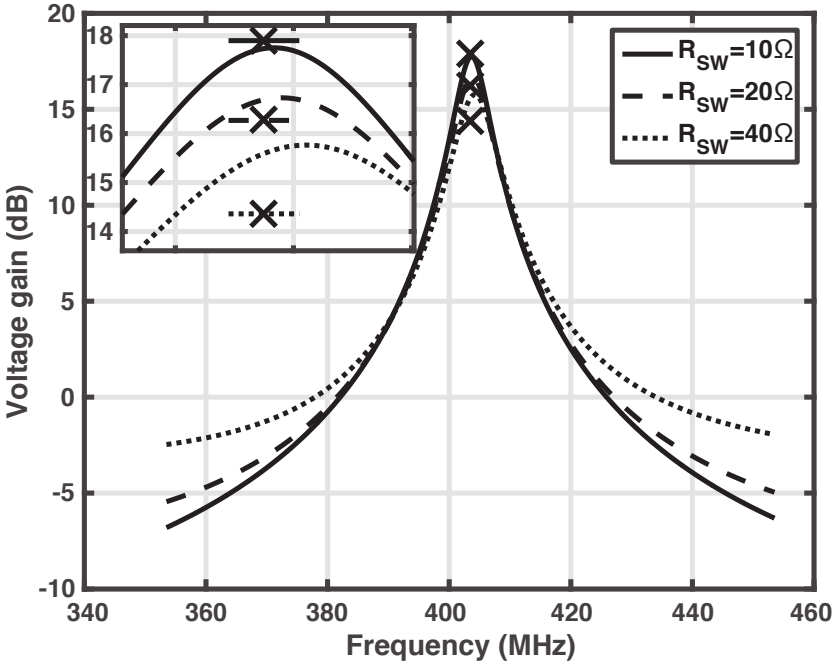



Figure 3.7: The effect of $R_{SW}$ on the peak RF gain of the proposed PFE. The calculated peak gains using the model shown in Fig. 3.3(c) and the impedances in Table 3.1 are marked by "X" and the corresponding line styles.

this effect is negligible for the proposed front-end since $Z_S$ and $Z_{in,M}$ are much greater than $R_{SW}$ in a proper design.

### 3.2.3 Bandwidth

For the same $R_{SW}$ and load capacitance $C_L$, the proposed front-end presents a narrower bandwidth with respect to its counterpart based

on a 50 Ω antenna impedance. We consider the model in Fig. 3.1(b) for comparing the two topologies. For frequencies further away from $f_{LO}$, all of the parallel terms $(4M+1)^2[Z_S(f_{in}+4Mf_{LO})+2R_{SW}]$ can be omitted because $Z_L(f_{in}\text{-}f_{LO})$ dominates. We also assume $2R_{SW} \ll Z_S(f_{in})$. Thus, in order to compare the input voltage of the mixer in the two topologies, we now only need to compare the equivalent Norton source $I_{in}(f)$ . While $I_{in}(f)$ is independent of frequency for the case of a 50 Ω antenna, $I_{in}(f)$ of the proposed topology experiences a third-order ($L_A$, $C_R$ and $L_S$) filtering when the physical model in Fig. 3.3(a) is transformed into its Norton counterpart. The proposed topology therefore offers more suppression at frequencies further away from $f_{LO}$ than the 50 Ω-based counterpart does. In other words, apart from the upconverted filtering effect of $C_L$, the bandwidth of the proposed topology is also narrowed by the passive network. The difference addressed above is also illustrated by the simulation results shown in Fig 3.6.

### 3.2.4 Noise analysis

Noise folding is the main noise degradation mechanism for a passive mixer. The proposed PFE presents interesting reduction of the noise folding effect. We analyze the noise behavior of the proposed PFE with respect to a 50 Ω based PFE. The improvement is demonstrated using a simple and qualitative approach, avoiding exhaustive analysis.

We consider the model shown in Fig. 3.8(a) for noise analysis. The input noise source and the source impedance are represented in the form of a Norton equivalent, and the switch resistance is merged with the source impedance. For an input noise current around $f_{LO}$, assume its transimpedance gain to baseband output is $A_R$. We also have that the noise around the Nth harmonic of $f_{LO}$ (N is an odd integer) folds down with a gain related to $A_R$, i.e., $A_R/N$ [19, 21]. The relative contribution of the noise folding effect (i.e., NF) can be analyzed by finding the Norton equivalent noise current $\overline{I_n^2}(f_{in})$ around the Nth harmonic of $f_{LO}$. We use the circuitry in Fig. 3.8(b) and (c) to do so for the proposed topology and its 50Ω-based counterpart, respectively. Let's consider a noise voltage source around the Nth harmonic of $f_{LO}$ ($|N|>1$), $\overline{V_n^2}(f_{in})$. The short-circuit noise current and hence the value of the Norton noise current source $\overline{I_n^2}(f_{in})$ in Fig. 3.8(c) is simply $\overline{V_n^2}(f_{in})/50^2$. In contrast, the $R_A$-$L_A$-$C_R$-$L_S$ network in Fig. 3.8 (b)

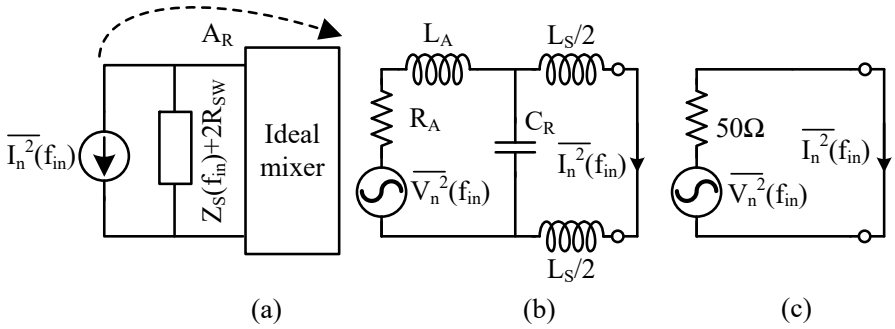



Figure 3.8: (a) Representing the input noise and switch noise as a Norton equivalent. (b) Circuitry for finding the Norton noise current source $\overline{I_n^2}(f_{in})$ of the proposed PFE, and (c) its 50 Ω-based counterpart.

provides third-order filtering, and $L_S$ has a high impedance, so $\overline{I_n^2}(f_{in})$ in Fig. 3.8 (b) is less than the one found in (c), and more importantly decreases with N. Thus, the proposed PFE significantly reduces the noise folding with respect to its 50 Ω-based counterpart, as further evidenced by the simulation results in Fig. 3.9.

The above noise analysis technique applies to switch thermal noise as well, as illustrated in Fig. 3.10. $\overline{I_n^2}(f_{in})$ in Fig. 3.10(b) is a frequency independent current which is determined by the ratio between $R_{SW}$ and 50 Ω. In contrast, since the source impedance in Fig. 3.10(a) increases with frequency, and is much greater than 50 Ω, $\overline{I_n^2}(f_{in})$ in Fig. 3.10(a) is much less than that in Fig. 3.10(b) and decreases with frequency. Hence, the thermal noise of the switch resistance can also be significantly suppressed by the proposed network in front of the mixer. This allows us to use small size switches to reduce the driving power of clock signals while retaining sufficient NF. The NF comparison of the two topologies is depicted in Fig. 3.11. Due to the reduction of noise folding, the proposed topology improves NF significantly (around 4.2 dB in the example of Fig. 3.11).

Although flicker noise contributes much less than thermal noise does in both PFEs, as shown in Fig 3.11, it appears that the flicker noise behavior of the proposed PFE is more pronounced than that of its 50 Ω-based counterpart. This could be understood with the aid of two popular explanations for the flicker noise mechanism of a passive mixer [49–51] as follows. The slowly varying gate-referred flicker

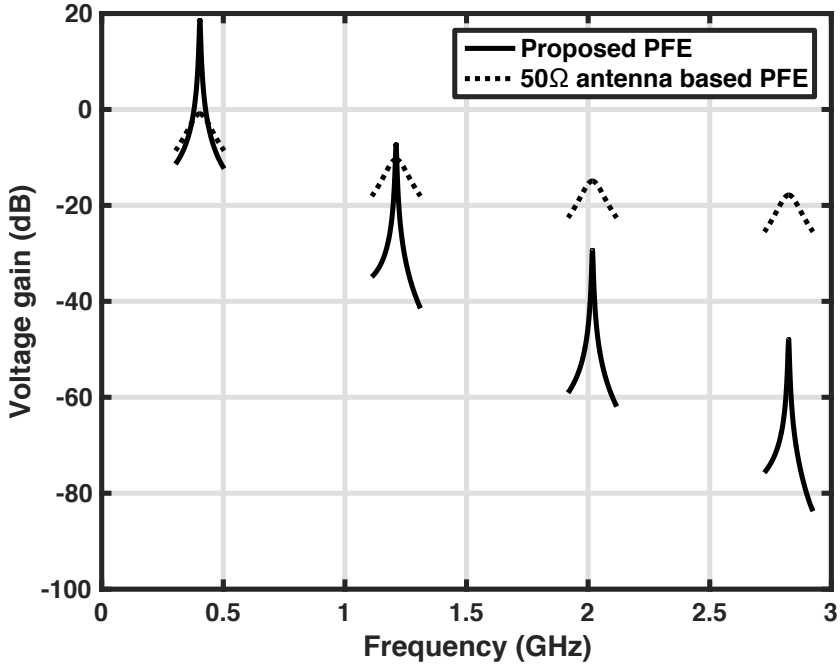



Figure 3.9: Desired signal transfer from $f_{LO}$ to baseband and unwanted foldings from $3f_{LO}$, $5f_{LO}$ and $7f_{LO}$ to baseband for the proposed PFE and its 50 Ω-based counterpart.

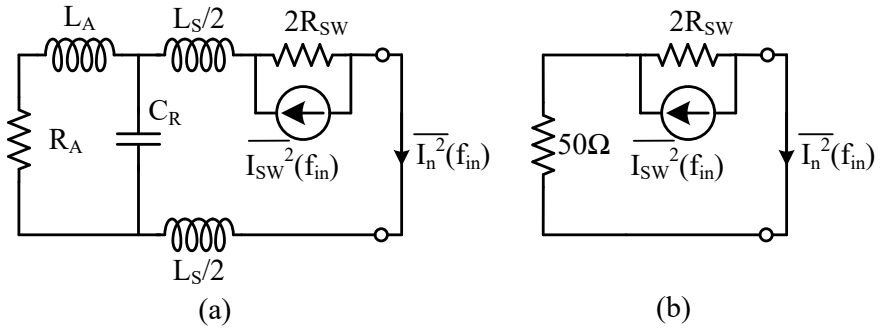



Figure 3.10: Circuitry for finding the Norton noise current source $\overline{I_n^2}(f_{in})$ of the switch thermal noise for (a) the proposed PFE, and (b) its 50 Ω-based counterpart.

noise randomly modulates the commutation instant which is ideally located at the zero crossings of the LO. This modulation results in a train of noise pulses which add to the ideal square-wave commu-

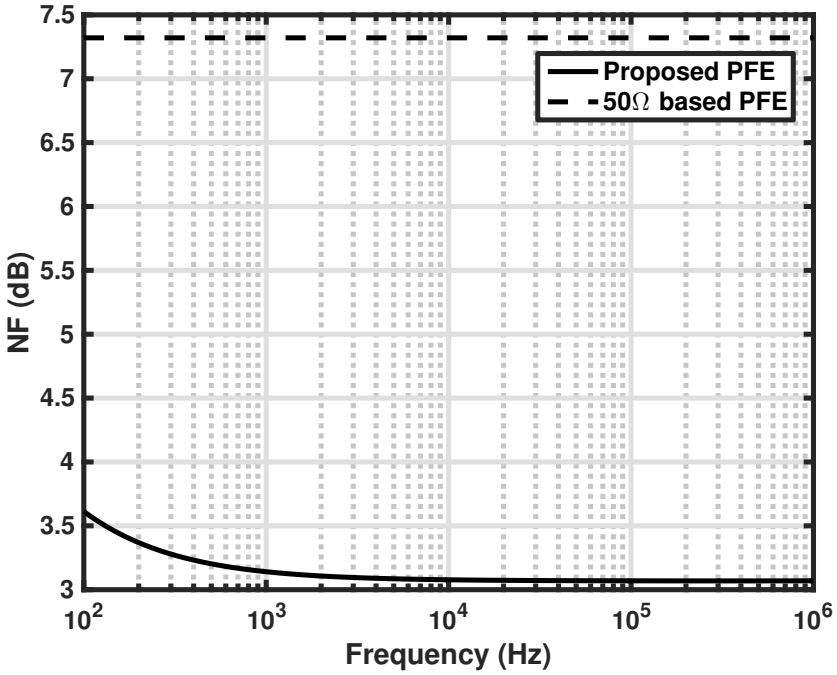



Figure 3.11: NF comparison of the proposed PFE and a 50 Ω-based PFE. The switch is implemented by a realistic MOSFET with a $R_{SW}$ around 50 Ω. The driving clock is considered to be noiseless.

tation waveform, and as a consequence, flicker noise appears at the output [49, 50]. Thus, the output flicker noise is proportional to the amount of input RF current to the passive mixer. As described in Section 3.2.1, for the same output capacitance, the proposed PFE delivers more output voltage than its 50 Ω-based counterpart, indicating that the former also has larger noise current at the input of the switches than the latter, thus more output flicker noise. Another explanation of the flicker noise mechanism is presented in [51], where the current due to the capacitive coupling of the large LO voltage to the drain nodes of the switches is said to be responsible for transferring the switch flicker noise to the output. In the proposed PFE, owing to the high impedance presented by the passive network at the drain nodes of the switches, the large LO voltage produces considerable voltage fluctuations at the drain nodes. These voltage fluctuations give rise to a non-zero-mean current in the channel of the switch, and hence the flicker noise of the switch manifests itself at the output. This effect is

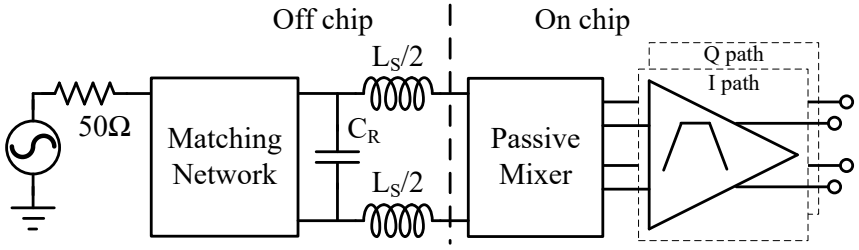



Figure 3.12: System diagram of the proposed PFE and a baseband LNA.

much less pronounced in the 50 Ω-based counterpart because 50 Ω is a very small wideband impedance in comparison with the impedance of the proposed passive network. Since the flicker noise of the mixer does not dominate the noise performance of the proposed PFE, we rely on the above two qualitative explanations to develop insight in the design process, thereby avoiding exhaustive analysis.

## 3.3 Passive front-end implementation

A direct-conversion receiver front-end is implemented to verify the results presented in the previous sections. The block diagram of the system is depicted in Fig. 3.12. An off-chip matching network transforms a standard 50 Ω source impedance into a desired inductive impedance to emulate an inductive antenna. This emulation is less accurate than a real inductive antenna, but it allows us to use standard 50 Ω-based equipment for measuring this proof-of-concept prototype. We elaborate on this point in the subsequent subsection. The passive network incorporates an extra $C_R$ and $L_S$ to offer high voltage gain to a differential quadrature 25% duty cycle passive mixer. The downconverted zero-IF signals are subsequently processed by a band-pass LNA to suppress DC offsets and to define the signal bandwidth. The prototype is designed for the 402-405 MHz frequency band of the IEEE 802.15.6 WBAN standard. The channel bandwidth is 300 kHz.

### 3.3.1 Passive network

A well-designed inductive antenna can present a quality factor as high as 74.5 ((4.4+j328) Ω) at 868 MHz [28], offering a remarkable passive voltage gain. Moreover, parasitics (of PCB tracks, ESDs, transistors, etc) can be merged with the resonant capacitance of the antenna, thereby resulting in a very compact interface and hence avoiding passive voltage gain degradation. However, the verification process of an inductive antenna-based system turns out to be complex. For example, in [28], measurements needed to be performed in an anechoic chamber to relatively well control the signal level received by the antenna. For this reason, we use a matching network to emulate the desired antenna impedance in this prototype. Limited quality factors of the employed matching network components limit the possible passive voltage gain and introduce extra noise as well. We aim for a quality factor of 10 in this design.

The impedance transformation network consists of a narrowband 50 Ω/100 Ω balun, a 12 pF capacitor and two 33 nH high quality factor inductors, as shown in Fig. 3.13. In principle, the ratio of the balun is preferably 1:1 since the 50 Ω source resistance needs to be transformed to a lower value. But a ratio of 1:2 is chosen here due to availability of the components. The 33 nH inductors have a high quality factor of 74 at 400 MHz. The transformed impedance $Z_A$ is measured and plotted in Fig. 3.14, presenting (17.4+j171.7) Ω, i.e., a Q of around 10, at 403.5 MHz. $L_S$ is chosen equal to around half of $L_A$, i.e., 30 nH, sufficiently increasing the input impedance of the mixer. The wideband property of $L_S$ is also critical since it should maintain its inductive behavior above $f_{LO}$, at least upto $3f_{LO}$ or $5f_{LO}$. The self-resonant frequency of the 15 nH inductors is 3.6 GHz, which is sufficiently high for $f_{LO}$=403.5 MHz. Owing to the strong dependence of the mixer's input impedance upon $C_R$ as addressed in Section 3.2.1, an off-chip capacitance trimmer with a tuning range of 0.65-2.5 pF is used to find an optimal value for $C_R$ during the measurement process.

ESD parasitic capacitances, as well as other off-chip and on-chip capacitances in front of the mixer input, denoted by $C_{ESD}$, prove problematic as they shunt the inductive source impedance, thereby degrading the desired impedance boosting effect. Utilizing the model shown

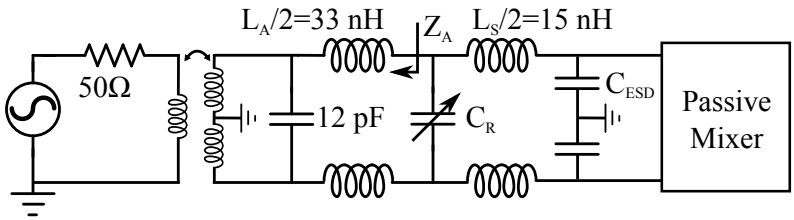



Figure 3.13: Passive network implementation.

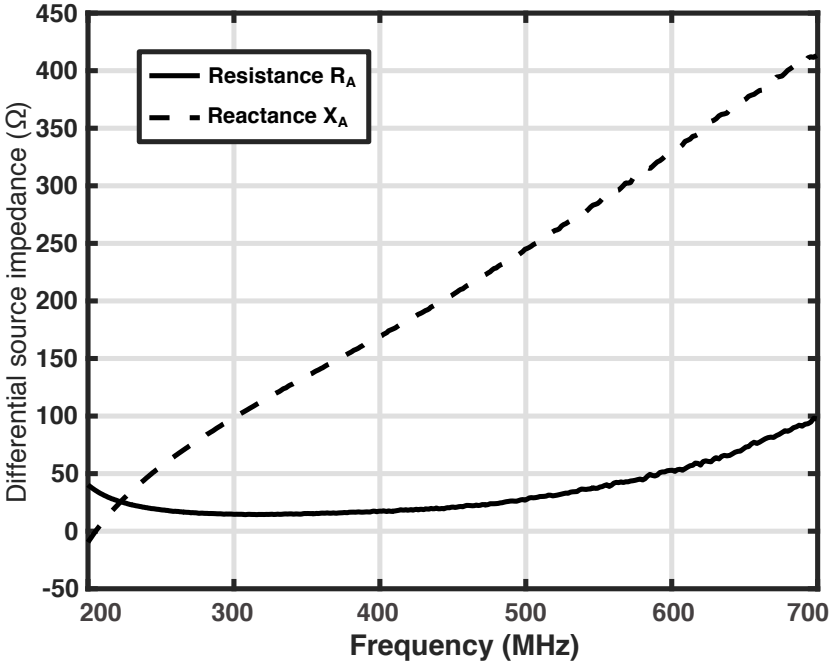



Figure 3.14: Measured output impedance of the impedance transformation network.

in Fig. 3.3(c), the effect of $C_{ESD}$ at $f_{LO}$ can be modeled as a shunt capacitance of $\pi C_{ESD}/4$, as conceptually illustrated in Fig. 3.15. The impact of this capacitance can be further understood by a numerical example as follows. For $X_A$=171.7 Ω at 403.5 MHz and $L_S$=0.5$L_A$, as a coarse approximation, the mixer input impedance $Z_{in,M}$ is equal to –j11.2$X_A$=-j1.9 kΩ as shown in Fig. 3.4. While $\pi C_{ESD}/4$ ($C_{ESD}$=218 fF) presents an impedance of –j2.3 kΩ at 403.5 MHz, the overall shunt impedance is degraded to –j1 kΩ, thereby halving the impedance boosted by $L_S$. This effect limits the improvement offered by $L_S$.

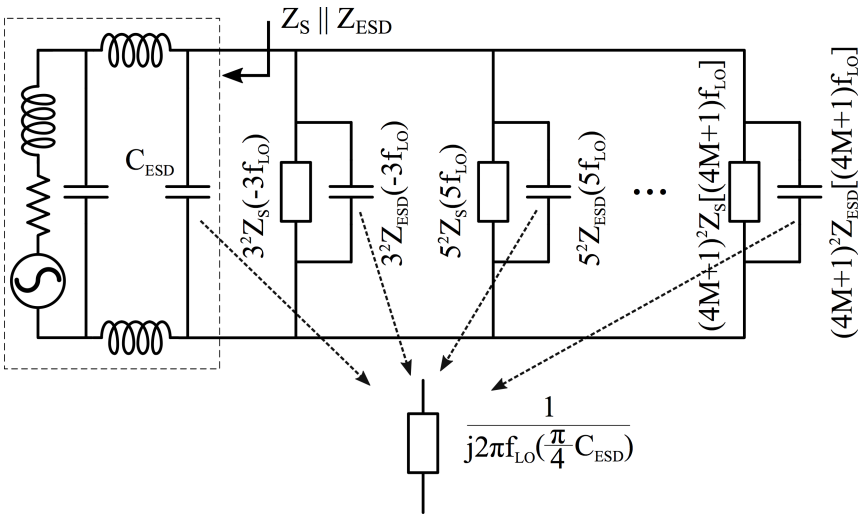



Figure 3.15: The impact of $C_{ESD}$ can be modeled as a capacitance of $\pi C_{ESD}/4$ around $f_{LO}$.

While several discrete components with large values are used for the sake of verification simplicity in this low frequency prototype, it's important to note that a fully integrated implementation is practical for higher frequencies if a real inductive antenna, e.g., the one reported by [28], is used. We elaborate on this point as follows. (1) For a real inductive antenna, the balun, the 12 pF capacitor and the 33 nH inductor shown in Fig. 3.13 can be omitted, and the antenna can be directly connected to a chip if $L_S$ is implemented on-chip. Now $C_{ESD}$ serves as a part of the desired resonant capacitance, rather than complicating the design. While the on-chip input capacitance of the mixer still causes the same impedance degradation effect, its value is much smaller than $C_{ESD}$. Consequently, the impedance boosting effect of $L_S$ can be better maintained, and hence a lower $L_S$ can be chosen for practical on-chip implementation. (2) Moving to higher frequency bands can also reduce the values of $L_A$ and $L_S$ for the same quality factor.

### 3.3.2 25% duty cycle quadrature passive mixer and clock generator

A double-balanced quadrature passive mixer driven by a 4-phase 25% duty cycle clock is implemented in 0.18 $\mu$m CMOS technology. The circuit diagram of the mixer is shown in Fig. 3.16(a). Deep N-well NMOS switches (W/L=12 um/0.18 um) are driven by a 1.2 $V_{PP}$ clock, providing an on-resistance $R_{SW}$ of 50 Ω. $R_{SW}$ appears rather big from a noise perspective but its noise folding effect can be significantly suppressed by the proposed passive network, and hence still meeting the system requirement. Consequently, the power consumption of the clock buffers can be reduced by the small size of the switches. Of course, a relatively big $R_{SW}$ may compromise the mixer's linearity, but it proves to be not a severe issue for this narrow-band low-power receiver. The drain nodes of the switches are biased by the DC feed of the balun, which is grounded to provide maximum gate-source/drain voltage swing over the switches. The source nodes of the switches are ac-coupled to a subsequent band-pass on-chip LNA. The load capacitors are MIM (metal-insulator-metal) capacitors of 20 pF.

The 4-phase clock generator is based on [40] and [52] and is shown in Fig. 3.16(b) and (c). An external $2f_{LO}$ source is converted into a differential signal via an off-chip balun and then AC-coupled to two self-biased buffers. A frequency divide-by-two loop generates a single-ended $f_{LO}$ clock, which is subsequently fed to a shift register to produce the 4-phase $f_{LO}$ clock. 25% duty cycle is obtained by ANDing the shift register's outputs with the $2f_{LO}$ clocks.

### 3.3.3 Band-pass low-noise amplifier

To reject the DC offset generated by the preceding stage, the LNA is configured as an ac-coupled band-pass filter, as shown in Fig. 3.17. The high-pass cutoff frequency $f_{HP}$ is set by $R_F$ and $C_F$ as $1/(2\pi R_F C_F)$. In order to make the inter-symbol-interference (ISI) negligible, $f_{HP}$ must be less than one-thousandth of the symbol rate [31], which is 187.5 Hz in this design. It's impractical to implement such a low $f_{HP}$ by on-chip passive devices. Thus, a pseudo-resistor [53] is employed to realize the big resistance required by $f_{HP}$, as shown in Fig. 3.17. As pseudo-resistors suffer from poor linearity, two of them are connected

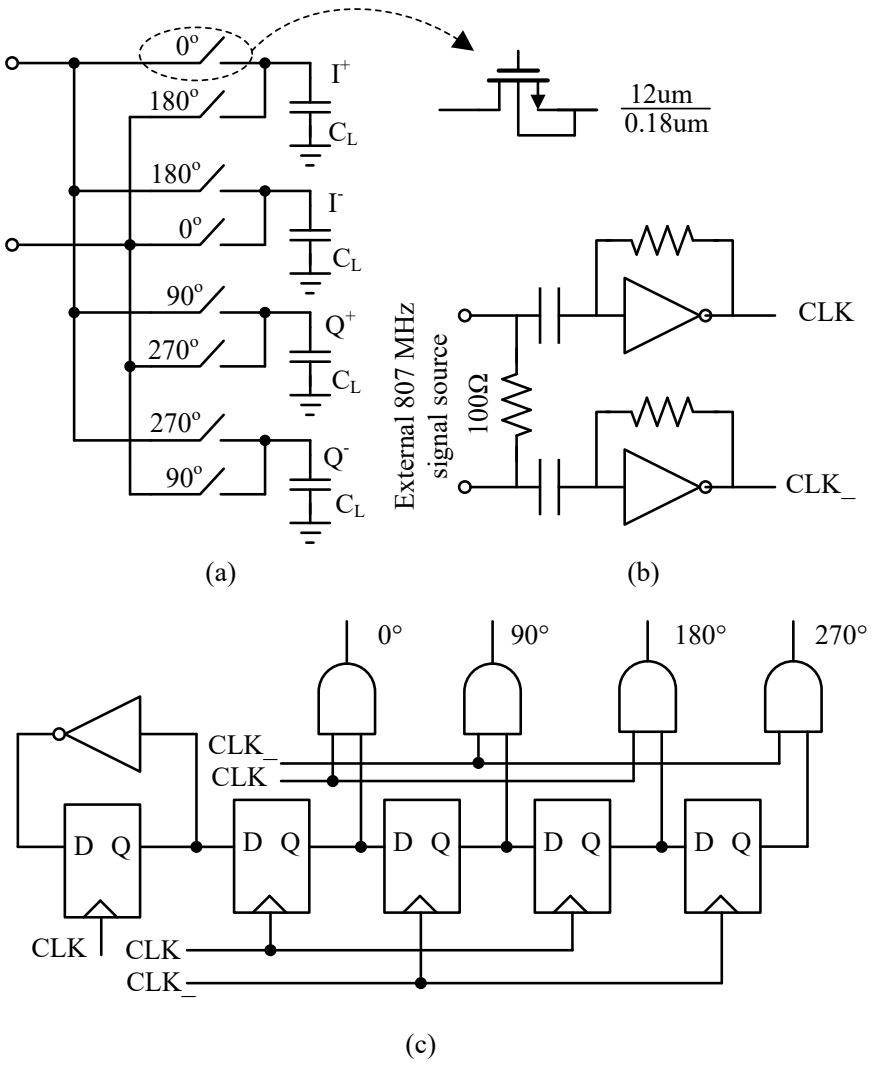



Figure 3.16: (a) 4-phase 25% duty cycle clock quadrature passive mixer. (b) Input buffer for external $2f_{LO}$ signal source. (c) 4-phase 25% duty cycle clock generator.

in series to reduce the voltage swing over the constituting transistors. Also, in practice, the nominal value of $R_F$ is much greater than what would be required for $f_{HP}$. This moves the frequency range being distorted by the the nonlinear $R_F$ below 187.5 Hz, so as to give negligible impact on signal integrity. Unavoidably, the extremely small $f_{HP}$ gives

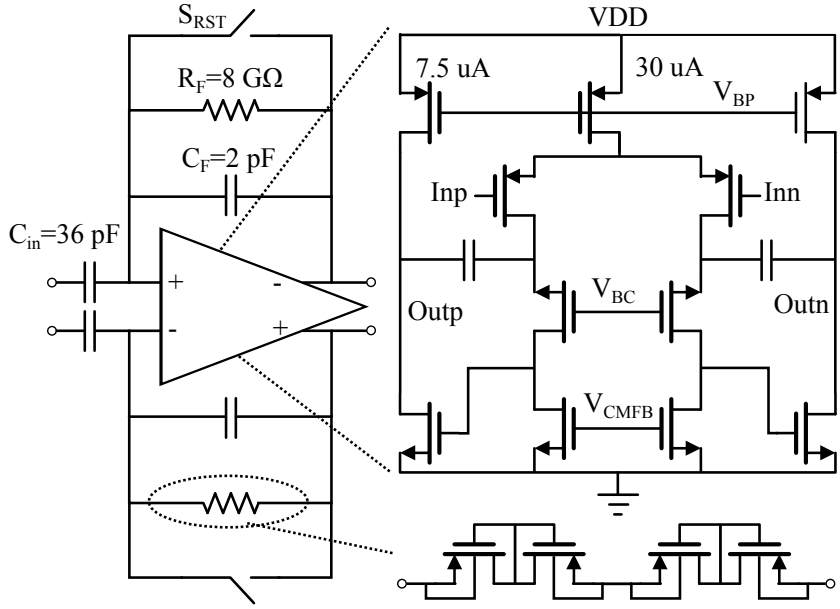



Figure 3.17: Band-pass LNA with feedback pseudo-resistors.

rise to a huge settling time constant, which is always constrained by communication standards. This issue is alleviated here by shunting the pseudo-resistor with a switch. When the amplifier is re-settling (for example, when the system is switching to another frequency channel), $S_{RST}$ is closed to help the amplifier settle rapidly. After that, $S_{RST}$ is opened to present the desired high-pass cutoff frequency. Considering the trade-off between capacitor size and the complexity of the pseudo-resistors, $R_F$ and $C_F$ are chosen equal to 8 GΩ and 2 pF, respectively, yielding a $f_{HP}$ of 10 Hz. The nonlinear $R_F$ varies from 7.65 GΩ to 8.65 GΩ over the voltage range from -250 mV to 250 mV. The passband gain is set to be 25 dB by the ratio between input capacitor $C_{in}$ and $C_F$. The low-pass cutoff frequency is designed to be around 250 kHz for a 150 kHz signal bandwidth. The amplifier in Fig. 3.17 is a fully differential two-stage low-noise amplifier with cascode compensation [54, 55]. Transistors are sized in order to optimize the noise performance of the amplifier.

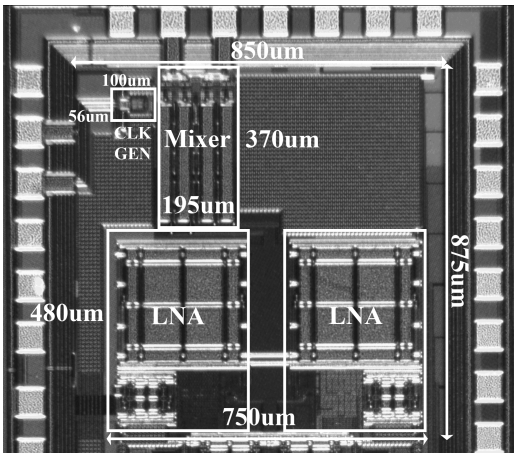



Figure 3.18: Die microphotograph.

## 3.4 Measurement results

This passive receiver front-end is fabricated in AMS 0.18 $\mu$m CMOS technology with an effective chip area of 0.75 mm$^2$. A microphotograph of the chip is shown in Fig. 3.18. The supply voltage is set to 1.2 V for all measurements. An external differential LNA serves as a differential-to-single ended buffer between the output of the on-chip LNA and external measurement equipment.

The performance targets for the passband voltage gain, passband bandwidth, NF and IIP3 are extracted from the system specifications defined in the IEEE 802.15.6 standard as follows. The channel bandwidth of the 402 MHz - 405 MHz band is 300 kHz, so the baseband bandwidth of interest for the measurement is 150 Hz - 150 kHz. The maximum input level is defined as -32 dBm, so the minimum gain is 36 dB if the signal level at the ADC's input needs to reach 4 dBm (i.e., 1 $V_{PP}$). Low-power short-range radios usually have relaxed requirements on NF and linearity. For instance, Bluetooth Low Energy can tolerate a NF as high as 19 dB for a sensitivity of -80 dBm. For this design, the modulation scheme, sensitivity, symbol rate and bit-error-rate are $\pi/4$-DQPSK, -89 dBm, 187.5 ksps and $10^{-5}$, respectively. These design targets are translated into a NF of 18.2 dB. Finally, linearity metric $IIP_3$ can be calculated for a scenario of -86 dBm desired signal and -76 dBm interference at both adjacent and alternate chan-

nels, yielding an $IIP_3$ of -58.5 dBm for a relative IM3 product of -25 dBc.

The measured downconverted voltage transfer function of the design is shown in Fig. 3.19. The passband gain is 36.6 dB, while the 3 dB high-pass cutoff and low-pass cutoff frequencies are 7.7Hz and 230 kHz, respectively. The more rapid roll-off that begins around 700 kHz arises from the limited bandwidth of the external LNA, which has a nominal value of 1 MHz. Considering the on-chip LNA has a simulated voltage gain of 25 dB, the voltage gain of the passive RF front-end is 11.6 dB. Using a source impedance that is equal to the measured impedance shown in Fig. 3.14, i.e., (17.4+j171.4) Ω at 403.5 MHz, post-layout simulations show a passive voltage gain of 12.7 dB, which consists of a -4.6 dB gain of the impedance transformation from 50 Ω to 17.4 Ω, and a subsequent 17.3 dB gain to the mixer output. The 1.1 dB discrepancy between the measured gain and the simulated gain mainly comes from the insertion loss of the off-chip balun ($< 1.5$ dB) [56]. The -4.6 dB voltage attenuation introduced by the step-down impedance transformation may raise questions over the effectiveness of using a source resistance smaller than 50 Ω. This is explained by Equation (3.12) and its subsequent description. Given that a 25% duty cycle quadrature passive mixer with a 50 Ω resistive source provides a theoretical gain of only -0.9 dB [43], the measurement confirms the enhanced gain provided by the passive network.

The output noise spectral density of the chip with a 50 Ω noise source is shown in Fig. 3.20. The input-referred integrated noise voltage over 150 Hz - 150 kHz is 3.68 p$V^2_{rms}$, yielding an integrated NF of 14.7 dB for a 50 Ω noise source. The spectrum is dominated by the flicker noise up to a frequency of approximately 5 kHz. After that, thermal noise becomes dominant and starts decreasing with frequency around 100 kHz due to the low-pass behavior of the on-chip LNA. Post-layout simulations using the measured (17.4+j171.4) Ω source impedance (at 403.5 MHz) show that the passive mixer exhibits a NF of 3.8 dB, and the equivalent integrated noise power of the on-chip LNA at its input is 30 p$V^2_{rms}$. Using the measured 11.6 dB gain, the two noise results are translated into an overall NF of 12.8 dB, which is 1.9 dB different from the measured 14.7 dB. Several effects could account for the 1.9 dB discrepancy. For example, the wideband behavior of the off-chip network could not be well modeled, and hence

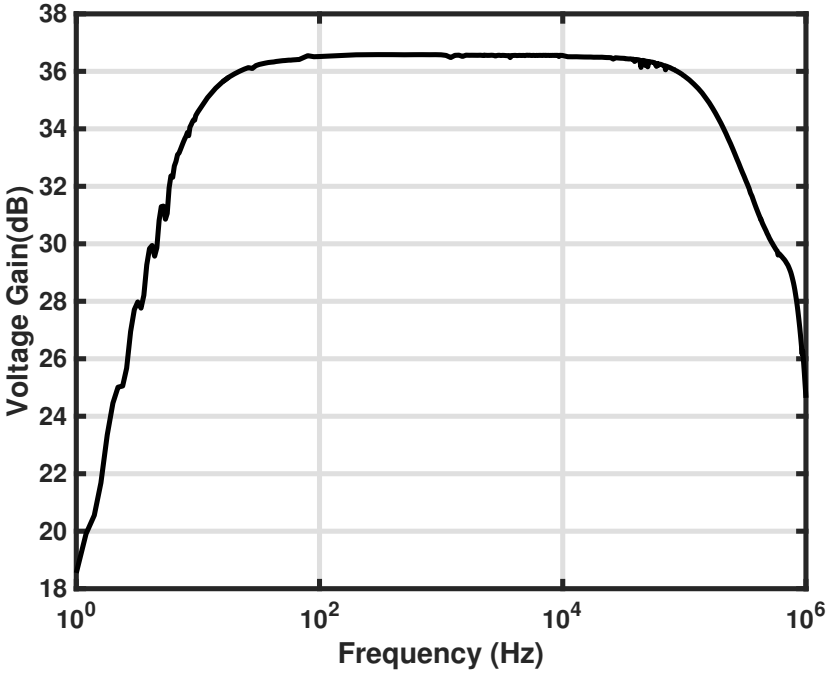



Figure 3.19: Measured downconverted frequency response from RF input to the output of the on-chip LNA.

the high-order noise folding effect may be more pronounced in practice than in the simulations. Also, the external clock, power supply, and on-chip noise coupling are all possible noise sources. However, the author could not establish the dominant noise source among these. Nevertheless, the measured NF is 3.5 dB lower than the NF target of the entire receiver chain, thereby being able to accommodate other noise sources, as well as distortion, offset, etc. The 14.7 dB NF is dominated by the noise of the on-chip LNA, rather than the passive mixer. It's actually more optimum to partition the noise budget such that the mixer dominates the overall NF since the power consumption of LO buffers can then be reduced. However, in this proof-of-concept design, it is for the consideration of reducing design risk that the noise performance of the mixer is over-designed.

Linearity metric $IIP_3$ is usually expressed as an input-referred power quantity for a 50 Ω power-matching scenario. However, the proposed passive network is not power-matched to a 50 Ω signal generator since it aims to maximize voltage gain, rather than power gain.

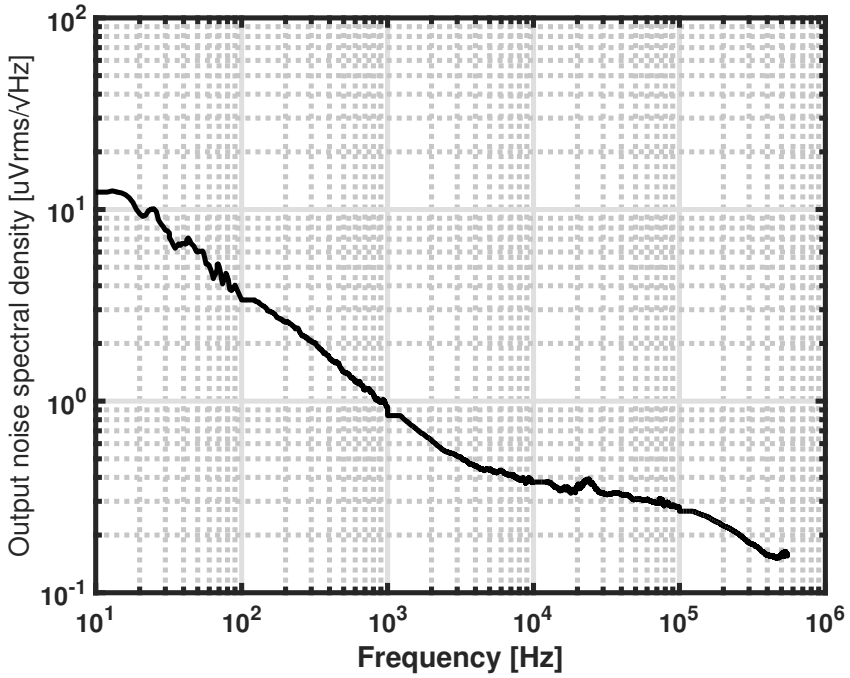



Figure 3.20: Output noise density at the on-chip LNA output for a 50 Ω noise source.

Thus, the input signal level is specified by a voltage quantity. The measured nonlinear behavior of the proposed design is shown in Fig. 3.21, indicating an in-band $IIP_3$ of 20.6 dBV. This is equal to 3.6 dBm for a 50 Ω resistance which is a more familiar way of reporting, although the translation is not rigorous. An $IIP_3$ of 3.6 dBm is much higher that the design target of -58.5 dBm, thus leaving sufficient margin for subsequent stages.

Table 3.2 summarizes the performance of the proposed PFE and that of two active front-ends and two passive front-ends. Compared with the active front-ends [57, 58], the proposed PFE has slightly higher NF (the difference $\leq$ 1.5 dB) but does not spend any power on active LNAs and mixers, and hence consumes much less overall power than the active counterparts, i.e., 1.09 mW with respect to 1.3 mW of [57] (without any LO circuitry and baseband stages) and 2.7 mW of [58]. [39] and [19] report a 25% duty cycle quadrature passive mixer with a standard 50 Ω interface and with a step-up transformer

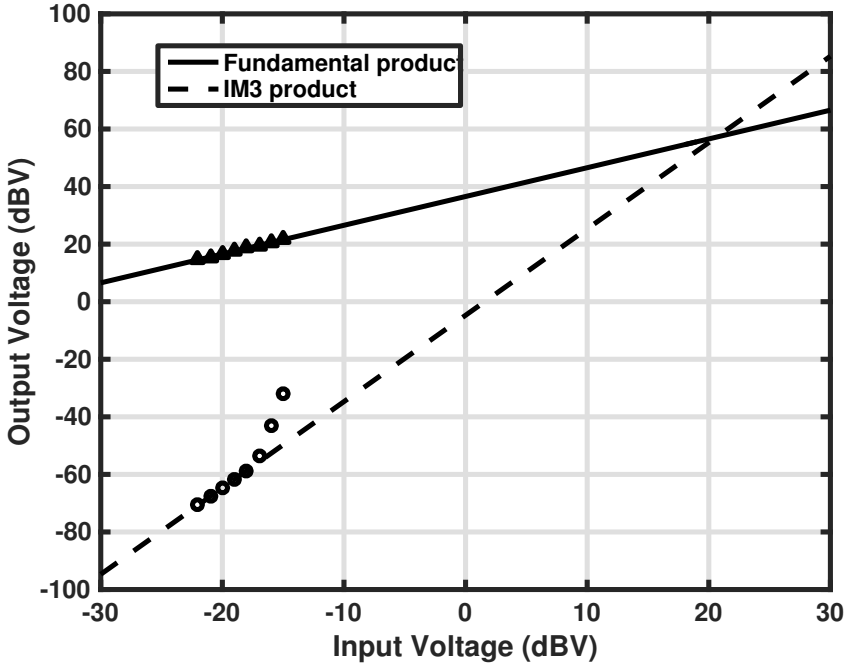



Figure 3.21: In-band $IIP_3$ measurement. Two input tones are located at 10 kHz and 20 kHz offset frequencies, respectively.

of a state-of-the-art passive voltage gain, respectively. This work has a passive voltage gain of 11.6 dB, which is close to the state-of-the-art of 12 dB [19] and much higher than the -0.9 dB theoretical limit of the 50 Ω based counterpart [39]. Despite being sufficient for the intended application, the noise performance of the proposed PFE seems much worse than that of [39] and [19]. However, it is important to note that the 14.7 dB NF is dominated by the baseband LNA in this prototype as described previously, and the simulated NF of the mixer alone is only 3.8 dB. Thus, the proposed passive network provides a state-of-the-art passive voltage gain and the gain can effectively improve the NF of the mixer. The 14.7 dB NF can be considerably reduced by increasing the power consumption of the baseband LNA, which is much smaller than that of the LO circuitry in the intended low-data-rate and low-bandwidth application. Although this work consumes less power than the works in [39] and [19] do, it might not be a fair way to compare with their energy efficiency, because of the very different LO frequencies, technologies, baseband bandwidth and applications. Con-

Table 3.2: Performance comparison.

| | TCAS-I '15[57][1] | TCAS-I '13[58][2] | ISSCC '09[39][3] | JSSC '15[19][4] | This work[3] |
|---|---|---|---|---|---|
| | Active front-end | | Passive front-end | | |
| Source | 50Ω | 50Ω | 50Ω | 50Ω | Inductive |
| Technology (nm) | 180 | 130 | 65 | 65 | 180 |
| Frequency (GHz) | 0.402-0.405 | 0.402-0.405 | 0.2-2.0 | 5.1-5.9 | 0.402-0.405 |
| BW of downconv. sig. (MHz) | 0.3 | 0.3 | 25 | 10 | 0.23 |
| RF+Mixer voltage gain (dB) | 25.7 | 31 | -0.9[5] | 12 | 11.6 |
| $R_{SW}$ (Ω) | | | 5 | 57 | 50 |
| NF (dB) | 13.2 | 13.6 | 6.5 | 5.3 | 14.7 |
| In-band $IIP_3$ (dBm) | -17[6] | 3 | 11 | 2.6 | 3.6 |
| Power (mW) | 1.3 | 2.7 | 67 | 11.6 | 1.09 |
| LNA | 0.94 | N.A. | | | |
| Mixer | 0.36 | 0 | N.A. | 0 | 0 |
| 25% LO Gen + LO buffers | | N.A. | N.A. | 1.2+0.4 =1.6 | 0.93 |
| Baseband stages | | N.A. | N.A. | 10 | 0.16 |
| Supply voltage (V) | 1.8 | 1.2 | 1.2 | 1 | 1.2 |
| Area/Active core ($mm^2$) | 1.6/N.A. | N.A./0.12 | N.A./0.13 | N.A./0.183 | 0.75/0.44 |
| Off-chip passive network | No | No | No | No | Yes |

1: Active LNA + active mixer.
2: Active LNA + passive mixer + one baseband stage + LO generator + LO buffers.
3: Passive front-end + one baseband stage + 25% LO generator + LO buffers.
4: Passive front-end + two baseband stages + 25% LO generator + LO buffers.
5: Theoretical limit for a 50Ω based passive mixer [43]. The reported gain is 19 dB including that of a baseband amplifier.
6: Calculated from the reported $P_{1dB}$ of -26.6 dBm by $IIP_3=P_{1dB}+9.6$ (dB).

sidering the power consumption of LO circuitry is heavily dependent on the switch size, comparing the required switch resistance of the three PFEs could be a better approach, which suggests that this work is more or less as efficient as [19]. The price paid for the benefits of the proposed architecture is the bulky off-chip passive network. However, as discussed in Section 3.3.1, the off-chip implementation is chosen for the sake of verification simplicity in this low-frequency prototype, and a fully integrated implementation (excluding the inductive antenna) is also practical.

## 3.5 Conclusions

This chapter proposes a passive receiver front-end that uses an inductive antenna impedance. The inductive antenna impedance introduces two extra degrees of freedom, i.e., resistance $R_A$ and inductance $L_A$, to increase the downconverted voltage of the front-end for a given antenna available power. The intermediate inductance $L_S$ of the front-

end increases the input impedance of the mixer considerably, thereby well maintaining the passive gain offered by the inductive impedance together with its resonant load. The proposed front-end and a base-band low-noise amplifier have been implemented to verify the voltage-boosting effect. The implementation has a passive gain of 11.6 dB, which is close to the state-of-the-art of 12 dB.

# Chapter 4

# Phase-domain ADCs

## 4.1 Introduction

In this chapter, analytical methods to compare a phase-domain (PhADC) and a pair of in-phase and quadrature ADCs (IQ ADC) are presented, aiming to provide deeper insight into their performance and to help designers make an optimum choice between them at system level. Phase signal-to-noise ratio (SNR) is proposed to facilitate the comparison of the PhADC and the IQ ADC. The phase signal-to-quantization-noise ratio (SQNR) is analytically related to the resolutions in phase and amplitude for the PhADC and the IQ ADC, respectively. The principal merits and drawbacks of the PhADC are then accurately formulated or addressed with the aid of several implementation examples of the PhADC and the IQ ADC.

After developing a good understanding of PhADCs, in Section 4.4, a new conversion algorithm and a corresponding circuit implementation are proposed to improve the energy efficiency of the PhADC. As addressed in Chapter 1, the reported PhADCs [20, 22, 33, 35] suffer from several limitations arising from the zero-crossing (ZC) algorithm used by them. An IQ-assisted conversion algorithm is presented to fundamentally avoid the accurate linear combination operation imposed by the zero-crossing algorithm. A charge-redistribution PhADC is demonstrated as an energy efficient implementation of the proposed algorithm.

Finally, the influence of amplitude nonidealities on the phase is quantified for the PhADC and compared with the IQ ADC where

necessary. It should be noted that although the analysis in Section 4.2, 4.3 and 4.5 are made for a ZC PhADC, most of this analysis still holds for a charge-redistribution PhADC. We hereafter assume the PhADC is a ZC PhADC in the following analysis sections unless otherwise noted.

## 4.2 Phase SQNR of IQ ADC and PhADC

### 4.2.1 IQ ADC

Analog baseband frequency/phase modulated I and Q signals are usually quantized by an IQ ADC, and then mapped onto phases in the digital domain during or before the phase demodulation. While the I and Q amplitude ADCs are characterized in the amplitude domain separately, it is more meaningful to characterize them together in the phase domain since eventually the phase is the only quantity processed by the phase demodulator. Therefore, the phase quantization noise introduced by the IQ amplitude quantization noise is analyzed here.

The phase quantization noise can be accurately formulated by a mathematical procedure as follows. Assuming the I amplitude quantization noise is uncorrelated with the I signal and so is its Q counterpart, the amplitude of the quantization noise are approximately uniformly distributed and spread more or less as white noise over the Nyquist bandwidth from dc to $f_s/2$ [59], where $f_s$ is the sampling frequency. The phase quantization noise then becomes:

$$e(i, q, \Delta i, \Delta q) = \arctan \frac{q + \Delta q}{i + \Delta i} - \arctan \frac{q}{i}, \tag{4.1}$$

where $i$ and $q$ are the amplitudes of the I and Q signals, and $\Delta i$ and $\Delta q$ are the quantization noise terms superposed on them, respectively. The power of the phase error is given by [60]:

$$P_{\varphi,QN} = \iiiint e(i, q, \Delta i, \Delta q)^2 \cdot f(\Delta i, \Delta q) \cdot d\Delta i \cdot d\Delta q \cdot di \cdot dq, \tag{4.2}$$

where $f(\Delta i, \Delta q)$ is the joint distribution density function of $\Delta q$ and $\Delta i$, which both have a uniform probability density function (PDF). However, since the integration result of (4.2) is complicated and it

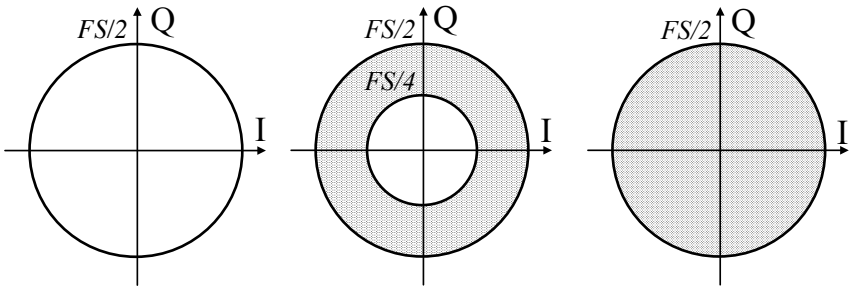



Figure 4.1: Vector distribution with random phase and (a) constant magnitude, (b) random magnitude within [$FS/4$, $FS/2$], and (c) random magnitude within [0, $FS/2$].

does not provide any intuitive insight, a simulation-based approach is employed here instead. Moreover, the phase quantization noise power is highly dependent on the distribution of the vector magnitudes. Two scenarios with different vector magnitude distributions are analyzed, i.e., a constant magnitude distribution and a random magnitude distribution within a certain range.

#### 4.2.1.1 Constant vector magnitude

A vector signal (i.e., a pair of I and Q signals) with constant magnitude $FS/2$ but random phase as shown in Fig. 4.1(a), is applied to an $N_{\mathrm{IQ}}$ bit IQ ADC with an amplitude least significant bit $\mathrm{LSB}_{\mathrm{IQ}}$. Following the quantization process of $i$ and $q$, the quantized amplitudes are converted into a quantized phase $\varphi_{\mathrm{IQ}}$. While amplitude quantization noise terms $\Delta q$ and $\Delta i$ are uniformly distributed over [$-\mathrm{LSB}_{\mathrm{IQ}}/2$, $\mathrm{LSB}_{\mathrm{IQ}}/2$], the phase quantization noise $e_{\varphi,\mathrm{IQ}}$ introduced by $\Delta q$ and $\Delta i$ is not distributed in the same way due to the nonlinear amplitude-to-phase conversion as indicated by (4.1). This indeed can be observed in Fig. 4.2(a), which plots the PDF of the phase quantization noise when the input signal has constant magnitude but random phase. It is also confirmed by simulations that the phase quantization noise PDF is uncorrelated with the input phase when the input phase spans the entire phase range, i.e., [0, $2\pi$).

The SQNR of output phase $\varphi_{\mathrm{IQ}}$ can now be calculated assuming

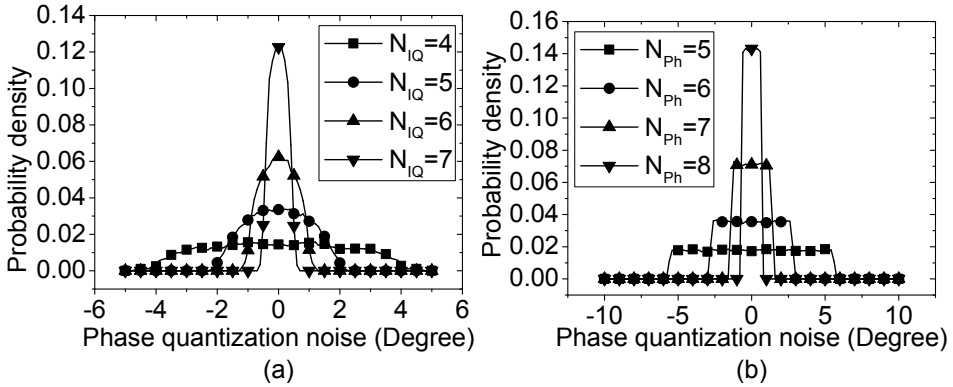



Figure 4.2: Phase quantization noise PDF of (a) an IQ ADC for $N_{\rm IQ} =$ 4, 5, 6, or 7 and a constant input vector magnitude, and (b) a PhADC for $N_{\rm Ph} = 5,\ 6,\ 7,$ or 8 and a constant input vector magnitude.

input phase $\varphi_{\rm IQ,in}$ is a full-scale sinewave:

$$\varphi_{\rm IQ,in} = \pi \sin(2\pi f t). \tag{4.3}$$

The rms value of the input phase is therefore:

$$\varphi_{\rm IQ,in,rms} = \frac{\pi}{\sqrt{2}}. \tag{4.4}$$

The phase SQNR for an ideal $N_{\rm IQ}$ bit IQ ADC is therefore:

$$\text{SQNR}_{\varphi,\rm IQ} = 20 \log_{10} \frac{\varphi_{\rm IQ,in,rms}}{e_{\varphi,\rm IQ,rms}} \,(\text{dB}), \tag{4.5}$$

where $e_{\varphi,\rm IQ,rms}$ is the rms value of the phase quantization noise, which can be determined by simulations. As shown by the upper curve in Fig. 4.3(a), $\text{SQNR}_{\varphi,\rm IQ}$ linearly increases with $N_{\rm IQ}$, which can be fitted to a linear function as:

$$\text{SQNR}_{\varphi,\rm IQ} = 6N_{\rm IQ} + 11.9\,(\text{dB}). \tag{4.6}$$

The SQNR of an amplitude ADC is usually quantified by a more intuitive metric, i.e., effective number of bits (ENOB) according to:

$$\text{ENOB} = \frac{\text{SQNR}\,(\text{dB}) - 1.76}{6.02}. \tag{4.7}$$

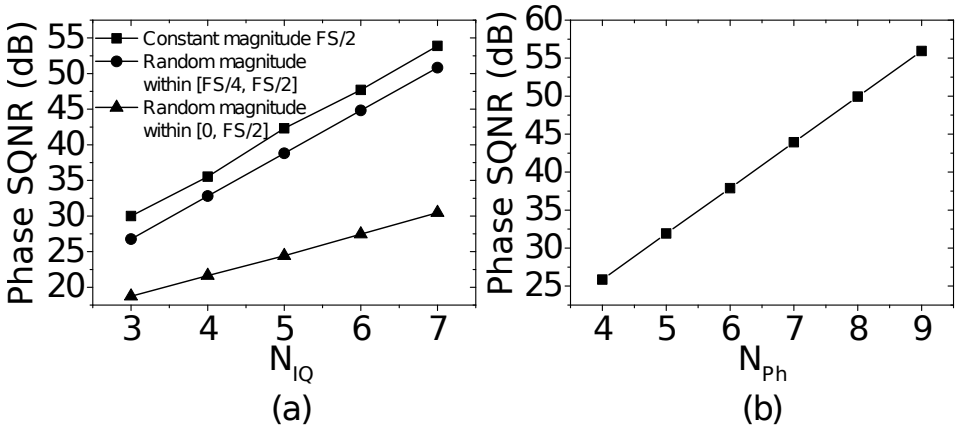



Figure 4.3: (a) Phase SQNR of an IQ ADC as a function of amplitude resolution $N_{\mathrm{IQ}}$ for different vector magnitude distributions. (b) Phase SQNR of a PhADC as a function of phase resolution $N_{\mathrm{Ph}}$; the phase SQNR is not affected by the vector magnitude variations.

A similar concept can be applied to $\mathrm{SQNR}_{\varphi,\mathrm{IQ}}$, yielding:

$$\mathrm{ENOB}_{\varphi,\mathrm{IQ}} = \frac{6}{6.02} N_{\mathrm{IQ}} + 1.69 \approx N_{\mathrm{IQ}} + 1.69, \tag{4.8}$$

which shows that phase ENOB is 1.69 bit greater than $N_{\mathrm{IQ}}$ for a constant-magnitude vector. However, realistic vector signals do not always have constant magnitudes. The phase SQNR for a non-constant magnitude vector is studied next.

#### 4.2.1.2 Non-constant vector magnitude

The vector magnitude in a practical receiver system might change with time-varying transmitting power and communication channel attenuation. As illustrated in Fig. 4.4(a), the amplitude quantization noise $(\Delta i, \Delta q)$ produces a larger phase quantization noise $(\Delta\varphi_1)$ at a small vector magnitude $(A_1)$ than it does at a large vector magnitude, i.e., $\Delta\varphi_0$ associated with $A_0$. Thus, the total phase quantization noise power associated with a non-constant vector magnitude is greater than that associated with a constant vector magnitude.

Let us consider the two vector distributions shown in Fig. 4.1(b) and (c), which both have random phase distributions and random vec-

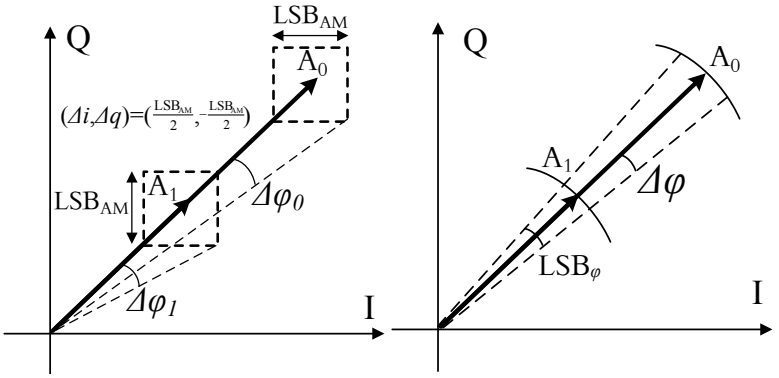



Figure 4.4: Phase quantization noise when the input vector has different magnitudes for (a) an IQ ADC, and (b) a PhADC.

tor magnitudes, but with different magnitude ranges, i.e., $[FS/4,\ FS/2]$ in (b) and $[0,\ FS/2]$ in (c), respectively. Since the vector magnitude is usually maintained within a limited range by a preceding variable gain amplifier (VGA) in practice, the vector distribution shown in Fig. 4.1(b) is more realistic and representative than the ones shown in Fig. 4.1(a) and Fig. 4.1(c). The SQNR of the quantized phase is calculated and plotted in Fig. 4.3(a), indicating that the phase SQNR decreases with increasing magnitude range. For the vector distribution shown in Fig. 4.1(b), a linear function can relate the phase SQNR and $N_{\mathrm{IQ}}$ as:

$$\mathrm{SQNR}_{\varphi,\mathrm{IQ,NM}} = 6N_{\mathrm{IQ}} + 8.7\,(\mathrm{dB}). \tag{4.9}$$

Thus, the ENOB of the phase output is:

$$\mathrm{ENOB}_{\varphi,\mathrm{IQ,NM}} \approx N_{\mathrm{IQ}} + 1.2. \tag{4.10}$$

The key observation from comparing (4.8) and (4.10) is that 0.49 bit phase ENOB is lost due to the increased magnitude range. In other words, an IQ ADC needs 0.49 bit extra to accommodate the varying vector magnitude and compensate for the phase ENOB degradation.

### 4.2.2 PhADC

Before comparing the phase SQNR of a PhADC with that of an IQ ADC, the phase SQNR of the PhADC also needs to be related to

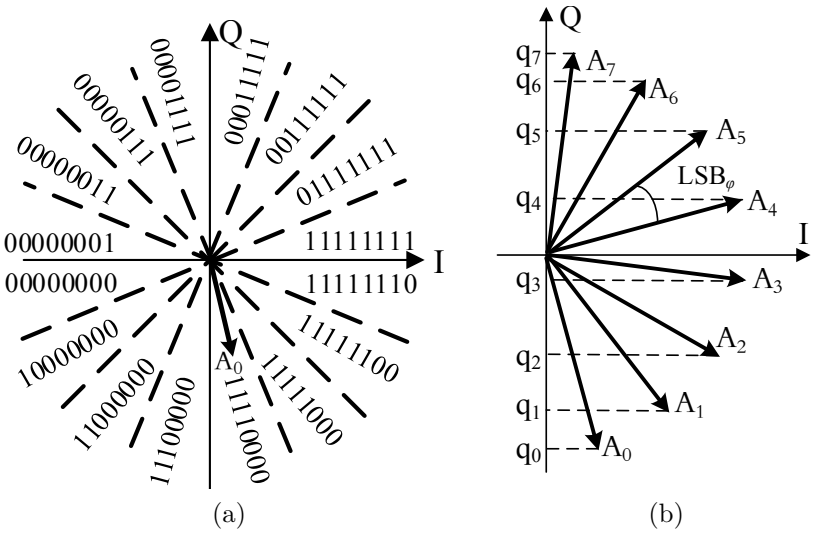



Figure 4.5: (a) The complex IQ plane is split into 16 uniform sectors by a 4 bit PhADC. (b) The Q projection of a vector $A_0$ and its seven rotated versions; the 8-bit words in (a) represent the signs (zero-crossing detections) of the 8 Q projections when the vector is in the corresponding phase sector.

phase resolution analytically for different vector magnitude distributions. This is discussed in this section.

A PhADC is an amplitude-to-phase converter with quantization functionality. For an $N_{\rm Ph}$ bit PhADC, the IQ-plane is split into $2^{N_{\rm Ph}}$ sectors with an angle of $\mathrm{LSB}_\varphi = 2\pi/2^{N_{\rm Ph}}$ between consecutive quantization intervals [22], as illustrated by the example in Fig. 4.5(a). The quantization is realized by generating and then detecting the signs (zero crossings) of the original and rotated I or Q projections. As shown in Fig. 4.5(b), the Q projection of vector $A_0$ and its rotated versions are $q_{0,1,\ldots 7}$, respectively. The 4 bit PhADC senses the zero crossings of $q_{0,1,\ldots 7}$, and counts the number of positive and negative zero crossings induced, then estimates the phase of $A_0$; the greater the number of the rotated projections, the higher the resolution of the phase. This quantization process can be seen in such a way that several input-dependent (unknown) quantization levels (e.g., $q_{0,1,\ldots 7}$) are generated to compare with zero (known) amplitude, which is oppo-

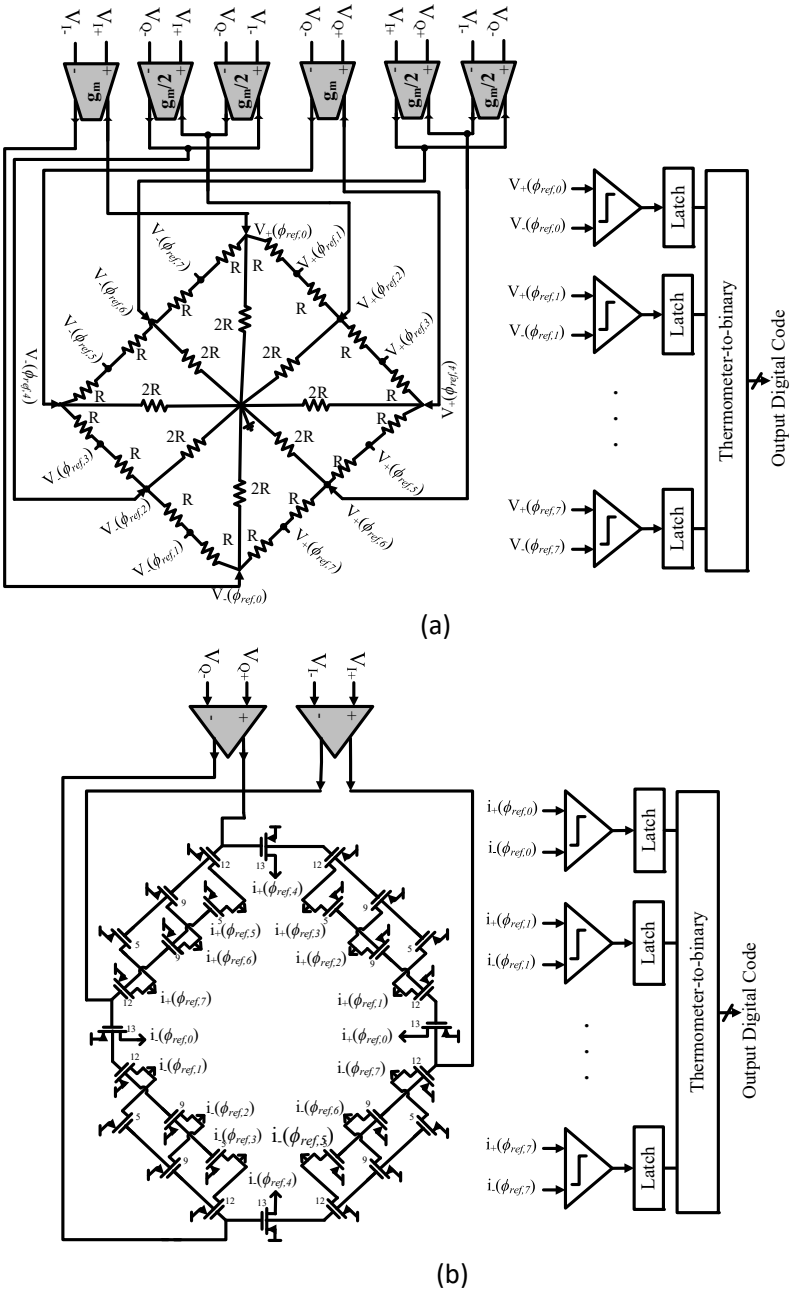



Figure 4.6: Block diagram of the ZC PhADC using (a) a resistive bridge [34, 35] and (b) a weighted current array [22].

site to the usual amplitude quantization process, i.e., several reference (known) quantization levels are generated to quantize an unknown input amplitude. However, in essence, both quantization processes are comparisons of one amplitude with several other amplitudes. This similarity can help us understand the influence of comparator offsets on the PhADC performance, as discussed in Section 4.5.

A rotated projection $q_k$ is related to the fundamental projections $i_0$ and $q_0$ as follows [22, 33]:

$$q_k = i_0 \cdot \sin \frac{k\pi}{2^{N_{\mathrm{Ph}}-1}} + q_0 \cdot \cos \frac{k\pi}{2^{N_{\mathrm{Ph}}-1}}, k = 0, 1, ..., 2^{N_{\mathrm{Ph}}-1} - 1. \quad (4.11)$$

This linear combination function can be implemented in circuitry either by a resistive bridge that converts input currents to phase-shifted voltages [34, 35], or a weighted current array that converts input voltages to phase-shifted currents [22]. Fig. 4.6(a) shows the block diagram of a resistor-bridge-based ZC PhADC. The resistor bridge converts the IQ currents to several phase-shifted voltages and these voltages are fed into the comparators which act as zero-crossing detectors. The outputs of the comparators form the thermometer digital code corresponding to the input signal phase. Fig. 4.6(b) shows the weighted-current-array-based approach. The current sources are properly sized to implement the coefficients of $i_0$ and $q_0$ in (4.11). The current-mode rotated versions of $i_0$ and $q_0$ are generated and their zero crossings can be detected by the subsequent comparators.

Being a linear quantizer in the phase domain, the quantization noise of the PhADC has properties similar to that of a linear amplitude ADC. It is accurate enough for most amplitude ADCs that the amplitude quantization noise for any ac signal that spans more than a few LSBs can be approximated by an uncorrelated sawtooth waveform having a peak-to-peak value of one LSB [61]. This assumption also holds true for the PhADC when the input phase spans the entire phase range, i.e., $[0, 2\pi)$. Fig. 4.2(b) shows the PDF of the phase quantization noise for a constant-magnitude input signal with random phase. Unlike the Gaussian-like distribution as shown in Fig. 4.2(a), the phase quantization noise is uniformly distributed over $[-\mathrm{LSB}_\varphi/2, \mathrm{LSB}_\varphi/2]$. The root-mean-square phase quantization noise is:

$$e_{\varphi,\mathrm{Ph,rms}} = \frac{\mathrm{LSB}_\varphi}{\sqrt{12}}. \quad (4.12)$$

Assuming the input phase is a full-scale sine wave expressed by (4.3) with an rms value given by (4.4), the SQNR of the quantized phase is:

$$\mathrm{SQNR}_{\varphi,\mathrm{Ph}} = 6.02N_{\mathrm{Ph}} + 1.76\,(\mathrm{dB}). \tag{4.13}$$

Hence, the ENOB of the PhADC is:

$$\mathrm{ENOB}_{\varphi,\mathrm{Ph}} = N_{\mathrm{Ph}}. \tag{4.14}$$

(4.13) is also well matched with the simulation results shown in Fig. 4.3(b), in which $\mathrm{SQNR}_{\varphi,\mathrm{Ph}}$ is plotted versus the phase resolution $N_{\mathrm{Ph}}$.

To be consistent with the analysis applied to the IQ ADC, the phase quantization noise distribution and the phase SQNR need to be analyzed in case the input vector magnitude is not constant as well. Since the PhADC is a direct linear quantizer in the phase domain, the phase quantization noise is independent from the vector magnitude. This independence is also conceptually illustrated in Fig. 4.4(b), showing that a large vector $A_0$ has the same phase quantization error as a small vector $A_1$. Therefore, (4.12), (4.13) and Fig. 4.3(b) also hold true for an input vector with a random magnitude and a random phase. Also, the phase quantization noise follows the same uniform distribution as the ones shown in Fig. 4.2(b).

The analysis in this section and Section 4.2.1 suggests that the phase SQNR of an IQ ADC decreases with increasing vector magnitude range, whereas that of a PhADC is immune to the vector-magnitude variation. In other words, from a system perspective, the IQ ADC needs extra bits to accommodate the varying vector magnitude, or the preceding automatic gain control (AGC) needs a finer gain resolution, whereas the PhADC can inherently accommodate the variation and relax the AGC control. This is one of fundamental benefits of the PhADC over the IQ ADC. This benefit becomes also evident from the measurement results reported in [22, 35], as well as the results in Section 4.4.3. We elaborate on this important property again in Section 4.4.3 with the aid of measurement results.

## 4.3 PhADC and IQ ADC comparison

The foregoing analysis formulates the vector-magnitude-variation accommodation effect of the PhADC. In this section, further compar-

isons between the two ADCs are made from several other perspectives. In IQ ADC-based low power receivers, moderate resolution (6-9 bit) and moderate speed (2.4-8 MS/s), SAR and pipeline ADCs are typically employed [62–64]. By contrast, PhADC-based low power receivers incorporate low phase resolution (4-5 bit) and moderate speed (1-20 MS/s) PhADCs [22,35,65]. We make the following observations on these two scenarios:

(1) Embedded demodulation. While the IQ ADC needs subsequent digital demodulation, the PhADC embeds most of the demodulation process in the quantization, thus saving the power and the area otherwise needed for the demodulation.

(2) Vector-magnitude variation accommodation. The 6-9 bit amplitude resolution of an IQ ADC can be translated into a phase $\text{ENOB}_{\varphi,\text{IQ}}$ of 7.7-10.7 bit as indicated by (4.8), which is more than that required by the FSK/PSK demodulation defined in low power wireless standards, e.g., BLE. This extra dynamic range is used to accommodate vector magnitude variations and interference. In contrast to the IQ ADC, a PhADC can inherently accommodate the magnitude variation as described in Section 4.2.2, and hence no extra phase dynamic range is needed for a PhADC.

(3) Interference accommodation. As mentioned above, the IQ ADC usually allocates some extra dynamic range to accommodate interference besides the magnitude variations, hence the desired channel can be precisely selected in the digital domain if the interference is not sufficiently suppressed by the stages preceding the ADC. However, the PhADC is not able to accommodate the interference even with extra phase dynamic range. This is because the amplitude interference is nonlinearly translated into a phase error of the desired phase, and the desired phase and the phase error are no longer carried by well-separated frequency channels as the desired amplitude and the interference at the input of the PhADC. These different attributes of interference accommodation mark an important application boundary between the two ADCs. That is, the PhADC is a more compact quantization and demodulation solution due to its embedded demodulation attribute, while the IQ ADC-based receiver can provide more channel-selection flexibility. For example, a simple $3^{\text{rd}}$-order analog channel selection filter and a 4 bit PhADC can already satisfy the requirements of the BLE standard [20], while IQ ADC-based receivers

can accommodate multiple low power wireless standards [63, 64].

(4) Energy efficiency. After many decades of research, today's IQ ADCs have become quite energy efficient in advanced IC processes. As an example, a SAR ADC in 40nm technology offers today a figure of merit (FoM) of 0.85 fJ/conv. step [66]. By contrast, the emerging PhADC has only a few reported silicon realizations and a state-of-the-art FoM of 8.3 pJ/conv. step in 0.13 $\mu$m technology [22]. Although the reported PhADCs are not as energy efficient as the IQ ADC yet, we want to address the fundamental energy difference between them, hence showing the room for improvement we could explore.

The following comparison is made in the typical operating condition of a PhADC, i.e., low phase resolution (4-5 bit) with no need to accommodate interference, demonstrating the preferable one of the two ADCs in such a condition. The translated amplitude resolution requirement of the IQ ADC is about 3-4 bit, as indicated by (4.10), which is less than that of the IQ ADCs in [62–64] (6-9 bit) since no interference need to be accommodated. This low resolution requirement makes flash, SAR and pipeline all possible architectures for the IQ ADC since they have the same order of energy efficiency [67]. The flash architecture is selected in the comparison due to its similarity with the most common PhADC architecture, i.e., the ZC PhADC [22,35]. Since the majority of the power consumption of both a flash ADC and a ZC PhADC is attributed to the comparators, the number of comparators is used to specify the power consumption. Also, the sampling rate and the input signals of both ADCs are assumed to be the same.

An $N_{\mathrm{IQ}}$ bit classical flash ADC has $2^{N_{\mathrm{IQ}}}-1$ comparators, thus an IQ ADC with two $N_{\mathrm{IQ}}$ bit ADCs has $2(2^{N_{\mathrm{IQ}}}-1)$ comparators. As described in Section 4.2.2, an $N_{\mathrm{Ph}}$ bit PhADC has $2^{N_{\mathrm{Ph}}-1}$ thresholds, so $2^{N_{\mathrm{Ph}}-1}$ comparators. If the IQ ADC and the PhADC have the same number of comparators, they have a resolution relationship as follows:

$$N_{\mathrm{Ph}} = \log_2(2^{N_{\mathrm{IQ}}}-1)+2, \tag{4.15}$$

indicating that $N_{\mathrm{Ph}}$ is roughly 2 bits larger than $N_{\mathrm{IQ}}$.

As noted in Section 4.2.1.2, the non-constant vector distribution shown in Fig. 4.1(b) is more realistic and representative than Fig. 4.1(a) and Fig. 4.1(c). Thus, the following comparison is made for an input vector with non-constant magnitude between $FS/4$ and $FS/2$. $\mathrm{ENOB}_{\varphi,\mathrm{IQ,NM}}$ and $\mathrm{ENOB}_{\varphi,\mathrm{Ph}}$ of the IQ ADC and the PhADC are

given by (4.10) and (4.14), respectively. Given the same number of comparators, i.e., their resolutions meet (4.15), the ENOB difference is:

$$\text{ENOB}_{\varphi,\text{Ph}} - \text{ENOB}_{\varphi,\text{IQ,NM}} = \log_2(2^{N_{\text{IQ}}} - 1) - N_{\text{IQ}} + 0.8, \quad (4.16)$$

showing that $\text{ENOB}_{\varphi,\text{Ph}}$ is higher than $\text{ENOB}_{\varphi,\text{IQ,NM}}$ as long as $N_{\text{IQ}}>1$ bit. For example, the ENOB difference is 0.7 bit when $N_{\text{IQ}}=4$ (i.e., both ADCs have 30 comparators). For another example, if both ADCs have a phase ENOB of 5 bit, the IQ ADC and the PhADC need 26 and 16 comparators ($N_{\text{IQ}}=3.8$ and $N_{\text{Ph}}=5$), respectively. Thus, the PhADC has a lower theoretical energy limit (fewer comparators) than the flash IQ ADC for a given phase ENOB. The favorable energy efficiency of the PhADC is contributed by two facts: (1) immunity to vector-magnitude variation, and (2) 1-D (phase-only) quantization rather than 2-D (IQ) quantization.

In summary, compared to the IQ ADC, the PhADC, due to its embedded demodulation attribute, is a more compact quantization and demodulation solution when interference accommodation is not required. Moreover, in the typical operating condition of the PhADC, i.e., low phase resolution with no need to accommodate the interference, the theoretical energy limit of the PhADC is addressed with respect to the IQ ADC. Considering a flash ADC as an example of the low resolution (3-4 bit) IQ ADC, the PhADC has a lower theoretical energy limit than the flash IQ ADC for a given phase ENOB due to the immunity to magnitude variation and the phase-only quantization, illustrating the great room for energy efficiency improvement that the emerging PhADC has.

## 4.4 A charge-redistribution PhADC

The foregoing analysis reveals several interesting attributes of the PhADC, as well as its limited energy efficiency. This section presents a more energy-efficient charge-redistribution PhADC.

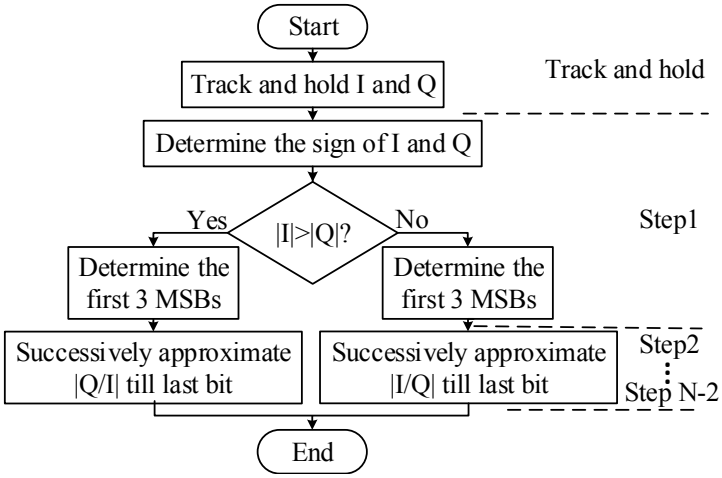



Figure 4.7: Flow chart of the proposed IQ-assisted conversion algorithm for an N bit PhADC.

### 4.4.1 Conversion algorithm and system architecture

The proposed IQ-assisted conversion algorithm relies on the simple mathematical fact that for the phase, $\varphi$, it holds:

$$\varphi = \begin{cases} \arctan \frac{Q}{I} & Q \leq I \\ \operatorname{arccot} \frac{I}{Q} & I < Q \end{cases}, \varphi \in [0, \frac{\pi}{2}] \tag{4.17}$$

where $I$ and $Q$ are the baseband in-phase and quadrature signals, respectively. Thus, the phase quantization between $[0, \frac{\pi}{2}]$ can be realized by the quantization of the ratio of either $\frac{Q}{I}$ or $\frac{I}{Q}$, depending on which one is greater, and the mapping onto $\varphi$. Considering the symmetrical properties of the arctan and arccot functions in the phase domain, the phase quantization over the entire phase range $[0, 2\pi]$ can be realized by the quantization of a ratio factor $a$, which is defined as:

$$a = \begin{cases} |\frac{Q}{I}| & |Q| < |I| \\ |\frac{I}{Q}| & |I| < |Q| \end{cases}, 0 \leq a \leq 1. \tag{4.18}$$

The range of $a$ indicates that the quantized phase is between 0 and $\frac{\pi}{2}$, but can be mapped back to the correct phase with the aid of the

relations in (4.17) and the signs of the $I$ and $Q$ signals. The quantization process of $a$ is essentially the same as that of a standard amplitude ADC, i.e., one amplitude is digitized by a reference amplitude, despite that the reference amplitude here is either the unknown $I$ or the unknown $Q$ rather than a known amplitude as is the case in the amplitude ADC. Consequently, the IQ-assisted algorithm could be implemented in a single (i.e., voltage or current or charge) domain like is done in a standard amplitude ADC. In contrast with the zero-crossing algorithm, the IQ-assisted algorithm doesn't employ a linear combination of the $I$ and $Q$ signals with various scaling factors, hence doesn't require additional power consumption and doesn't suffer from any performance degradation introduced during the combination.

Fig. 4.7 shows the flow chart of the proposed algorithm for an N bit PhADC. After sampling the amplitudes of $I$ and $Q$, three comparisons are made in Step 1, viz., $I > 0$?, $Q > 0$?, and $|I| > |Q|$?. The result of $|I| > |Q|$? can be resolved by determining $Q{>}I$? and $-Q{>}I$? with the aid of the signs of $I$ and $Q$. Therefore, the first three most significant bits (MSBs) of the phase can be determined by the four comparisons in Step 1. In the next N-3 steps, $I$ or $Q$ is digitized by $(\pm)Q$ or $(\pm)I$ using a successive approximation algorithm, resolving the remaining N-3 bits. While any other standard amplitude conversion algorithm can also be applied from Step 2 to the end, the successive approximation algorithm is adopted to facilitate energy efficient charge domain operation.

The proposed 5 bit charge-redistribution PhADC diagram is shown in Fig. 4.8. Both the $I$ and $Q$ voltages are tracked and then held by a track-and-hold (T/H) circuit as well as a charge-redistribution DAC. The simultaneous T/H operation is controlled by the signal SAP. The voltages being held by two T/H circuits, i.e., $\mathrm{T/H_I}$ and $\mathrm{T/H_Q}$, are $Q_H$ and $I_H$, respectively. In conversion Steps 1-3, $Q_H$ behaves as the reference voltage of $\mathrm{DAC_I}$, while $I_H$ is the reference voltage of $\mathrm{DAC_Q}$. Four comparators, i.e., $\mathrm{Comp_{I1}}$, $\mathrm{Comp_{I2}}$, $\mathrm{Comp_{Q1}}$ and $\mathrm{Comp_{Q2}}$, determine the first 3 MSBs in Step 1. The last two bits can be resolved by a T/H circuit, a DAC and a comparator in the charge domain with low power consumption. Digital control logic decodes the comparator outputs and controls the switching procedure of $\mathrm{DAC_I}$ and $\mathrm{DAC_Q}$ via $\mathrm{S_I}$ and $\mathrm{S_Q}$, respectively. In order to save power consumption further, all blocks are gated according to the conversion phases as illustrated

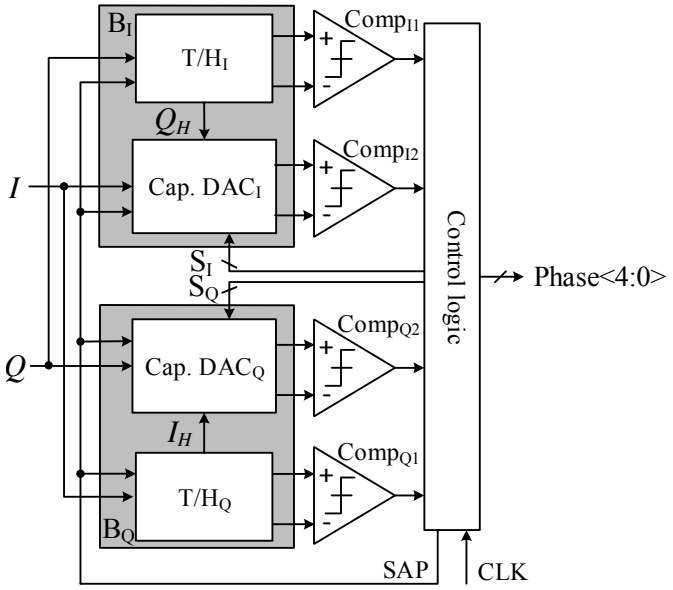



Figure 4.8: Proposed 5 bit PhADC block diagram.

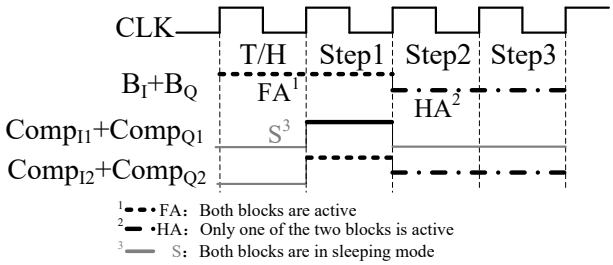



Figure 4.9: Circuit blocks are gated according to conversion phases.

in Fig. 4.9. Blocks $B_I$ and $B_Q$ denote the combination of $T/H_I$ and $DAC_I$, and of $T/H_Q$ and $DAC_Q$, respectively.

## 4.4.2 Circuit design

### 4.4.2.1 Charge-redistribution DAC

The capacitance network of the PhADC implements another T/H operation besides the one made by the active T/H circuits, feedback DAC and summation node. As the phase is nonlinearly related to the ratio of $I$ and $Q$ (or $Q$ and $I$) due to the arctan and arccot relations,

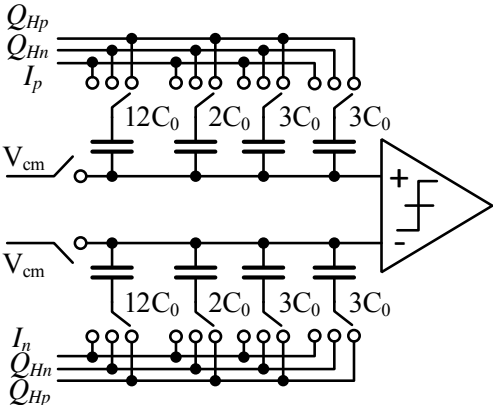



Figure 4.10: 2 bits unary-weigthed charge-redistribution $\mathrm{DAC_I}$. $\mathrm{DAC_Q}$ has the same architecture.

in order to extract the linear phase, we need to nonlinearly map this ratio onto the quantized phase. In order to do so, two monotonic nonlinear unary DACs are implemented to approximate the nonlinear tan and cot functions between $[0, \frac{\pi}{2}]$ as follows:

$$\begin{aligned}
\tan\frac{\pi}{16} &= \frac{Q}{I} \approx \frac{2}{10}, \quad \cot\frac{7\pi}{16} = \frac{I}{Q} \approx \frac{2}{10} \\
\tan\frac{2\pi}{16} &= \frac{Q}{I} \approx \frac{4}{10}, \quad \cot\frac{6\pi}{16} = \frac{I}{Q} \approx \frac{4}{10} \\
\tan\frac{3\pi}{16} &= \frac{Q}{I} \approx \frac{7}{10}, \quad \cot\frac{5\pi}{16} = \frac{I}{Q} \approx \frac{7}{10} \\
\tan\frac{4\pi}{16} &= \frac{Q}{I} = 1 \quad , \quad \cot\frac{4\pi}{16} = \frac{I}{Q} = 1
\end{aligned} \tag{4.19}$$

As shown in Fig. 4.8, the approximated tan function is realized by $\mathrm{DAC_Q}$ with $Q$ being the input voltage and $I_H$ being the reference voltage, whereas the cot function is realized by $\mathrm{DAC_I}$ with $I$ being the input voltage and $Q_H$ being the reference voltage. The architectures of the two DACs are identical. The largest error generated by the approximation is only $0.7^\circ = 0.06$ times the phase least significant bit (LSB), which is not a dominant source of error.

The DAC in the I signal path, $\mathrm{DAC_I}$ shown in Fig. 4.10, is taken as an example to describe its major design considerations. A differential DAC architecture is employed here since the $I$ and $Q_H$ as shown in Fig.

4.8 have different common mode voltages. Moreover, the differential architecture suppresses the odd-order amplitude nonlinearities of $I$ and $Q_H$, hence reducing the phase error introduced by them. Each side of the differential network has 20 unit capacitors, which are segmented in such a way that the scaling factors in (4.19) can be obtained by the differential switching operation, viz., $\frac{2}{10} = \frac{12}{20} - \frac{8}{20}$, $\frac{4}{10} = \frac{14}{20} - \frac{6}{20}$, and $\frac{7}{10} = \frac{17}{20} - \frac{3}{20}$. The unit capacitor is implemented as a metal-metal capacitor by using only metal 5 (the one below the "analog metal") with a small value of 2.4 fF, which achieves a good trade-off between power efficiency and accuracy. Since $Q_{Hp}$ and $Q_{Hn}$ vary between 0.35 V to 0.85 V, complementary switches are used for $Q_{Hp}$ and $Q_{Hn}$ to reduce the nonlinearity.

#### 4.4.2.2 T/H circuit and comparator

The low precision T/H circuit shown in Fig. 4.11(a) [68] is used in our design, due to its favorable energy efficiency and sufficient linearity in this relatively low resolution prototype. In post-layout simulations, the T/H circuit achieves a THD of -43 dB with a 499 kHz 1 Vpp input, and consumes 1.6 $\mu$A.

Due to the limited driving ability of the T/H circuit and the small value of the capacitor network (i.e., around 50 fF at each input node of the comparator), kickback noise is of primary concern in the comparator selection and design. We adopt the static comparator shown in Fig. 4.11(b) [69] for our design. Two reset NMOS switches in parallel with the NMOS latch in [69] are replaced by a single switch M12, precharging Nodes $V_{op}$ and $V_{on}$ before the decision phase to increase speed. However, the precharged $V_{op}$ and $V_{on}$ may give rise to a static current in the subsequent SR latch during the reset phase if $V_{op}$ and $V_{on}$ are directly connected to the SR latch. For this reason, AND gates A1 and A2 are added to isolate the SR latch from the precharged analog voltages. The comparator can operate at 4 MHz clock rate. Its maximum input-referred offset measured through 200 Monte Carlo runs is 15 mV. M10 + M11 in Fig. 4.11(b), and M9 + M10 in Fig. 4.11(a) are used to enable/disable the comparator and the T/H circuit, respectively, thereby saving unnecessary power.

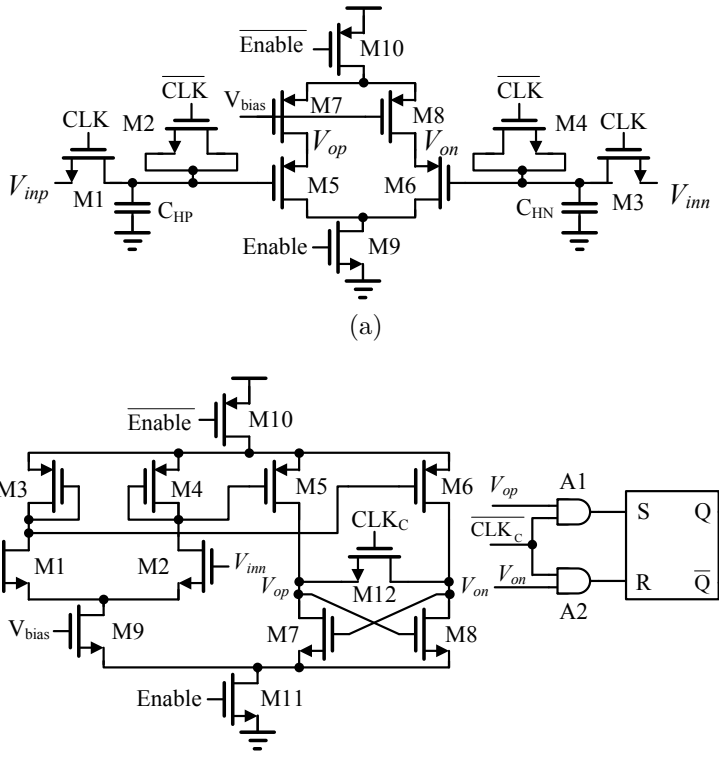



Figure 4.11: (a) Track-and-hold circuit. (b) Comparator circuit.

### 4.4.3 Measurement results

The prototype charge-redistribution PhADC is fabricated in 0.18 $\mu$m AMS CMOS technology with a core chip area of 0.059 mm$^2$. A micrograph of the die is shown in Fig. 4.12. The performance of the ADC is measured at 1.2 V and a 1 MS/s sampling rate. The 5 bit output is captured using a logic analyzer and fed to MATLAB for performance evaluation.

The dynamic performance of a standard amplitude ADC is usually measured with a single-tone input signal. Similarly, a complex signal (i.e., a pair of I and Q signals) with a single-tone phase input, i.e., $\pi\cos(\omega t)$ is used here to characterize the proposed PhADC. Due to the nonlinear relationship between the phase and the complex signal, the spectrum of the complex signal corresponding to the single-tone phase consists of several frequencies harmonically related to the phase

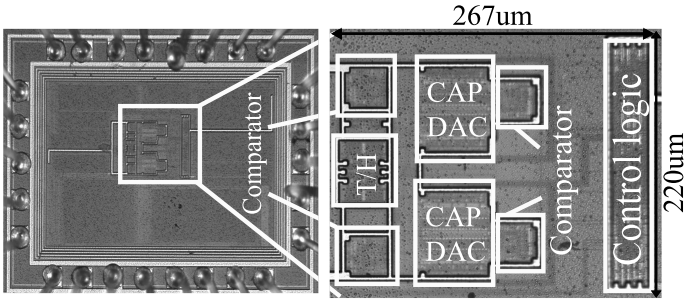



Figure 4.12: Die micrograph of the charge-redistribution PhADC

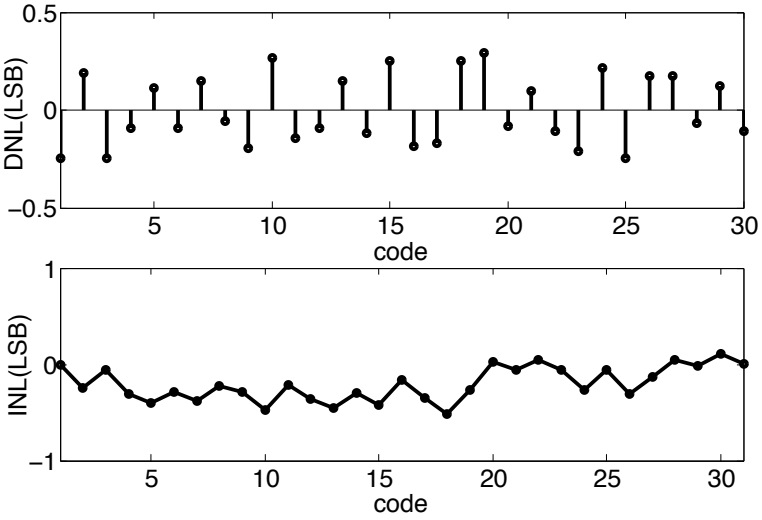
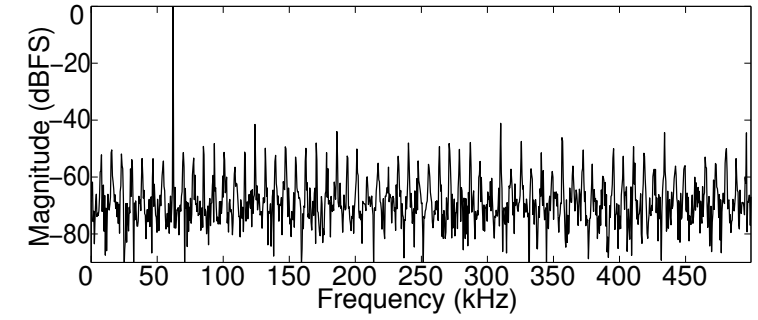


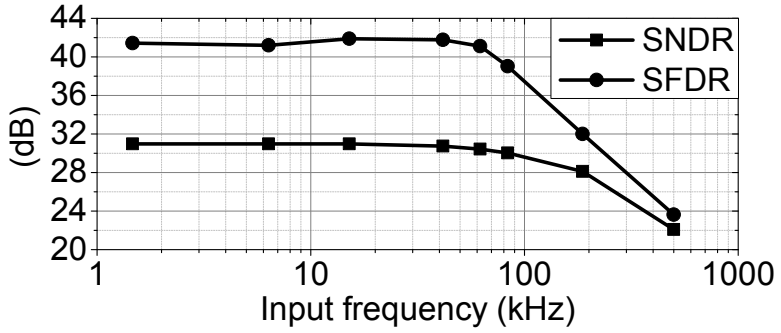

Figure 4.13: Measured DNL and INL. The differential peak-to-peak voltages of the I and Q signals are 900 mV.

frequency. For example, if only the first two non-DC frequency components of the I and Q signals are taken into account, the bandwidth of the I and Q signals is 8 times the phase frequency. Considering the channel bandwidths of low power short range standards, e.g. IEEE 802.15.6 [10], ranging from 300 kHz to 1 MHz, this prototype is designed for a phase frequency up to 62 kHz, and is specified up to the Nyquist frequency (i.e., 499 kHz).

The maximum DNL and INL are +0.29/-0.29 LSB and +0.11/-0.52 LSB, respectively, as shown in Fig. 4.13. Fig. 4.14(a) shows the output spectrum for a 62.01 kHz input phase, and Fig. 4.14(b) shows




(a)




(b)

Figure 4.14: (a) Measured spectrum (2048-point FFT) at 1 MS/s with a 62.01 kHz input phase. (b) SNDR and SFDR as a function of input phase frequency. The differential peak-to-peak voltages of the I and Q signals are 900 mV.

the SNDR and SFDR as a function of the input phase frequency. The SNDR at 1.5 kHz is 30.98 dB, i.e., yielding an ENOB of 4.85 bit, while the ERBW is 187 kHz. The decreased SNDR with increasing frequency is mainly due to the expanded bandwidth of the complex signal and the frequency-dependent nonlinearity of the T/H circuit. Like the PhADC in [22, 35], the proposed PhADC also features a large amplitude dynamic range (DR) as shown in Fig. 4.15. The SNDR at 1.2 Vpp is 30.9 dB, and drops by 3 dB at 0.4 V, indicating an amplitude DR of 9.5 dB. This proves an important property of the PhADC addressed in Section 4.2.2, i.e., its immunity to vector-magnitude variations. The SNDR should ideally remain constant over the input variation since the phase quantization noise is independent

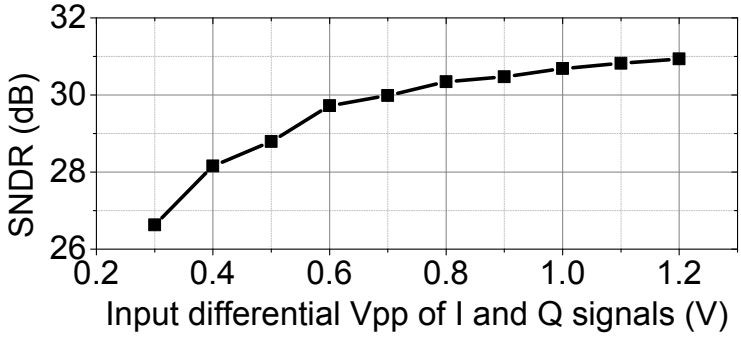



Figure 4.15: Measured SNDR as a function of the differential peak-to-peak voltages of the I and Q signals with a phase frequency of 62.01 kHz.

from the input amplitude. However, other circuit nonidealities, such noise and offset, become more pronounced as the input amplitude decreases, thereby degrading the SNDR.

The ADC consumes 10.76 $\mu$A from a 1.2 V power supply, translating into a FoM of 1.2 pJ/step at 1 MS/s. The performance of the proposed ADC is summarized and compared with prior art in Table 4.1.

Table 4.1: Performance comparison.

| | [22] | [35] | This work |
|---|---|---|---|
| Technology ($\mu$m) | 0.13 | 0.18 | 0.18 |
| Power supply (V) | 1 | 1.2 | 1.2 |
| Power ($\mu$W) | 25 | 348 | 12.9 |
| Sampling rate (MS/s) | 20 | 3.2 | 1 |
| Resolution (bit) | 4 | 4 | 5 |
| ENOB (bit) | 3.61 | - | 4.85 |
| ERBW (kHz) | 123.1[a] | - | 187 |
| FoM[b] (pJ/step) | 8.3 | - | 1.2 |
| Amplitude DR (dB) | 19[a,c] | 41[d] | 9.5[c] |
| Chip area (mm$^2$) | 0.015 | 0.044 | 0.059 |

[a]Estimated from [22]. [b]FoM=Power/($2^{\mathrm{ENOB}}$·2·ERBW).
[c]The range over which SNDR remains constant within 3dB.
[d]The range over which the maximum quantization error $< 0.5$ LSB.

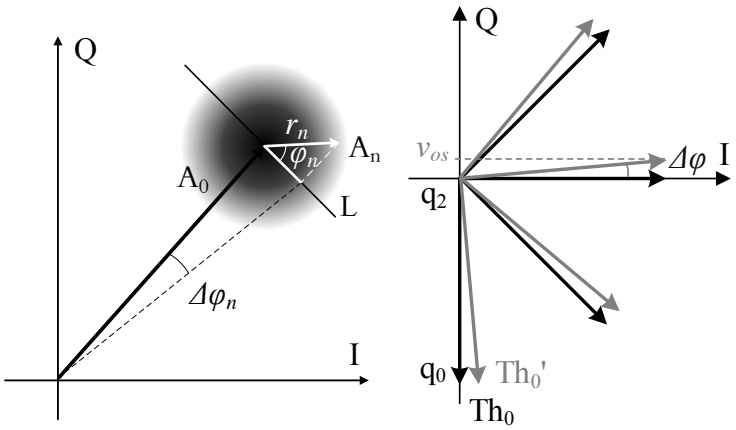



Figure 4.16: (a) Phase noise caused by complex Gaussian amplitude noise. (b) Phase reference level fluctuation caused by comparator offsets for a 3 bit PhADC.

## 4.5 Phase nonidealities of the PhADC

Our analysis and implementation of the PhADC thus far has not elaborated on the effect of common amplitude nonidealities, which usually manifest themselves as noise, gain errors and offsets injected by preceding stages, as well as the amplitude errors introduced during conversions. Due to the different quantization mechanism of the PhADC with respect to that of an IQ ADC, the influence of the amplitude nonidealities on the phase should be analyzed and compared with the IQ ADC if necessary. The amplitude errors introduced during conversions highly depend on the circuit architecture of the PhADC. We focus on the effects of comparator offset of the ZC PhADC here.

### 4.5.1 Input noise

Since all noise introduced before the ADCs affects the phase SNR of both an IQ ADC and a PhADC in the same manner, the analysis below first takes the IQ ADC as an example and then simply extends the conclusions to the PhADC. Assuming the input noise of both I and Q signals are white Gaussian noise with zero mean and a stan-

dard deviation $\sigma_{\text{noise}}$, a vector $A_0$ and its complex Gaussian noise are shown in Fig. 4.16(a). $r_n$ is the magnitude of the noise vector and $\varphi_n$ is its phase with respect to line L (perpendicular to $A_0$) in the figure. The magnitude of the vector $A_0$ is $FS/2$. Using a small angle approximation, the phase noise $\Delta\varphi_n$ introduced by noise vector $A_n$ is approximated as:

$$\Delta\varphi_n \approx \tan\Delta\varphi_n = \frac{r_n \cos\varphi_n}{FS/2}. \tag{4.20}$$

It is necessary to evaluate the validity of the small-angle approximation. [70] has proven that the PDF of the phase noise $\Delta\varphi_n$ can be approximated as a Gaussian distribution if the input amplitude SNR is higher than 6.5 dB. Considering that the reported PhADCs in [20, 22, 33, 35] and the proposed PhADC in Section 4.4 target communication standards such as Bluetooth Low Energy and IEEE 802.15.6, the required SNR at the input of the PhADC is around 12 dB or higher. Thus, the Gaussian approximation is valid for the PhADCs for these applications. Based on the approximated Gaussian distribution presented in [70], if the input amplitude SNR is 12 dB, the standard deviation of the phase noise is 10.2°. cos(10.2°) is equal to 0.98, which is very close to unity, and hence the small-angle approximation made for 4.20 is sufficiently accurate for an SNR of 12 dB or higher.

The noise magnitude $r_n$ and noise phase $\varphi_n$ of the complex Gaussian noise have Rayleigh and uniform distributions respectively, and they are statistically independent of each other [60]. The power of the phase noise is given by [60]:

$$P_{\varphi,\text{noise}} = \int_0^{+\infty}\int_{-\pi}^{\pi}(\frac{r_n\cos\varphi_n}{FS/2})^2 f(r_n,\varphi_n)d\varphi_n dr_n, \tag{4.21}$$

where $f(r_n, \varphi_n)$ is the joint density of $r_n$ and $\varphi_n$. The density functions of $r_n$ and $\varphi_n$ are:

$$f(r_n) = \frac{r_n}{\sigma^2_{\text{noise}}} e^{-r_n/2\sigma^2_{\text{noise}}} \quad r_n \in [0, +\infty), \tag{4.22}$$

$$f(\varphi_n) = \begin{cases} 1/2\pi & \varphi_n \in (-\pi, +\pi) \\ 0 & \text{otherwise} \end{cases}. \tag{4.23}$$

Thus, the joint density function of $r_n$ and $\varphi_n$ is:

$$f(r_n, \varphi_n) = \frac{r_n e^{-r_n/2\sigma^2_{\text{noise}}}}{\sigma^2_{\text{noise}}} \frac{1}{2\pi} \; r_n \in [0, +\infty), \; \varphi_n \in (-\pi, +\pi). \quad (4.24)$$

Substituting (4.24) into (4.21), we get:

$$P_{\varphi,\text{noise}} = \frac{\sigma^2_{\text{noise}}}{(FS/2)^2} = \frac{P_{\text{am,noise}}}{(FS/2)^2}, \quad (4.25)$$

where $P_{\text{am,noise}}$ is the amplitude noise power. Since $P_{\varphi,\text{noise}}$ is independent of the phase of $A_0$, the average phase noise power over the entire phase range is still (4.25) as long as the vector magnitude is constant. It is reasonable to assume that the amplitude quantization noise is uncorrelated with the input amplitude and so is its phase counterpart, as noted in Section 4.2.1; thus both the IQ amplitude and phase are assumed to be sinusoidal. The power of the IQ amplitude is $P_{\text{IQ,sig}} = \frac{(FS/2)^2}{2}$. If the SNR of the IQ signal is defined as $\text{SNR}_{\text{am}} = P_{\text{IQ,sig}}/P_{\text{am,noise}}$, (4.25) can be rewritten as:

$$P_{\varphi,\text{noise}} = \frac{1}{2\text{SNR}_{\text{am}}}. \quad (4.26)$$

If quantization noise is not taken into account, SNR is:

$$\text{SNR}_{\varphi,\text{noise}} = \frac{P_\varphi}{P_{\varphi,\text{noise}}} = \frac{\pi^2/2}{1/(2\text{SNR}_{\text{am}})} = \pi^2 \text{SNR}_{\text{am}}, \quad (4.27)$$

where $P_\varphi$ is the phase signal power. It can also be expressed in dB as:

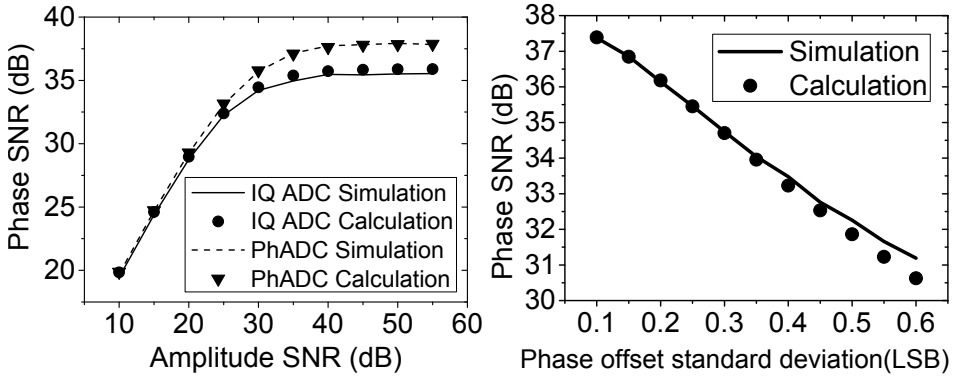
$$\text{SNR}_{\varphi,\text{noise}} = \text{SNR}_{\text{am}} + 10 \text{ (dB)}. \quad (4.28)$$

The total SNR with quantization noise and $P_{\varphi,\text{noise}}$ is:

$$\text{SNR}_{\text{IQ},\varphi,\text{TN}} = \frac{1}{1/\text{SNR}_{\text{IQ},\varphi} + 1/\text{SNR}_{\varphi,\text{noise}}}, \quad (4.29)$$

where $\text{SNR}_{\text{IQ},\varphi}$ is given by (4.6). $\text{SNR}_{\text{IQ},\varphi,\text{TN}}$ can be rewritten as a function of $\text{SNR}_{\text{am}}$ and $N_{\text{IQ}}$ by substituting (4.6) and (4.27) into (4.29), resulting in:

$$\text{SNR}_{\text{IQ},\varphi,\text{TN}} = \frac{\pi^2 \text{SNR}_{\text{am}}}{\pi^2 \text{SNR}_{\text{am}} 10^{-(0.6N_{\text{IQ}}+1.19)} + 1}. \quad (4.30)$$




(a) (b)

Figure 4.17: (a) Phase SNR as a function of amplitude SNR for a 4 bit IQ ADC and a 6 bit PhADC. (b) SNR degradation due to comparator offsets for a 6 bit PhADC.

The above analysis also holds true for the PhADC if the $\mathrm{SNR}_{\mathrm{IQ},\varphi}$ in (4.29) is replaced by (4.13), thus the phase SNR of the PhADC considering both the quantization noise and the phase noise is:

$$\mathrm{SNR}_{\mathrm{Ph},\varphi,\mathrm{TN}} = \frac{\pi^2 \mathrm{SNR}_{\mathrm{am}}}{\pi^2 \mathrm{SNR}_{\mathrm{am}} 10^{-(0.602 N_{\mathrm{Ph}}+0.176)} + 1}. \tag{4.31}$$

The accuracies of (4.30) and (4.31) are verified by simulations using a 4 bit IQ ADC and a 6 bit PhADC respectively, as shown in Fig. 4.17(a). The difference between the calculations and simulations is less than 0.5dB, and is caused by the small angle approximation.

In summary, if both the IQ ADC and the PhADC are limited by the input noise rather than the quantization noise, their phase SNR is 10dB higher than $\mathrm{SNR}_{\mathrm{am}}$ as shown by (4.28). When the phase quantization noise is taken into account, the quantization noise becomes more dominant than the input noise with increasing $\mathrm{SNR}_{\mathrm{am}}$. In the given example, $\mathrm{SNR}_{\mathrm{IQ},\varphi,\mathrm{TN}}$ and $\mathrm{SNR}_{\mathrm{Ph},\varphi,\mathrm{TN}}$ are not limited by $\mathrm{SNR}_{\mathrm{am}}$ anymore when $\mathrm{SNR}_{\mathrm{am}}$ is larger than 30dB.

The above analysis, particularly (4.28), translates a phase SNR into an equivalent amplitude SNR, which is a more familiar measure for analog circuitry. This equivalent amplitude SNR facilitates the system analysis of a receiver using a PhADC, which is addressed in Chapter 5.

### 4.5.2 Comparator offsets

Let us first consider the effect of comparator offset in a standard flash ADC. The input-referred offset of a comparator consists of static components (e.g. threshold mismatch of an input pair), as well as dynamic components caused by the nonlinear transconductance of the latches. It is usually acceptable to characterize the offset by a Gaussian distribution with zero mean and a standard deviation $\sigma_{\mathrm{OS}}$ [59]. The fluctuation of reference levels caused by the comparator offset in a flash amplitude ADC can be seen as a random noise source in series between the input signal and an ideal quantizer if the input signal is assumed to vary sufficiently [59]. Thus, a flash ADC can be modeled as an ideal quantizer with an input as:

$$v_{\mathrm{in,OS}} = v_{\mathrm{in}} + v_{\mathrm{OS}}, \tag{4.32}$$

where $v_{\mathrm{in}}$ is the input signal, and $v_{\mathrm{OS}}$ is the comparator offset with a standard deviation $\sigma_{\mathrm{OS}}$.

We now determine the effects of comparator offsets on the PhADC. As noted in Section 4.2.2, an $N_{\mathrm{Ph}}$ bit PhADC can be seen as an amplitude quantizer with $2^{N_{\mathrm{Ph}}-1}$ unknown quantization levels, which are all compared with a known zero amplitude (i.e., zero-crossing detection). This is similar to a flash amplitude ADC, which instead has multiple known quantization levels and an unknown input. Therefore, it is also valid to assume that the PhADC with comparator offsets behaves as an ideal PhADC with a Gaussian distributed "zero" amplitude as:

$$\mathrm{zero}_{\mathrm{OS}} = 0 + v_{\mathrm{OS}}. \tag{4.33}$$

The phase noise introduced by $v_{\mathrm{OS}}$ can be conceptually explained by an example in Fig. 4.16(b) as follows. $q_{0,1..3}$ are the original and three rotated Q projections of phase quantization level $Th_0 = -\pi/2$, and the projection $q_2$ should ideally be zero. The Gaussian-"zero" amplitude makes $q_2$ fluctuate around zero, thus resulting in a fluctuation of $Th_0$. If the fluctuation around zero is $v_{\mathrm{OS}}$ as shown in Fig. 4.16(b), the phase error on $Th_0$ is $\Delta\varphi = \arcsin \frac{v_{\mathrm{OS}}}{FS/2}$, which can be approximated using a small angle approximation as $\Delta\varphi = \frac{v_{\mathrm{OS}}}{FS/2}$. Therefore, the overall effect of the comparator offsets is introducing Gaussian distributed phase offsets into all phase quantization levels, which now is exactly the same as the effect of the offsets on the flash amplitude ADC as

discussed above. Moving the offsets of all quantization levels into an equivalent one in series with the input phase, the input becomes:

$$\varphi_{\mathrm{Ph,OS}} = \varphi + \varphi_{\mathrm{OS}}, \tag{4.34}$$

where $\varphi_{\mathrm{OS}}$ has a Gaussian distribution with zero mean and a standard deviation $\sigma_\varphi = \frac{\sigma_{\mathrm{OS}}}{FS/2}$. The offset now plays exactly the same role as the Gaussian noise discussed in Section 4.5.1. Thus, the power of $\varphi_{\mathrm{OS}}$ is:

$$P_{\mathrm{Ph},\varphi,\mathrm{OS}} = \frac{\sigma_{\mathrm{OS}}^2}{(FS/2)^2}, \tag{4.35}$$

If the quantization noise is not taken into account, SNR becomes:

$$\mathrm{SNR}_{\mathrm{Ph},\varphi,\mathrm{OS}} = \frac{P_\varphi}{P_{\mathrm{Ph},\varphi,\mathrm{OS}}} = \frac{(\pi FS)^2}{8}\frac{1}{\sigma_{\mathrm{OS}}^2}. \tag{4.36}$$

Replacing $\mathrm{SNR}_{\varphi,\mathrm{noise}}$ and $\mathrm{SNR}_{\mathrm{IQ},\varphi}$ in (4.29) with $\mathrm{SNR}_{\mathrm{Ph},\varphi,\mathrm{OS}}$ and (4.13), the total SNR with quantization noise is:

$$\mathrm{SNR}_{\mathrm{Ph},\varphi,\mathrm{QN+OS}} = \frac{\pi^2}{\pi^2 10^{-(0.602N_{\mathrm{Ph}}+0.176)} + 2\sigma_\varphi^2}. \tag{4.37}$$

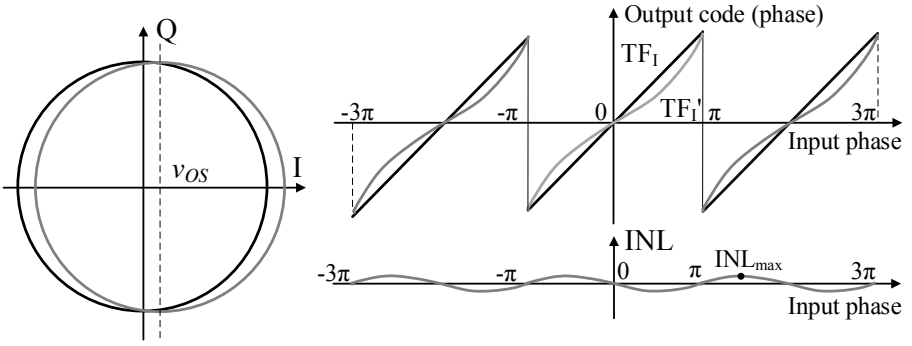
The accuracy of (4.37) is verified by the simulation results shown in Fig. 4.17(b), which indicate that a small angle approximation is less valid at higher offset values, but the approximation error is still less than 0.5dB.

The key observation in the above analysis is that the effect of the comparator offsets can be modeled as a phase noise with a Gaussian distribution at the input and be formulated as (4.37).

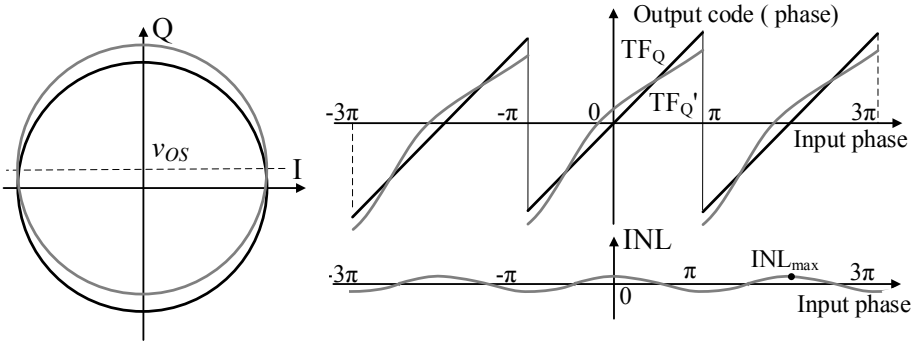
### 4.5.3 IQ offsets and IQ amplitude mismatch

The above analysis shows that the noise has the same effect on an IQ ADC as on a PhADC. However, two other amplitude nonidealities, i.e., IQ offset and IQ amplitude mismatch, behave differently in the two ADCs, as described next.

Due to the nonlinear amplitude-to-phase conversion, IQ offsets and amplitude mismatch can produce nonlinear phase distortions. Although theoretically both the IQ ADC and PhADC suffer from this effect in the same way, it is well known in practice that the mismatch




(a)




(b)

Figure 4.18: Vector trajectory shifting and nonlinear phase transfer functions due to (a) I offset, and (b) Q offset. The shape of $TF_I$' and $TF_Q$' are verified using Matlab simulations and redrawn in the figure.

and the offset can be detected and calibrated if necessary before amplitude is converted into phase for the IQ ADC, whereas the direct mismatch and offset detection cannot be employed for the PhADC due to the absence of amplitude information. Therefore, the effects of phase nonlinearity are only analyzed for the PhADC.

An ideal PhADC has a linear transfer function, as the curve $TF_I$ shows at the right hand side of Fig. 4.18(a), resulting in a circular output trajectory centered exactly at the origin of the IQ plane for a constant-magnitude input vector, as depicted at the left hand side of the figure. When an positive offset $v_{OS}$ is added to the I amplitude, the

trajectory is shifted to the right and the corresponding phase transfer function changes to the nonlinear curve $TF_I$'. Similarly, the nonlinear transfer function caused by a Q offset with a value of $v_{OS}$ is shown in Fig. 4.18(b), which has the same shape as the one in Fig. 4.18(a) but with a phase shift of $\pi/2$. It is readily appreciated that $TF_I$' is an odd-order nonlinear function with a maximum integral nonlinearity (INL) of $INL_{max}$, whereas $TF_Q$' has both even-order and odd-order nonlinear terms albeit with the same $INL_{max}$. The difference of $TF_I$' and $TF_Q$' shows that I and Q offsets have different effects on the phase distortion when the two-dimensional vector is mapped onto the one-dimensional phase.

A formal analysis can be carried out to derive the nonlinear transfer functions of $TF_I$' and $TF_Q$' and then calculate the total harmonic distortion (THD) and $INL_{max}$, which can specify the nonlinearity in a static and dynamic manner, respectively. However, as we will see, none of nonlinear terms is much more prominent than the other when the input phase full scale is $2\pi$, thus a simplification to a few dominant nonlinear terms doesn't have sufficient accuracy. Therefore, we must resort to simulations to verify the effect of the IQ offset on the $INL_{max}$ and THD.

The $INL_{max}$ of $TF_I$' and $TF_Q$' is the same, and Fig. 4.19(a) shows that $INL_{max}$ increases with the offset for a 6 bit PhADC. When the nonlinearity is quantified in a dynamic manner with a $2\pi$ full-scale sinusoidal input phase, the output spectrum is shown in Fig. 4.20 for a PhADC with an I offset and a Q offset, respectively. The spectrum shows that the I offset only introduces odd-order nonlinearity whereas the Q offset introduces both even and odd-order nonlinearities. Moreover, a Q offset gives rise to greater nonlinearity distortions than an I offset with the same value does, which can be observed in Fig. 4.21 showing THD as a function of the I and Q offset.

The nonlinearity asymmetry of I and Q offset (i.e., different THDs for the same offset value) may lead to the following confusion. In a quadrature receiver system, the defining of the I path and the Q path is arbitrary, and the two paths are completely identical. If a Q offset introduces greater THD than an I offset with the same value does, which one of the two paths should be better designed in practice? This confusion can be resolved as follows. The asymmetry basically arises from using a frequency-domain metric (i.e., THD) to specify

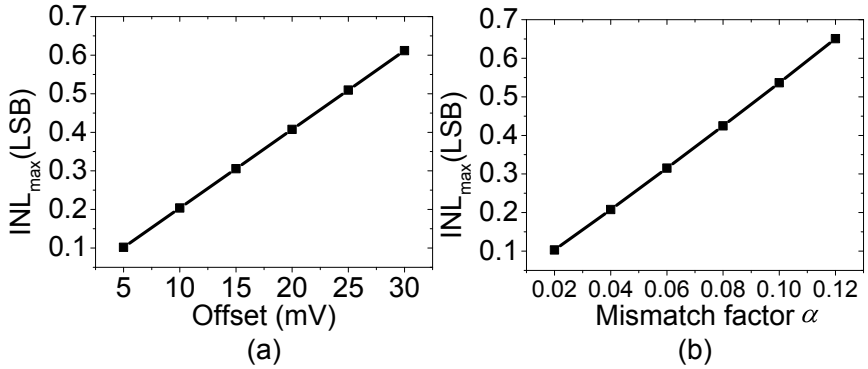



Figure 4.19: $\mathrm{INL}_{\max}$ as a function of (a) I or Q offset, and (b) mismatch factor $\alpha$. The full scale of I and Q signals is 1V. A 6 bit PhADC is assumed.

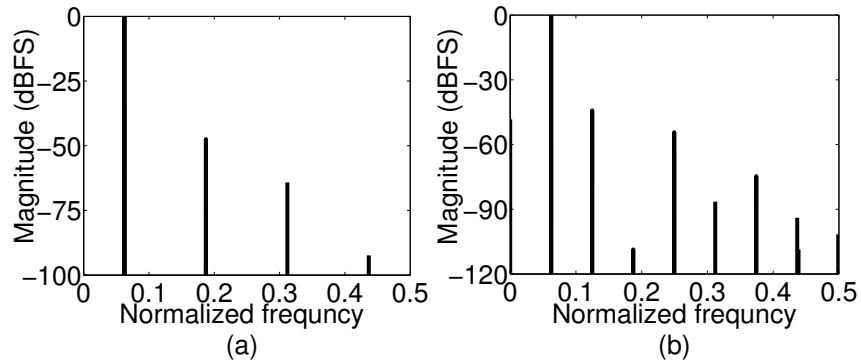



Figure 4.20: Example of phase harmonic distortions due to (a) I offset (10mV), and (b) Q offset (10mV). The full scale of I and Q signals is 1V. Phase quantization noise is not taken into account. The corresponding nonlinear phase transfer functions of (a) and (b) are conceptually shown in Fig. 4.18(a) and Fig. 4.18(b), respectively.

the impact of the I and Q offsets. The asymmetry could disappear if we use other metrics such as $\mathrm{INL}_{\max}$ (Fig. 4.19) or RMS phase error, since both of the two metrics do not depend on the nonlinearity types (even-order or odd-order) of the transfer functions shown in Fig. 4.18, thereby giving no difference between the case with an I offset and the one with a Q offset. From demodulation perspective, using $\mathrm{INL}_{\max}$ or

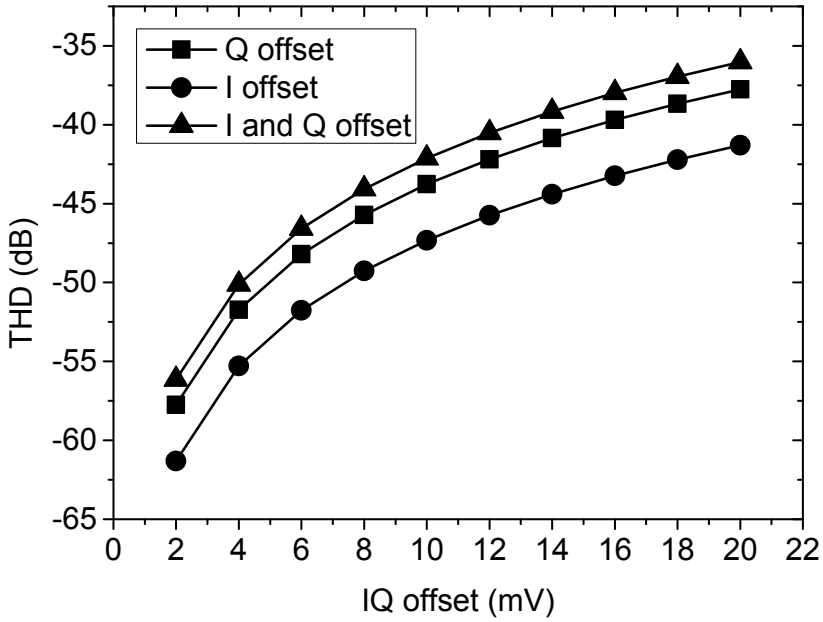



Figure 4.21: THD as a function of I and Q offsets. The full scale of I and Q signals is 1V.

RMS phase error might be more meaningful than using THD, since the overall bit error rate is determined by the average phase error, which has little dependence on the nonlinearity types of the transfer functions shown in Fig. 4.18. Nevertheless, frequency-domain metrics (SNR, SNDR, THD, etc.) are generally most powerful and familiar metrics since they can well represent the impact of most nonidealities such as noise, frequency-dependent effects, etc. Hence, for the sake of consistency, we also use THD in addition to $\mathrm{INL_{max}}$ to specify the impact of the I and Q offset.

A similar analysis can also be applied to examine the effect of IQ amplitude mismatch. As shown in Fig. 4.22, when the I and Q full scale $FS_{\mathrm{I}}$ and $FS_{\mathrm{Q}}$ have a mismatch factor

$$\alpha = 1 - \frac{FS_{\mathrm{I}}}{FS_{\mathrm{Q}}}, \tag{4.38}$$

the vector trajectory is elliptical instead of circular, and the corresponding phase transfer function is an odd-order nonlinear curve $\mathrm{TF_{mis}}$' with $\mathrm{INL_{max}}$ increasing with $\alpha$ [Fig. 4.19(b)]. The output spec-

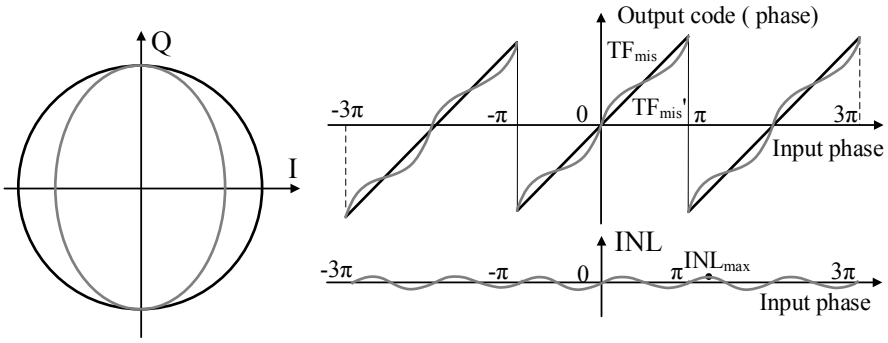



Figure 4.22: Vector trajectory shifting and phase nonlinearities due to IQ amplitude mismatch.

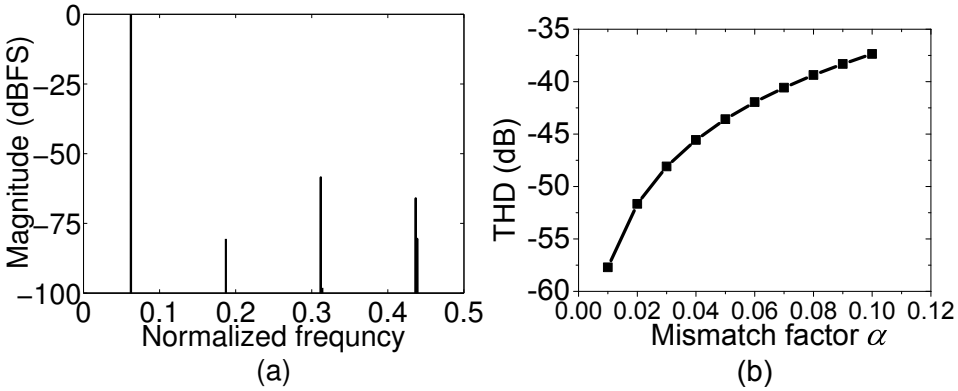



Figure 4.23: (a) Example of phase harmonic distortion due to IQ amplitude mismatch ($\alpha$=0.01). Phase quantization noise is not taken into account. (b) THD as a function of $\alpha$. The corresponding nonlinear phase transfer function of (a) is conceptually shown in Fig. 4.22.

trum of a PhADC suffering from IQ amplitude mismatch is shown in Fig. 4.23(a) and the resulting THD is plotted versus mismatch factor $\alpha$ in Fig. 4.23(b).

This section reveals that, during the conversion of a two-dimensional vector to a one-dimensional phase, both offsets and mismatch of the amplitude can be transferred into nonlinearities of the phase.

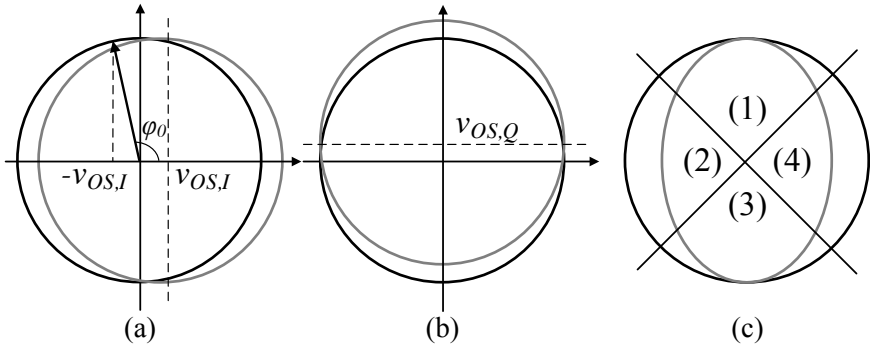



Figure 4.24: Vector distribution imbalance caused by (a) I offset, (b) Q offset and (c) IQ amplitude mismatch.

### 4.5.4 IQ offsets and IQ amplitude mismatch detection

The above analysis shows that nonlinearities introduced by offset and amplitude mismatch may significantly degrade the phase SNR of a PhADC, thereby dictating proper techniques to detect and calibrate the offset and the mismatch. A mixed-signal approach, i.e., detecting the offset and the mismatch in the digital domain and calibrate them in the analog domain is usually incorporated in a system with an IQ ADC. Similarly, a digital phase-domain detection principle is proposed for the PhADC as well in this section, offering a possibility for calibration in the analog domain.

The principle can be conceptually described by Fig. 4.24(a). Assume a circular vector trajectory is shifted to the right side of the complex plane by a positive I offset. In such a case, there are more vectors in the right half of the plane than in the left half if originally all vectors are evenly distributed along the circle. Therefore, the amplitude and sign of the I offset can be estimated by detecting the distribution density of the vectors in the right and left half planes. This principle holds also true for the Q offset when detecting the distribution density in the top and bottom half planes as shown in Fig. 4.24(b), as well as for the amplitude mismatch when detecting the density in Regions (1), (2), (3) and (4) as shown in Fig. 4.24(c). Thus, the amplitude mismatch and the offset detection can both be realized by a simple density analysis process in the digital domain without too much extra

effort.

We now formulate the imbalance by taking the example of the I offset in Fig. 4.24(a). Due to the offset $v_{\mathrm{OS,I}}$, phase $\varphi_0$ is now shifted to $\frac{\pi}{2}$, indicating that all vectors between $[-\varphi_0, \varphi_0]$ are now in the right half of the shifted vector circle. Hence, the distribution imbalance between the right and left half planes is:

$$\mathrm{IMB_{OS}} = \frac{2\varphi_0}{2\pi} - \frac{2(\pi - \varphi_0)}{2\pi} = \frac{2\varphi_0}{\pi} - 1. \tag{4.39}$$

Substituting $\varphi_0 = \frac{\pi}{2} + \arcsin\frac{v_{\mathrm{OS,I}}}{FS/2}$ into (4.39), we get:

$$\mathrm{IMB_{OS}} = \frac{2\arcsin\frac{v_{\mathrm{OS,I}}}{FS/2}}{\pi} \approx \frac{4v_{\mathrm{OS,I}}}{\pi \cdot FS}. \tag{4.40}$$

This equation holds also true for the distribution imbalance between the top and bottom half planes if $v_{\mathrm{OS,I}}$ is replaced by Q offset $v_{\mathrm{OS,Q}}$.

Regarding the IQ amplitude mismatch, as shown in Fig. 4.24(c), its effect is the distribution imbalance between Regions (1) + (3) and Regions (2) + (4), denoted by $\mathrm{IMB_{mis}}$. Similar calculations as (4.39) and (4.40) apply to $\mathrm{IMB_{mis}}$ and yield:

$$\mathrm{IMB_{mis}} = 1 - \frac{4\arctan(1-\alpha)}{\pi}. \tag{4.41}$$

Simulation results in Fig. 4.25 show that the distribution imbalance increases with offset and amplitude mismatch, which is consistent with (4.40) and (4.41).

The above analysis provides an effective approach to detect the IQ offset and the IQ amplitude mismatch in the digital domain, enabling the possibility to calibrate them in the analog domain, which is usually necessary in a receiver system. Note that, in order to calculate the absolute value of the offsets, one of $FS_{\mathrm{I}}$ and $FS_{\mathrm{Q}}$ should be available (the other one can be calculated from the known one, $\alpha$ and (4.38)), as indicated by (4.40). This can be accomplished by employing one auxiliary amplitude ADC in the calibration procedure.

## 4.6 Conclusions

In this chapter, both the IQ ADC and the PhADC are formulated from a phase SNR point of view, which facilitates a comparison between

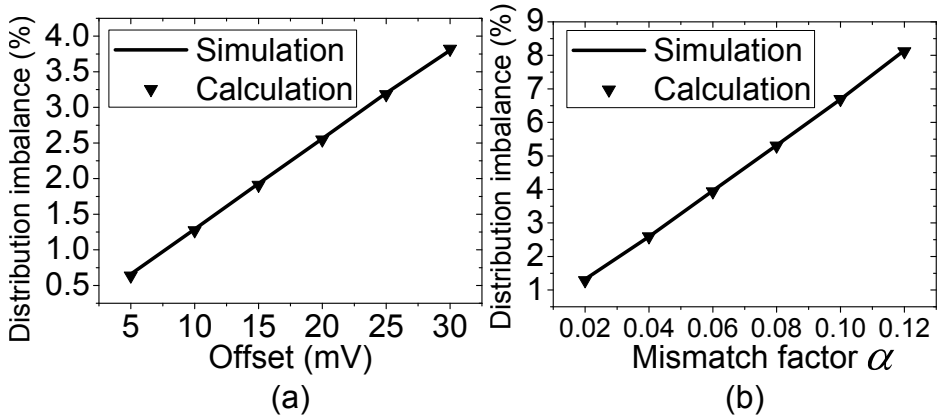



Figure 4.25: Vector distribution imbalance as a function of (a) IQ offset (the full scale of I and Q signals is 1V) and (b) IQ amplitude mismatch.

the two ADCs. The theoretical comparison together with state-of-the-art silicon implementations of both ADCs leads to the following observations:

1. In comparison with an IQ ADC, a PhADC, due to its embedded demodulation attribute, is a more compact quantization and demodulation solution when interference accommodation is not required.

2. After many decades of research, today's IQ ADCs are more energy-efficient than the emerging PhADC. However, we want to address the fundamental energy difference between them, hence showing the room for improvement we could explore. In the typical operating condition of a PhADC, i.e., low phase resolution with no need to accommodate the interference, a PhADC has a lower theoretical energy limit than an IQ ADC for a given phase ENOB, thereby showing the great room for energy efficiency improvement that the emerging PhADC has.

Having discussed the interesting attributes of the PhADC, we proposed an IQ-assisted conversion algorithm and a corresponding circuit topology to improve the energy efficiency of the PhADC. Thanks to the successive approximation (SAR)-like algorithm and charge-domain

operation, the prototype achieves a FoM of 1.2 pJ/step, which is better than the state-of-the-art of 8.3 pJ/step.

Explicit relationship between the input amplitude SNR and the output phase SNR of the PhADC has been formulated. This relationship facilitates the system analysis of a receiver using a PhADC. We elaborate on this point in Chapter 5.

Finally, this chapter reveals that, for a PhADC, IQ offset and IQ mismatch are translated into phase nonlinearity. In order to provide a cancellation possibility for the offset and mismatch, a simple mismatch and offset detection technique in the phase domain has been proposed and then verified principally.

# Chapter 5

# A 402 MHz receiver for IEEE 802.15.6 WBAN standard

## 5.1 Introduction

Chapters 3 and 4 demonstrate the performance of the proposed passive front-end (PFE) and the charge-redistribution phase-domain analog-to-digital convertor (PhADC), respectively. In this Chapter, the PFE and the PhADC are used to construct a receiver system. A programmable-gain amplifier (PGA) and a $2^{nd}$-order filter are designed to link the PFE and the PhADC. Using the performance specifications of the circuitry together with the analysis outcomes of the PhADC presented in Chapter 4, the benefit of using the PhADC for a receiver system is studied. Like the PFE, the system also aims to comply with the specifications of the 402-405 MHz band of the IEEE 802.15.6 standard.

## 5.2 System implementation

A receiver system with the proposed PFE and the PhADC is depicted in Fig. 5.1. The analog baseband section consists of a PGA and a $2^{nd}$-order filter. The PGA provides sufficient and adjustable voltage gain to accommodate time-varying input RF signal amplitudes. Although the PFE, baseband low-noise amplifier (BB LNA) and PGA

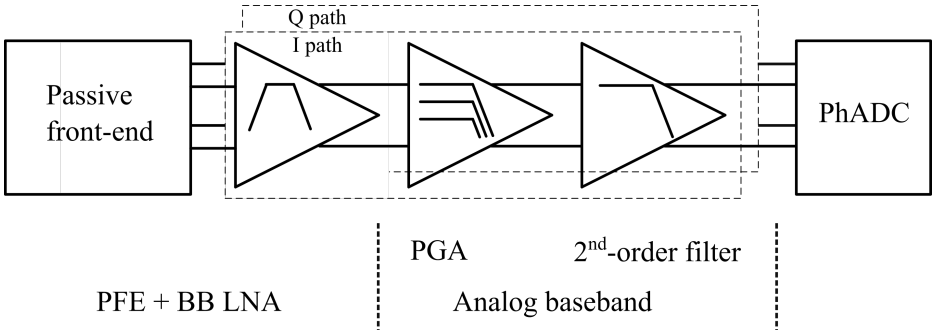



Figure 5.1: A receiver system with a PFE and a PhADC.

can suppress out-of-band or even out-of-channel interference, a $2^{nd}$-order filter is necessary to attenuate the close adjacent and alternate channel interference [20]. The performance of the analog baseband section is characterized by simulations.

The PGA circuit topology is shown in Fig. 5.2. The amplifier employs a $g_m$-boosted differential pair with source degeneration [20, 71]. In this configuration, the passband gain is determined by the degeneration resistor $R_d$, output resistor $R_O$, and the current ratio of the two stages (4:1 here), which is $R_O/2R_d$ for this implementation. Gain programmability is obtained by controlling switch-resistor $R_d$, which has a range of 1.56 kΩ to 100 kΩ. For a constant $R_O$ of 400 kΩ, the PGA has a programmable gain of 6 dB to 42 dB in steps of 6 dB. The bandwidth of the PGA is larger than that of the filter so as to make the filter dominate the overall bandwidth, which is characterized in the following description. An offset cancellation current source is connected in parallel with the bias current sources of the first stages to compensate the offsets of the receiver chain. No automatic cancellation mechanism has been provided in this implementation.

The $2^{nd}$-order filter employs a Sallen&Key topology, as shown in Fig. 5.3 [20]. The cut-off frequency is given by $1/2\pi\sqrt{R_1R_2C_1C_2}$ for the topology. In this implementation, $C_1$ and $C_2$ are chosen to be 832 fF and 416 fF, respectively, while $R_1$ and $R_2$ have a nominal value of 600 kΩ, giving a nominal cut-off frequency of 450 kHz. This value is larger than the desired 150 kHz to account for the limited bandwidth of preceding stages as well as the parasitic capacitance of the filter. Both $R_1$ and $R_2$ have a 2 bit calibration range to compensate for

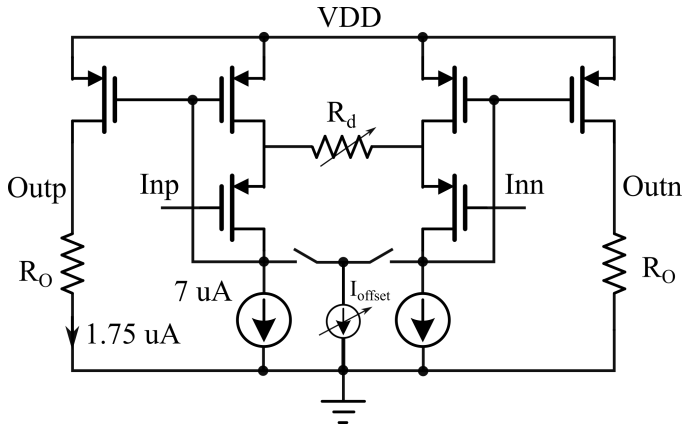



Figure 5.2: PGA circuit.

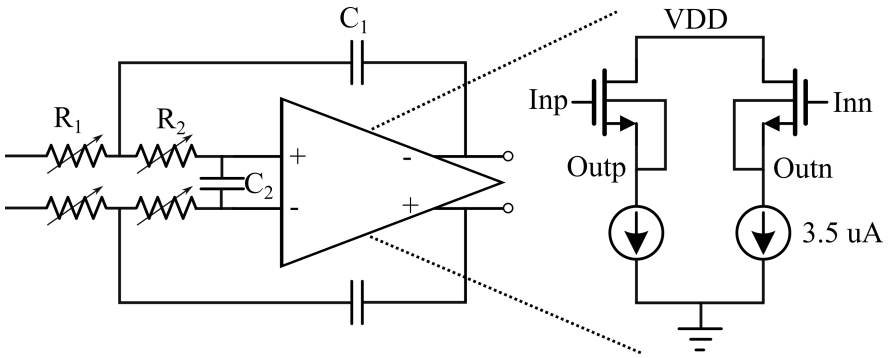



Figure 5.3: 2nd-order Sallen&Key filter.

process variations. The unity-gain amplifier deploys a simple and low power source-follower topology. The body of the deep N-well NMOS is tied to its source to provide an unity gain and good intrinsic linearity. The source follower also shifts the common-mode voltage of both input signals down to a proper level for the subsequent PhADC.

The simulated overall frequency response and input-referred noise spectral density of the cascaded PGA and filter are shown in Fig. 5.4 and Fig. 5.5, respectively. The on-resistances of the switches being used by $R_d$ yield a small error in the resistance value of $R_d$, which becomes more pronounced as $R_d$ decreases. Due to this resistance error of $R_d$ as well as the limited loop gain, the larger high passband gains are a bit less than the desired gain settings. The 3-dB bandwidths of the frequency responses are 141 kHz. The integrated noise voltage

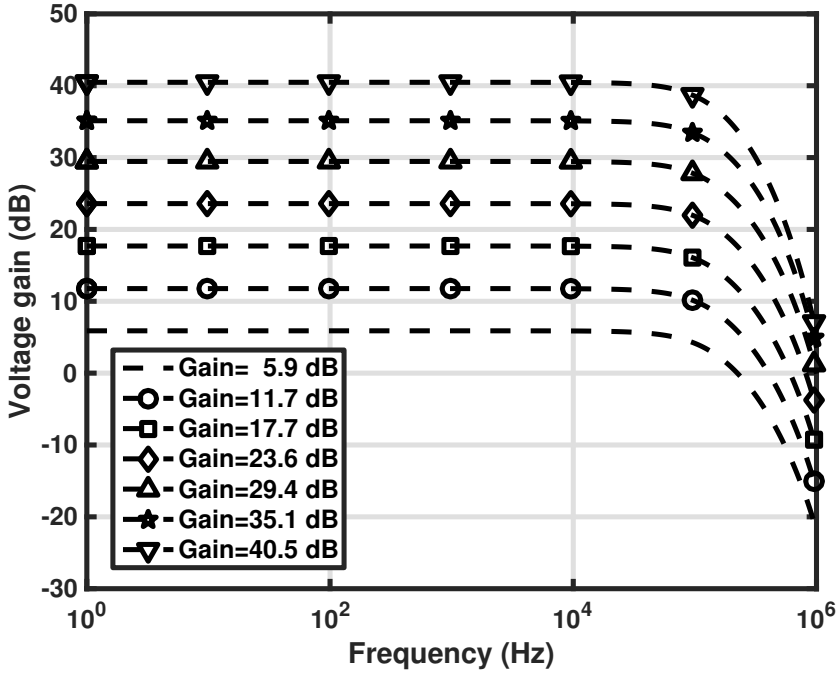



Figure 5.4: Overall frequency response (magnitude only) of cascaded PGA and filter for various gain settings.

over 150 Hz-150 kHz varies from 35.9 $pV^2_{rms}$ to 5.6 $nV^2_{rms}$ for different gain settings.

## 5.3 System performance

Taking into account the measured performance of the PFE and BB LNA presented in Chapter 3, the overall NF and $IIP_3$ preceding the charge-redistribution PhADC are shown in Fig. 5.6. As an example, we consider the performance at the highest gain setting (i.e., 77.1 dB) for the following system evaluation.

We first translate the phase SNDR of the PhADC into an equivalent amplitude SNR, which is a more familiar measure for the preceding stages. Eqn. (4.28) establishes a relationship between phase SNR and amplitude SNR for an ideal PhADC. This relationship can be used to transform a nonideal PhADC into an ideal PhADC with a limited input amplitude SNR, as illustrated in Fig. 5.7. Note that the

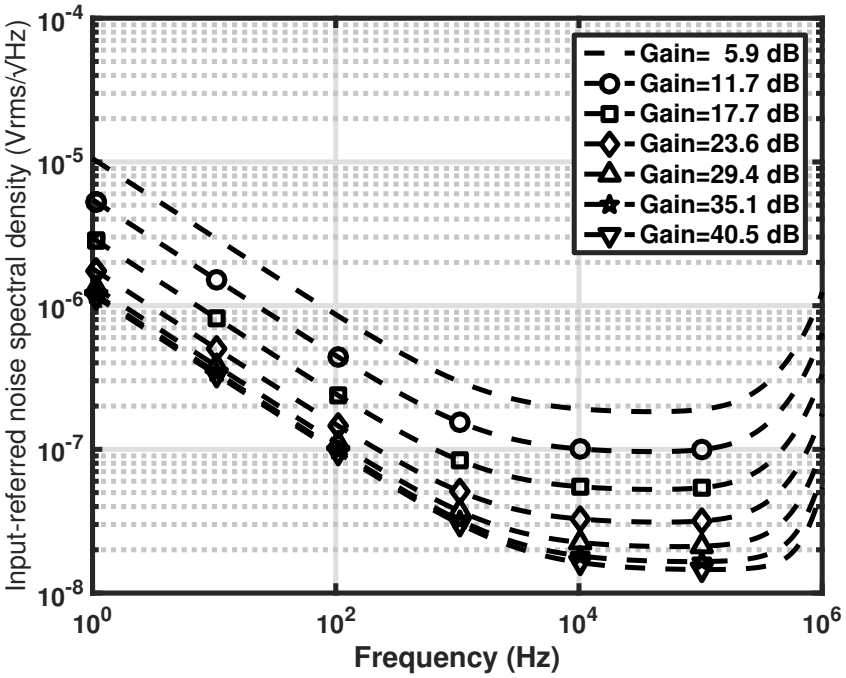



Figure 5.5: Input-referred noise spectral densities of the cascaded PGA and filter for various gain settings.

modeling shown in Fig. 5.7 is most valid when the phase nonidealities manifest themselves only as phase noise without other nonidealities such as phase distortion. This is because the input amplitude noise of an ideal PhADC manifests itself only as phase noise at the output as long as the input SNR is not too small, i.e., higher than 6.5 dB as addressed in [70]. As shown in Fig. 4.14(b), the output phase SNDR of the presented PhADC is dominated by phase noise rather than phase distortion if the input frequency is below the ERBW. Thus, we consider that the modeling shown in Fig. 5.7 is valid for the analysis in this section.

As mentioned in Section 4.4.3, the phase SNDR of the PhADC reduces only 3 dB as the input amplitude decreases 9.5 dB, due to its immunity to amplitude variations. This property proves beneficial to the sensitivity of the system. We elaborate on this point in the following performance study.

We first set the signal level at the PhADC input to full scale, which

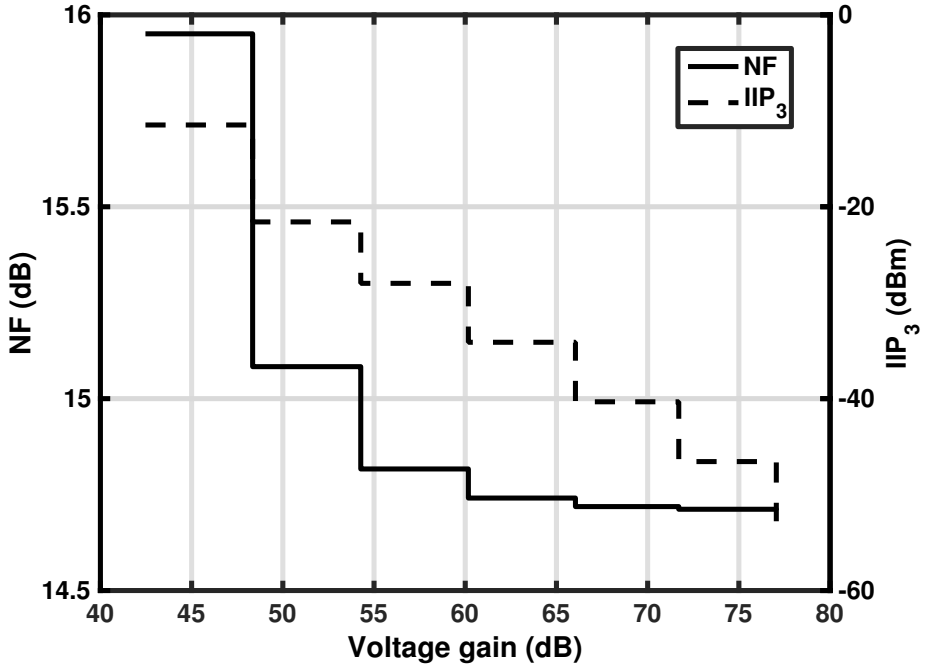



Figure 5.6: Overall NF and $IIP_3$ preceding PhADC.

is 1 Vpp (equivalent to +4 dBm in a 50 Ω system) for the proposed 1.2 V system. The corresponding antenna input level for the highest gain setting is -73.1 dBm. Fig. 5.8(a) shows the system performance at this input signal level. The phase SNDR of the PhADC is 30.8 dB as shown in Fig. 4.14, which is equivalent to that of an ideal PhADC with an input signal of +4 dBm and an input-referred amplitude noise of -16.8 dBm, as indicated by Eqn. (4.28). The input-referred amplitude noise is the equivalent of the phase nonidealities of the PhADC, e.g., the phase quantization noise and the phase nonlinearity. The noise level at the output of the analog BB is -27.5 dBm, and the total noise at the interface of the analog BB and the PhADC is -16.4 dBm (the sum of -16.8 dBm and -27.5 dBm). Thus, the overall SNR at the interface is 20.4 dB (= +4 dBm + 16.4 dBm). Note that we have not considered the intermodulation product generated by the adjacent-channel interference at the moment.

We then set the signal level at the PhADC input to the lowest of the measured range, i.e., -6.5 dBm (0.3 $V_{PP}$), as shown in Fig. 5.8(b). The resulting output phase SNDR is 26.6 dB as shown in Fig.

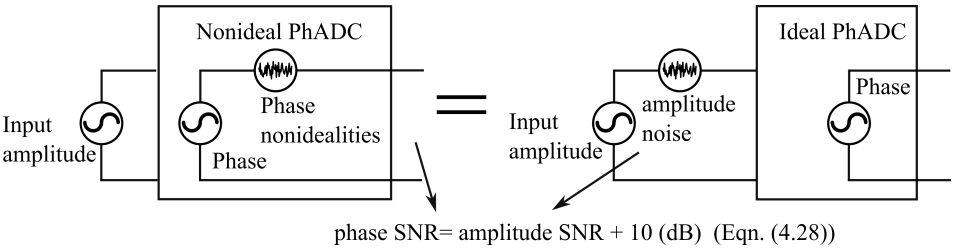



Figure 5.7: Modeling an nonideal PhADC by an ideal PhADC with limited input amplitude SNR.

4.14, and the equivalent input amplitude noise of the PhADC is -23.1 dBm as indicated by Eqn. (4.28). Comparing this equivalent input amplitude noise level (-23.1 dBm) with that shown in Fig. 5.8(a) (-16.8 dBm), it is important to note that the noise level decreases with the signal level, which is a favorable effect introduced by the PhADC's immunity to amplitude variations. While this property of the PhADC has been studied in detail in Section 4.2.2, we provide here a direct explanation of the above favorable effect to avoid repetition from the previous chapter.

Since the phase of a pair of quadrature signals does not depend on their amplitudes, the output phase SQNR of an ideal N bit PhADC does not depend on the input amplitudes and only relies on the N bit resolution. Considering the relationship shown by Eqn. (4.28), we know that the equivalent input amplitude SNR of the ideal N bit PhADC is constant, and hence the equivalent input amplitude noise decreases with the input signal level. By contrast, the equivalent input amplitude noise of an ideal N bit amplitude ADC is constant and does not decrease with the input signal level. For a system using the PhADC, the dependence of the equivalent input amplitude noise (of the PhADC) upon the input signal level is beneficial to the sensitivity of the system since the input-referred noise decreases as the received signal gets weak. This statement can be better understood with the aid of the numerical results shown in Fig. 5.8(a) and (b). The overall amplitude SNR at the PhADC input is 20.4 dB in Fig. 5.8(a) for an antenna input of -73.1 dBm. When the antenna input is reduced to -83.6 dBm as shown in Fig. 5.8(b), the overall amplitude SNR would be reduced to 9.9 dB for a system using an amplitude ADC, while it is 15.3 dB for the presented system as shown in Fig. 5.8(b),

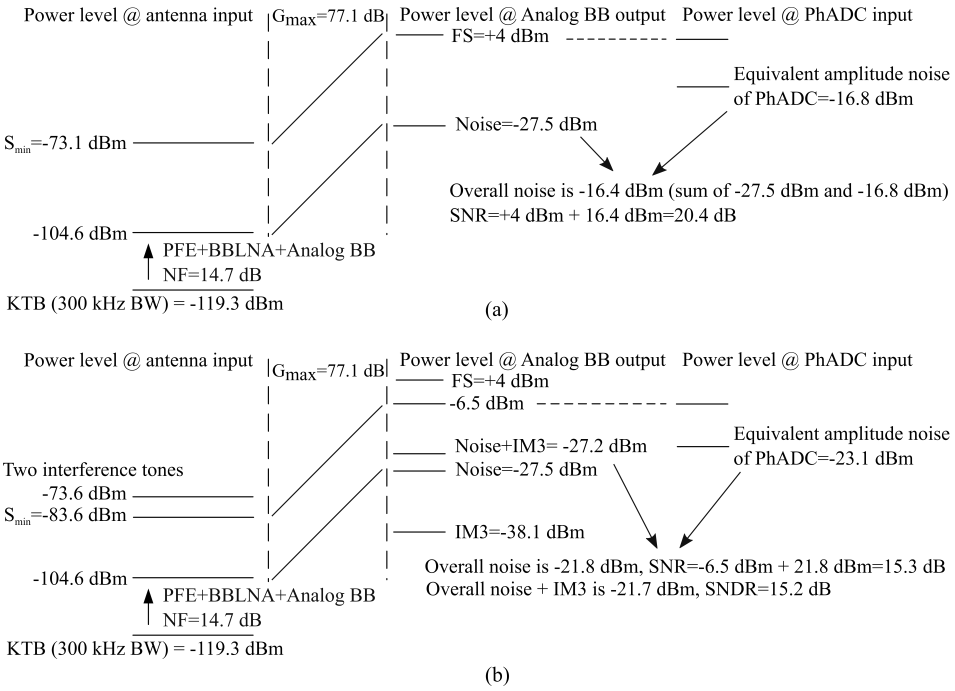



Figure 5.8: System performance evaluation for an input level of (a) -73.1 dBm and (b) -83.6 dBm.

thereby allowing a weaker antenna input than the system using the amplitude ADC does. Note that the phase SNR of the presented PhADC still drops by 4.2 dB rather than remaining constant as the input amplitude reduces from +4 dBm to -6.5 dBm. This is because the amplitude nonidealities, such as noise and offset, become more pronounced as the input amplitude decreases, thereby degrading the output phase quality.

More generalized conclusions can be drawn from Fig. 5.9, which is a conceptual illustration of the amplitude SNR requirements for a PhADC and an amplitude ADC. We assume a weakest possible signal at the ADC input, which corresponds to the scenario of a desired-sensitivity-level signal at the system input and the greatest amplification preceding the ADC. The required amplitude SNR of a PhADC is the ratio between the weakest input signal and the noise budget of the PhADC, while that of an amplitude ADC is the ratio between the full scale and the noise budget of the amplitude ADC. Obviously, the

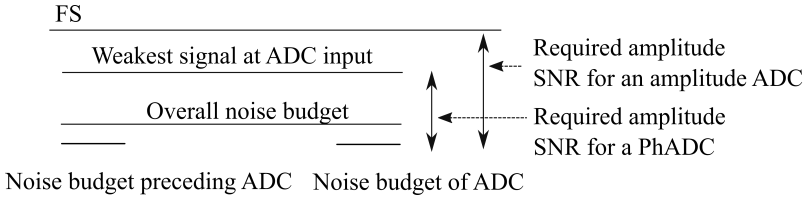



Figure 5.9: Conceptual illustration of the amplitude SNR requirements for a PhADC and an amplitude ADC.

former one is more relaxed than the latter one, suggesting that the PhADC needs a smaller amplitude dynamic range than the amplitude ADC does to meet a given sensitivity requirement. The difference between the two required amplitude SNR depends on several system parameters. We use some of the performance numbers described above to give a numerical example.

As required by the IEEE 802.15.6 standard, the desired sensitivity level is -89 dBm, which can be amplified to -11.9 dBm by the proposed PFE and the analog BB. Considering the noise level of -27.5 dBm preceding the ADC and the required SNR of 12 dB by the standard, the input-referred noise budget of the ADC is -26.4 dBm if other sources of nonidealities are not considered. This noise budget translates to a required amplitude SNR of 30.4 dB for an amplitude ADC. By contrast, the noise budget translates to a required equivalent amplitude SNR of 14.5 dB for a PhADC, which is equal to a phase SNR of 24.5 dB when the input signal amplitude is -11.9 dBm as indicated by Eqn. (4.28).

In summary, due to the PhADC's immunity to input amplitude variations, the PhADC needs a smaller equivalent amplitude dynamic range than the amplitude ADC does to meet a given sensitivity requirement of the receiver system. For the proposed PFE and the IEEE 802.15.6 application, two ADCs (for I and Q paths) with a SNR of 30.4 dB are needed if an amplitude ADC is used, while one PhADC with a phase SNR of 24.5 dB (when the input amplitude is -11.9 dBm) is sufficient if a PhADC is used.

After revealing the benefit of using the PhADC for a receiver system, we now evaluate the overall performance of the proposed receiver. We set the signal level at the PhADC input to the lowest of the measured range, i.e., -6.5 dBm (0.3 $V_{PP}$), as shown in Fig. 5.8(b). For a

maximum gain of 77.1 dB (36.6 dB of PFE+BB LNA and 40.5 dB of analog BB), the -6.5 dBm translates to an antenna input signal level of -83.6 dBm. This is 5.4 dB higher than the desired sensitivity level of -89 dBm of the IEEE 802.15.6 standard. Unfortunately, we could not evaluate the scenario with an antenna input weaker than -83.6 dBm due to the fact that the PhADC has not been specified for the input below 0.3 $V_{PP}$. The overall SNR is evaluated at the interface of the analog BB and the PhADC. As required by the IEEE 802.15.6 standard, the adjacent interference level is chosen to be 10 dB higher than the sensitivity level. The alternate interference is set to the same level as the adjacent one. With an $IIP_3$ of -52.8 dBm, the interference generates an IM3 product of -38.1 dBm, which is 10.5 dB lower than the noise floor preceding the PhADC. Adding up all of the noise, IM3 product and the equivalent amplitude noise of the PhADC at the interface, an SNDR of 15.2 dB is achieved, which is higher than, and thus fulfills, the SNR of 12 dB required by the IEEE 802.15.6 standard for $\pi/4$-DQPSK demodulation with a BER of $10^{-5}$. DC offset is of course a concern for this direct-conversion receiver. Assuming the DC offset generated by the mixer is strongly suppressed by the bandpass BB LNA, the DC offset of the BB LNA and analog BB has a simulated standard deviation $\sigma$ of 3.4 mV for the minimum gain and 23 mV for the maximum gain. This offset can be manually compensated at the interface described in Section 5.2.

## 5.4 Conclusions

This chapter presents a receiver system using the passive receiver front-end and the charge-redistribution PhADC proposed in Chapters 3 and 4 respectively. Using the measured performance of the front-end and the PhADC, the simulated performance of the PGA and the $2^{nd}$-order filter and the analysis outcomes of the PhADC presented in Chapter 4, the benefit of using the PhADC for a receiver system is estimated. Due to the PhADC's immunity to input amplitude variations, the PhADC needs a smaller equivalent amplitude dynamic range than the amplitude ADC does to meet a given sensitivity requirement of the receiver system. For the proposed PFE and the IEEE 802.15.6 application, two ADCs (for I and Q paths) with an SNR of 30.4 dB

are needed if an amplitude ADC is used, while a PhADC with a phase SNR of 24.5 dB (when the input amplitude is -11.9 dBm) is sufficient if a PhADC is used. For an antenna input level of -83.6 dBm (which corresponds to the minimum input level that has been specified for the PhADC), the presented receiver system demonstrates an overall SNDR of 15.2 dB, which is 3.2 dB higher than, and thus fulfills, the 12 dB SNR required by the IEEE 802.15.6 standard.

# Chapter 6

# Conclusions and future work

## 6.1 General conclusions

This dissertation focuses on low-power techniques for a short-range receiver. The freedom of antenna impedance and the phase-only modulation property of FSK/PSK signals are exploited in the pursuit of low power consumption. In Chapter 1, the motivation for the above two perspectives is addressed by studying state-of-the-art low-power receivers, followed by the challenges and objectives of this dissertation.

In Chapter 2, the feasibility of using a non-50 Ω antenna impedance for an active receiver front-end is studied. A general co-design principle is first presented for electrically-short antenna-electronics interfaces. It is argued that power transfer is not the only design objective in these interfaces, but that the impedances of antenna and load need to be optimized for either voltage or current, depending on which is more favorable to measure with the electronics. The first condition is to conjugate match the antenna-electronics interface as this maximizes both the voltage and current at the load. The second condition is to determine at which impedance level conjugate matching should occur in order to further increase the load voltage or current. This design principle has been applied to a co-design example of an inductive antenna impedance and a low-noise amplifier (LNA). A passive voltage gain can be achieved by using the proposed principle, and hence NF can be reduced without sacrificing power consumption.

In Chapter 3, the feasibility of using a non-50 Ω antenna impedance for a passive receiver front-end is studied. As described in Chapter 2,

an inductive antenna impedance proves beneficial for increasing the passive voltage gain of an antenna-LNA interface. Chapter 3 aims for the same voltage-boosting effect by incorporating the inductive antenna impedance in a passive front-end (PFE). The analysis in Chapter 3 reveals that the inductive antenna impedance introduces two extra degrees of freedom, i.e., antenna resistance $R_A$ and antenna inductance $L_A$, to increase the downconverted voltage of the front-end for a given antenna available power. In order to well maintain the passive voltage gain offered by the inductive antenna impedance together with its resonant load, the passive mixer should present a high-quality-factor capacitive input. This is achieved by incorporating an intermediate inductance in the passive network. Analytical methods for the desired signal transfer and noise behavior of the proposed PFE are presented to facilitate the design. The proposed front-end and a baseband LNA are implemented to verify the voltage-boosting effect. The implementation has a passive voltage gain of 11.6 dB, which is close to the state-of-the-art of 12 dB.

Chapter 4 deals with the analysis and design of phase-domain analog-to-digital converters (PhADCs). First of all, a thorough comparison of PhADCs and (in-phase and quadrature) IQ ADCs is presented. Compared to an IQ ADC, a PhADC, due to its embedded demodulation attribute, is a more compact quantization and demodulation solution when interference accommodation is not required. For the energy efficiency comparison of the two ADCs, considering a flash ADC as an example of the low resolution (3-4 bit) IQ ADC, the PhADC has a lower theoretical energy limit than the flash IQ ADC for a given phase ENOB due to the immunity to magnitude variations and the phase-only quantization, thereby showing the great room for energy efficiency improvement that the emerging PhADC has. Second, having discussed the interesting attributes of the PhADC, we propose an IQ-assisted conversion algorithm and a corresponding circuit topology to improve the energy efficiency of the PhADC. Thanks to the successive approximation (SAR)-like algorithm and charge-domain operation, the prototype achieves a FoM of 1.2 pJ/step, which is better than the state-of-the-art of 8.3 pJ/step. Finally, the explicit relationship between the input amplitude SNR and the output phase SNR of the PhADC has been formulated. This relationship facilitates the system analysis of a receiver using a PhADC.

Using the PFE and the charge-redistribution PhADC proposed in Chapter 3 and Chapter 4 respectively, a receiver system is constructed in Chapter 5. Based on the measured performance of the front-end and the PhADC, the simulated performance of a PGA and a $2^{nd}$-order filter and the analysis outcomes of the PhADC presented in Chapter 4, the benefit of using the PhADC for a receiver system is quantified. For the proposed PFE and the IEEE 802.15.6 application, two ADCs (for I and Q paths) with a SNR of 30.4 dB are needed if an amplitude ADC is used, while a PhADC with a phase SNR of 24.5 dB (when the input amplitude is -11.9 dBm) is sufficient if a PhADC is used. For an antenna input level of -83.6 dBm (which corresponds to the minimum input level that has been specified for the PhADC), the presented receiver system demonstrates a sufficient overall SNR for the IEEE 802.15.6 standard, thereby paving the way to fully-integrated low-power receivers for the standard.

## 6.2 Original contributions

- The co-design principle of a non-50 Ω antenna impedance and an LNA. (Chapter 2)

- Analytical methods and design of a passive receiver front-end using an inductive antenna impedance. (Chapter 3)

- A mathematical analysis of PhADCs and IQ ADCs from the phase domain point of view. (Chapter 4)

- An IQ-assisted algorithm and the design of a charge-redistribution PhADC. (Chapter 4)

- Silicon implementations of the passive receiver front-end and the charge-redistribution PhADC in AMS 0.18 $\mu$m CMOS technology. (Chapters 3 and 4)

- Quantification of the benefit of using a PhADC for a receiver system. (Chapter 5)

## 6.3 Recommendations for future work

Several topics deserving further investigation are the following.

A practical issue of using an inductive antenna for a receiver system is the measurement complexity. Precisely controlling and specifying the signal level as well as noise level at the input of an antenna proves very challenging. Thus, a reliable measurement method for a non-50 Ω antenna-based system is valuable and needs more investigation.

The passive receiver front-end presented in Chapter 3 employs several off-chip passive components. It is therefore interesting to implement them fully on chip. Several challenges as well as benefits may arise from such an on-chip implementation. First of all, the quality factors and inductance values of the on-chip passive inductors will be poorer than those of their off-chip counterparts. Second, a single-balanced passive mixer might be more feasible than the double-balanced topology used in the proposed front-end, because the former requires only one inductor at the mixer input while the latter needs two. Finally, the on-chip implementation is expected to suffer less from the parasitic capacitances of PCB tracks, IO pads, etc.

We used a qualitative approach to analyze the noise behavior of the proposed passive front-end in Chapter 3. Formulating the noise folding behavior of a passive mixer with arbitrary source and load impedances would be valuable.

An IQ amplitude mismatch and offset detection technique for PhADCs is proposed and verified principally in Chapter 4. Using the proposed technique, the amplitude offset and mismatch of a receiver using a PhADC can be estimated by detecting the phase imbalance among the four phase quadrants after the analog-to-phase conversion. A feedback path can therefore be constructed between the PhADC output and an offset/mismatch compensation interface of the receiver. The closed loop will help the compensation interface settle to the proper compensation values of the offset and mismatch. Incorporating this cancellation loop in a receiver system can improve its sensitivity.

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# List of Publications

## Journal Papers

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2. Leila Rajabi, Mehdi Saberi, **Yao Liu**, Reza Lotfi, and Wouter A. Serdijn, "A Charge-Redistribution Phase-Domain ADC Using IQ-Assisted Binary-Search Algorithm," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, early access, publication year: 2017.

3. Mark Stoopman, **Yao Liu**, Hubregt J. Visser, Kathleen Philips and Wouter A. Serdijn, "Co-Design of Electrically-Short Antenna-Electronics Interfaces in the Receiving Mode," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol.62, no.7, pp. 711-715, July 2015.

4. **Yao Liu**, Reza Lotfi, Yongchang Hu and Wouter A. Serdijn, "A Comparative Analysis of Phase-Domain ADC and Amplitude-Domain IQ ADC," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 62, no. 3, pp. 671-679, March 2015.

## Conference Proceedings

1. **Yao Liu**, Duan Zhao, Yongjia Li and Wouter A. Serdijn, "A 5b 12.9$\mu$W Charge-redistribution Phase-domain ADC for Low Power FSK/PSK Demodulation," *Proc. IEEE European Solid State Circuits Conference (ESSCIRC)*, Venice, Italy, pp.275-278, 22-26 Sept. 2014.

2. **Yao Liu** and Wouter A. Serdijn, "An LNA With Optimally Mismatched Antenna Interface for Energy Harvesting Sensor Nodes," *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, Beijing, China, pp.1853-1856, 19-23 May 2013.

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