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# Study on Characteristics and UIS of Hexagonal Planar SiC VDMOSFETs With Varied JFET Width

Hou-Cai Luo, Huan Wu, Jing-Ping Zhang, Bo-Feng Zheng, Lei Lang, Guo-Qi Zhang, *Fellow, IEEE*, and Xian-Ping Chen, *Member, IEEE*

***Abstract*—The hexagonal cell topology of planar SiC VDMOSFETs with varied JFET width ($L_{JFET}$) are designed and manufactured in this study. $L_{JFET} = 1.4\mu m$ has the best HF-FOM ($R_{on}\times C_{gd}$) and HF-FOM ($R_{on}\times Q_{gd}$) by comparing the dynamic and static parameters of each design. Besides, the UIS reliability and failure mechanism for series designs are investigated by experiment and TCAD simulation. The results show that the high temperature is generated by energy dissipation during avalanche and it drives the parasitic BJT conduction, causing $I_{ds}$ out of control and instantaneous heat concentration in a very short time. The extremely high temperature causes internal cracking of the material and metal melting, resulting in gate-source short circuit and device damage. It would provide suggestions for device design and reliability consideration.**

***Index Terms*—SiC VDMOSFET, hexagonal cell topology, avalanche reliability, BJT, UIS.**

## I. INTRODUCTION

SILICON carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFETs) present one of excellent potential candidates to replace silicon-based insulated gate bipolar transistors (Si IGBTs) in power electronics due to their fast switching frequency, low dissipating power, high thermal conductivity, and large current density [1]. These outstanding features of SiC MOSFETs are due to the properties of SiC material. There are wider band gap, higher thermal conductivity, larger critical electric field strength in SiC material compared with that of Si. Due to these exceptional properties, SiC MOSFETs have significant potential in power systems, such as electric vehicles, charging stations, and photovoltaic inverters [2]. Over the years, advancements in design and fabrication technology have led to the commercialization of SiC MOSFETs in the power electronics market.

Two main technology directions exist in SiC MOSFETs, distinguished by differences in their gate electrode structure: planar gate structure (simplified SiC VDMOSFET) and trench gate structure (simplified SiC UMOSFET) [3]. In comparison to SiC VDMOSFETs, SiC UMOSFETs exhibit higher power density and lower ON-resistance. However, the SiC UMOSFETs are less robust in the blocking state as the gate oxide has to withstand a higher electric field. The gate oxide electric field in planar SiC VDMOSFETs is substantially decreased by reducing the distance between the two P-Based regions, also known as JFET width, abbreviated as $L_{JFET}$ in this study. The conductivity of SiC VDMOSFETs is decrease as the narrow $L_{JFET}$. However, the electric field strength maintained by the gate oxide during the avalanche breakdown condition would increase as the $L_{JFET}$ increases. If the $L_{JFET}$ is too large, the device may easily suffer damage from gate oxide breakdown [4]. The $L_{JFET}$ geometric parameter is critical in balancing the conduction characteristics and reliability of SiC VDMOSFETs [5]. Moreover, the characteristics of SiC VDMOSFETs are not only impacted by $L_{JFET}$, but also by different cell topologies. Compared to the linear strip distribution, the hexagonal topology distribution provides a higher cell density and improves conduction characteristics in SiC VDMOSFETs according to previous studies [6], [7]. In the case of 1.2kV SiC VDMOSFETs with $L_{JFET} = 1.4\mu m$, the hexagonal topology demonstrates 58.7% lower specific ON resistance compared to the linear topology [8]. Therefore, the hexagonal topology is a crucial aspect to be taken into consideration while designing SiC VDMOSFETs.

Reliability is a critical issue in the power system, especially for SiC MOSFETs. Numerous studies have investigated reliability and failure mechanisms, including short circuit [9], surge current [10], avalanche [11], gate oxide stress [12], [13], and so on. Additionally, previous studies [14], [15] have explored how $L_{JFET}$ impact device performance and reliability, with a focus on short-circuits and avalanche. However, it is worth noting that all prior research on avalanche reliability has solely

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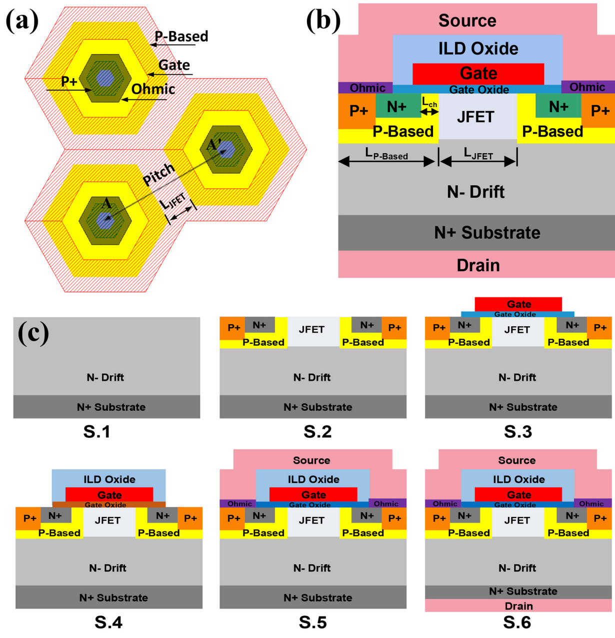


Fig. 1. (a) The hexagonal cell topology, (b) cross section of A-A', (c) the key stages for manufacturing process of SiC VDMOSFETs.

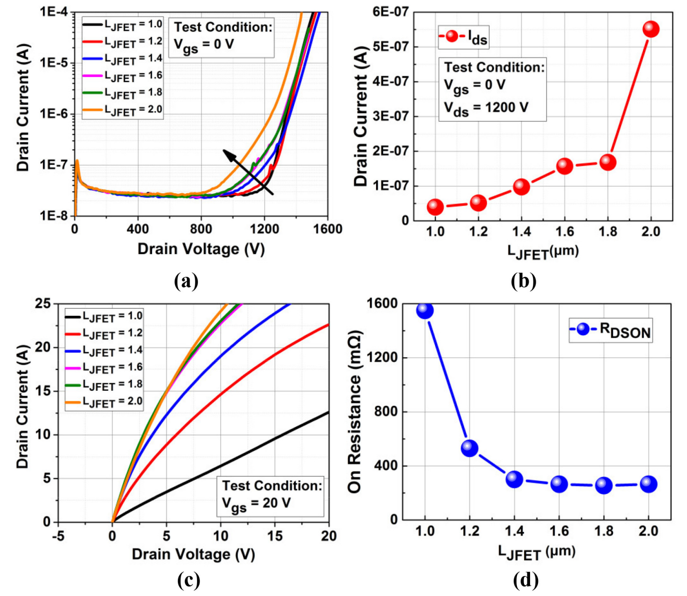


Fig. 2. (a) Blocking characteristic of DUTs and (b) $I_{ds}$ at $V_{ds}$= 1200V, $V_{gs}$ = 0V as a function of $L_{JFET}$. (c) Output characteristic of DUTs at $V_{gs}$ = 20V, $I_{ds}$ = 5A. (d) Specific ON resistance of DUTs as a function of $L_{JFET}$.

concentrated on the conventional linear topology [15]. The characteristics and avalanche reliability of SiC VDMOSFETs with hexagonal topology is seldom. Therefore, this study analyzes the static properties and dynamic characteristics of SiC VDMOSFETs with hexagonal topology and different $L_{JFET}$. In addition, avalanche capability and failure mechanisms are also investigated by using unclamped inductive switching (UIS) test and technology computer-aided design (TCAD) simulation.

## II. Device Structure and Fabrication

The hexagonal cell topology in 1200V SiC VDMOSFETs with various $L_{JFET}$ (1.0$\mu$m, 1.2$\mu$m, 1.4$\mu$m, 1.6$\mu$m, 1.8$\mu$m, 2.0$\mu$m) are designed and fabricated. The topology is illustrated in Fig. 1(a) and (b) alongside the cross section of SiC VDMOSFETs, showcasing the P-Based, Gate, Ohmic, and P+ regions. The distance from A to A' marks the cell pitch. The channel region width is $L_{ch}$, which equals 0.5$\mu$m. The P-Based region width is $L_{P\text{-}Based}$, which is equal to 3.3$\mu$m.

Based on the previous design, SiC VDMOSFET chips with a hexagonal cell topology and a blocking voltage of 1200V are manufactured. The key stages of fabrication are shown in Fig. 1(c), including 6 steps. S.1: An epitaxial layer thickness of 10$\mu$m with a concentration of 8e15 cm$^{-3}$ is grown on a 6-inch SiC wafer. The wafer is cleaned, followed by etching of aligned marks. S.2: Ion implantation is performed in the P+ source region and P-Based region using a self-aligned process that creates 0.5$\mu$m spacers via polysilicon deposition and etching. Then, N+ source ion implantation is employed to form a conduct channel in P-based region. Additionally, slight N-type implantation is executed in the JFET region to enhance the dopant concentration and adjust the threshold voltage. S.3: Gate oxide is formed through thermal oxidation, and the wafer is annealed in a NO atmosphere in order to reduce SiC/$SiO_2$ defects. Polysilicon is then deposited and etched to produce the gate electrode. S.4: An isolated oxide layer (ILD) is subsequently formed on the polysilicon to protect the gate structure, and then it is etched between the gate and source. S.5: The source ohmic contact is established via rapid thermal annealing. To create source and gate pads, a 4$\mu$m-thick AlSiCu layer is deposited. Nitride and polymide deposition are utilized to protect the chip termination, and front-side processing is finished. S.6: The SiC wafer is then thinned to decrease conduction resistance from 350$\mu$m to 180$\mu$m. Laser annealing is used to activate the ohmic contact, and backside metallization for the drain electrode is deposited, signaling the end of the fabrication process. After production, they are packed into a TO247-3.

## III. Device Characterization

This study tested fabricated devices with different $L_{JFET}$ characteristics, measuring various parameters such as drain voltage versus drain current ($I_{ds}$-$V_{ds}$), leakage current versus JFET width characteristic ($I_{ds}$-$L_{JFET}$), output characteristics ($I_{ds}$-$V_{ds}$@$V_{gs}$), and specific ON-resistance versus JFET width ($R_{on,sp}$-$L_{JFET}$). The obtained results are depicted in Fig. 2. The drain-source leakage current remains almost constant below 800V, but gradually increased with $L_{JFET}$ increment when $V_{ds}$ was greater than 800V. All designs exhibit blocking voltages above 1200V for $I_{ds} \geq 10\mu$A, with Fig. 2 (b) displaying the extracted leakage current at $V_{ds}$ = 1200V. Additionally, Fig. 2(c) shows the output characteristics under conditions of $V_{gs}$ = 20V measurement. The $R_{on,sp}$ characteristics of $L_{JFET}$ are shown in Fig. 2(d), based on the results obtained at $V_{gs}$ = 20V and $I_{ds}$ = 5A. As the size of $L_{JFET}$ increases from 1.0$\mu$m to 1.4$\mu$m, there is a marked decrease in $R_{on,sp}$. Conversely,

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TABLE I
SUMMARY OF EXPERIMENTAL RESULTS

| | L_J1.4 | H_J1.0 | H_J1.2 | H_J1.4 | H_J1.6 | H_J1.8 | H_J2.0 |
|---|---|---|---|---|---|---|---|
| JFET density | 0.079 | 0.144 | 0.166 | 0.187 | 0.207 | 0.226 | 0.242 |
| BV [V] | 1546 | 1510 | 1523 | 1550 | 1510 | 1506 | 1435 |
| Vth [V] | 3.21 | 3.21 | 3.2 | 3.24 | 3.26 | 3.24 | 3.24 |
| $R_{on,sp}$ [mΩ-cm$^2$] | 20.8 | 44.8 | 15.3 | 8.7 | 7.7 | 7.4 | 7.7 |
| $C_{gd,sp}$ [pF/cm$^2$] | 173 | 164 | 175 | 210 | 247 | 260 | 271 |
| $Q_{gd,sp}$ [nC/cm$^2$] | 368 | 283 | 377 | 424 | 490 | 520 | 541 |
| FOM ($R_{on}$×$C_{gd}$) [mΩ-pF] | 3590 | 7332 | 2674 | 1830 | 1902 | 1926 | 2086 |
| FOM ($R_{on}$×$Q_{gd}$) [mΩ-nC] | 7662 | 12680 | 5760 | 3685 | 3770 | 3849 | 4164 |

*Note: L_J1.4 represents linear strip cell topology with $L_{JFET}$ = 1.4μm. H_J1.0 represents hexagonal cell topology with $L_{JFET}$ = 1.0μm. BV@$I_{ds}$ = 100μA. $C_{gd,sp}$@ $V_{ds}$ = 800V.

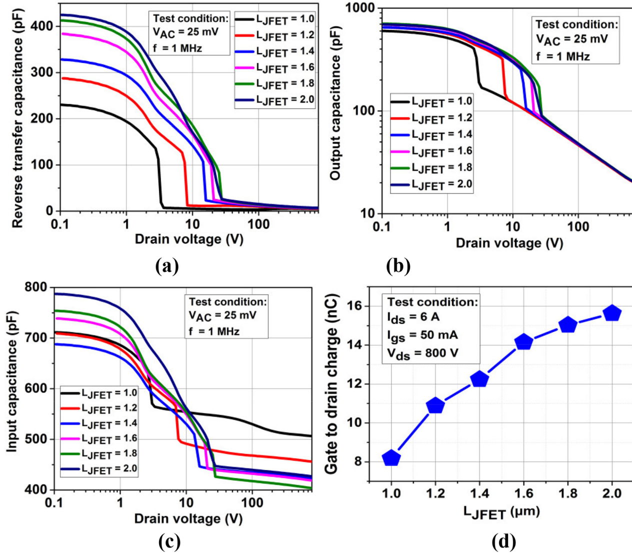


Fig. 3. (a) Reverse transfer capacitance, (b) output capacitance, and (c) input capacitance characteristics of DUTs. (d) Gate to drain charge characteristics versus $L_{JFET}$.

there is a gradual decrease from 1.6$\mu$m to 2.0$\mu$m, indicating that the resistance of the JFET region has a relatively insignificant effect. The threshold voltage ($V_{th}$) is a crucial parameter, extracted under the condition of $V_{gs} = V_{ds}$ @ $I_{ds}$ = 2mA. The results for different $L_{JFET}$ are shown in following Table I.

Further, dynamic properties are evaluated by measuring capacitance versus drain voltage (C-V) and gate charge (Qg) characteristics. The results are shown in Fig. 3. As seen in Fig. 3(a), there is a noticeable rise in the reverse transfer capacitance ($C_{rss}$) as the $L_{JFET}$ dimensions augment from 1.0$\mu$m to 2.0$\mu$m. This increase is attributed to the enlarged overlap area between the gate and drain, thereby amplifying the gate-to-drain capacitance ($C_{gd}$), where $C_{rss} = C_{gd}$. Additionally, Figure 3(b) highlights the output capacitance behavior ($C_{oss}$), which exhibits certain distinctions from $C_{rss}$. The $C_{oss}$ value for $L_{JFET}$ is at its least for 1.0$\mu$m, while $L_{JFET}$ measuring 1.2$\mu$m and 1.4$\mu$m demonstrate nearly the same $C_{oss}$ value at $V_{ds}$ = 0.1V. $L_{JFET}$ measuring 1.6$\mu$m, 1.8$\mu$m and 2.0$\mu$m show almost identical $C_{OSS}$ valure. The $C_{ds}$ value is higher for $L_{JFET}$ measuring 1.2$\mu$m due to increased cell count with the same die size, according to the formula $C_{oss} = C_{gd} + C_{ds}$. Fig. 3(c) displays the input capacitance ($C_{iss}$) characteristics of DUTs. There is no obvious regular pattern of increasing $L_{JFET}$ from 1.0$\mu$m to 2.0$\mu$m. The equation $C_{iss} = C_{gd} + C_{gs}$ shows that $C_{gd}$ increases with $L_{JFET}$ increment. However, $C_{gs}$ depends on the overlap area between gate and source and the number of cells. The study measured $Q_{gd}$ against a series of $L_{JFET}$, with the results presented in Fig. 3(d). A linear increase in $Q_{gd}$ is observed with an increase in $L_{JFET}$, which is consistent with the previously mentioned $C_{gd}$.

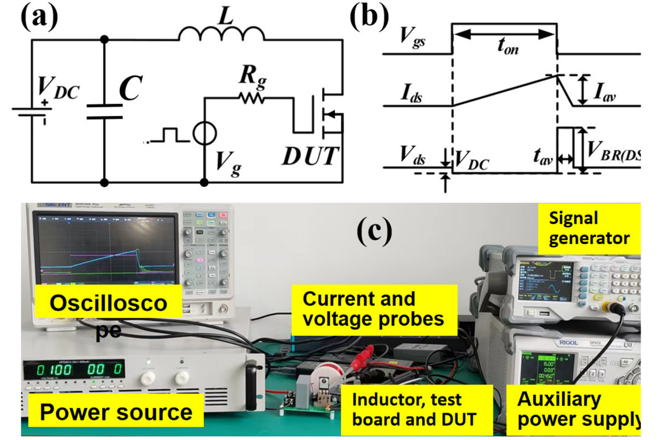


Fig. 4. (a) Simplified circuit diagram, (b) waveforms of $V_{gs}$, $I_{ds}$, and $V_{ds}$ and (c) UIS test platform. $V_{DC}$ = 100V, L = 2mH, $V_{gs}$ = -5/+20V.

Table I displays the experimental results for hexagonal SiC VDMOSFETs with different $L_{JFET}$ widths as well as for traditional linear strips with 1.4$\mu$m $L_{JFET}$. The JFET densities are calculated as (JFET area)/(die area). The breakdown voltage of all designs (measured at $I_{ds}$ = 100$\mu$A) is above 1400V, which is much higher than the rating voltage of 1.2kV. And all of the threshold voltage exceed 3.2V. The measured $R_{on,sp}$ value for $L_{JFET}$ = 1.8$\mu$m in hexagonal topology design is the smallest. For $L_{JFET}$ = 1.4$\mu$m, the $R_{on,sp}$ in linear strip topology is 20.8mΩ·cm$^{-2}$, while it is 8.7mΩ·cm$^{-2}$ in hexagonal topology. The measured HF-FOM for all hexagonal topologies are observed from $L_{JFET}$ = 1.0$\mu$m to 2.0$\mu$m. The optimum hexagonal design with $L_{JFET}$ = 1.4$\mu$m has better HF-FOM ($R_{on}$×$C_{gd}$) by 1.96 and HF-FOM ($R_{on}$×$Q_{gd}$) by 2.08 compared with the linear strip topology design.

## IV. UIS EVALUATION AND RELIABILITY INVESTIGATION

The circuit schematic, principle and equipment employed for the UIS test are shown in Fig. 4. The collection of instruments comprises of an oscilloscope, high-voltage power supply, signal generator, low-voltage power supply, current probe, voltage probe, and testing board. The high-voltage power supply is responsible for generating the required bus voltage for testing purposes, which in this research is set at 100V. The signal generator supplies a drive signal to operate the DUTs in ON and OFF states, which corresponds to the inductance charging and DUT avalanche phases. The low-voltage power supply provides the voltage required for the gate driver of the DUTs. The oscilloscope displays the results of the avalanche waveform in this test. Simplified $V_{gs}$, $I_{ds}$, and $V_{ds}$ waveforms during avalanche are seen in Fig. 4(b). When the DUT operates at the ON state, the inductor is charging and

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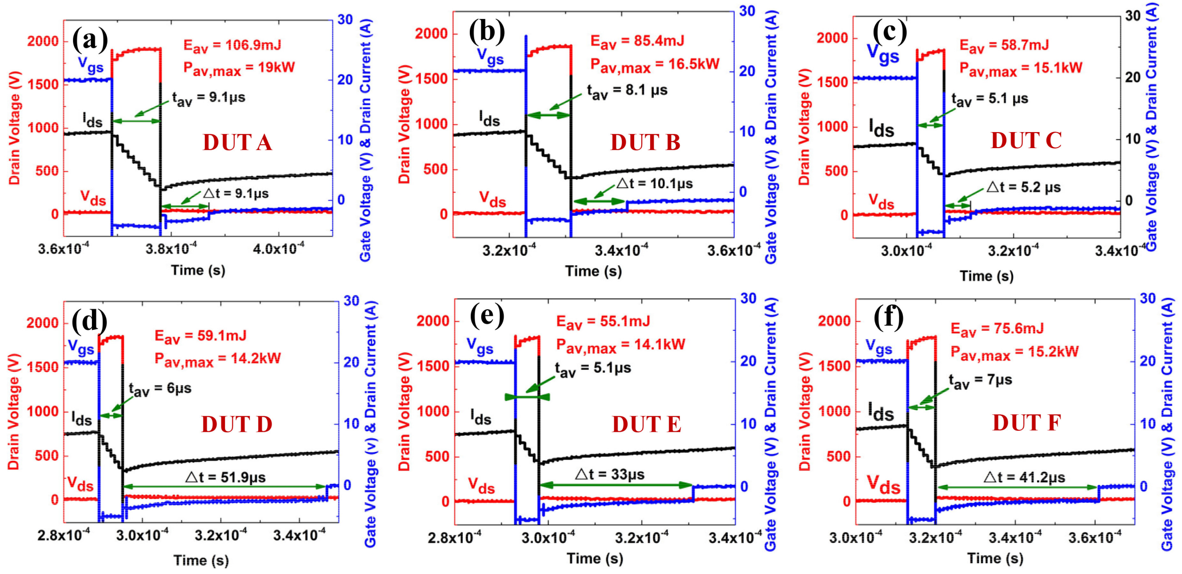


Fig. 5. Failure waveforms of various $L_{JFET}$ during UIS experiment.

the $I_{ds}$ rising. The $I_{ds}$ can be obtained by flowing formula:

$$dI_{ds} = \frac{V_{DC}}{L}dt$$

When the DUT switches off and the energy stored in the inductor is released uncontrollably. A high di/dt in the inductor induces an extremely high voltage at the DUT, and the device operates on avalanche breakdown. The avalanche time ($t_{av}$) is calculated using the following formula:

$$t_{av} = \frac{I_{av}}{V_{BR(DSS)} - V_{DC}} \times L$$

During avalanche breakdown, the energy stored in the inductor is released into thermal dissipation in DUT until the avalanche is finished. The calculated avalanche energy ($E_{av}$) is as following:

$$E_{av} = \int_0^{t_{av}} V_{BR(DSS)} \cdot I_{av}(t)dt$$

where $I_{av}(t)$ is avalanche current varies with time.

## V. UIS Results and Discussion

The SiC VDMOSFETs with hexagonal cell topology and different $L_{JFET}$ widths (1.0$\mu$m, 1.2$\mu$m, 1.4$\mu$m, 1.6$\mu$m, 1.8$\mu$m, and 2.0$\mu$m) were used to investigate avalanche reliability and failure mechanism under UIS. For clarity, series of devices are designated as DUT A, DUT B, DUT C, DUT D, DUT E, and DUT F. The experimental procedure proceeds as follows: a new device is selected for the UIS test and subjected to an increasing avalanche current until failure occurs during avalanche breakdown. The electrical parameters of the final failure, including $V_{gs}$, $I_{ds}$, and $V_{ds}$, are extracted. This process is repeated with devices of identical specifications until consistent experimental results are achieved. The failure waveforms are shown in Fig. 5. The avalanche energy ($E_{av}$), maximum dissipation power during avalanche breakdown ($P_{av,max}$) and avalanche duration ($t_{av}$) are calculated and exhibited in the picture. Burnt out time of gate voltage (Δt) is also extracted and shown in the picture. Δt describes the time from the end of the avalanche to the failure of gate. As can be seen from the picture, the voltage of all DUTs in the avalanche process is basically the same, and they are all around 1750V. And as the avalanche breakdown continues, the voltage gradually rises. This is because a lot of heat is generated in DUTs during avalanche process, causing the avalanche breakdown voltage of silicon carbide to rise. Notably, DUT A had the largest $E_{av}$ at 106.9mJ. The $E_{av}$ of DUT B, C, D, E and F are 85.4mJ, 58.7mJ, 59.1mJ, 55.1mJ and 75.6mJ, respectively. The avalanche energy is converted into loss during avalanche breakdown. The larger the $E_{av,}$ the more severe the heat loss experienced by the device during the avalanche process. At the same time, the maximum power loss of the device in the process of avalanche breakdown is calculated according to $P_{av,max}$ = U × I formula. U is the $V_{ds}$ during avalanche breakdown, and I is the $I_{ds}$. $E_{av}$ is used to evaluate the heat generated, while $P_{av,max}$ is used to evaluate the maximum dissipation power during avalanche. The larger $P_{av,max}$, the faster heating rate, which also means the greater thermal shock. DUT A has a $P_{av,max}$ of 19kW, indicating that the device experiences the greatest instantaneous thermal shock inside the material. The $P_{av,max}$ of DUT B, C, D, E and F are 16.5kW, 15.1kW, 14.2kW, 14.1kW and 15.2kW respectively. As can be seen from the picture, the avalanche energy is positively correlated with the avalanche breakdown time. The greater avalanche energy, the longer avalanche lasts. DUT A has a $t_{av}$ of 9.1$\mu$s and DUT B has a $t_{av}$ of 8.1$\mu$s.

After dropping the $t_{av}$, the $V_{ds}$ drops from the avalanche breakdown voltage to zero, but the $I_{ds}$ is out of control. At this moment, the $V_{gs}$ begins to gradually rise from −5V. And $V_{gs}$ increased with the increase of time. The possible reason is that due to the avalanche breakdown and $I_{ds}$ out of control, the temperature of the DUTs increases sharply, and the schottky

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TABLE II
SUMMARY OF UIS EXPERIMENT RESULTS

| Design | $E_{av}$ (mJ) | $t_{av}$ (μs) | $P_{av,max}$ (kW) | Δt (μs) |
|---|---|---|---|---|
| DUT A | 106.9 | 9.1 | 19 | 9.1 |
| DUT B | 85.4 | 8.1 | 16.5 | 10.1 |
| DUT C | 58.7 | 5.1 | 15.1 | 5.2 |
| DUT D | 59.1 | 6 | 14.2 | 51.9 |
| DUT E | 55.1 | 5.1 | 14.1 | 33 |
| DUT F | 75.6 | 7 | 15.2 | 41.2 |

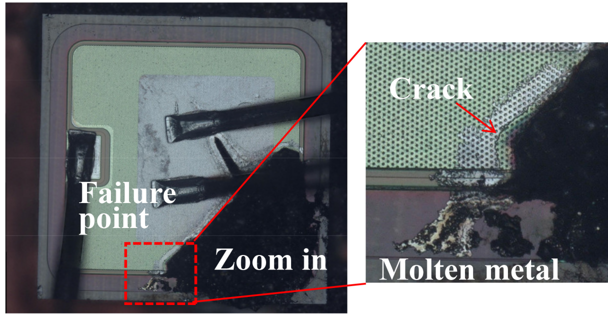


Fig. 6. Optical microscope images and zoom in for failed device.

current increases under gate oxide while the driver power remains unchanged, resulting $V_{gs}$ increase. After Δt, the $V_{gs}$ suddenly rises sharply, meaning the device damage. It is worth noting that the Δt varies with different designs and it does not seem to be related to $E_{av}$. DUT A, B, and C have similar Δt values of 9.1$\mu$s, 10.1$\mu$s, and 5.2$\mu$s, respectively. However, in DUT D, E, and F, Δt are 51.9$\mu$s, 33$\mu$s, and 41.2$\mu$s, respectively, which is almost 4 times that of DUT A and more than 6 times that of DUT C. It is well known that devices are mainly caused by thermal runaway in UIS tests. However, such a large Δt means that there may be some different failure mechanisms between DUT A, B, C and DUT D, E, F. For clarity, UIS experiment results are summarized in Table II.

Further, all the DUTs after avalanche failure are decapsulated. We compared all the failure devices, and found that the failure location is random. One of the optical microscope image is shown in Fig. 6. A failure position point located at the lower right corner of the chip. The black material is carbonized after the ablation of the molding compound and can not be cleaned by chemical solution, meaning that the device experienced extremely high temperature during avalanche process. The failure location point is scaled up, as seen in the picture, the metal melts and flows to the terminal insulation area from active region. In addition, there is a crack along the residual edge of the molding compound that spans many cells in length. The random failure position can be explained from that some defects in the chip are randomly distributed due to manufacturing process fluctuations, resulting low blocking voltage capacity of some cells. And the avalanche occurs first in those weak cells under the UIS test. During avalanche breakdown, the energy stored in the inductor is released instantaneously to heat in those cells, resulting in extremely high temperature thermal shock in the device and internal

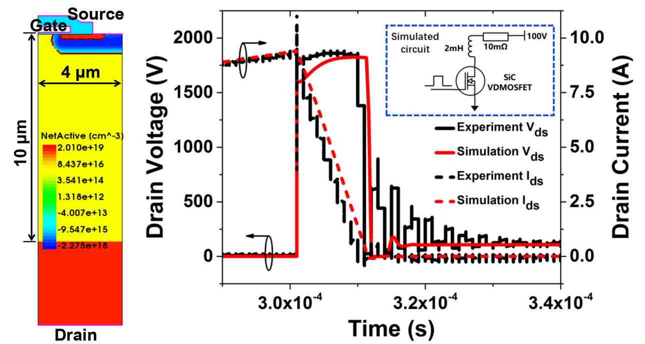


Fig. 7. $I_{ds}$ and $V_{ds}$ of half-cell simulation results for DUT C under the UIS test before avalanche failure.

cracking between the materials. The results are consistent with those reported in previous studies [16].

Further, the half-cell structure SiC VDMOSFETs was constructed according to the experimental structure and parameters by TCAD. Mixe-mode module was applied in TCAD simulation, and the simulated circuit was shown in Fig. 7. Besides, the self-heating model is considered in the simulation. Considering that there is resistance in the actual circuit, 10mΩ resistance is introduced in the simulation circuit diagram. The inductance L (2mH) in the simulation is the same as that in the actual test. The figure shows the match between the experimental test waveform and the simulation waveform of DUT C before the failure. The zigzag in the experimental waveform is due to the low bandwidth of the oscilloscope. It can be seen from the figure that there is a good agreement between the simulated waveform and the actual waveform, which means that the simulation can qualitatively determine the changes between the internal physical quantities of the device in the UIS working process.

Fig. 8 shows the failure mechanism of DUT during avalanche breakdown by using TCAD simulation. Fig. 8 (a) shows the simulated waveform of DUT C avalanche failure. t1 and t2 in Fig. 8(a) represent two moments are used to explore how the physical parameters change in the device. Fig. 8(b) shows the cell structure and circuit schematic of SiC VDMOSFET and current path at t1 and t2. As shown in Fig. 8(c), during avalanche breakdown (t1), the avalanche current flows from the drain through the P-Based region to the source to release avalanche energy. However, between t1 and t2, the channel is opened and the avalanche current exists at both the P-Based and the channel region. The reason is that a lot of heat is generated during avalanche breakdown, leading to $R_B$ rise. When the voltage between $R_B$ exceeds 2.7V (PN junction drop voltage in SiC), the parasitic BJT is ON, resulting in $I_{ds}$ uncontrollable. t2 point indicates that the $I_{ds}$ is uncontrollable. This phenomenon is confirmed by experimental waveform in Fig. 5.

As $I_{ds}$ is out of control, the internal temperature of the device is further increased sharply. Fig. 8 (d) shows the internal temperature distribution at t1, t1∼t2, and t2. It can be seen from the picture that the highest temperature is mainly concentrated in the JFET region. And with the increase of

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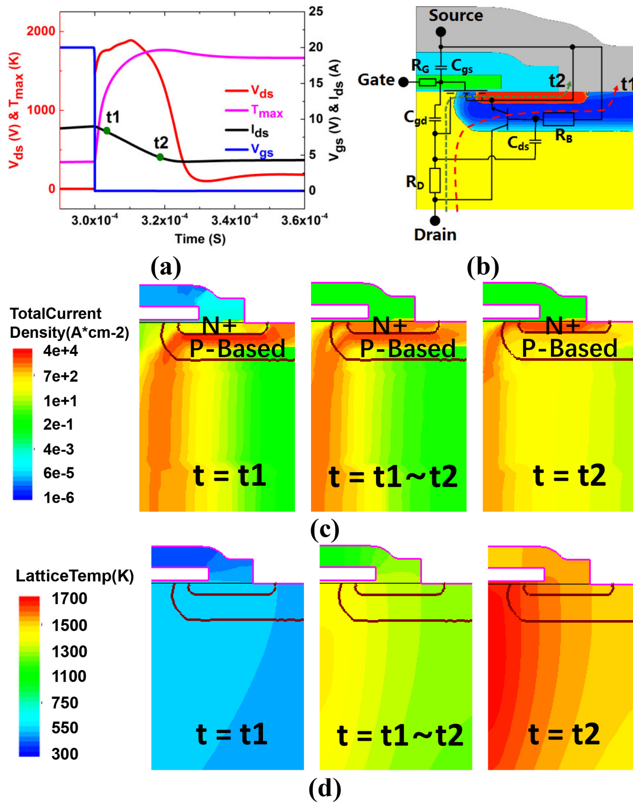


Fig. 8. (a) Simulated waveform for DUT C during avalanche failure. (b) Simulated results circuit schematics and avalanche current paths. (c) Current density within device, and (d) lattice temperature distribution at time point t1, t1∼t2, and t2.

time from t1 to t2, the lattice temperature rises sharply. At t2, the highest temperature reached 1700K, exceeding the melting point of aluminum. The optical microscopic image in Fig. 6 confirms this conclusion. A conjure is proposed that cracks occur inside the material due to sharply internal thermal stress, resulting in device damage. As time increases, the maximum temperature expands from the JFET region to the source contact. The larger $L_{JFET}$, the longer it takes for the temperature to spread. Therefore, the Δt of DUT F is much longer than that of DUT A in Fig. 5.

## VI. Conclusion

In this paper, the hexagonal cell topology of planar SiC VDMOSFETs with varied $L_{JFET}$ are designed and manufactured. The static properties, dynamic characteristics, and UIS test are investigated. $L_{JFET} = 1.4\mu$m has the best HF-FOM by comparing the dynamic and static parameters of each design. The reliability and failure mechanism of different designs under UIS test were investigated by experiment and TCAD simulation. During avalanche process, the device generates a lot of heat instantaneously, resulting in parasitic BJT conduction, current out of control and failure. The instantaneous extreme high temperature causes internal cracking of the material and metal melting, resulting in device damage. Besides, The heat is mainly concentrated in the JFET region during avalanche breakdown. $V_{gs}$ mutates after the current is out of control since that molten metal contacts the gate through a crack, resulting in gate-source short circuit.

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