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RESEARCH ARTICLE

Converter Design for High Temperature Superconductive Degaussing Coils

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ABSTRACT Detection of the magnetic signature of ships can be avoided by using a degaussing system; a set of on-board copper coils that compensates for the magnetic signature. High temperature superconductors (HTS) are currently investigated as a replacement for copper degaussing coils. By using HTS, we have to deal with higher currents and therefore with higher power supply losses. Also, large current leads are needed which introduces extra losses. This paper investigates different possible solutions to minimize these losses. Four H-bridge-based MOSFET topologies are presented that were designed to reduce the power supply and current lead losses. The first topology uses an H-bridge configuration so that the degaussing current can freewheel through the low-resistance MOSFETs. The second topology places the H-bridge inside the cryostat so that the current leads can be made smaller. The third topology includes a smoothing capacitor in the cryostat so that the current leads and input current are even smaller. The fourth topology uses a transformer so that the current leads can be eliminated. Measurements were done to determine the MOSFETs and capacitor performance in liquid nitrogen. The simulated losses of the four topologies are compared to determine the most energy-efficient option for supplying current to the HTS coils. It was found that by submerging multiple parallel MOSFETs in liquid nitrogen, the on-state resistance is decreased and the current supply can be made more efficient. Also, by placing a smoothing capacitor inside the cryostat, the current lead losses can be minimized significantly. The benefits of using a transformer do not outweigh the transformer losses.

INDEX TERMS Converter, cryocooled electronics, cryostat, degaussing, high temperature superconductors, magnetic signature, parallel MOSFETs.

I. INTRODUCTION

Ships distort Earth's magnetic field due to their permeability [1]. The distortion can be detected by sea mines or sensors. In order to avoid detection, ships can reduce their magnetic signature by degaussing [2]. A degaussing system consists of a set of on-board copper coils which create an opposing magnetic field to that of the magnetic signature [3].

To create the degaussing field, a high magnetomotive force is needed. As a result, a significant amount of heat is dissipated in the copper degaussing coils because of the Ohmic losses. To eliminate these losses, the possibility of using high temperature superconductors (HTS) instead of copper degaussing coils is currently under investigation [4], [5], [6].

A feature of HTS is that it can facilitate a much higher current density than copper. When a higher current is used, the number of turns can be reduced while still maintaining the needed magnetomotive force. This is useful because HTS tape is expensive and the large degaussing coils on a ship demand long lengths of wire. If the current exceeds the critical current of the tape, the superconductor goes out of its superconductive state. This should be avoided. Two problems arise when utilizing fewer turns with a higher current.

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Firstly, the power supply for the HTS coils needs to deliver more current than for the copper coils. Current supplies typically dissipate more energy at higher current levels. This would make the HTS system less efficient than the copper system for the same magnetomotive force rating [7].

Secondly, current leads are needed to connect the source at room temperature to the HTS at cryogenic temperature. Through the current leads, heat leaks into the cryostat. The losses are expected to be significant [8]. The current leads need to be able to handle the large current as well. In order to minimize Ohmic losses, they have to be designed with a sufficient cross-section. This causes more heat to leak into the cryostat which needs to be cooled away.

A solution to reduce the energy dissipation in the current source is to connect the HTS coil through an H-bridge topology. The idea is to avoid a forward voltage drop in series with the current path. By using MOSFETs with a low on-state resistance, the degaussing current will decay slowly during the discharge state because of the low resistance in the current path and the large inductance of the HTS degaussing coil [9]. Because of the low resistance, we can use a small duty cycle. During the short charging state of the coil, there will be high energy dissipation in the source. However, during the long discharge state, almost no energy is dissipated.

A way to reduce the size of the current leads is to move part of the electronics inside the cryostat. This will reduce the rated current of the current leads, but it will introduce extra losses inside the cryostat. Also, a rectifier can be added in the cryostat so that the energy to the degaussing coils can be transferred by induction using a transformer. This would eliminate the need of current leads at all, but introduce even more losses in the cryostat because of the forward voltage of the rectifier. As a side effect, the MOSFET losses are decreased when they are placed inside the cryostat, because the on-state resistance can be lower at cryogenic temperatures [10]. The extra heat that is introduced inside the cryostat needs to be lifted by the cooler. This is known to be very inefficient [11].

The objective of this paper is to investigate different possible current supply designs for a HTS degaussing coil. We will test the previously presented ideas to answer the following research questions:

- Is it more energy efficient to move part of the electronics into the cryostat?
- Is it more energy efficient to use a transformer in order to eliminate current leads?

To answer these questions, we estimate and compare the efficiency of several converter topologies. This is done by identifying and quantifying the sources of loss in the power supply topologies. In addition to the the electrical losses, also the cryostat losses are taken into account. Only the loss sources which differ from topology to topology are taken into consideration. Measurements are conducted to find the performance of the MOSFETs and capacitors in liquid nitrogen.

Section II defines the requirements for the power supply and presents the different converter topologies. In section III, all the sources of loss of the topologies are identified and modelled. Section IV presents and discusses the results. Finally, section V draws a conclusion.

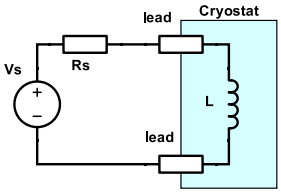

FIGURE 1. Topology 0: the power source directly connected to a HTS degaussing coil.

TABLE 1. Requirements of the load.

Symbol	Quantity	Value	Unit
I_r	Rated current	100	A
ΔI_r	Current ripple	0.5	%
L	Inductance	15	mH

II. CONVERTER DESIGN

The most obvious configuration to power a HTS degaussing coil is to directly connect the degaussing coil to a current source as shown in figure 1. In this case, the HTS degaussing coil is placed inside a cryostat in order to ensure that the HTS material is in superconductive state. Two current leads are needed which connect the HTS coil at cryogenic temperature to the current source at room temperature. The current leads cause heat to enter the cryostat which needs to be cooled away. The current source constantly needs to deliver the required current which causes losses represented by R_s. As a reference, this configuration is considered as topology 0.

In section II-A, the requirements and assumptions of the system are defined. In section II-B, the alternative topologies are presented which are expected to be more efficient.

A. REQUIREMENTS

To compare different current source topologies, the specifications for the degaussing coils are needed. They are determined and taken from previous work [12]. A FEM model of a full-sized ship with 15 degaussing coils was constructed to find the rated current, I_r, and inductance, L, of the degaussing coils. In this research, the degaussing coil with the highest current rating is chosen to be the load for which the current source needs to be designed. The specifications for this coil are given in table 1. The current source should be bi-directional.

The following assumption are made in the ship model and in this paper:

- The degaussing coils have linear inductance
- There are no mutual inductances between the degaussing coils
- The cryostat uses liquid nitrogen and operates at a temperature of 77 K
- There are no blocking losses in the MOSFETs

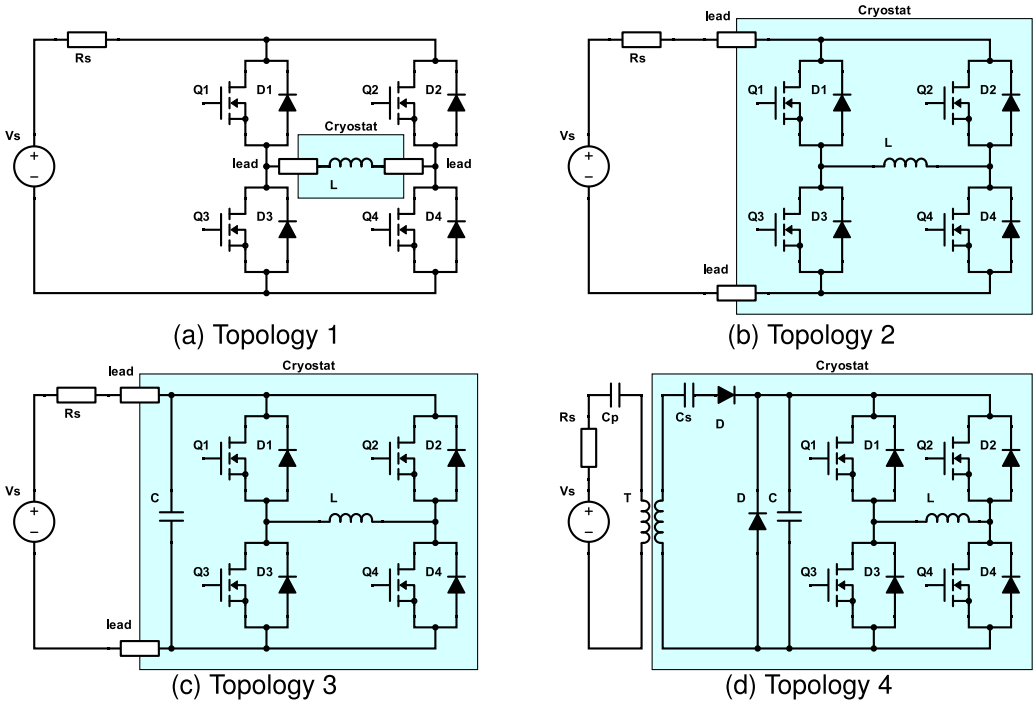

FIGURE 2. Converter topologies. (a) Only the degaussing coil in the cryostat, large current leads needed. (b) H-bridge added to the cryostat. More losses within cryostat, but smaller current leads needed. (c) A smoothing capacitor added in the cryostat. Even smaller current leads needed. (d) Rectifier added to cryostat to eliminate the need of current leads at all.

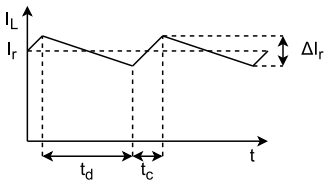

FIGURE 3. HTS coil current waveform.

B. TOPOLOGIES

In this paper, we will consider a MOSFET-based H-Bride topology as the basic design for the converter. As needed, an H-bridge is able to provide the current in both directions. The rated degaussing current is quite high, so a device like an IGBT with a fixed voltage drop would have more losses than MOSFETs. For example, an IGBT with a forward voltage of 0.7 V that conducts 100 A will dissipate a power of 70 W. A MOSFET with an on-state resistance of 500 $\mu\Omega$ only dissipates 5 W for the same case. The on-state losses can even be lowered by placing multiple MOSFETs in parallel. Figure 3 shows the waveform of the current in the HTS coil. The low resistance in combination with the high inductance and no resistance of the HTS degaussing coil will cause the current to decay very slowly during discharge state, t_d. Most of the losses occur during the relatively short charging state, t_c.

1) TOPOLOGY 1

The HTS coil is placed inside a cryostat and is connected to the output of the H-Bridge through current leads as shown in figure 2a. The degaussing coil is charged by closing Q_1 and Q_4. During the discharging state, Q_3 and Q_4 are closed. The source now only has to deliver current during the charging state, which is expected to be very short compared to the discharging state because of the large time constant of the degaussing coil in combination with the MOSFETs. The current leads have to be rated for the rated degaussing current I_R.

2) TOPOLOGY 2

The HTS coil is placed inside the cryostat together with the H-Bridge as shown in figure 2b. The current leads can be made smaller because they only have to be sized for the RMS current during the cycle. The on-state resistance of the MOSFETs drops because they are placed inside the liquid nitrogen. This will reduce the duty cycle even further. However, the conduction and switching losses of the MOSFETs are dissipated inside the cryostat which adds to the cryostat losses.

3) TOPOLOGY 3

A smoothing capacitor is added inside the cryostat as shown in figure 2c. This capacitor causes the current that flows through the current leads to change from short high current pulses, to a steady DC current. Now the source doesn't have to be able to deliver the rated current, I_r, anymore. It will also decrease the Ohmic losses in the current leads. However, the capacitor will add extra losses inside the cryostat.

TABLE 2. Relevant values from the model in case of no parallel MOSFETs.

Symbol	T_1	T_2	T_3	T_4	Unit
D	3.6	1.3	0.6	0.5	%
f_s	16.98	5.35	5.38	5.38	Hz
$I_{s(RMS)}$	18.9	11.4	0.77	3.2	A
$I_{C(RMS)}$	-	-	7.7	7.1	A
$I_{D(RMS)}$	-	-	-	2.26	A

4) TOPOLOGY 4

A transformer is added where the secondary side is inside the cryostat as shown in figure 2d. This eliminates the need of current leads at all. Because of the low duty cycle, the current that flows in the smoothing capacitor is expected to be low. A diode is needed to rectify the current, but the power dissipation shouldn't be too high because of the low secondary current.

III. METHODOLOGY

In order to compare the topologies to one another, the efficiencies are analysed. For this, the sources of losses that differ per topology are quantified. The sources are then added and the total power loss, P_{tot}, is found as follows:

$$P_{tot} = P_s + P_{circ} + COP^{-1}\,(P_{cl} + P_{circ} + P_{sw}) \tag{1}$$

where P_s are current source losses, P_{circ} the circuit losses, P_{cl} the current lead losses, P_{sw} the switching losses and COP is the coefficient of operation of the cooler. Depending on the topology, some of the circuit losses are dissipated inside the cryostat. The current lead losses are dissipated inside the cryostat as well. These losses need to be cooled away by the cooler and therefore divided by COP.

To find the amount of energy loss, the waveforms of the currents in the circuit are needed. A model was created in the circuit software PLECS to test the topologies and retrieve the waveforms of the currents. As an example, table 2 shows the values for the duty cycle D, the minimum switching frequency f_s, and the RMS values for the source current I_s, capacitor current I_C and the diode current I_D for the case where there are no parallel MOSFETs. These values have been obtained for a 100 A current with 0.5% ripple as stated in table 1. The source voltage, V_s, is set at 10 V.

The on-state resistance of the MOSFETs and the performance of the capacitors are determined by measurements. Each of the sources of loss identified in equation (1) are further examined in the following subsections.

A. SWITCHING LOSSES

The switching losses are estimated according to the following equation:

$$P_{sw} = f_s N_p (E_{on} + E_{off} + E_{onD} + E_{dead}) \tag{2}$$

where f_s is the switching frequency, N_p the number of parallel MOSFETs, E_{on} is the MOSFET switch-on energy, E_{off} is the MOSFET switch-off energy and E_{onD} is the diode energy during MOSFET switch-on transient. The switch off losses in the diode, E_{offD}, are assumed to be zero. The dissipated energy components are estimated according to the following equations:

$$E_{on} = \int_0^{t_{ri}+t_{fu}} u_{DS}(t) i_D(t)\,\mathrm{d}t \tag{3}$$

$$E_{onD} = \int_0^{t_{ri}+t_{fu}} u_D(t) i_F(t)\,\mathrm{d}t \tag{4}$$

$$E_{off} = \int_0^{t_{ru}+t_{fi}} u_{DS}(t) i_D(t)\,\mathrm{d}t \tag{5}$$

where t_{ri} is the current rise time, t_{fi} the current fall time, t_{ru} the voltage rise time and t_{fu} the voltage fall time. The rise times, fall times, currents and voltages are calculated using the datasheet parameters [13].

During the dead-time the degaussing current needs to flow through a diode. The power dissipated in the diode can be expressed as follows:

$$E_{dead} = T_d(V_f I + R_D I^2) \tag{6}$$

where T_d is the dead time, V_f is the forward diode voltage drop, R_D is the diode resistance and I is the diode current. The voltage drop over the diode is much higher than the on-state voltage drop over the MOSFETs. In combination with the high degaussing current, the losses are much higher during the dead time than during the rest of the switching cycle. This causes extra losses inside the cryostat when the MOSFETs are inside the cryostat. This also causes the current to decay faster during the discharge state. The dead time should therefore be kept to a minimum.

B. CIRCUIT LOSSES

The circuit losses are divided into the following components:

$$P_{circ} = P_{DSon} + P_{PCB} + P_{trans} \tag{7}$$

where P_{DSon} are the on state losses in the MOSFETs, P_{PCB} the copper losses on the PCB and P_{trans} the transformer losses. The on-state losses are estimated as follows:

$$P_{DSon} = \frac{1}{N_p} I_{DS}^2 R_{DSon}(T) \tag{8}$$

where N_p is the number of parallel MOSFETs, I_{DS} the MOSFET current and $R_{DSon}(T)$ the on-state resistance as a function of temperature.

C. COMPONENT CHARACTERISTICS AT CRYOGENIC TEMPERATURE

For the topologies in this research, it is essential that the MOSFETs have an as low as possible on-state resistance. With this in mind, the SiR178DP by Vishay was chosen. While it is known that MOSFETs are generally able to perform in a cryogenic environment [10], it is still necessary to verify that this is also the case for this particular type of MOSFET. Besides, the on-state resistance at 77 K needs to be known in order to estimate the performance of the topologies. The on-state resistance of the MOSFET was measured at room temperature and in liquid nitrogen. Six samples were

TABLE 3. Measured components behaviour in LN_2.

Symbol	Quantity	$\bar{x}$	s_N	Unit
R_{DSon}(293 K)	On-state resistance	611	30.1	μΩ
R_{DSon}(77 K)	On-state resistance	404	8.2	μΩ
C (293 K)	Capacitance	216	0.32	μF
C (77 K)	Capacitance	161	0.45	μF

tested. Table 3 shows the mean, $\bar{x}$, and the standard deviation, s_N, of this measurements. It can be seen from the measured results that the on-state resistance of the selected MOSFETs is about 34% lower when submerged in liquid nitrogen. The measured on-state resistance values are a bit higher than the datasheet values. This is probably due to measuring some resistance at the leads of the MOSFETs.

Not every capacitor can operate at cryogenic temperatures [14]. Electrolytic capacitors, for example, freeze and lose their capacitive abilities. For the smoothing capacitor in topologies 3 and 4 however, a large capacitance is needed. For this, the best option is to use tantalum solid capacitors. The capacity of six samples of 220 μF tantalum solid capacitors was measured at room temperature and at 77 K. Table 3 shows the mean value and the standard deviation of these measurements. Though the capacitors lose about 20% of their capacitance, they still work at cryogenic temperatures.

The transformer is chosen to be of a flat air-cored helix type. The use of a core is not possible, because this would be a bad thermal insulator for the cryostat. A COMSOL simulation was done where the primary inductance, L_p, is equal to the secondary inductance, L_s. The coupling factor of the transformer was found to be 0.2. In order the improve the efficiency of the power transfer, resonant inductive coupling is used. Capacitors C_p and C_s are placed in series with the inductors at the primary and secondary side so that:

$$C_p = C_s = \frac{1}{L_s(2\pi f)^2} \tag{9}$$

where f is the transformer frequency.

D. CURRENT LEAD LOSSES

The losses in the current leads consist of two parts; the heat flow through the current lead into the cryostat and the heat generated inside the current lead because of Ohmic losses. These can be modelled as follows [15]:

$$dT = -\frac{dl}{kA}\dot{Q} \quad d\dot{Q} = I^2\frac{dl}{\sigma A} \tag{10}$$

where dT is the temperature difference, l the length, k the thermal conductivity, A the cross-section, $\dot{Q}$ the heat flow, $d\dot{Q}$ the generated heat, I the current and σ the electrical conductivity of the current lead. The heat flow due to the current leads has to be minimized, so the diameter of the current leads should be as low as possible. On the other hand, by decreasing the diameter, the generated heat increases due to Ohmic losses. There is a trade-off. The solution for the minimum heat flow through the current lead $\dot{Q}_{min}$ can be found by combining Equation (10):

TABLE 4. Current lead parameters for topologies T_1, T_2, T_3, and T_4.

Symbol	Quantity	T_1	T_2	T_3	T_4	unit
I_{peak}	peak current	I_r	I_r	DI_r	-	A
I_{avg}	average current	I_r	$\sqrt{D}I_r$	DI_r	-	A
l	length	10	10	10	-	cm
A	cross-section	5.13	0.59	0.037	-	mm^2
R	resistance	0.46	3.98	63.1	-	mΩ
$\dot{Q}$	heat influx	9144	1051	66	0	mW

$$\dot{Q}_{min} = I\sqrt{\frac{2k}{\sigma}(T_H - T_L)} \tag{11}$$

where T_H is the temperature outside the cryostat and T_L is the temperature inside the cryostat. From the minimum heat flow, the optimal wire length to surface area ratio follows. In our case we choose the current lead to be 10 cm and the optimal surface area is calculated. It should be noted that equation (11) assumes a constant current. However, for topology 2, the current through the leads differs during the switching cycle. In this case, we will model the generated heat as follows:

$$d\dot{Q} = \frac{dl}{\sigma A}\frac{1}{T_s}\int_0^{T_s} I(t)^2\,dt = D\left(\frac{I}{D}\right)^2\frac{dl}{\sigma A} \tag{12}$$

where T_s is the length of the switching cycle and D is the duty cycle. The calculated dimensions of the current leads are presented in table 4 for the case that there are no parallel MOSFETs.

E. COOLING EFFICIENCY

To check the merits of putting electronics inside the cryostat, the efficiency of the cooling process must be known. If, by placing an element inside the cryostat the losses decrease more than it costs to cool them away, it is considered a good choice. The efficiency of the cooling process is limited by the efficiency of the Carnot cycle and the efficiency of the cooler itself. The coefficient of operation, COP, can then be expressed as follows:

$$COP = \frac{\dot{Q}}{P} = \eta\epsilon_c = \eta\frac{T_L}{T_H - T_L} \tag{13}$$

where $\dot{Q}$ is the heat lifted from the cooler, P the power used by the cooler, η the efficiency of the cooler, ϵ_c the efficiency of the Carnot cycle, T_H the temperature outside the cryostat and T_L the temperature inside the cryostat. Since the cryostat operates at a temperature of 77 K, the efficiency of the Carnot cycle is 0.36. The efficiency of coolers for the power rating for degaussing systems can be assumed to be 0.2 [11], [16]. That means that for every Watt that is dissipated inside the cryostat, the cooler consumes 14 Watts of power. This is an efficiency of 7.14%.

IV. RESULTS

A. POWER BALANCE

With all the loss sources known, the balance can be made of the total loss of the topologies. The losses per component per

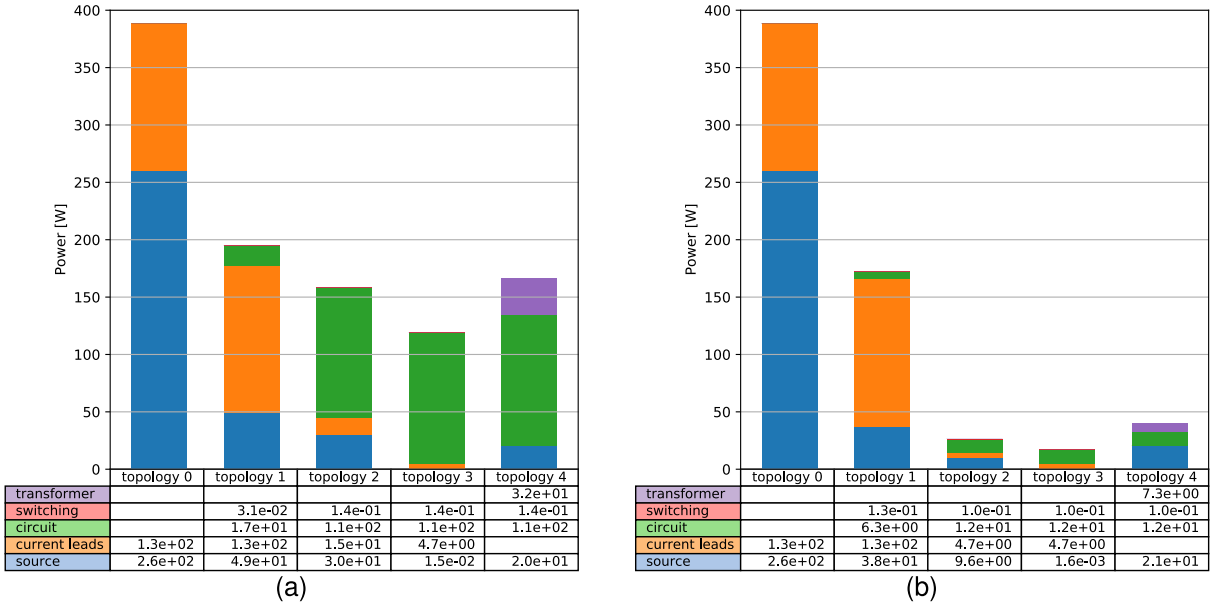

FIGURE 4. Power losses in each topology for (a) one MOSFETs per switch and (b) ten parallel MOSFETs per switch.

topology are shown in figure 4. The topologies from section II are compared with topology 0 from figure 1.

The power balance is shown for the case with no parallel MOSFETs in figure 4a. It can be seen that for topology 0, the main contributor is the loss in the current source. This part is so big, because the rated current constantly has to flow through the source. Also, the current leads are sized for the rated current. This makes the current lead losses high as well.

For topology 1, the source losses are considerably lowered compared to topology 0. This is because the rated current only flows from the source during the charge state. During the discharge state, the source current is zero. The current lead losses are still high, because the leads are still rated for the rated current. The circuit losses because of the MOSFETs and PCB are small, but present as well. The switching losses are insignificant, which is explained by the low switching frequency which is possible in this configuration.

For topology 2, the current leads can be made much smaller. This has a large effect on the power loss in the current leads. However, the circuit losses become much larger. This is because the components are now inside the cryostat, so a lot more cooling power is needed. Also, the switching losses happen inside the cryostat, but they are still very small compared to the other losses. It should be noted that the source losses also are a bit lower than for topology 1. This is because the resistance of the MOSFETs is lower in liquid nitrogen and therefore the duty cycle is lower as well.

For topology 3, the source and current lead losses are decreased even further. This is because the source current waveform is smoother which causes the RMS value of the source current to be lower than in the previous cases. The capacitor adds extra losses inside the cryostat, but these are insignificant.

For topology 4, a transformer is added to remove the current lead losses completely. However, the current lead losses were already very small in topology 3, so it does not have a large effect. There are extra transformer and rectifier losses inside the cryostat however. Also, the source losses are increased more. The total added losses are higher than in the previous case.

For the topologies in which the components are placed inside the cryostat, it seems that circuit losses, which include the on-state losses, become dominant because of the coefficient of performance of the cooler. A way to lower these losses is to place multiple MOSFETs in parallel so that the resistance is lower. Figuer 4b shows the power balance of the topologies again, but now with ten parallel MOSFETs per switch. Now the circuit losses become much smaller. Also, the current lead losses and the source losses become smaller. This is because the lower resistance enables a lower duty cycle. To determine a right amount of parallel MOSFETs in the final design, figure 5a shows the total power dissipation as a function of parallel MOSFETs. It can be seen that even by placing one extra MOSFET in parallel, the power can be decreased drastically. Placing more than ten MOSFETs in parallel does not seem to have a large impact on the final power use.

From figure 4 it can be concluded that the most energy efficient solution is topology 3. Besides energy-efficiency, this solution is also a practical one. The source does not have to be able to deliver the rated current so it can be made much smaller. The capacitor can be slowly charged during relatively long discharge times. Topology 4, which uses a transformer, does not add more advantages. Also, it adds more complexity to the circuit. It is not useful to use a transformer.

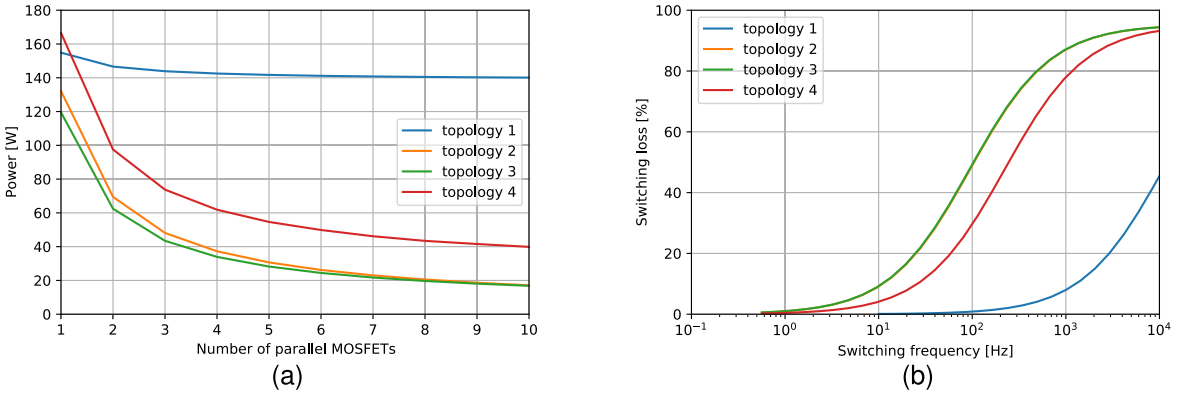

FIGURE 5. (a) Added power of the loss sources as a function of parallel MOSFETs. (b) switching losses in percentage of the total losses as a function of switching frequency.

B. SWITCHING FREQUENCY

In the analysis until now, the topologies use the lowest switching frequency possible while still meeting the current ripple requirement of 0.5%. It can be argued that is useful to use a higher switching frequency so that the current ripple can be lowered. Also a higher switching frequency causes the ripple in the magnetic signature to be damped more [12]. However, a higher switching frequency also causes more switching losses. For the topologies where the MOSFETs are placed inside the cryostat, the switching losses are even higher because of the coefficient of performance of the cooler. For an optimal design figure 5 shows the percentage that the switching losses are of the total amount of losses. For topology 1, where the MOSFETs are not placed inside the cryostat, it can be seen that the converter can operate above 1 kHz without any problems. For the topologies where the MOSFETs are placed inside the cryostat, the switching losses become too high in this range. It should also be noted that a higher switching frequency in combination with the low duty cycle that is used in this topologies can cause problems. The on-state of the MOSFETs is very short compared to the off-state. If the frequency is also high, the on time of the MOSFET might be too short to switch.

V. CONCLUSION

Several converter topologies were investigated to be applied for HTS degaussing coils in this paper. Measurements were done to validate the performance of the electronic components in liquid nitrogen. It was shown that it is more energy efficient to place the MOSFETs inside the cryostat. By doing this, the rated current for the current leads is drastically decreased and therefore the losses as well. However, by placing the MOSFETs inside the cryostat, the cooler needs to lift more heat. This is an inefficient process. This can be counteracted by placing multiple MOSFETs in parallel so that the conduction losses inside the cryostat are limited. As a side effect of cooling and paralleling the MOSFETs, the time constant of the load increases. This is beneficial for the energy efficiency of the converter. By adding a smoothing capacitor inside the cryostat, the current leads can be made even smaller. This also limits the need for large peak currents from the current source. It is not useful to use a transformer to completely remove the current leads. The secondary coil and the rectifier inside the cryostat introduce more losses than that the elimination of the current leads yield. Besides, a transformer makes the circuit more complex.

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