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An Energy-Efficient Capacitively-Biased Diode-Based Temperature Sensor in 55-nm CMOS

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***Abstract*—This work presents an energy-efficient diode-based CMOS temperature sensor. It is based on the capacitively-biased diode (CBD) working principle and can operate with a 1-V supply voltage. Instead of using a separate CBD front-end and ADC, a new architecture is proposed in which the CBD front-end is directly embedded into the 1^{st} stage of a 1-bit 2^{nd}-order switched-capacitor $\Sigma\Delta$-ADC, thereby improving both energy efficiency and accuracy. The circuit was fabricated in a standard 55-nm CMOS process and occupies an active area of 0.021 mm^2. The measured inaccuracy is $\pm$0.6°C (3σ) from -55 to 125 °C after a 1-point calibration. Furthermore, it consumes 2.2 μW and achieves a resolution of 15 mK in a conversion time of 6.4 ms, which corresponds to a competitive resolution FoM of 3.2 pJ·K^2.**

***Index Terms*—CMOS temperature sensor, diode, energy efficient, capacitively-biased.**

I. Introduction

CMOS temperature sensors are essential parts for many applications, such as on-chip thermal management [1], [2] and frequency compensation [3]. Among the different types of CMOS temperature sensors, BJT or diode-based types are the most widely used thanks to their high accuracy and low calibration cost. However, traditional designs usually require an over-1V supply voltage [4], [5], and their accuracy degrades in advanced CMOS processes [6]. To improve the performance of such sensors in advanced process nodes, capacitively-biased 'diodes' (CBD) was explored recently [1], [2]. A simplified diagram of the CBD structure and its simulated behavior at different temperatures and initial voltages is shown in Fig. 1. If a pre-charged capacitor discharges through a diode, the diode voltage V_D follows a logarithmic function of time regardless of the initial voltage after an initial short period (tens of ns) [1]. For the same reason, V_D is insensitive to supply noise. With a fixed discharging interval, the residual voltage V_D is complementary to absolute temperature (CTAT). A proportional-to-absolute-temperature (PTAT) voltage ΔV_D can also be generated by two CBDs with different discharging intervals. Advantageously, the CBD front-end only has dynamic power and is compatible with a sub-1V supply voltage.

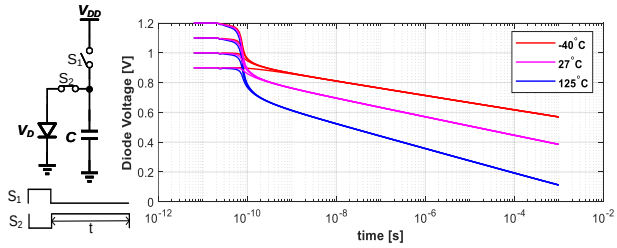

Fig. 1. Working principle of the CBD structure.

Recently, several CBD-based temperature sensors have been reported. In [1], a CBD front-end is combined with a SAR ADC, which can work with a low supply voltage of 0.85 V and achieves a compact area of 2500 μm^2 in a 16-nm FinFET process. However, its energy efficiency (>20 pJ·K^2) is limited. A relaxation-oscillator-based readout scheme was proposed in [2] , which achieves a state-of-art energy efficiency of 0.36 pJ·K^2. However, its 1.8% relative inaccuracy (R-IA) is still inferior to traditional BJT-based designs after a 1-point trim. In general, despite the mentioned advantages of the CBD principle, it is still challenging to use it in a temperature sensor with both high accuracy and high energy efficiency.

This letter is an extension of [7]. It presents an energy-efficient CBD-based temperature sensor, where the CBD front-end is embedded in a switched-capacitor (SC) $\Sigma\Delta$ ADC directly, thereby improving both the sensor's energy efficiency and accuracy. Fabricated in a standard 55-nm CMOS process, it achieves a relative inaccuracy of 0.67% in a wide temperature range of -55 °C to 125 °C and has a competitive resolution FoM of 3.2 pJ·K^2.

II. Working Principle

Fig. 2 shows the working principle of this CBD-based temperature sensor. By using two CBD structures with different discharging intervals t_1 and t_2, CTAT voltages V_{D1} and V_{D2} can be generated. Their difference voltage $\Delta V_D = V_{D1} - V_{D2}$ is PTAT. To boost the temperature sensitivity of ΔV_D, a large but accurate time ratio t_2/t_1 (e.g.,128) can be easily achieved in the digital domain by dividers. By using ΔV_D as the input signal, and V_{D1} as the reference voltage, the ratio X=$\Delta V_D/V_{D1}$ can be digitized by an ADC. As shown in Fig.

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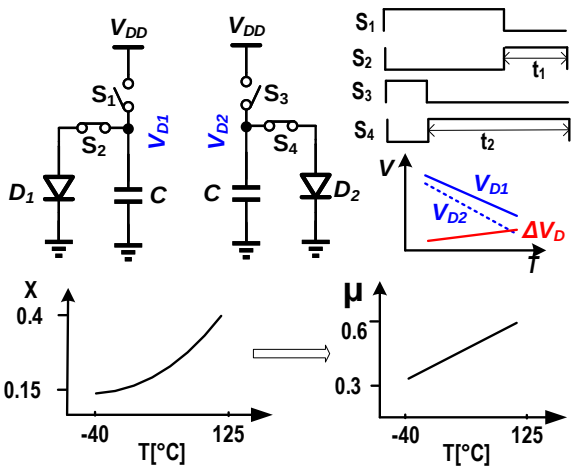

Fig. 2. Working principle of the CBD sensor

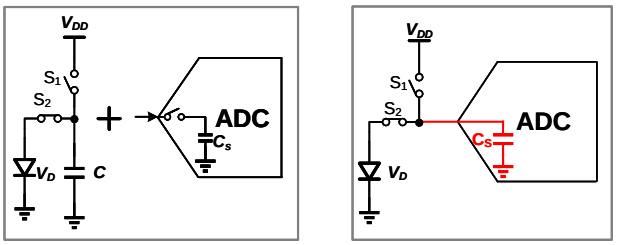

Fig. 3. (a) Separated CBD front-end and ADC; (b) Merged CBD and ADC.

2, although X is a nonlinear function of temperature as in [8], it can be linearized in the digital domain:

$$\mu = \frac{k\Delta V_D}{k\Delta V_D + V_{D1}} = \frac{k \cdot X}{k \cdot X + 1} \tag{1}$$

and then converted to temperature with

$$T = A \cdot \mu + B \tag{2}$$

where k, A, and B are fitting coefficients.

To digitize X=$\Delta V_D/V_{D1}$, the temperature sensor consists of a CBD-based front-end and an ADC. Traditionally, the front-end and the ADC are designed separately, as shown in Fig. 3(a). However, due to the passive nature of a CBD front-end, the residual voltage on the capacitor has a limited driving capability. To drive the ADC's sampling capacitor, a relatively large capacitor in the CBD front-end or an additional voltage buffer is required. In either case, this will increase the area and power consumption. To address this issue, a new architecture is proposed in which the capacitor in the CBD front-end is merged with the sampling capacitor in the SC ADC directly. As shown in Fig. 3(b), the sampled temperature-dependent voltages can then be digitized directly without additional circuitry, thus improving both energy efficiency and accuracy.

In this work, the CBD front-end is embedded into the 1^{st} stage of an incremental 1-bit 2^{nd} order SC $\Sigma\Delta$-ADC. Fig. 4 shows the simplified diagram of this sensor. To make the CBD front-end compatible with the 1-bit DAC of the SC $\Sigma\Delta$-ADC,

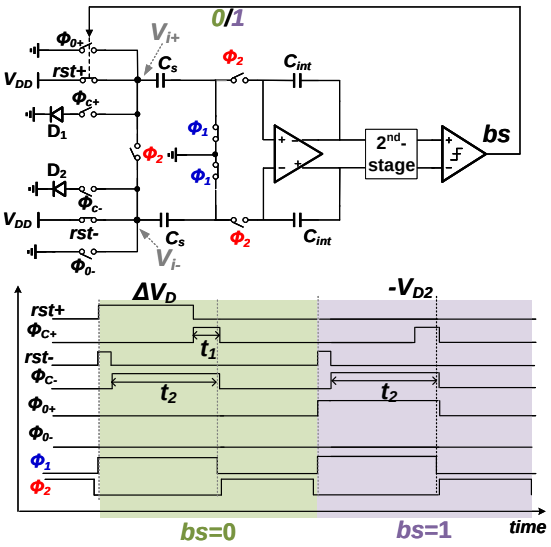

Fig. 4. Block and timing diagram of the proposed temperature sensor.

a bit-stream (bs) dependent sampling scheme is employed [9]. When the output of the modulator bs is 0, ΔV_D is processed by the loop, while for bs=1, $-V_{D2}$ is processed. This results in a bs average equal to X=$\Delta V_D/V_{D1}$. Then X can be linearized and converted to temperature by (1) and (2).

The timing diagram of the proposed sensor is shown in Fig. 4, where the sampling phase ϕ_1 is divided into several sub-phases. To generate ΔV_D when bs=0, the differential-input sampling capacitors C_S (500fF) are charged to V_{DD} during the reset phase rst_+/rst_-. During ϕ_{C+} and ϕ_{C-}, the capacitors C_S in the positive and negative branches discharge through two diodes with time intervals of t_1=25 ns and t_2=3.2 μs, respectively. Both of them stop discharging at the end of ϕ_1, generating ΔV_D. When bs=1, $-V_{D2}$ is generated by shorting V_{i+} to ground during ϕ_1, such that only the $-V_{D2}$ term remains from V_{i-}. During ϕ_2, the inputs are shorted together, allowing input common-mode tracking.

III. Circuit Implementation

In this work, two kinds of CBD-based sensors are designed with the same readout interface. One of them use P+/Nwell diodes as sensing elements, while the other one is based on diode-connected parasitic PNP transistors. Both types have the same p-n junction area of 20 μm^2. However, the P+/Nwell diode does not have the usual ring of P+ substrate contacts around the Nwell. As a result, most of the current will flow via the Nwell to ground.

Fig. 5 shows the circuit implementation of the switches in the CBD front-end. To reduce the leakage current while keeping small parasitic capacitance, a minimum size T-switch is used for S_1. As a result, one of the two PMOSFETs is always in the deep cutoff region. To achieve both small on-resistance and small leakage current, S_2 is implemented with a NMOS I/O transistor (thick oxide). An on-chip clock booster is used to drive it with a 1-V supply voltage.

As shown in Fig. 6, a 1-bit 2^{nd} order feed-forward SC $\Sigma\Delta$-modulator is employed in this work. To achieve high

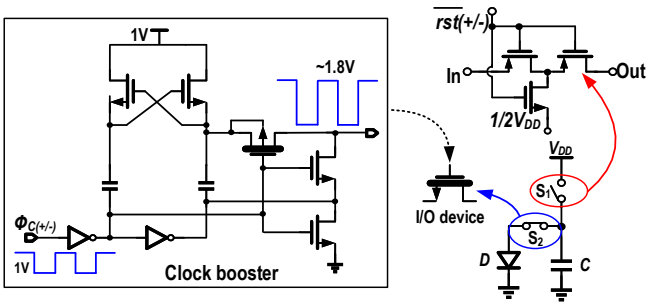

Fig. 5. Switch implementation in the CBD front-end.

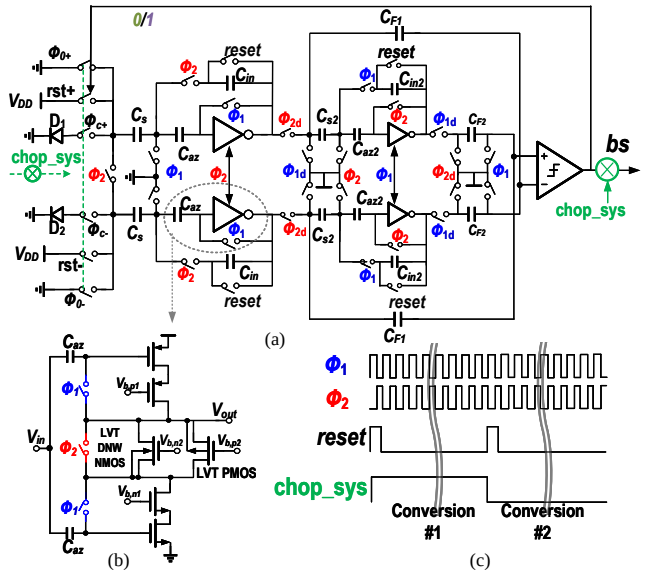

Fig. 6. (a) Circuit diagram of the temperature sensor; (b) implementation of the inverter-based amplifier; (c) timing diagram of the system-level chopping.

energy-efficiency, pseudo-differential inverter-based amplifiers [10] are used in both integrators. The amplifier is auto-zeroed to reduce its offset and 1/f noise. The auto-zero capacitor C_{az} in the first integrator is 2 pF, which is 4x larger than the sampling capacitor C_S to mitigate its folded noise. As in [11], a SC common-mode feedback (CMFB) circuit is used to avoid output common-mode drift. To operate from a 1-V supply voltage, floating current sources are implemented with low threshold voltage (LVT) transistors, with their bodies tied to their sources to further lower their threshold voltages. Since the floating current sources only define the current during ϕ_1, the LVT transistors will not degrade the amplifier's gain during ϕ_2 (>60dB over corners). The first integrator draws 500 nA while the second stage draws 250 nA. To reduce residual offset, system-level chopping is applied to the modulator over two conversions [9]. The modulator is reset at the beginning of each conversion. The input chopper is implemented by multiplexers in the digital domain to swap the input control timing signals, thereby avoiding the need for extra analog switches.

The phase signals shown in Fig. 4 are generated by on-chip control logic, derived from an external 40-MHz clock. To generate the pulse width of t_1 and t_2 from the system

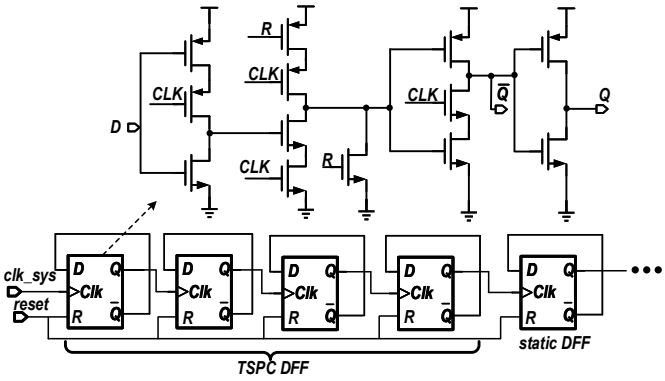

Fig. 7. Circuit diagram of the TSPC DFF-based dividers.

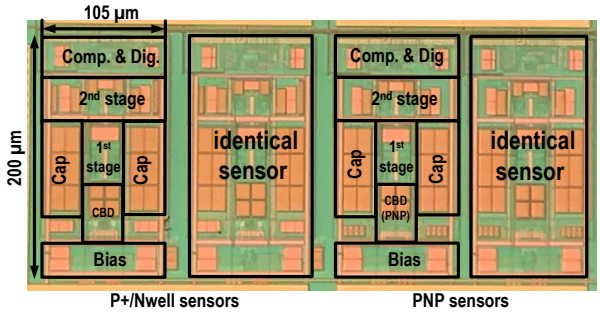

Fig. 8. Die photo of the proposed temperature sensors.

clock, a clock divider chain is required, which dominates the digital power. As shown in Fig. 7, dynamic true single phase clock (TSPC) D flip-flops (DFFs) are employed in the first four stages of the clock divider circuit. According to simulations, this saves about 30% of power compared to traditional static DFFs. To avoid reliability issues at low frequencies, static DFFs are used in the following stages.

IV. Measurement Results

As shown in Fig. 8, four sensors per chip were fabricated in a standard 55-nm CMOS process, each occupying 0.021 mm^2. Two of them use P+/Nwell diodes as sensing elements, while the other two are based on diode-connected parasitic PNP transistors. Measured at room temperature, each sensor consumes 2.2 µW from a 1-V supply, about 50% of which is dissipated by the digital logic. For flexibility, the sinc^2 decimation filters are implemented off-chip.

Sixteen chips (32 sensors of each type) were characterized from -55 °C to 125 °C. As shown in Fig. 9 (top), all the sensors have a similar temperature dependency. After the linearization with eq. (1) and (2), the sensors show untrimmed 3σ inaccuracies of ± 2.8 °C (P+/Nwell) and ± 3.7 °C (PNP) without system-level chopping, respectively. As shown in Fig. 9 (middle), the errors drop to ± 1.4 °C (P+/Nwell) and ± 1.6 °C (PNP) with system-level chopping. After a 1-point offset trim and fixed systematic error correction, the 3σ inaccuracies become ±0.6 °C (P+/Nwell) and ±0.8°C (PNP) from -55 °C to 125 °C.

FFTs of the bit-stream outputs of both sensors are shown in Fig. 10. Both sensors have similar noise floors, which are

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Parameters	This work	[1]	[2]	[4]	[5]	[6]
Tech.(nm)	55	16	28	160	180	22
Type	Diode	Diode	MOS	PNP	NPN	PNP/ MOS
Area (mm^2)	0.021	0.0025	0.017	0.16	0.35	0.0043
Supply (V)	1-1.3	0.85-1	0.85-1.15	1.5-2	1.6-2.2	0.97-1.3
Power (μW)	2.2	18	33.75	6.9	9	50
T. Range (°C)	-55 to 125	-15 to 105	-10 to 90	-55 to 125	-40 to 125	-30 to 120
Inaccuracy (°C)	±0.6	+1.5/ -2.0	±0.9	±0.06	±0.13	±1.07
R-IA(%)	0.67	2.9	1.8	0.06	0.16	1.4
Trim points	1	0	1	1	1	1
Resolution (°C)	0.015	0.3	0.01	0.015	0.00167	0.58
Tconv (ms)	6.4	0.013	0.1	5	218	0.032
Res. FoM* (pJ·K^2)	3.2	21	0.36**	7.8	5.4	540

* Res. FoM = Energy/Conversion · Resolution^2
** Excluding the frequency-to-digital converter

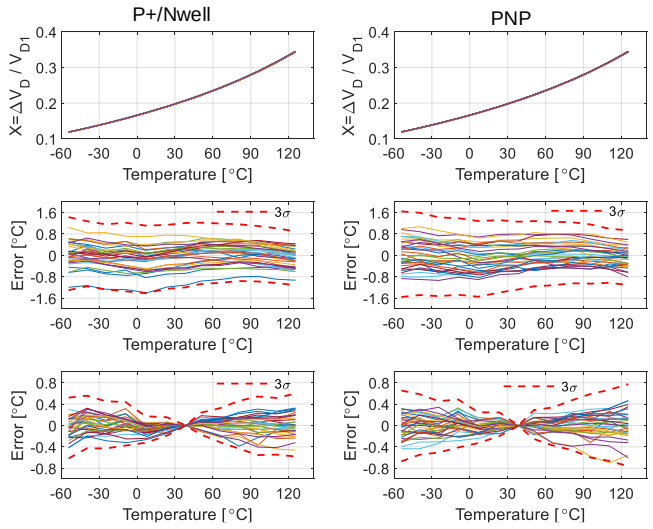

Fig. 9. Measured digital output of the P+/Nwell and PNP sensors (top); measured untrimmed errors (middle) and errors after 1-point trim and fixed systematic non-linearity correction (bottom).

dominated by the kT/C noise of the SC readout interfaces. To evaluate the resolution accurately, the effect of ambient temperature drift is suppressed by differential measurements on identical sensors [3]. Fig. 10 (bottom) shows the measured resolution vs. conversion time plot of both sensors. The sensors achieve a resolution of 15 mK in a conversion time of 6.4 ms, which corresponds to a resolution FoM of 3.2 pJ· K^2. At room temperature, the P+/Nwell sensor has a supply sensitivity of 3.7 °C/V from 1 V to 1.3 V, which is limited by the supply dependent on-resistance of the sampling switch (S_2 in Fig. 5). The residual IR voltage drop across the switch will add to the diode voltage, thus causing this error.

V. Comparison and Conclusion

The proposed P+/Nwell sensor's performance is summarized in Table I and compared to the state-of-the-art. Compared

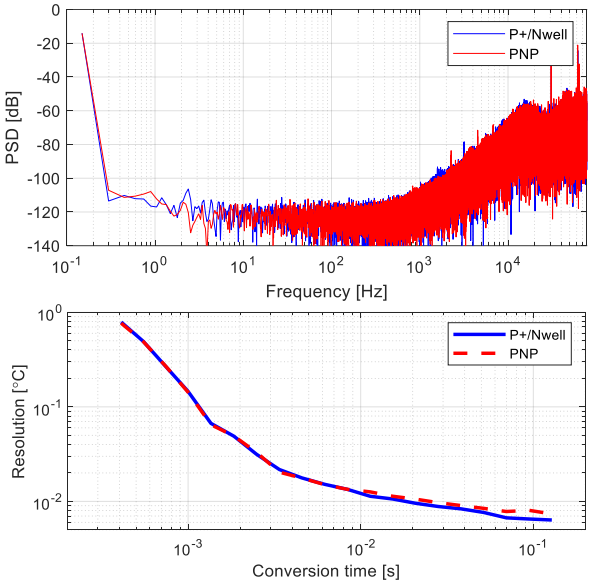

Fig. 10. PSD of the free-running sensor output bit-stream (top); resolution vs. time plot (bottom).

to other CBD sensors [1], [2], this design has a much wider temperature range from -55 to 125 °C and a better relative inaccuracy of 0.67%. Compared to traditional designs [4], [5], this sensor can operate from a 1-V power supply and achieve a competitive resolution FoM of 3.2 pJ·K^2.

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