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Graphene-based Complementary-Style Logic Gate with Memory-Lock.

Nicoleta Cucu Laurenciu[1], and Charles Timmermans[1], and Nicolo de Groot[1], and Sorin D. Cotofana[2]

***Abstract*— As CMOS feature size vertiginously approaches atomic limits, high leakage and power density and exacerbating IC production costs are prompting for development of new materials, devices, beyond von-Neumann architectures and computing paradigms. Within this context, graphene has emerged as a promising post-Si front runner, owing to its remarkable properties. In this paper, we propose a generic graphene-based complementary-style Boolean gate structure with memory-lock, that allows logic and non-volatile memory co-location. The gate with memory-lock is composed of 2 cells - a pull-up cell performing the gate Boolean function and a pull-down cell performing the inverted Boolean function. Each cell in turn, has a graphene logic layer that carries out Boolean gates computation, and a graphene memory layer for storing the logic state of the gate. As simulation vehicle we considered an inverter gate with memory-lock. Simulation results indicate a current ratio of write/read to/from memory of $1.64 \cdot 10^2$ for gate input low, and of $2.55 \cdot 10^2$ for gate input high. Furthermore, the inverter with memory-lock exhibits a $128\times$ smaller area footprint when compared to the traditional physically separate logic (e.g., 7nm inverter gate) and memory (e.g., 7nm 6T SRAM cell), establishing the potential of proposed structure with memory-lock for more compact and energy efficient future beyond CMOS nano-electronic implementations, and making it highly promising for high-density computations.**

I. Introduction

The ever increasing need for miniaturization, faster execution speed, cost reduction, and lower power consumption has been steadfastly sustained in the past by CMOS aggressive downscaling. However, as atomic dimension limits are being approached, novel solutions at the circuit, device and material level, are highly demanded in order to keep the pace with the market computing necesities. Furthermore, with the data deluge continuously increasing, the Von-Neumann architectures, where memory units and processing units are physically separated, cannot keep the pace anymore and are exhibiting rapidly growing performance bottlenecks. Having the memory co-located together with the logic, offers a viable manner of overcoming to a certain extent these bottlenecks. One strand of research in this direction that is showing potential is constituted by in-memory computing. Non-Boolean threshold logic with latching ability have been proposed [1]. Various 3D transistor-alike structures with a stack of materials devised such that it can perform logic but also have some ability to retain information on different time scales have been proposed, e.g., floating-gate FET [2], [3], [4], ferroelectric FET, [5] etc. Tunneling phenomena are one of the primary mechanisms underlying these transistors operation.

At the same time, various 2D materials have merged, with graphene and carbon-based nanoelectronics being one of the potent contenders to Si based counterparts [6], [7]. Graphene is a 2D carbon atom honeycomb lattice with a set of properties which when taken together are unique and quite remarkable, notably room temperature electron mobility that is $10\times$ higher than Si, low effective electron masses, ultimate thinness, high thermal conductivity, as well as ballistic carrier transport with long carrier mean-free paths [8], [9], [10]. In the past few years, a growing number of theoretical and experimental studies looking at the 2D-2D tunneling in vertical graphene-insulator-graphene heterostructures, have been published [11], [12], [13], [14], [15], [16], [17], [18], [19]. Some of such devices however often require cryogenic temperatures for their operation, or the presence of a magnetic field, or they make use of high voltages, which can be rather cumbersome aspects from a circuit design standpoint in the sense they involve additional provisions to ensure the operation conditions. Furthermore, for some devices, the tunneling-based memory reading process is often destructive for the stored information, i.e., reading can be done one time only.

In this paper, we propose a complementary style Boolean gate with memory-lock. The gate relies on two cells with memory-lock. One cell can be regarded as a 3D structure with 2 layers: one graphene layer which performs logic computation, and another graphene layer on top that performs the memory function. The two graphene layers are separated from each other by tunneling h-BN layer(s). The band-gap opening and ballistic transport through the graphene logic layer are modulated via source, drain, top gate, and back gate voltages, while an additional control gate placed on top of the memory layer facilitates the memory operation. The cell can function either as logic only (by disabling the memory layer), or as a logic with memory, when making use of the control gate as well. Two such logic cells with memory-lock are arranged complementarily in order to form a logic gate, e.g., for an INV gate, the upper cell maps INV functionality onto its conductance, while the down cell maps BUFFER functionality onto its conductance. Conceptually speaking the construction is similar to the way an inverter gate is created with a p-MOS and an n-MOS transistor. However, functionally speaking, we are not dealing with transistors, as the logic layer can map the function of an entire gate and not only of one transistor. It was shown previously in the literature that Boolean gates can be constructed in various ways with

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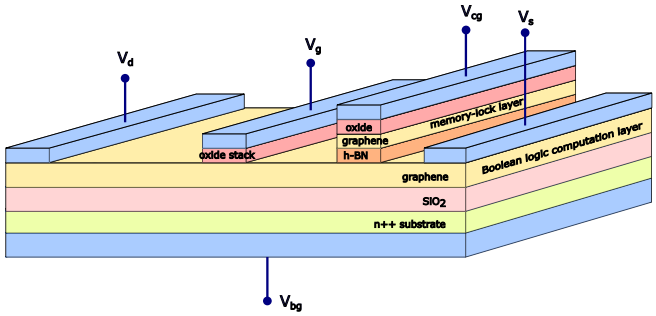

Fig. 1: 3D structure of a GNR-based logic cell with memory-lock.

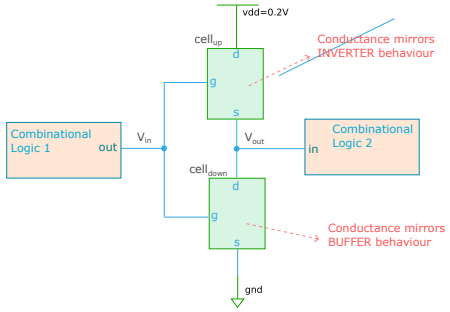

Fig. 2: Complementary-style GNR-based inverter Boolean gate with lock memory.

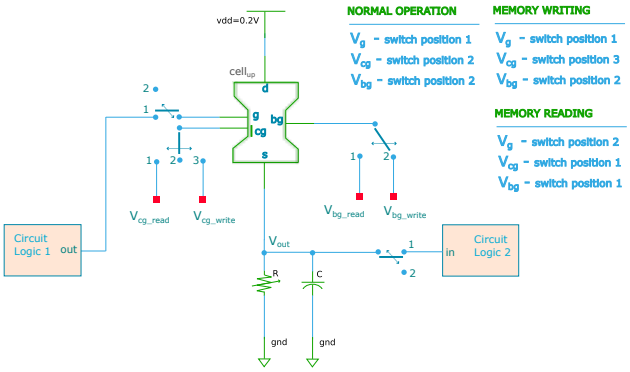

Fig. 3: Circuit diagram of considered test case.

GNR devices [20], [21], [22], [23]. Simulation results for an inverter upper cell indicate a current ratio of $1.64 \cdot 10^2$ when the gate logic state for gate logic input $V_g = 0\,\mathrm{V}$ is written/read to/from memory, and a ratio of $2.55 \cdot 10^2$ for the case when the gate logic input is $V_g = 0.2\,\mathrm{V}$. Furthermore, when compared to traditional combination of physically separate logic and memory (e.g., inverter gate + 6T SRAM cell in 7nm FinFET CMOS), the proposed inverter gate with memory-lock results in $128\times$ area savings. Thus, colocating logic and memory via proposed complementary-style logic gate with memory-lock, results in a more compact and energy efficient implementation, facilitating higher parallelism and more complex computing with smaller footprint, and making it highly promising for high-density computations.

The remaining of this paper is structured as follows: Section II presents the proposed device structure and modus operandi. Section III outlines the computation model formalism underlying the device physical operation, while Section IV entails the obtained simulation results and discusses potential use cases. Finally, we conclude the paper with some remarks in Section V.

II. Device Structure and Operation

In this section, we first describe the structure of a Graphene Nanoribbon (GNR)-based cell with memory-lock, and then we exemplify the modus operandi of an inverter gate with memory-lock. We note however, that this is by no means restrictive and the same design principles could be extended as well to other Boolean gates with one or two inputs.

A. Device Structure

Figure 1 depicts the 3D structure of the proposed device. It consists primarily of a graphene logic layer and a graphene memory-lock layer. The graphene logic layer mirrors the Boolean functionality in its conductance as a result of external voltages induced modulation (i.e., drain V_d, source V_s, top gate V_g and back gate V_{bg}). Additionally the GNR geometry and contacts topology play an important role as well to the GNR band-gap opening and conductance behaviour. The graphene memory-lock layer is separated from the logic layer by h-BN tunneling layer(s). h-BN is a 2D layer material featuring a wide bandgap ($\approx 5.97\,\mathrm{eV}$), and is frequently employed as an atomically thin tunneling barrier and high quality insulator [16]. The memory-lock layer acts similarly to a floating gate and serves for storing the state of the logic layer for later usage. This state can be mirrored from the logic layer to the memory layer via tunneling mechanisms, and will be preserved in memory while the memory layer is disconnected from power (V_{cg} disconnected). The reading of the memory state is nondestructive, and is accomplished by mirroring the state back from memory to the logic layer to be used for further propagation through the rest of the circuit. By combining 2 such cells in a complementary manner, one can obtain a Boolean gate, as exemplified in Figure 2 for an inverter gate. The gate comprises an upper cell with memory-lock and a down cell with memory-lock that operate in a complementary manner. Specifically, the upper cell logic layer conductance will map a Boolean inverter functionality, while the down cell logic layer conductance will map a Boolean buffer functionality. The memory layers GNRs will also store charges complementarily. Further, for easiness of discourse, we restrict our discussion to the upper cell with memory-lock, while the down part is replaced with a resistor, as illustrated in Figure 3.

B. Writing

During the writing process, the gate voltage V_g is connected to the circuitry output from amont. The logic layer performs a certain desired Boolean functionality, and the afferent logic state will be mirrored to the memory layer. When writing from the logic layer to the memory layer, the applied control gate voltage value V_{cg} should be such that when we have

a low current in the logic layer, it will result in little to none tunneling of carriers in the memory layer, while a high current in the logic layer will result in carriers tunneling to the memory layer. Once the writing is completed, power is removed from the memory layer by letting V_cg floating, in order for the memory layer to preserve the stored charges to some indefinite extent.

C. Reading

When reading, the applied control gate voltage V_{cg} value should be such that the charges stored on the memory layer will not tunnel back to the logic layer. The memory layer would thus behave like a doped insulator, that will yield a voltage drop across the h-BN layer(s) of Q_{stored}/C_{hBN}. For logic "1" stored in memory we have $Q_{stored} \neq 0$, and thus the modulation of the logic layer channel by the V_{cg} will be smaller, while for logic "0" as there are no charges stored in the memory layer, the effect of V_{cg} on the logic layer conduction will be higher. When reading, V_g is disconnected from the amont circuit, as to not perturb the logic value that is being read from the memory.

D. Erasing

Charge erasure from the memory layer, is accomplished by applying a negative gate control voltage V_{cg}, that will enable deplete the charge stored in memory via carriers tunneling. Every write operation is preceded by an erase stage.

III. Modelling Formalism

When a positive control gate voltage V_{CG} is applied on the memory layer, an energy difference between the 2 graphene layers Dirac points will be induced. As the Fermi level of the memory layer is shifted upwards towards the conduction band, and the Fermi level logic layer is shifted downwards towards the valence band, the tunnel barrier height is reduced, and electrons can tunnel from the filled states in the logic layer to the empty states in the memory layer. Similarly for a negative control gate V_{CG}, the carriers can tunnel from the memory layer to the logic layer. Thus, the applied bias and control voltages modify the electrochemical potentials (Fermi levels) of the graphene layers, which in turn dictate the transport properties. Subsequently, in Section III-A we derive the Fermi shifts for the 2 graphene layers and in turn the carrier densities, while in Section III-B we present the used formalism governing the transport in the logic layer.

A. Vertical Tunneling-Induced Fermi Shifts

Figure 4 graphically exemplifies for the case of tunneling from logic to memory, the energy bands for the 2 graphene layers separated by the h-BN tunneling barrier. In this figure, ϵ_{DL} and ϵ_{DM} denote the Dirac points, μ_L and μ_M the electrochemical potentials, and ΔE_{FL} and ΔE_{FM} the Fermi energy shifts with respect to the Dirac points for the logic and memory graphene layer, respectively. V' and V'' are the voltage drops across the control gate oxide, and h-BN tunneling layer, respectively, and U_L is the logic

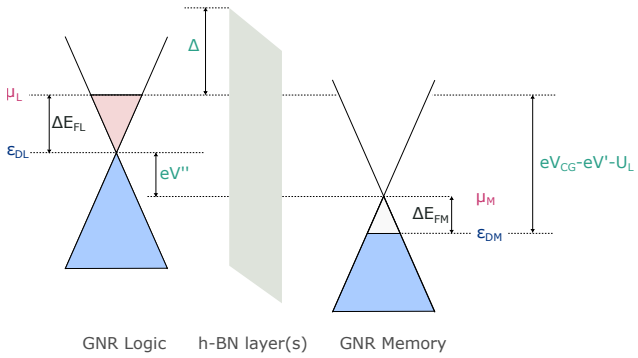

Fig. 4: Energy band diagram of the device.

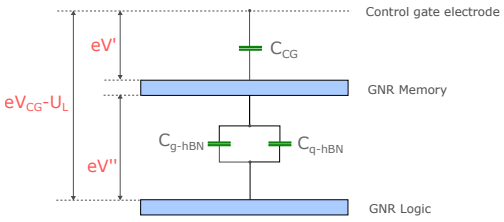

Fig. 5: Equivalent capacitive circuit.

layer channel potential. From Figure 4 ensues the following relation:

$$e\,V_{CG} - U_L = e\,V' + \Delta E_M + e\,V'' + \Delta E_L. \quad (1)$$

Let $\sigma_{1,M,L}$ denote the surface charge densities for the control gate, graphene memory layer and graphene logic layer respectively. The charge neutrality condition demands $\sigma_1 + \sigma_M + \sigma_L = 0$, and expressing the charges with reference to Figure 5, results in:

$$\begin{aligned} &\sigma_1 = C_{CG} \cdot V'; \quad \Rightarrow \quad -\sigma_M - \sigma_L = C_{CG} \cdot V' \\ &\sigma_L = C_{hBN} \cdot V'', \end{aligned} \quad (2)$$

where $C_{hBN} = C_{g-hBN} + C_{q-hBN}$ is the equivalent capacitance of the h-BN layer obtained by connecting in parallel the geometric and the quantum capacitance of the h-BN layer [24], while $C_{CG} = \epsilon_0 \cdot \epsilon_{r_{ox}}/d_{ox}$ is the control gate oxide capacitance. Equations 2 and Equation 1 are then solved numerically for ΔE_M and ΔE_L.

σ Computation: The total carrier density σ on each graphene layer follows $\sigma = e\,(n - p + N_D - N_A)$, where N_D and N_A are the n-type and p-type doping concentrations for the graphene, and n and p are the electrons and holes 2D carrier densities.

$$\begin{aligned} n &= \int_0^{\infty} D(E) \cdot T_{WKB}(E) \cdot [f_0(E - \Delta E)]\, dE \\ p &= \int_{-\infty}^{0} D(E) \cdot T_{WKB}(E) \cdot [f_0(\Delta E - E)]\, dE, \end{aligned} \quad (3)$$

where $f_0(E)$ denotes the Fermi-Dirac distribution function at temperature T, $D(E)$ is the density of states per unit area of graphene, and $T_{WKB}(E)$ is the graphene to graphene interlayer tunneling probability of carriers. The density of

states, $D(E)$, reads as [25]:

$$DoS(E) = \frac{g_s\, g_v\ |E|}{2\pi(\hbar\, \nu_F)^2} \tag{4}$$

with ν_F the Fermi velocity of carriers ($\approx c/300$), g_s and g_v the spin and valley degeneracy which in the case of graphene are both equal to 2. For the logic layer, there are also carriers from the drain to source conduction that need to be accounted for, and the density of states is computed self-consistently from Poisson-NEGF procedure, as detailed in Section III-B. The tunneling probability T_{WKB}, is estimated via the Wentzel-Kramers-Brillouin (WKB) approximation [26] as:

$$T_{\text{WKB}}(E) \approx exp\left(\frac{-2\sqrt{2\,m^*}}{\hbar} \cdot \int_0^d \sqrt{(\Delta(x) - E_x)}\, dx\right), \tag{5}$$

where E_x is the incident electron energy in the direction perpendicular to the barrier, m^* denotes the effective mass of electron (hole) inside the hBN barrier, $\hbar$ is the reduced Planck constant, $\Delta(x)$ is the barrier height at position x in the barrier (the energy gap between graphene valence/conduction band and hBN valence/conduction band), d is the thickness of the tunnel barrier (for one hBN layer d =3.4 Å), Δ =1.5 eV, and $m^* = 0.5 \cdot m_0$, where m_0 is the free electron mass [27], [28], [16].

B. Logic Layer Transport

The graphene logic layer is described by a Hamiltonian matrix $H = H_0 + U_L$, which models the interactions between neighbour carbon atoms (via H_0), and incorporates all the external as well as the internal potentials (e.g., top gates voltages, and back gate voltage) via U_L. H_0 is constructed by using semi-empirical (tight-binding) calculations, as follows:

$$H_0 = \sum_{i,j} t_{i,j}\, |i\rangle\, \langle j|\,, \tag{6}$$

$$\text{where } t_{i,j} = \begin{cases} \tau, & \text{if atoms } i \text{ and } j \text{ are adjacent} \\ 0, & \text{otherwise.} \end{cases} \tag{7}$$

First nearest-neighbor (1NN) interactions are accounted for via hopping energy between atoms $\tau = -2.7\,\text{eV}$. The potential distribution matrix U_L is determined self-consistently as the solution of the 2D Poisson equation:

$$\nabla \cdot [\epsilon(\mathbf{r})\ \nabla U_L(\mathbf{r})] = -\frac{\rho(\mathbf{r})}{\epsilon_0}, \tag{8}$$

where $\mathbf{r} = x\hat{\mathbf{x}} + y\hat{\mathbf{y}}$ is a position vector in space, $\epsilon(\mathbf{r})$ is the dielectric permittivity of the materials at position $\mathbf{r}$, and ρ represents the net charge density distribution. The Poisson equation is numerically solved by making use of the finite difference method. The drain and source contacts with different electrochemical potentials sustain the logic layer channel conduction. The interactions between the 2 contacts and the channel are modelled via the contact self-energy matrices Σ_S and Σ_D, respectively. The transmission function $T(E)$, which models the probability of one electron being transmitted between the source and the drain contacts, is given by:

$$T(E) = \text{Trace}\left[\Gamma_D\ G_R\ \Gamma_S\ G_R^\dagger\right] \tag{9}$$

where

$$G_R(E) = [EI - H - \Sigma_D - \Sigma_S]^{-1}, \tag{10}$$

$$\Gamma_{S,D} = i[\Sigma_{S,D} - \Sigma_{S,D}^\dagger]. \tag{11}$$

The carriers charge density per unit energy $N_L = n_L - p_L - (N_{DL} - N_{AL})$, with

$$\begin{aligned} n_L &= \frac{1}{2\pi} \cdot \int_{-\infty}^{\infty} \text{Trace}\left[G_R \cdot G^n(E) \cdot G_R^\dagger\right] dE \\ p_L &= \frac{1}{2\pi} \cdot \int_{-\infty}^{\infty} \text{Trace}\left[G_R \cdot G^p(E) \cdot G_R^\dagger\right] dE, \end{aligned} \tag{12}$$

with $G^n(E) = \Gamma_D \cdot f_0(E - \mu_D) + \Gamma_S \cdot f_0(E - \mu_S)$, and $G^p(E) = \Gamma_D \cdot (1 - f_0(E - \mu_D)) + \Gamma_S \cdot (1 - f_0(E - \mu_S))$.

The channel current is derived using Landauer formula, as:

$$I = \frac{q}{h} \int_{-\infty}^{+\infty} T(E) \cdot (f_0(E - \mu_D) - f_0(E - \mu_S))\ \text{d}E, \tag{13}$$

where $\mu_{S,D}$ represent the source and drain contacts Fermi energy. Finally, the conductance, when the logic layer GNR is exposed to the bias voltage $V = V_\text{D} - V_\text{S}$, writes as:

$$G = \frac{I}{V_D - V_S}. \tag{14}$$

IV. Simulation Results

Subsequently, we present the topology of an inverter cell with memory-lock, validate its correct operation, and further discuss on potential utilization scenarios. The inverter cell we shall discuss about forms the upper part of an inverter Boolean gate, and as illustrated in Figure 3 the complementary down buffer cell was replaced by a resistor, as to not complicate the proof of concept. Figure 6 graphically illustrates the GNR shape for the logic layer of the upper inverter cell from a Boolean inverter gate. The GNR geometry and gates topology were optimized for 0.2 V operating voltage, mainly motivated by the fact that we wanted a proof of principle while maintaining the GNR dimensions within a feasible range. Figure 7 describes the biasing of the cell when in memory write / memory read mode, and the afferent drain to source current behaviour. From Figure 7, it can be observed for the cell write mode that when logic input V_g =0 V is applied, there is little to none variation in the output current, and tunneling is inhibited. When applying V_g =0.2 V the current increases 2 orders of magnitude, as charges are from the logic layer are tunneled to the memory layer. For the cell reading mode, when there charge is not present in the memory layer, V_{cg} will modulate to a larger extent the drain to source current when compared to the case when charge is present in the memory. The cell erasure mode precedes every write stage, and is enabled by a V_{cg} =−0.3 V.

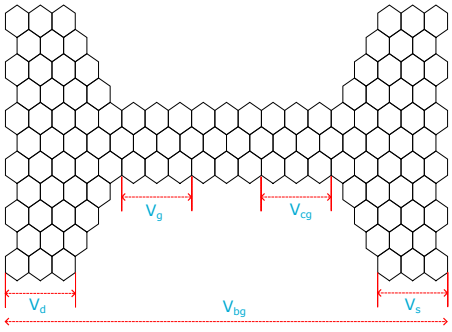

Fig. 6: Logic layer GNR geometry for the inverter cell with memory-lock.

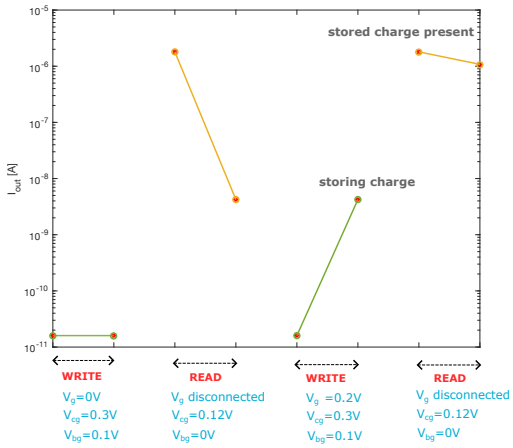

Fig. 7: Output current of the inverter graphene cell with memory-lock.

Simulation results indicate a current ratio of $1.64 \cdot 10^2$ when the gate logic state for gate logic input low (V_g =0 V) is written/read to/from memory, and a ratio of $2.55 \cdot 10^2$ for the case when the gate logic input is high (V_g =0.2 V).

A potential advantage of building a gate with 2 cells arranged in a complementary manner is that this introduces a certain degree of freedom at design time, in the sense that the desideratum performance (low leakage current, high ON/OFF current ratio, etc.) is related foremost to the whole system of 2 cells rather than to the individual cells. Thus one cell could in principle deviate from the system performance as long as its complementary cell in the gate will compensate for and the net result of the system as a whole will be the desired one. This observation holds true for both the logic layers and the memory layers in a 2-cell complementary-style gate with memory-lock.

One scenario of utilization of such gates, could be to use a buffer Boolean gate with memory-lock as a replacement for the conventional flash memory, which is currently affected by high leakage current caused by thermally induced Poole–Frenkel conduction, and as a result by low ON/OFF current ratio and high OFF state power consumption.

Another scenario of utilization would be to have the inverter Boolean gate with memory-lock as part of a circuit. During read mode, the inverter gate V_g would be disconnected from the circuit in amont as not to perturb the reading process. During the writing mode, the inverter gate output V_{out} would be disconnected from the circuit in aval. However if brief and small voltage oscillations at the output of the gate are acceptable to propagate through the rest of the circuit, then there would be no need for disconnecting the circuit in aval during cell writing. The magnitude of perturbations would depend on the matching between the complementary cells, and the ON/OFF current ratio. In normal operation mode with no biasing for the memory layer, only the logic layer would be functional and the gate would behave as a regular inverter. While we illustrated the techniques for an inverter gate with memory-lock, we note that a similar reasoning could be applied to devise other 1 or 2-input Boolean gates with memory-lock. This would allow one to save the logic state at different points in a circuit virtually cost-free (excluding the switches for the biasing network), eliminating thus the need for additional costly memory structures. To get more insight into the potential area savings, we consider in 7nm FinFET CMOS technology (V_{DD} =0.7 V) [29] a 6T SRAM cell which serves as memory + one inverter which serves as logic, and compare vs. proposed inverter gate with memory-lock in terms of active area, as illustrated in Figure 8. Since in this paper we addressed only the upper cell of the inverter gate with memory lock, we assume the area of the inverter gate is 2× the area of the inverter upper cell. The active area of the CMOS inverter is $4.84 \cdot 10^2 \text{nm}^2$, and of the SRAM cell is $9.68 \cdot 10^2 \text{nm}^2$, giving a total area of $1.45 \cdot 10^3 \text{nm}^2$ while the area of the proposed inverter with memory-lock is $1.13 \cdot 10^1 \text{nm}^2$, which translates to 128× area savings. Thus, colocating logic and memory in the same 3D structure similar to the complementary-style logic gate with memory-lock that we presented above, yields a more compact and energy efficient implementation, which in turn would enable higher parallelism and more complex operations with smaller footprint, making it highly promising for high-density computations.

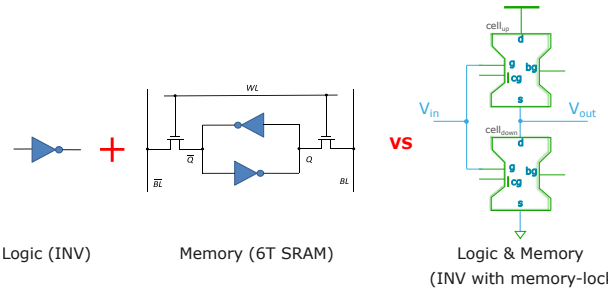

Fig. 8: Conventional separate logic + memory vs. proposed colocated logic + memory.

V. Conclusions

In this paper, we proposed a generic graphene-based complementary style Boolean gate structure with memory-lock, and investigated its potential as logic-memory colocated building block for post CMOS circuits. To this end, we introduced a generic cell with a logic graphene layer that does Boolean

computation, and a graphene memory layer on top for retaining the logic state. The two graphene layers are separated by a hBN layer(s). Combining 2 such cells in a complementary manner (from the logic functionality standpoint) yielded a Boolean gate with memory-lock. As research vehicle we considered an inverter gate, nevertheless the structure we proposed is generic and could be translated as well for other Boolean gates. Simulation results indicate a current ratio of write/read to/from memory of $1.64 \cdot 10^2$ for gate input low, and of $2.55 \cdot 10^2$ for gate input high. Furthermore, the inverter with memory-lock exhibits a $128\times$ smaller area footprint when compared to the traditional physically separate logic (e.g., 7nm inverter gate) and memory (e.g., 7nm 6T SRAM cell), establishing the potential of proposed structure with memory-lock for more compact and energy efficient future beyond CMOS nano-electronic implementations, and making it highly promising for high-density computations.

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