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4.4 A 23-to-29GHz Receiver with mm-Wave N-Input-N-Output Spatial Notch Filtering and Autonomous Notch-Steering Achieving 20-to-40dB mm-Wave Spatial Rejection and -14dBm In-Notch IP1dB

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Digital beamforming receivers (RXs) support MIMO operation and offer great flexibility and accuracy in multi-beam formation and calibration. However, compared with analog phased-array and hybrid systems, due to the absence of any rejection for spatial in-band blockers, the RX/ADC dynamic range and linearity should be high enough to prevent array saturation. Therefore, the use of self-steering spatial notch filters (SNFs) is necessary to aid the digital beamformers and reduce RX/ADC power consumption while strong blockers exist. To address that, the sub-6GHz RXs in [1,2] synthesize a baseband spatial notch impedance and translate it to RF by passive mixers. However, this technique cannot be directly applied at mm-wave frequencies as the impedance translational performance of the passive mixers degrades significantly. Hence, the mm-wave beamformer in [3] realizes a cascadable SNF at an intermediate frequency (IF). However, the front-end mm-wave components like mixers and phase shifters have to tolerate strong blockers, thus degrading RX linearity. Besides, it uses multiple IF buffers and VGAs for signal scaling and combining, which could be power-hungry if a similar method is adopted to realize a mm-wave SNF. To improve on those limitations, we propose a scalable SNF structure, which (1) suppresses the strongest in-band blocker at mm-wave frequencies, (2) supports N-input-N-output MIMOs, and (3) requires no active blocks except the phase shifters. A two-step autonomous notch-steering technique is also developed to adjust the SNF notch direction power-efficiently and accurately.

Figure 4.4.1 depicts the conceptual block diagram of the proposed mm-wave SNF. It comprises a central closed-loop autonomous notch steerer (ANS), along with a phase shifter (PS) and a bidirectional voltage-current converter (BVCC) per each element. The second ports of all BVCCs are connected to a common node X. The BVCC is a two-port network that can convert voltage to current from port-1 to port-2 with a complex forward transconductance gain of G_{21} as well as current to voltage from port-2 to port-1 with a complex backward transimpedance gain of R_{12}.

To explain the SNF operation intuitively by using the superposition theorem, first assume that the input signal is only active at the second antenna, which directly results in a voltage at the output of the second PS, V_2. The BVCC converts this voltage to a current, $I_2 = V_2G_{21}$. I_2 is then divided equally at node X and flows back towards the BVCCs of the other three branches, thus realizing the same voltage of $V_2R_{12}G_{21}/3$ at their PSs' outputs. Similarly, the output voltages of the third and fourth PS respectively generate $V_3R_{12}G_{21}/3$ and $V_4R_{12}G_{21}/3$ at the PSs' outputs of the other branches. Consequently, by considering the contributions of all antennas, the total voltage at the first PS's output is $V_{SUM1}=V_1+(V_2+V_3+V_4)\square R_{12}G_{21}/3$. Note that $V_1=V_2=V_3=V_4$ as the blockers' amplitudes are the same at the input of RX branches and the ANS aligns their phases at the PSs' outputs. This simplifies V_{SUM1} to $V_1\square(1+G_{21}R_{12})$. Consequently, to realize a notch at the blocker angle, $|G_{21}R_{12}|$ must be unity, and the summation of G_{21} and R_{12} phases must be 180°. This is a general result, which can be implemented with various circuitries. Figure 4.4.1 bottom-right shows three possible candidates, the OTA-based gyrator, the lumped λ/4 transmission line (T-line), and the lattice all-pass filter (APF). At mm-wave frequencies, the APF is favorable as it is not power-hungry like the gyrator and can satisfy the above criterion in larger bandwidth (BW) compared with the λ/4 T-line (See Fig. 4.4.1).

To enable or disable the SNF, a switch is added between node X and ground. In the disabled mode, the switch is turned on to shunt the BVCCs' output currents to ground. As a result, the PSs' output voltages are no longer affected by the other elements, thus making RX gain constant over incident angles. Moreover, the APF also acts as an impedance inverter and realizes a relatively high impedance at the BVCC's inputs (PS's outputs). Hence, the PS's gain and RX NF are not compromised in this mode.

Without any prior knowledge about the spatial blocker, the ANS tunes the PSs to align the phases of the strongest blocker at the PSs' outputs. Consequently, a phase-detection loop can be employed to minimize the phase difference ($\Delta\varphi$) between the PSs' outputs. However, the phase-detection gain of mm-wave phase detectors (PDs) is proportional to the amplitudes of their input signals. Therefore, the loop gain and accuracy of the phase alignment are substantially degraded when the blocker amplitude drops. Besides, the locking point considerably shifts when the signal-to-interference ratio (SINR) at its input ascends towards 0dB (see Fig. 4.4.2). In the proposed SNF, as $\Delta\varphi$ reduces during the phase alignment process, the blocker amplitude at the PS's output reduces and the SINR rises drastically, both of which eventually translate to large steady-state $\Delta\varphi$ adjustment errors, thus limiting the notch depth and direction accuracy. Hence, this method alone cannot automatically and robustly adjust the notch direction. Fortunately, as $\Delta\varphi$ reduces, the presence of the spatial blocker and desired signal respectively become stronger and weaker at node X. Hence, the phase shifters and notch direction can also be tuned based on maximizing the detected voltage amplitude at this node. However, the voltage-detection loop could end at the undesired local peaks if the initial $\Delta\varphi$ is >90° (see Fig. 4.4.2). Therefore, we utilize the two methods to implement a two-step ANS. In the first step, the phase-detection loop coarsely adjusts the notch direction and brings $\Delta\varphi$ to the useful range of the voltage-detection loop ($\Delta\varphi$<90°). Next, the voltage-detection fine-tuning loop takes over to reduce $\Delta\varphi$ to 0°.

Figure 4.4.3 shows the schematic of the proposed mm-wave four-element RX. For power efficiency, the gm-boosting and current-reusing techniques are applied to the LNA and active mixer, respectively. The vector-modulated PS follows the LNA and employs a high-order hybrid coupler for quadrature generation. An IF beamformer (IFBF) is implemented to either remove the blocker residue of the mm-wave SNF or make a second notch to suppress another spatial blocker. For ANS realization, the PD is made with a mixer-based multiplier and an LPF, and the voltage detector (VD) uses the Dickson rectifier to detect the downconverted signal from node X. As a prototype, off-chip ADCs and MCU are used to sample the PD/VD outputs, and conduct the loop control, respectively.

Fabricated in a 40nm CMOS process, the RX occupies an area of 2.8mm^2 (Fig. 4.4.7), while consuming 51mA per element from a 1.1V supply. Figure 4.4.4 shows continuous-wave measurement results. The single RX element achieves 23 to 29GHz BW, 30dB peak gain, 4.8-to-7.1dB NF and <-10dB S11. When the SNF is enabled, it exhibits a maximum of 40dB spatial rejection, and guarantees >20dB rejection over both full field-of-view and operation BW for all the four elements. The notch-depth variations over different channels are due to the gain and phase mismatch between the front-end components (LNA, PS) of RX elements. When the SNF is disabled, only <3.2dB gain reduction at the notch direction is observed. In another scenario shown in Fig. 4.4.4 bottom-middle, the SNF first forms a 24dB notch at -26° (blue curve) and then the IFBF is enabled in two modes. In the blocker residue removal mode, the IFBF increases the rejection at -26° by 14dB (red), while in the other mode, it creates another 35dB notch at 9° (green). With no spatial filtering, the measured in-band IP1dB is -34dBm and improves by 9dB, 17.5dB, and 20dB when only IFBF, only mm-wave SNF, and both notch filters are enabled, respectively.

Figure 4.4.5 top shows the ANS adjustment procedure and its related signals. In the first step, the notch direction is adjusted by minimizing the PD output. However, due to the PD's gain drop and -10dB input SINR, a residue phase difference ($\Delta\varphi$) of -53° is observed when the PD's output approaches 0. In the second step, the ANS tries to maximize the VD's output voltage and eventually $\Delta\varphi$ reaches 0. The entire procedure takes only 14 steps, and can be quite fast if the control loop is implemented on-chip. Due to the ANS robustness, the mm-wave SNF maintains its rejection as the input SINR rises from -30 to -3dB. Figure 4.4.5 also shows RX performance when tested with a desired -49dBm 100MS/s 64-QAM signal at 0° along with co-channel independently modulated blockers. In the first test, the mm-wave SNF rejects the blocker by 37dB to achieve EVM=-27.9dB at the RX output when facing a -34dBm blocker at -26° incident angle. In the second test, two in-band blockers (-35dBm at -23.5° and -41dBm at 27°) are applied to the RX. The mm-wave SNF suppresses the stronger blocker before the mixers while the other one is rejected by the IFBF at baseband, thus resulting in EVM=-25.5dB. The output SINR can be further improved by digital beamforming since the RX is not saturated by in-band blockers and the four-channel signals are preserved. Compared with the relevant prior art mm-wave/RF RXs in Fig. 4.4.6, this work is the only one offering N-input-N-output SNF at mm-wave frequencies, and also demonstrates competitive performance, especially in in-notch IP1dB, spatial notch width, NF, area, and power consumption.

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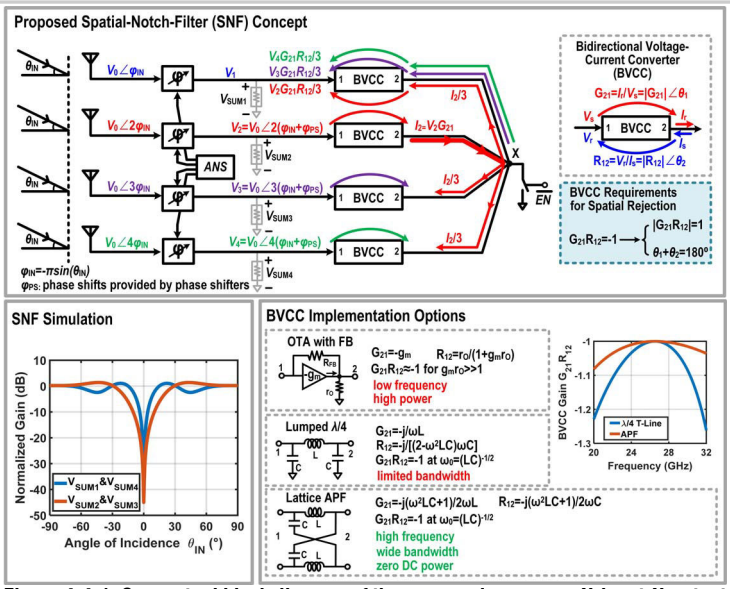

Figure 4.4.1: Conceptual block diagram of the proposed mm-wave N-input-N-output spatial-notch filter (SNF).

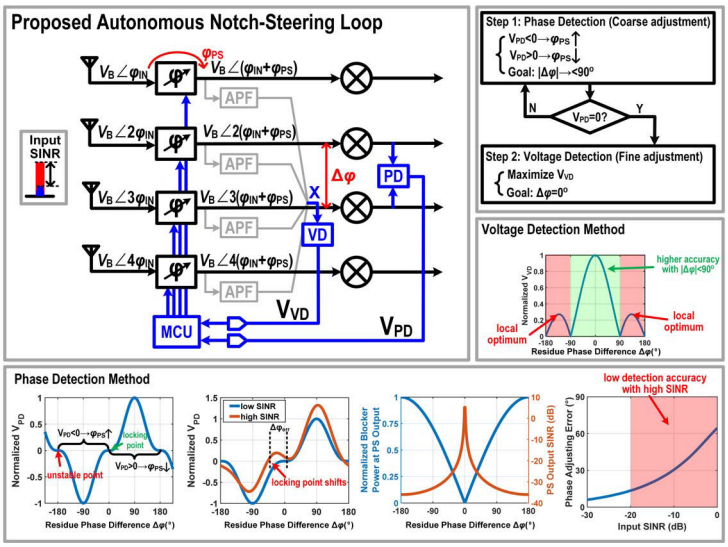

Figure 4.4.2: The proposed automatic self-steering block exploiting both phase-detection and voltage-detection methods.

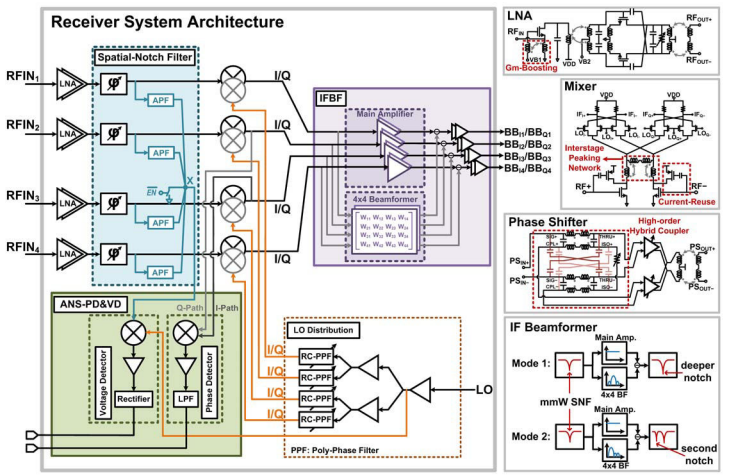

Figure 4.4.3: System architecture and circuit implementation of the proposed mm-wave four-element receiver.

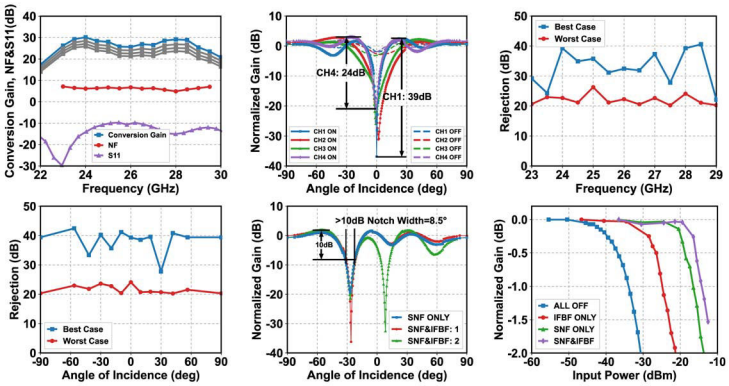

Figure 4.4.4: Single-element RX gain, NF and S11; in-band normalized gain versus angle of incidence for different RX elements; best/worst-case notch rejection versus frequency and angle of incidence; IF beamformer effects on RX gain, and IP1dB for in-notch incidence.

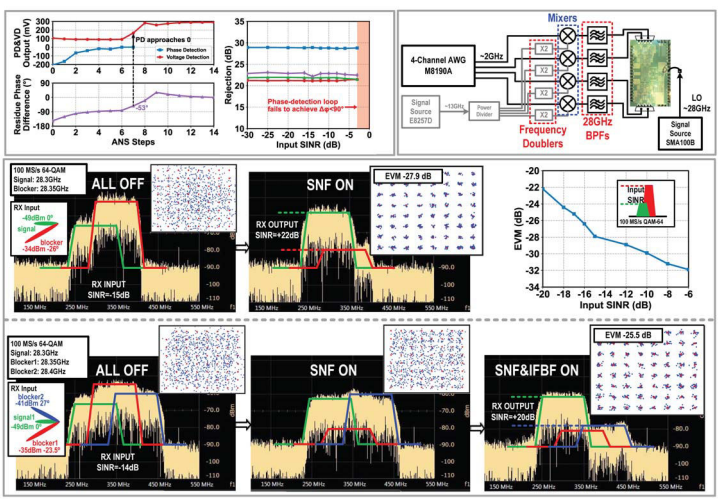

Figure 4.4.5: Measured phase/voltage-detector output voltages and corresponding phase alignment error during ANS adjustment procedure; Measurement setup, and measured RX EVM performance when facing different in-band spatial blockers.

	mm-Wave Spatial Notch RXs				Sub-6GHz Spatial Notch RXs	
	This Work	M. Huang ISSCC19 [3]	M. Huang ISSCC18 [4]	R. Garg ISSCC20 [5]	L. Zhang JSSC16 [1]	L. Zhang JSSC17 [2]
Functionality	MIMO mm-Wave SNF	MIMO Array-based ASF	MIMO SSA	MIMO SNF	MIMO SNF	MIMO SNF
Technology	40nm CMOS	45nm CMOS SOI	130nm SiGe BiCMOS	65nm CMOS	65nm CMOS	65nm CMOS
Frequency (GHz)	23~29	27~41	22~30	28	0.1~1.7	0.1~3.1
NFmin (dB)	4.8	4.3	4.2	6	1.7	2.1
Conversion Gain (dB)	30	36	33	>16	41	43
No. of Inputs/Outputs	4/4	4/4	8/2	4/4	4/4	4/4
N-Input-N-Output SNF	Yes	Yes	No	Yes	Yes	Yes
Spatial Order of Notch	4 (Scalable)	4 (Scalable)	2 (Fixed)	4 (Scalable)	4 (Scalable)	4 (Scalable)
Maximum mm-Wave/RF Notch Depth (dB)	40	0	40[a]	0	8	N/A
Maximum IF Notch Depth (dB)	35	62/50/51	37[a]	37	24	56
Minimum >10dB Cancellation Spatial Notch Width (°)	8.5~14 (CH1&4) 22~24 (CH2&3)	27~32	48~58	~11 (CH1&4)[a] ~22 (CH2&3)[a]	~27[a]	~30[a]
In-Notch P1dB (dBm)	-14	-19	N/A	N/A	N/A	-25
Autonomous Notch Steering	Yes	Yes	Yes	No	No	No
Notch Depth Degradation after Self-steering as the Input SINR Rises from -30dB to -3dB	~0	~7[a]	18[f]	N/A	N/A	N/A
Block/Signal Incidence Angle Difference in Modulation Measurement (°)	26	30	30	N/A	N/A	26
Blocker/Signal Frequency Offset/Modulation BW	50%	50%	50%	N/A	N/A	>400%[c]
Desired Signal EVM after Blocker Suppression (dB)	Input SINR -15dB 100MS/s 64QAM: -27.9	Input SINR -8dB 200MS/s 64QAM: -29.3[a] 500MS/s 64QAM: -27.7[a]	Input SINR -10dB 100MS/s 64QAM: -26.2[a] 500MS/s 64QAM: -25.2[a]	Input SINR 0dB 100MS/s 16QAM: -20.25[b]	N/A	Input SINR -11dB 1MS/s QPSK: -13.8[b]
Power Consumption /RX Element (mW)	56.1(44.1[d])	70~85	70	112.4 (28.1/beam)	35~40	29~36.8
Chip Area (mm²)	2.8 (2.08[e])	23.4	21.6	10.6	1.2	2.25

[a] Estimated from figures. [b] Over-the-air (OTA) measurement results. [c] CW blockers
[d] Power consumption excluding LO buffers, estimated from simulation. [e] Core area.
[f] From follow-up TMTT paper

Figure 4.4.6: Performance summary and comparison table with relevant prior art mm-wave/RF RXs.

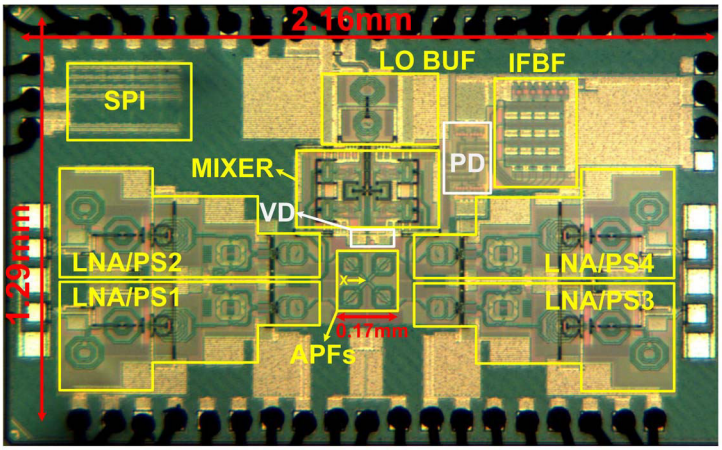

Figure 4.4.7: Die micrograph.

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