A Wideband Low-Power Cryogenic CMOS Circulator for Quantum Applications

Ruffino, Andrea; Peng, Yatao; Sebastiano, Fabio; Babaie, Masoud; Charbon, Edoardo

DOI
10.1109/JSSC.2020.2978020

Publication date
2020

Document Version
Final published version

Published in
IEEE Journal of Solid-State Circuits

A Wideband Low-Power Cryogenic CMOS Circulator for Quantum Applications

Andrea Ruffino, *Student Member, IEEE*, Yatao Peng, *Member, IEEE*, Fabio Sebastiano, *Senior Member, IEEE*, Masoud Babaie, *Member, IEEE*, and Edoardo Charbon, *Fellow, IEEE*

***Abstract*— Quantum computers require classical electronics to ensure fault-tolerant operation. To address compactness and scalability, it was proposed to implement such electronics as integrated circuits operating at cryogenic temperatures close to those at which quantum bits (qubits) operate. Circulators are among the most common blocks used in the qubit readout chain, but they are currently discrete devices with a bulky footprint, thus preventing large-scale system integration. For this reason, we present here a detailed description of the first fully integrated CMOS circulator operating from 300 K down to 4.2 K to be an integral part of cryogenic quantum computing platforms. At 300 K, the circuit's operating frequency is centered around 6.5 GHz with 28% fractional bandwidth, and it has 2.2-dB insertion loss, 2.4-dB noise figure, and 18-dB isolation while consuming 2.5-mW core power. These results are achieved thanks to a fully passive architecture based on *LC* all-pass filters, which allows achieving a 1.6× increase in fractional bandwidth and the lowest power consumption with respect to the state of the art while using only 0.45 mm^2 of core area. This allows miniaturization of circulators in power-constrained multi-qubit readout systems.**

***Index Terms*— Circulator, Cryo-CMOS, quantum computer, qubit, qubit processor, qubit readout, RFIC.**

I. Introduction

QUANTUM computers are an emerging solution to address the ever-growing need for computational power and, in particular, to solve today's intractable problems, such as the simulation of complex molecules, the design of new materials with specific properties, and the prime factorization of large numbers [1], [2]. A quantum computer operates by processing the information stored in quantum bits (qubits), whose base state can be represented by $|0\rangle$ and $|1\rangle$.

The most promising implementation to build large-scale quantum computers is solid-state quantum bits, such as spin qubits [3] and superconducting qubits [4]. These qubits are typically required to operate at deep-cryogenic temperatures to work in the quantum regime. Hence, they are kept in dilution fridges, while the electronic setup required for their readout and control is implemented by commercial instruments at room temperature. Such an approach is feasible only when a few (<100) qubits are used. However, existing qubits have coherence times and gate fidelities that do not allow them to be used directly as computational elements. Consequently, quantum error correction (QEC) [5] needs to be applied by encoding multiple physical qubits into a single logical qubit. Hence, a practical quantum computer will need to handle thousands if not millions of qubits, thus the need for compact and scalable classical control circuits in physical proximity to the qubits. For this reason, CMOS circuits operating directly at cryogenic temperatures (cryo-CMOS) have been proposed [6], [7] to read out and control large numbers of qubits, thus paving the way to future co-integration of qubits and classical control.

Superconducting qubits are typically addressed by dispersively coupling the qubit to a resonator and by reading the state-dependent frequency shift [8] of the feedline transmission curve under weak RF signal. Spin qubits [9] are commonly read out by radio frequency reflectometry [10] or direct gate reflectometry [11]: in this case, the weak readout signal is coupled to a resonator, matched to 50 Ω, and the resistance of the readout electrometer (for RF reflectometry) or the qubit gate capacitance (for dispersive gate sensing) vary depending on the qubit state. The power or the phase of the signal reflected by the qubit, thus, carries the information on the qubit state and can be read out.

Typical readout systems for spin qubits and superconducting qubits show close similarities with RF wireless receivers, as shown in Fig. 1. Qubits are coupled to a resonator, tuned at the readout frequency, and the signal goes through one or multiple cryogenic amplification stages; then, it is down-converted by a mixer, typically in a homodyne or low-IF scheme, and then, it is filtered and digitized to be processed at room temperature. Current systems employ several discrete components, such as directional couplers, circulators, and amplifiers operating at cryogenic temperatures, together with commercial instruments, such as vector signal analyzers, operating at 300 K. The ultimate goal would be to move all readout and control circuitry to cryogenic temperatures while maintaining a compact form factor and leaving only the user interface at 300 K.

Manuscript received August 16, 2019; revised November 21, 2019 and January 30, 2020; accepted February 13, 2020. Date of publication March 17, 2020; date of current version April 23, 2020. This article was approved by Associate Editor Hongtao Xu. This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 688539. *(Corresponding author: Andrea Ruffino.)*

Andrea Ruffino, Yatao Peng, and Edoardo Charbon are with the School of Engineering, École Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland (e-mail: andrea.ruffino@epfl.ch).

Fabio Sebastiano and Masoud Babaie are with the Quantum and Computer Engineering Department, Delft University of Technology (TU Delft), 2628 Delft, The Netherlands.

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2020.2978020

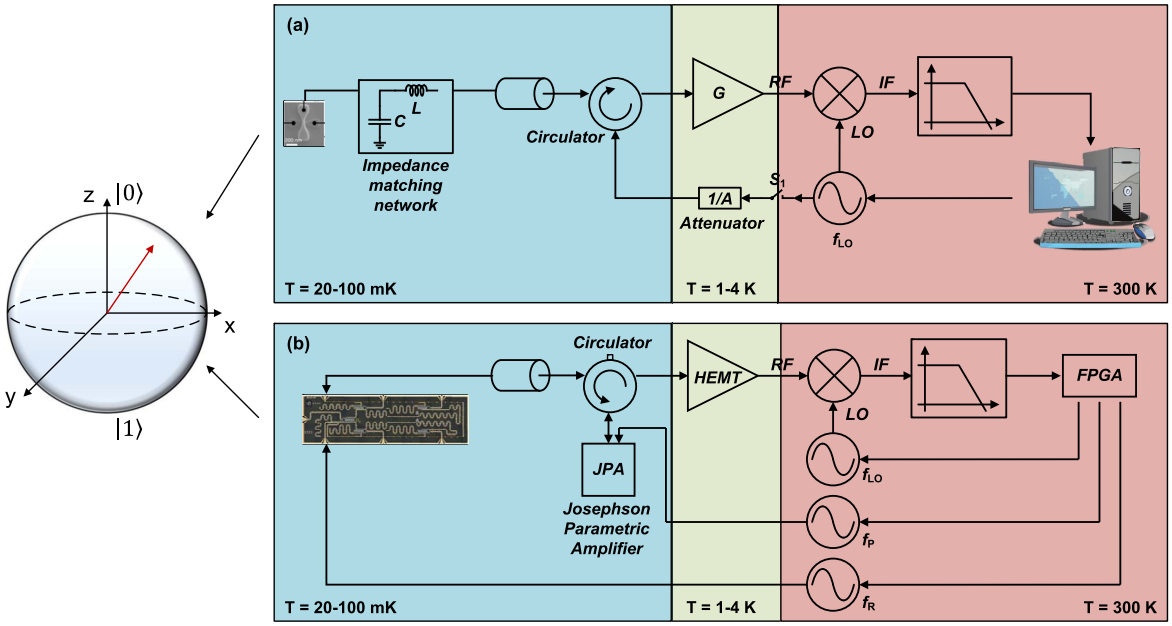

Fig. 1. Current implementations of typical qubit readout schemes using ferrite circulators for (a) spin qubit processors [11] and (b) superconducting qubit processors [8]. The color coding represents temperature variation along the chain, from base temperature (20–100 mK) in blue to room temperature (300 K) in red. The ultimate goal is to move all control and readout electronics at cryogenic temperatures.

Among the mentioned components, cryogenic circulators are very widely used in qubit readout systems [8], [12]. However, they are currently realized by bulky discrete ferrite devices [13]. Hall effect circulators have been demonstrated [14], [15], but they still employ magnetic fields. Hence, a non-magnetic cryogenic integrated circuit (IC) implementation would be a significant step toward overall system scalability.

Integrated non-magnetic circulators operating at room temperature have recently been proposed [16]–[20] in CMOS technology. Such circulators exploit linear periodic time-variant (LPTV) circuit operation to create non-reciprocity. Such technique resulted in a variety of implementations targeting shared-antenna interfaces for different communication standards, at frequencies below 1 GHz [16], [17], [19], at 25 GHz [18], and at 60 GHz [20].

The circuit implementations and design requirements of these approaches, however, cannot be directly applied to the needs of circulators for qubit readout since the frequency of interest is in the 5–8-GHz range, where most superconducting qubit frequencies lie [8]. This band could be potentially interesting for spin qubits if their readout frequency is increased so that currently employed directional couplers [10] could be replaced by RF circulators. However, the techniques proposed so far for CMOS circulators are not well suited to such a band. Moreover, full-duplex circulators have shown a trend for high power handling [19] due to transmitter requirements, while circulators for quantum computing are inherently small-signal circulators only.

Active CMOS circulators have been explored in the frequency of interest [21], [22]; however, their noise performance has been shown to be insufficient.

Circulators for qubit readout are currently implemented by ferrite circulators [13], whose performance, indicated in Table I, sets the ideal design requirements. However, to address miniaturization with an IC realization, some design compromises need to be made. Circulators for qubits require a cryogenic operation, as they are commonly placed at temperatures between 0.02–4 K inside dilution fridges. This imposes very stringent requirements on power consumption, so as to meet the limited cooling power budgets of the cryostats. At the base temperature, the maximum cooling power is in the order of 10 μW, which is currently out of reach for integrated circulator solutions. If the circulator is operated at higher temperatures (1–4 K), the power budget can be set to 2 mW [7], especially if the circulator is shared among multiple qubits. Cryogenic circulators must also have a small area since they will ultimately need to be integrated into a compact, scalable IC controller. We, therefore, set a maximum design target of few mm by few mm. The operational frequency of the circulator should be in the 6.5-GHz band [8]. Moreover, scalability calls for multiplexing techniques since large area and power savings can be obtained by sharing the same

TABLE I
DESIGN SPECIFICATIONS OF CRYOGENIC CIRCULATORS FOR QUANTUM COMPUTING

	Specifications	Ferrite circulators [13]
Working temperature	0.02-4 K	0.02-300 K
Center frequency	6.5 GHz	6 GHz*
Bandwidth	2 GHz	4 GHz*
Insertion loss	< 1 dB	0.4 dB*
Isolation	18 dB	18 dB*
Noise temperature	< 1 K	7 K*
Area	$< 5 \times 5$ mm^2	35×45 mm^2
Power consumption	< 2 mW	0

*Reported data are at 77 K.

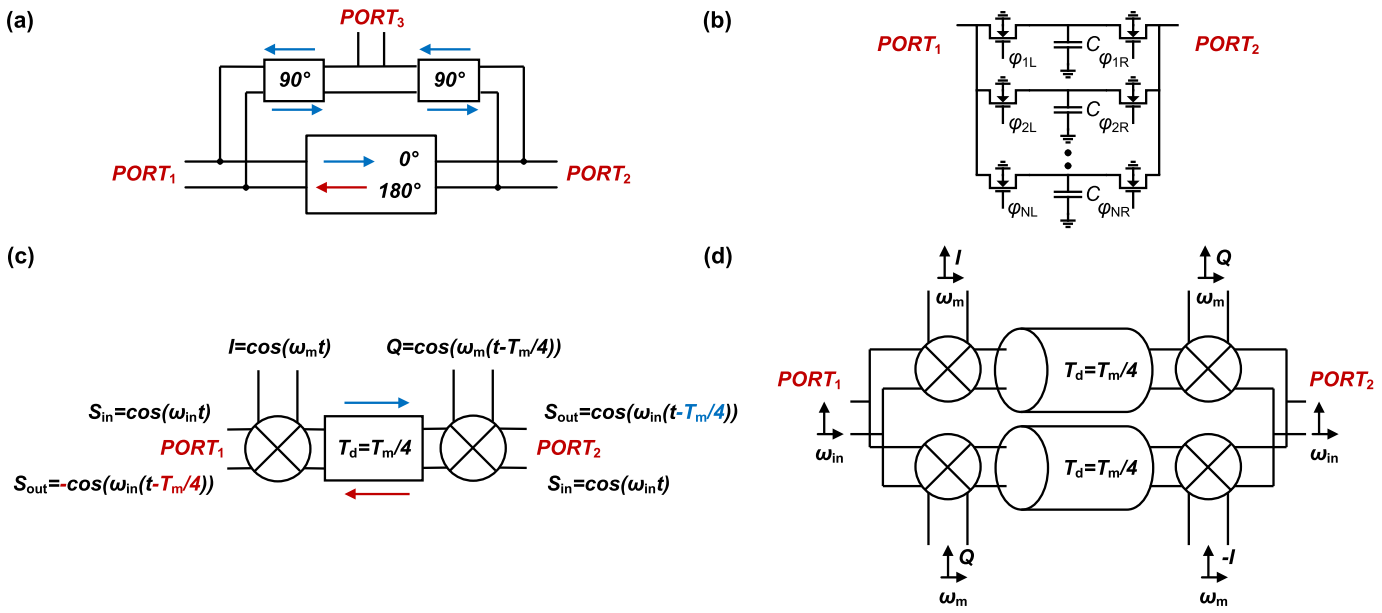

Fig. 2. Block diagram of (a) staggered-commutation circulators, showing (b) N-path filter implementation of the non-reciprocal branch, (c) single-branch, and (d) I/Q double-branch implementations of the broadband gyrator.

electronics for multiple qubit channels, so frequency-encoded readout, such as frequency multiplexing, is advisable, thus requiring bandwidth maximization. If a 10-MHz bandwidth is set for each qubit, with a 10-MHz spacing, then one could multiplex 100 qubits in a 2-GHz circulator bandwidth, in line with the size of currently available quantum processors. Finally, meeting the performance of passive discrete circulators in terms of insertion loss (and noise) is quite challenging in an IC, so the target insertion loss should be smaller than 1 dB, and the isolation should be at least 18 dB. The insertion loss specification converts to a noise equivalent temperature of less than 1 K. If scalability is the main requirement, then area, power consumption, and bandwidth become high priority design targets. The presented design specifications are summarized in Table I.

To address these requirements, this article presents a detailed discussion of the first integrated cryo-CMOS circulator [23], based on a proposed architecture exploiting all-pass filters, targeting low power and wideband operation for quantum computing applications. This work represents a proof-of-concept of cryogenic integrated CMOS circulators, it explores the implications of an integrated solution, and, as such, it is only a first step toward the full replacement of current setups. In the following, we explain the theory, the design, the implementation, and the characterization of the proposed cryo-CMOS circulator.

This article is organized as follows. Section II briefly reviews integrated CMOS circulators and then develops the theory of the proposed all-pass filter implementation, highlighting the advantages for low power, large bandwidth, and small area. Section III describes the implementation of the proposed cryo-CMOS circulator. Section IV describes the operation and modeling of the circulator at cryogenic temperature. Section V details the measurements of the circulator at 300 K and 4.2 K. Section VI comments about other possible applications of this work. Section VII concludes this article.

II. Wideband Low-Power Staggered Commutation Circulators

Integrated CMOS circulators have been recently proposed by exploiting time-varying circuits to break the Lorentz reciprocity, thus realizing staggered commutation [24]. From a top-level perspective, as shown in Fig. 2(a), they have been realized with a loop, composed of two reciprocal branches, providing 90° phase shift in either direction, and a non-reciprocal branch, causing a 0°/180° phase shift, depending on the signal direction. In this way, constructive interference (360°) is achieved in one direction of circulation, and destructive interference (180°) is obtained in the opposite direction.

Two families of circuits have been built on such generic block diagram, depending on the actual implementation of the different branches: the N-path filter approach [16], [17] and the broadband gyrator approach [18]–[20]. The LPTV section has been implemented either by an N-path filter for GSM band below 1 GHz [16], [17] or by a gyrator including a switched transmission line for *K*-band at 25 GHz [18], or a switched band-pass filter at 60 GHz [20].

A. N-Path Filter Circulators

In the N-path filter approach, the reciprocal branches are realized as *CLC* low-pass filter T-sections, while the non-reciprocal branch incorporates a switched capacitor filter, namely, a two-port N-path filter, as shown in Fig. 2(b), where the two sets of switches are controlled by low duty cycle non-overlapping phase-shifted clocks. Such a phase shift can introduce non-reciprocity in the filter phase response [17],

which is inherited by the branch. When the phase shift is set to 90°, this creates a 90°/−90° non-reciprocity. When a reciprocal 90° branch is added, the required non-reciprocal 0°/180° branch is formed.

Such an approach has some disadvantages: the clock frequency needs to be the same as the input frequency, so high-frequency circulators would require high-frequency clocks, causing large power consumption; moreover, the bandwidth of the circulator's non-reciprocal response is limited to the sharp band-pass response of N-path filters.

B. Broadband Gyrator Circulators

The broadband gyrator approach implements the non-reciprocal branch by employing a passive filter between two sets of I/Q mixers. A differential implementation of such a structure is shown in Fig. 2(c). When there is an incoming signal at frequency ω_{in}, the mixers commute at clock frequency ω_m, with $\omega_m < \omega_{in}$. The internal filter is producing a phase shift, or equivalently, a time-delay T_d, which is equal to $T_m/4$, where $T_m = 2\pi/\omega_m$ is the clock period. In the forward direction, this gives a transmission with a delay of $T_m/4$, while in the reverse direction, the system yields a delay of $T_m/4$ and a sign flip. The periodical time variance caused by mixers results in non-reciprocal behavior.

Under such assumptions, the S-parameters of the two-port gyrator can be represented by [18]

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0 & -e^{-j\frac{\pi}{2}\left(\frac{\omega_{in}}{\omega_m}\right)} \\ +e^{-j\frac{\pi}{2}\left(\frac{\omega_{in}}{\omega_m}\right)} & 0 \end{bmatrix}. \quad (1)$$

This gives lossless non-reciprocal transmission at odd multiples of the clock frequency $\omega_{in} = (2n-1)\,\omega_m$ [18]. Such property is ideally obtained over substantial bandwidth, limited only by the internal filter bandwidth.

This structure suffers, however, from S-parameter degradation in the presence of duty cycle mismatch. To mitigate this problem, the architecture can be modified to include a parallel quadrature path similar to the path presented above, where clock signals are shifted by 90° [18]. Such a double-branch implementation, shown in Fig. 2(d), can achieve 90° or −90° phase shift according to the signal direction at odd multiples of the clock frequency. Thus, when it is embedded into an additional reciprocal 45° section on each side, it can perform the required 0°/180° gyrator function.

In the recent implementations [18], [19], the internal filter has been realized as a multi-section lumped-element Bragg-limited $\lambda/4$ transmission line at the clock frequency to achieve the required $T_m/4$ time delay. The clock frequency was chosen to be $\omega_m = \omega_{in}/3$. Also the other filters in the reciprocal branches have been implemented with artificial transmission lines to realize a circulator at 25 GHz. Another circulator implementation at 60 GHz [20] has employed some extra inductors at the input and output of each I/Q mixer to tune out the capacitance of the mixer switches and mitigate the tradeoff between a small switch R_{ON} and additional unwanted parasitic capacitance C_p. However, such an approach still uses a multi-section transmission line to realize the required delay.

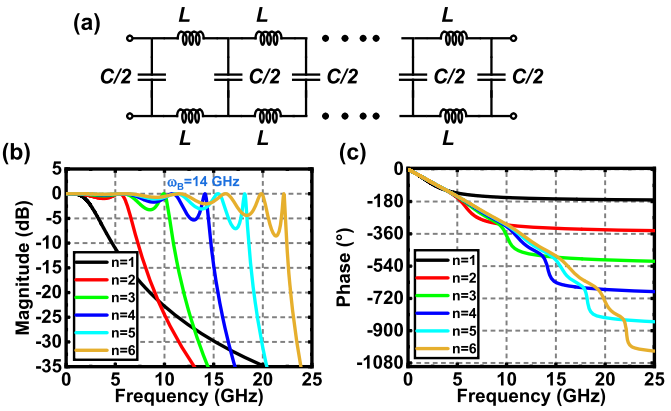

Fig. 3. Multi-section artificial transmission line (a) schematic, (b) transfer function magnitude, and (c) phase for different number of sections. The lines have been designed to all achieve the same time delay $T_d = T_m/4$ for $\omega_{in}/\omega_m = 3$ and input frequency $f_{in} = 6.5$ GHz.

C. All-Pass Filter Circulators

The presented solutions cannot be applied directly to the design of a low-power wideband circulator in the frequency of interest. The N-path filter approach would require low duty cycle non-overlapping phases at the 6.5-GHz operating frequency ω_{in}, which would require extremely power-hungry clock drivers. The switched transmission line approach, instead, would impose a $\lambda/4$ transmission line at the clock frequency. A reduction of clock frequency to minimize power would result in a too large and lossy transmission line implementation at the frequency of interest.

Indeed, to reduce the circulator's power consumption, the clock frequency ω_m needs to be reduced since the switching of mixer capacitance at the clock rate is the primary source of power dissipation. If ω_m is reduced, the equivalent time delay required by the filter becomes larger. In a transmission line, this would require a longer line, which could be realized only with more equivalent LC sections, causing more area and insertion loss or reduced bandwidth, if a smaller number of sections is used.

Indeed, in the artificial transmission line approach, as shown in a differential implementation in Fig. 3(a), each lumped element section provides a unit delay $t_d = \sqrt{L \cdot C}$. Thus, multiple sections are required to achieve the required delay $T_d = T_m/4$. However, the filter behaves like a transmission line only within its bandwidth, that is, until half of the Bragg frequency, $\omega_B = \frac{2}{\sqrt{L \cdot C}}$, as shown in Fig. 3(b). By setting such a limit, one can obtain

$$t_d = \sqrt{L \cdot C} = \frac{1}{\omega_{in}}. \quad (2)$$

This can, in turn, determine the number of sections required to achieve the desired time delay

$$n = \frac{T_d}{t_d} = \frac{\pi}{2} \cdot \left(\frac{\omega_{in}}{\omega_m}\right). \quad (3)$$

If one considers the values of inductors and capacitors required to implement the artificial unit section, namely, $L = (Z_0/\omega_{in})$ and $C = (1/(Z_0 \cdot \omega_{in}))$, one can also calculate the total

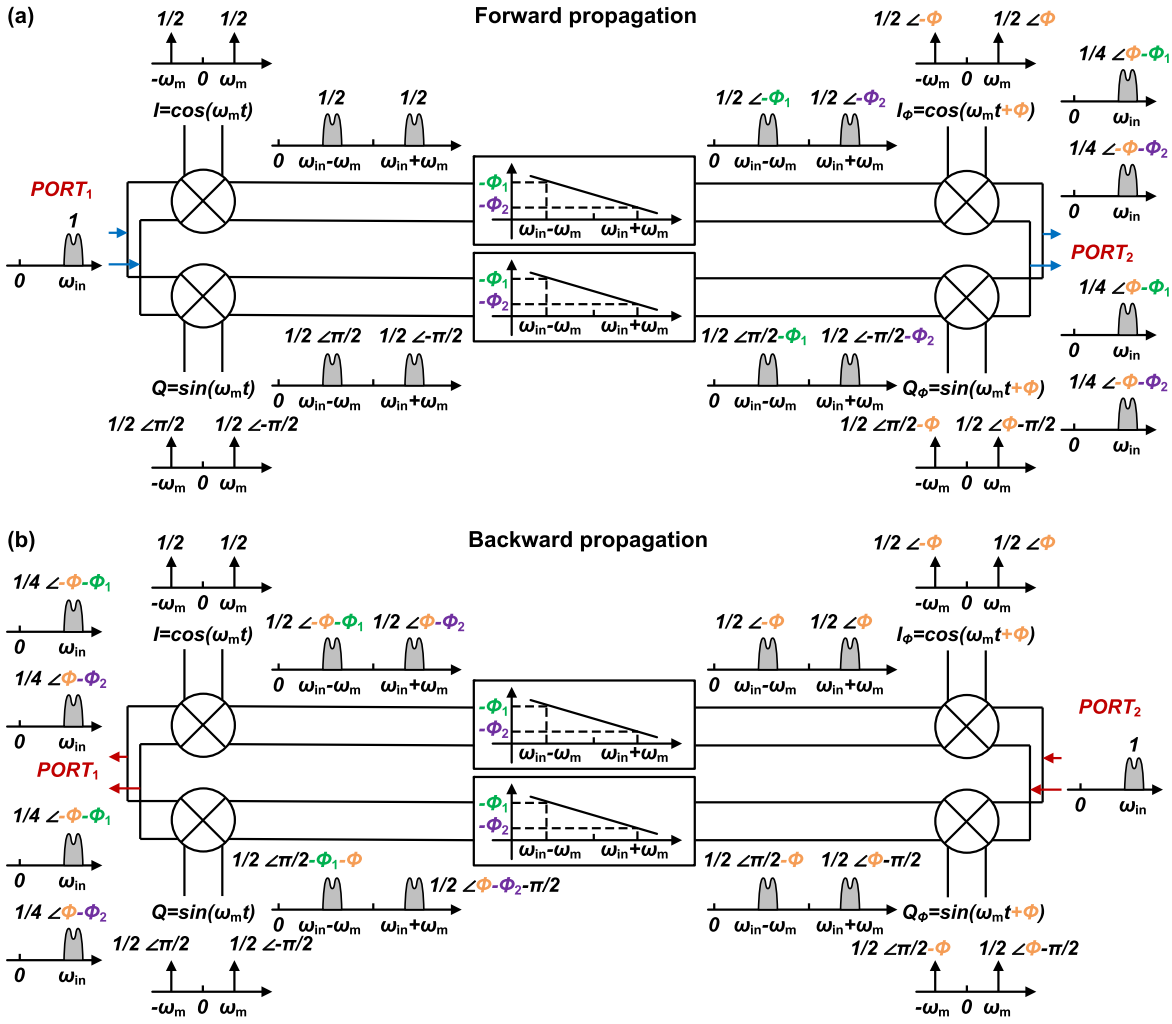

Fig. 4. Phase-frequency domain analysis of (a) forward propagation and (b) backward propagation in the non-reciprocal branch of the all-pass filter circulator.

inductance required as

$$L_t = n \cdot L = \frac{\pi}{2} \cdot \left(\frac{\omega_{\text{in}}}{\omega_{\text{m}}}\right) \cdot \frac{Z_0}{\omega_{\text{in}}}. \tag{4}$$

This demonstrates the undesirable tradeoff between the reduction of the dynamic power consumption and area/insertion loss.

Moreover, the phase relationship for an n-section line is given by the following relationship, as shown in Fig. 3(c):

$$\theta(\omega) = -n \cdot 2 \cdot \arcsin\left(\frac{\omega}{\omega_{\text{B}}}\right). \tag{5}$$

Consequently, the group delay can be calculated as

$$\tau(\omega) = -\frac{d\theta(\omega)}{d\omega} = \frac{2n/\omega_{\text{B}}}{\sqrt{1-\left(\frac{\omega}{\omega_{\text{B}}}\right)^2}}. \tag{6}$$

This analysis applies to both the transmission line implementation [18] and the case where the transmission line is embedded into tuned resonators [20] since the properties of the multi-section lumped-element artificial line still apply.

To mitigate these problems, an alternative architecture needs to be used.

To better capture the mechanisms of the non-reciprocal branch, one should analyze it in the frequency domain. To do so, we generalize the double-branch architecture to include mixer clocks shifted by a phase shift ϕ, as shown in Fig. 4. In this case, a signal traveling at frequency ω_{in} is mixed in the two parallel paths with I/Q clocks at frequency ω_{m}, generating two mixing products at $\omega_{\text{L}} = \omega_{\text{in}} - \omega_{\text{m}}$ and $\omega_{\text{H}} = \omega_{\text{in}} + \omega_{\text{m}}$ in each of the two branches, with different phase shifts due to the I/Q mixing. In each branch, difference and sum-frequency components undergo additional phase shifts $\phi_1 = (\omega_{\text{in}} - \omega_{\text{m}})\tau$ and $\phi_2 = (\omega_{\text{in}} + \omega_{\text{m}})\tau$, respectively, caused by the internal filter. Finally, the two frequency components in the I and Q paths remix again at frequency ω_{m} but, in this case, with ϕ-shifted I/Q polarity, thus generating mixing products at $\omega_{\text{in}} - 2\omega_{\text{m}}$, ω_{in}, and $\omega_{\text{in}} + 2\omega_{\text{m}}$. The two components at $\omega_{\text{in}} - 2\omega_{\text{m}}$ and $\omega_{\text{in}} + 2\omega_{\text{m}}$ are out of phase with each other, and therefore, they cancel out. The four components at ω_{in} can instead add up constructively if one imposes that they all have the same phase, meaning $\phi - \phi_1 = -\phi - \phi_2$ or $\phi_1 - \phi_2 = 2\phi$. In this case, lossless transmission with a phase shift $\phi - \phi_1$ can be obtained. In the reverse direction, the same analysis can show that the lossless transmission can be obtained with

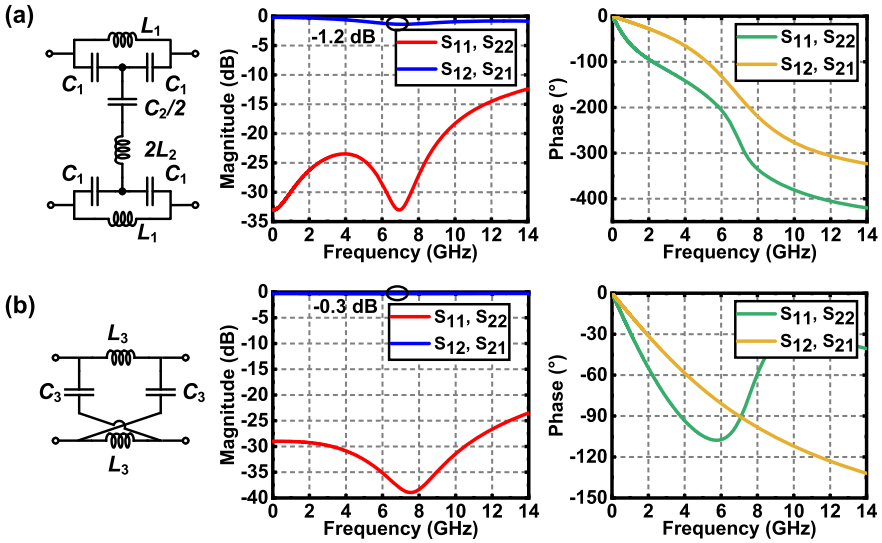

Fig. 5. Schematic and transfer function post-layout simulation at 300 K of (a) second-order bridged-T all-pass filter and (b) first-order lattice all-pass filter.

a different phase shift $-\phi - \phi_1$. Under such assumptions, the resulting S-parameters are

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0 & +e^{-j(-\phi-\phi_1)} \\ +e^{-j(\phi-\phi_1)} & 0 \end{bmatrix}. \tag{7}$$

Under the presented analysis, the phase-domain conditions for non-reciprocal operation can be expressed as

$$\begin{cases} \phi = -\pi/2 \\ \phi_1 - \phi_2 = 2\phi = -\pi \\ \phi_1 = \pi/2. \end{cases} \tag{8}$$

These equations are the fundamental design equations of the circulator.

Now, to address the requirements of circulator design for quantum computing applications (i.e., 5–8-GHz band, low power consumption, and small area), the parameters in these equations and, consequently, the circuit architecture need to be appropriately chosen.

To mitigate the adverse effect of duty cycle mismatch, the phase shift between clock signals has to be 90°, thus yielding a differential I/Q clock scheme; this is represented by the first design equation in (8).

To address a power target of 2 mW, we choose to operate with a clock frequency around 1 GHz; therefore, given our band of interest centered around 6.5 GHz, we decide to operate with a clock frequency $\omega_m = \omega_{in}/5$. The resulting modulation index $m = \omega_{in}/\omega_m$ is chosen to be 5.

The core functionality of the circulator is then described by the second equation in (8), which establishes that the phase shifts of the difference-frequency ω_L and the sum-frequency ω_H need to be 180° apart. If ω_m is reduced to minimize power consumption, then the two components ω_L and ω_H become closer to each other, requiring the internal filter in the non-reciprocal branch to be highly dispersive.

Under these assumptions, artificial transmission lines would require too many first-order sections to provide the required phase shifts at closely spaced frequencies ω_L and ω_H, falling into the usual tradeoff with loss.

For this reason, we propose to use a second-order filter, and we decide to use an all-pass filter, capable of providing phase shift ideally without affecting the amplitude. A filter that can satisfy such conditions at the required frequency is a bridged-T LC all-pass filter, of which a differential implementation is shown in Fig. 5(a).

The values of the different components for the single-ended case are [25]

$$L_1 = \frac{2Z_0}{\omega_0 Q} \tag{9}$$

$$L_2 = \frac{QZ_0}{2\omega_0} \tag{10}$$

$$C_1 = \frac{Q}{\omega_0 Z_0} \tag{11}$$

$$C_2 = \frac{2Q}{\omega_0\left(Q^2-1\right)Z_0}. \tag{12}$$

The transfer function of such filter can be expressed as

$$H(s) = \frac{s^2 - \left(\frac{\omega_0}{Q}\right)s + \omega_0^2}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2}. \tag{13}$$

Consequently, the magnitude of the filter transfer function is

$$|H(\omega)| = \frac{\sqrt{\left(\omega_0^2-\omega^2\right)^2 + \frac{\omega_0^2\omega^2}{Q^2}}}{\sqrt{\left(\omega_0^2-\omega^2\right)^2 + \frac{\omega_0^2\omega^2}{Q^2}}} = 1. \tag{14}$$

The phase response of this filter can instead be expressed as

$$\angle H(\omega) = -2\arctan\left(\frac{\omega\cdot\omega_0}{Q\cdot\left(\omega_0^2-\omega^2\right)}\right). \tag{15}$$

Consequently, the group delay of the second-order all-pass filter is calculated as

$$\tau(\omega) = -\frac{d\angle H(\omega)}{d\omega} = \frac{2Q\omega_0\left(\omega_0^2+\omega^2\right)}{Q^2\left(\omega_0^2-\omega^2\right)^2 + \omega_0^2\omega^2}. \tag{16}$$

The center frequency of the circulator ω_{in} can be placed at the center of the all-pass filter ω_0, where the phase shift is 180°, while the two components ω_L and ω_H can be placed where the phase shift of the filter is 90° and 270°, respectively. Such a second-order filter allows to satisfy the fundamental non-reciprocity condition at frequencies closer to the center frequency, due to the steep phase response, as required by the choice $\omega_m = \omega_{in}/5$.

The two phase shifts at the difference and sum frequency can be expressed as

$$\phi_1|_{\omega=\omega_L=\omega_0-\omega_m} = -2\arctan\left(\frac{1}{Q}\frac{\omega_0}{\omega_m}\frac{\omega_0-\omega_m}{2\omega_0-\omega_m}\right) \quad (17)$$

$$\phi_2|_{\omega=\omega_H=\omega_0+\omega_m} = +2\arctan\left(\frac{1}{Q}\frac{\omega_0}{\omega_m}\frac{\omega_0+\omega_m}{2\omega_0+\omega_m}\right). \quad (18)$$

Now, using the assumption that $\omega_0 \gg \omega_m$, one can express the difference between the two phase shifts as follows:

$$\phi_2 - \phi_1 = 4\arctan\left(\frac{1}{Q}\cdot\frac{\omega_0}{2\omega_m}\right). \quad (19)$$

By imposing $\phi_2 - \phi_1 = \pi$, one can express the required Q as

$$Q = \frac{1}{2}\left(\frac{\omega_0}{\omega_m}\right). \quad (20)$$

One can then calculate the total inductance required for the all-pass filter implementation as follows:

$$L_t = L_1 + L_2 = \frac{Z_0}{\omega_{in}}\cdot\left(\frac{2}{Q}+\frac{Q}{2}\right). \quad (21)$$

If one uses the expression found for Q in (20), one can write

$$L_t = \frac{Z_0}{\omega_{in}}\cdot\left(4\frac{\omega_m}{\omega_{in}}+\frac{1}{4}\frac{\omega_{in}}{\omega_m}\right). \quad (22)$$

This expression is valid for a single I or Q branch. The transmission line architecture can operate with a single path (I or Q), as shown in [19] and [20], since all the mixing harmonics created by the square wave clock are passed within its bandwidth. In principle, also, an all-pass filter can operate with a single path; however, this increases the sensitivity of insertion loss to duty cycle mismatch [18] in the I/Q clock generation. This can be mitigated by adding tunability to the phase of the I/Q clock but at the cost of increased power consumption.

If (22) is compared to the equation obtained in the case of the transmission line implementation (4), the total inductance values for $\frac{\omega_{in}}{\omega_m} = 5$ are, respectively, $7.85\frac{Z_0}{\omega_{in}}$ and $2.05\frac{Z_0}{\omega_{in}}$ for a single-branch implementation in both cases, while such values are doubled for an I/Q double-path realization. This shows that the inductance required by the all-pass filter approach is always smaller, even comparing a single path transmission line approach with the presented double-branch I/Q all-pass filter.

Although this approach is conceived to reduce clock frequency, addressing power reduction, which is the first requirement set for cryogenic circulators, at the same time, it benefits compactness, which is the second requirement, since a smaller number of smaller passives (in particular inductors) is used with respect to a multi-section transmission-line approach

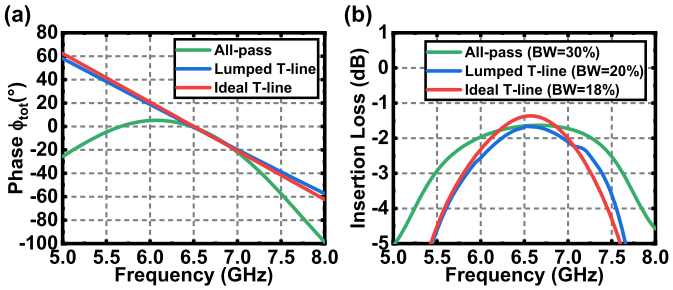

Fig. 6. (a) Comparison between the all-pass filter, the artificial transmission line, and the ideal transmission line approach, for $\omega_{in}/\omega_m = 5$, in terms of overall constructive/destructive circulator phase relationship. (b) Simulated insertion loss and 1-dB bandwidth of an entire circulator constructed using each of the elements in the comparison and ideal mixers with $R_{ON} = 10\ \Omega$.

(with or without band-pass filter). This favors insertion loss and noise figure as well since fewer inductors are in series with the signal path.

Finally, due to the phase choices in the second-order all-pass filter, one can choose the non-reciprocal branch insertion phase to be 90°, as described by the third design equation in (8). This allows eliminating the need for additional 45° sections as used in [18]. This again reduces the number of passive components, improving compactness and insertion loss of the circulator.

To close the circulator loop, we propose to implement the reciprocal branches with LC all-pass filters as well, but in this case, first-order lattice filters are enough for the required 90° phase shift. The schematic of the filter is shown in Fig. 5(b), and the values of the components are

$$L_3 = \frac{Z_0}{\omega_0} \quad (23)$$

$$C_3 = \frac{1}{\omega_0 Z_0}. \quad (24)$$

The resulting transfer function can be expressed as

$$H(s) = \frac{\omega_0 - s}{\omega_0 + s}. \quad (25)$$

The magnitude of the transfer function can be demonstrated to be constantly equal to 1 also in this case:

$$|H(\omega)| = \frac{\sqrt{\omega_0^2+\omega^2}}{\sqrt{\omega_0^2+\omega^2}} = 1. \quad (26)$$

The phase can instead be expressed as

$$\angle H(\omega) = -2\arctan\left(\frac{\omega}{\omega_0}\right). \quad (27)$$

Now that the architecture of the proposed circulator is complete, the last property, the bandwidth, can be discussed. Such property arises from the interaction, in the phase domain, between the phase relationships of the non-reciprocal branch and the two reciprocal branches.

The use of the all-pass filter approach shows to have benefits on bandwidth as well. The second-order all-pass filter can provide a phase shift in all frequency regions, apart from the two plateaux, where it flattens out to 0° and 360°. The phase response of such a filter is highly linear around its center

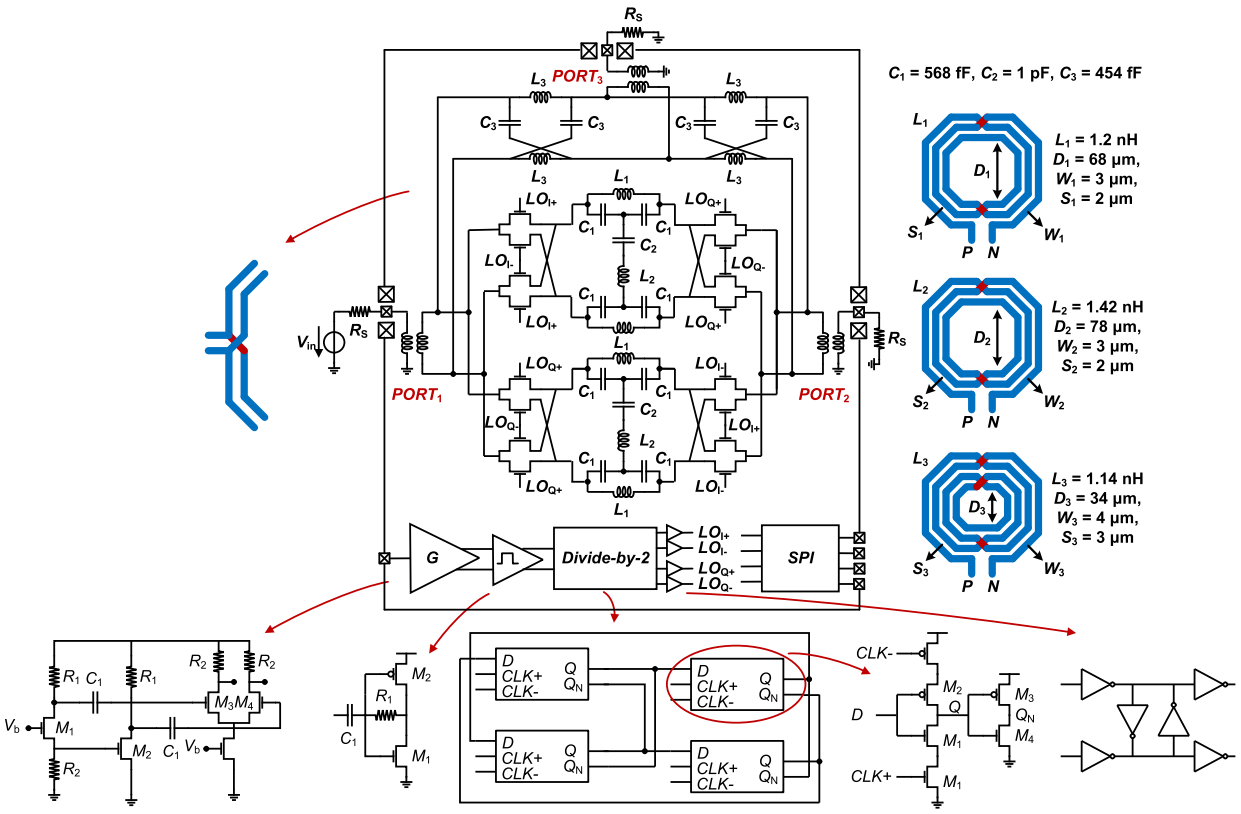

Fig. 7. Circuit schematic of the designed circulator, including the circulator core and details of the auxiliary structures.

frequency, which means that the required phase relationship set by the second design equation in (8) can be maintained over a large frequency band. As the input frequency deviates from the designed center of the all-pass filter, the components ω_{L} and ω_{H} move accordingly, and the phase relationship is maintained as long as they both are in the linear region, until one of the two falls into the phase plateaux. This contributes to set the bandwidth of the circulator.

While this happens in the phase domain, there is ideally no filtering in the magnitude domain. This is a significant advantage with respect to high-order multi-section low-pass or band-pass filters, in which the phase relationship needs to be maintained while inside the filter bandwidth, to avoid magnitude attenuation of the frequency components. For such filters, one must extend the bandwidth to achieve phase shift at frequencies far from the cutoff.

If one considers the phase response of the second-order all-pass filter expressed in (15), it is possible to calculate the phase shifts ϕ_1, obtained when $\omega = \omega_{\mathrm{L}} = \omega_{\mathrm{in}} - \omega_{\mathrm{m}}$, and ϕ_2, obtained when $\omega = \omega_{\mathrm{H}} = \omega_{\mathrm{in}} + \omega_{\mathrm{m}}$, for variable ω_{in}. Their difference $\phi_2 - \phi_1$ determines how the second design equation in (8) is satisfied across variable input frequency, and when this diverts from the designed 180°, non-reciprocity is affected and bandwidth is limited. This phase difference is equal to 180° at the center of the all-pass filter and is always smaller than that, so it varies non-monotonically around it, showing a plateau (with zero derivative).

If one then considers the phase response of the first-order all-pass filter ϕ_3 expressed in (27) obtained when $\omega = \omega_{\mathrm{in}}$ for variable input frequency, this phase is equal to 90° at the center of the all-pass filter ω_0 and varies monotonically around it.

The overall condition for circulation is set by $\phi_2 - \phi_1 = 180°$ in the non-reciprocal branch and $\phi_3 = 90°$ in the two reciprocal branches, so one can combine them into one equation, namely, $\phi_{\mathrm{tot}} = \phi_2 - \phi_1 - 2\phi_3 = 0$. This quantity is plotted in Fig. 6(a).

In the case of an artificial transmission line implementation, the phase shifts ϕ_1 and ϕ_2 of the non-reciprocal branch, the phase shift ϕ_3 of the two $\lambda/4$ reciprocal branches, and the phase shift ϕ_4 of the additional $\lambda/8$ sections can all be expressed by (5). They vary monotonically around the center frequency ω_0.

The overall condition for circulation in this case is $\phi_2 - \phi_1 = 180°$ in the non-reciprocal branch, $\phi_3 = 90°$ in the two reciprocal branches, and $\phi_4 = 45°$, so one can combine them into one equation, namely, $\phi_{\mathrm{tot}} = \phi_2 - \phi_1 - 2\phi_3 - 2\phi_4 + 90° = 0$. This quantity is plotted in Fig. 6(a) for both ideal and artificial transmission lines, designed to achieve the same circulator function for the same ω_0 and ω_{m} as the designed all-pass filter architecture.

As one can see, if an error of 20° is tolerated in the overall constructive/destructive circulator phase relationship, the bandwidth over which this condition is satisfied is extended for the all-pass filter approach with respect to the transmission line case.

The reason is that the non-monotonic deviating phase of the second-order all-pass filter in the non-reciprocal branch partially compensates for the deviation of phase in the two

reciprocal branches. In the transmission line case, there is no compensation, and actually, deviations from the ideal value at the center of the circulator are enhanced both at low and high frequencies, thus reducing the bandwidth. This explains why the bandwidth of the circulator can be extended, as demonstrated by the comparison simulation in Fig. 6(b).

III. Cryo-CMOS Circulator

The proposed circulator, shown in Fig. 7, has been implemented in 40-nm CMOS technology with an ultra-thick top metal layer option. The overall architecture includes two reciprocal branches realized by first-order lattice LC all-pass filters and a non-reciprocal branch with two parallel I/Q paths, including a second-order bridged-T LC all-pass filter and passive mixers.

Inductors in the LC filters have been realized as multi-turn (3–4) spiral inductors with ultra-thick metal layer conductor and thick layer underpass. Capacitors have been realized as multi-finger interdigitated MOM capacitors. Inductors and capacitors have been designed to achieve the required phase shifts at the design frequency, according to the presented equations. Mixers have been implemented as differential nMOS-only passive mixers with aspect ratio $W/L = 50\ \mu$m/40 nm in a deep n-well to isolate from substrate noise. MOSFETs have been optimized to tradeoff R_{ON} resistance, causing additional insertion loss since in series with the signal path, and parasitic capacitance C_p, which produces unwanted phase shifts in the signal. The design values for the final implementation are $R_{ON} = 10\ \Omega$ and $C_p = 15$ fF at 300 K.

In the transmission line implementation [18], [19] (and with extra inductors in [20]), the parasitic capacitance C_p can be absorbed in the transmission line and reciprocal sections. However, with the proposed all-pass filter approach, the topology does not include shunt capacitors, so this feature cannot be exercised. Therefore, mixer parasitic capacitance and connections over non-negligible distance cause unwanted phase shifts in the reciprocal and non-reciprocal sections. The reciprocal parasitic phase shift is estimated from post-layout and electromagnetic (EM) simulation to be in total 12° at 300 K. Such parasitic reciprocal and non-reciprocal phase shifts have been compensated for in their respective sections, with an empirical redesign of the first-order and second-order all-pass filters to embed this extra phase shift, by tuning the component values to achieve an ideal circulator function in the overall system. The transfer functions of the modified filters are then less close to ideal values, therefore more sensitive to phase variations. The consequent tradeoff is that the parasitic capacitance of mixers should be kept to a minimum to make the compensation feasible. This amounts to reducing the size of the nMOS mixers, which, in turn, increases R_{ON} resistance. This has been mitigated by using low threshold voltage devices.

To realize connections between first-order and second-order all-pass filters over a non-negligible distance, microstrip edge-coupled differential lines in the topmost ultra-thick metal layer have been used. Cross-swapping has been used to obtain the same length for the two paths.

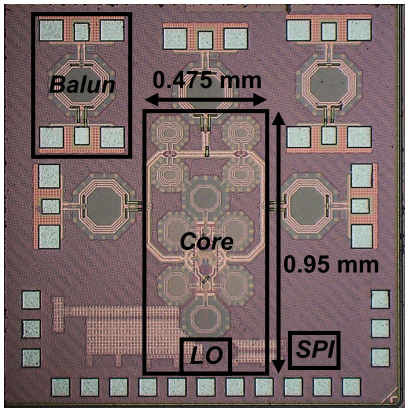

Fig. 8. Chip micrograph of the designed circulator, showing the circulator core, transformer baluns, clock generation path, and auxiliary structures.

The system has been designed to be differential. Therefore, transformer baluns have been included to convert the 50-Ω differential signal to 50-Ω single-ended for RF probing with GSG probes. A 50-Ω (tunable) on-chip termination resistor has been included at the secondary of the transformer for testing purposes. Separate transformers have been included on-chip to de-embed their influence from the measurement results of the circulator. De-embedding structures for SOLT calibration and de-embedding have been included on a separate chip.

The system has been designed for a target circulator center frequency ω_{in} of 6.5 GHz, with a clock signal $\omega_m = \omega_{in}/5$, yielding 1.3 GHz.

To generate the four required differential I/Q clock signals, an on-chip clock generation circuitry has been designed. A sinusoidal input at double frequency (2.6 GHz) is provided externally. An active common-source common-gate single-ended-to-differential amplifier generates a differential signal, which is then clipped to a square wave by further gain stages. This signal is fed into a C^2MOS latch-based divider, which generates the four I/Q differential phases, and finally, phase aligners and buffers drive the clock into the mixers. The devices used in the mixers and clock driver circuits are low threshold voltage, standard oxide nMOS/pMOS transistors with a nominal supply voltage of 1.1 V. The maximum tolerable gate-oxide voltage for such devices is 1.6 V. Therefore, the maximum safe operating region signal that the circulator can tolerate, to avoid oxide breakdown, is in the order of +14 dBm. This is well below the region where the circulator is going to be operated in the target application.

The local oscillator (LO) path and, especially, its input amplifier stages have been largely overdesigned to guarantee the circuit operation under large variations of circuit parameters, expected at cryogenic temperatures; therefore, its power consumption has not been optimized.

Together with the analog and RF circuitry, a digital SPI is included on-chip, to control tunability in the amplifier biasing points and especially to tune the controllable port impedance during testing.

The described circulator has been fabricated and the chip micrograph is shown in Fig. 8. The circulator core area, thanks to the all-pass filter approach, occupies only 0.45 mm^2.

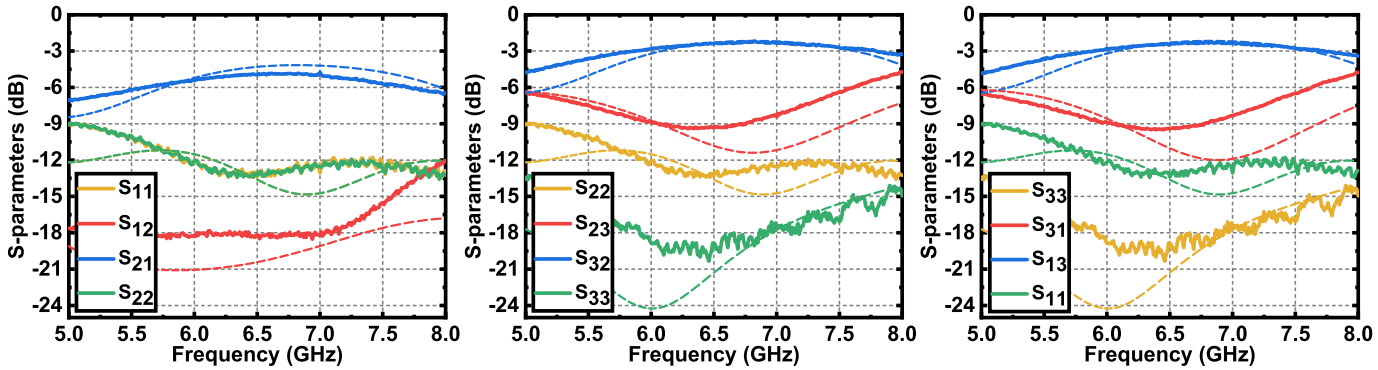

Fig. 9. Circulator S-parameter simulation (dashed line) and measurements (solid line) at 300 K.

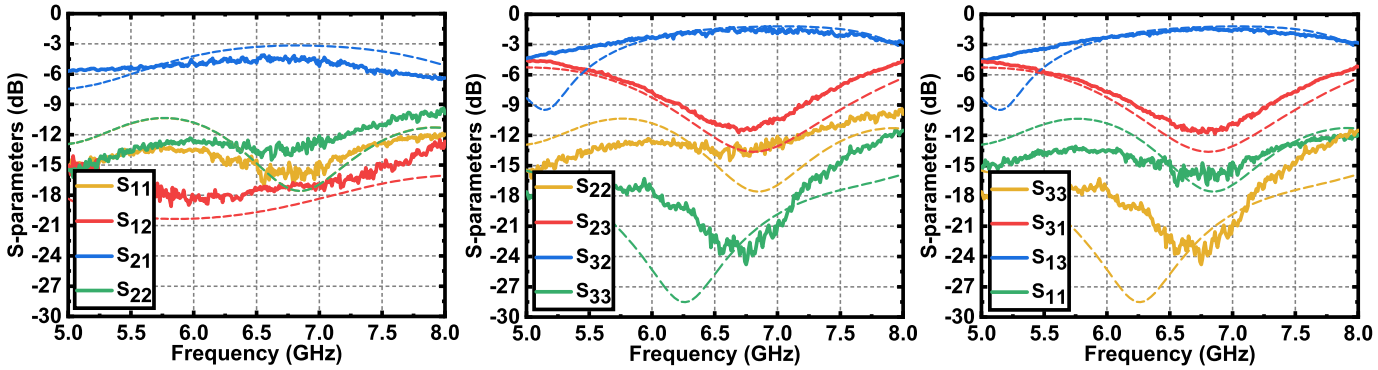

Fig. 10. Circulator S-parameter simulation (dashed line) and measurements (solid line) at 4.2 K.

IV. Cryogenic Temperature Design and Modeling

The circulator has been designed for operation from room temperature to cryogenic temperature, where it is supposed to be used in the target application. Room temperature operation has been used as a benchmark for functionality, while performance targets have been set for cryogenic operation at 4.2 K.

During operation at cryogenic temperature, many circuit parameters deviate considerably from their room temperature nominal value and modify the performance of the fundamental blocks in the circuit. At 4.2 K, carriers freeze out in the semiconductor substrate [26], thus causing a reduction of the available carrier density and a substantial increase in the bulk resistance; at the same time, the carrier mobility increases due to the reduced scattering mechanisms. Metals increase their conductivity, which, for high purity copper, is estimated to be ∼5 times larger than at room temperature [27].

Passive components are expected to increase their quality factor at cryogenic temperature. Inductors are expected to increase their Q factor by ∼2.6 times [28] due to the reduction of losses in the presence of a high resistivity substrate and reduced metal resistivity, while the value of inductance is going to reduce by ∼5% [28]. Capacitors are also going to have an increased quality factor due to reduced metal resistance, while the value of capacitance is going to increase by ∼3% [28]. The same will happen to all high-frequency differential lines that are going to experience lower insertion loss at 4.2 K.

Among active components, MOSFET transistors are going to experience an increase in threshold voltage V_{th} [29] by ∼100 mV. Although V_{th} increases, carrier mobility in the channel will increase by a larger factor, which will cause higher transconductance g_{m} and lower channel resistance. Therefore, for transistors used as switches, such as those used in the nMOS passive mixers, one expects a reduction of R_{ON} resistance, hence an improvement in conversion loss. In transistors used in saturation as amplifiers, such as those in the LO path, one expects reduced voltage headroom due to threshold voltage increase and larger gain for the same bias current. This explains the large overdesign of the LO path to guarantee operation under all conditions.

While predictive models exist for room temperature, there are no accurate models for cryogenic circuit design. For this reason, measurements and modeling steps [28] have been carried out prior to the design phase to assess the performance of passive RF circuits at cryogenic temperature, to be used for a first prediction (since the circuit is mostly passive) of the circuit performance at 4.2 K.

Modified design kit models have been developed for passives, in particular inductors and capacitors, accounting for variations at 4.2 K of the nominal value and parasitic components. These especially account for a largely increased substrate resistance, while reduced metal resistance has been included in post-layout extraction for ultra-thick top-metal layer only (used for all high-frequency lines). Finally, a modified substrate for EM simulation has been used for custom-designed passives, such as transformers, to predict

their behavior at 4.2 K. Lastly, only a modified channel resistance has been included in the transistor model to capture the main effect of the R_{ON} resistance reduction.

Simulations have been carried out at 300 K with standard design kits, and S-parameter results are overlaid in Fig. 9.

Simulations have also been performed with the modified cryogenic models and substrate to predict the performance of the passive circulator core at 4.2 K, and the S-parameter results are shown in Fig. 10.

The designed circulator has been considered for operation at cryogenic temperature; however, it could not be optimized, as the device models that have been established are still only partial. Active devices' behavior, including parasitics and noise performance, is not captured in such models, so this still represents a further optimization margin with respect to a full simulation with PDK models available at room temperature.

V. Measurements

The fabricated 40-nm circulator prototype has been bonded to a PCB for room temperature and cryogenic RF measurements in a probe station. The DC, analog low frequency, and digital lines have been connected to the PCB with phosphor bronze lines for thermal isolation, while the GSG pads have been left exposed for RF probes.

A. DC Measurements

The DC measurements have been performed in the presence of an external 2.6-GHz sinusoid to generate the required I/Q differential 1.3-GHz clock signals. The circulator core, including the on-chip frequency divider and the phase aligners with buffers driving the mixers, consumes 2.3 mA from the 1.1-V power supply, thus resulting in 2.5-mW power dissipation at 300 K. The additional amplifiers and gain stages consume 9 mA, thus resulting in additional 9.9-mW power dissipation, for structures required by on-chip testing. The overall power consumption of the prototype chip at 300 K is 12.4 mW.

When the circuit is cooled down to 4.2 K under the same voltage biasing conditions, the circulator core consumes 1.9 mA, resulting in 2.1 mW power dissipation, while the auxiliary circuitry consumes 7.7 mA, contributing to an additional 8.4-mW power dissipation at cryogenic temperature.

B. S-Parameter Measurements

The circulator S-parameters have been measured with RF probing in a Lake Shore CPX probe station. A Keysight N5245A PNA-X has been used as a vector network analyzer (VNA) to measure S-parameters, Aim-TTi MX100TP power supplies for biasing, and Keysight PSG E8267D signal generator was employed to provide the external LO signal. The complete measurement setup is shown in Fig. 11. The SOLT calibration has been performed prior to measurements to de-embed the effect of cables and probes, while transformer baluns at each of the three ports have been de-embedded thanks to separate test structures on-chip.

The S-parameter results at 300 K are reported in Fig. 9; the circuit operates with a 1-dB insertion loss and isolation

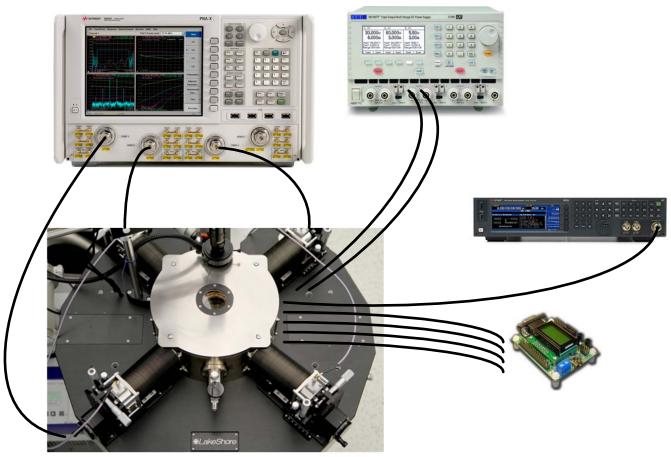

Fig. 11. Diagram of the test setup used for S-parameter measurements.

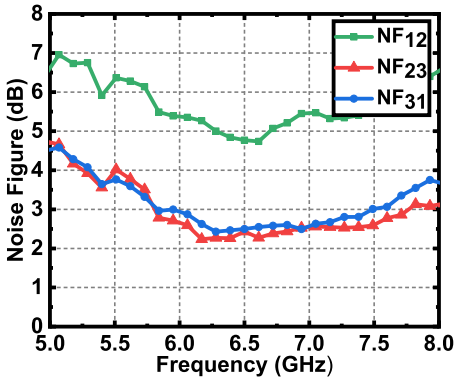

Fig. 12. Circulator noise figure measurements at 300 K.

bandwidth from 5.6 to 7.4 GHz, with a minimum insertion loss of 2.2 dB and a maximum isolation of 18 dB. The bandwidth of the circulator is defined [18] as the frequency overlap $[f_1, f_2] \cap [f_3, f_4]$ between the 1-dB bandwidth $[f_1, f_2]$ of the insertion loss parameter (e.g., S_{32}) and the 1-dB bandwidth $[f_3, f_4]$ of the isolation parameter (e.g., S_{12}). This results in non-reciprocity over a 28% fractional bandwidth, while impedance matching at all ports is maintained below -10 dB. This is in line with expectations from post-layout simulations. As suggested from the circuit symmetry, the S-parameters involving ports 1–3 and ports 2–3 show the same trend, while circulation between ports 1–2 is different, since the signal goes through the non-reciprocal section directly. The insertion loss involving ports 1–2 is higher than the others due to the loss of the passives in the second-order all-pass filters and also due to imperfect constructive interference, originated by imperfect matching to the required phase relationship. The reduced isolation between ports 3–2 and 1–3 is due to the fact that they are comprised between the two reciprocal branches, so they experience weaker non-reciprocity, and is also subject to imperfect destructive phase interference. The insertion loss can be improved in the same design by using a single path implementation, as in [19] and [20] (at the cost of more sensitivity to duty cycle mismatch [18]), instead of a double I/Q branch, and by improving the quality factor of the designed

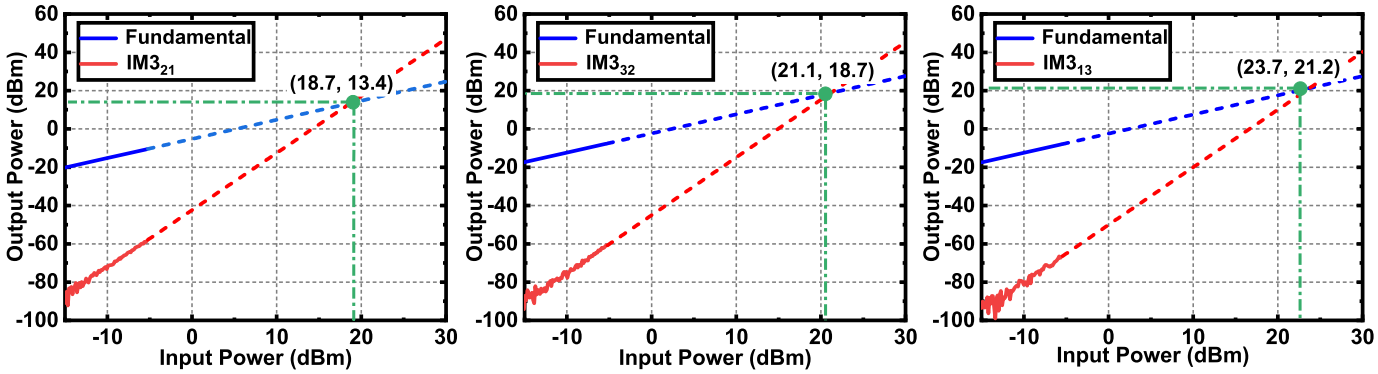

Fig. 13. Circulator linearity measurements at 300 K.

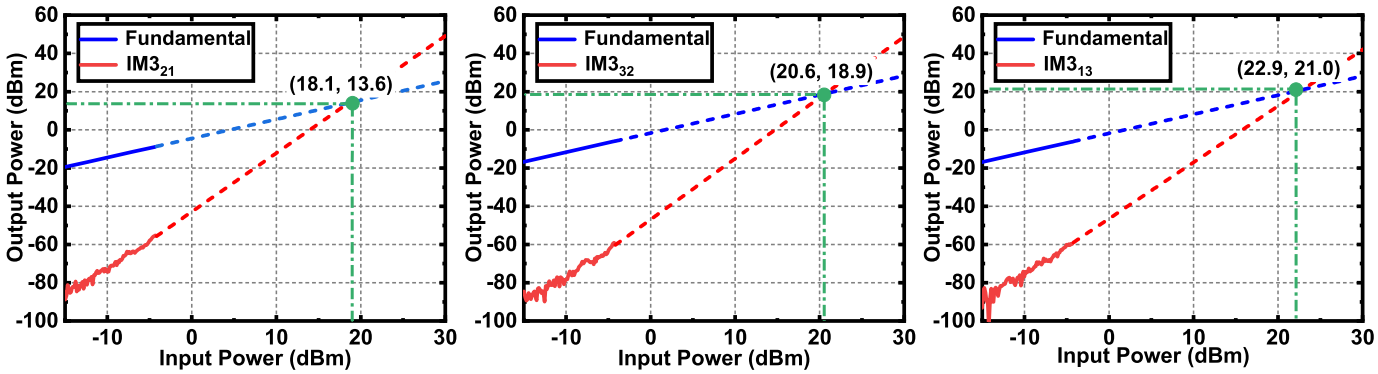

Fig. 14. Circulator linearity measurements at 4.2 K.

passives or using a better RF technology. The imperfect interference can be improved, with benefit on both insertion loss and isolation, by adding tunability in the filter capacitors and by adding phase control to the I/Q clock generation, to achieve more perfect phase matching. Moreover, in this work, a second-order all-pass filter is used. In principle, if a higher order filter is used, one could think that higher isolation can be achieved, by using the increased degrees of freedom to achieve better inter-stage impedance matching and more accurate phase matching. However, in the real implementation, many more passives, especially inductors, would be required, and their limited Q factor would result in extra loss, which would decrease the final destructive interference. Therefore, this might not result in better isolation, depending on the technology.

The S-parameters have been measured at 4.2 K as well, and the results are shown in Fig. 10. The same measurement setup as for 300 K has been used, but SOLT calibration has been repeated at 4.2 K, taking care to correct for reduced reference load resistance in the calibration kit. New transformer measurements have been taken to de-embed their (reduced) loss at 4.2 K. In particular, the insertion loss of de-embedding baluns is measured to be 2.1 dB at 300 K while it becomes 1.3 dB at 4.2 K. The circulator operates over a 1-dB insertion loss and isolation bandwidth between 5.8 and 7.6 GHz, while the minimum insertion loss is reduced to 1.3 dB and the maximum isolation becomes 17 dB.

As expected from cryogenic behavior, the operational bandwidth is slightly shifted toward higher frequency; this can be explained by a decrease in inductance, while capacitor values are almost kept constant. The minimum insertion loss is reduced since the quality factor of passives is increased and the R_{ON} resistance is smaller.

C. Noise Measurements

The noise performance of the circulator has been measured at 300 K using the source-mismatch-corrected noise figure measurement capabilities of the PNA-X with the same measurement setup as for S-parameters. The measured results are shown in Fig. 12 and they show good agreement with insertion loss measurements from S-parameters, with a minimum noise figure of 2.4 dB. The measurement accuracy with such setup is ± 0.1 dB, which is the noise figure of a reference through after all calibrations.

The noise of the circulator at 4.2 K, without considering contributions from clock feedthrough, is going to be determined from the passive core, whose noise is going to be the same as the measured 1.3-dB insertion loss at 4.2 K, namely, yielding a noise temperature of 1 K. Phase noise of the clock can be a concern in this case, but it can be filtered in the far-out region from the carrier by a band-pass filter, while clock feedthrough can still be cause of local noise increase at the frequency of the clock harmonics that fall in the band of the circulator.

D. Linearity Measurements

Finally, the circulator's linearity has been measured at 300 K, using the PNA-X as for S-parameters, performing

TABLE II
COMPARISON TABLE WITH STATE-OF-THE-ART INTEGRATED CIRCULATORS

	This work		[17]	[18]	[19]	[20]	[21]
Technology	40-nm CMOS		65-nm CMOS	45-nm SOI	180-nm SOI	45-nm SOI	45-nm SOI
Working temperature (K)	4.2	300	300	300	300	300	300
Architecture	All-pass		N-path	T-line	T-line	Band-pass	Active
Frequency (GHz)	5.8-7.6	5.6-7.4	0.61-0.97[1]	22.7-27.3	0.86-1.08	50-56.8	5.3-7.3[1]
Modulation index	5		1	3	3	7	N.A.
Insertion loss 2-3/ANT-RX (dB)	1.3	2.2	1.7	3.2	2.1	3.1	5
Isolation (dB)	17	18	>20	18.5	>25	>20	>30
Fractional bandwidth[2] (%)	28	28	4.3	18	17	14.5	6.3
Noise figure 2-3/ANT-RX[3] (dB)		2.4-3.4	4.3	3.3-4.4	2.9-3.1	3.2	20
IIP3 (dBm)	>+18.1	>+18.7	+27.5	+20.1	+50	+19.4	20
Core area	0.45 mm^2 λ^2/4727		25 mm^2 λ^2/5760	2.16 mm^2 λ^2/67	16.5 mm^2 λ^2/5789	1.72 mm^2 λ^2/18	1.57 mm^2 λ^2/1442
Power consumption (mW)	2.1/10.5[4]	2.5/12.4[4]	59	78.4	170	41	415
Normalized power P_{DC}/f_0 (mW/GHz)	1.6	1.9	75	3.1	175	0.8	66

[1]Range of center frequency tunability, [2]1-dB insertion loss and isolation bandwidth, [3]Data is at 300 K for all works, [4]Core (divider and mixer buffers) power and overall power consumption respectively.

S-parameter and power calibrations. IM3 versus input power has been measured to derive IIP3 and OIP3, and the measured results are shown in Fig. 13. The measured IIP3 is higher than +18.7 dBm in all directions of circulation.

Linearity has been measured at 4.2 K as well, without a modified setup, and the results are plotted in Fig. 14. The measured IIP3 is larger than +18.1 dBm in all directions of circulation, which is sufficient for quantum computing applications since the handled signal is very small (−90 dBm) and well below the non-linear region.

VI. DISCUSSION

The presented circulator is targeting quantum computing applications, but it could also be used for full-duplex transceiver applications, as the proposed techniques are also useful at 300 K. The closest application could be for 5G new radio in the sub-6-GHz band, where the presented design techniques could be adapted without major modifications. In this case, however, the design targets would be quite different; power consumption should still be minimized, but large power handling and linearity should become a priority to meet transmitter requirements. To achieve this, techniques to enhance linearity, such as the one proposed in [16], should be applied, and the use of device stacking and thick-oxide transistors, as in [19], should be chosen.

VII. CONCLUSION

This article presents a 40-nm CMOS circulator operating from 300 K to 4.2 K, designed for quantum bit readout. A staggered commutation circulator with a new all-pass filter architecture is designed to address the reduction of power consumption, bandwidth extension, and compact area. Thanks to the use of a second-order bridged-T all-pass filter, a large modulation index $m = 5$ is achieved, thus reducing power consumption while using smaller area than multi-section transmission line approaches. Thanks to the linear phase response, the fractional bandwidth is also extended.

A power consumption of only 2.5 mW is achieved at 300 K, while this is reduced to 2.1 mW at 4.2 K. A fractional bandwidth of 28% between 5.6 and 7.4 GHz is achieved at 300 K, with a 2.2-dB minimum insertion loss, 18-dB isolation, and 2.4-dB noise figure. While keeping the same fractional bandwidth, the circulator operates between 5.8 and 7.6 GHz with a 1.3-dB minimum insertion loss and 17-dB isolation at 4.2 K. The active area of the circuit is only 0.45 mm^2. A complete comparison with state-of-the-art circulators is provided in Table II.

Such a circuit allows miniaturization and multiplexing in multi-qubit readout systems for power-constrained cryostats.

ACKNOWLEDGMENT

The authors would like to thank all the members of the AQUA laboratory in the Netherlands and in Switzerland, for useful discussions and Prof. D. DiVincenzo for insightful discussions about circulators for quantum computing.

REFERENCES

[1] R. P. Feynman, "Simulating physics with computers," *Int. J. Theor. Phys.*, vol. 21, nos. 6–7, pp. 467–488, 1982.
[2] A. Montanaro, "Quantum algorithms: An overview," *NPJ Quantum Inf.*, vol. 2, no. 1, Jan. 2016.
[3] F. A. Zwanenburg *et al.*, "Silicon quantum electronics," *Rev. Mod. Phys.*, vol. 85, pp. 961–1019, Jul. 2013.

[4] P. Krantz, M. Kjaergaard, F. Yan, T. P. Orlando, S. Gustavsson, and W. D. Oliver, "A quantum engineer's guide to superconducting qubits," *Appl. Phys. Rev.*, vol. 6, no. 2, Jun. 2019, Art. no. 021318.
[5] A. G. Fowler, M. Mariantoni, J. M. Martinis, and A. N. Cleland, "Surface codes: Towards practical large-scale quantum computation," *Phys. Rev. A, Gen. Phys.*, vol. 86, no. 3, Sep. 2012, Art. no. 032324.
[6] B. Patra *et al.*, "Cryo-CMOS circuits and systems for quantum computing applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan. 2018.
[7] J. C. Bardin *et al.*, "29.1 A 28nm Bulk-CMOS 4-to-8GHz <2 mW cryogenic pulse modulator for scalable quantum computing," in *IEEE Int. Solid- State Circuits Conf. ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 456–458.
[8] D. Ristè *et al.*, "Deterministic entanglement of superconducting qubits by parity measurement and feedback," *Nature*, vol. 502, no. 7471, pp. 350–354, Oct. 2013.
[9] J. M. Elzerman, R. Hanson, L. H. Willems van Beveren, B. Witkamp, L. M. K. Vandersypen, and L. P. Kouwenhoven, "Single-shot read-out of an individual electron spin in a quantum dot," *Nature*, vol. 430, no. 6998, pp. 431–435, Jul. 2004.
[10] D. J. Reilly, C. M. Marcus, M. P. Hanson, and A. C. Gossard, "Fast single-charge sensing with a rf quantum point contact," *Appl. Phys. Lett.*, vol. 91, no. 16, Oct. 2007, Art. no. 162101.
[11] M. F. Gonzalez-Zalba, S. Barraud, A. J. Ferguson, and A. C. Betz, "Probing the limits of gate-based charge sensing," *Nature Commun.*, vol. 6, no. 1, p. 6084, Jan. 2015.
[12] T. Botzem *et al.*, "Tuning methods for semiconductor spin qubits," *Phys. Rev. Appl.*, vol. 10, no. 5, Nov. 2018, Art. no. 054026.
[13] *QuinStar Technology*. Accessed: Jan. 30, 2020. [Online]. Available: http://www.quinstar.com
[14] G. Viola and D. P. DiVincenzo, "Hall effect gyrators and circulators," *Phys. Rev. X*, vol. 4, no. 2, May 2014, Art. no. 021019.
[15] A. C. Mahoney *et al.*, "On-chip microwave quantum Hall circulator," *Phys. Rev. X*, vol. 7, no. 1, Jan. 2017, Art. no. 011007.
[16] J. Zhou, N. Reiskarimian, and H. Krishnaswamy, "9.8 Receiver with integrated magnetic-free N-path-filter-based non-reciprocal circulator and baseband self-interference cancellation for full-duplex wireless," in *Proc. IEEE Int. Solid-State Circuits Conf. ISSCC Dig. Tech. Papers*, Jan. 2016, pp. 178–180.
[17] N. Reiskarimian, J. Zhou, and H. Krishnaswamy, "A CMOS passive LPTV nonmagnetic circulator and its application in a full-duplex receiver," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1358–1372, May 2017.
[18] T. Dinc, A. Nagulu, and H. Krishnaswamy, "A millimeter-wave non-magnetic passive SOI CMOS circulator based on spatio-temporal conductivity modulation," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3276–3292, Dec. 2017.
[19] A. Nagulu and H. Krishnaswamy, "Non-magnetic CMOS switched-transmission-line circulators with high power handling and antenna balancing: Theory and implementation," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1288–1303, May 2019.
[20] A. Nagulu and H. Krishnaswamy, "28.5 Non-magnetic 60GHz SOI CMOS circulator based on Loss/Dispersion-engineered switched band-pass filters," in *Proc. IEEE Int. Solid- State Circuits Conf. ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 446–448.
[21] K. Fang and J. F. Buckwalter, "A tunable 5–7 GHz distributed active quasi-circulator with 18-dBm output power in CMOS SOI," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 11, pp. 998–1000, Nov. 2017.
[22] B. Tang, X. Gui, J. Xu, Q. Xia, and L. Geng, "A dual interference-canceling active quasi-circulator achieving 36-dB isolation over 6-GHz bandwidth," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 6, pp. 409–411, Jun. 2019.
[23] A. Ruffino, Y. Peng, F. Sebastiano, M. Babaie, and E. Charbon, "A 6.5-GHz cryogenic all-pass filter circulator in 40-nm CMOS for quantum computing applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 107–110.
[24] N. Reiskarimian and H. Krishnaswamy, "Magnetic-free non-reciprocity based on staggered commutation," *Nature Commun.*, vol. 7, no. 1, Apr. 2016, Art. no. 11217.
[25] R. Levy, "Realization of practical lumped element all-pass networks for delay equalization of RF and microwave filters," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 12, pp. 3307–3311, Dec. 2011.
[26] F. Balestra and G. Ghibaudo, "Brief review of the MOS device physics for low temperature electronics," *Solid-State Electron.*, vol. 37, no. 12, pp. 1967–1975, Dec. 1994.
[27] M. Mehrpoo *et al.*, "Benefits and challenges of designing cryogenic CMOS RF circuits for quantum computers," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2019, pp. 1–5.
[28] B. Patra, M. Mehrpoo, A. Ruffino, F. Sebastiano, E. Charbon, and M. Babaie, "Characterization and analysis of on-chip microwave passive components at cryogenic temperatures," 2019, *arXiv:1911.13084*. [Online]. Available: http://arxiv.org/abs/1911.13084
[29] A. Beckers, F. Jazaeri, and C. Enz, "Cryogenic MOS transistor model," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3617–3625, Sep. 2018.

Andrea Ruffino (Student Member, IEEE) was born in Turin, Italy, in 1991. He received the B.Sc. degree *(cum laude)* in engineering physics from the Politecnico di Torino, Turin, in 2013, and the triple-joint M.Sc. degree *(cum laude)* in micro and nanotechnologies for integrated systems from the Politecnico di Torino, the Institut National Polytechnique de Grenoble (INPG), Grenoble, France, and École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, in 2015. He is currently pursuing the Ph.D. degree in cryogenic CMOS electronics for spin and superconducting qubits with EPFL.

From 2015 to 2016, he was with Hypres, Inc., Elmsford, NY, USA, where he was involved in designing superconducting readout circuits in rapid single flux quantum (RSFQ) technology for superconducting nanowire detectors. In 2016, he joined EPFL. His current research interests include analog and RF integrated circuit design, cryogenic CMOS electronics for quantum computing applications, superconducting electronics, and sensors.

Yatao Peng (Member, IEEE) received the B.Eng. degree in information engineering from Tianjin Normal University, Tianjin, China, in 2010, and the Ph.D. degree in electronics engineering from the University of Chinese Academy of Sciences, Beijing, China, with a focus on multi-band/wideband RF front-end circuits in wireless communication stations.

From 2016 to 2017, he was a Post-Doctoral Researcher with the University of Macau, Macau, China, where he was involved in CMOS millimeter-wave integrated circuit design. From 2017 to 2018, he was with the National University of Singapore, Singapore, where he served as a Researcher to develop CMOS phase-shifter modules for hybrid integrated flexible electronic systems. He is currently a Scientist with Advanced Quantum Architecture Laboratory, École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland. His current research interests include CMOS cryogenic RF circuits for quantum computing applications.

Fabio Sebastiano (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees *(cum laude)* in electrical engineering from University of Pisa, Pisa, Italy, in 2003 and 2005, respectively, the M.Sc. degree *(cum laude)* from the Sant'Anna School of Advanced Studies, Pisa, in 2006, and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 2011.

From 2006 to 2013, he was with NXP Semiconductors Research, Eindhoven, The Netherlands, where he conducted research on fully integrated CMOS frequency references, deep-submicrometer temperature sensors, and area-efficient interfaces for magnetic sensors. In 2013, he joined the Delft University of Technology, where he is currently an Assistant Professor. He has authored or coauthored one book, 11 patents, and over 60 technical publications. His main research interests are cryogenic electronics for quantum computing, quantum computing, sensor readouts, and fully integrated frequency references.

Dr. Sebastiano is also a member of the Technical Program Committee of the RFIC Symposium, an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, and a Distinguished Lecturer of the Solid-State Circuits Society. He was a co-recipient of the Best Student Paper at International Symposium on Circuits and Systems (ISCAS) in 2008, the Best Paper Award at International Workshop on Advances in Sensors and Interfaces (IWASI) in 2017, and the Best IP Award at Design, Automation and Test in Europe (DATE) Conference in 2018.

Masoud Babaie (Member, IEEE) received the Ph.D. degree *(cum laude)* in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2016.

In 2006, he joined the Kavoshcom Research and Development Group, Tehran, Iran, where he was involved in designing wireless communication systems. From 2009 to 2011, he was the CTO of the Kavoshcom Research and Development Group. From 2014 to 2015, he was a Visiting Scholar Researcher with the Berkeley Wireless Research Center, Berkeley, CA, USA. In 2016, he joined the Delft University of Technology, where he is currently a tenured Assistant Professor. He has coauthored one book, two book chapters, 11 patents, and over 40 technical publications. His current research interests include RF/millimeter-wave integrated circuits and systems for wireless communications and cryogenic electronics for quantum computation.

Dr. Babaie has been a Committee Member of Student Research Preview (SRP) of the IEEE International Solid-State Circuits Conference (ISSCC) since 2017 and will join the Technical Program Committee of the IEEE European Solid-State Circuits Conference (ESSCIRC) in 2020. He was a co-recipient of the 2015–2016 IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award and the 2019 IEEE ISSCC Best Demo Award. In 2019, he received the Veni Award from the Netherlands Organization for Scientific Research (NWO).

Edoardo Charbon (Fellow, IEEE) received the Diploma degree from ETH Zürich, Zürich, Switzerland, in 1988, the M.Sc. degree from the University of California at San Diego, La Jolla, CA, USA, in 1991, and the Ph.D. from the University of California at Berkeley, Berkeley, CA, USA, in 1995, all in electrical engineering and EECS.

He has consulted with numerous organizations, including Bosch, X-Fabs, Texas Instruments, Maxim, Sony, Agilent, and the Carlyle Group. He was with Cadence Design Systems from 1995 to 2000, where he was the Architect of the company's initiative on information hiding for intellectual property protection. In 2000, he joined Canesta, Inc., as the Chief Architect, where he led the development of wireless 3-D CMOS image sensors. Since 2002, he has been a member of the Faculty of the École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, where has been a Full Professor since 2015. From 2008 to 2016, he was with the Delft University of Technology, Delft, The Netherlands, as the Chair of VLSI Design. He is also a Distinguished Visiting Scholar with the W. M. Keck Institute for Space, California Institute of Technology, Pasadena, CA, USA, and a fellow of the Kavli Institute of Nanoscience Delft, Delft. He has authored or coauthored over 350 articles and two books. He holds 21 patents. His interests span from 3-D vision, fluorescence-lifetime imaging microscopy (FLIM), fluorescence correlation spectroscopy (FCS), and near-infra-red optical tomography (NIROT) to super-resolution microscopy, the time-resolved Raman spectroscopy, and cryo-CMOS circuits and systems for quantum computing.