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Wideband and High-Efficiency Radiation from Chip with Artificial Dielectric Superstrates

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***Abstract*—We present an approach to realize wideband and low-loss antennas and antenna arrays on chip. The radiators are loaded with an artificial dielectric superstrate to improve the bandwidth and the overall efficiency. An example of design is proposed, consisting of an array of connected-dipole elements operating in a frequency band around 300 GHz. The antenna elements are located in the close proximity of a metal plane that functions as a shield from the lossy silicon substrate. Although the distance from the ground plane is only one fortieth of the wavelength, a bandwidth of 15% is achieved by loading the antenna with an artificial dielectric superstrate with high equivalent permittivity. The artificial dielectric does not support surface waves as a real dielectric, due to its anisotropic property. Consequently, remarkably high efficiency can be achieved with this radiation concept (>60% from simulation).**

***Index Terms*—Artificial dielectric, on-chip antennas, wideband antenna.**

I. Introduction

As the operating frequency of radar and wireless communication systems increases, the separation of antenna and electronic circuit designs is no longer possible. The recent demand for compact low-cost transceivers in short-range communication and sensor applications is urging the necessity to integrate the antennas with the electronics. Automotive radars and ultrafast wireless communication are two applications with huge market potentials that require a high level of integration. Thus, the recent trend is to place the antennas as close as possible to the electronic circuits, on the same semiconductor chip, to facilitate the interconnection.

Although leading to low-cost compact systems, on-chip integrated antennas have never shown good performance because of their intrinsic low efficiency. These antennas are limited by problems such as narrow bandwidth, low front-to-back radiation ratio and high surface-wave loss. A typical layer stack of a chip is shown in Fig. 1 and consists of a thin layer of silicon dioxide (SiO_2), about 10 μm thick, on which the antenna is realized (e.g., a dipole or a slot antenna). A conducting metal plane separates the SiO_2 slab from a thick silicon (Si) layer. The metal plane has the purpose to shield the antenna from the underlying silicon, since this latter is characterized by very high losses [1].

When a dipole antenna is located at a small electrical distance from a metal plane, the electric current tends to cancel out with the image current and the antenna can be matched only over an extremely narrow bandwidth. Furthermore, if a slot is in the close proximity of a metal plane, a very large portion of the power is lost due to the excitation of strong parallel plate waveguide (PPW) modes between the slot plane and the backing reflector. A solution to mitigate this problem was proposed in [2]: by including a quartz superstrate above the chip, the antenna tends to radiate predominantly in the direction of such material, reducing the amount of power that remains confined within the SiO_2 layer in the form of PPW modes. However, such superstrate supports the propagation of surface waves, which limits the maximum achievable efficiency and can deteriorate the quality of the radiation patterns.

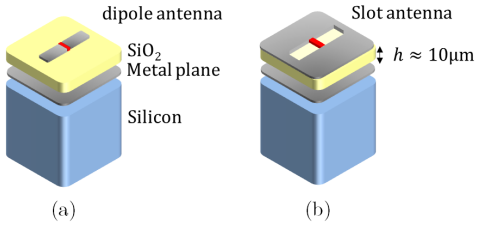

Fig. 1. (a) Dipole and (b) slot antennas on a silicon chip.

Another option that has been utilized to eliminate substrate losses consists in etching away the substrate locally under the antenna structure [3]. However, an antenna located on a SiO_2 membrane will tend to radiate equal power in the lower and upper half spaces, with poor front-to-back ratio. A solution to improve the front-to-back ratio without generating surface-wave losses was recently presented in [4]. In that work, an integrated double-slot antenna operating at 300 GHz was loaded with artificial dielectric layers (ADL). The silicon was etched away under the double slot. Due to its anisotropy, the ADL synthesize a slab with very high permittivity material for rays that travel normal to the stratification, but low effective permittivity for angles tending to grazing. Thus total internal reflection at the interface between ADL and air does not occur, with almost negligible power being launched into surface waves. Despite the good efficiency of the design in [4], the etching of the silicon still increases the manufacturing costs, because of the long process needed to etch through the wafer and release the membranes.

In this work, we propose a design that exploits the ADL but does not require the removal of the silicon under the antenna. The shielding metal is kept between the antenna and the lossy substrate. The radiator is composed of an array of connected dipoles, located at a distance of 12 μm from the

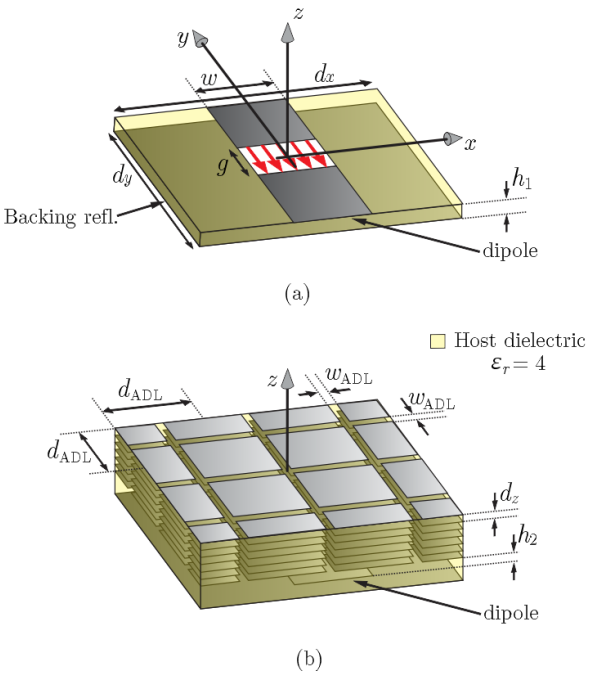

Fig. 2. Unit cell of a connected-dipole array on chip, (a) without any superstrate and (b) loaded with ADL superstrate.

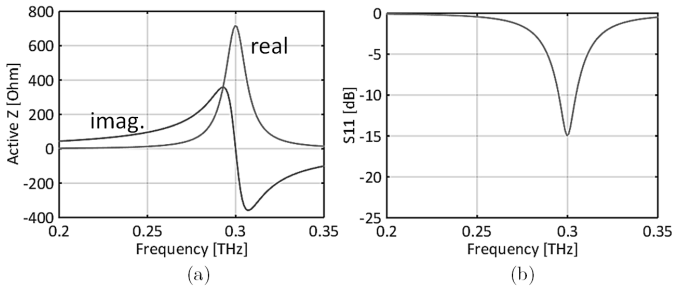

Fig. 3. Active input impedance and reflection coefficient of the unit cell in Fig. 2(a).

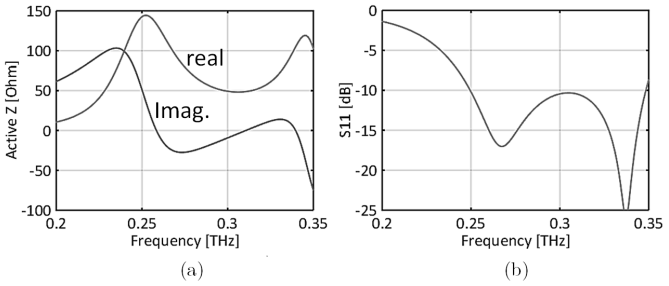

Fig. 4. Active input impedance and reflection coefficient of the unit cell in Fig. 2(a), when the array is loaded with an homogeneous dielectric slab with relative permittivity $\varepsilon_r = 32$ and height of 35μm.

ground plane. Full-wave simulations show a relative bandwidth of 15% around 300 GHz with a 2×4 array, and total efficiency higher the 60%. Wider bandwidths can be obtained with larger arrays.

II. Antenna Concept

Connected array of dipoles have been proposed in the past to achieve wideband designs, both at microwave and THz frequencies [6]–[8]. The connection between the elements allows the currents to travel along the entire array without supporting the typical resonances of half-wavelength dipoles. Practically, the bandwidth of a connected array is limited by the distance from the ground plane, that is used to ensure unidirectional radiation.

The unit cell of a connected array on chip can be depicted as in Fig. 2(a). The distance from the ground plane is indicated with h_1 and is assumed to be equal to 12 μm, as in typical stacks of complementary metal-oxide semiconductor (CMOS) or BiCMOS technology. The dielectric between the dipole and the ground plane is assumed to be SiO_2, with relative permittivity $\varepsilon_r = 4$. When considering 300 GHz as operating frequency, the distance from the backing reflector is smaller than $\lambda_d/40$ (λ_d is the wavelength in the dielectric) and thus even a connected array cannot be matched over a wide bandwidth. To highlight this aspect, the active input impedance and the reflection coefficient of the unit cell in Fig. 2(a) are shown in Fig. 3. The array period is set to $d_x = d_y = 230$ μm and the width of the dipole and the size of the feeding gap are $w = 107$ μm and $g = 12$ μm, respectively. These geometrical parameters have been found with an optimizer based on a genetic algorithm, combined with the closed-form spectral Green's function solution of connected arrays [5], [7]. It can be observed that the matching can be achieved only over a very narrow band of about 3%.

To improve the bandwidth performance, we now consider the case when the same array depicted in Fig. 2(a) is loaded with a homogenous dielectric slab with very high relative permittivity (e.g. $\varepsilon_r = 32$) and 35 μm thick. Enhanced performance can be achieved with this new configuration, as shown in Fig. 4. A relative bandwidth of 30% is observed, when referring to a normalization impedance of 100 Ω.

A practical way to implement a superstrate with high permittivity is to use artificial dielectric layers (ADL) as done in [4]. The unit cell becomes the one shown in Fig. 2(b). The ADL consists of a cascade of planar electrically small patches embedded in a host medium to synthesize a much higher equivalent permittivity [9]. The fabrication of the ADL can be performed with a CMOS back-end compatible integrated circuit process, as described in [4]. The performance achieved with this configuration is shown in Fig. 5. The bandwidth performance is comparable to the case of homogeneous dielectric. The main advantage of ADL compared to standard dielectric is that high permittivity can be achieved without supporting surface waves. This beneficial property is a consequence of the anisotropic characteristics of the ADL, which implement high permittivity only for the field traveling orthogonal to the stratification, but low permittivity for the field propagating towards grazing angles.

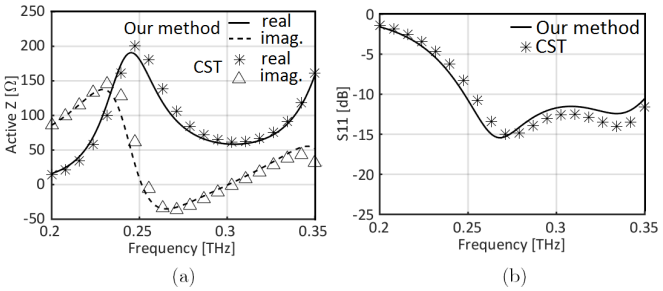

Fig. 5. (a) Active input impedance and (b) active reflection coefficient, for the unit cell in Fig. 2(b). Results obtained with the spectral Green's function method in [5] are compared with CST simulations [10].

III. Finite Array Simulations

The results shown in the last section refer to infinite array simulations. We now report the simulated performance of a finite array of 2×4 elements. The array layout is depicted in Fig. 6, where the ports are numbered from 1 to 8. The entire structure has been simulated with CST [10]. The active reflection coefficient, reported in Fig. 7(a), yields a −10 dB bandwidth of about 15% centered at 285 GHz. It can be noted that the achieved bandwidth is narrower than the infinite array approximation (Fig. 5(b)). This behavior is expected due to the relatively small size of the array, resulting in strong edge effects. Configurations including larger number of elements exhibit wider bandwidth. The simulated results refer to an ideal excitation of the dipoles, realized with a delta-gap, and to infinitely thin metal layers. A more realistic design that includes feeding lines and the actual metal thickness will be carried out and presented at the time of the conference.

The total efficiency, which includes the Ohmic and dielectric losses, as well as the mismatch losses, is higher than 60% within the matching bandwidth. Ohmic losses are lower than 2 dB, when considering aluminum as the metal for the dipoles and the ADL (with conductivity of $\sigma = 2.6 \times 10^7$ S/m), and copper for the ground plane ($\sigma = 4.5 \times 10^7$ S/m).

The radiation patterns in terms of gain are presented in Fig. 8, for three frequencies within the bandwidth of operation. The array provides a maximum gain higher than 8.5 dBi. The total area occupation of the antenna and the ADL is 1×1.45 mm^2.

Regarding the envisaged fabrication, the antenna can be realized with a commercial CMOS or Bi-CMOS process, whereas the ADL can be manufactured with a dedicated CMOS back-end compatible process [4] and used as an add-on component.

IV. Conclusion

A novel concept to realize efficient and wideband radiation from chips was presented. This antenna solution merges the concepts of connected arrays and ADL superstrates, to enhance the performance of typical on-chip radiators. A design example was also provided, consisting of an array of 2×4 connected dipoles, operating in the presence of a 7-layer ADL superstrate. The simulated performance indicates a bandwidth of 15%, total efficiency exceeding 60% and maximum gain higher than 8.5 dB.

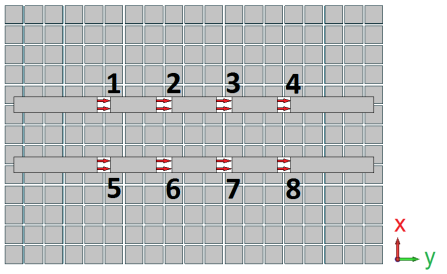

Fig. 6. Layout of the 2×4 connected-dipole array with ADL structure. The metalization is hosted by an infinite slab of SiO_2.

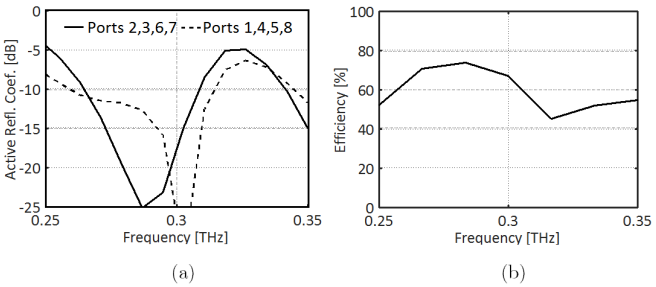

Fig. 7. (a) Active reflection coefficient of the array elements in Fig. 6 and (b) total efficiency. Results are obtained with CST simulations [10].

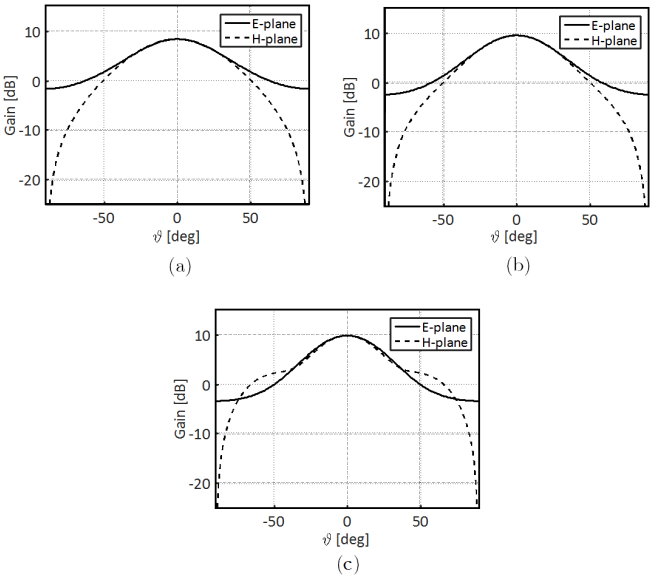

Fig. 8. Simulated gain patterns in the E- and H-plane at (a) 267 GHz, (b) 283 GHz and (c) 300 GHz.

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