Master Thesis

A Low-Power CMOS Wind Sensor

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Challenge the future

MASTER THESIS

A LOW-POWER CMOS WIND SENSOR

by

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ABSTRACT

This work describes a low-power and low-cost alternative to mechanical wind sensors, suitable for volume production in standard CMOS processes. The CMOS wind sensor operates in the electro-thermal domain; therefore, it has no moving parts and therefore requires very little maintenance. Moreover, the CMOS wind sensor is an active sensor, compared to its mechanical counterpart. Its sensitivity can be easily adjusted by changing the magnitude of the excitation signal.

Despite the manufacturing advantages of CMOS technology, the wind sensor has not attained commercial success in the market. This is due, in part, to process spread and packaging artifacts that have resulted in offset, nonlinearity and angle errors in detecting wind speed and direction. Because of this, expensive manual calibration is required to compensate these errors. Furthermore, its power consumption, in the order of tens of milliwatts, is not yet low enough to compete with its MEMS counterparts.

In this thesis, the design of a new version of the wind sensor is described, which aims to address the drawbacks of previous designs. Four extra resistors were added at each corner to electrically compensate for packaging artifacts, with the aim of reducing calibration costs. Larger thermopiles (a number of thermocouples in series) were used, resulting in a greater signal-to-noise ratio (SNR). Internal signals were buffered to output pads to gain more insight into the magnitude of the sensor's internal signal swings. With these improvements, the resulting wind sensor chip consumes less than 30 mW of heating power and has an accuracy of ±0.6 m/s (speed) for wind speeds ranging from 1 to 25 m/s, and ±2.5°(direction) for a range of 4 to 25 m/s.

Contents

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Many people have supported me during this project. Without them, completing this challenge would have been impossible. Therefore, I want to take a moment to thank them for their effort.

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This work is mainly based on the work of Wouter Brevet and Jiangfeng Wu, but also on previous work. 'It is by standing on the shoulders of giants', quoting Isaac Newton. Therefore, I want to thank them for their work on which I could build.

Finally, I would like to thank my family and friends, my sister for the graphical design and especially my wife, Alida. She has always patiently supported me, and motivated me to push through. Thank you for your love.

I want to dedicate this work to my Lord, God and Saviour, for it is He who gives me the breath of life, every single day.

And the LORD God formed man of the dust of the ground,
and breathed into his nostrils the breath of life;
and man became a living soul.
Genesis 2:7 KJV

1

INTRODUCTION

Flow sensors have a wide range of applications, such as industrial process monitoring, domestic water consumption and research on respiratory diseases [1]. The thermal wind sensor is a specific type of flow sensor. It estimates the wind direction and magnitude by measuring the cooling effect of flowing air on a heated substrate. The most obvious use of a wind sensor is in a weather station, but wind sensors also find application in air transportation, weather forecasting, energy conversion, architecture, sealing, farming, indoor climate control [2] and even in Mars rovers [3].

1.1. WIND SENSORS

Traditional wind sensors are mechanical, consisting of propellers or cups to measure the wind speed and vanes to detect the wind direction. Other sensors, like Laser Imaging Detection And Ranging (LIDAR), use the optical domain [4][5], utilizing the changing refraction coefficient of air in the presence of wind. Another use of the optical domain is found in the work of Meng et al., who senses the movement of an optical fiber as a function of wind speed [6]. Ultrasonic wind sensors use the acoustic domain [7]. They measure wind speed based on the time of flight of sonic pulses between pairs of transducers. The sensor from H. Irwin [8] uses the the principle of the Preston tube and can be categorized in the pneumatic domain. Here, the sensor utilizes the relation between wind speed and differences in air pressure. Wind sensors using the thermal domain are known as thermal wind sensors. In thermal wind sensors, the wind speed and direction influence the heat distribution within the system.

The category of thermal wind sensors is quite diverse. An overview of the different existing thermal wind sensors can be found in [2][9]-[11]. Therefore, this introduction will be limited to a discussion of the state-of-the-art of MEMS thermal wind sensors, and the history of the thermal wind sensors that have been developed at Delft University of Technology (section 1.3).

One of the first mentions of a CMOS sensor to measure (wind) flow, dates back to 1974 [12]. Since then, many variations and improvements have taken place. Many sensors have been realized with MEMS technology. They benefit from the small dimensions that can be achieved, and custom features that can be added regarding the different elements of the sensor. With these benefits, high sensitivity and low power consumption can be achieved [9][13]. Some known drawbacks are their higher (manufacturing) cost than normal chips and their fragility.

One of the most recent MEMS thermal wind sensor publications is from the beginning of 2017 [14]. Using only 14.5 mW, this sensor can measure wind speeds of up to 33 m/s with less than 5% accuracy error.

1.2. WORKING PRINCIPLE

1.2.1. THERMAL DOMAIN

The wind sensor utilizing the thermal domain is explained in more detail in this section. A thermal wind sensor consists of heaters to thermally excite a substrate, thermopiles to convert the thermal signals to the electrical domain, and electronics to realize the required signal processing. Figures 1.1-1.3 show a CMOS wind sensor chip glued to a ceramic disk, to protect the chip from contamination but still exchange heat with the wind. For convenience, only the parts of the chip needed for measurements in one dimension are shown. An orthogonal sensor provides measurements in two directions, which allows extraction of wind direction and magnitude. This configuration is one of the (non-MEMS) ways of realizing a wind sensor.

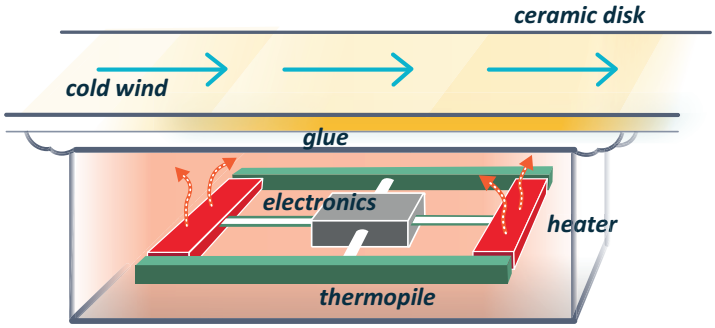


Figure 1.1: Cold wind crossing the ceramic disk, to which the thermal wind sensor is mounted.

Assume cold air flow, shown in blue in figure 1.1, crossing the surface of the chip from left to right. The heaters at the two edges of the chip provide constant heat to the chip, and the air traveling on the surface gets warmed up by the chip. The upstream side (left) encounters colder air than the downstream side (right), because the air has heated up while it travels over the surface of the chip due to the wind. This eventually results in a thermal gradient within the chip, as shown in figure 1.2.

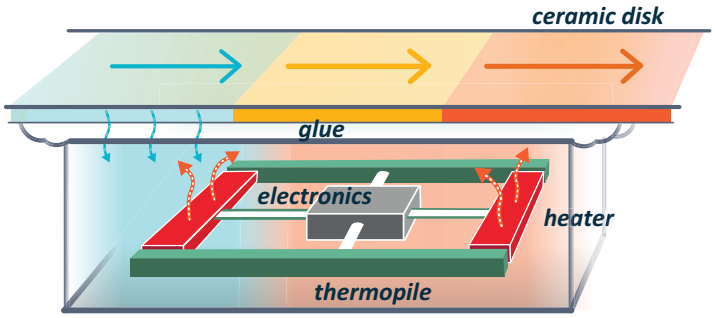


Figure 1.2: Thermal gradient within the chip due to the cooling effect of the wind.

To detect this thermal gradient, two thermopiles are placed orthogonally to the heaters. Due to the Seebeck effect, the thermopiles develop a voltage proportional to the thermal gradient. The wind magnitude is converted into the electrical domain and electronics in the chip can be used to further process this signal.

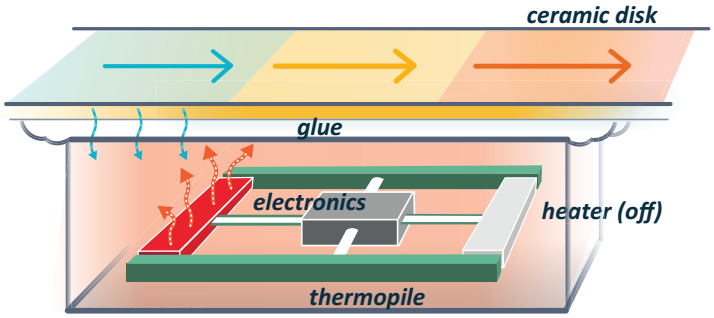


Figure 1.3: On-chip heaters activate to restore the thermal balance in the chip.

Alternatively, The thermal wind sensor may be operated according to a force-feedback principle, where a feedback loop works to restore the thermal balance on chip by increasing the heater drive depending on the thermopile voltage. This is illustrated in figure 1.3. The power spent to restore or keep the balance contains information about the wind speed. In fact, the power ratio of the two heaters can be directly related to a wind speed. This relation is discussed in section 4.3. To enable the formation of a thermal gradient on the chip, the chip must always be at a higher temperature than the ambient. To ensure this, heaters constantly dissipate some power.

The chip offers two modes of operation: one in which the total power consumption of the heaters is dynamic and one in which it is constant. The dynamic power mode aims to achieve a constant temperature difference between the chip and the ambient temperature by dynamically changing the power dissipated in the thermopiles, to ensure a more linear relation between wind speed and modulator output. This is referred to as the Constant Temperature Difference mode (CTD) [15]. The main drawback of CTD is the need for an external temperature sensor, to determine the temperature difference between chip temperature and ambient temperature. However, in the constant power (CP) mode, a constant amount of power is dissipated on the heaters to keep the chip above the ambient, at an indefinite temperature.

There are two ways to extract information about the wind from such a system. In the temperature gradient mode, the power is equally distributed over the chip and the thermal gradient on the chip is read out. In the temperature balance mode, the power is distributed with a ratio to balance the temperature gradient [16]. The thermal wind sensor of this work uses the CP mode with temperature balancing.

1.2.2. ELECTRICAL DOMAIN

The feedback from the output of the thermocouples to the input of the heaters is realized in the electrical domain. This is visualized in figure 1.4, the circuit that has been implemented by J. Wu [9]. The first component in the electrical domain is the thermopile, several in series connected thermocouples. A thermocouple consists of two types of material with different Seebeck coefficients. A temperature gradient along the length of the thermocouple will give rise to a proportional output voltage converting the information to the electrical domain.

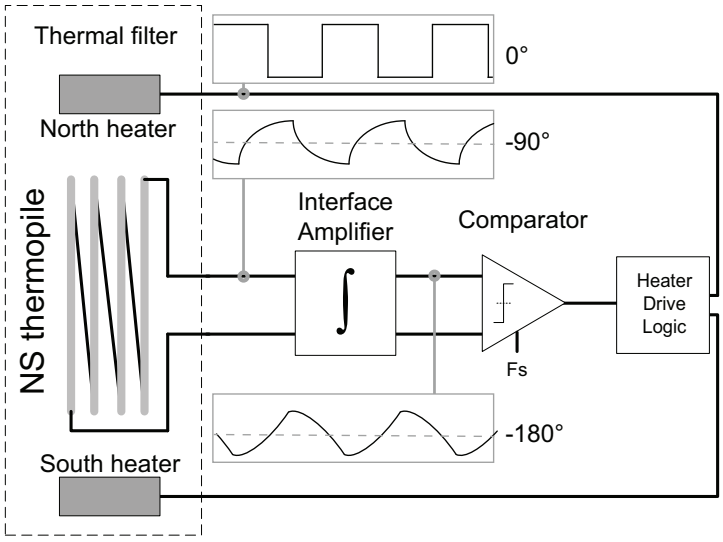


Figure 1.4: A hybrid system view of a thermal wind sensor [17], including signals.

The operation of the circuit in figure 1.4 is as follows: the output voltage of the thermopile is integrated and is fed to the input of a comparator. The comparator evaluates the sign of the integrated signal, determining which side of the chip is currently cooler. The corresponding heater is activated, to warm that side up. This converts the signal back to the thermal domain, closing the feedback loop.

The output of the comparator is used as the output signal for the system. When no input signal (wind) is present, both north and south heaters from figure 1.4 are activated alternately. With wind present, the average of the output signal contains the information about the strength of the wind in the direction of the

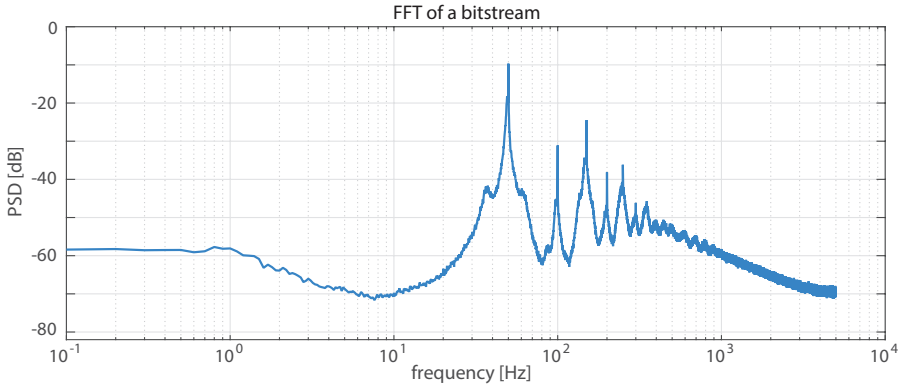


Figure 1.5: A fft of a bitstream at 27 mW heater power and a clock frequency of 10 kHz.

thermopiles.

It is important to note that in this system, there are two integrators: one in the thermal domain and one in the electrical domain. The silicon chip has a thermal capacity, and behaves like a lossy integrator for heat signals. The second integrator is formed as a Gm-C in the electrical domain, connected to the thermopile output. The presence of the two integrators and the quantizer in the feedback makes the system very similar to a second-order ΣΔ modulator. This means that the system also features noise shaping; quantization noise originating from the one bit comparator is filtered to higher, out-of-band frequencies. The 'lossy integrator' results in a reduced noise transfer function gain, thereby ensuring stability [18]. A high DC gain would cause the thermopile output signals to exit the stable region of the ΣΔ [9].

The presence of an electronic integrator in combination with the 'lossy integrator' in the feedback loop causes oscillations. This happens at the frequency where the phase shift in the loop is a total of 180°, as shown in figure 1.4. The integrator contributes 90°, the other 90° is due to the layout dependent thermal delay; a shorter distance will cause the system to oscillate at a higher frequency. To calculate a wind speed, at least one period of this oscillation is required. Averaging over more periods increases resolution and precision. Figure 1.5 shows an example of a power spectral density of a bitstream, where the energy is at an oscillation frequency of 50 Hz and its harmonics.

1.3. TU DELFT THERMAL WIND SENSOR

The wind sensor designed in this work is an improved version of the thermal wind sensor developed in TU Delft. Over the last several decades, numerous people contributed to the design, starting with the very basic design of A.F.P. Van Putten and S. Middelhoek, in 1974 [12]. The schematic and layout are shown in figure 1.6 and only consisted of four thermistors (resistors with thermo-resistive effect) in a bridge configuration, capable of measuring wind speeds in one direction. It consisted of a 1.5 x 1.5 mm silicon chip, whose thickness was reduced to 50 µm. It was operated in open loop, measuring the voltage change in the bridge due to the resistor changes caused by the airflow. The cooling of the resistors which are normal to the flow, is somewhat larger than that of the resistors which are parallel to the flow. As future work, the authors suggested that the readout electronics could be realized on the same chip.

Two years later, a paper was published by R.W.M. van Riet and J.H. Huijsing, now using a bipolar junction transistor (BJT) based differential temperature sensor in CTD mode, on a 1.5 x 2 mm chip [19]. The experimental setup was capable of measuring wind speeds up to 15 m/s in one direction, but results were "dependent on the aerodynamic properties of the chip and its base." In 1982, the same principle was tested on a 2 x 2 mm chip [20]. The schematic and picture are shown in figure 1.7.

June 1983, about 1½ years later, Van Putten wrote an article on a double bridge architecture on a chip sized 4 x 4 mm [21]. It's a continuation of the work shown in figure 1.6, where now the common mode (fault) signal and the differential flow signal are split up. This was done by using two bridges, of which one was rotated 90° with respect to the other. When using both outputs in a differential fashion, as shown in figure

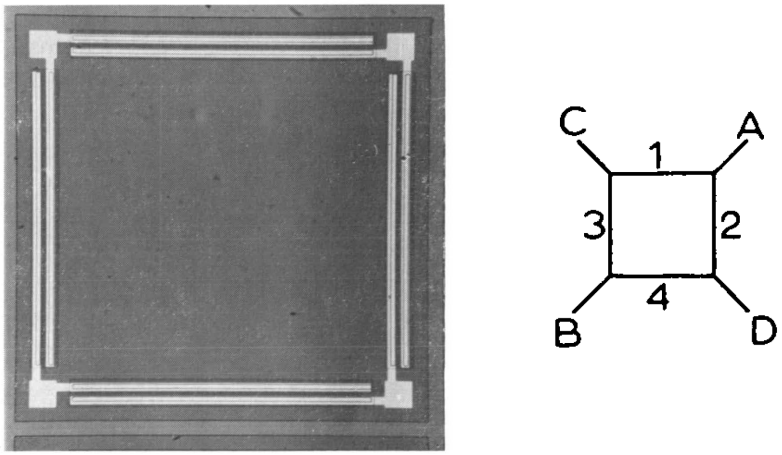


Figure 1.6: Layout and schematic of first TU Delft wind sensor [12].

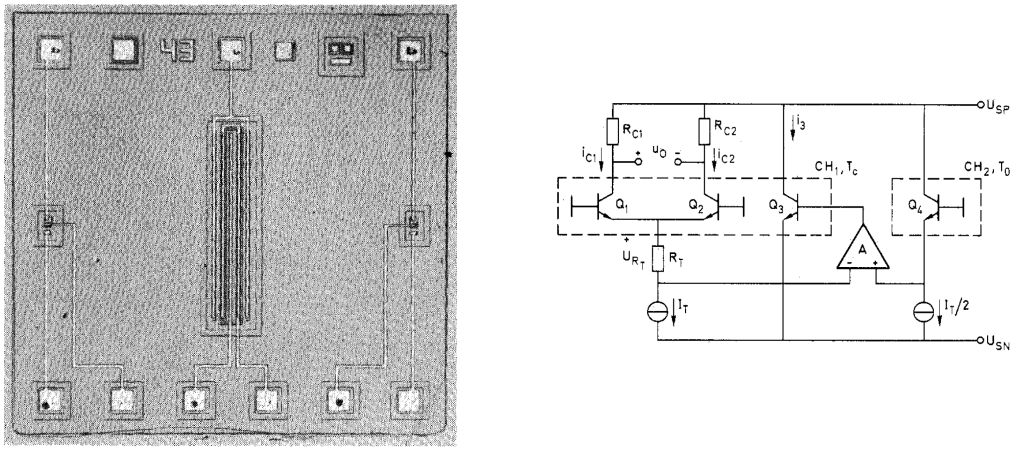


Figure 1.7: Layout and schematic of a BJT based wind sensor [20].

1.8, all errors that effect both bridges the same would cancel out, while wind causes two signals with opposite polarity. The author repeatedly mentioned ambient temperature changes as example. “Compared with the single bridge, a reduced offset level, an increased signal level and improved stability with respect to time and temperature are achieved.”

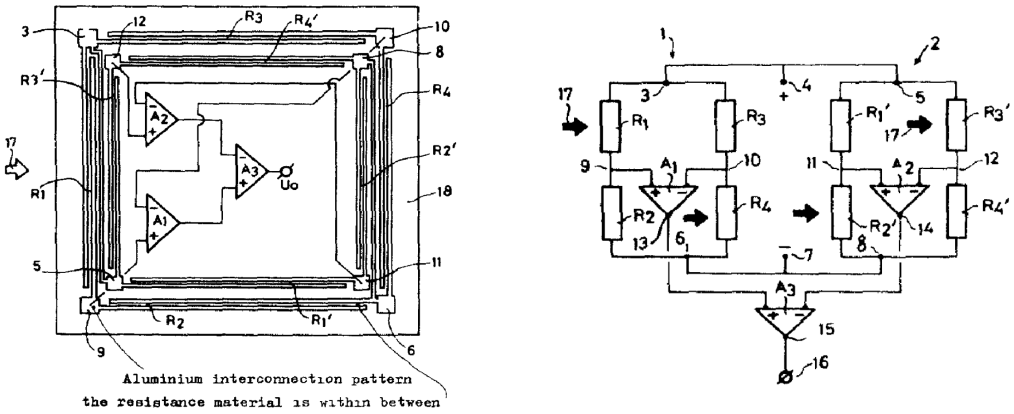
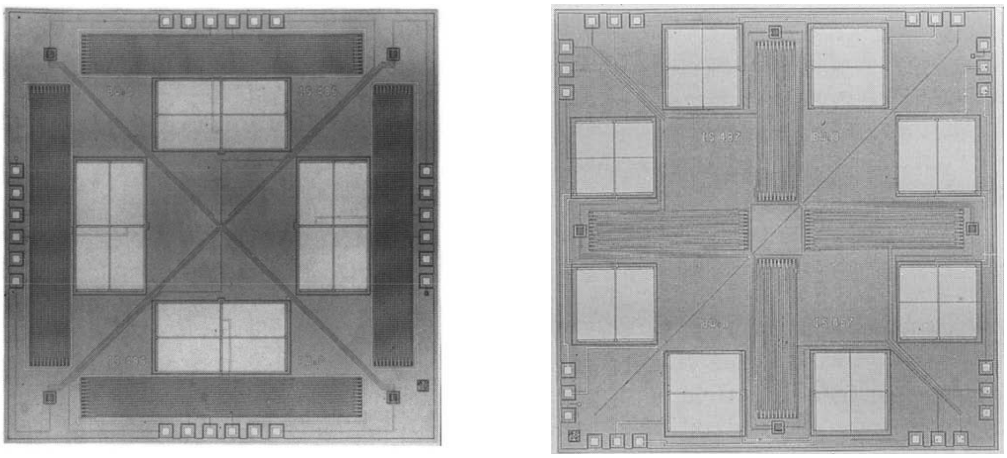


Figure 1.8: Layout and schematic of a double bridge architecture wind sensor[21].

In 1988, B.W. van Oudheusden used thermopiles to determine temperature differences [22]. “The advantage of using a thermopile for the measurement of the on-chip temperature difference is that it needs no zero adjustment, as the previously employed transistor pair did.” It was here where current wind sensor configurations found their origin. Figure 1.9a shows the layout of the 6 x 6 mm sensor chip, where along

the edges, the thermopiles can be identified. The four blocks more to the middle are the heaters, and four transistors are added to sense temperature differences to compare with previous work or to facilitate the CTD mode. Using the CTD mode implies a variable power consumption, depending on the wind speed. Van Oudheusden reported a ±2° angle inaccuracy for 360° of one particular wind speed, "similar to the accuracy of the position angle itself". More results followed in his Ph.D. thesis in 1989, also showing an alternative layout, the crosshair shape, shown in figure 1.9b and an etched flow sensor. Besides that, results regarding laminar and turbulent wind, probe configurations and pitch angles are shown [23]. These were the basis for future (commercial) wind sensor packaging.



(a) The square layout

(b) The crosshair layout

Figure 1.9: Layout of two two-dimensional flow sensors by B.W. van Oudheusden (6 x 6 mm) [22][23].

In 2001, several articles were published on the wind sensor, mainly by K.A.A. Makinwa and J.H. Huijsing [24][25]. Big steps were taken regarding the integration of the circuitry. It was integrated on a 4 x 4 mm chip [26] and ΣΔ modulation techniques were used, resulting in a wind sensor with a maximum speed and direction inaccuracy of ±5% and ±3°, respectively, in the range of 1 - 25 m/s [27]. This was the first chip where the CP mode in place of the CTD mode was employed [28], and similarly the thermal balancing mode in place of the thermal gradient mode, meaning that without external temperature sensor, 600 mW of power was dissipated with a dynamic ratio, all on-chip. In the Ph.D. thesis of K.A.A. Makinwa, published in May 2004, the theory and different architectures (and modes) are discussed [16].

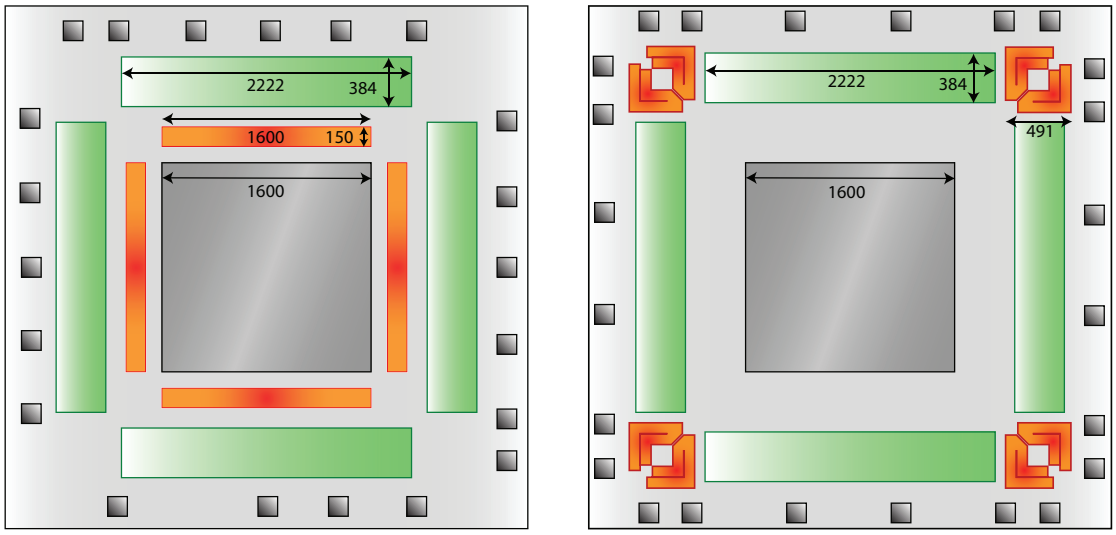
Latest major contributions are the theses of J. Wu [9] and W. Brevet [17]. In the first design, J. Wu brought an electronic integrator in the loop, making it behave like a second order ΣΔ modulator. This was already proven successful in the chip's overheat regulating loop [29], and has now been applied to the thermal balancing mode.

J. Wu also investigated the effect of chopping the integrator over using auto-zeroing. Auto-zeroing has been used to minimize offset and 1/f noise of the amplifiers of the thermopile output signals [30]. Since chopping proved to work better, later designs inherited this.

The oscillation frequency is dependent on the distance between the heater and the corresponding thermopile. Not only the distance, but also the temperature of the silicon influences the speed of the heat pulse [31]. Therefore, the oscillation frequency contains information about the temperature of the substrate. J. Wu exploited this temperature dependence and used the oscillation frequency as temperature sensor. Despite the heaters disturbing the measurement, the wind sensor was capable of measuring temperature with an accuracy within ±1 °C.

The wind sensor consumed 25 mW and was able to measure with a speed and angle accuracy of ±4% and ±2°, respectively, over the range of 1 - 25 m/s. A layout diagram can be found in figure 1.10a.

Following experiments by W. Brevet involved moving the physical location of the heaters, as shown in



(a) Original topology, also used by J. Wu [9].

(b) Modified by W. Brevet [17].

Figure 1.10: Topologies of the TU Delft wind sensor by J. Wu [9] and W. Brevet [17]. Sizes in µm.

figure 1.10b. By moving the heating resistors closer to the point of measuring, i.e., the ends of a thermopile, the sensor's performance was expected to improve. Since the physical thermal path was shorter, the system responded faster and was less prone to process and packaging artifacts. Measurements showed that the performance had not improved, which might indicate erroneous reasoning. Power consumption did not change, but maximum speed and angle errors increased to ±6% and ±6°, respectively, after reducing te range to 4 - 25 m/s.

Moving heaters to the borders of the chip increases the range of the system, since the differential power dissipated by the heaters increases. W. Brevet implemented the Return To Heat (RTH) function, to increase the range of the averaged output. Ideally, the specified maximum wind speed would cause the output to be (near) maximum as well. The RTH feature turns on all heaters, half the time of Fs, resulting in more common mode and less differential power distribution. As a direct consequence, the system needs a bigger power ratio to balance the temperature gradient and utilizes therefore more of its dynamic range.

Another implication of the change in heater position, is the oscillation frequency of the system. A higher oscillation frequency also means a shorter minimum conversion time and reduced averaging error due to averaging over a non-round number of periods. Therefore, this design uses a simpler decimation (averaging) scheme.

1.4. AIMED IMPROVEMENTS

This work aims to improve the design of the wind sensor and to address unanswered questions from the previous iterations. The signal swing on the integrators was an unknown design parameter. Earlier studies failed to accurately measure the signals at the integrator outputs. This design aims for an increase in signal swing at the integrator outputs to ensure minimal performance degradation due to noise sources in this stage. Hence, test outputs were included to allow the amplitude of these signals to be accurately measured. This way, later designs can be further improved and tuned towards an optimal signal swing.

The techniques of auto-zeroing and chopping for the integrator improved the accuracy of the wind sensor and allowed the heater power dissipation to be drastically reduced, from 600mW to 25mW. This indicates that offset and 1/f noise are significant sources of error. Although chopping the integrator reduces the effect of these error sources, it introduces residual ripple that can negatively affect operation by drowning small signals and reducing resolution. Either reduction of the ripple or enhancement of the signal swing is desired.

The heaters will be placed back alongside the thermopiles, like in the design of J. Wu. This will bring back

the oscillation frequency to lower values and the environment is more likely to be uniform. Non-uniformity at the corners can be caused by discontinuity in glue at the bottom and sides of the silicon chip. Larger heater area's also implies better matching.

Furthermore, as W. Brevet suggests, four extra heaters can be added to generate the temperature gradient that is normally caused by the wind. If found to be effective, manual calibration work in a wind tunnel can be replaced by measurements outside a wind tunnel. Figure 1.11 shows the desired layout with the extra heaters, main heaters and thermopiles in yellow, red and green, respectively.

Besides, a reduction in power consumption is required to improve the state-of-the-art. Lowering it below 25mW is desirable, but this is not a hard requirement in this design.

In the design of W. Brevet, many choices regarding layout have been made trying to boost the performance of the temperature sensor. Mainly the spread in component parameters were carefully evaluated to be guaranteed of the right operation. Despite the effort to increase the precision of the temperature sensor, the maximum error increased to ±1.3 °C. This work will not focus on the temperature sensor.

Performance in terms of inaccuracy and maximum angle error is key. For a state-of-the-art wind sensor, the design goals are a maximum wind speed error of 2% and a maximum angle error of 2° over a range from 1 - 25 m/s.

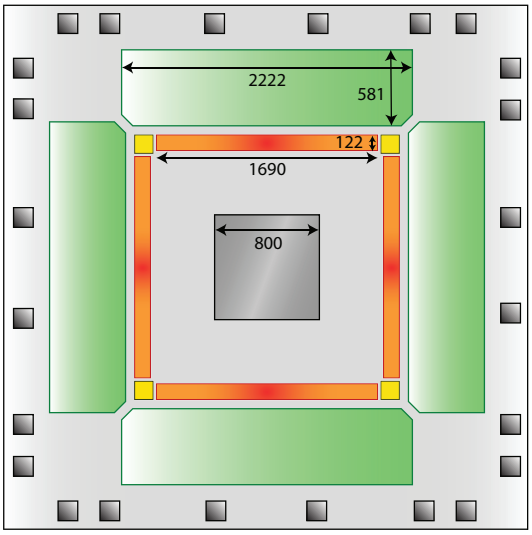


Figure 1.11: Topology used in this work. Sizes in µm.

1.5. THESIS ORGANIZATION

This chapter has provided a review of common wind sensor architectures, explained the working principles of the thermal wind sensor and the history of the TU Delft wind sensor. Chapter 2 will give an in depth view of the design of the individual system blocks, followed by the measurements in chapters 3 and 4. Concluding remarks and recommendations are given in chapters 5 and 6.

2

DESIGN PROCESS

Following sections will discuss each of the components from figure 2.1.

2.1. THERMOPILES

The thermopiles are the most essential blocks in the sensor. They convert the temperature gradient to an electrical signal to be further processed by the loop. To realize a differential signal, two thermopiles on opposite sides of the sensor are connected in series, and their common terminal is grounded to realize a 0V common mode level, as shown in figure 2.1. Each thermopile has been built from 24 in series connected thermocouples, also referred to as 'arms', with a total length of 2222 µm and width of 581 µm to increase the voltage output. (Figure 2.1 shows only two arms for each thermopile for the sake of simplicity.) Figure 2.2 shows how each thermopile is built, by stacking the Seebeck effect of the p^+ diffusion. This material has a Seebeck coefficient S of 300 - 1000 µV/K, the return path aluminum contributes -1.7 µV/K (both at 27 °C) [32]. Metal 2 (M2) shielding achieves protection from electromagnetic influences, for example, the off-chip transceiver electronics.

The thermopiles are made bigger, 1½ times the area of previous designs, to increase SNR. As shown below, the SNR of a thermopile is proportional to the area of the thermopile, not the number of arms.

If n in series connected thermocouples form a thermopile of length l and width w, the total length of the path has a resistance R_{tp} equal to

$$R_{tp} = R_{\square} \frac{n * l}{w} \tag{2.1}$$

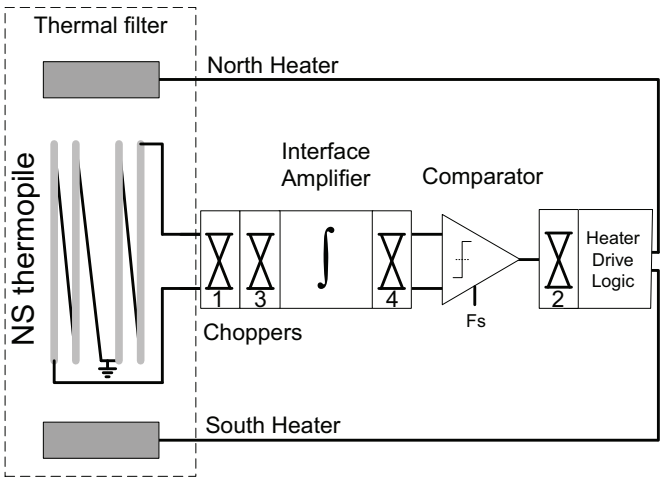


Figure 2.1: A schematic overview of the wind sensor chip.

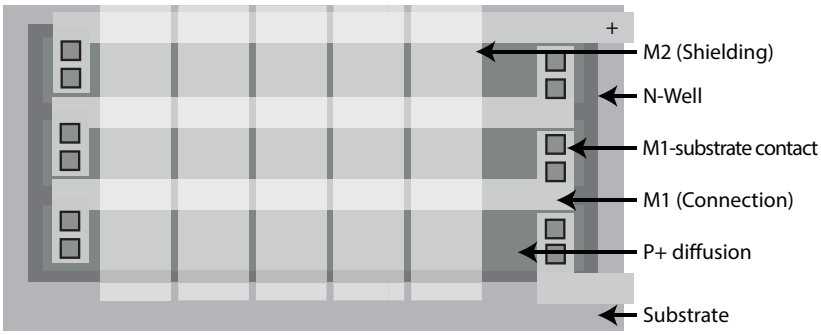


Figure 2.2: The layout of the thermopiles in the substrate [17].

where $R_\square$ is the sheet resistance. The noise power P_n is proportional to the resistance and can be written as

$$P_n = 4k_B T R_{tp} \Delta f \tag{2.2}$$

where k_B is the Boltzmann constant and T is the temperature in Kelvin. The signal power can be written as

$$P_{sig} = (\Delta T * n * S)^2 \tag{2.3}$$

with sensitivity S and where temperature difference ΔT can be replaced with $l * \delta T$, since temperature gradient times the length results in the temperature difference over the thermopile. Dividing the signal power by the noise power results in

$$\text{SNR} = \frac{P_{sig}}{P_n} \tag{2.4}$$

$$= \frac{(l * \delta T * n * S)^2}{4k_B * T * \Delta f * \left(R_\square \frac{n*l}{w}\right)} \tag{2.5}$$

$$= \frac{(\delta T * S)^2}{4k_B * \Delta f * R_\square} * (l * n * w) \tag{2.6}$$

$$\propto W * l \tag{2.7}$$

where total thermopile width W replaces $n * w$ (neglecting isolation borders. Besides, the low ohmic return paths have been neglected in the calculations.) The number of arms in a constant area influences the signal and noise levels, but not their ratio. Since thermopile design influences the signal amplitude, this is discussed in section 2.2.1.

2.2. INTEGRATOR

The integrator consists of a transconductance amplifier and an integration capacitor. The schematic of the amplifier can be found in figure 2.3, a folded cascode topology, to maximize output swing, with choppers at the input and at the PMOS and NMOS current sources. The input pair of the amplifier is made of PMOS transistors. Using PMOS input transistors enables 0V common-mode input and a high input impedance. To minimize mismatch, a cross-coupled layout has been used. Common mode feedback is implemented by transistors M11 and M12, biased in their linear resistive region and connected at their drains. Their summed dimensions are equal to M6, and with equally biased current sources in the different branches, this results in an output common mode voltage of Vcm [9].

Offset in the integrator has a negative effect on the system performance. The input referred offset of the integrator is indistinguishable from the voltage signals coming from the thermopiles, and causes the loop to react by creating an undesired temperature differential on the chip. Therefore, chopping is utilized to reduce the offset of the transconductance stage from 4 mV to about 30 µV. Besides the integrator choppers, also a system level chopper is used, to reduce any residual offset coming from non-idealities in the chopper switches. These are choppers 1 and 2 from figure 2.1, one of which is incorporated in the control logic.

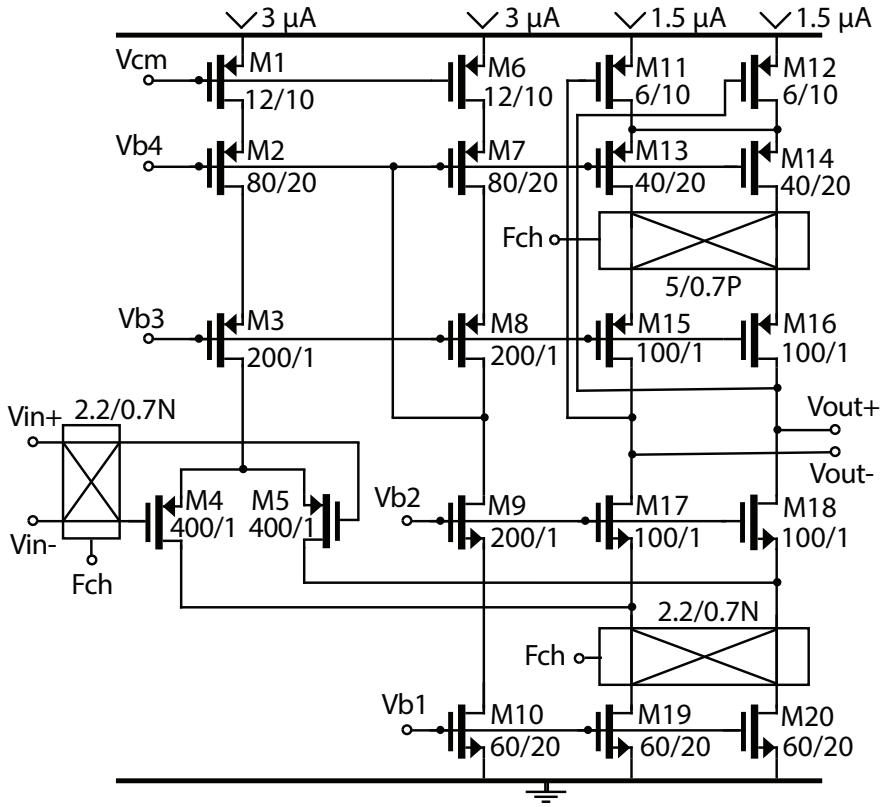


Figure 2.3: The folded cascode integrator used.

J. Wu implemented timing to reduce resolution loss due to ripple, a chopping artifact [9]. The diagram of the signal timing can be observed in figure 2.4. The sampling clock Fs was brought out phase with respect to the chopping clock Fch that controls choppers 3 and 4. The sampling now happens halfway every falling ripple slope (indicated with the x), thereby preventing ripple influence.

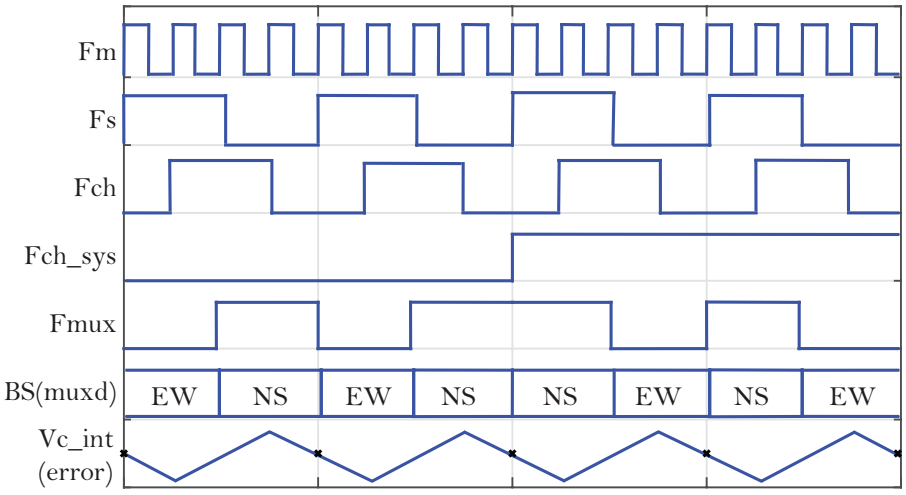


Figure 2.4: Timing diagram

The design of the integrator has not been modified, since it was proven to work by Brevet's and Wu's work. Offset of the integrator before and after chopping was verified to be 4 mV and 30 uV respectively, using a Monte Carlo simulation. Simulation results are shown in figure 2.5.

The layout was completely redone, making the whole integrator more compact than before. Besides, all

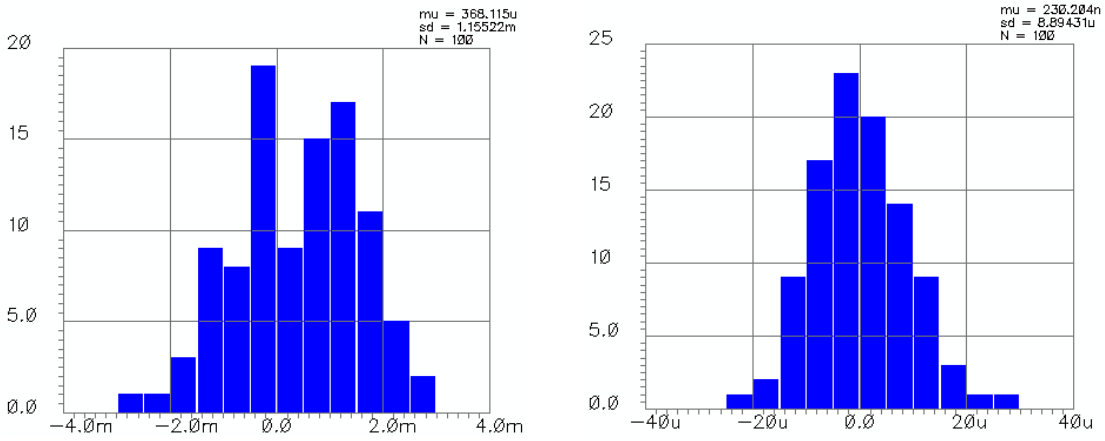
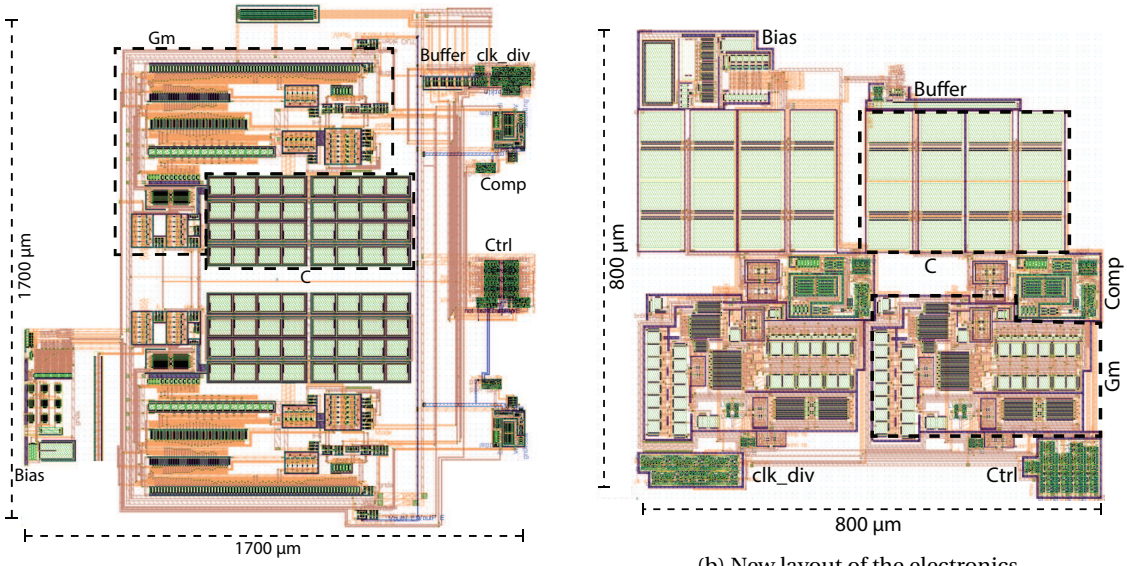


Figure 2.5: Monte Carlo simulation results: Before and after chopping.

redundant circuitry (from previous designs) is removed. The layout used by W. Brevet and the new layout are shown in figure 2.6. Instead of creating a long row of same-sized transistors, the new layout has the transistors placed with required dimensions, closest to the signal path, thereby preventing the signal from traveling long distances. Integration capacitor sizes are reduced and different blocks placed close together.



(a) Layout of the electronics from W. brevet [17].

(b) New layout of the electronics.

Figure 2.6: Integration capacitor signal swing and ripple.

2.2.1. IMPROVING SIGNAL SWING

As explained in section 1.4, a greater signal swing at the output of the Gm-C integrator is desired. Boosting the signal across the integration capacitor can be done in three ways: increasing the original signal entering the amplifier, boosting the gain of the amplifier or reducing the size of the integration capacitor. Since the amplifier's design was already proven, it was not modified. The other two options are both applied.

Boosting the signal entering the integrator can be done in several ways: increasing the excitation signal by spending more power in the heaters or by increasing the total length of the thermocouples. Since another goal is to reduce power consumption, only the second option is implemented. In the previous designs, thermopile area was kept the same for the sake of comparison. This was no longer necessary, and therefore the total thermopile area was increased by approximately 50% to a total width of 581 µm. The length is kept constant

on a value of 2.22 mm. According equation 2.7, this will improve the SNR of the thermopile by 1.5 times, equivalent to 1.8 dB. Besides area, the thermocouple width (arm width) is also changed. By using smaller, and thus, more arms, the thermopile produces a stronger signal (and proportionally more noise). Instead of 12, a total of 24 arms are now implemented per thermopile. As a result, the resistance of each thermopile increased from 86 kΩ to 220 kΩ. Figure 2.7 shows the post-layout simulated impedance and phase shift of the previous and new thermopile over frequency.

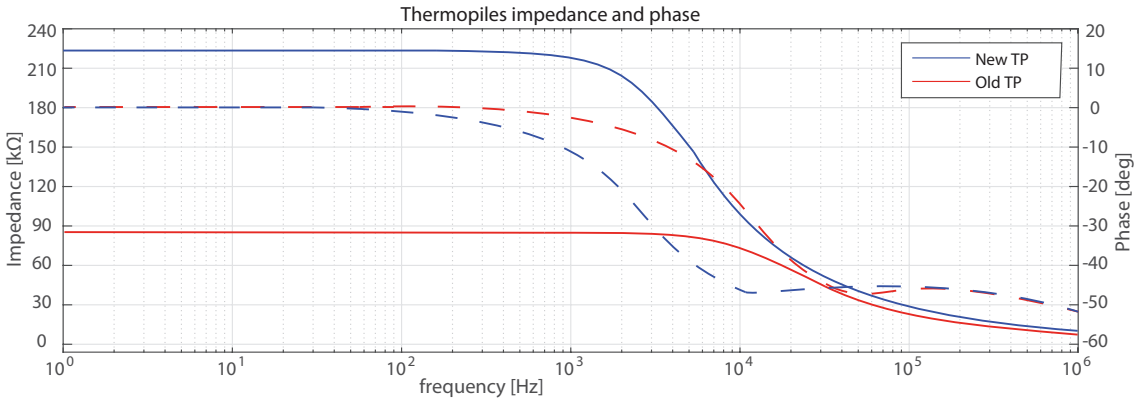


Figure 2.7: Thermopile impedance of previous and new design.

Reducing the size of the integration capacitors has a practical limit. The amplitude of the signal needs to stay well within the linear range of the integrator. According to $V_o = V_i * G_m/sC$, the output voltage will double when the integration capacitors size is halved. However, there is another limit to reducing its size. Since the oscillation frequency can be as low as 30 Hz [9], a linear transfer function of the integrator around that frequency needs to be ensured. Obeying a rule of thumb, this is done by placing the f_{-3dB} not higher than 1/10th of the signal frequency, i.e., below 3 Hz. A (post layout) AC simulation can be found in figure 2.8, showing the f_{-3dB} at 2.5 Hz after reducing the capacitor value from 130 pF to 65 pF.

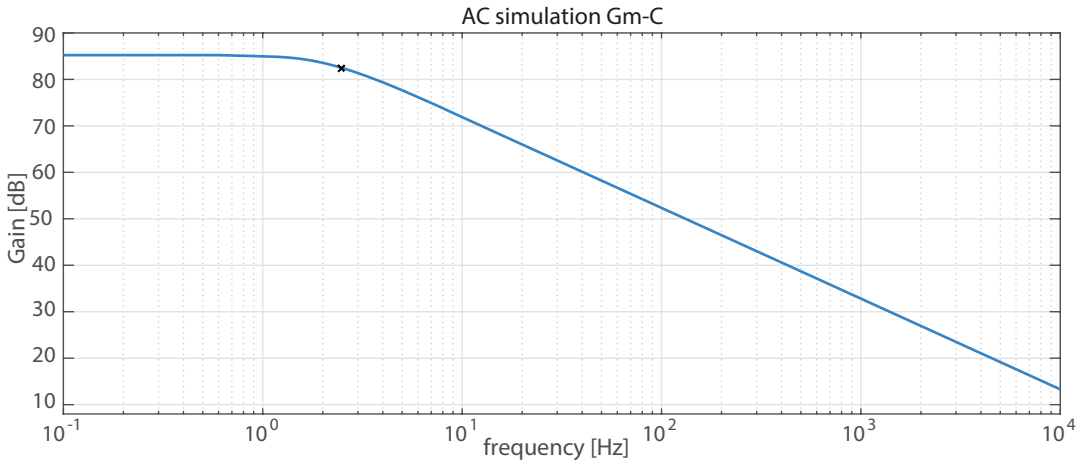
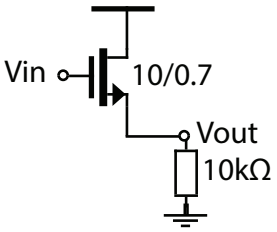


Figure 2.8: An AC simulation of the Gm-C integrator.

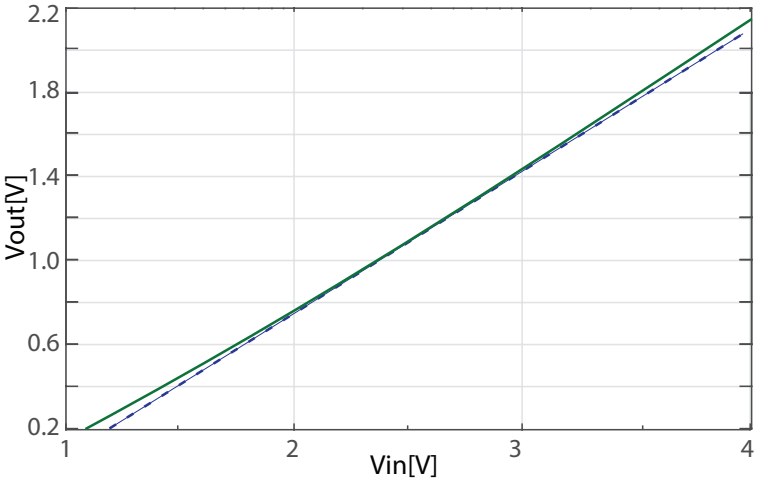
2.2.2. MEASURING SIGNAL SWING

In the previous section, steps were taken to boost the signal swing on the integration capacitors. These signals were still of unknown amplitude, and therefore, circuitry to be able to observe these nodes was implemented. Because resistive loading of the transconductance stage is not desired, MOSFETs are used in source follower configuration, with their sources connected to the pad. They need to be connected to ground with an external 10kΩ resistor in the measurement setup, as shown in figure 2.9a. Based on the simulation shown in figure 2.9b, the integration capacitor voltage V_{in} can be approximated from the measured voltage V_{out} by the linearized relation $V_{in} = V_{out} * 1.4 + 0.97$ for V_{out} around 1. The relation becomes more intuitive when written

as $V_{out} = V_{in} * 0.7 - 0.7$ for V_{in} around 2½ (Vcm), meaning that the output follows the input with an offset of -0.7 and a gain of 0.7.



(a) Circuit diagram of the source follower.



(b) Transfer of the source follower.

Figure 2.9: Source follower used to buffer integration capacitor signals to output pads.

2.3. COMPARATOR

In figure 2.10, the schematic of the comparator is shown. The comparator has a preamplifier with a gain of 60dB [9], that drives a latch, which is reset by $\overline{Fs}$ after each decision by M1. It is followed by a common source gain stage for level recovery followed by an SR latch.

The comparator is the same as the one designed by J. Wu [9]. It was not modified or replaced. A flaw in the layout of the comparator, a clock line mismatch, causes the decision level of comparator to be around 3mV of input voltage. When this offset level is moved to the input of the integrator, it's differentiated (going backward through the integrator) and becomes zero. Therefore, it ideally has no influence on the performance. However, as soon as system level chopping is applied, the offset across the integration capacitor is flipped, causing a dead time until the 3mV offset is restored, as shown in figure 2.11. Note that in this figure the offset of the integrator is assumed to be zero (no ripple).

Figure 2.12 shows the layout of the comparator, at the point where the clock line $\overline{Fs}$ (shown in red) crosses and follows one of the signal paths to the drains and gates of the cross-coupled transistors, which are the most

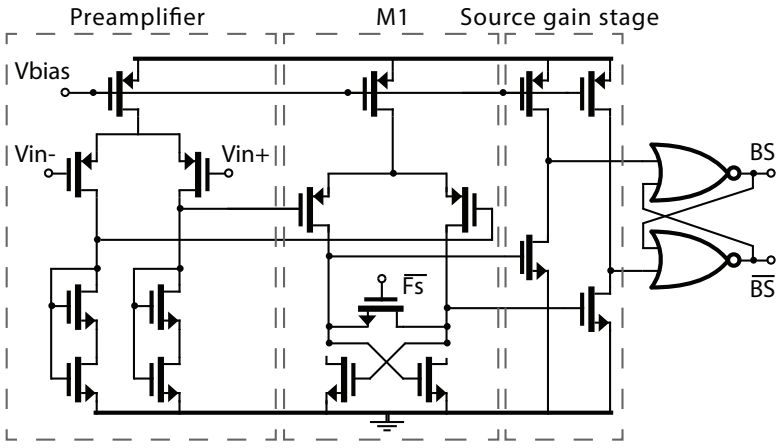


Figure 2.10: A schematic view of the used comparator.

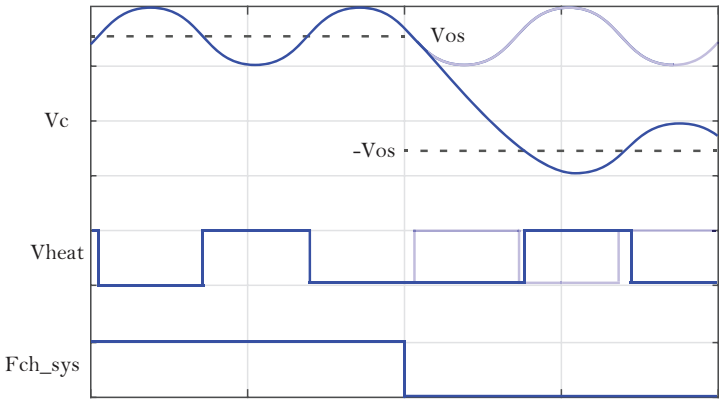


Figure 2.11: The integration capacitor voltage settles to the negative offset value.

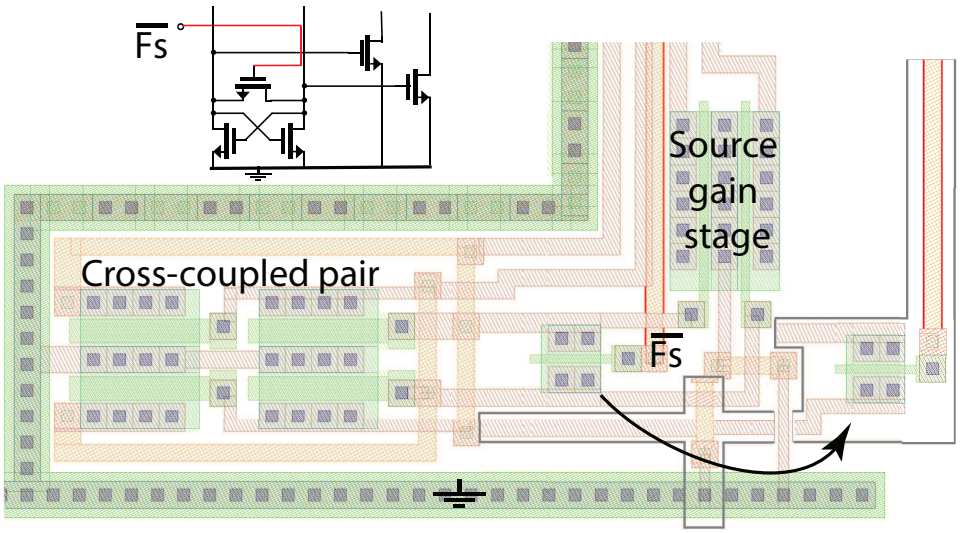


Figure 2.12: The comparator clock line layout error and a suggested solution.

sensitive nodes. Clock injection is causing offset in the decision level of the comparator. This can be easily prevented by moving the clocked transistor such that the gate can be accessed without crossing any lines, as shown in the gray box.

2.4. LOGIC

The schematic for the digital logic is shown in figure 2.13. It generates the timing for the signals to be captured by the digital logic and provides the control signals for system level chopping, Return-To-Heat mode capabilities and polarity change. In the RTH mode, all heaters are activated for a certain period of the cycle to achieve common mode heating. The polarity mode introduce a -1 in the loop. This is a safety measure to prevent a failure due to inconsistent reasoning of the signs of signals outputted by the thermopiles as function of temperature. If the system does not work, the signal 'pol', also controllable from outside, can be set to high (5 V). All control signals are pulled down with large resistors to ground, so that they can be left disconnected if their values are not required to be changed during operation.

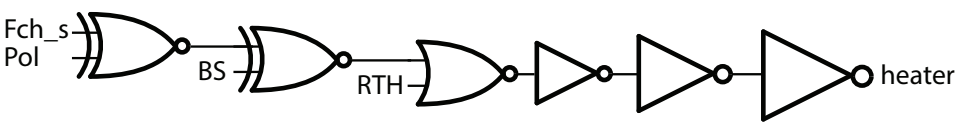


Figure 2.13: A schematic overview of the wind sensor heater driver logic.

2.5. HEATERS

The power dissipated on the heaters can be varied by regulating the voltage across them or by changing the resistor value. The voltage can be regulated during operation, but the resistor value needs to be selected during design. The maximum power consumption is kept at 25 mW per resistor, so the heater is made 1 kΩ. The heaters are n^+ diffusion resistors driven by a NMOS transistor connected to a separate power supply. When the NMOS transistors are driven high, current flows through them, and they each dissipate 0.14 mW of power as heat.

2.6. TEST HEATERS

Four extra heaters are positioned in the spaces between the regular heaters (yellow in figure 1.11). These heaters are connected to bond pads so they can be controlled from off chip. The main goal of these heaters is to emulate the wind such that information about offset, gain error and non-linearity can be obtained without performing wind tunnel measurements. During measurements, the test heaters are used to cancel offset by heating the sensor such that a balanced situation exists, in terms of power distribution of the ΣΔ loop. A way of viewing it, is to say that the test heaters account for asymmetric heat leakage. 2.5 kΩ resistors are used, so only a maximum of 10 mW per test heater can be consumed, sufficient for its purpose. The test heaters are realized in n^+ diffusion, just like the main heaters.

2.7. MATCHING

A key element in this design is symmetry. Any heat generated by the heaters needs to be transported across the chip uniformly, and also, the heat transfer to the ceramic disc the die is mounted on, should be symmetric. Any variation will generate an offset. Matching is only possible by careful layout design and also with attention to packaging.

Matching in the chip is done by making each side (or quadrant) as symmetrical as possible, and copying it to the other sides. All pads, thermopiles and heaters are placed with a four-quandrant symmetry to the center of the die. The control logic is in the center of the chip. The amount of wires bonded to each side is kept limited and the same in number, to balance and limit heat leakage. Also, shielding is used on clock lines and thermopiles, to prevent coupling from or to nearby signal lines.

All layout circuitry is placed rather compact to leave enough room for the thermopiles. The circuitry is placed in the exact center for the sake of symmetry. The leftover space was filled with decoupling capacitors, over 1000 pF all together. This stabilizes the supply voltage for the heaters and the circuitry, assisted by the off chip capacitors.

3

DESKTOP MEASUREMENTS

The fabricated wind sensor chip has been packaged in two different packages: a Dual In-line ceramic Package (DIP) and a custom-made Wind Sensor Package (WSP). The DIP is used to validate the functionality of the chip with desktop measurements. The WSP is used to measure the performance in a wind tunnel, and will be discussed in chapter 4. The DIP has all 17 sensor pads connected to I/O pins. This includes connections for testing and calibrating the sensor. The pin-out table of the package can be found in appendix A.

3.1. SETUP

A graphic representation of the setup can be found in figure 3.1. LabVIEW is used for the data acquisition, combined with the NI USB-6259 data acquisition board. The DIP chips are placed on a custom-made Printed Circuit Boards (PCB) for characterization. The PCB connects the digital input and outputs of the wind sensor to the DAQ, and also buffers analog signals for integrator signal swing characterization. Besides that, shunt resistors are added to measure the matching of the heaters (see section 2.7). The schematic of the PCB can be found in appendix B.

3.2. OPTIMAL SAMPLING FREQUENCY AND POWER DISSIPATION

The quality of the output signal can be quantified by analyzing the output bitstream of the wind sensor in the frequency domain. In these measurements, the wind sensor output is observed without the input signal (the wind) present. However, packaging imperfections such as the varying thickness of the glue cause inherent thermal imbalance on the chip when common mode heat is applied. Figure 3.2 shows the frequency domain

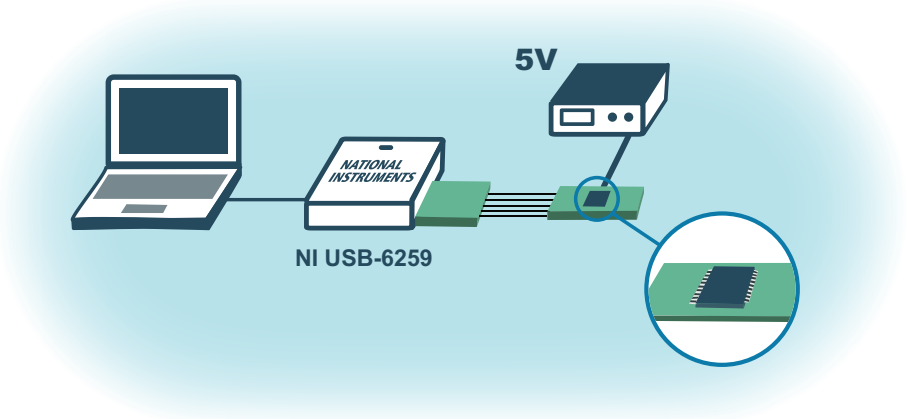


Figure 3.1: A schematic representation of the DIP test setup.

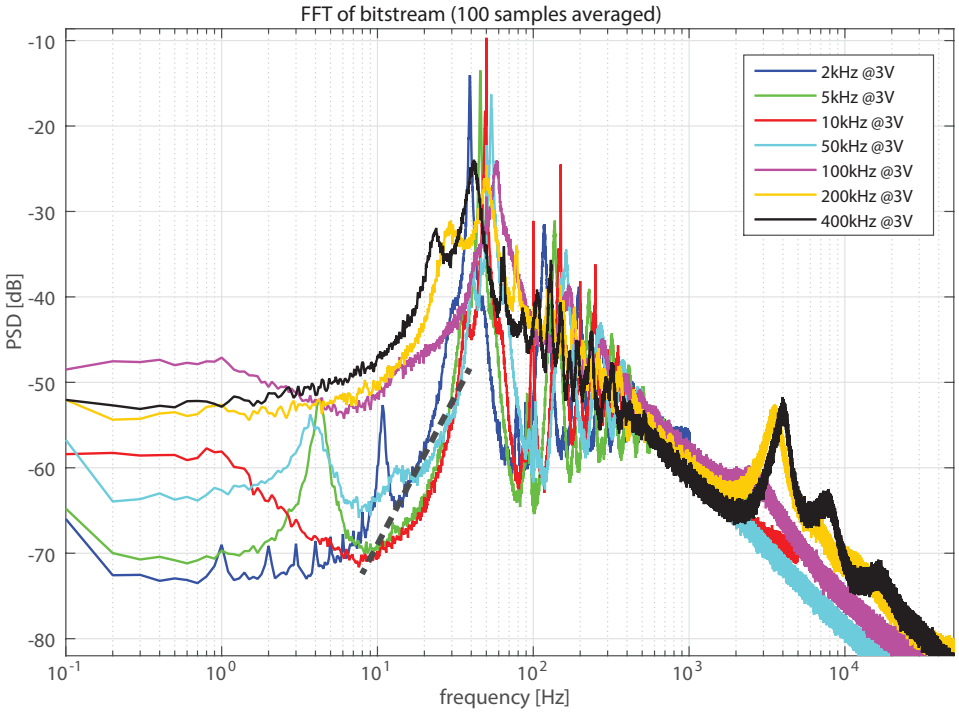


Figure 3.2: An fft over different modulation frequencies Fs.

output of the wind sensor for different clock frequencies. Second order noise shaping, which is expected due to the ΣΔ behavior is observed between 8 Hz and 40 Hz, after which the power spectrum spikes. At that frequency the system oscillates, with the mechanism described in section 1.2.2. It is clear that the system behaves the best between sampling frequencies of 5 kHz and 50 kHz.

For wind speed measurements, frequencies up to 1 Hz are of interest. In this frequency range, the fft of the bitstream should show nothing but quantization noise. Besides a high Signal to Quantization and Noise Ratio (SQNR) in the low frequency area, a well-defined oscillation frequency is also desired. This indicates stable operation and the presence of a well defined thermal delay between the thermopiles and the heaters. Based on these two criteria, a clock frequency of 5 kHz and a heater power of 27 mW are selected as settings.

3.3. SIGNAL SWING MEASUREMENTS

In figure 3.4, the voltage across the integration capacitor is shown, when the wind sensor is operated with 27 mW power consumption and 5 kHz sampling clock frequency. The signal has a common mode voltage of 2.5 V to ensure the largest headroom for signal swing. The differential swing is measured to be about 200 mV; far smaller than the 7 V it can handle. Figure 3.4 also shows the zoomed in time version of the integration capacitor voltage. Ripples at a frequency *Fch*, are observed, as artifacts of the chopped transconductor. The slope of the triangular ripple is measured to be 140 V/s. This corresponds to an input referred offset of 0.5 mV, which is well within the simulated maximum of 4 mV, as shown in section 2.2. The ripple amplitude is inversely proportional to the chopping frequency. Lower frequencies cause a larger ripple amplitude. As long as the ripple is small enough not to drive the transconductance into a nonlinear regime, the timing described in section 1.3 will mitigate any negative effects.

3.4. HEATER AND TEST HEATER MATCHING

The main heaters are rated at 1 kΩ and operated using a CMOS transistor as a switch. When RTH mode is off, two of the heaters are activated and connected to the power supply at all times. This complicates attempts to measure the heater resistance by looking that the heater supply current. The test heaters however, are connected to a common ground, but each has its own power connection pad. Since the test heaters are smaller, further apart and placed in the same process layer, their matching can be used as a an indicator for

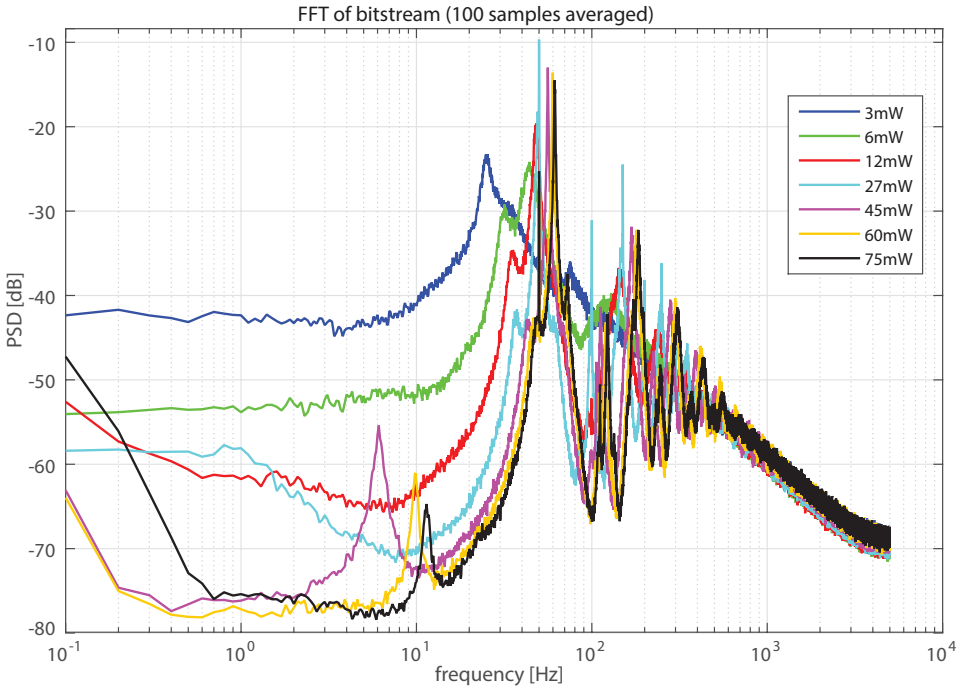


Figure 3.3: An fft over different power consumptions.

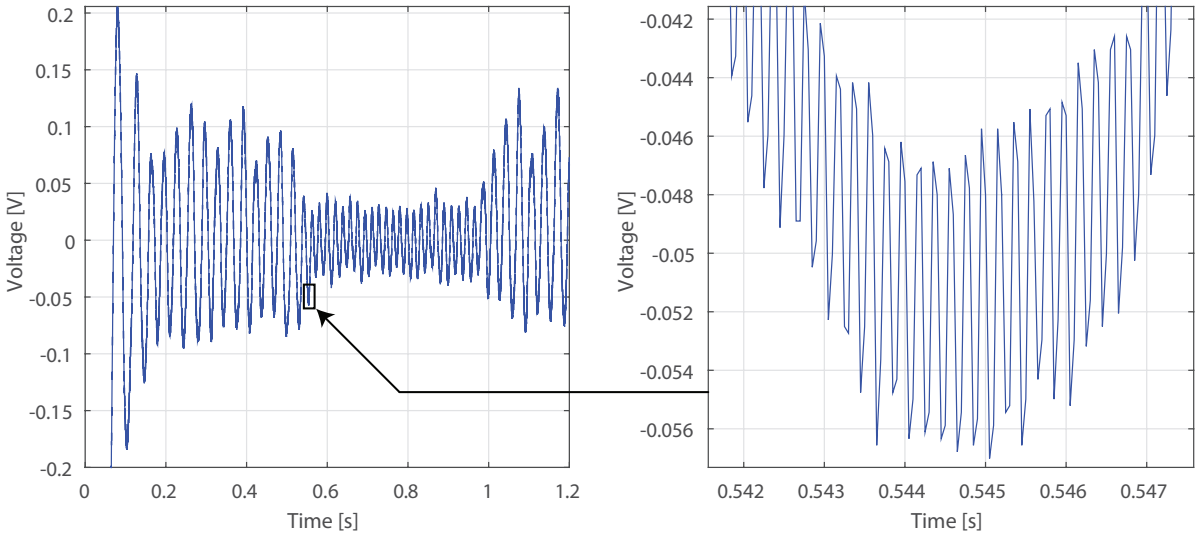


Figure 3.4: Integration capacitor signal swing and ripple.

the matching of the main heaters. The mismatch of the test heaters on a single chip was measured, and shows a maximum mismatch of 0.002%, which is negligible.

3.5. LOW POWER OPERATION

As shown in figure 3.3, the system still shows oscillatory behavior when a heater power of 3 mW is used. In this case, although the oscillation frequency is halved, the system is still operational. However, while the system's performance suffers drastically from the reduced excitation signal, the bitstream average remains in the same range. The sensor needs the same time to thermally re-balance the chip, because in the low power situation, less energy is lost.

3.6. LINEARITY

The bitstream average contains information about the wind speed. The relation is based on King's law, shown in relation 3.1. King's law describes the situation of a heated surface. The overheat, ΔT, is linear proportional to the total consumed power P. The wind speed U, however, has system dependent coefficients G and H to relate it to the power needed to keep an overheat temperature.

$$P = \left(G + H\sqrt{|U|}\right)\Delta T \tag{3.1}$$

$$\frac{\delta P}{P} = \frac{\sqrt{U}}{A + B\sqrt{U}} \tag{3.2}$$

In the constant power mode, a constant overheat temperature is not maintained. The relation needs to be modified to equation 3.2, where $\frac{\delta P}{P}$ is the power ratio needed to correct the gradient caused by the wind in one direction and where A and B are constants, dependent on dimensions and material properties [16].

For a wind direction, both perpendicular wind speeds can be calculated. Combining the two resulting vectors will result in a third vector with the total wind speed (in that 2D plane) and the direction of that wind. Alternatively, using equation 3.3 and 3.4 can be used to solve the wind angle. In two directions, two relations hold two unknown values, and therefore can be solved.

$$\delta P_{NS} = \frac{P\sqrt{U}}{A_{NS} + B_{NS}\sqrt{U}} * \cos(\theta) \tag{3.3}$$

$$\delta P_{EW} = \frac{P\sqrt{U}}{A_{EW} + B_{EW}\sqrt{U}} * \sin(\theta) \tag{3.4}$$

To investigate calibration through the use of test heaters, a sample is put upside down on a flat surface. Every test heater is swept from 0 to 2.4 V, consuming a maximum of 2.3 mW. The result of this measurement is shown in figure 3.5. (Note that some bitstream averages are multiplied by -1 to match their sign.) Unfortunately, the absence of wind causes a stronger memory effect, visible at the complete left, where every line should start at the same position. Some lines are slightly non-parallel, meaning a gain error. More testing to accurately detect this difference could be one of the first steps towards calibration without the use of a wind tunnel.

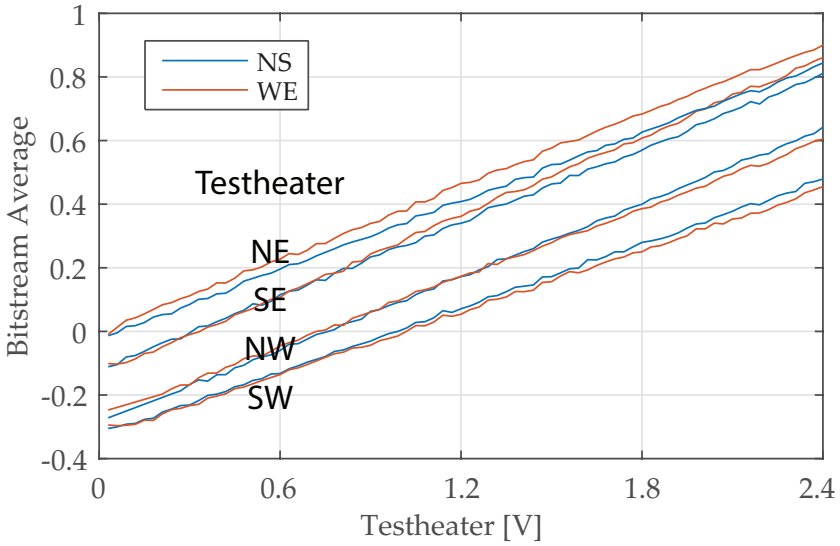


Figure 3.5: Sweeps of every test heater.

4

WIND TUNNEL MEASUREMENTS

4.1. SETUP

Packaging is done by a professional third party. A picture of the packaged wind sensor can be found in figure 4.1. The same package as the previous versions of the thermal wind sensor was utilized to characterize the wind sensor in a wind tunnel, to achieve a fair comparison with the previous generations. The disk in the center is made of aluminum. The center of the disk is hollow and is finished with a small layer of ceramic material. Underneath, the wind sensor chip is glued with thermally conductive glue. The whole packaging process requires a lot of repeatability and precision. For example, any mismatch in glue thickness or surface smoothness, can influence the the final accuracy of the sensor. To reduce heat loss through bond wires, 5 I/O signals are not bonded.

Figure 4.2 gives an impression of the complete setup used. Wind speeds in the tunnel were set by tuning the power source of a fan and checking the reference sensor, angles were entered digitally after which a motor rotates the sensor within the wind tunnel. LabVIEW is used for the data acquisition, combined with the NI USB-6259 DAQ.

Two custom-made PCBs are used to send and receive digital data over two long CAT 5 cables with differential signaling, to facilitate operation over a long distance outside the wind tunnel chamber, an operator friendly environment. An LDO regulator is used to ensure a constant power supply for the wind sensor. A programmable DAC has been used to realize a variable power source for each test heater and the main heaters. The RTH mode can be toggled using a switch. Schematics of the PCBs can be found in appendix B.

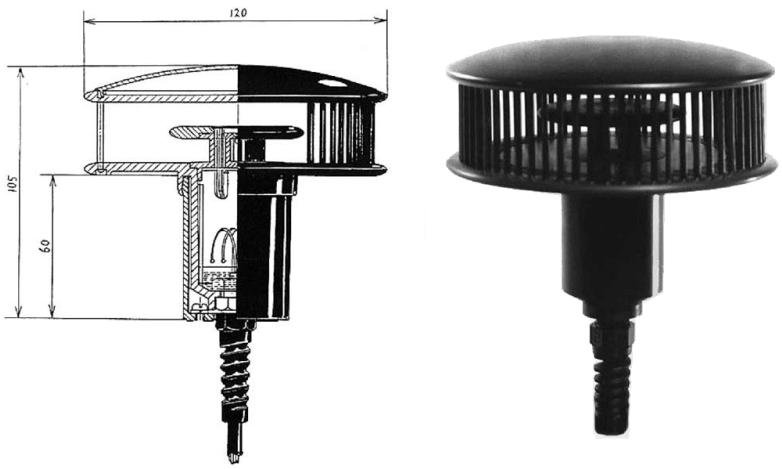


Figure 4.1: The wind sensor package (WSP) [33]

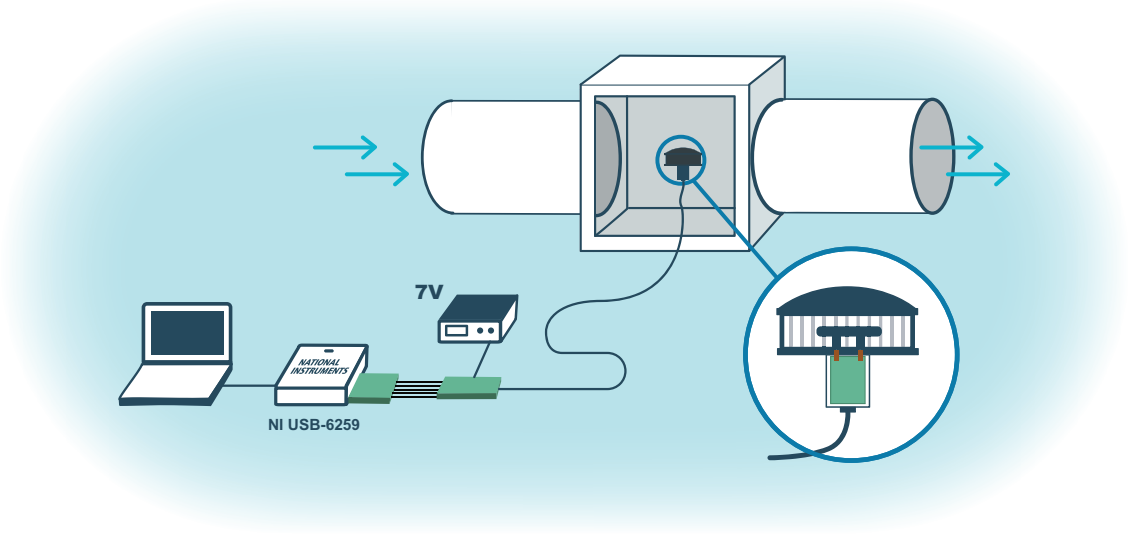


Figure 4.2: Test setup with WSP in wind tunnel.

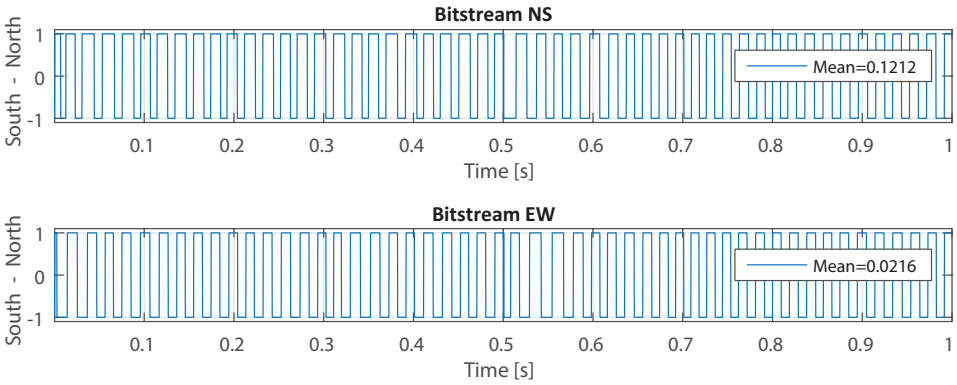


Figure 4.3: Bitstream of p3 at 1 m/s.

Several samples were prepared for wind tunnel measurements. Due to the precision required in the packaging steps and fragile components, only two survived the packaging process. They are referred to as p2 and p3. The results mentioned, are from sample p3, which performed best. P2 has similar results, but a single measurement point was off repeatedly.

4.2. WIND SENSOR DATA

After doing a series of 25 measurements of 1 second per wind speed and angle, the last 10 measurements are selected for processing. 5 wind speeds and 12 different angles are measured. A total of 600 data samples are processed by MATLAB. One sample contains the bitstreams of both directions and is split up and saved. One of the saved samples is shown in figure 4.3. In this measurement, the wind sensor measures a set wind of 1 m/s in the North - South direction. The bitstream average in that direction is 0.12, which means a wind has been detected. The East - West direction has an average near zero. The combination of these two numbers can be used to derive the measured angle of the wind.

4.3. FIT ADJUSTMENTS

Equation 3.3 and 3.4 are the starting points for the fit, to relate the bitstream to the wind speed. To account for offset and rotational errors, terms $D\sqrt{U}$, E and δ were added, forming equation 4.1. Since the four test heaters are now used to cancel offsets in this work, the offset terms become redundant. Only the last, E, is kept for accounting for any residual offset.

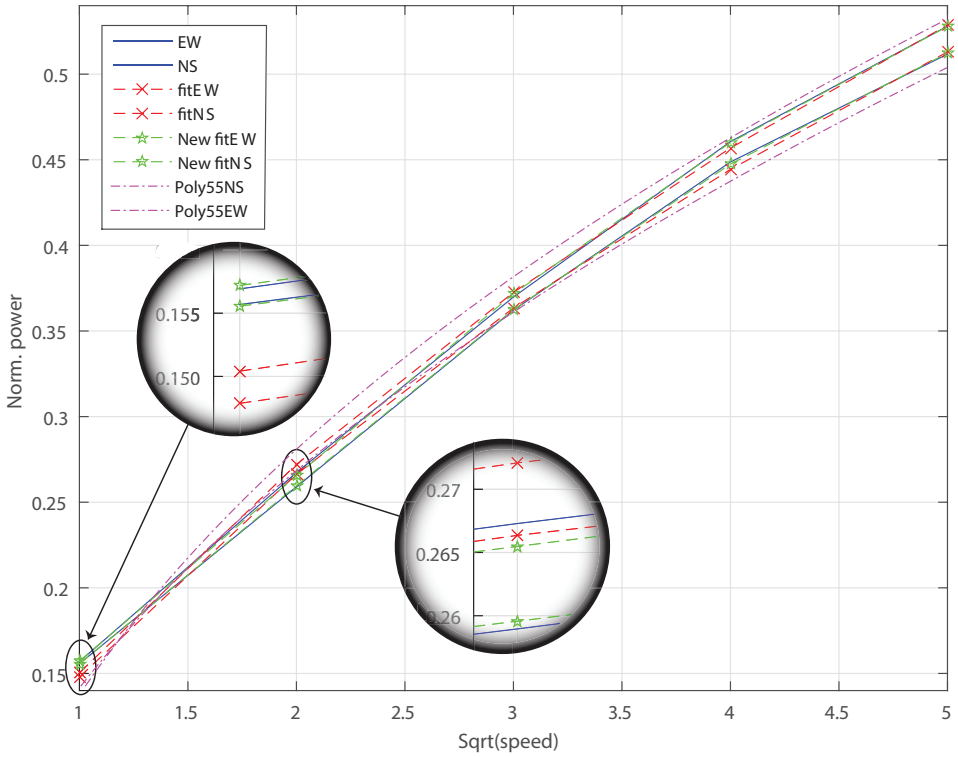


Figure 4.4: A graphical view of equations 4.1 and 4.2.

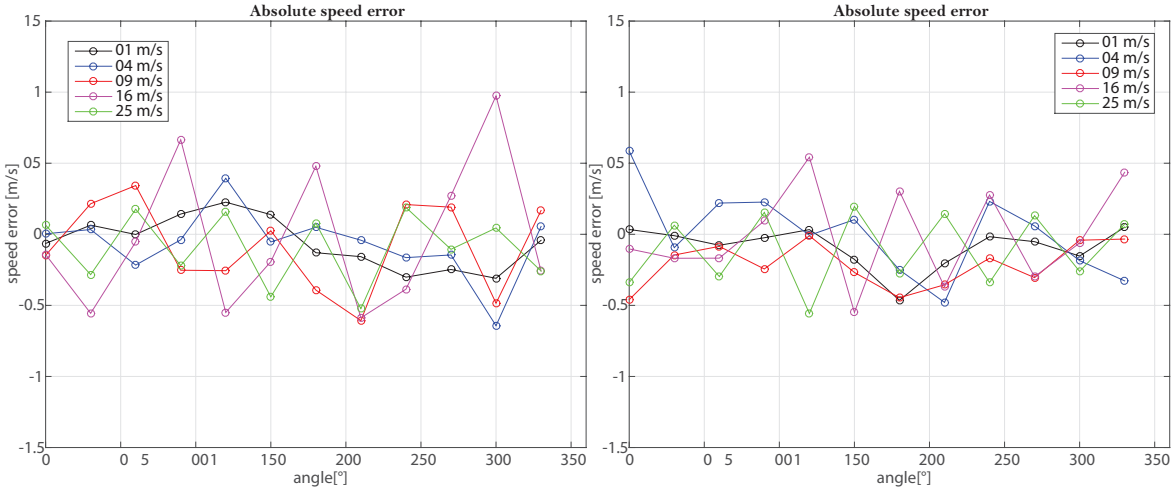
$$\delta P_{NS} = \frac{P\sqrt{U}}{A_{NS} + B_{NS}\sqrt{U}} * \cos(\theta + \delta_{NS}) + D_{NS}\sqrt{U} + E_{NS} \tag{4.1}$$

$$\delta P_{NS} = \left(\frac{P\sqrt{U}}{A_{NS} + B_{NS}\,(U + F_{NS})} + \frac{D_{NS}}{U} \right) * \cos(\theta + \delta_{NS}) + E_{NS} \tag{4.2}$$

Using equation 4.1 as model for the fit, results turned out worse in comparison to the work of W. Brevet [17]. Therefore, adjustments were made to see if a more accurate model could be generated. Previous works [9] make use of the two-dimensional, fifth-order polynomial fit (poly55); a standard function of MATLAB. This fit made the higher wind speeds correspond well to the bitstream average, but lower wind speeds still showed some offset error. In figure 4.4, the fit equation 4.1 is plotted, where MATLAB has calculated (fitted) the parameter constants. The zoom on 1 m/s and 4 m/s wind speed, shows the error in the relation. With some experimenting, equation 4.2 is generated, mostly solving all the bigger gaps. The coefficient $\frac{D}{U}$ provides error reduction for lower speeds and coefficient F enables a shift of the curve. The extra parameters give opportunity to a tighter fit. This new fit only performs worse in higher speeds. In the final solution, a combination of equation 4.2 and the poly55 is selected, where 1 - 16 m/s and 25 m/s is evaluated by equation 4.2 and the poly55, respectively. The optimal transition needs to be determined with extra measurement points in that range, but is for now determined by an exponential being ~0 at the first range and ~1 at 25 m/s.

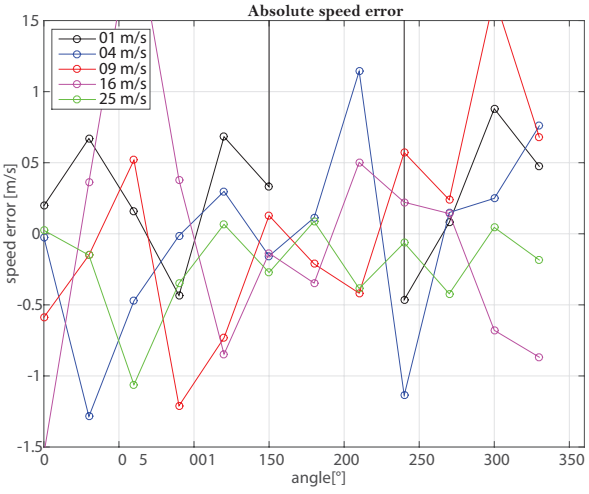
4.4. RESULTS

Matlab is used to select the optimal fit coefficients, such that minimal error is left, resulting in 'measured wind speeds and angles'. In figures 4.5a-4.5c, the absolute speed errors are plotted over the 12 angles. Note the difference in sample (p2 or p3), power (10 or 30 mW) and frequency (5 or 10 kHz). In figure 4.5d, the angle error is plotted. At a speed of 1 m/s, this error significantly increases. It is suspected that this is caused by a different, more laminar behavior of wind at low speeds whereas the wind behavior turns turbulent at higher wind speeds. A laminar wind will give different results [23]. Note that the used approach assumes that all errors are constant, i.e., that a new set of measurements show same results.

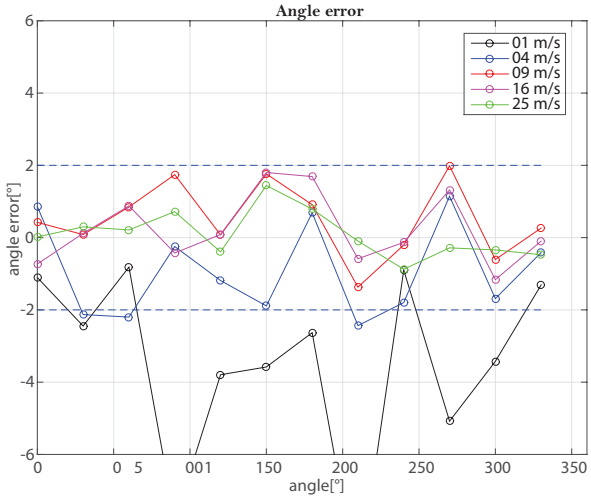


(a) p2, 5kHz, 30mW

(b) p3, 5kHz, 30mW



(c) p3, 10kHz, 10mW



(d) p3, 5kHz, 30mW

Figure 4.5: Results

5

CONCLUSION

In table 5.1, a comparison is made to previous works. Not all goals set at the beginning of the work were achieved, specifically in terms of the maximum inaccuracy of speed and direction, but the measurements for the signal swing has been insightful. A slight increase of power consumption was observed and extra sensitivity for high sampling clock frequencies were seen. The reason for this reduction in performance can be found by comparing the previous designs, which are quite alike. Only a few things are left to blame. In this chapter, a conclusion is drawn from the results.

Table 5.1: Comparison table

	This work	W. Brevet[17]	J. Wu[9]	Y. Zhu et al.[14]
Publication year	2018	2015	2011	2017
Technology	0.7 µm CMOS	0.7 µm CMOS	0.7 µm	MEMS
Open-/Closed-loop	Closed-loop	Closed-loop	Closed-loop	Open-loop
Read-out circuit	On-chip	On-chip	On-chip	PCB (153 mW)
Wind speed range (m/s)	1-25	1-25	1-25	0-33
Power dissipation (mW)	30	25	25	14.5
Decimation filter	fixed sinc1	fixed sinc1	tracking	Not given
Speed error % (or m/s)	±13 %* (or 0.6 FR)	±6 % * (or 0.6 *)	±4 %	±5%
Direction error	±2.5°*	±6°*	±2°	±5°
Temperature sensor	no	yes	yes	no

*This performance is not achieved on Full Range(FR), but on the range 4-25 m/s.

The main difference between this design and that of W. Brevet, is the location of the heaters. For that matter, a comparison with the work of J. Wu is more feasible, since the heaters are placed roughly in the same position. Compared to his design, the main difference is the layout, which is completely redone. The electronics are made very compact, which might have led to extra parasitic capacitances. This can also explain why the new design does not function properly at higher clock speeds, while the previous design performed better. Although clock shielding is used, it is only applied to the connections between the bondpad and the buffer in the center electronics.

Furthermore, the thermopiles have been made smaller and longer, thereby increasing their resistance. In combination with the parasitic capacitances and the gate capacitances of the following integrator, this forms a low-pass filter. The effect of lowering the pole in the filter has been neglected, but might have contributed negatively by the extra filtering of high frequency components in the signal.

Also the package of the wind sensor is a 'black box'. It was done in China and so it is unknown how much of the performance variation can be due to the packaging process. Considering that the previous packaging was done about two years ago, packaging variations could have been substantial and have accounted for the

increased error in this work.

The performance of W. Brevet, noted in table 5.1, is based on his best sample. Next to this sample, results of 3 other samples are shown in his thesis[17]. A larger set increases the chance of a good sample. Since this work only relies on two successfully tested samples, more samples could very well push the best performance closer to the design goals.

6

RECOMMENDATIONS

As shown in section 3.3, a 0.5 mV input referred offset is detected. The resulting ripple might be one of the limiting factors for the resolution and a contribution to the maximum error. Although the mentioned timing diagram should ideally solve the ripple problem, its load on the integrator might still cause an error. Currently, a folded cascode amplifier is used in the integrator. Every transistor pair contributes to the offset by their mismatch. Going from a folded cascode to a telescopic topology, the transistor pairs which are sensitive to mismatch, will be reduced from 3 to 2. Besides that, a ripple reduction loop could be implemented.

In this design, the existing comparator from previous designs is used. This comparator has an asymmetry in the clock lines, creating a several millivolts of offset. This will cause the system to stabilize to a slightly imbalanced situation, as explained in section 2.3. A better-matched and more energy efficient comparator can be made to resolve this issue.

A whole other topology could be investigated, where the thermopiles are rotated by 90 degrees. The crosshair shape might give advantages over the current shapes. Additionally, a lot of area was left over for decoupling capacitors when all separate blocks were layed out. More area could be used for the thermopiles, as well as the circuitry. The compact layout increases the sensitivity to higher clock speeds.

More applications for the test heaters could be investigated. For example, implementing a zoom ADC [34] where the heaters are part of the coarse ADC. In this situation, the test heaters are activated such that the larger wind effects are accounted for. In that case, the main heaters in the $\Sigma\Delta$ loop only need to digitize the smaller signals. More interesting could be this same principle, but only applied at the higher wind speeds, such that the dynamic range of the wind sensor is increased. A draw back for this approach is the risk at non-uniformities and the need for extra calibration points.

The test setup in the wind tunnel, as shown in figure 4.2, can be much simplified by shortening the long cable that transports signals into the wind tunnel chamber. The complete setup can be moved inside the wind tunnel chamber, except the laptop. A long USB cable can connect the NI USB-6259 DAQ to the laptop, outside the room. Complicated trancieve PCBs become unnecessary.

BIBLIOGRAPHY

[1] M. Shikida, T. Matsuyama, T. Yamada, M. Matsushima, and T. Kawabe, "Development of implantable catheter flow sensor into inside of bronchi for laboratory animal", *Microsystem Technologies*, vol. 23, no. 1, pp 175-185, 2017.

[2] Y. Zhu, B. Chen, M. Qin, and Q.A. Huang, "2-D Micro-Machined Thermal Wind Sensors — A Review," *IEEE Internet of Things Journal*, vol. 1, no. 3, pp. 216–232, Jun. 2014.

[3] S. Espejo, J. Ceballos-Cáceres, A. Ragel-Morales, S. Sordo-Ibáñez, L. Carranza-González, J.M. Mora-Gutiérrez, M. Lagos-Florido, and J. Ramos-Martos, "MEDA Wind Sensor Front End ASIC", 2016.

[4] F. Hall, R. Huffaker, R. Hardesty, M. Jackson, T. Lawrence, M. Post, R. Richter, and B. Weber, "Wind measurement accuracy of the NOAA pulsed infrared Doppler lidar," *Applied optics*, vol. 23, no. 15, pp. 2503-2506, 1984.

[5] R.Targ, B. Steakley, J. Hawley, L. Ames, P. Forney, D. Swanson, R. Stone, R. Otto, V. Zarifis, P. Brockman, R. Calloway, S. Klein, and P. Robinson, "Coherent lidar airborne wind sensor II: flight-test results at 2 and 10 μmm", *Applied optics*, vol. 35, no. 36, pp. 7117-7127, 1996.

[6] Q.H. Meng, P.F. Qi, K. Wu, S.H. Zhu, and M. Zeng. "2-D Wind Velocity Measurement Using a Vertically Suspended Optical Fiber Combined With a Photosensor Array", *IEEE Transactions on Instrumentation and Measurement*, 2017.

[7] M. Neal, C. Sauzé, B. Thomas, and J. Alves, "Technologies for autonomous sailing: wings and wind sensors," *Proceedings of the 2nd IRSC, Matosinhos, Portugal, July*, pp. 6-12, 2009.

[8] H. Irwin, "A simple omnidirectional sensor for wind-tunnel studies of pedestrian-level winds" *Journal of Wind Engineering and Industrial Aerodynamics*, vol. 7, pp. 219–239, 1981.

[9] J. Wu, *A Low-Power Thermal Wind Sensor in CMOS Technology*, M.SC. Thesis, Delft University of Technology, 2013.

[10] J. Kuo, L. Yu, and E. Meng, "Micromachined Thermal Flow Sensors — A Review," *Micromachines*, vol. 3, no. 3, pp. 550–573, Mar. 2012.

[11] V. Balakrishnan, H.P. Phan, T. Dinh, D.V. Dao, and N.T. Nguyen, "Thermal Flow Sensors for Harsh Environments", *Sensors*, vol. 17, no. 9, pp. 1424-8220, 2017.

[12] A.F.P. van Putten and S. Middelhoek, "Integrated silicon anemometer," *Electronics Letters*, vol. 10, no. 21, pp. 425-426, Oct. 1974.

[13] Y. Ye, Z. Yi, S. Gao, M. Qin, and Q. Huang, "DRIE trenches and full-bridges for improving sensitivity of 2-D micromachined silicon thermal wind sensor," *Journal of Microelectromechanical Systems*, vol. 26, no. 5, pp. 1073-1081, 2017.

[14] Y. Zhu, M. Qin, Y. Ye, Z. Yi, K. Long, and Q. Huang, "Modelling and characterization of a robust, low-power and wide-range thermal wind sensor," *Microsystem Technologies*, vol. 1, pp. 001–015, 2017.

[15] K.A.A. Makinwa and J.H. Huijsing, "Constant power operation of a two-dimensional flow sensor", *IEEE Transactions on Instrumentation and Measurement*, vol.51, no.4, pp.840-844, 2002.

[16] K.A.A. Makinwa, *Flow Sensing with Thermal Sigma-Delta Modulators*, Ph.D. Thesis, Delft University of Technology, 2004.

[17] W. Brevet, *A Low-Power CMOS Wind Sensor with Corner Heaters*, M.SC. Thesis, Delft University of Technology, 2015.

[18] P. Kiss, J. Arias, D. Li, "Stable high-order delta-sigma DACs", *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 1, pp. 985-988, 2003.

[19] R.W.M. van Riet and J.H. Huijsing, "Integrated direction-sensitive flowmeter," *Electronics Letters*, vol. 12, no. 24, pp. 647-648, 1976.

[20] J.H. Huijsing, J.P. Schuddemat, and W. Verhoef, "Monolithic integrated direction-sensitive flow sensor," *IEEE Trans. Electron Devices*, vol. 28, no. 1, pp. 133-136, 1982.

[21] A.F.P. van Putten, "An integrated silicon double bridge anemometer", *Sensors and Actuators*, vol. 4, no. 3, pp. 387-396, 1983.

[22] B.W. van Oudheusden, "Silicon flow sensors", *Proc. IEE*, vol. 135, no. 5, pp. 373-380, Sept. 1988.

[23] B.W. van Oudheusden, *Integrated Silicon Flow Sensors*, Ph.D. Thesis, Delft University of Technology, 1989.

[24] K.A.A. Makinwa and J.H. Huijsing, "A wind-sensor interface using thermal sigma delta modulation techniques", *Sensors and Actuators A: Physical* vol. 92, no. 1, pp. 280-285, 2001.

[25] K.A.A. Makinwa and J.H. Huijsing, "A wind-sensor with integrated interface electronics", *Circuits and Systems ISCAS 2001*, vol. 8, pp. 356-359, 2001.

[26] K.A.A. Makinwa and J.H. Huijsing, "A wind sensor with an integrated low-offset instrumentation amplifier", *ICECS '01* vol. 3, pp. 1505-1508, 2001.

[27] K.A.A. Makinwa and J.H. Huijsing, "A smart wind sensor using time-multiplexed thermal $\Sigma\Delta$ modulators", *Proc. ESSCIRC '01*, vol. 1, pp. 452-455, Sept. 2001.

[28] K.A.A. Makinwa and J.H. Huijsing, "Constant power operation of a two-dimensional flow sensor using thermal sigma-delta modulation techniques", *Instrumentation and Measurement Technology Conference, Proceedings of the 18th IEEE*, vol.3, pp.1577-1580, 2001.

[29] K.A.A. Makinwa and J.H. Huijsing, "A 2^{nd} order thermal sigma-delta modulator for flow sensing", *Digest of IEEE Sensors*, pp. 549–552, 2005.

[30] K.A.A. Makinwa and J.H. Huijsing, "A smart CMOS wind sensor," *Digest of ISSCC Technical Papers*, ISSCC, pp. 432–479, 2002.

[31] C.P.L. Van Vroonhoven, *Integrated Temperature Sensors based on Heat Diffusion*, Ph.D. Thesis, Delft University of Technology, 2015.

[32] E.F.C. Meng, *MEMS Technology and Devices for a Microfluid Dosing System*, Ph.D. Dissertation, California Institute of Technology, Pasadena, CA, USA, 2003.

[33] K.A.A. Makinwa, J.H. Huijsing, and A. Hagedoorn, "Industrial design of a solid-state wind sensor", *Sensors for Industry, 2001. Proceedings of the First ISA/IEEE Conference*, pp. 68-71, 2001.

[34] B. Gönen, F. Sebastiano, R. van Veldhoven, and K.A.A. Makinwa, "A Hybrid ADC for High Resolution: The Zoom ADC", *Hybrid ADCs, Smart Sensors for the IoT, and Sub-1V & Advanced Node Analog Circuit Design*, Springer, 2018, pp. 99-117.

A

CHIP & DIP PIN-OUT

Table A.1: Pin description

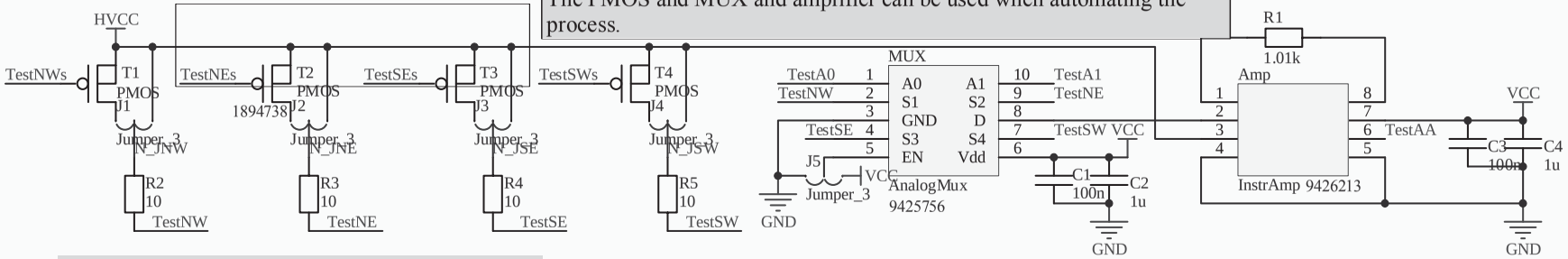
Chip pad	Name	I/O	Test	DIP pin	Description
1	TestNW	I	x	21	North-West testheater positive terminal
2	IntNS+	O	x	20	Positive terminal of the North-South integration capacitor
3	Clk	I		19	4 times f_s. Must be programmable with range 4kHz-400kHz
4	Clk_cl	I		18	1 Hz signal used for slow chopping & readout synchronisation
6	TestNE	I	x	16	North-East testheater positive terminal
9	Hvdd	I		13	Heaterpower, between min and 5.5V)
10	Hgnd	I		12	Heater ground
11	IntEW-	O	x	11	Negative terminal of the East-West integration capacitor
13	TestSE	I	x	9	South-East testheater positive terminal
14	IntEW+	O	x	8	Positive terminal of the East-West integration capacitor
15	Pol	I	x	7	Polarity bit; flips the system sign. (flip = high)
16	BS_mux	O		6	$\Sigma\Delta$ Bitstream, time multiplexed NS and EW signals.
17	En_RTH	I	x	5	Enables Return To Heat (disable = high)
18	TestSW	I	x	4	South-West testheater positive terminal
21	Gnd	I		1	Ground of the system
22	Vdd	I		24	Power of the system, 5V
23	IntNS-	O	x	23	Negative terminal of the East-West integration capacitor
5, 7, 8 12, 19 20, 24	NC			2, 3, 10 14, 15, 17, 22	Not connected

B

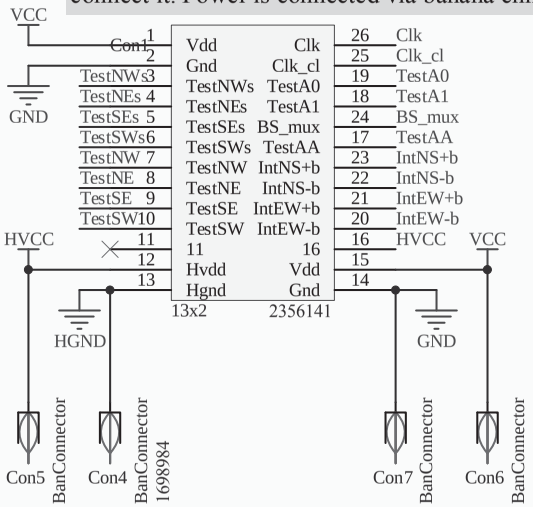
PCB SCHEMATICS

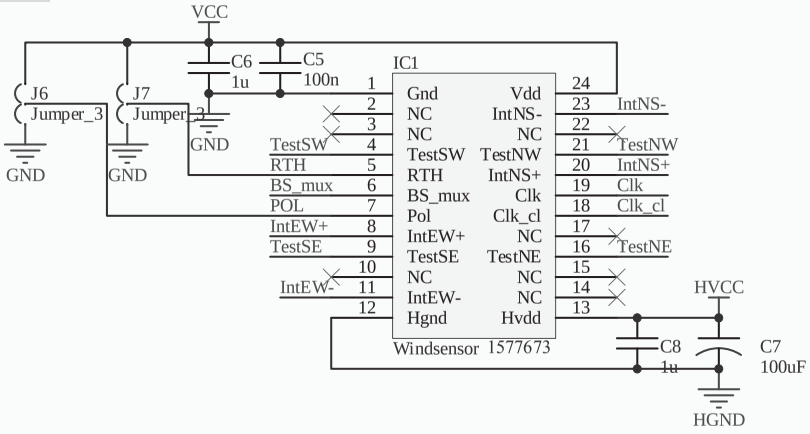
Below are the schematics of the three PCBs used to perform the measurements. The first schematic is the PCB used to test the wind sensor in its DIL package. The second and third schematics are the send (computer) and receive (wind sensor) side. Only the bitstream travels in opposite direction. The two PCBs are connected with two LAN (UTP) cables; 16 wires in total. Underneath the components, the Farnell order numbers are noted. See the Farnell website for documentation on individual components.

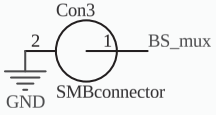
This branch is used to measure matching with the 10 ohm shunt resistors. The PMOS and MUX and amplifier can be used when automating the process.



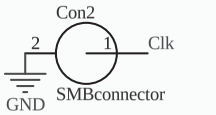
This is a normal PCB header. A flat cable is used to connect it. Power is connected via banana cnnectors

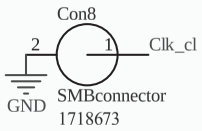


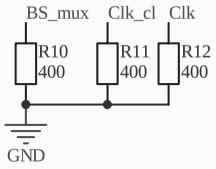


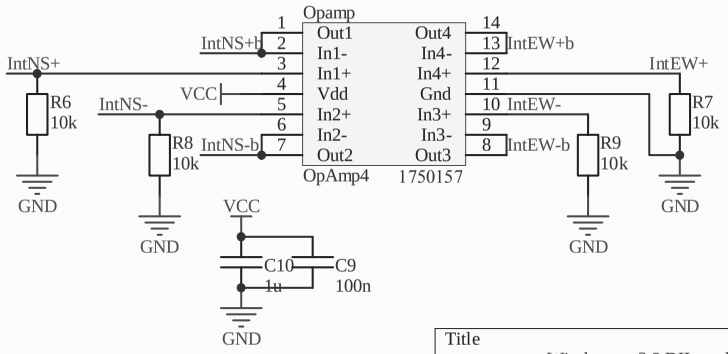


Optional termination resistors, SMB connectors for the clock signals.









The integration capacitor outputs need to be terminated with 10kΩ. To isolate this from the line, an OpAmp is used.

Title	Windsensor 3.2 DIL package PCB	
Size: A4	Number:	Revision: V1
Date: 20-1-2017	Sheet of	
File: O:\PCBs\Windsensor3.2_DIL\Toplvl.SchDoc	Drawn By: Arjan vd Kruijt	

Signals enter via SMB cables from the break-out PCB of the NI-USB device. 7V is supplied by an external voltage source, enters via banana connectors.

7V
LDO
Vin
GND
Out
GND
4 GND
1663375

5V
C5 100n
C6 1u
GND

Cab1 SMBcable
Cab2 SMBcable

Con1 SMBconnector
GND 2
1 Bitstream

Con3 SMBconnector
2
1 sync
R6 2447283
GND

Con4 SMBconnector
2
1 Data
R7 2447283
GND

Con5 SMBconnector
2
1 Clk
R8 2447283
GND

Con6 SMBconnector
2
1 Clk_cl
R9 2447283
GND

7V Con7 BanConnector

Con8 BanConnector 1698984
GND

Trn1 1470441

Bitstreamz 1	1B	Vcc	16	5V	
Bitstreamy 2	1A	1D	15	sync	
Bitstream 3	1R	1Y	14	synca	
5V 4	1DE	1Z	13	syncb	
5	2R	2DE	12	5V	
6	2A	2Z	11	Datab	
7	2B	2Y	10	Dataa	
GND 8	GND	2D	9	Data	

5V
C7 100n
C8 1u
GND

Trn2 1470441

1	1B	Vcc	16	5V	
2	1A	1D	15	Clk	
3	1R	1Y	14	Clka	
5V 4	1DE	1Z	13	Clkb	
5	2R	2DE	12	5V	
6	2A	2Z	11	Clk_clb	
7	2B	2Y	10	Clk_cla	
GND 8	GND	2D	9	Clk_cl	

Signals are made differential to be send over cable

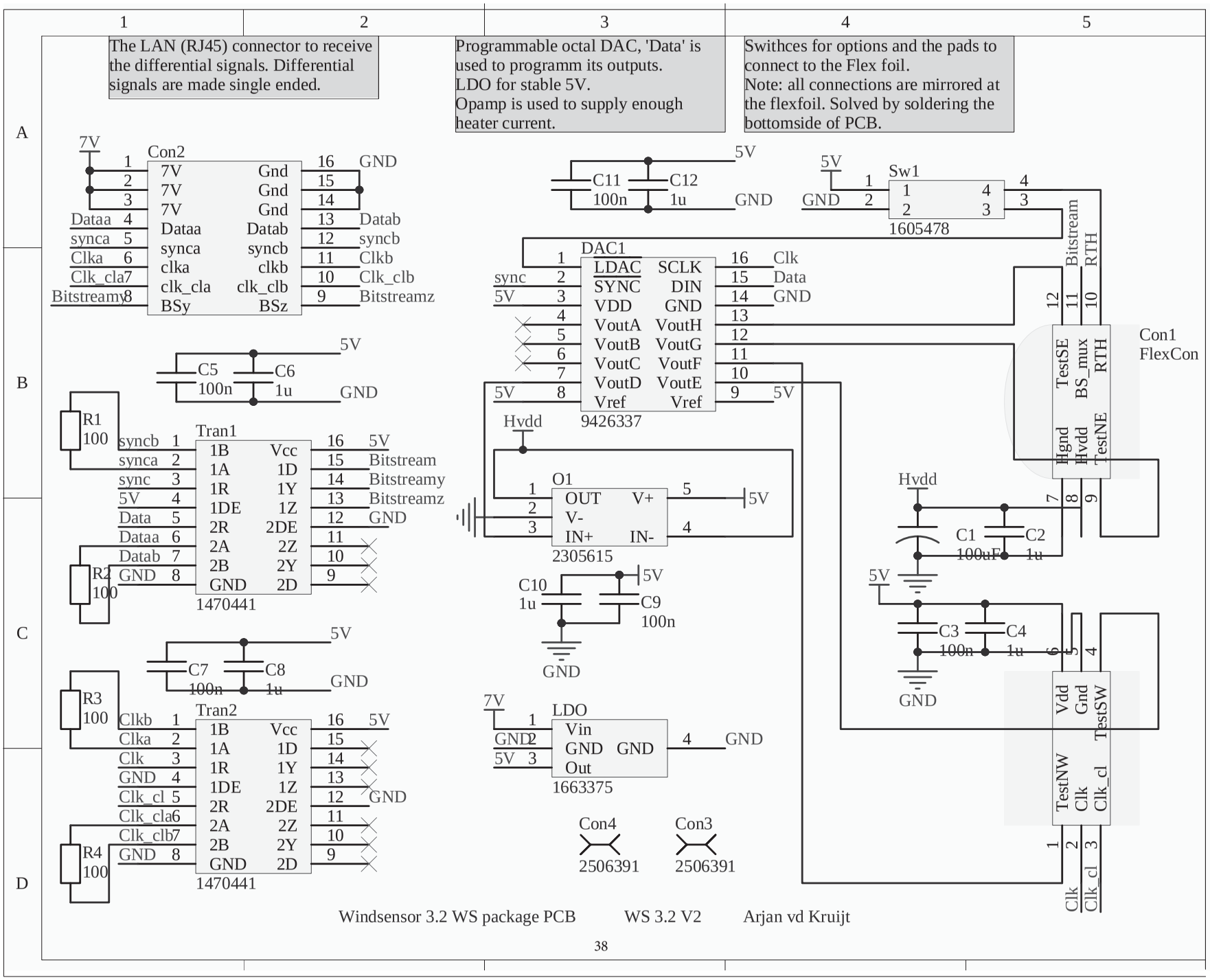
1860583
7V
Con2 1860583

1	O/	Br	16	Clk_cla	
2	O	Br/	15	Clk_clb	
GND 3	G/	G	14	GND	
Dataa 4	B	B/	13	syncb	
Datab 5	B/	B	12	synca	
GND 6	G	G/	11	GND	
Clkb 7	Br/	O	10	Bitstreamy	
Clka 8	Br	O/	9	Bitstreamz	
GND 21	L2-	L4-	17	GND	
22	L2+	L4+	18		
GND 23	L1-	L3-	19	GND	
24	L1+	L3+	20		

sync R1 2447283
5V R2 2447283
R3 2447283 Bitstream
R4 2447283 PIN
R5 100

UTP cable with LAN-connectors (RJ45) used to easaly connect the two PCB's. Lower pins are LED to check if signals are active.

Title	Windsensor 3.2 WS package PCB		
Size: Tabloid	Number:	Revision: WS 3.2 V2	
Date: 1/4/2018	Sheet of	Arjan vd Kruijt	
File: C:\Users\..\WSP2a.SchDoc	Drawn By:		



Windsensor 3.2 WS package PCB WS 3.2 V2 Arjan vd Kruijt