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Abstract

Nanostructures of platinum-carbon nanocomposite material have been formed by electron-beam induced deposition (EBID). These consist of nanodots and nanowires with a minimum size ~20 nm, integrated within ~100 nm nanogap *n*-type silicon-on-insulator transistor structures. The nanodot transistors use ~20 nm Pt/C nanodots, tunnel-coupled to Pt/C nanowire electrodes, bridging the Si nanogaps. Room-temperature single-electron transistor operation has been measured, and single-electron current oscillations and 'Coulomb diamonds' observed. In nanowire transistors, the temperature dependence from 290 – 8 K suggests that the current is a combination of thermally activated and tunnelling transport of carriers across potential barriers along the current path, and that the Pt/C is *p*-type at low temperature.

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1. Introduction

For over 40 years, CMOS technology has delivered progressive and dramatic improvements in the speed, complexity and packing density of integrated circuits, through reduced device dimensions and new device structures. However, with minimum feature sizes < 10 nm, increasingly challenging barriers are encountered in both device physics and technology [1, 2, 3, 4]. Although alternative materials and devices are being considered, e.g. III-V and III-V on silicon structures [5], hetero-junction tunnel field effect transistors TFETs [6, 7], graphene [8] and $MoSi_2$ [9], there will be significant manufacturing problems with the inclusion of these technologies. At scales < 10 nm, quantum effects are increasingly likely to influence adversely the behaviour of all these devices, even those which do not explicitly operate using these effects, e.g. quantum dot (QD) devices. For example, the operation of a nominally 'classical' Fin-FET, with a fin only ~ 4 nm wide, has been shown to be fundamentally limited by quantum confinement [4]. Finally, at dimension < 5 nm, quantum effect devices such as single-electron (SE) devices in silicon [11-13] look increasingly attractive.

Advances in high resolution lithographic and fabrication techniques, e.g. SPL [14, 15], EBL [16, 17], and NIL [18], have created alternative fabrication routes for 'beyond CMOS' <10 nm electronic device structures. At these dimensions one technique which has attracted attention is focused electron-beam-induced deposition (EBID). This facilitates the direct formation at the nanoscale of both metallic and dielectric nanostructures, through the localised electron-beam induced decomposition of an adsorbed precursor molecule, typically a gas/vapour, on any kind of substrate [20-22], although a liquid precursor has also been demonstrated [23]. Here, the electron beam interacts with the substrate and the adsorbed layer of precursor molecules, which dissociate into volatile species and are then pumped out of the system, and non-volatile species, which adhere to the sample surface to form the deposited structure.

Examples of EBID precursor gases include trimethyl (methylcyclopentadienyl)-platinum (IV) ($MeCpPtMe_3$) and $W(CO)_6$. The spatial resolution of EBID is determined by the probe size, and by the convolution of the energy dependent spatial distribution of incident electrons with both the electrons emitted from the substrate, and the energy dependent cross section for dissociation of precursor molecules at the substrate surface. The dissociation cross-section, which typically has a peak in the energy range at a few 100 eV, to some degree can overlap the energy distribution of the

secondary electrons (SE) generated in the substrate and emitted from the surface. Electrons that are generated in the deposited structure itself also contribute to this dissociation process, and enhance the growth of the structure. Proximity effects resulting from electrons scattered during the exposure of neighbouring structures further contribute to dissociating adsorbed precursor molecules, thus affecting EBID pattern sizes. Hence, defining the correct writing strategy is of great importance to achieve pattern sizes in the sub-10 nm range. Lines with widths of 2.9 nm FWHM, with a pitch of 6.1 nm, have been patterned in a 30 kV SEM using a platinum precursor [24], and dots with diameters ~ 1 nm have been patterned in a 200 keV scanning transmission electron microscope (STEM), using a tungsten precursor [25].

Device fabrication applications that have been facilitated by EBID have included electrical connections to nanowires and nanotubes [26-29], growth of nanowires, [30-32], fabrication of Pt tips for field-emission electron sources, [33, 34], field emission arrays [35, 36], nanopore nanomachining for molecule detection and DNA sequencing [37], patterned catalyst deposition [38, 39], and lithographic mask repair [40].

The electrical transport properties of EBID structures have also received attention. These include studies of tungsten-based metal-insulator-metal (MIM) tunnel junctions for single electron transport devices [41] and Pt/SiO_2/W MIM diodes [42]. Single electron transistors (SETs) with atomic layer deposition (ALD) formed tunnel barriers have been investigated [43] and the conduction mechanism studied in suspended and non-suspended Pt/C nanowires [44, 45, 46, 47]. These works show that EBID Pt-based deposition creates a nanocomposite material where Pt nanocrystals, a few nanometers to ~10 nm in size, are embedded within an amorphous C matrix. Carbon content tends to be much greater than the Pt content, and the Pt acts as an impurity within the amorphous semiconductor formed by the C [46]. The conduction mechanism through the nanocomposite resembles conduction in a doped amorphous semiconductor, and is a complex function of the concentration of the Pt nanocrystals, and the density of states in the amorphous C. Here, the latter consists of localised ‘band-tail’ states around the Fermi energy, leading towards delocalised states further away from the Fermi energy, beyond ‘mobility edges’ [46]. The ‘band-gap’ corresponding to the mobility edges is comparatively large, ~2 eV. At low bias and low temperatures, conduction occurs via variable range hopping through the localised states, and/or the percolation network formed by the Pt nanocrystals [45, 46]). At higher biases and energies, conduction also occurs through the C delocalised states beyond the mobility edges [46]. The disordered nature of the Pt/C nanocomposite leads to a strong temperature dependence of resistance [45, 46].

The presence of Pt nanocrystals within the Pt/C nanocomposite can lead to single-electron charging effects. Single-electron transistor operation has been observed in nanowires [41, 45, 47, 48], where charging occurs on islands created by the Pt nanocrystals or by nanowire roughness, or created by explicitly defining EBID Pt/C nanodots ~50 nm – 100 nm in size, isolated by ALD alumina tunnel barriers [43]. In the latter case, single-electron oscillations were reported at 0.3 K. For the nanowire case, while the nanocrystals are in principle small enough (down to ~ 3 nm, e.g. Ref [46]) for room-temperature single-electron charging in the nanowires, the maximum reported operating temperature for single-electron oscillations is ~200 – 230 K [41, 47], with Coulomb diamonds measured from 4.2 K [48] to 65 K [45].

In this paper, we present the electrical characteristics of EBID Pt/C nanowire and nanodot transistors, integrated within the thin top Si layer of silicon-on-insulator materials. The Pt/C nanostructures are deposited across ~100 nm wide nanogaps between heavily doped *n*-type source and drain point-contact regions. Pt/C nanodots were fabricated with a minimum diameter ~20 nm, separated on either side by <10 nm nanogaps from Pt/C nanowire electrodes having a minimum width ~20 nm and thickness ~10 nm, Figure 1(a). The nanowire electrodes extended to Si source and drain regions, bridging the ~100 nm wide nanogap between these. Si side gates were used to electrostatically control the current. Other device configurations investigated consisted of nanowire-only Pt/C deposits. In comparison, earlier studies of Pt/C EBID devices have included nanodots ~50 – 100 nm in diameter [43] and nanowires ~30 nm – 1 μm in length [44, 46]. Our measurements show that the Pt/C behaves as a *p*-type amorphous semiconductor. A SET, operating at room temperature, is formed by the ~20 nm nanodot device. Single-electron current oscillations with gate voltage, and 'Coulomb diamond' characteristics in the source-drain conductance as a function of drain and gate voltages, are observed. In a Pt/C nanowire device, a strong reduction in source-drain current is seen as the measurement temperature is reduced from 290 K – 8 K. In our Si-Pt/C-Si device configuration, current transport is a combination of thermally activated and tunnelling carrier transport across potential barriers along the current path, formed at the Pt/C interface and/or at grain boundaries within the Pt/C deposit. At low temperature, the gate dependence of the device current implies *p*-type semiconducting behaviour in the Pt/C.

2. Fabrication

The device structures used in this work were fabricated in a (100) oriented SOI wafer with a ~12 nm thick top Si layer and ~30 nm buried oxide layer. The top Si layer was heavily doped with phosphorous at ~10^{20} /cm^3. 10 mm × 10 mm chips were used for device fabrication, each of which held a 4 × 4 array of circuits. In each circuit, 8 device structures were defined, where the source, drain and gate electrodes could all be addressed independently. Devices were formed by using EBID to place Pt/C source/drain extensions and nanodots in the gaps left between source and drain electrodes, see Figure 1(a). In the fabrication process sequence, the entire pre-EBID device patterns in the Si were defined simultaneously using electron beam lithography, i.e. bond pads, lead-in areas, and source, drain and gate contact regions. Electron beam exposure was performed using a Vistec VB6-HR machine operating at 100 kV. A bilayer lift-off resist structure was used, comprising 100k MW PMMA, ~40 – 50 nm thick, beneath 950k MW PMMA, also ~40 – 50 nm thick, both sequentially post-baked at 180 C for 120 s. The central device area (200 μm × 200 μm) was written with a 7.8 nA beam (estimated diameter 2 - 3 nm) and the outer area (interconnect and bond pad regions) with a 184 nA beam (estimated diameter 70 nm). The areal dose was ~600 μC/cm^2. The exposed resist was developed for 10 s in a MEK: MIBK: IPA in the ratio 1: 5: 15, followed by 100% IPA rinse and then blown dry. A thin layer of Al (~ 30 nm) was deposited by thermal evaporation at a pressure ≈ 10^{-7} – 10^{-6} mbar and resist lift-off undertaken in acetone. The Al pattern acted as a mask to etch the thin Si layer to give a trench isolated pattern, this being transferred into the underlying oxide by reactive ion etching to a depth of 200 nm using SF_6 (30 sccm) and O_2 (10 sccm) plasma, with power 100 W at a potential of 200 V, pressure 100 mTorr, temperature 20 ºC and time 1 min. The Al mask was then removed by wet etching in ~ 3% HCl. Thermal oxidation at 900 ^oC for 5 minutes was used to form a thin SiO_2 layer, capping the Si and protecting the electrodes. A low magnification SEM micrograph of the device chip with the 8 individual transistors is shown in Figure 1(b). It will be seen that each device has a unique source and gate, but there are common drains between devices 1 and 2, 3 and 4, 5 and 6 and 7 and 8. In previous work [49] this oxidation process had been used to reduce the width of the silicon channel within a silicon point-contact 'neck' to allow isolation of a single, or a few morphologically defined silicon islands a few nanometres in size, creating ultra-small quantum dots. However, in this work, the neck was 'cut back' in the EBL patterns to leave a nanogap in the silicon between the source and drain instead, as shown in Figure 1(c).

Contact windows were opened in this oxide to the silicon conductors and their bond pads using photolithography. Photoresist S1828 was spin-coated at 500 rpm for 10 s, and then at 4500 rpm for 50 s, to form a resist layer ~ 3.5 μm thick, followed by a 120°C hotplate bake for 2 mins. A dark field mask was exposed using a power density of 5.3 mW/cm^2 for 160 s and developed in MF319 for ~ 2 min followed by a descum for 3 min and a HF dip for 1 min. A metal layer consisting of ~20 nm Cr and ~200 nm Al was deposited by evaporation. The chips were covered with a protective layer of PMMA ~ 400 nm thick, then were diced using a Spectra Physics Talon UV laser micromachining system (wave length 355 nm, max. power 40 watts) using 60 cuts at 75% maximum power. The PMMA was removed in acetone. As a final step in this process, EBID was used to deposit extensions to the source and drain contacts, and deposit the nanodot.

The EBID device patterning was performed using a FEI Nova Nano Lab 650 SEM incorporating patterning software. The sample was held at a eucentric height with the gas injection nozzle located approximately 100 μm above the sample surface. An electron beam energy of 19 keV was used at a working distance of 5.25 mm, with a beam current of 39 pA and a beam diameter < 2 nm. A precursor gas of trimethyl (methylcyclopentadienyl)-platinum ($MeCpPtMe_3$) was used, with the deposited patterns expected to consist of Pt grains in a C matrix with a Pt:C ratio of approximately 1:5 [50]. The gas flow was stabilized on the sample surface prior to electron beam patterning, which was undertaken in two steps. First the two electrode extensions were exposed using multiple rastered passes, so that in effect each pixel was exposed for a total of 4 ms. A gap of 50 nm was left between the two contact extensions and following their deposition the electron beam was blanked and the gas pumped out of the chamber. The structure could then be imaged to locate the exact position of the gap. The island was then defined as a circle with a diameter of 2 nm, patterned with a dwell time of 4 ms and only 2 passes. Finally, a single-process-step EBID technique offers a higher level of control to achieve ~10 – 20 nm feature sizes, in comparison with multiple process steps and resist-based e-beam lithography.

It is recognised that EBID processes contribute a halo effect. This was not cleaned because the amount of material deposited was so small and spread over a quite a large area and as such would not have formed a conducting layer. At 19 keV, the energy at which the deposition was performed, the diameter of the disk from which the backscattered electrons are emitted is 2.47 μm [51]. Assuming a worst case scenario that the number of electrons generated by the backscattered electrons, SE2, is equal to the number of electrons directly generated by the primary electrons, SE1, and that the SE1 electrons are emitted from an area with a diameter of ~ 3 nm (a convolution of the

probe size and the inelastic mean free path), the surface density is approximately 1.5×10^{-6} times smaller than the SE1 surface density. On this basis an estimate of the number of atoms deposited in the 100 nm wide gap between source and drain electrodes, assuming a continuous 20 nm wide EBID line of 10 nm height and 100 nm length, is about 7.4×10^5 atoms. Assuming that the same number of atoms is deposited in the halo, of diameter 2.47 μm, the number of atoms per nm^2 is only 0.12, leading neither to a closed conducting surface layer nor likely to have an effect on the electrical characteristics of the nano-island devices.

SEM micrographs of the nanodot structures are shown in Fig. 2. The silicon source, drain and gate electrodes prior to nanodot deposition are shown in (a). The extended electrodes and nanodot following EBID are shown in (b). As estimated from the SEM image, the gap to the island on the LHS is 9.7 nm, that on the RHS 4.5 nm, with the dot diameter being 22.5 nm. A further SEM image of the same device, taken at a tilt angle of 45° is shown in (c). The SEM image of another device with a nanodot diameter of ~11 nm is shown in (d). Finally, with such small deposits, usually the aspect ratio is ~1-2. Using this aspect ratio, and inspection of SEM images, we estimate that the deposit thickness is ~10 nm.

3. Electrical Characterisation

Room temperature (RT = 290 K) measurements of the drain-source current vs. drain and gate voltage were performed using a 4-point probe station in conjunction with either an Agilent 4155B parameter analyser or a combination of Keithley 236 source measurement units (SMUs) interfaced with a computer. Subsequent data analysis of the results was undertaken using Matlab programmes. For the temperature dependent measurements, from 290 – 8 K, samples of interest were wire bonded into chip carriers and inserted in a CTI-Cryogenics closed cycle helium cryostat. Characterisation were performed by measuring I_{ds} as V_{ds} was swept from negative to positive voltage at constant V_{gs}, with a step in V_{gs} from one curve to the next. A hold time ~10 seconds was used between curves. The direction of the V_{ds} sweep could be reversed without changes in the characteristics. Device characteristics were broadly stable during measurements, i.e. the measurement voltage range could be adjusted without major variation in the characteristics, though small switches in current magnitude were possible, attributable to charging of defect states near the current path.

The RT drain current (I_{ds}) and drain conductance (g_{ds}) vs. drain (V_{ds}) and gate (V_{gs}) voltage characteristics of a Pt/C nanodot device (Device A, SEM image in Fig. 2(b)) are shown in Figure 3. The nanodot is ~20 nm in diameter, with ~50 nm long Pt/C nanowire electrodes on either side, isolated by few-nanometre scale gaps from the nanodot. The nanowire electrodes lead to Si point-contact regions. The measured data for I_{ds} vs. V_{ds}, V_{gs} using a 3D plot are shown in Figure 3(a). I_{ds} is seen to increase non-linearly with V_{ds}, in a symmetrical manner for $\pm V_{ds}$. Current oscillations with a period $\Delta V_{gs} \sim 0.5$ V are seen, with finer, irregular fluctuations superimposed on these from one $I_{ds} - V_{ds}$ sweep to the next. The main current oscillations can be better investigated by using moving average (over 7 points) thin-plate spline fits to the data (Fig. 3(b)). A logarithmic plot of the magnitude of drain conductance $|g_{ds}|$, extracted from the smoothed data in (b), and plotted vs. V_{ds} and V_{gs} as a log scale colour, planar image is shown in Figure 3(c). The plot of log $|g_{ds}|$ allows diamond-like regions, marked 'A' and 'B', to be seen, within which g_{ds} is small, for small V_{ds} values and $0 < V_{gs} < 1.2$ V. The corresponding oscillation in g_{ds} continues for $V_{gs} > 1.2$ V, however, full diamond-like regions are not seen, as there is a low conductance region near $V_{ds} = 0$ V which cannot be modulated to larger g_{ds} values in a manner similar to the area between diamonds 'A' and 'B'. The I_{ds} vs. V_{ds} characteristics at different values of V_{gs}, offset from each other, are shown in Figure 3(d) using a 2D plot. Here, the relative extent of modulation of I_{ds} curves by V_{gs} can be observed. The gate modulation of I_{ds} vs. V_{gs}, at constant V_{ds}, are shown on a linear scale in Figure 3(e) and log (f). Both the measured data (scatter points) and the spline fits to these are shown.

The electrical characteristics of Figure 3 may be attributed to the formation of a room temperature single-electron transistor (SET) [13, 49]. Here, the diamond-like regions 'A' and 'B', and the gate oscillation in I_{ds} may be associated with Coulomb diamonds, and gate modulated single-electron current oscillations, respectively [13]. The likely origin of the charging island, leading to SET behaviour, is the ~20 nm scale Pt/C nanodot (Fig. 2(b)). An alternative hypothesis is the existence of nanocrystals within the Pt/C nanowire electrodes. In the former case, the tunnel barriers isolating the charging island are the nanogaps between the nanodot and the electrodes. In the latter case, the origin of the tunnel barriers is less clear, and the existence of potential barriers at grain-boundaries surrounding the charging nanocrystals would be necessary.

The Coulomb diamond regions 'A' and 'B' in Fig. 3(c) can be used to extract the tunnel barrier (C_1 and C_2) and gate (C_g) capacitances for the nanodot [13]. Using the width of diamond 'A' parallel to the V_{gs} axis, $\Delta V_{gs} = e/C_g = 0.62$ V, we find $C_g = 0.26$ aF. Assuming equal voltage drops across the two tunnel barriers, the width of the diamond parallel to the V_{ds} axis, $\Delta V_{ds} = 2E_{cg} = 2e/C_t = 0.1$ V,

where $C_t = C_1 + C_2 + C_g$ is the total nanodot capacitance and $E_{cg} = e/C_t$ is the Coulomb gap. This gives C_t = 3.2 aF. As the top and bottom corners of the diamond are very close to a vertical line drawn through the diamond centre, (red dotted line), this implies that $C_1 \approx C_2 = C$. This gives $C_t = 2C + C_g$ and hence, C = 1.47 aF. This value may be associated with the ~20 nm diameter Pt/C composite nanodot in the device, where at room temperature, both the Pt and the amorphous C are conducting. Using the self-capacitance of the nanodot, assuming a spherical shape, this is given by $C_{dot} = 4\pi\varepsilon_0 r$, where r is the nanodot radius and ε_0 the permittivity of free space. In our case, $r \sim$ 10 10 nm, giving C_{dot} = 1.1 aF ~ C, as extracted from the electrical characteristics. Finally, the Coulomb gap $E_{cg} = e/C_t$ = 50 meV and the single-electron charging energy $E_c = E_{cg}/2$ = 0.25 meV ≈ $k_B T$ at room temperature T = 290 K. This suggests that single-electron effects in the device at room temperature would be relatively weak, as is the case in the results of Fig. 3.

The temperature dependence from 290 K – 8 K of the I_{ds} - V_{ds}, V_{gs} characteristics from a second Pt/C nanodot/nanowire device (Device B) are shown in Figure 4. Here, the I_{ds} - V_{ds} characteristics are diode-like, with a turn-on voltage $V_t \sim$ 0.5 V at 290 K. The asymmetric, diode-like nature of the curves is unlike the symmetrical characteristics seen for Device A (Fig. 3). While a weak, irregular oscillation exists in I_{ds} vs. V_{gs} at 290 K, this is not as prominent as in the data of Fig. 3. A small current step can also be seen in I_{ds} near V_{ds} = 0 V. As the measurement temperature T is reduced, V_t increases to ~1 V by T = 100 K. For $T <$ 100 K (Fig. 4(e) and (f)), V_t increases further to ~2 V at V_{gs} = 0 V. Furthermore, V_t increases with V_{gs}, leading to a reduction in I_{ds} at a constant value of V_{ds}, which is behaviour not seen for $T \geq$ 100 K.

The I_{ds} vs. V_{ds} characteristics at V_{gs} = 0 V, from 290 – 8 K are shown in Figure 5, using linear (a) and log plots (b). In Fig. 5(b), the increase in V_t as T reduces can be seen. The current step in I_{ds} is clearer for lower temperatures, e.g. 100 K and 150 K (Fig. 5(b)). Arrhenius plots of log (I_{ds}) vs. 1/T, for V_{ds} = 1, 0.75 and 0.5 V are shown in Figures 5(c) and (d). For $T >$ 200 K, there is a large increase in I_{ds} with increasing temperature, implying a thermally activated current flow across a potential barrier along the current path. Linear fits to the data from 290 – 200 K (d) allow extraction of the activation energy E_a, from the slope of the equation for the fit, $\log(I_{ds}) = (T^{-1})(E_a/k_B) + c$, where the last term is the y-axis intercept. We find that $E_a \sim$ 0.2 eV, and may be associated with the height of the dominant potential barrier along the current path (Si-Pt/C-Si) through the device. For $T <$ 100 K, there is little variation in I_{ds}, implying a tunnel dominated rather than thermally activated conduction regime.

A band diagram model is used to explain the temperature dependence of Figs. 4 and 5, shown schematically in Figure 6. Potential barriers can exist at the interface between the Pt/C nanowires and the Fermi seas in the heavily doped source and drain Si point contacts (Fig. 6(a)). The potential barriers may be formed by the native oxide on the Si point contacts, and by the trapping of charge carriers in both the Si and in the deposit by interface traps. The Fermi energies in the Si source and drain, and Pt/C deposit regions, are E_{FS}, E_{FD}, and $E_{F\text{-}d}$ respectively. The Pt/C deposit is assumed to be an amorphous semiconductor, due to the C matrix in the Pt/C [46]. Figure 6(a) shows schematically the density of states (red line) in the Pt/C, with mobility edges at energies $E_{c\text{-}d}$ and $E_{v\text{-}d}$ above and below the Fermi energy. States lying at energies within the mobility edges are localised and those without are de-localised. The amorphous semiconductor picture is supported in our data as (1) I_{ds} is strongly thermally activated by three orders of magnitude from 290 – 100 K (Fig. 5(c)), as would be expected in a semiconducting rather than a metallic picture, and (2) gate modulation of I_{ds} can be seen for lower temperatures. Furthermore, for argument (2), the increase in V_t and reduction in I_{ds} with increasing gate voltage V_{gs} at low temperature suggests *p*-type behaviour and hole transport in the Pt/C, at least at low temperature, as discussed in detail below. Hence, $E_{F\text{-}d}$ is shown closer to the lower mobility edge $E_{v\text{-}d}$. For simplicity, tunnel barriers within the deposit, due to potential barriers at the Pt nanocrystal boundaries, are not shown, though these can also be significant, particularly at low temperatures. Furthermore, while the model shows dominant hole transport below the lower Pt/C mobility edge $E_{v\text{-}d}$, at higher temperatures thermally excited electron current above the mobility edge $E_{c\text{-}d}$ is also possible.

In the case of temperatures $T > 100$ K, both thermally activated and tunnelling current paths can exist, labelled ‘1’ and ‘2’ respectively (Fig. 6(b)). From the Arrhenius plots in Fig. 5(c), for T within the range 290 K > T > 200 K, not only is there is a reduction in the thermally activated carrier concentration in the deposit, there is also a reduction in the thermally activated current over the source potential barrier, path ‘1’. Furthermore, for $T > 200$ K, path ‘1’ dominates, for the range 200 K > T > 100 K both paths ‘1’ and ‘2’ are significant, and for $T < 100$ K, the tunnelling path ‘2’ dominates (Fig. 6(c)). The reduction in hole concentration and thermally activated current as the temperature falls (compare (b) to (c)), leads to an increase in V_t. At lower temperatures, the majority of current can be associated with hole injection from the source, as the hole concentration within the Pt/C may reduce substantially, limiting the number of carriers available from the Pt/C.

The tunnelling current may be modulated by gate voltage (Fig. 6(d)). Applying $V_{gs} > 0$ V lowers the bands in the deposit and reduces the gate-source voltage dropping across the source tunnel barrier.

This brings the energy point '*a*' at which holes tunnel from the source closer to the mobility edge $E_{v\text{-}d}$, where the density of 'valance' band states is lower. Ultimately, the tunnelling point '*a*' may be pushed above $E_{v\text{-}d}$ (Fig. 6(d)), turning the device 'off' as seen in the characteristics of Fig. 4. This gate effect would be further enhanced by any modulation of the source tunnel barrier resistance. If this resistance reduces with applied voltage, e.g. with a narrowing of the tunnel barrier, then the reduction in voltage $V_{ds} - V_{gs}$ across the barrier for $V_{gs} > 0$ V (Fig. 6(d)) would increase its resistance at a given V_{ds}, and hence reduce I_{ds}. A combination of raised energy states in the deposit and an increase in the tunnel barrier resistance can occur, in both cases reducing I_{ds} with V_{gs}. Finally, for $T > 100$ K, the increase in the thermally activated current (path '1'), combined with the thermal generation of holes in the deposit, dominate over modulation of the tunnelling current (path '2'), suppressing observation of any gate modulation of I_{ds}.

The room temperature electrical characteristics of two additional types of devices are shown in Fig. 7. An SEM image (a) of a device having a nanowire only and without a nanodot, (Device C) is shown in Figure 7(a). Here, the I_{ds} - V_{ds}, V_{gs} characteristics (b) have a large $V_t \sim \pm 2$ V, implying stronger potential barriers than for the Device A (Fig. 3). A single complete current peak is seen in I_{ds} vs. V_{gs} (c), however multiple current peaks are not seen in a manner similar to the characteristics in Fig. 3. While the characteristics in Fig. 7(b) and (c) may have a single-electron charging origin similar to the characteristics in Fig. 3, as only a single peak is observed, this behaviour is not well established. Furthermore, the lack of an explicitly fabricated nanodot implies that if a single-electron charging origin exists, then isolated nanocrystals need to exist within the nanowire. Figure 7(d) and (e) show an SEM image of a device with a thick (~10 nm) and wide (~50 nm) Pt/C deposit (Device D), and the corresponding electrical characteristics, respectively. Here, the current is much higher, ~100 nA, due to the wider deposit. This value may be compared with I_{ds} ~1 nA in the nanodot device (Fig. 3), and ~10 nA in the nanowire device (Device C, Fig. 7(a)), where the deposits are much finer, and tunnel gaps exist (Device A, Fig. 2(b)). In Fig. 7(e), current saturation occurs in the characteristics, again supporting a semiconducting picture. Current saturation in Pt/C, followed by an increase in current at higher bias, has been attributed to the suppression of current due to the build-up of charge at the dead-ends of a percolation network in the Pt/C, followed by a rise in current as de-localised states beyond the mobility edges become accessible [46]. A similar effect may occur in the characteristics of Device 'D' (Fig. 7(e)).

Overall, a total of ten Pt/C nanowire and nanodot transistors were fabricated. In all cases, the height of the deposits was estimated to be ~10 nm. Six devices used nanodots and four used nanowires, of

varying dimension. Three of the nanodot transistors had dimensions (length, width, height) of 15 nm × 15 nm × 10 nm. In three further devices, the nanodots were 16 nm × 26 nm × 10 nm, 13 nm ×13 nm × 10 nm, and 11 nm × 11 nm × 10 nm in size. In five nanodot devices, the conductance in the linear *I-V* regions outside the Coulomb gap, or a low current threshold region, varied from 11 nS (13 nm ×13 nm ×10 nm nanodot) to 70 nS (16 nm × 26 nm × 10 nm nanodot), with average value of 36 nS. For one outlying nanodot device, there was no low current region and the I_{ds}-V_{ds} curve was linear, with high conductance ~2000 nS. This implied low resistance tunnel barriers, possibly due to substantial Pt/C deposition in the nanogaps on either side of the nanodot.

Oscillations in I_{ds} vs. V_{gs} were seen in two of the six nanodot devices (Devices A and B), three further devices showed low current thresholds or current steps in the I_{ds}-V_{ds} characteristics but no gate effect, and the I_{ds}-V_{ds} characteristic of one device was linear. For room-temperature single-electron effects, it is necessary not only that $E_c > k_BT$ but also that the tunnel barrier height > k_BT and resistance > the quantum resistance, R_q = 26 kΩ. As the nanodot dimensions were broadly similar across 5/6 devices, the lack of single-electron effects in some of these devices is more likely to be due to variation in the tunnel barrier height and/or resistance.

For the nanowire devices, the dimensions were 115 nm × 10 nm × 10 nm and 120 nm × 28 nm × 20 nm for two devices each, with average conductance ~40 nS outside the low current threshold region. This value is similar to that in the nanodot devices, as even in the case of the nanodots, there are nanowire electrode regions on either side bridging the Si nanogap (Fig. 2). Only one of these devices (Device C) showed oscillations in I_{ds} vs. V_{gs}.

In the case of some devices (e.g. the device in Fig. 2(d)), deposition in the nanogap region may lead to very narrow gaps or possible contact to the electrodes. However, in this case, the deposits on either side of the nanodot form constrictions between the nanodot and the electrodes. In Si SETs, constrictions such as these define tunnel barriers [52], due to depletion of charge carriers by surface traps. Devices of this form can still show oscillations in I_{ds} with V_{gs}, implying isolation of the nanodot, either by tunnel barriers formed by breaks in the constricted deposit region, or due to depletion of charge carriers to traps, generating a potential barrier.

4. Conclusion

The RT SET behaviour observed in Fig. 3 may be compared to very strong RT single-electron effects observable recently in Si point-contact quantum dot (QD) transistors, based on ultra-small QDs < 5 nm in diameter [49]. In those devices, the QDs were estimated to be as small as ~ 1.6 nm in diameter resulting in both single-electron charging and quantum confinement effects occurring at RT. The single-electron addition energy for the smallest devices was shown to be E_a ~ 0.8 eV >> k_BT at 290 K. The nanodot in the device of Fig. 2(b) is much larger, ~20 nm in size, such that the total capacitance C_t ~ 3.2 aF is not small enough for very strong room-temperature single-electron charging effects. However, in comparison with Si point-contact QD transistors, where some randomness in the location of the QD within the point-contact exists, the use of an EBID nanodot allows greater flexibility in the precise placement of the nanodot within a pre-defined device structure.

In summary, we have presented the electrical characteristics of EBID Pt/C nanowire and nanodot transistors, integrated within Si nanodevices. The Pt/C nanostructures were deposited across ~100 nm wide nanogaps between heavily doped *n*-type Si source and drain point-contact regions, fabricated in silicon-on-insulator material. Pt/C nanodots were fabricated having a minimum diameter ~20 nm, with Pt/C nanowire electrodes on either side bridging a ~100 nm wide nanogap between the Si source and drain regions. Si side gates were used to electrostatically control the current. A further device configuration investigated consisted of nanowire-only Pt/C deposits of different widths. Measurements showed that the Pt/C behaved as an amorphous semiconductor, with *p*-type behaviour at least at low temperature. A single-electron transistor, operating at room temperature, was formed by the ~20 nm nanodot device. Here, single-electron current oscillations and 'Coulomb diamond' electrical characteristics were observed. In the Pt/C nanowire devices, the *p*-type semiconducting nature of the devices was determined from gate measurements, and temperature dependences from 290 K – 8 K. Current transport was seen to be a combination of thermally-activated and tunnelling transport of holes across potential barriers along the current path, formed at the Pt/C interface and/or at grain boundaries within the Pt/C deposit.

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Figures

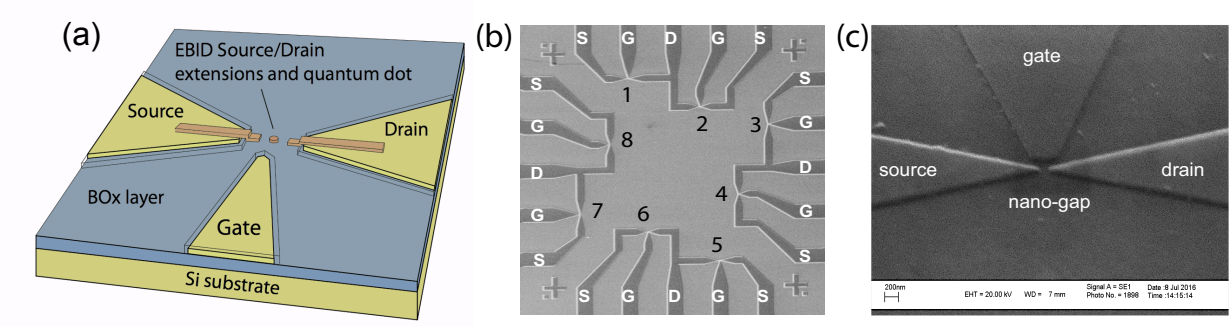

Figure 1. (a) Schematic diagram of the device structure showing the silicon source, drain and gate electrodes together with the EBID Pt/C leads and nanodot structure. (b) A low magnification SEM micrograph annotated to show the central area containing 8 device structures (numbered), each with a nanogap between the source and common drain, and a single side gate. The distance between the crosses is 200 μm. (c) SEM of device prior to EBID showing the source, drain and gate electrodes.

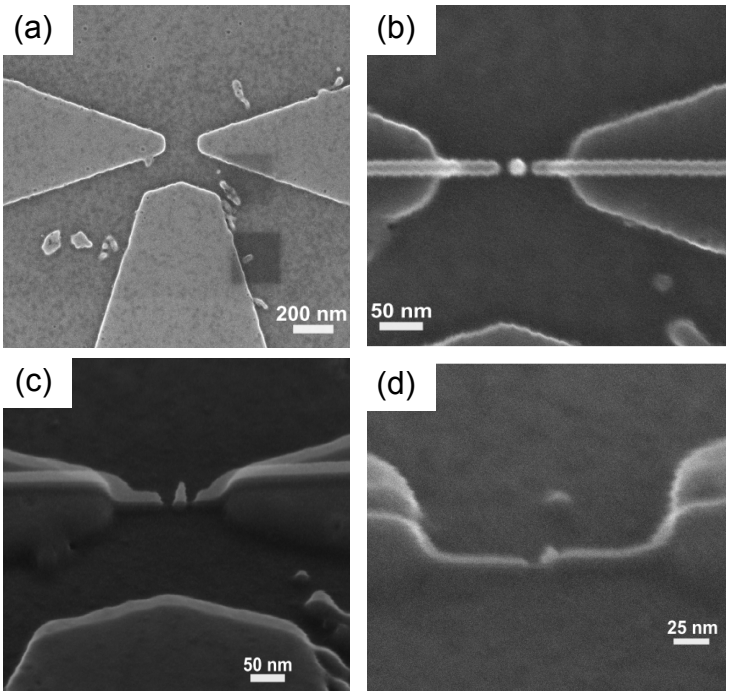

Figure 2. SEM micrographs showing the structure of a typical nanodot fabricated by Pt/C EBID. (a) The silicon source, drain and gate electrodes prior to nanodot deposition, (b) the extended electrodes and nanodot after EBID showing the gap to the nanodot, the LHS is 9.7 nm, and the RHS 4.5 nm, with the dot diameter being 22.5 nm, as estimated from the SEM image, (c) SEM images of the same device taken at a tilt angle of 45°. (d) SEM image of a further device, having a nanodot with diameter ~11 nm.

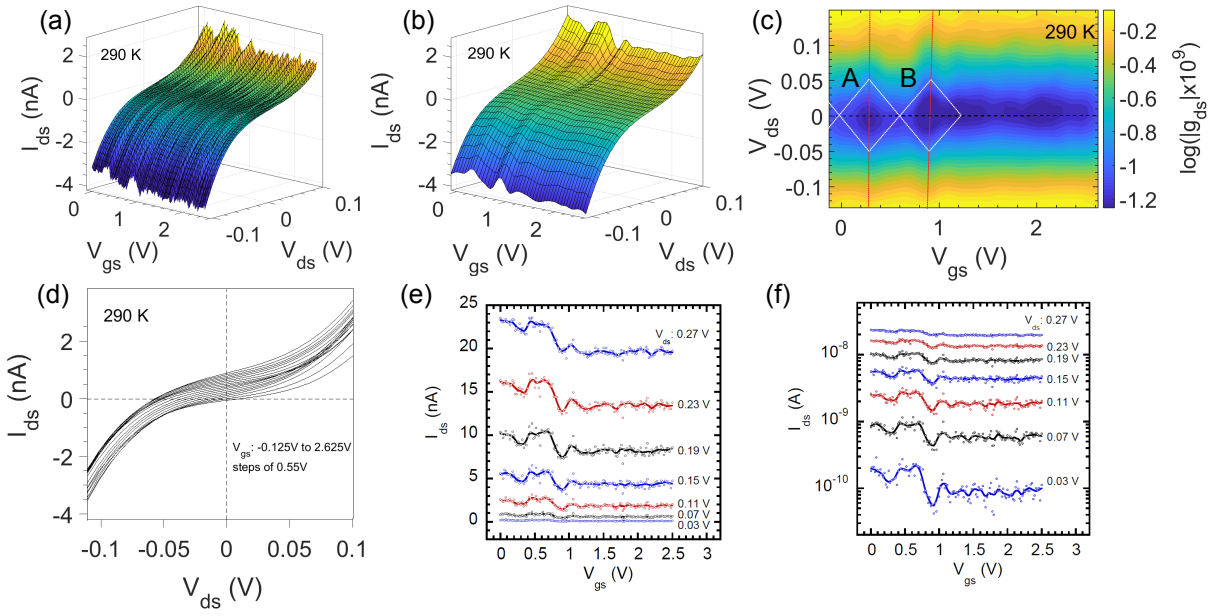

Figure 3. Room temperature electrical characteristics of a ~20 nm nanodot device (Device A). (a) A 3-D plot showing I_{ds} as a function of V_{ds} and V_{gs}. (b) Data of (a) re-plotted following an averaged, thin-plate spline fit, to show more clearly the oscillation of I_{ds} vs. V_{gs}. (c) Log $|g_{ds}|$, plotted using a linear colour scale, as a function of V_{ds} and V_{gs} and showing two diamond-like regions highlighted in white. (d) A 2-D plot of I_{ds} as a function V_{ds}, for values of V_{gs} from -0.125 V to 2.625 V, in steps of 0.55 V superimposed. Curves are offset from each other for clarity. (e) I_{ds} as a function of V_{gs} at 7 values of V_{ds}, from 0.03 V to 0.27 V. (f) Data of (e) re-plotted using a log scale for I_{ds}, to highlight current oscillations at the lowest V_{ds} values.

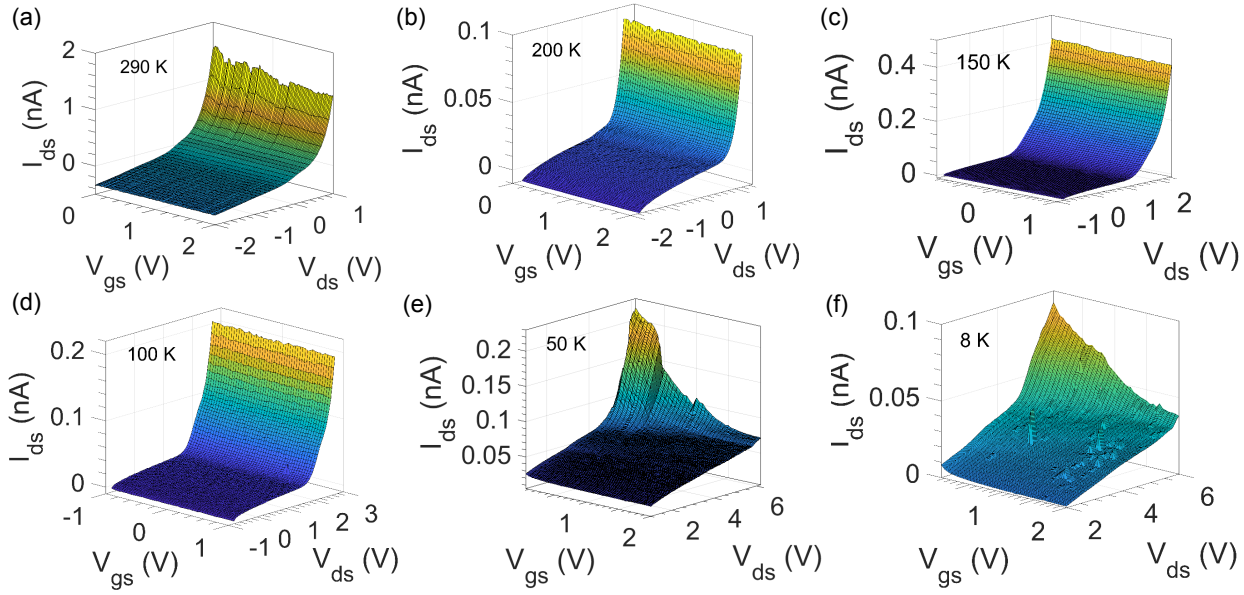

Figure 4. I_{ds} vs. V_{ds} and V_{gs} electrical characteristics of a nanodot/nanowire device (Device B), measured from (a) room temperature dependence through (b) 200 K, (c) 150 K, (d) 100 K, (e) 50 K and (f) 8 K.

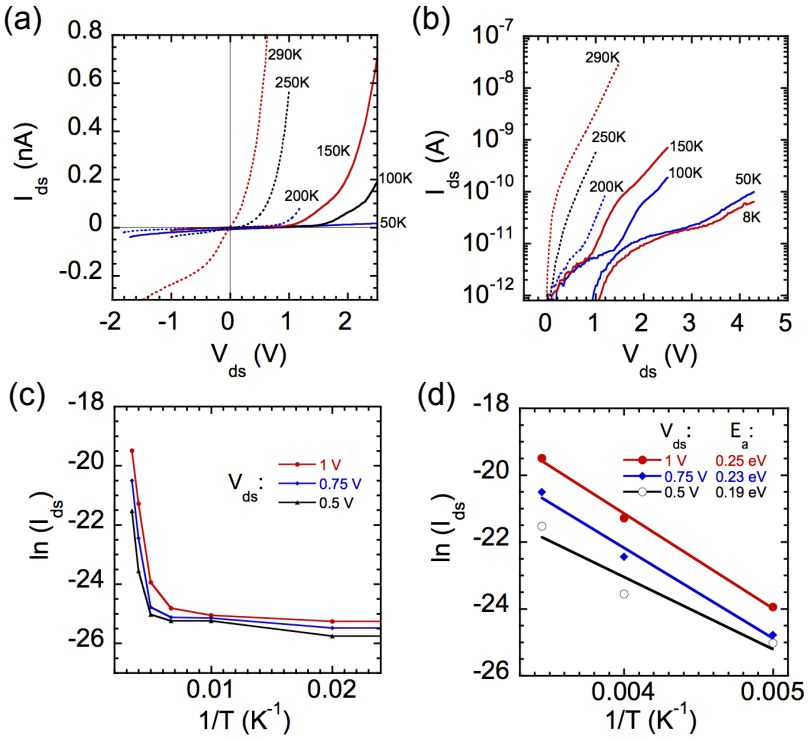

Figure 5. Electrical characteristics of Device B. (a) I_{ds} as a function of V_{ds} at V_{gs} = 0 V, for temperatures from 290 – 50 K. (b) Re-plot of (a) with I_{ds} displayed on a log scale. (c) Arrhenius plot of log $|I_{ds}|$ vs. $1/T$ for three values of V_{ds}, 0.5, 0.75 and 1 V. (d) Arrhenius plot for the higher temperatures (290 – 200 K), enabling activation energies of 0.19 – 0.25 eV to be extracted.

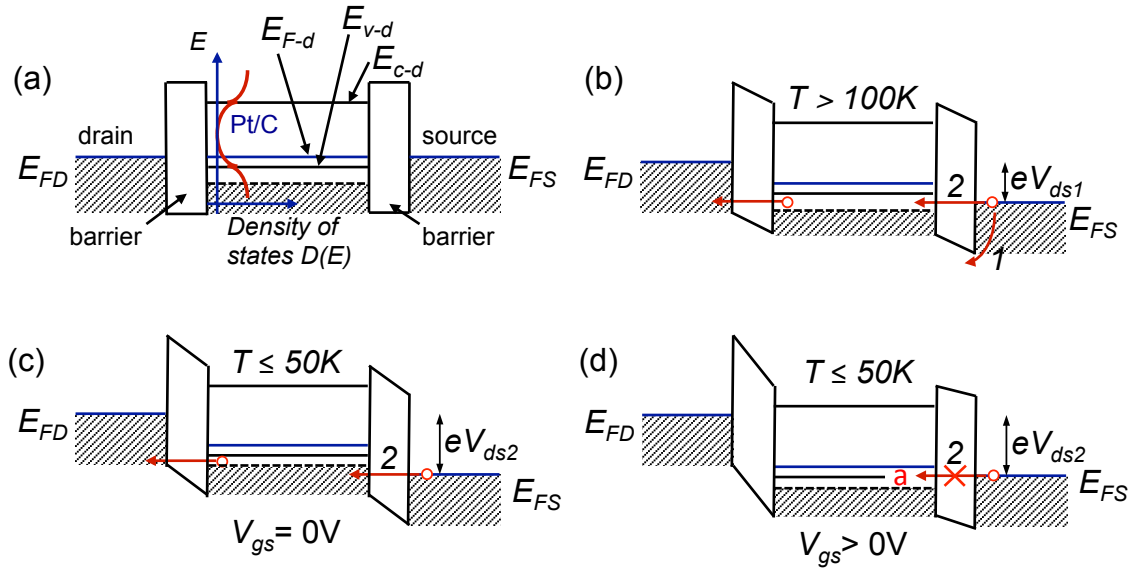

Figure 6. Schematic band diagrams for the Pt/C nanowire/Si point contact device, at various temperature and bias. (a) Band diagram at zero bias. Fermi seas are shown in the heavily doped Si source and drain contacts and a *p*-type semiconductor is assumed for the Pt/C deposit (see main text). Here, the diagonally shaded regions represent filled electronic states. In the Pt/C, the *p*-type nature implies that empty (hole) states exist between $E_{v\text{-}d}$ and the highest energy filled states (dashed line). The density of states $D(E)$ in the Pt/C is also shown schematically (red line). Potential barriers exist at the deposit/Si interfaces. (b) Bands at $T > 100$ K, with application of a drain-source bias V_{ds1}.A thermally activated (path '1') and a tunnelling (path '2') current path exist. (c) Band at T ≤ 50 K, with application of an increased drain-source bias V_{ds2} to obtain the same current as for (b). (d) Band at T ≤ 50 K, with application of drain-source bias V_{ds2} and gate bias $V_{gs} > 0$ V.

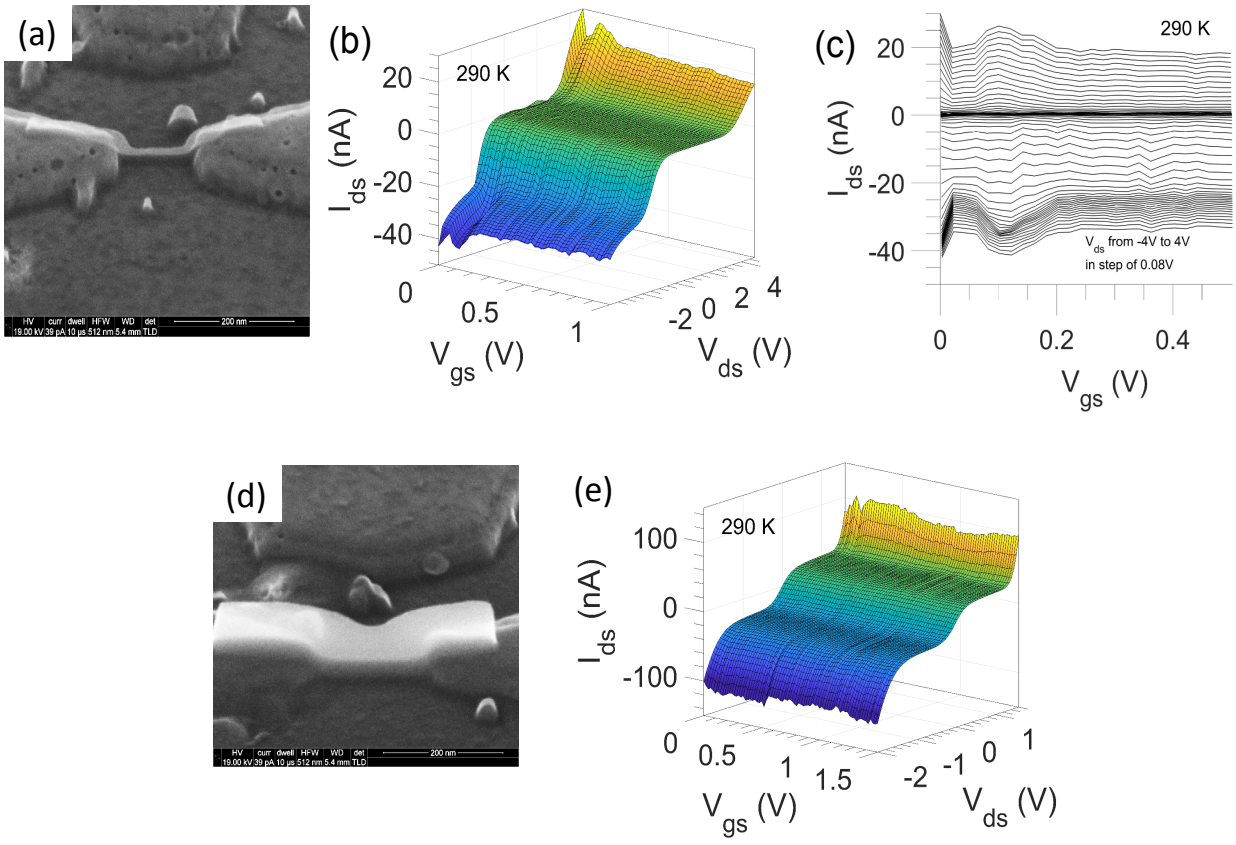

Figure 7. SEM images and electrical characteristics for two further types of structures, Device C (a – c) and Device D (d – e). (a) SEM image of Device C, a nanowire with a width of ~ 12.5 nm (b) I_{ds} vs. V_{ds} and V_{gs} electrical characteristics at 290 K. (c) I_{ds} plotted as a function of V_{gs} for Device C, for selected values of V_{ds}, from -4 V to +4V. A single peak in I_{ds} is observed for low $V_{gs} < 0.2$ V. (d) SEM image of Device D, a thick and wide nanowire. (e) I_{ds} vs. V_{ds} and V_{gs} electrical characteristics at 290 K.