Delta-Sigma Control Loop For Energy-Efficient Electrical Stimulation with Arbitrary-Shape Stimuli

Rashidi, Amin; Rivandi, Hassan; Grubor, Miloš; Agostinho, Andre ; Sadio, Valter ; Santos, Marcelino ; Serdijn, Wouter; Giagka, Vasiliki

DOI
10.1109/BioCAS58349.2023.10388625

Publication date
2023

Document Version
Final published version

Published in
Proceedings of the 2023 IEEE Biomedical Circuits and Systems Conference (BioCAS)

2023 IEEE Biomedical Circuits and Systems Conference (BioCAS) | 979-8-3503-0026-0/23/$31.00 ©2023 IEEE | DOI: 10.1109/BioCAS58349.2023.10388625

Delta-Sigma Control Loop For Energy-Efficient Electrical Stimulation with Arbitrary-Shape Stimuli

Amin Rashidi*†, Hassan Rivandi*, Miloš Grubor*, André Agostinho‡, Valter Sádio‡, Marcelino Santos ‡, Wouter Serdijn*, and Vasiliki Giagka*§
*Dept. of Microelectronics, Delft University of Technology, Delft, The Netherlands
†imec The Netherlands, Eindhoven
‡Silicongate, Lisbon, Portugal
§Fraunhofer Institute for Reliability and Microintegration IZM, Berlin, Germany
Email: a.rashidi@ieee.org, v.giagka@tudelft.nl

***Abstract*—This paper presents a novel multi-channel stimulation backend with a multi-bit delta-sigma control loop, which enables precise adjustment of the stimulation current through modulation of the supply voltage. This minimizes the overhead voltage of series circuitry to the stimulation load and avoids the associated energy loss. Additionally, to address the bandwidth limitations commonly encountered in battery-less implants, we propose incorporating amplitude and duration scaling of the arbitrary stimulation waveform. The waveform is programmable with 64 7-bit samples and 4 scaling factors per channel, resulting in a minimum of 68% data reduction per channel compared to using the waveform without scaling. The proposed circuits are designed and simulated in 180nm BCD technology occupying a total silicon area of 9mm^2. The fully integrated backend has a minimum compliance voltage of 8.5V and features a switched-capacitor multi-output DC-DC converter (MODDC) with pulse-skipping capability, a CMOS-only high-voltage (HV) multiplexer, and a unique HV H-bridge. Programming a sine-wave stimulus with a 4mA amplitude and a duration of 256μs achieved a signal-to-noise ratio of 40dB within a 10kHz bandwidth. For the same waveform, power efficiencies of 94% and 68% were observed without and with MODDC, respectively. Additionally, when programming constant-current stimuli ranging from 0.26mA to 4mA, high efficiencies of 78-97% and 23-79.4% were achieved without and with MODDC, respectively.**

***Index Terms*—Electrical stimulation back-end, Delta-sigma control loop, power efficiency, arbitrary waveform**

I. Introduction

In recent years, neurostimulator implants have made significant advancements in the treatment of neural disorders. However, to overcome the critical limitations and safety concerns associated with employing batteries [1], there is a growing focus on employing wireless powering methods for neurostimulators [2]–[6]. This poses challenges related to permissible power consumption and data communication bandwidth for some wireless implants.

Electrical neurostimulators commonly employ voltage-mode stimulation (VMS) or current-mode stimulation (CMS) methods to activate neural tissue, prioritizing either higher efficiency or increased safety, respectively. In a CMS back-end, the supply-voltage level needs to be designed high enough to leave a minimum overhead for the current driver in case of full-range stimuli and maximum electrode-tissue-interface (ETI) impedance. However, in cases where a lower supply level would be sufficient (i.e., for a lower current amplitude or ETI impedance), any excess voltage drop across the current driver leads to excess power dissipation. To address this concern, several supply voltage scaling methods have been proposed in the literature [7]–[15]. Notably, in [8] and [7], the supply voltage level is modulated to achieve a controlled current and eliminate the need for current drivers. However, both of these works are based on inductive converters and thus require external components, and have no/limited support for multi-channel scenarios and arbitrary stimulation waveforms.

This work was supported by the Electronic Components and Systems for European Leadership (ECSEL) Joint Undertaking Project Moore4Medical under Grant H2020-ECSEL-2019IA-876190.

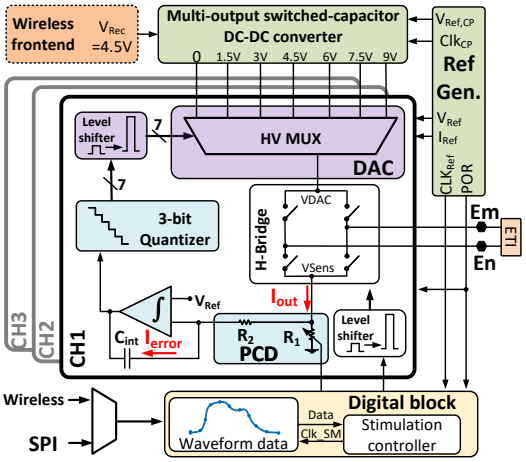

Fig. 1: Block diagram of the proposed Delta Sigma Loop.

Multiple studies have shown that using non-rectangular waveforms can enhance the selectivity, efficacy, and energy efficiency of the stimulation [16]–[20]. However, these advantages come with the trade-off of increased complexity and a larger amount of programming data. In this work, we propose an energy-efficient and bandwidth-aware stimulation back-end utilizing a novel delta-sigma loop ($\Delta\Sigma$L). It achieves a peak efficiency of 80% while providing precise current control, multi-channel capability, and arbitrary-waveform support.

II. System Architecture

Fig. 1 depicts the block diagram of the proposed 3-channel stimulation backend. A rectified voltage (V_{REC} = 4.5V) generated by a wireless front-end is input to a multi-output DC-DC converter (MODDC) to produce 6 supply rails. The

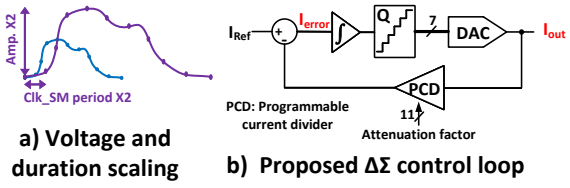

Fig. 2: Proposed a) scaling method b) Delta Sigma Loop.

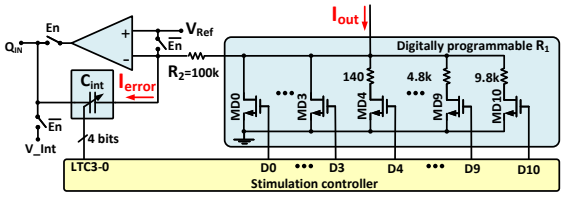

Fig. 3: Schematic diagram of the sensing circuits.

MODDC is shared among all channels and supports energy saving in multi-channel scenarios, as detailed in [9], [10]. A reference-generator circuit generates essential reference, clock, and power-on-reset (POR) signals required by other blocks. Configuration data including the arbitrary waveform can be programmed via SPI or wireless data demodulators. To accommodate bandwidth limitations encountered in the majority of battery-less implants, the arbitrary waveform is programmed with only 64 7-bit samples, utilizing voltage and duration scaling to adjust the stimuli amplitude and duration (Fig. 2(a)). Voltage scaling involves multiplying each waveform sample by 4-bit gain factors, programmable for the cathodic and anodic phases of each channel. Duration scaling is achieved by modifying the access time to waveform registers through changes in the period of the associated clock signal (clk_SM). The proposed voltage scaling eliminates the need for 11-bit samples to achieve 7-bit resolution for the smallest amplitude, resulting in a 36% reduction in required data. Additionally, reusing the same waveform for both cathodic and anodic phases, possibly with different scaling factors further reduces the required data by at least 50%. As a result, a minimum data reduction of 68% per channel can be achieved.

To minimize the overhead voltage of the current-driver circuitry and the associated power loss, a novel ΔΣL is proposed in this work. Fig. 2 (b) depicts a simplified block diagram of the proposed ΔΣL while a more detailed circuit implementation of it is shown in Fig. 1. The stimulation output current (I_{out}) is sensed and attenuated using a programmable current divider (PCD) for comparison with a reference current (I_{Ref}) to detect any potential current error (I_{error}). This error is then integrated over time, quantized, and used to adjust I_{out} through a 7-level digital-to-analog converter (DAC). The DAC is implemented using a high voltage (HV) multiplexer that connects one of the MODDC outputs to the ETI, in a pulse-density modulated format. The Signal and Noise Transfer Functions of the loop can be formulated as $STF = \omega_p/(s+\omega_p)$, and $NTF = s/(s+\omega_p)$, respectively, where ω_p is the integrator's pole. $\omega_p = 1/(2\pi \times R_2 \times C_{\rm int})$ is defined by R_2 and the integrator's capacitor, $C_{\rm int}$. Therefore, by designing ω_p at least 3 times higher than the bandwidth of the target neurons, it doesn't affect the stimuli while the noise will be filtered out by the neuron [21]. By analyzing Fig. 2(b), and by assuming $R_2 \gg (R_1||Z_{\rm ETI})$, I_{error} becomes:

$$I_{error} = \frac{R_1 \times I_{\rm out} - V_{\rm Ref}}{R_2} = \frac{R_1}{R_2} I_{\rm out} - \frac{V_{\rm Ref}}{R_2} \qquad (1)$$

where $V_{\rm ref}$ is a reference voltage at the positive terminal of the integrator. Thus, the attenuation factor and $I_{\rm ref}$ are equal to R_1/R_2 and $V_{\rm ref}/R_2$, respectively. In the steady state that $I_{\rm error}$ is zero, $I_{\rm out}$ can be calculated as:

$$I_{\rm out} = \frac{R_2}{R_1} I_{\rm Ref} = \frac{V_{\rm Ref}}{R_1} \qquad (2)$$

Hence, $I_{\rm out}$ is dependent on $V_{\rm Ref}$ and R_1. According to (2), the average voltage across R_1 is equal to $R_1 \times I_{\rm out} = V_{\rm Ref}$. Consequently, a smaller $V_{\rm Ref}$ reduces power loss across the sensing resistor. However, in order to relax the integrator design, $V_{\rm Ref}$ is chosen to be significantly higher than the offset and noise of a basic integrator. Still, off-chip tuning of $V_{\rm Ref}$ is implemented to compensate for possible offset. Finally, the PCD assists in reducing $C_{\rm int}$ by attenuating the sensed current.

III. Circuit Implementation

A. Sensing and Quantization Circuits

As formulated in Equation (2), $I_{\rm out}$ can be programmed by configuring R_1. The equation can be equivalently expressed as $I_{\rm out} = V_{\rm Ref} \times G_1$, where G_1 represents the conductance of R_1. For binary programming of $I_{\rm out}$, R_1 is implemented in 11 branches with binary-weighted conductances, as shown in Fig. 3. The smaller conductances are implemented using high-density poly-resistors in series with NMOS switches (MD4-MD10), while the bigger conductances are implemented by sizing the NMOS transistors (MD3-MD0) with a specific triode resistance when driven by the 1.8V digital level. The lengths of all the transistors as well as the segment width of poly-resistors are chosen well bigger than their minimum value to decrease their sensitivity to process variations. A PMOS-input 2-stage amplifier is employed in the integrator, and $C_{\rm int}$ is designed with a 4-bit binary-weighted capacitive bank to enable programming of ω_p. When the stimulator is not enabled (i.e., not in either of the cathodic or anodic phases), the amplifier's output disconnects from $C_{\rm int}$, and $C_{\rm int}$ is charged to an initial voltage level. The integrator is followed by a 3-bit quantizer that is implemented using a flash analog-to-digital converter (ADC).

B. High-Voltage DAC and H-Bridge

In the proposed ΔΣL, the DAC is implemented using a high-voltage multiplexer that connects pre-generated supply rails to the stimulation load based on the quantizer's outputs (D0-D2). To avoid using bulky DMOS transistors, two-step multiplexing is proposed in this work, as depicted in Fig. 4 (a). In the first step, the LS-MUX and HS-MUX multiplexers in Fig. 4 are controlled by D0 and D1 to connect one of 4 lower supply rails to VDL and one of 4 higher supply rails

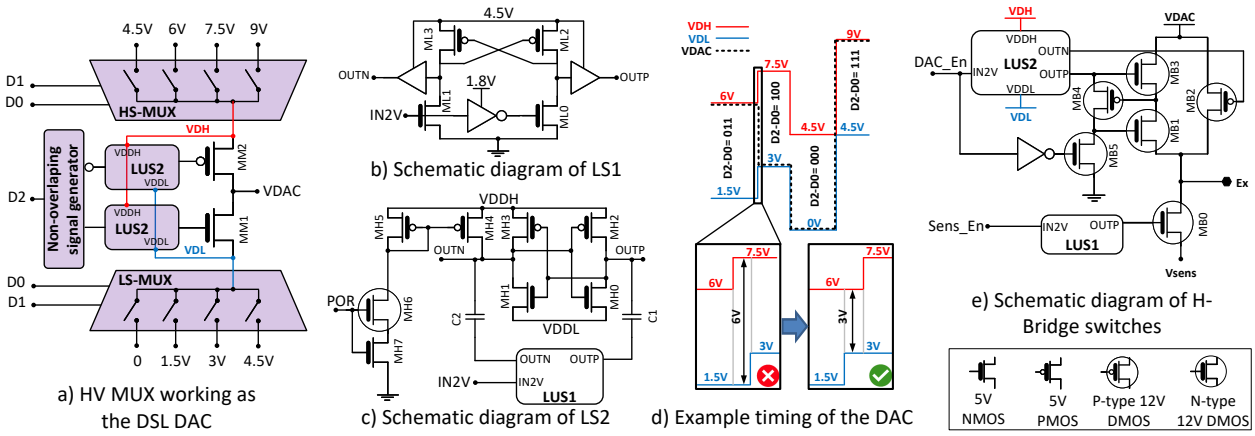

Fig. 4: Schematic and timing diagram of high-voltage DAC and H-bridge. The bulk of all the transistors in this figure are connected to their gates. An N+ buried layer is used for isolating the substrate of the NMOS devices when needed.

to VDH. As a result, a 4.5V supply ribbon (SR) is generated between VDH and VDL. In the second step, controlled by D2, transistors MM1 and MM2 and their driving circuits realize another 2-to-1 multiplexer that operates within the 4.5V SR and delivers either VDL or VDH to the VDAC node. This way, none of the switching transistors experience a differential voltage greater than 4.5V and can thus be implemented by 5V CMOS devices. To prevent short currents between VDH and VDL during D2 transitions, a non-overlapping signal generator with a 5-ns dead time is employed. All the switches in the LS-MUX and HS-MUX are transmission gates (TGs) driven by level shifters LS1 (Fig. 4(b)) and LS2 (Fig. 4(c)), respectively. LS1 is a conventional P-latch level-up shifter designed to shift the 1.8V logic level (IN2V) to 4.5V. LS2 is designed based on the capacitive-coupled floating level shifter to shift 1.8V and zero logic levels to VDDH and VDDL, respectively [22]. In Fig. 4(c), MH0-MH4 represents back-to-back inverters that latch digital data between VDDH and VDDL levels. The latch status changes at the INV2 edges, due to the high-pass characteristic of C1 and C2. However, due to the 4.5V separation between VDDH and VDDL, LS1 shifts IN2V to the 4.5V level first. Without a start-up circuit, the initial status of LS2 is determined by noise or mismatch. Thus, during the start-up phase, MH4-MH7 pull up the negative output, OUTN, to VDDH.

Fig. 4(d) shows the importance of timing synchronization between LS-MUX and HS-MUX. In this figure, an example of the VDH, VDL, and VDAC levels for digital inputs D2-D0=$\{011,100,000,111\}$ is illustrated. At the bottom of this figure, it can be observed that if VDL switches later than VDH during the SR's rising edges, there will be a brief moment that VDH - VDL $> 5V$ which overstresses transistors MM1 and MM2 and their driving LS2s. To address this issue, a digital circuit is designed to detect whether the D2-D0 inputs are increasing or decreasing at each switching time and accordingly apply a 10ns delay to the D1-D0 inputs of either LS-MUX or HS-MUX. Consequently, for the SR's rising and falling edges, VDH and VDL are delayed, respectively.

The schematic diagram of the switches implemented in the H-Bridge is shown in Fig. 4(e). Each electrode connected to the H-Bridge is either linked to the sensing circuits (Vsense) or to the output of the $\Delta\Sigma$L's DAC (VDAC). As Vsense operates at a small voltage level, a single N-type DMOS, MB0, driven by a LS1 can be used as the switch between the electrode and Vsense. However, A typical TG cannot be used as a switch between VDAC and the electrode due to the varying voltage levels at VDAC, which range from 0V to 9V. This is because the gate-source voltage limitation of DMOS devices, usually 5V, can lead to device breakdown. In this work, a novel transmission gate is designed that can handle this range of input signals with zero quiescent current consumption by leveraging the VDH and VDL signals generated in the first stage of the DAC circuit. To this end, an LS2 circuit adjusts the levels of the input control signal (DAC_En) to match VDH and VDL. Thus, when VDAC is between 4.5 and 9V (connected to VDH), VDL=VDAC-4.5V or VDH=VDAC appears at the gate of MB2 to close or open the switch between VDAC and the electrode, respectively. When VDAC is between 0 and 4.5V (connected to VDL), MB3-MB5 are responsible for the desired switching functionality. Specifically, for closing the switch, the gate of MB3 is driven by VDH = VDAC + 4.5V, causing MB3 to turn on and charge the gate of MB4 to the VDAC level. Subsequently, MB4 turns on with $V_{GS} = \mathrm{VDAC} - \mathrm{VDL} = 4.5\mathrm{V}$. Similarly, MB4 charges the gate of MB1 to VDL until MB1 also turns on, thereby connecting VDAC to the electrode. At the end of each stimulation pulse, passive charge balancing is carried out by driving MB0 connected to both electrodes.

C. Multi-output DC-DC converter

Fig. 5 illustrates the schematic diagram of the proposed MODDC that generates 6 fixed-ratio outputs, both below and above the $4.5\,\mathrm{V}$ input voltage. The 6 voltage rails at $1.5\,\mathrm{V}$, $3\,\mathrm{V}$, $4.5\,\mathrm{V}$, $6\,\mathrm{V}$, $7.5\,\mathrm{V}$, $9\,\mathrm{V}$ voltage levels are generated using one bulk and two boost switched-capacitor converters. A high switching frequency of $24\,\mathrm{MHz}$ and interleaving methods reduce the required capacitance values and allow on-chip implementation of the flying (C_f) and output capacitors (C_o).

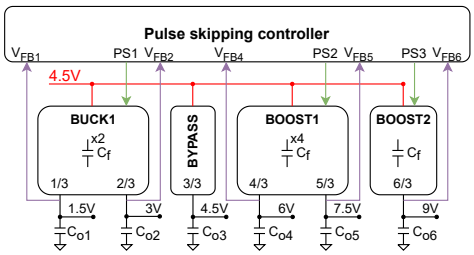

Fig. 5: Top-level block diagram of the DC-DC converter.

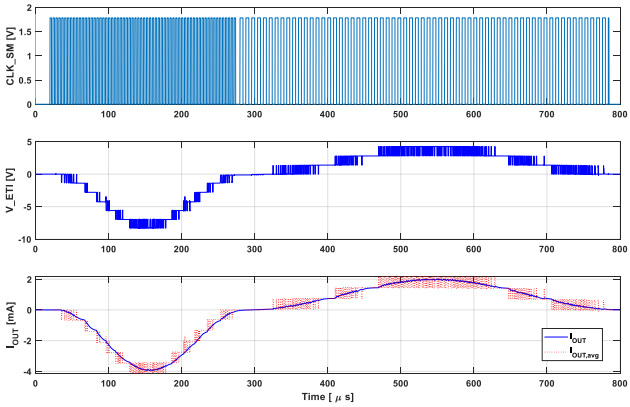

Fig. 6: transient simulation results for an asymmetric stimulus

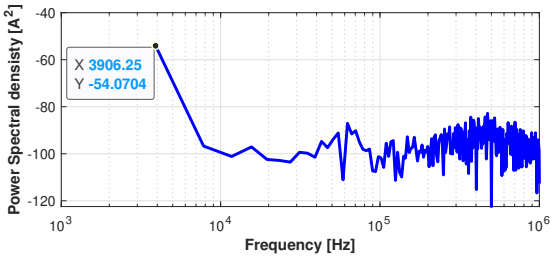

Fig. 7: Power spectral density for the sine stimulation current.

Each rail is capable of sourcing up to $4\,\mathrm{mA}$ current with a voltage drop below $5\,\%$ of the ideal voltage level. All stages, including the bypass stage, provide over-current protection and soft-start features. To reduce the switching losses caused by the high parasitic capacitance of the integrated capacitors, the parasitic charge-sharing scheme proposed in [23] is adopted. To increase the power-conversion efficiency at light loads, a pulse-skipping regulation scheme is implemented for each stage. The pulse-skipping controller senses the output voltages through the V_{FBx} signals and blocks the charge pumping clock, using the PSx signals, when the output level reaches a fixed portion of the ideal ratio ($96\,\%$).

IV. Results

The proposed stimulation backend is designed and simulated in TSMC 180nm bipolar-CMOS-DMOS (BCD) technology and occupies a total area of $9\mathrm{mm}^2$ including pads.

Fig. 6 showcases the results of a transient simulation using an asymmetric biphasic stimulus with a sine waveform as the programmed arbitrary waveform. To initiate from zero, the programmed sine wave incorporates a DC offset equal to half of its amplitude and a phase shift of 270 degrees. The cathodic phase is programmed with a full range current

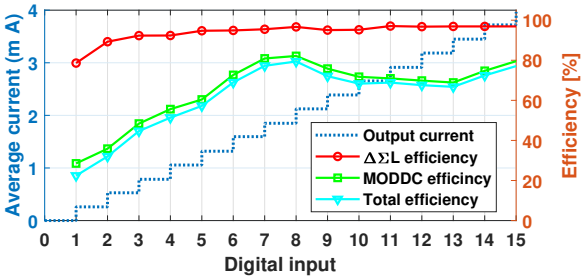

Fig. 8: Average I_{OUT} and efficiencies for constant current.

TABLE I: Summary of Specifications and Comparison

characteristics	This Work	TBCAS'19 [8]	TBCAS'11 [7]
Technology (nm)	180 BCD	180 HV	350
Voltage scaling method	ΔΣL + MODDC	Ultra high frequency pulsed	Inductive DC-DC converter
Max. efficiency	80.5%	68 %	35-50 %
Arbitrary waveform	Yes	No	No
External components	No	Yes	Yes
Efficient multi-channel	MODDC [9]	with TDM	No
Stimulation current	≤4mA	≤10 mA	≤0.45 mA
Compliance voltage	8.5 V	3.5 V	3.3 V
Verification	Simulation	Measurement	Measurement

amplitude lasting $256\mu s$, whereas the anodic phase is half in amplitude and double in duration. The figure from top to bottom illustrates the state clk_SM, the voltage over the ETI (V_{ETI}), and the stimulation current (I_{out}). Additionally, the bottom plot includes a low-pass filtered version of the stimulation current, with a provisional bandwidth matching that of the target neuron (10kHz). Fig. 7 depicts the power spectral density of the stimulation current during the cathodic phase. The plot reveals that the modulation noise can be effectively filtered out by the neuron's bandwidth. As a result, a signal-to-noise ratio (SNR) of 40dB which is equivalent to an effective number of bits (ENOB) of 6.2 bits has been calculated for the bandwidth of 10 kHz. For this waveform, the simulated efficiency of the DSL, MODDC, and all circuits are determined to be 94%, 72%, and 68% respectively.

Fig. 8 illustrates the simulation results for the average I_{out} level, and the circuit efficiencies when programming constant current waveforms with 4-bit resolution. Accordingly, The efficiency of the DSL and MODDC circuits falls within the range of 79-97% and 23-79.4% respectively. As a result, the overall peak efficiency of the entire stimulation backend is determined to be 79.4%

V. Conclusions

An energy-efficient and bandwidth-aware stimulation backend for arbitrary-waveform stimulation is reported. The proposed circuit benefits from a novel delta-sigma control loop, and a fully integrated MODDC for scaling the stimulator's supply level. This work shows peak efficiencies of 80.5% and 68% when programming constant current and sinusoidal waveforms, respectively. A summary of the specifications and a comparison table are presented in Table I.

REFERENCES

[1] E. W. Lau, "Technologies for prolonging cardiac implantable electronic device longevity," *Pacing and Clinical Electrophysiology*, vol. 40, no. 1, pp. 75–96, Dec. 2017.

[2] Y. Liu *et al.*, "Bidirectional bioelectronic interfaces: System design and circuit implications," *IEEE Solid-State Circuits Mag.*, vol. 12, no. 2, pp. 30–46, Jun. 2020.

[3] A. Rashidi, S. Hosseini, K. Laursen, and F. Moradi, "Stardust: Optogenetics, electrophysiology and pharmacology with an ultrasonically powered dust for parkinson's disease," in *2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. IEEE, 2019, pp. 109–110.

[4] A. Rashidi, M. Zamani, T. Mondal, S. Hosseini, K. Laursen, B. Corbet, and F. Moradi, "Ultrasonically powered and controlled microsystem for dual-wavelength optogenetics with a multi-load regulation scheme," *IEEE Solid-State Circuits Letters*, 2023.

[5] D. K. Piech, B. C. Johnson, K. Shen, M. M. Ghanbari, K. Y. Li, R. M. Neely, J. E. Kay, J. M. Carmena, M. M. Maharbiz, and R. Muller, "A wireless millimetre-scale implantable neural stimulator with ultrasonically powered bidirectional communication," *Nature biomedical engineering*, vol. 4, no. 2, pp. 207–222, 2020.

[6] H. Rivandi and T. L. Costa, "A 2d ultrasound phased-array transmitter asic for high-frequency us stimulation and powering," *IEEE Transactions on Biomedical Circuits and Systems*, 2023.

[7] S. K. Arfin and R. Sarpeshkar, "An energy-efficient, adiabatic electrode stimulator with inductive energy recycling and feedback current regulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 1, pp. 1–14, Otc. 2011.

[8] A. Urso, V. Giagka, M. van Dongen, and W. A. Serdijn, "An ultra high-frequency 8-channel neurostimulator circuit with 68% peak power efficiency," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 5, pp. 882–892, May 2019.

[9] A. Rashidi, N. Yazdani, and A. M. Sodagar, "Fully implantable, multi-channel microstimulator with tracking supply ribbon, multi-output charge pump and energy recovery," *IET Circuits Devices Syst.*, vol. 15, no. 2, pp. 104–120, Dec. 2021.

[10] K. Kolovou-Kouri, A. Rashidi, F. Varkevisser, W. A. Serdijn, and V. Giagka, "Energy savings of multi-channel neurostimulators with non-rectangular current-mode stimuli using multiple supply rails," in *Proc. Annu. Int. Conf. Eng. Med. Biol. (EMBC)*, Jul. 2022, pp. 3443–3446.

[11] X. Zeng *et al.*, "A 12-V single-input multiple-independently configurable-output dynamic voltage scaling supply in standard 0.18-μm CMOS for electrical stimulation applications," *IEEE Solid-State Circuits Let.*, vol. 5, pp. 33–36, Feb. 2022.

[12] M. W. Kim and J. J. Kim, "Energy-efficient fast-transient dynamic reconfigurable charge pump for multi-channel electrical stimulation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2022.

[13] A. Rashidi, N. Yazdani, and A. M. Sodagar, "Fully-implantable, multi-channel, microstimulator with tracking supply ribbon and energy recovery," in *2016 38th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*. IEEE, 2016, pp. 1818–1821.

[14] W. Ahn, K.-H. Nguyen, J. Lim, K. S. Min, H. Lee, S. Ha, and M. Je, "An energy-efficient, scalable neural stimulation ic with adaptive dynamic voltage switching for cochlear implant system," in *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2023, pp. 1–5.

[15] I. Williams and T. G. Constandinou, "An energy-efficient, dynamic voltage scaling neural stimulator for a proprioceptive prosthesis," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, no. 2, pp. 129–139, 2013.

[16] R. Collu, E. J. Earley, M. Barbaro, and M. Ortiz-Catalan, "Non-rectangular neurostimulation waveforms elicit varied sensation quality and perceptive fields on the hand," *Scientific Reports*, vol. 13, no. 1, p. 1588, Jan. 2023.

[17] S. Culaclii *et al.*, "A biomimetic, soc-based neural stimulator for novel arbitrary-waveform stimulation protocols," *Frontiers in Neuroscience*, vol. 15, p. 697731, Jul. 2021.

[18] Z. Gilbert *et al.*, "A review of neurophysiological effects and efficiency of waveform parameters in deep brain stimulation," *Clin. Neurophysiol.*, May 2023.

[19] T. J. Foutz and C. C. McIntyre, "Evaluation of novel stimulus waveforms for deep brain stimulation," *J. Neural Eng.*, vol. 7, no. 6, p. 066008, Nov. 2010.

[20] A. Rashidi, F. Varkevisser, V. Giagka, T. L. Costa, and W. A. Serdijn, "Low-cost shaping of electrical stimulation waveforms for bioelectronic medicine with improved efficiency and selectivity," in *9th Dutch Bio-Medical Engineering Conference*, 2023.

[21] F. Varkevisser, A. Rashidi, T. L. Costa, V. Giagka, and W. A. Serdijn, "Pre-filtering of stimuli for improved energy efficiency in electrical neural stimulation," in *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS)*, Nov. 2022, pp. 312–316.

[22] Z. Liu and H. Lee, "A 100V gate driver with sub-nanosecond-delay capacitive-coupled level shifting and dynamic timing control for ZVS-based synchronous power converters," in *Proc. Cust. Integr. Circuits Conf.*, Nov. 2013, pp. 1–4.

[23] A. Rashidi, N. Yazdani, and A. M. Sodagar, "Fully-integrated, high-efficiency, multi-output charge pump for high-density microstimulators," in *Proc. IEEE Life Sci. Conf. (LSC)*, Dec. 2018, pp. 291–294.