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Design of a Fan-Out Panel-Level SiC MOSFET Power Module Using Ant Colony Optimization-Back Propagation Neural Network

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***Abstract*— A new panel-level silicon carbide (SiC) metal oxide semiconductor field effect transistor (MOSFET) power module was developed by using the fan-out and embedded chip technologies. To achieve the more effective thermal management and higher reliability under thermal cycling, a new optimization method called Ant colony optimization-back propagation neural network (ACO-BPNN) was developed for optimizing SiC modules, and contrast it with the Response Surface Method (RSM). First, the heat dissipations of SiC MOSFET with different redistribution layer (RDL) materials were simulated through the ANSYS finite element simulation. Then, the RSM was adopted to design the experiments for optimization. Third, the optimized design considering both junction temperature and thermal-mechanical stress is obtained using RSM and ACO-BPNN. The results show that: 1) compared with nano-silver, copper has a relatively good heat dissipation effect, but nano-silver has a better thermodynamic performance, and 2) ACO-BPNN can provide more accurate optimization results without having to construct a fitness function like RSM. After optimization, the thermal management and the thermal-mechanical stress can be improved by about 3% and 11%, respectively.**

***Index Terms*— Ant colony algorithm, back propagation neural network (BPNN), embedded packaging, fan-out, response surface, SiC MOSFET.**

I. Introduction

With recent developments in power electronics technology, high-powered semiconductors have been widely used in electric vehicles, wind power generation, high-speed trains, smart grids, aerospace, and other applications. These recent developments have been geared toward producing high voltage and high power density [1]. Silicon (Si)-based power electronics have maximized their potential for applications that involve high temperature, high voltage, and high frequency. Silicon carbide (SiC)-based power electronics have been adopted because they are superior to Si-based power electronics in industrial applications that involve high temperature and high voltage.

SiC-based power electronics are superior to Si-based power electronics for the following reasons. SiC MOSFET has a lower threshold voltage and lower on-resistance at high temperatures, which results in superior forward voltage drop and low loss at high temperatures [2]. SiCs have higher voltage and lower switching loss per unit area, which makes them more suitable for application in traction converter systems and power transmission systems [3]. In addition, SiC has lower output capacitance and gate charge and can be switched at higher rates of change of voltage and current [4]. The high switching speed, low switching loss, and high switching frequency of SiC improve the power density and efficiency of power systems. The switching loss of Si insulated-gate bipolar transistors (IGBTs) increases significantly at higher temperatures; however, the switching loss of SiC MOSFETs only slightly changes at higher temperatures [5].

However, the application of SiC MOSFETs in power electronics is mainly limited by its inferior reliability [6], [7]. For instance, transient overloads and short circuits are more likely to occur in SiC MOSFETs than Si IGBTs due to the

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more compact die area and thinner gate oxide of SiC MOSFETs [8]. SiC MOSFET also experiences interlayer dielectric erosion, electrode layering, and time-dependent portal oxide breakdown if it operates long term at high temperatures. In addition, with increasing operating temperature and switching frequency, the long thermal cycle of SiC MOSFETs accelerates the stripping of wire bonding, solder cracks, and other parts.

Packaging can be used to enhance the reliability of SiC MOSFET power modules [9]. Aluminum wire bonding is preferred for packaging in traditional power modules. However, line-key connections limit the performance of SiC power modules by introducing parasitic inductance over 10 nH [10]. Switching at high rates of change of current leads to voltage overshoot and increases the switching loss of power modules. Traditional packaging materials (such as Tin-based lead-free solders) used in Si-based power modules are unable to withstand high temperatures exceeding 200 °C. This limits the application of traditional packaging materials in power modules for high-temperature applications. The growth of intermetallic compounds and formation of Kirkendall voids challenge the reliability of power modules. To avoid such growths and formations, sintered metallic nanoparticles have been proposed as potential interconnection layers for packaging high-powered electronics in the future [11].

Response surface methodology (RSM) using design of experiments (DOEs) is helpful in understanding and optimizing response variables [12], [13]. RSM is often used to improve models after important factors are determined using filter design or factor design. RSM is ideal when the number of independent variables is small, usually no more than three.

Ant colony optimization (ACO) is a probabilistic algorithm used to find optimal paths through graphs [14]. ACO was used for local weighted structural equation modeling in [15]. In [16], the parameters of isotherm and kinetic models were estimated using ACO, which did not affect the non-linearity of the models. The performance of the pre-processed ACO algorithm was analyzed based on visual quality, computation time, and its ability to preserve useful edges [17].

The traditional ACO method is as follows: multi-objective optimization algorithm and finite element method are combined to optimize the structure. It means that the fitness function value is calculated by the finite element analysis software in the optimization algorithm, which is fed back to the optimization algorithm for optimization. Finally, the optimization result is obtained. This method is relatively easy to implement for simple model or simulation, because its finite element simulation requires less calculation, shorter calculation time, and less computer space taken up by the calculation result. However, for some complex simulations that need cycling, the computing power of the existing computer is far from enough to meet the requirements of this method. Therefore, it is necessary to develop more efficient calculation instead of finite element simulation. The neural network algorithm can be trained to obtain more accurate prediction results, which can be used in the optimization algorithm.

This article studied the impact of chip location, redistribution layer (RDL) materials, and RDL thickness on embedded fan-out SiC MOSFET power modules during thermal cycling and heat dissipation. RSM and an ACO-back propagation neural network (ACO-BPNN) were used to optimize heat dissipation and stress distribution in the model of the embedded fan-out SiC MOSFET power module. The purpose of this article is to compare two methods, i.e., ACO-BPNN and RSM, to clarify the advantage of ACO-BPNN in optimization.

II. Finite Element Modeling and Simulation

The position of the SiC chip, RDL thickness, and RDL materials were considered in optimizing the packaging of embedded fan-out SiC MOSFET power modules [1]. The aim of optimization was to achieve the best thermodynamic performance without exceeding the maximum heat-resisting temperature of 300 °C [1]. Nano-silver is used to connect chips to substrates. However, Jing Qi, an Italian company, has developed electroplating technology for silver nanoparticles. Nano-silver is now being adopted for electrical interconnection layers [18].

A. SiC MOSFET and Phase-Leg Power Module

SiC MOSFET devices are manufactured from an N-drift layer growing on a heavily doped N+ substrate. The drift layer is sandwiched between the N+ substrate and the p-body to form a vertical volume diode. The body diode is a PiN diode and is anti-parallel with the SiC MOSFET channel. The foremost characteristic of PiN diode is in the turn-OFF transient where reverse recovery can be observed as a result of minority carrier extraction from the drift layer [19].

As is studied in [20], Fig. 1 shows the equivalent circuit model of the SiC MOSFET. It is described by an ideal MOSFET voltage-controlled current source, three parasitic capacitors, and an antiparallel diode. Parasitic capacitances of SiC MOSFET include gate–source capacitance (C_{GS}), drain–source capacitance (C_{DS}), and gate–drain capacitance (C_{GD}) [21]–[23]. C_{GS} consists of a constant overlap oxide capacitance between gate and source and a constant capacitance between gate and source metallization, which are in parallel. C_{DS} is the bias-dependent depletion capacitance of P-body/N-drift junction and is given by

$$C_{DS} = C_{DS0}\left(\frac{V_{bi}}{V_{bi} + V_{DS}}\right)^{M} \tag{1}$$

where C_{DS0} is a constant, V_{bi} is the built-in potential between P-body and N-drift junction, and M is a fitting parameter.

Fig. 2 shows a circuit diagram of phase-leg SiC MOSFET module, which consists of a high-side SiC MOSFET (HS-MOS) and a low-side SiC MOSFET (LS-MOS).

B. 3-D Modeling

We have described the MOSFET encapsulation process in detail in [20]. MOSFET packaging begins with producing a 0.18-mm core plate by compressing a 0.1-mm-thick layer of Bismaleimide–Triazine (BT) laminate, two 0.04-mm-thick layers of Bismaleimide–Triazine (BT) pre-preg, and two

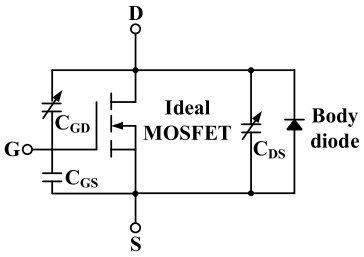

Fig. 1. Equivalent circuit model of the SiC MOSFET.

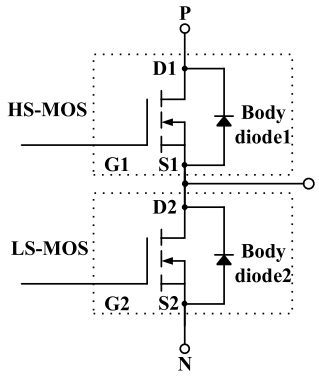

Fig. 2. Circuit diagram of phase-leg SiC MOSFET power module.

3-μm-thick layers of copper foil under high temperature and pressure. A mechanical drilling system is used to drill through the hole in the core plate to establish internal RDLs. The core plate is then attached to a layer of photo imageable dielectric (PID) and placed on a heating plate set to 60 °C. A SiC MOSFET is placed in the core plate through the hole and covered with another layer of PID. There is a gap of about 25 μm between the SiC MOSFET and the core plate. Due to the flow capacity of PID at high temperatures, the holes in the BT core plate and the gap between the SiC MOSFET and BT core plate are filled by PID.

Referring to previous research [20], a 3-D model of the embedded fan-out SiC MOSFET power module was created, as shown in Fig. 3(a). Referring to Fig. 3(d), the model consists of SiC MOSFET chip, BT pre-pregs, BT laminate, RDLs, and solder masks.

Metal has different elastic moduli at different temperatures; therefore, six different elastic moduli were assigned to the RDLs at temperatures of 233, 271, 309, 347, 385, and 423 K. Young's moduli of RDL materials, nano-silver, and copper at various temperatures were plotted in Fig. 4 [24].

C. Simulating Conditions and Properties of Materials

According to JEDEC JESD22-A106B standard [25], the thermal cycling simulation condition selected in this article is shown in Fig. 5. The temperature range is 233–423 K, which is stress-free. The conversion time from the high to the low temperature is 60 s, and the conversion speed can be estimated as 38 K/s. Five thermal cycles are calculated in this simulation. The properties of the materials used in the simulation of the thermal cycle are listed in Table I [26]–[28].

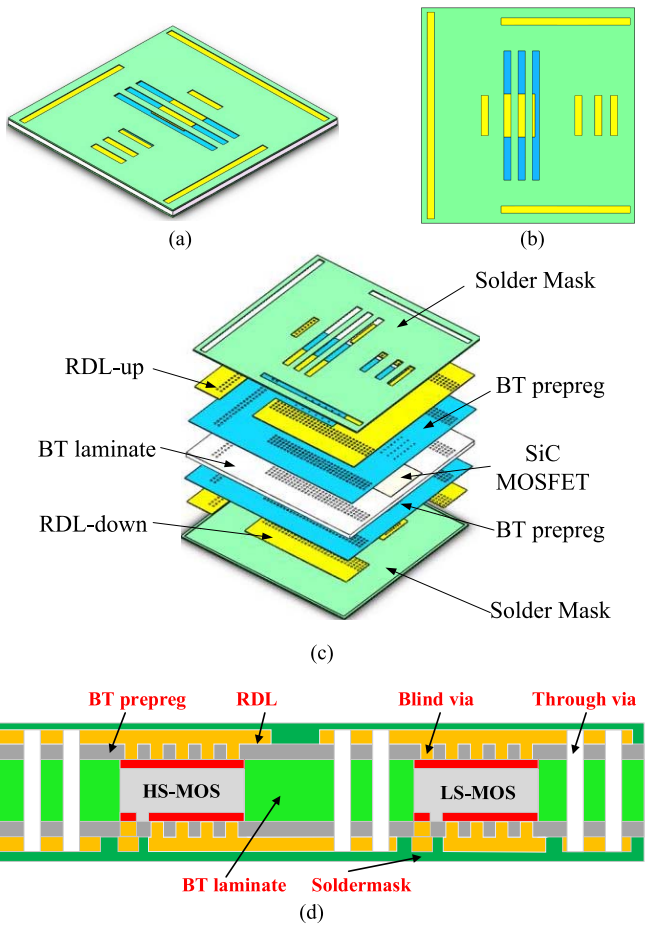

Fig. 3. (a) 3-D model of the fan-out panel-level SiC MOSFET power module. (b) Top views of the 3-D SiC module. (c) Components of the 3-D model of the embedded fan-out SiC MOSFET power module. (d) Cross-sectional views of the 3-D SiC module.

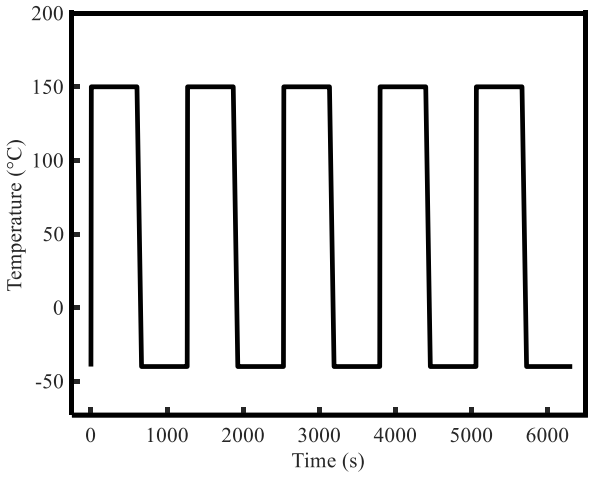

Fig. 4. Simulation condition of temperature during thermal cycling.

D. Range of Chip Location

The range of SiC MOSFET chip location is limited to the left through via, up through via, and down through via. The location of SiC MOSFET chips is also limited by chip size, RDL size, and solder mask. These limitations are illustrated in Fig. 6.

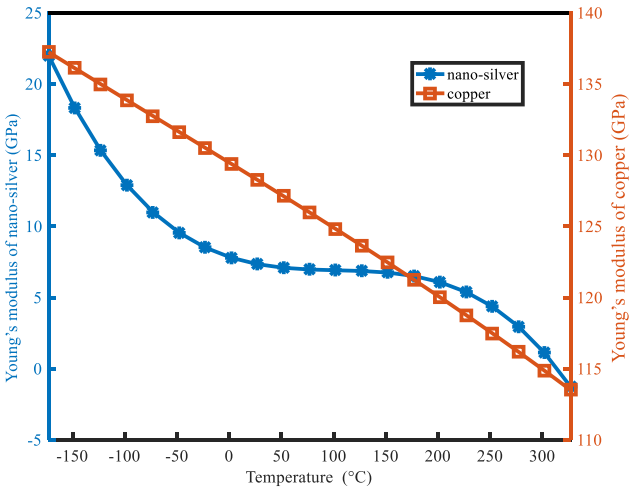

Fig. 5. Young's modulus of nano-silver and copper RDL materials at various temperatures.

TABLE I
PROPERTIES OF THE MATERIALS USED IN THE SIMULATION OF THE MODEL

Material	Modulus E (GPa)	Poisson ratio v	Coefficient of thermal expansion α (ppm/K	Thermal conductivity k (W/mK)
SiC MOSFET	400	0.142	5.1	150
BT pre-preg	24	0.38	6.9	0.8
BT laminate	24	0.38	5.3	0.8
Nano-Ag	See Figure	0.37	19.6	238
Cu	See Figure	0.36	17	390

The range of SiC MOSFET chip location in the x- and y-directions is given by the following equations:

$$l_x = L - a - b - e - 0.1 \tag{2}$$

$$l_y = L - c \cdot 2 - e - 0.1 \times 2 \tag{3}$$

where L is the length of the power module, while a, b, c, and e are different limitations labeled in Fig. 6.

Consider two chips that are centrally symmetric at the center point of the range of possible chip locations. The corresponding coordinate system is shown in Fig. 7.

Consider the center of the chip on the right of Fig. 7. The two chips are centered symmetrically relative to the origin, and the distance between both chips is 0.2 mm.

Thus, the range of possible SiC MOSFET chip positions was determined using the following equation:

$$x_r \in [2 \text{ mm}, 4.45 \text{ mm}]$$
$$y_r \in [-2.5 \text{ mm}, 2.5 \text{ mm}] \tag{4}$$

where x_r is the x-coordinate of the chip on the right side of Fig. 7, and y_r is the y-coordinate of the chip on the left side of Fig. 7.

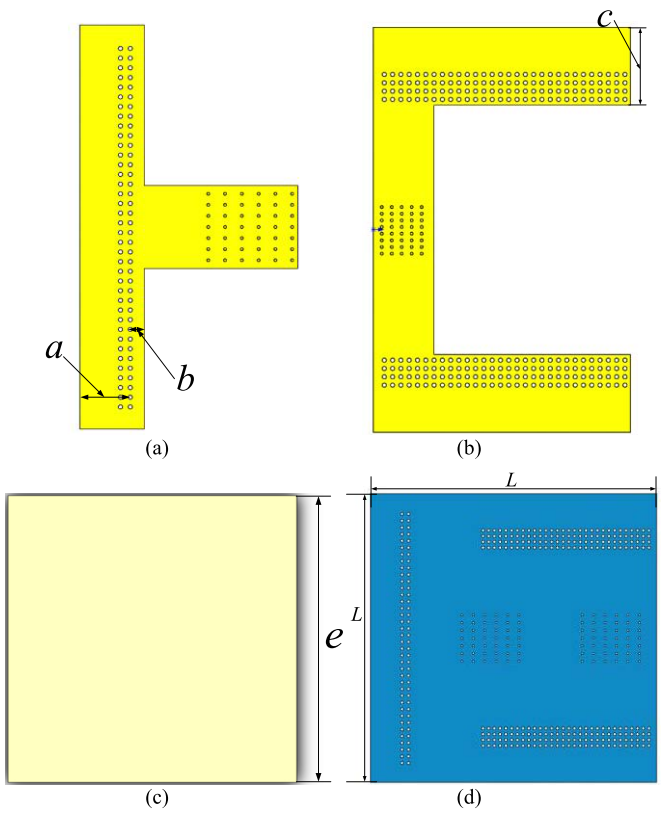

Fig. 6. (a) RDL limitation in the x-direction. (b) RDL limitation in the y-direction. (c) Size of the chip. (d) Size of the power module.

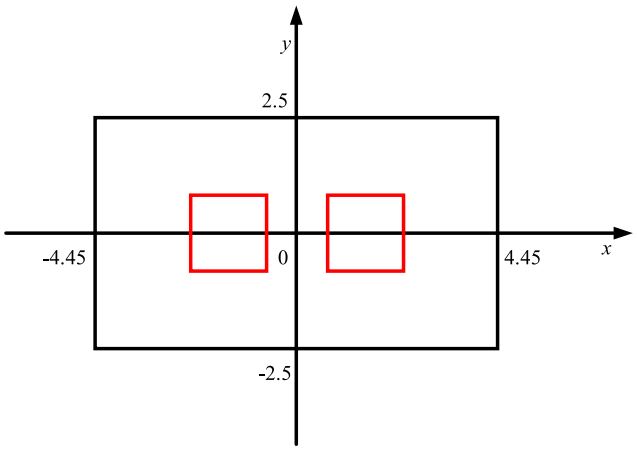

Fig. 7. Coordinate system of two chips centrally symmetric at the center point of the range of possible chip locations.

E. Thermal Simulation

The internal thermal conduction structure of the package module has been described in detail in [20].

In the thermal simulation, two SiC MOSFET chips are set as heat sources, whose power losses are 103.68 W. It is double-sided cooled, and its convective heat transfer coefficient is set as 15 W/m^2·°C, and the initial temperature is 25 °C. The simulation results of heat dissipation in embedded fan-out SiC MOSFET power modules with RDL materials of nano-silver and copper are shown in Fig. 8(a) and (b),

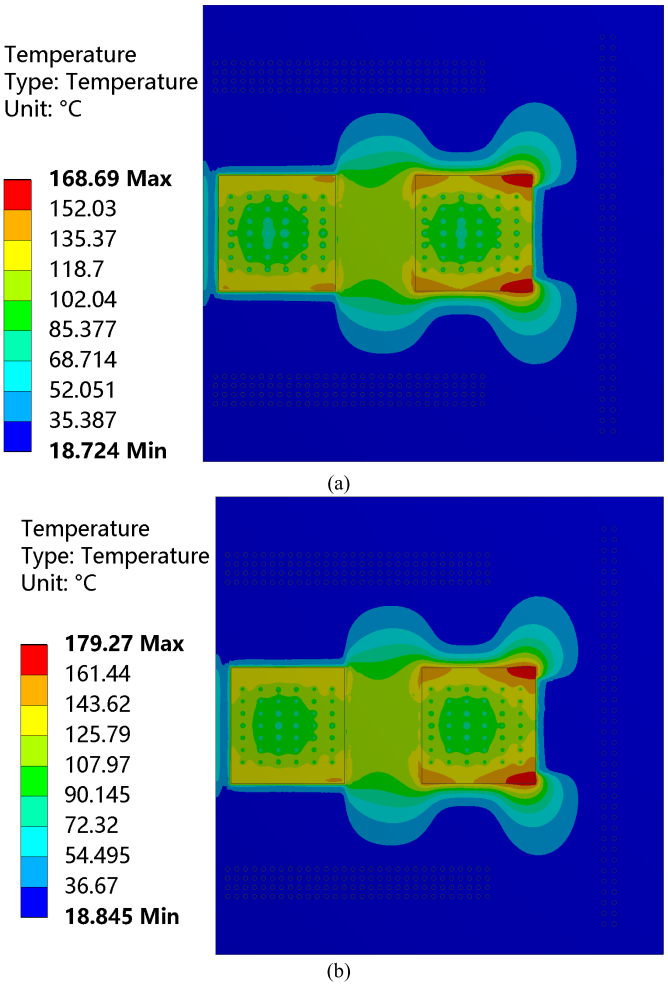

Fig. 8. Simulation of heat dissipation in SiC MOSFET chips. (a) RDL with copper. (b) Nano-silver with RDL.

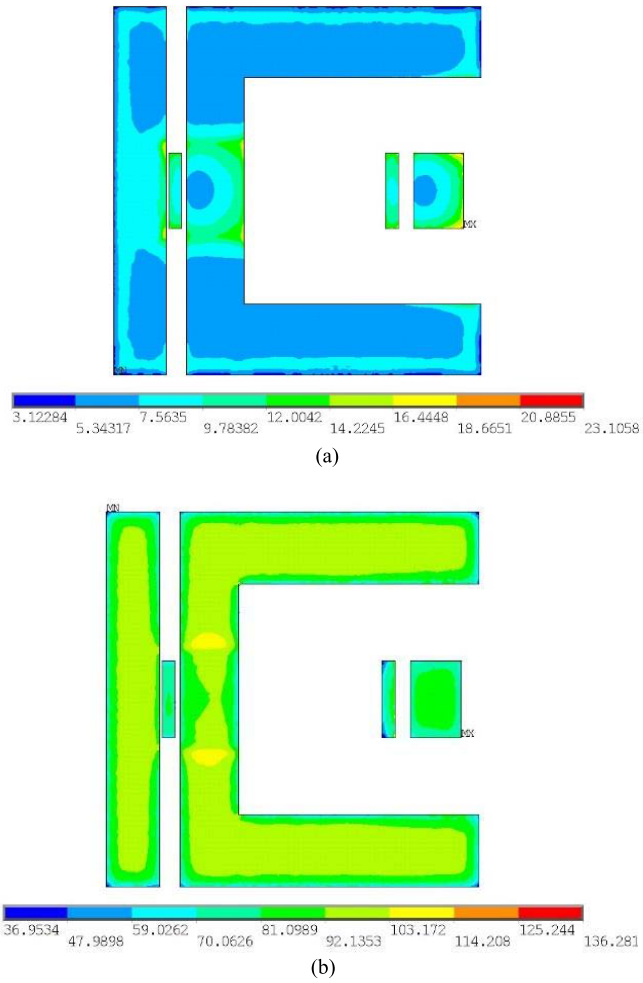

Fig. 9. Simulation of stress distribution in RDLs. (a) Nano-silver. (b) Copper.

respectively. Referring to Fig. 8, copper lowers working temperature from 179.27 °C to 168.69 °C compared with nano-silver. This decrease in temperature was due to the higher thermal conductivity of copper, and this temperature is significantly higher than the silicon chip maximum junction temperature 125 °C. Due to the high-temperature resistance of SiC chips, SiC MOSFET devices can work at high temperatures.

F. Thermo-Mechanical Simulation

The simulation results of stress distributions during thermal cycling in nano-silver and copper RDLs are shown in Fig. 9. Referring to Fig. 9, maximum stress occurs at the edges of the RDL. RDL is directly impacted by the heat because it is located directly below the SiC MOSFET chip. The thermal expansion coefficient of nano-silver and copper is different, which leads to interface stratification issues [29]. The thermal performance of nano-silver was much better than that of copper.

III. Optimization and Analysis

A. DOE

RSM with DOE is helpful in understanding and optimizing response variables. rms is often used to improve models after important factors have been identified through factor design. Considering the location of SiC MOSFET chips, the simulation results of DOE are shown in Table II.

Using MINITAB, quadratic multinomial regression fitting was carried out on the simulation results in Table II. The regression models for maximum temperature and maximum stress were obtained using the following equations:

$$T = -16.92x + 0.06y + 2.51x^2 + 0.32y^2 - 0.04xy + 208.67 \quad (5)$$

$$\sigma = 1.12x + 0.42y - 0.39x^2 + 0.11y^2 - 0.09xy + 25.89 \quad (6)$$

where T is the highest temperature in the device, and σ is the maximum stress in RDL.

Three sets of validation simulations were conducted to validate the model of the embedded fan-out SiC MOSFET power module. The results of these simulations are shown in Table III.

B. RSM Optimization

RSM used (5) and (6) to optimize heat dissipation and stress distribution in the model of the embedded fan-out SiC

TABLE II
SIMULATION RESULTS OF DOE

Serials	x	y	Highest temperature (°C)	Maximum stress (MPa)
1	2	-2.5	187.02	25.25
2	4.45	-2.5	184.85	23.63
3	2	2.5	187.35	27.02
4	4.45	2.5	184.71	24.31
5	2	0	184.26	28.90
6	4.45	0	183.56	23.11
7	3.225	-2.5	182.76	27.49
8	3.225	2.5	181.59	27.10
9	3.225	0	180.20	24.74
10	3.225	0	180.20	24.74
11	3.225	0	180.20	24.74
12	2	-2.5	187.02	25.25
13	4.45	-2.5	184.85	23.63
14	2	2.5	187.35	27.02
15	4.45	2.5	184.71	24.31
16	2	0	184.26	28.90
17	4.45	0	183.56	23.11
18	3.225	-2.5	182.76	27.49
19	3.225	2.5	181.59	27.10
20	3.225	0	180.20	24.74
21	3.225	0	180.20	24.74
22	3.225	0	180.20	24.74

TABLE III
VERIFICATIONS

Serials	x	y	T (°C)	Stress (MPa)	Temperature error	Stress error
1	2.5	-2.5	184.5	25.3	0.19%	3.6%
2	3	0	180.6	25.4	0.07%	1.3%
3	3.5	2.5	182.8	24.6	0.44%	1.6%

TABLE IV
OPTIMIZED PROPERTIES OF THE MODEL

	Target	Lower limit	Expected value	Upper limit	Weight
Temperature (°C)	Minimum	180	180	188	1
Stress (MPa)	Minimum	23	23	30	1

MOSFET power module. The contour plots of temperature and stress are shown in Fig. 10(a) and (b), respectively, and the surface diagram of temperature and stress is shown in Fig. 10(c) and (d), respectively. Finally, the response optimizer in MINITAB was used to calculate and optimize the model. The optimized properties of the model are shown in Table IV.

1) The optimal properties were obtained at chip location $x = 3.856$ mm and $y = -0.025$ mm.
2) The expected temperature and stress from RSM optimization were 180.707 °C and 24.453 MPa, respectively.

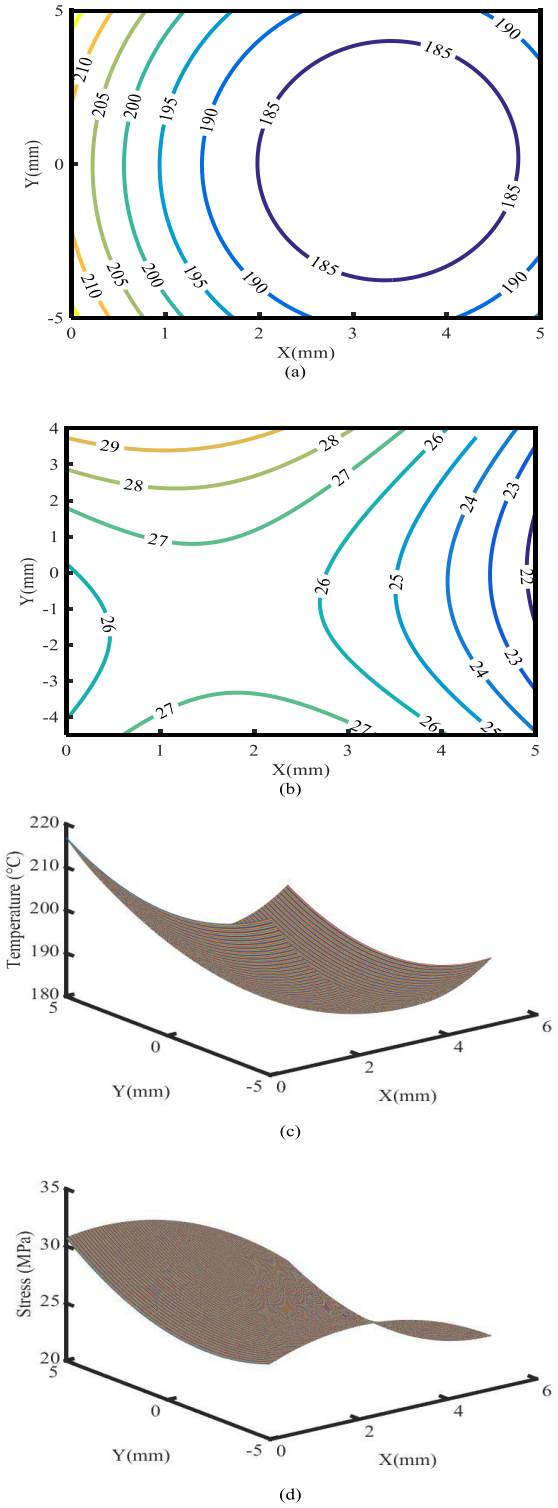

Fig. 10. Contour plots of (a) temperature and (b) stress; the surface contour of (c) temperature and (d) stress.

3) An analysis of the optimized model showed that optimal heat dissipation and thermal stress were obtained when the x-coordinate of the right-side chip in Fig. 7 was 3.865 mm, and its y-coordinate was −0.025 mm.

C. ACO-BPNN

As shown in Fig. 11, the operation of the ACO-BPNN is detailed as follows.

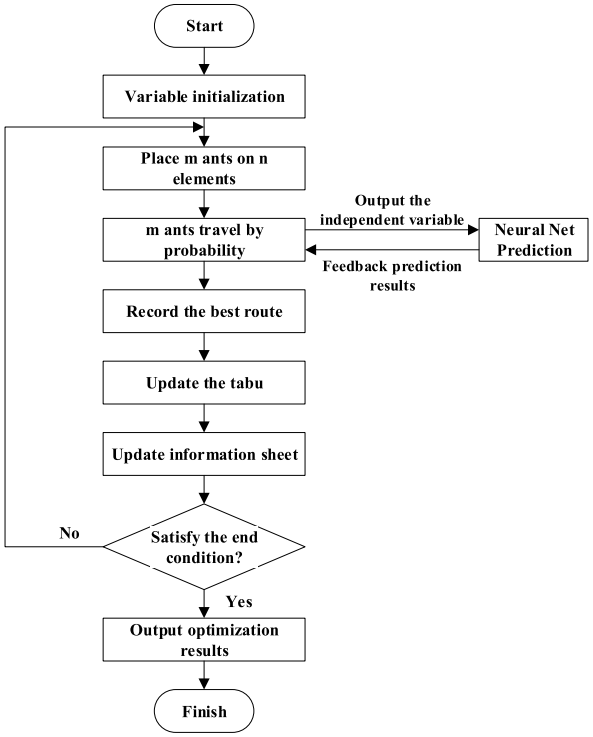

Fig. 11. Flowchart of ACO-BPNN.

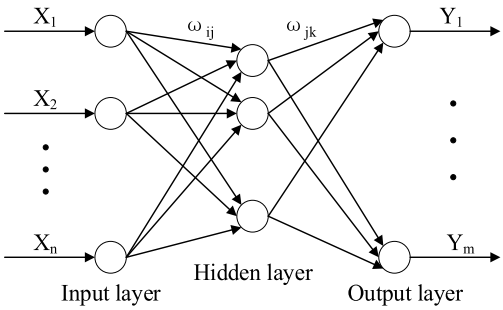

Fig. 12. Neural network topology diagram.

1) First, the normal optimization algorithm is carried out to output the value of independent variables.
2) Each time the fitness value is calculated, the neural network prediction algorithm is called to predict the temperature and thermal stress of X and Y output by the optimization algorithm.
3) The prediction results are fed back into the optimization algorithm and the iteration continues.

In this article, we conducted 180 simulations as the training set of the neural network. This training set covers the whole feasible region of the chip. As shown in Fig. 12, NN consists of three layers: input layer, output layer, and hidden layer. Based on the training, the case temperature and stress of each chip position obtained by the ant colony algorithm iteration is calculated. The case x-coordinate and y-coordinate of each MOSFET are selected as the input, and the stress and temperature of each MOSFET is regarded as the output. The hidden layer of BP NN is set as 9. In addition, in BP NN, the learning rate is 0.01, the maximum number of network training is 1000, and the minimum mean square error is set as 0.00004.

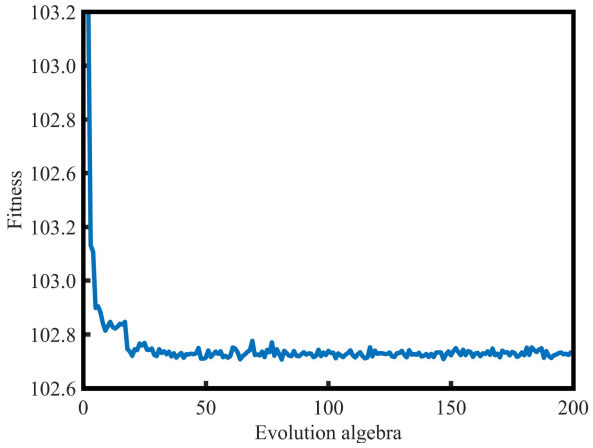

Fig. 13. Fitness evolution curve.

TABLE V
COMPARISON OF THE JUNCTION TEMPERATURE AND MAXIMUM STRESS BEFORE AND AFTER OPTIMIZATION

	After RSM	After ACO-BPNN	Before optimization	Percentage improvement by RSM	Percentage improvement by ACO-BPNN
Temperature T (°C)	180.71	180.40	187.02	3.38%	3.50%
Stress σ (MPa)	24.453	24.728	27.490	11.05%	10.04%

The operation of the ACO algorithm is detailed as follows.

1) The parameters of the algorithm were initialized as follows: the number of ants m is set as 20; the maximum number of iterations G is set as 200; the pheromone evaporation coefficient R_{ho} is set as 0.9; the transfer probability constant P_0 is set as 0.2, and the step size of local search step is set as 0.1.
2) The initial position of the ant was randomly generated. The value of its fitness function was calculated and set as the initial pheromone path. The probability of state transition was then calculated.
3) The process of updating the location of the ants in the colony begun by conducting local search when the state transition probability was less than the transition probability constant. Global search was then conducted to generate new ant locations, and boundary conditions were processed using the boundary absorption method. Finally, the ant location was updated within range.
4) The fitness of the new ant location was calculated to determine whether an ant had moved. The pheromone path was updated if movement was detected.
5) If the termination condition was met, the process stopped, and the optimized values were output. If the termination condition was not met, the process continued.

Then, through the iteration of ant colony algorithm, the path with the highest concentration of accumulated pheromone is determined. That is the optimal solution. The fitness evolution curve obtained by iteration is shown in Fig. 13.

The predicted response from the ACO-BPNN was that the temperature was 180.40°C and the stress was 24.728 MPa. An analysis of the results of ACO-BPNN showed that optimal

heat dissipation and thermal stress were obtained when the x-coordinate of the chip on the right side of Fig. 7 was 3.7 mm, and its y-coordinate was 0 mm. Referring to Table V, the results obtained through RSM and the ACO-BPNN were similar, which proved the accuracy of the model. Continuing in Table V, ACO-BPNN improved temperature by 3.50%, and RSM improved stress by 11.05%.

IV. Conclusion

This article studied the impact of chip location, RDL material on an embedded fan-out SiC MOSFET power module during thermal cycling, and heat dissipation. Finite element models of RDL layers with different chip locations, different materials, and different thicknesses were created. Thermal simulation of the SiC MOSFET power module was conducted under different RDL materials. This simulation demonstrated that copper was better than nano-silver at dissipating heat. The thermal cycling thermo-mechanical simulations were performed to reveal that nano-silver had a better thermodynamic performance than copper. RSM and an ACO-BPNN were used to optimize heat dissipation and stress distribution in the model. Both methods achieved optimization at similar chip locations. ACO-BPNN improved temperature 3.50%, and RSM improved stress by 11.05%.

There are still some challenges of this project in the future works: the further experimental verification is needed. Besides the optimization of chip location distribution, some other parameters, such as thickness, chip size, and so on, should be considered in the thermal cycling reliability optimization.

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