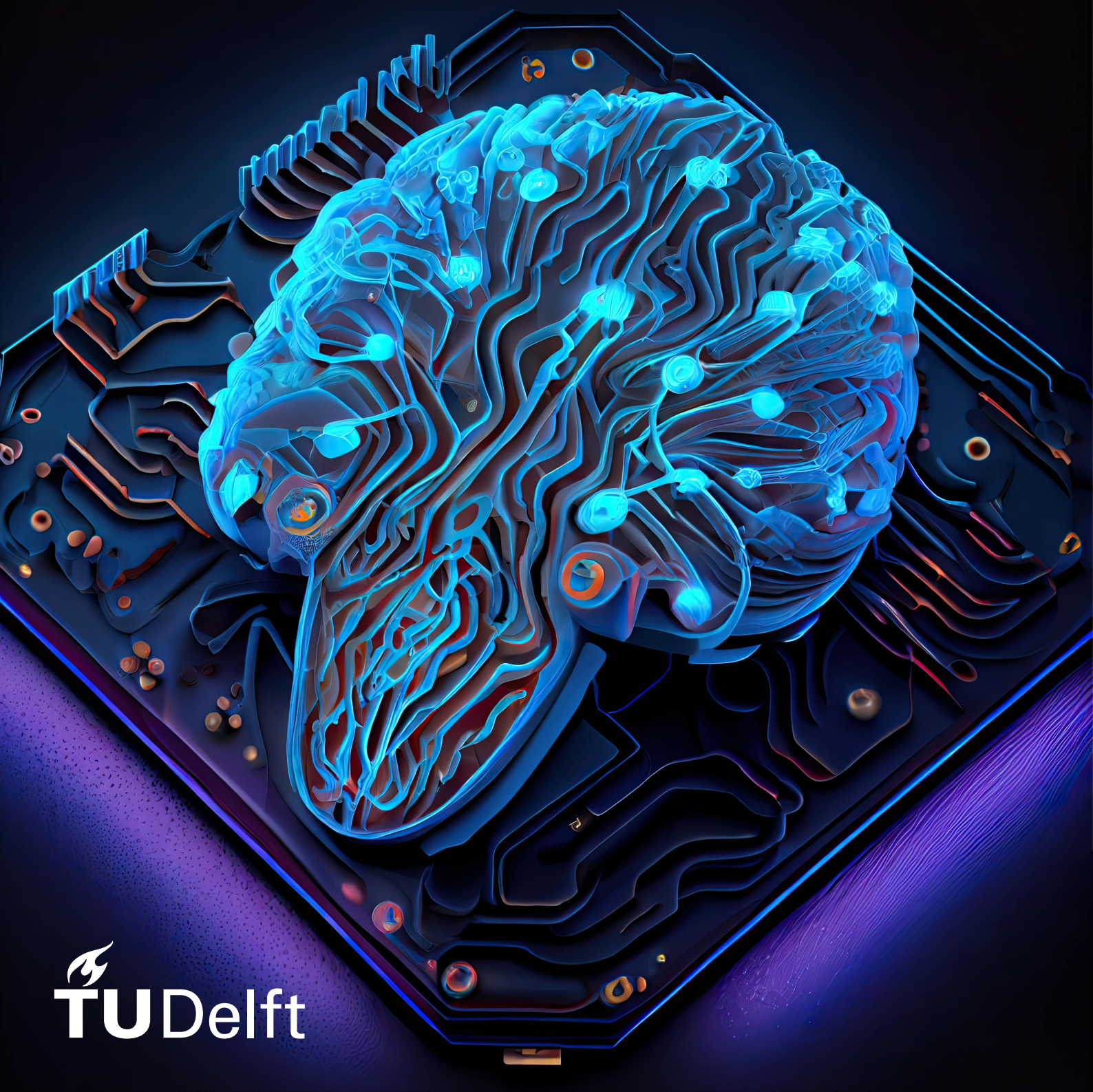
A Novel Neural Recording IC with Adaptive Gain Control for Wide-Dynamic Range Closed-Loop Neural Interfaces

Remy Zhang



TU Delft

A Novel Neural Recording IC with Adaptive Gain Control for Wide-Dynamic Range Closed-Loop Neural Interfaces

by

Remy Zhang

in partial fulfillment of the requirements for the degree of

Master of Science

in Electrical Engineering

at the Delft University of Technology,

to be defended publicly on Monday October 23, 2023 at 9:30.

Supervisor:	Dr. D.G. Muratore	Department of Microelectronics, TU Delft
	MSc. B.H.B.M. Abdelgaliel	Department of Microelectronics, TU Delft
Thesis committee:	Dr. D.G. Muratore	Department of Microelectronics, TU Delft
	Dr. S. Du	Department of Microelectronics, TU Delft

Project Duration: September 2022 - September 2023
Student number: 4835182

This thesis is confidential and cannot be made public until October 23, 2023.

Abstract

Abstract— **Bidirectional neural recording ICs faces the challenge of simultaneous stimulation and recording. The recording IC should endure large stimulation artifacts while capturing weak neural signals excited by the stimuli. The stimulation artifacts can be as large as hundreds of millivolts, which can saturate the recording front end. Conventional neural-recording ICs use a low-noise-amplifier (LNA), a programmable-gain amplifier (PGA) followed by an analog-to-digital converter (ADC), leading to low power consumptions and great noise performances. However, the dynamic range (DR) is usually limited to 50 dB. State-of-the-art recording ICs using direct-conversion ADCs have been introduced to increase the DR. However, the typical power and area consumption for these architectures are exceeding the requirements for next-generation brain-computer interfaces. This work proposes a novel neural-recording IC system architecture with saturation prevention in presence of large stimulation artifacts. The proposed architecture consists of an AC-coupled boxcar sampler, switched-capacitor low-pass filter followed by a 10-bit asynchronous SAR ADC. The integrated voltage at the output of the boxcar sampler is sampled by the ADC and monitored by a level-cross detection block. Based on the output of the level-cross detection block, the integration time, and thus the gain, can be tuned to different configurations pre-defined in a look-up table (LUT). The additional noise penalty due to noise-folding from decreasing the integration time is compensated by oversampling and averaging. The proposed system architecture is partially implemented at transistor level while the ADC and digital blocks are modeled using verilog-A as a proof-of-concept. The analog front-end achieves a DR of $69.5\,\mathrm{dB}$ with a peak-to-peak maximum input amplitude of $180\,\mathrm{mV_{PP}}$ and a typical ENOB of 8.01 bits.**

Keywords— Bidirectional neural interface, artifact mitigation, wide dynamic range (DR), boxcar sampler, asynchronous successive approximation register (SAR), analog-to-digital converter (ADC), saturation prevention, automatic gain control

Acknowledgements

I am very grateful that I have had the opportunity to work on this challenging topic. Coming up with a novel system architecture that has not been proposed in the state-of-the-art literatures was not easy and this can be substantiated by the fact that two proposed system architectures during the project could not meet our expectations. My MSc thesis started more than a year ago, it was a very long and difficult journey, but definitely not lonely. I would like to extend my gratitude to those who have contributed to my thesis work.

First of all, I would like to express my sincere gratitude to Dr. Dante Muratore for giving me the opportunity to pursue my thesis project in his group, known as the Smart Brain Interfaces Group. I am grateful for the freedom you gave me to pursue this challenging project. Your expertise in the field of analog and mixed-signal IC design has definitely helped me to become a better IC designer compared to when I started.

Equally deserving recognition is my daily supervisor and a very talented PhD candidate Bakr Abdelgaliel. Not only do I appreciate the guidance and support you gave me during my project, but I also enjoyed the fact that we could talk about anything, may it be about transistors or just about our daily lives.

The same recognition goes to my fellow MSc students and my office mate who joined together with me in the group: Hsukang and Ronald. We often shared our ideas together and had long discussions, which was very helpful to think in a different way. But the major recognition goes to the nice and fun atmosphere you guys created in the office. I am certain that you guys will become a very skilled IC engineer.

Throughout my thesis project, there were many difficulties. I would like to express my gratitude to my girlfriend, Xiaochuan. Thank you for believing in me. Your trust and support always kept me positive during the project.

Last, but not least, I am profoundly grateful to my parents. I appreciate the support and the unconditional trust that you gave me to pursue my own career in this field. I will forever remember the impact you have had on my life.

Contents

List of Figures

List of Tables

1

Introduction

1.1. Background

1.1.1. Stanford Artificial Retina Project

Over the past few decades, brain-computer interfaces (BCI) have enabled treatment of neurological disorders like epilepsy and Parkinson's disease [1]. A remarkable advancement by the Stanford Artificial Retina team aim to restore vision in blind individuals [2] by using a novel architecture. Figure 1.1 illustrates the fundamental principle behind this breakthrough.

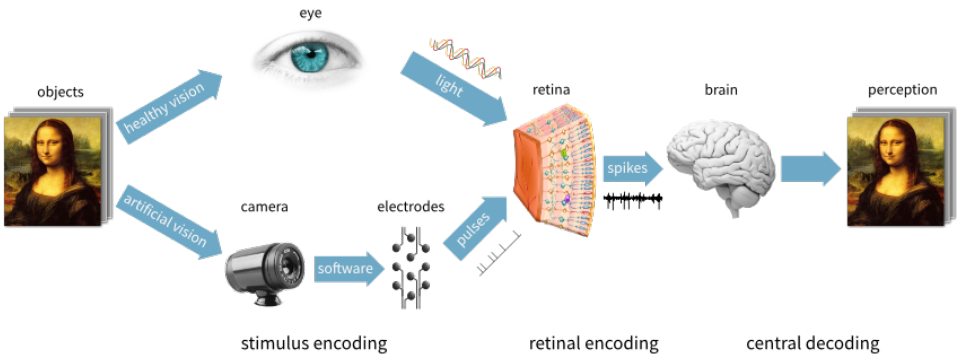


Figure 1.1: Illustration of the Stanford Artificial Retina Project. Source: [2]

The process begins with a camera capturing a digital image of an object, followed by software translating this image into electrical signals. These signals are then utilized to stimulate

the neurons located near the inner surface of the retina, known as retina ganglion cells (RGCs), via microelectrode arrays (MEAs). These ganglion cells respond to the stimulation by exciting neural spikes, allowing the brain to recreate the original object's perception. However, activating cells in close proximity to the electrode during stimulation may result in an imprecise object representation, since the RGCs comprise of varied cell types which represents different types of visual information. To accurately translate an image captured by the camera to the naturalistic neural code, the Stanford Artificial Retina proposed the system illustrated in Fig. 1.2. The initial step of the system involves calibrating the location and the cell type of the available RGCs through the recording of spontaneous cell activities. This dictionary outlines the probability of exciting a neural spike in the recorded RGCs. Ultimately, the neurons that can be accessed are stimulated in accordance with the camera's image during runtime. To produce meaningful visual signals, the electrode array requires at least 10^4 channels [4].

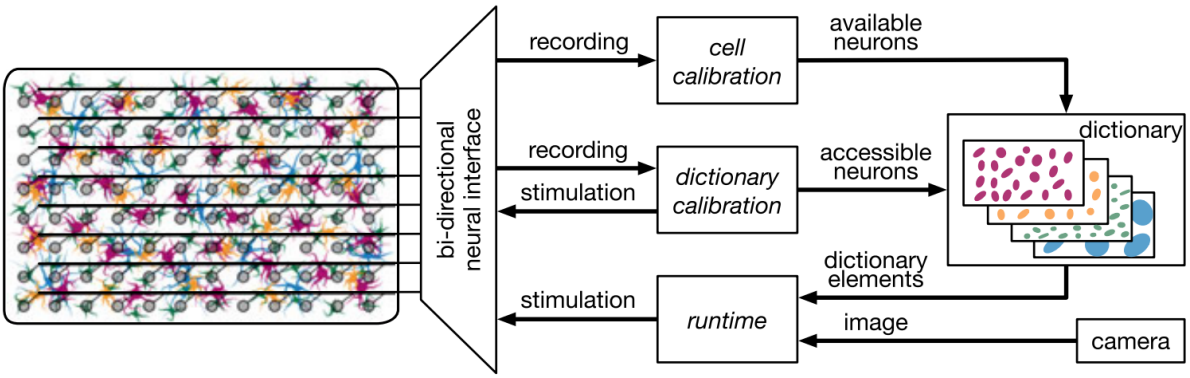


Figure 1.2: Illustration of the system-level overview of the Stanford Artificial Retina. Source: [3]

1.2. State of the art

1.2.1. Stimulation Artifacts

To perform the operations aforementioned, a bi-directional neural interface is required. One of the the main challenges of a bi-directional neural interface is to withstand the stimulation artifacts. In Fig. 1.3, the origin of stimulation artifacts is illustrated. During stimulation, the currents flowing through the electrodes result in a voltage potential drop, resulting in a direct stimulation artifact. After stimulation, the charge remaining at the interface will result in a gradual-decaying potential, defined as the residual artifact.

Notably, the amplitude of the stimulation artifacts can be order of magnitudes larger than the neural responses as illustrated in Fig. 1.4. Due to the finite range of the amplifier, the resulting artifacts will saturate the front-end device. Even after stimulation, the slow-decaying residual artifacts can last several milliseconds [6], which could also saturate the front-end and blind the neural spike recording, thereby missing important neural information. In [7], it has been

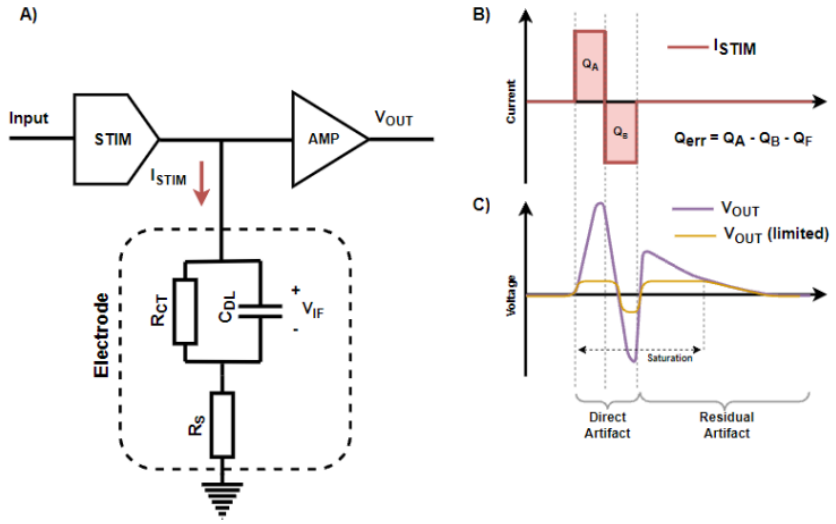


Figure 1.3: Illustration of the origin of stimulation artifacts: (A) Simplified bi-directional neural interface with linear ETI model;(B) a biphasic charge-balanced current stimulus waveform; (C) Amplifier output with infinite dynamic range and with a limited dynamic range indicating saturation of the device. Source: [5]

shown that 27% of the spikes are lost when the front-end is saturated for 2 ms after stimulation. Missing neural spikes result in loss of information which cannot

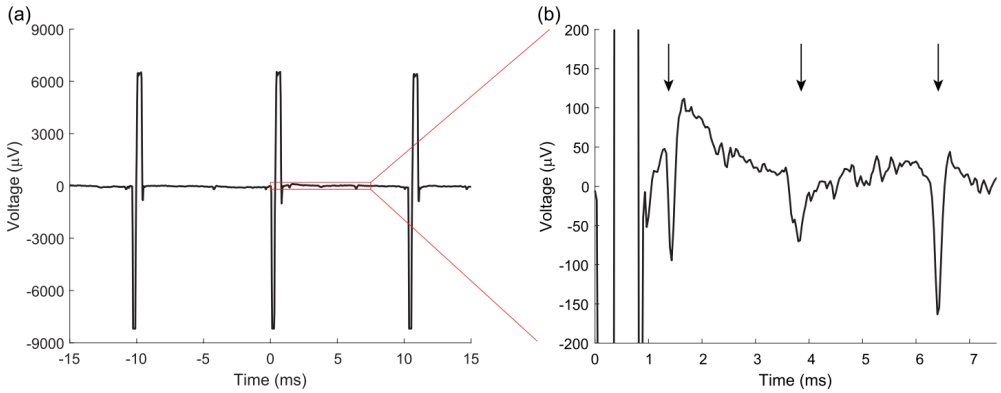


Figure 1.4: An example recording during microstimulation. Stimulation artifacts are several order of magnitudes larger than the neural spike. (a) Stimulation artifacts. (b) Underlying neural spike. Source: [8]

1.2.2. Artifact Mitigation

Figure 1.5 illustrates several stimulation artifact mitigation techniques in the signal chain of bi-directional neural interfaces. The only way to reduce the stimulation artifact at the ETI is to apply artifact mitigation techniques at the stimulation site. Front-end mitigation techniques can be used to prevent saturation of the recording interface. The back end artifact mitigation

technique can be applied if the front-end properly digitizes the artifact to recover the recorded neural information.

Stimulation mitigation techniques

Stimulation site mitigation techniques include waveform shaping and charge balancing. A novel stimulation artifact reduction technique has been developed to construct a stimulation waveform that can maximally reduce the residual artifact duration and therefore achieving fast artifact recovery [9]. The efficacy of this algorithm is heavily reliant on precise modeling of the electrode-tissue interface. This algorithm assumes that the ETI impedance is linear time-invariant. In reality, the ETI impedance is non-linear and time-variant and should be modelled as accurate as possible to minimize the recovery time.

In contrast to widely accepted opinions [10], it has been shown that a perfect charge-balanced stimulation waveform does not result in charge-balancing at the electrode[11]. Therefore, charge-balanced stimulation does not necessarily reduce the residual artifact and thus does not necessarily improve the recovery time.

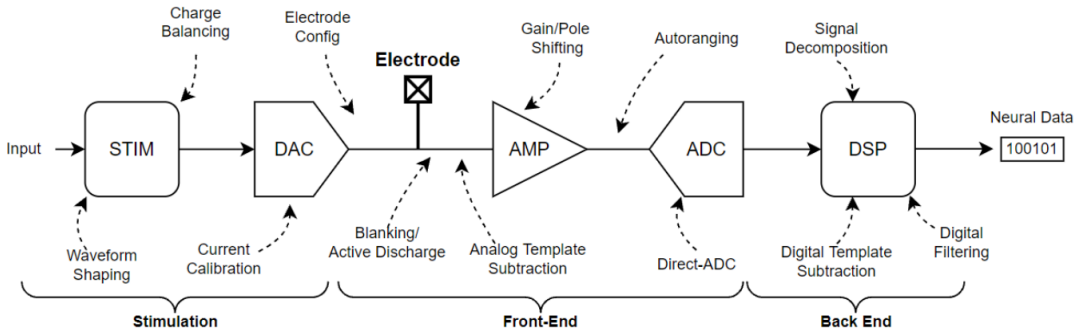


Figure 1.5: Possible stimulation artifact mitigation techniques in the signal chain of a bi-directional neural interface. Source: [5]

Front-End mitigation techniques

Blanking: A straightforward approach to avoid saturation is the blanking technique. This technique disconnects the recording channel from the electrode during stimulation by using a switch [12]. In presence of a residual artifact, the switch must be disconnected even after stimulation. The precise reconnecting timing is difficult to predict since the residual artifact can vary depending on stimulation waveforms and ETI. Furthermore, all the information from the electrode are lost during blanking. Therefore, this technique in combination with fast artifact recovery time is required to prevent loss of neural information immediately after stimulation.

Analog template subtraction: Analog template subtraction is another technique used to suppress the artifact [13]. This technique generates an artificial template of the stimulation artifact. and is subtracted from the input during every stimulation cycle. In case of differences between the template and the actual stimulation artifact, the result of the subtraction can still saturate

the front-end, especially since the residual artifact is difficult to predict. Figure 1.6 illustrates this stimulation artifact cancellation technique using a hybrid hardware and software approach as proposed in [13] to cancel the direct stimulation artifact and to optimize the cancellation of residual artifact.

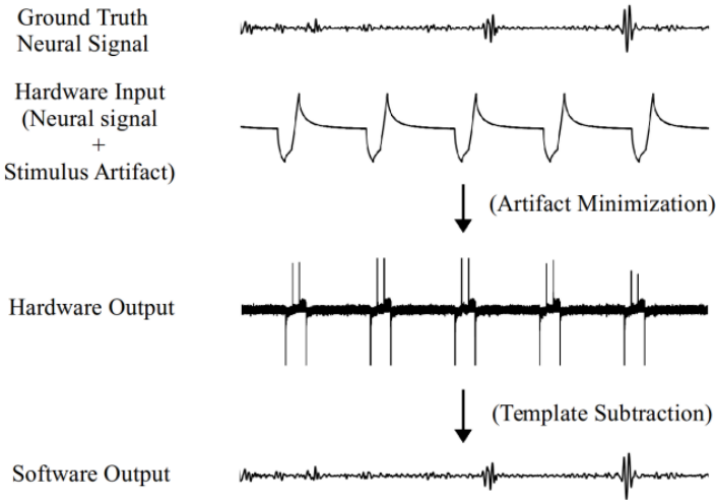


Figure 1.6: An example of an artifact mitigation technique using analog template subtraction. Source:[13]

Gain/Pole Shifting: Gain shifting implies that during the amplification stage, the gain is varied with respect to time. This technique can be applied to avoid front-end saturation of direct artifact by adapting the gain during stimulation. Pole shifting implies that the high-pass cut-off frequency of the filter implemented in the front-end are shifted to a higher frequency. However, if the frequency of the stimulation artifacts reside in the same bandwidth of interest as the neural spike, which is the case for action potentials [14], implementing pole shifting will be ineffective.

Direct-ADC: Direct ADCs, such as a sigma-delta converter, can be used to directly convert the input neural signal into a digital output. Figure 1.7 illustrates a potential implementation of a direct ADC architecture. The direct ADC integrates the amplifier directly inside the body of the ADC. At the input of the amplifier, the input voltage V_{in} is subtracted by the previous sample, preventing the front-end from being saturated.

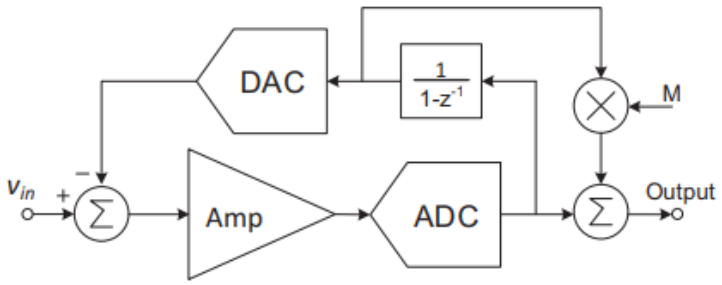


Figure 1.7: An example of a direct ADC architecture. Source:[15]

Back-end mitigation techniques

If the artifact can be recorded by a high dynamic range front-end, digital back-end techniques can be used to mitigate the artifacts.

Data reconstruction: A simple method to mitigate stimulation artifacts is to identify and remove the artifact segments and reconstruct the data using interpolation as illustrated in Fig. 1.8. This technique relies on the accurate peak detection algorithm of the stimulation artifact as the data between the start and end of the artifact are removed [16], [17]. Therefore, this method is suitable for low frequency neural signals such as local field potentials. For high frequency neural signals such as an action potential, the discarding of data could result in important information being lost [10].

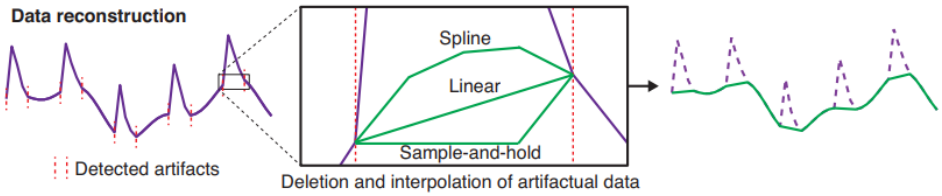


Figure 1.8: Back-end mitigation using digital reconstruction. Source:[10]

Digital subtraction: Another technique is to use digital template subtraction as illustrated in Fig. 1.9. Similar to analog template subtraction, an artificial template is generated and can be subtracted from the recorded data [18]. Since the subtraction is performed in the digital domain, high accuracy recovery can be obtained if the front-end records the stimulation artifact without distortion.

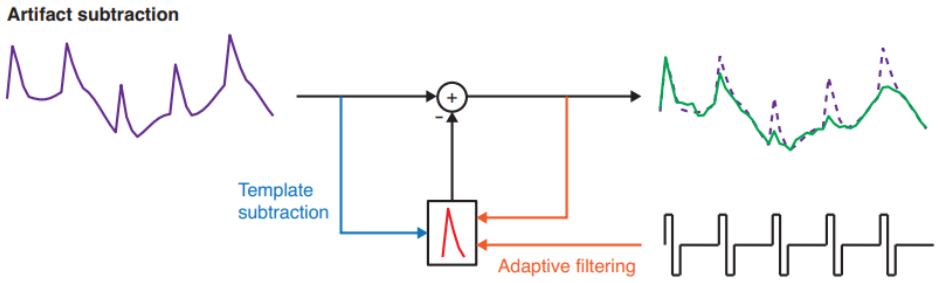


Figure 1.9: Back-end mitigation using digital subtraction. Source:[10]

Component Decomposition: Component decomposition methods such as ensemble empirical mode decomposition or independent component analysis can be used to separate the recorded waveform into artifact and non-artifact components to reconstruct the underlying neural signal [19]. Figure 1.10 illustrates the idea behind the component decomposition method. Intensive computational resources required for the reconstruction results in a highly complex on-line integration.

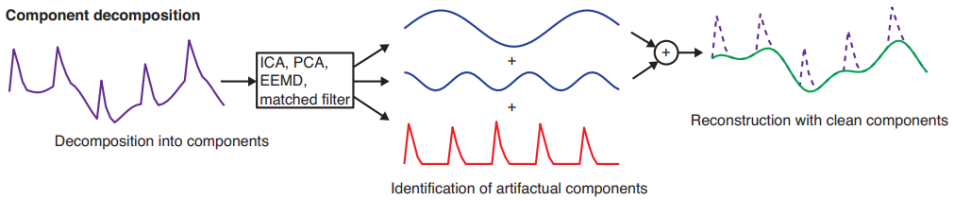


Figure 1.10: Back-end mitigation using digital decomposition. Source:[10]

1.3. Problem Statement

In the context of the Stanford Artificial Retina project, it is noteworthy that the relevant neural spikes always occur after the stimulation phase. This temporal difference enables the possibility of recording direct artifacts and neural spikes distinctively. Given the significant difference in amplitude between direct artifacts and neural spikes, the front-end must amplify the relatively weak neural signals while withstanding the artifact during the stimulation process. To achieve the objectives set forth by the Stanford Artificial Retina project, it is essential to develop a compact and low-power analog front-end solution to achieve a single-cell resolution. Moreover, a key aspect for the recording front-end is to obtain a high dynamic range, which is essential for capturing large stimulation artifacts and neural signals accurately to allow the possibility to apply back-end stimulation artifact techniques. Meanwhile, recording artifacts with high accuracy allows a profound study into the time-varying and non-linear ETI impedance, which in turn can be used to reduce the stimulation artifact when applying mitigation techniques that are reliable on the accurate modelling of the ETI impedance. Therefore, the aim of this work is to propose a compact and low-power novel system architecture that can record during and after stimulation, without saturating the front-end in presence of the stimulation artifacts.

1.4. Neural Recording Interfaces

Illustrated in Fig. 1.11 are the current front-end recording architectures consisting of a neural amplifier and ADC [20]–[22] or a direct-conversion ADC that has an amplifier integrated inside [23]–[26]. The following section briefly discuss the possible amplifier and ADC architectures targeted for neural recording interfaces.

1.4.1. Recording Amplifiers

As mentioned previously, several factors should be considered while designing an amplifier: sufficient gain, high signal-to-noise ratio (SNR), wide DR, low power consumption and a compact device. In this part, three architectures for the recording amplifier are discussed.

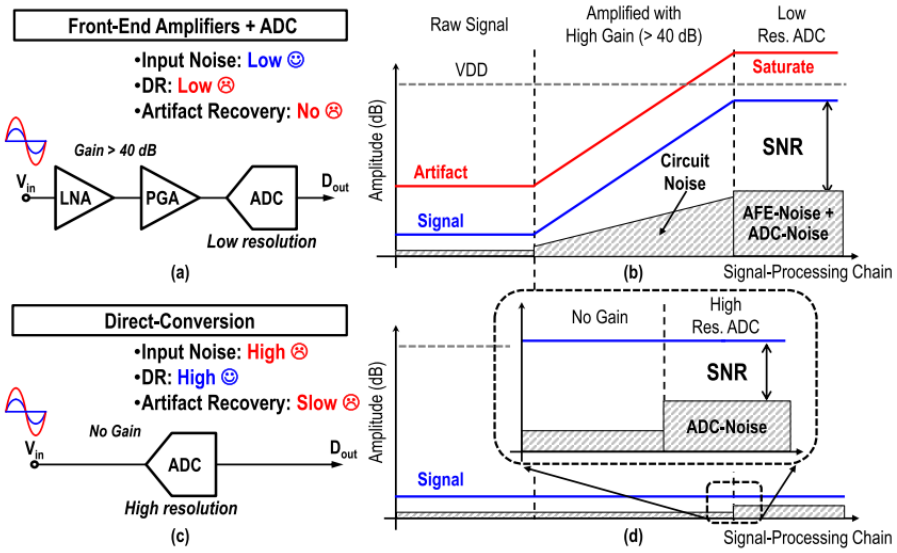


Figure 1.11: (a) Block diagram and (b) SNR analysis of the conventional neural recording IC. (c) Block diagram and (d) SNR analysis of the direct ADC based neural-recording IC. Source:[22]

.

AC-Coupled Amplifiers

The electrode DC-offset (EDO) and the flicker noise introduced by the amplifier can significantly impact the performance of the front-end recording. The offset voltage can saturate the front-end amplifier and can be orders of magnitude larger than the neural signal. Therefore, a capacitively-coupled instrumention amplifier (CCIA), as shown in Fig. 1.12 is typically used to remove the EDO while providing sufficient gain [20], [27]. The input capacitors block the EDO and the feedback capacitor in combination with the feedback resistor together create a high-pass pole in the signal transfer to reduce the flicker noise.

The main disadvantage of this architecture is the large area consumption. The feedback capacitor C_f is determined by the requirement for a high-pass pole, which is usually at very low frequency. Since the resistor is limited to several hundreds of MΩ in IC technology, the feedback capacitor cannot be minimized to save area. Furthermore, the input capacitor C_{in} is determined by the gain requirement shown in Equation 1.1.

$$A_{CL} = \frac{C_{in}}{C_f} \tag{1.1}$$

To overcome this issue, pseudo-resistors are typically used to obtain resistances in the range of 10 GΩ to keep the capacitors as small as possible [28]. However, pseudo-resistors are very sensitive to PVT variations and suffers from non-linearity. Other methods such as switched resistors (SR) and segmented SR have been proposed to obtain a large equivalent resistance for the high-pass pole implementation [29]–[31].

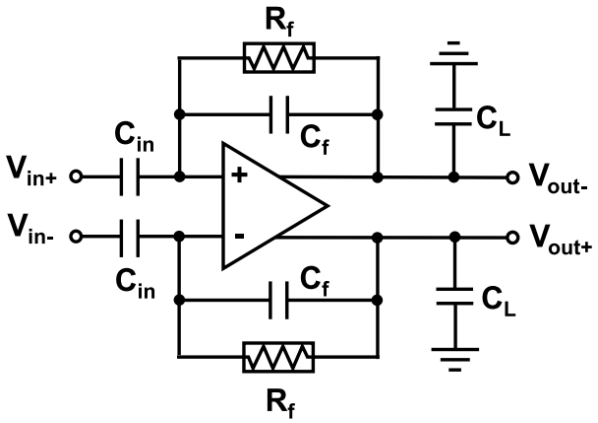


Figure 1.12: Differential CCIA architecture including feedback resistors to implement a high-pass pole

Boxcar Integrator

Another potential architecture is the boxcar integrator shown in Fig. 1.13. The output current I_{out} of the operational transconductor (OTA) is integrated on the capacitor over a fixed time window. With the finite output impedance r_o taken into consideration, the voltage over the capacitor is defined as:

$$V_C = g_m r_o [1 - e^{T_{int}/r_o C}] \tag{1.2}$$

Here, g_m is the transconductance of the OTA and T_{INT} is the time period in which the output current of the OTA is integrated over the capacitor. Due to its open-loop architecture, the gain is only dependent on the OTA and therefore it suffers from process variations. Nonetheless, the elimination of the feedback capacitors will be appealing for compact AFEs. This architecture

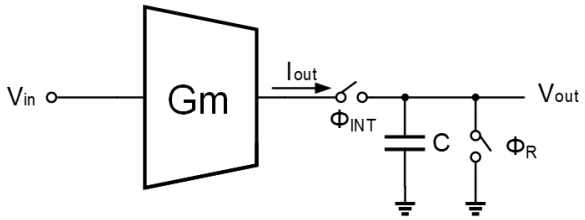


Figure 1.13: A Gm-C integrator

is popular in ADCs that require anti-aliasing filters, since the fixed time window integration creates a sinc-filter with nulls at $1/T_s$, where T_s is the sampling period of the ADC. This results in minimum penalty from noise folding when sampling [32] by achieving an equivalent noise bandwidth (ENBW) of $f_s/2$, where f_s is the sampling frequency at the output of the integrator. Figure 1.14 shows the transfer function $|H(f)|$ of the boxcar sampler with finite output impedance. Away from the nulls, the transfer function simplifies to the equation shown in (1.3).

$$|H(f)| = (1 - \frac{T_s}{r_o C}) \frac{g_m T_s}{C} |\frac{\sin(\pi T_s f)}{\pi T_s f}| \tag{1.3}$$

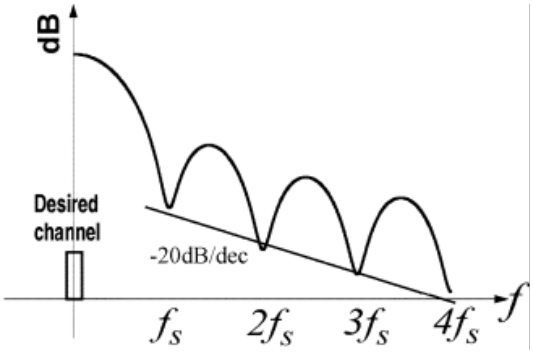


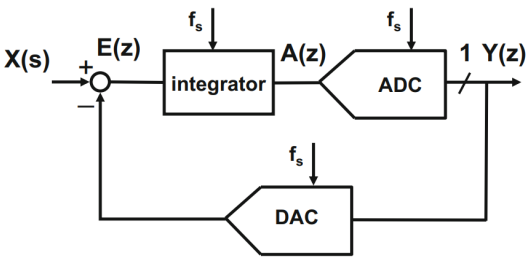
Figure 1.14: The transfer function of a boxcar sampler with finite output impedance [32].

1.4.2. Analog-to-Digital Converters

Oversampled ADC

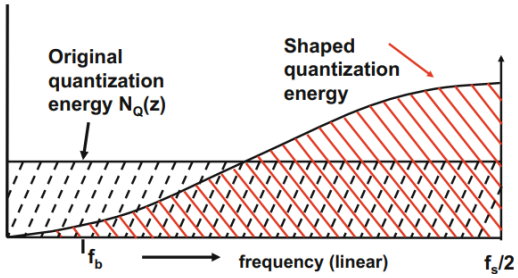
Oversampled ADCs use a sampling frequency (f_s) considerably higher than Nyquist frequencies ($f_{nyquist}$). Assuming that the quantization error of a N-bit ADC can be approximated as white noise, the noise power will therefore be spread out over a larger frequency range, which can be filtered to obtain a higher SNR. If the signal bandwidth is fixed, the SNR increases by:

$$\Delta\text{SNR} = 10\log_{10}(\frac{f_s}{f_{nyquist}}) = 10\log_{10}(\text{OSR})$$



(a)

Figure 1.15: Basic architecture of a sigma-delta modulator



(a)

Figure 1.16: Noise shaping characteristic of a sigma-delta converter.

This indicates that oversampling by a factor of four increases the effective resolution by one bit. In sigma-delta converters as shown in Fig. 1.15a, oversampling in combination with feedback and integration in the signal path is utilized to obtain noise-shaping characteristics as shown in

Fig. 1.16a, where quantization noise is pushed towards higher frequencies. For an n-th order noise shaping, this results in an in-band SNR increase of:

$$\Delta\mathrm{SNR} = 20\log_{10}\left(\frac{\mathrm{OSR}^{(n+0.5)}\sqrt{2n+1}}{\pi^{n}}\right) \tag{1.4}$$

Oversampled ADCs are widely used [22]–[24], [26], [33], [34] in neural interfaces to convert raw neural signals directly into digital codes with an amplifier integrated inside the ADC to avoid saturation due to large simulation artifacts, significantly improving the DR. However, to meet the input-referred noise (IFR) requirement over a neural signal bandwidth, high-resolution $\Sigma\Delta$ modulators are usually used [33], [34]. For example, in [33], a third-order cascade of integrators were implemented which consumes significant power and area. Although in [23], a first-order modulator was implemented which minimizes power consumption, the resolution obtained (ENOB of 9.4) over a bandwidth of 250 Hz does not allow recording of action potentials. Furthermore, $\Sigma\Delta$ modulators usually requires chopping and input capacitors to suppress the flicker noise and the EDO.

Another type of oversampled converter is the Δ-modulator. In [26], the Δ-modulator has been implemented for an neural interface. The advantage of using a Δ-modulator for a neural interface is the suppression of DC offset without using passive components, therefore eliminating the necessity of input capacitors.

The neural interface presented in [26] implements clock-boosting and auto-ranging to record during stimulation without being blinded by the direct artifacts. The sampling frequency is boosted to cope with the transient speed of the artifact while the quantization step sizes is relaxed using radix-2 exponential auto-ranging algorithm.

SAR ADC

Successive approximation register (SAR) ADC has gained its popularity for neural recording interfaces due to its medium to high resolution and high power efficiency. Fig. 1.17 illustrates the basic architecture of a SAR ADC. The analog input voltage $\mathrm{V_{in}}$ is sampled and held using a sample-and-hold circuit. The conversion starts by comparing the sampled voltage with the DAC output $\mathrm{V_{DAC}}$. The DAC voltage is adjusted depending on the comparison result and the approximation is further refined based on a binary search algorithm. Fig. 1.18 shows an example of a 4-bit SAR ADC conversion.

The integration of SAR ADCs within multichannel neural recording systems presents a challenge mainly focused on the design of an area-efficient capacitor DAC array. The DAC module typically consumes substantial on-chip area. To address this issue, various neural applications have explored sharing the SAR ADCs across multiple channels to reduce the die area [35], [36]. Although compact capacitor array implementations have been proposed for conventional SAR ADCs [37], [38], their integration into neural recording interfaces has not been studied to date. Figure 1.19 shows the die photo of the ADC in [37]. With an effective area of $0.0013\,\mathrm{mm}^2$, this approach holds considerable promise for future integration within neural applications.

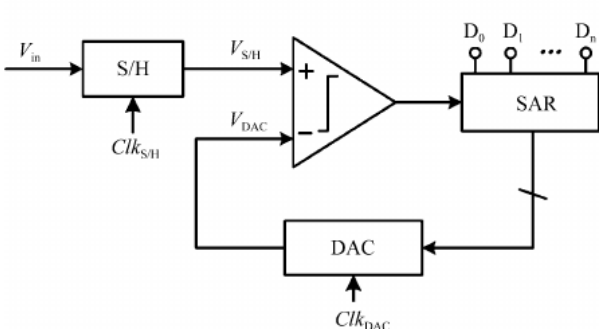


Figure 1.17: Block diagram of a SAR ADC.

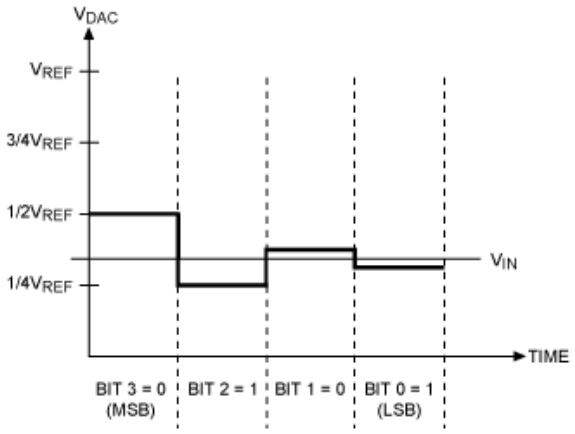


Figure 1.18: A 4-bit SAR ADC conversion example

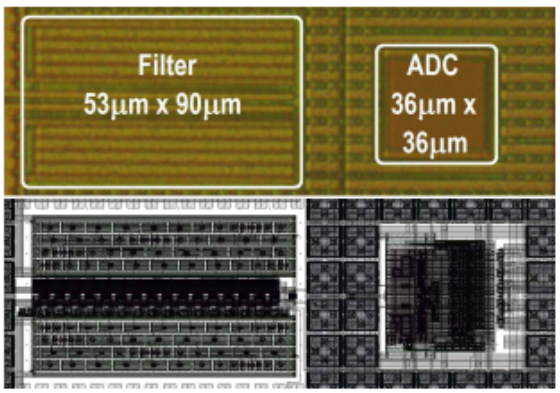


Figure 1.19: Die photo and layout of the SAR ADC proposed in [37]

AFE Comparison

To fairly compare AFE architectures for neural interfaces, the combined performance of the front-end amplifier and the ADC should be taken into account. The performances of some state of the art works that have either SAR or an oversampled ADC integrated in the recording front-end are listed in Table 1.1.

The objective of this work is to develop a neural recording system able to capture stimulation artifacts. While oversampled ADCs tend to achieve high DR levels, the associated area overhead makes this architecture less suitable for large-scale array implementation. If a SAR ADC is chosen, the use of a front-end amplifier to amplify weak neural spikes is necessary. However, to prevent front-end saturation due to stimulation artifacts, the gain must be adaptable. One feasible approach to achieve this is an AC-coupled amplifier with variable capacitors to program the closed loop again. However, a substantial area should be allocated to these capacitors in this approach. As an alternative, a Gm-C integrator could be used to adapt the gain by adjusting the integration time. This method could potentially fulfill the need to adjust amplification while also reducing the amount of area required.

Table 1.1: Performance of the state of the art works.

	[39]	[40]	[41]	[22]	[26]
Architecture	LNA + SAR ADC	LNA + PGA + SAR	Delta Modulator	LNA + PGA + ΣΔ-ADC	Delta Modulator
DR (dB)	48.6	53.5	86	99.5	79
Input Range	$6.4\,mV_{PP}$	$700\,mV_{PP}$	$110\,mV_{PP}$	$1600\,mV_{PP}$	$200\,mV_{PP}$
Artifact Rejection Method	No	Adaptive IIR Filter	Adaptive Digital Filter	Adaptive Gain	Autoranging + Clock boosting
Power/Ch (μW)	2.7	4.3	3.21	9.8/13.6	1.1/10.8
Area/Ch (mm^2)	0.018	0.66	0.0025	0.72	0.018

2

System Architecture

2.1. Architecture Definition

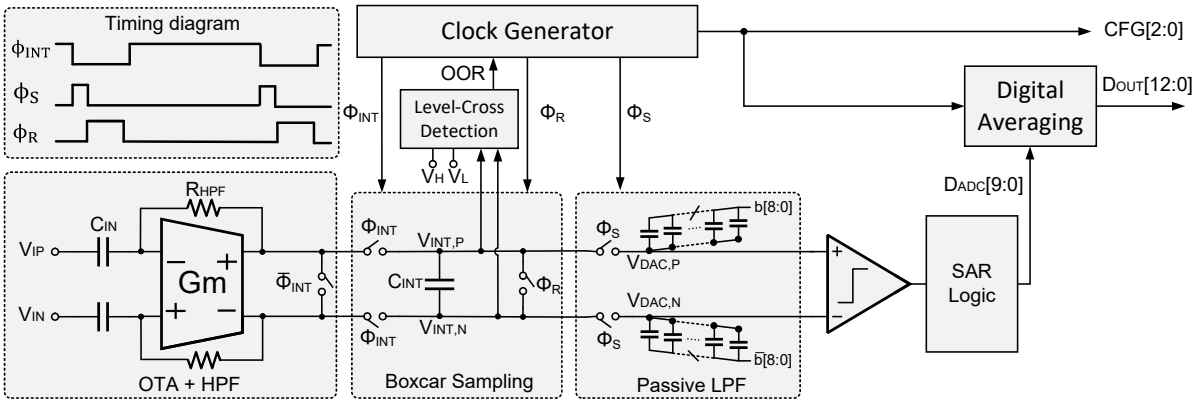


Figure 2.1: Proposed neural recording system architecture

Figure 2.1 illustrates the proposed neural recording system architecture. An AC coupled boxcar sampler with input capacitors C_{IN} and a feedback resistor R_{HPF} is implemented to remove the DC offset and to implement a high-pass pole which cut-off frequency is defined as:

$$f_L = \frac{g_m r_o}{2\pi R_{HPF} C_{IN}} \tag{2.1}$$

The boxcar sampling minimizes the noise penalty due to folding. The boxcar output integrated on capacitor C_{INT} is sampled on the CDAC of the SAR ADC during T_S to implement a switched capacitor low-pass filter (SC-LPF) with a cut-off frequency described in (2.2).

$$f_{SC-LPF} = \frac{1}{2\pi R_{eq} C_{DAC}} = \frac{C_{INT}}{2\pi C_{DAC}} \frac{1}{T_{INT} + T_S} \tag{2.2}$$

Here, T_{INT} is the time elapsed from the integration of the output of the OTA on C_{INT} and T_S is the sampling period of the ADC.

If only the pole of the SC-LPF is taken into account, at f_{SC-LPF}, the signal is attenuated by -3 dB. However, the sinc response of the boxcar sampler introduces additional attenuation. The -3 dB frequency of a sinc function is calculated as follows:

$$\frac{\sin(T_{INT} f)}{T_{INT} f} = \frac{1}{\sqrt{2}}$$

$$T_{INT} f = 0.443$$

Therefore, the -3 dB frequency of the boxcar sampler is given as:

$$f_{boxcar} = \frac{0.443}{T_{INT}}$$

The values of C_{INT} and C_{DAC} are determined by solving the following equation for the desired cut-off frequency f_{-3dB} of the system :

$$\frac{\sin(T_{INT} f_{-3dB})}{T_{INT} f_{-3dB}} \cdot \frac{1}{\sqrt{1 + (2\pi f_{-3dB}(T_{INT} + T_S)\frac{C_{DAC}}{C_{INT}})^2}} = \frac{1}{\sqrt{2}} \tag{2.3}$$

For example, solving equation (2.3 for $f_{-3dB} = 5$ kHz gives the capacitors ratio $C_{INT}/C_{DAC} = 2.9$ for $T_{INT} = 48$ µs and $T_S = 1$ µs.

Under normal condition, when only low amplitude action potentials are present at the input, the boxcar sampler integrates for a fixed time period of T_{INT}. This allows a sufficient amplification of the input signal before being converted by the ADC. However, during and after stimulation, the stimulation artifacts will saturate the front-end. To avoid this, the input amplification should be reduced. In order to achieve this, T_{INT} can be reduced to shorten the integration time which decreases the gain of the boxcar sampler. The decreased gain results in an increased noise level from the ADC when referred to the input of the system. Furthermore, the ENBW of this system described in (2.4) increases due to reduction in T_{INT}, resulting in

additional noise folding when sampled on the boxcar.

$$\mathrm{ENBW} = \frac{1}{\mathrm{T_{INT}}} \tag{2.4}$$

To compensate for this, the ADC can be oversampled whenever the integration time is reduced, as long as it satisfies (2.5).

$$\mathrm{N} \cdot \mathrm{T_{INT}} < \mathrm{T_{system}} - \mathrm{T_S} - \mathrm{T_R} \tag{2.5}$$

Here, N is the oversampling ratio and $\mathrm{T_{system}}$ is the data output period of the system. The output of the ADC will be accumulated and then averaged to increase the in-band SNR as explained in Section 1.4.2.

A level-cross detection block, illustrated in Fig. 2.2 is implemented to detect large amplitude input signals. It sends an out-of-range (OOR) flag to the clock generator of the boxcar sampler whenever the voltage over $\mathrm{C_{INT}}$, $\mathrm{V_{INT}}$, crosses the threshold of the level-cross-detection block. The clock generator iterates through a pre-defined look-up table (LUT) containing multiple configurations of gain ($\mathrm{A_v}$) and integration time ($\mathrm{T_{INT}}$) as illustrated in Fig. 2.3. Upon the detection of an out-of-range condition, the clock generator stops the ongoing integration process at the next iteration of the LUT. This procedure ensures fixed integration times and synchronization with the subsequent blocks of the system. If the system stops the boxcar integration immediately after the OOR is flagged instead of using a pre-defined LUT, $\mathrm{T_{INT}}$ must be exactly known to recompute the gain, which requires a very high speed and a high resolution timer. Furthermore, this results in an infinite number of possible gain settings and an asynchronous system which complicates the digital signal processing afterwards. Therefore, a LUT of finite $\mathrm{T_{INT}}$ settings is implemented. The values of $\mathrm{T_{INT}}$ are designed such that during oversampling, the numbers of samples taken corresponds to 2^{n}, where n is an integer. This is necessary to avoid complex digital averaging techniques.

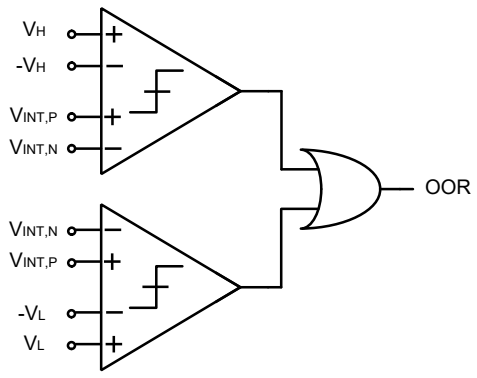


Figure 2.2: Schematic of the level-cross detection block

Figure 2.4 illustrates the timing characteristics of the proposed system architecture. In presence of a high-amplitude signal, the integrated voltage on the capacitor $\mathrm{V_{INT}}$ crosses the OOR

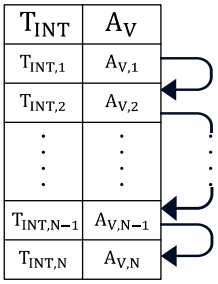


Figure 2.3: An illustration of the look-up table iteration process.

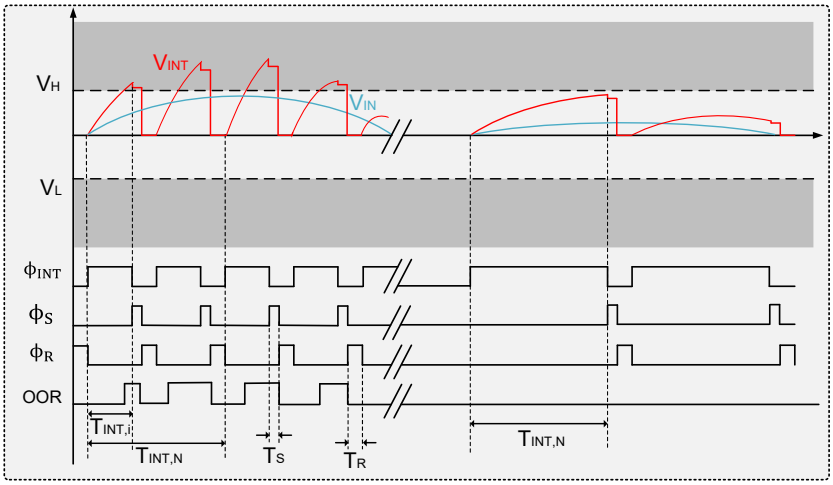


Figure 2.4: Timing diagram of the proposed system where the response to large and small amplitude signals is shown.

threshold, causing the integration to stop at the subsequent iteration of the LUT. This specific gain configuration is locked for the duration equal to T_{system}, which corresponds to the data output rate of the system, and is reset at the start of the next cycle. If the gain is not kept constant during T_{system}, the system can adapt to all the possible gain configurations in the LUT depending on the input signal, resulting in an asynchronous and unpredictable system. In that case, the digital reconstruction block after the ADC should recompute the data according to the gain after every ADC conversion, before being accumulated, which results in more complexity and power consumption. Thus, by locking the gain configuration during T_{system}, the ADC samples can be accumulated before the recomputation block as all the samples have the same gain configuration. Therefore, the power and timing constraints within the following digital blocks are relaxed. If the threshold of the level-cross detectors remain uncrossed for low-amplitude signals, T_{INT} reaches the final iteration $T_{INT,N}$, which can be expressed as:

$$T_{INT,N} = T_{system} - T_S - T_R$$

The presented architecture for neural recording systems automatically control the gain in presence of large amplitude signals by adapting the integration time according to the input signal magnitude. Therefore, large amplitude signals can be kept within the input range of the ADC. This increases the upper limit of input range, which results in an increase of the DR, while

targeting for a compact low-power design. The targeted specifications and the corresponding justifications [42] are shown in Table 2.1.

Table 2.1: Targeted specifications for the proposed closed-loop neural recording interface

Parameter	Value	Justification
Input referred noise	< 10 uVrms	To distinguish the EAP from the noise.
Input voltage swing	200 mVpp	To withstand the stimulation artifact.
Variable Gain	1 - 100 V/V	To prevent front-end saturation while providing sufficient gain to the EAP.
Bandwidth	300 - 5 kHz	Frequency range of the EAP.
ADC Resolution	10 bits	To distinguish different EAPs.

2.2. System Analysis

This section describes the system transfer function and the noise analysis.

2.2.1. Transfer function

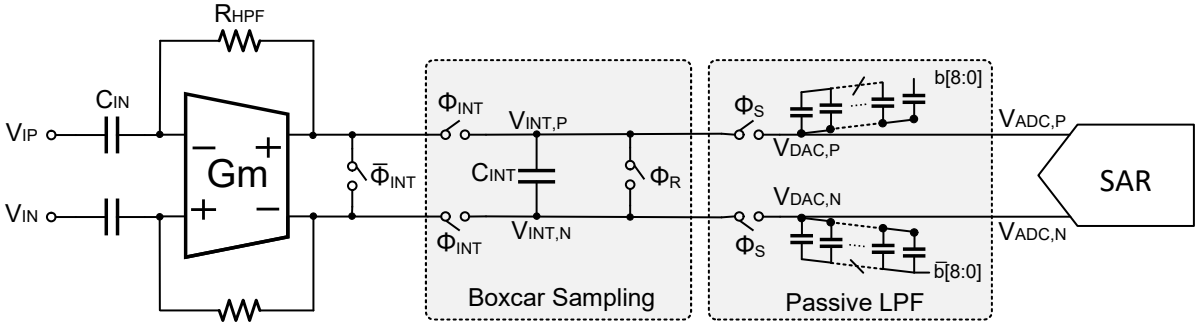


Figure 2.5: Part of the system architecture of which the transfer function is derived.

To have a better understanding of the proposed system, the transfer function of the circuit shown in Fig. 2.5 should be derived. In this case, the input of the ADC is considered as the transfer function output to simplify the derivation. Equation 1.3 already described the transfer function of the boxcar sampled Gm-C integrator. However, this OTA also includes a feedback resistor and input capacitors to implement a high-pass filter with a cut-off frequency shown in (2.1). The $g_m r_o$ term is introduced by applying Miller's theorem to the feedback resistor.

After the boxcar sampling, the signal is further filtered using a passive LPF consisting of switched capacitors. Here, C_{INT} is reused as a switched-capacitor resistor [43]. Therefore, the location of the pole due to the SC-LPF can be described by (2.2).

By combining the transfer functions, a simplified model of the system can be derived as shown in Fig. 2.6. From the transfer functions, it becomes evident that the low-pass pole of both the boxcar sampler and the SC-LPF will exhibit a shift in response to integration time adjustments.

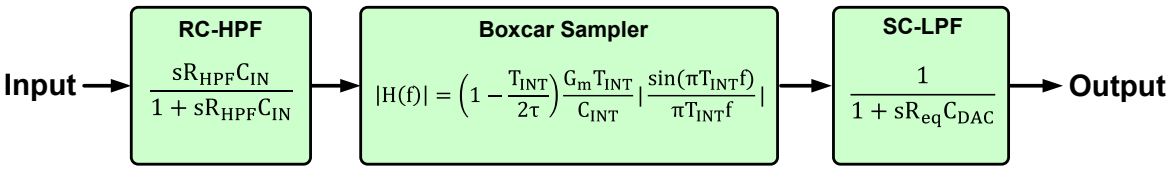
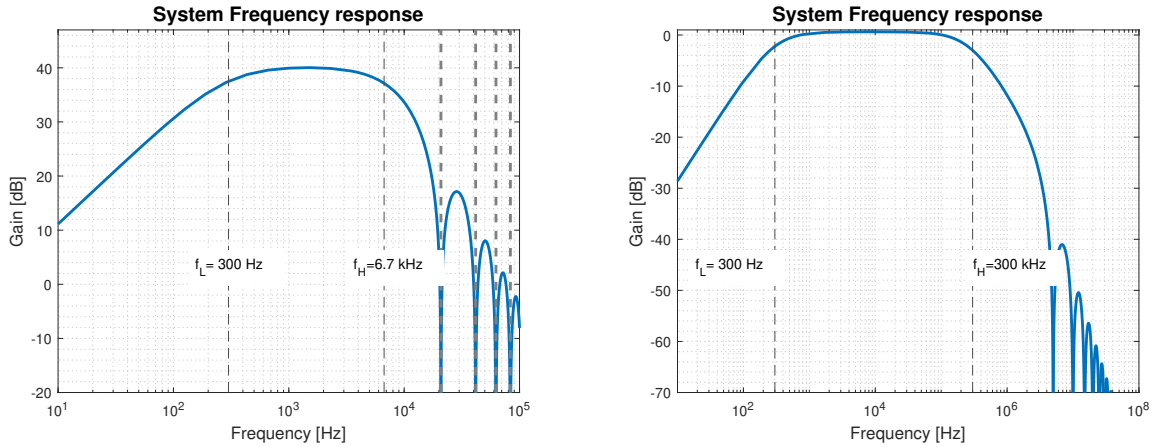


Figure 2.6: Part of the system architecture described with transfer functions.

Figure 2.7 illustrates the magnitude characteristics of the overall transfer function of the black box representation in two extreme cases of T_{INT}. It is evident that as T_{INT} is reduced, the system's gain decreases, aligning with the system requirements. However, this reduction in T_{INT} also results in a displacement of the low-pass pole to a higher frequency, the consequences of which are discussed in Section 2.2.2.



(a) $T_{INT} = 48\,\mu s$ **(b)** $T_{INT} = 200\,ns$

Figure 2.7: Frequency response of the black box model

2.2.2. Noise analysis

The noise characteristics of the system should be investigated to understand how these changes impact the fidelity of the input signal. For the targeted application, only one input node is connected to the signal while the other functions as a reference node. Therefore, the noise analysis is performed single-ended. However, due to the symmetry of the system, the differential input noise can be calculated by scaling the single-ended noise by a factor of 2. The noise sources discussed in this section are highlighted in Fig. 2.8.

The noise exhibited by the OTA is directly referred to the input and is strongly dependent on its circuit architecture. For now, assume that the input-referred noise power spectral density (PSD) of the OTA is equal to that of a single transistor as defined in (2.6).

$$V^2_{n,OTA} = \frac{4k_B T\gamma}{g_{m,OTA}}[V^2\,Hz^{-1}] \tag{2.6}$$

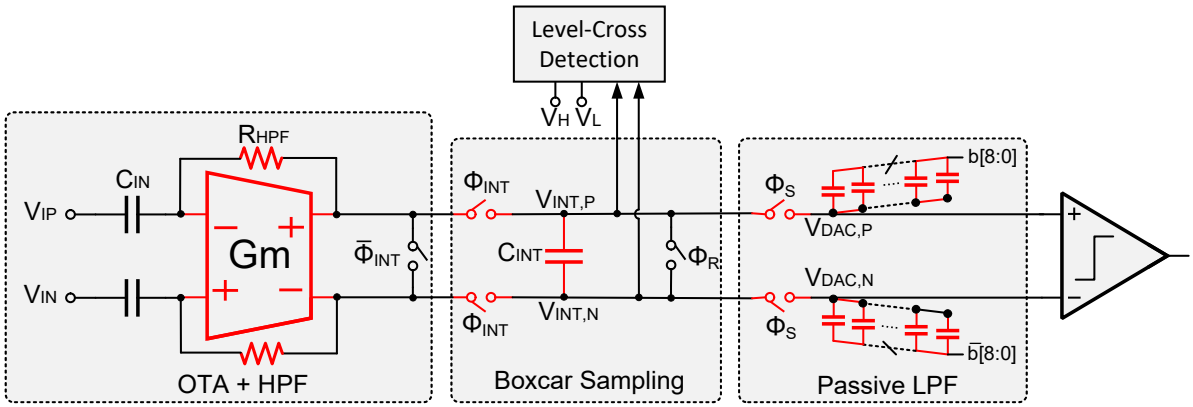


Figure 2.8: Part of the system architecture with the noise sources highlighted in red.

Again, by applying Miller's theorem to R_{HPF}, the input-referred noise PSD of the resistor can be described as in (2.7).

$$V^2_{n,R_{HPF}} = \frac{4k_B T R_{HPF}}{(g_{m,OTA} r_o)^2} [V^2\,Hz^{-1}] \tag{2.7}$$

The level-cross detection instance consists of two continuous-time comparators with inputs connected to C_{INT}. As the output of the LCD is a digital signal, the LCD noise does not affect the output unless the noise is significantly larger than the threshold voltage of the comparators. Therefore, the noise contribution of the LCD is ignored. The boxcar integrator introduces sampling noise which is equal to:

$$V^2_{n,rms,BC} = \frac{k_B T}{C_{INT}} [V^2] \tag{2.8}$$

The sampling voltage noise resulting from the boxcar is attenuated by $\frac{C_{INT}}{C_{INT}+C_{DAC}}$ due to charge sharing of C_{INT} and C_{DAC}.

The sampling noise of the passive LPF is defined as:

$$V^2_{n,rms,LPF} = \frac{k_B T}{C_{DAC}} [V^2] \tag{2.9}$$

where C_{DAC} is the single-sided total capacitance of the SAR DAC.

Referring all the noise sources to the input gives the equation shown in (2.10)

$$V^2_{n,rms,in} = V^2_{n,OTA} \cdot BW + \frac{V^2_{n,rms,BC} \cdot \frac{(C_{INT}}{C_{INT}+C_{DAC}})^2}{A_v^2} + \frac{V^2_{n,rms,LPF}}{A_v^2} \tag{2.10}$$

Here, BW is the system bandwidth and R_{on} is the on-resistance of the SC-LPF sampling switch. A_v is the voltage gain at the output of the boxcar The system bandwidth is directly related to the integration time and from the transfer function analysis in section 2.2.1, it was concluded that the bandwidth changes with the integration time T_{INT}. Therefore, more noise will be folded into the bandwidth of interest at the input of the ADC when decreasing T_{INT}. Furthermore, the reduction of T_{INT} results in a lower gain. Therefore, the sampling noises of the boxcar and the SC-LPF become more dominant as the gain decreases. Overall, the reduction of integration time lead to increased input-referred noise. During normal operation, the noise of the OTA is the most dominant at the ADC input, as this is amplified by A_v^2, the sampling noises can be neglected. As the integration time decreases, the sampling noises become consistently more dominant.

2.2.3. Variable Gain Configuration

The system is configured to have multiple gain configurations to adapt to varying input amplitudes. To achieve this, T_{INT} is adjusted by the clock generator to limit the current integrated over C_{INT}. The voltage gain from the input to V_{INT} is defined in (2.11).

$$A_v = \frac{V_{INT}(t)}{V_{in}(t)} = g_m r_o (1 - e^{-T_{INT}/r_o C_{INT}}) \tag{2.11}$$

with $T_{INT}|_{max} = 48\,\mu s$. Using the parameters in Table 2.3, the gain of integrator is simulated and illustrated in Fig. 2.9. Due to the large integration capacitor, the gain is not fully settled at $T_{INT}|_{max}$. However, this is necessary to obtain a low gain at small integration times. For $T_{INT} << r_o C_{INT}$, the gain can be approximated as:

$$A_v \approx \frac{g_m T_{INT}}{C_{INT}}$$

The system uses a pre-calibrated look-up table to store the gain value for each configuration and is shown in Table 2.2. The ratios of the highest gain configuration with respect to the lower gain configurations are calculated, such that the digital processing stage can recompute the input by multiplying this ratio with the output data. This requires dividers to recompute the gain. If the gain can be calibrated to be multiples of two as illustrated in Fig.2.10, only a logic shifter is required. However, the exponential part of the boxcar gain settling results in a non-linear gain configuration. To obtain gains in power of two, a very high resolution timer in the order of 1 ns is required, which would require an external clock of 1 GHz. Therefore, a divider is implemented for the proposed system.

Table 2.2: Gain configuration with different integration times.

T_{INT} **[µs])**	0.2	0.4	0.8	1.6	2.8	8	48
A_v **[V/V]**	0.99	1.98	3.92	7.69	13.06	32.96	90.83

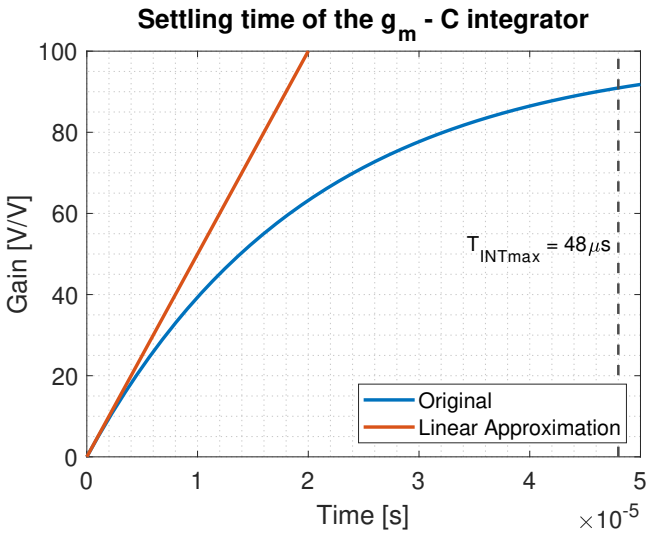


Figure 2.9: Gain simulation of the $g_m - C$ integrator with exponential settling and linear approximation.]

T_{INT}	A_V
$T_{INT,1}$	$A_{V,N}$ / 2^N
$T_{INT,2}$	$A_{V,N}$ / 2^(N-1)
⋮	⋮
$T_{INT,N-1}$	$A_{V,N}$ / 2
$T_{INT,N}$	$A_{V,N}$

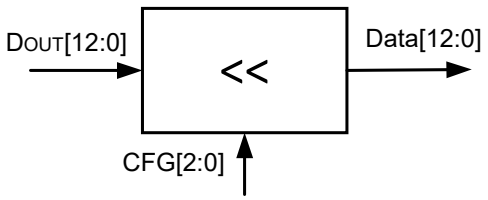


Figure 2.10: Digital processing requirement of the output stage

The design parameters used to verify the analysis are shown in Table 2.3. These parameters are chosen such that the targeted specifications of the system is met. The mathematical analysis performed in this chapter verifies the potential adaptation of this system architecture for the target application in theory.

Table 2.3: Design parameters used to simulate the transfer function of the system

Parameter	Value	Justification
g_m	4 µS	To meet the input-referred noise requirement and the desired gain.
r_o	25 MΩ	To meet the desired gain and the OTA settling speed.
C_{IN}	1.1 pF	To meet the input impedance requirement for the target application.
R_{HPF}	75 GΩ	To implement a high-pass pole at the desired frequency.
C_{INT}	400 fF	To meet the desired gain and settling within time window and to implement a SC-LPF.
C_{DAC}	128 fF	To implement a SC-LPF [1].
T_{INT}	200 ns -48 µs	To meet the variable gain requirement.

3

Circuit Implementation

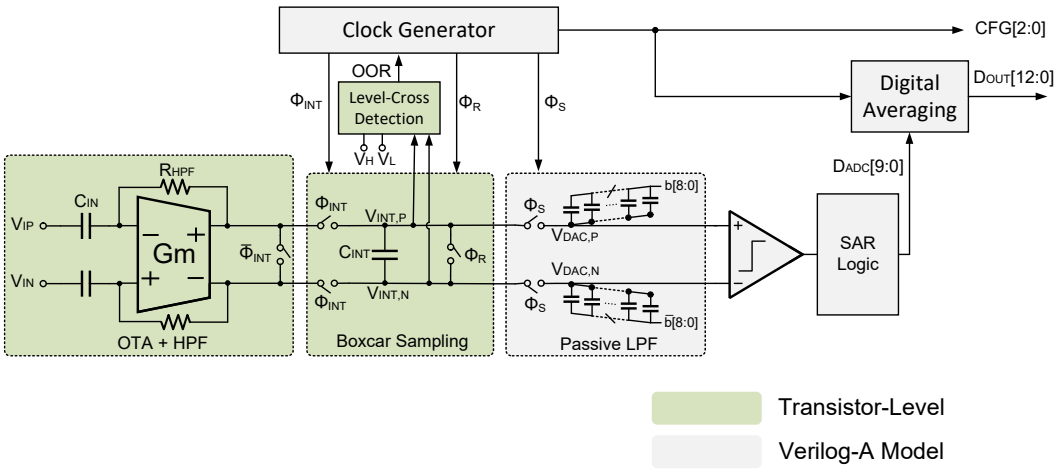


Figure 3.1: Proposed system architecture with color indicating the level of implementation.

This chapter describes the circuit implementation of the proposed system architecture. For proof-of-concept, the ADC (except the DAC) and the digital blocks are designed in Verilog-A while the remaining blocks are implemented in transistor-level. The main design challenge of the proposed system is the OTA, as it should maintain linear over a wide input range ($\sim \pm 100\,\text{mV}$) while consuming minimum area and power. The level-crossing comparators should be designed according to the timing requirements of the clock generator.

3.1. OTA

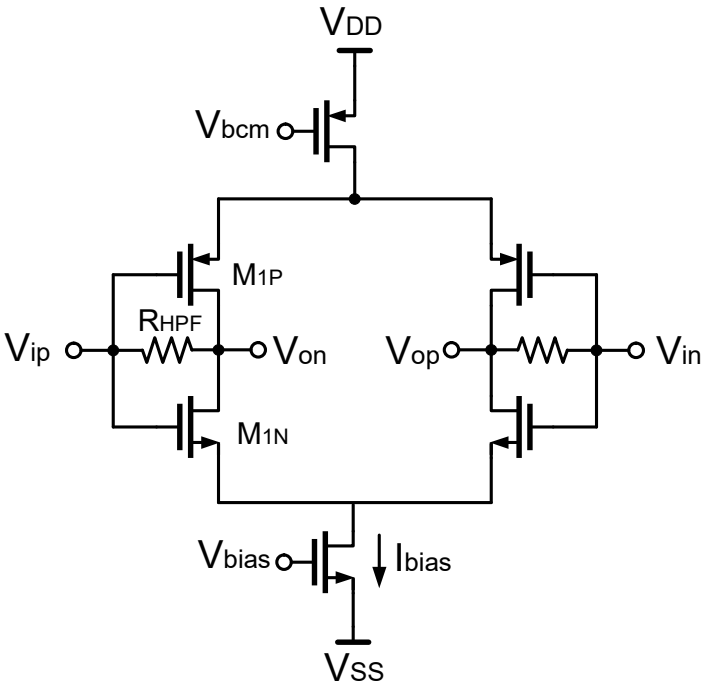


Figure 3.2: Schematic of the implemented inverter-based OTA.

An inverter-based OTA is used for this system as this architecture can achieve a low noise efficiency factor (NEF) [44]. Figure 3.2 shows the schematic of an inverter-based OTA with self-biasing resistor and common-mode feedback[1]. The gain of this OTA is described in (3.1) and the input-referred thermal noise PSD is described in (3.2). The OTA should be designed to have an input-referred noise of $10\,\mu V_{rms}$.

$$A_v = -(g_{m,n} + g_{m,p})(r_{o,n} || r_{o,p}) \quad [V/V] \tag{3.1}$$

$$V_{n,OTA} = 2 \cdot \frac{4k_B T(\gamma_n + \gamma_p)}{g_{m,n} + g_{m,p}} \quad [V^2\,Hz^{-1}] \tag{3.2}$$

Assuming that $\gamma_n = \gamma_p$ and $g_{m,n} = g_{m,p}$, the equation in (3.2) simplifies to (3.3).

$$V_{n,OTA} = \frac{8k_B T \gamma_{n,p}}{g_{mn,p}} \quad [V^2\,Hz^{-1}] \tag{3.3}$$

[1]The common-mode feedback circuit is implemented by a finite gain and finite BW Verilog-A op-amp model with resistive sensing.

The flicker noise of the OTA is described in (3.4)

$$V_{1/f,OTA,} = \left(\frac{2K_n}{C_{ox,n}WL} + \frac{2K_p}{C_{ox,p}WL}\right) \int \frac{df}{f} \quad [V^2\,Hz^{-1}] \tag{3.4}$$

OTA Design

The OTA is designed using the g_m/I_D methodology [45]. As the output current of the OTA is integrated over C_{INT} with different integration times, the worst case scenario should be considered. The maximum input voltage at which the OTA must be linear is 100 mV, while the minimum integration time is 200 ns. Therefore, the slew-rate of the OTA should be larger than:

$$SR = \frac{I_{out}}{C_{INT}} = \frac{\Delta V}{\Delta t} = 0.5\,V\,\mu s^{-1} \tag{3.5}$$

To achieve this, the output current of the OTA should be 200 nA. Therefore, the circuit should at least be biased above 200 nA. Hence, the OTA is biased at 250 nA. To maximize the noise efficiency, the g_m/I_D-ratio should be chosen to be $25\,S\,A^{-1}$, which will bias the transistors in weak inversion. Therefore, the g_m of the each transistor in the inverter is 3.125 µS. The supply voltage is set to $V_{DD} = 1.8$ mV to comply with the wide input range.

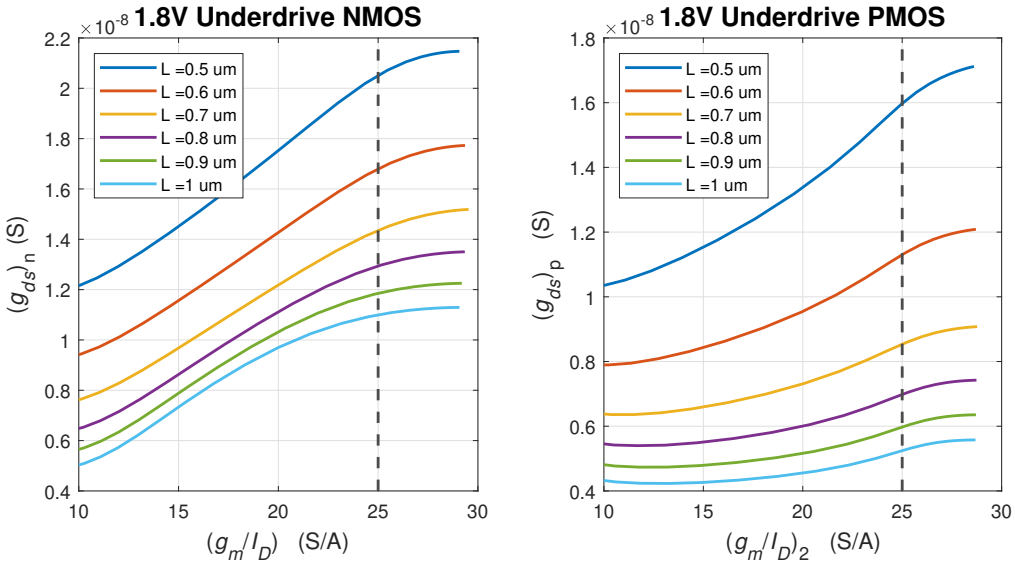


Figure 3.3: g_{ds} vs g_m/I_D for 1.8 V nmos and pmos devices computed using pre-generated LUT.

As illustrated in Fig. 3.3, the length of the nmos and pmos devices, L_n and L_p, at a given inversion level can be computed for the given DC gain. However, choosing the lengths for the desired gain will lead to short devices. Since the flicker noise is dominant at low-frequencies, short devices will introduce large amount of flicker noise. Therefore, the length is increased every iteration to meet the input-referred noise requirement while the other parameters are

recomputed again. The width of the device can then be computed by the current density J_D vs g_m/I_D plot as illustrated in Fig. 3.4 using equation (3.6).

$$J_D = \frac{I_D}{W} \tag{3.6}$$

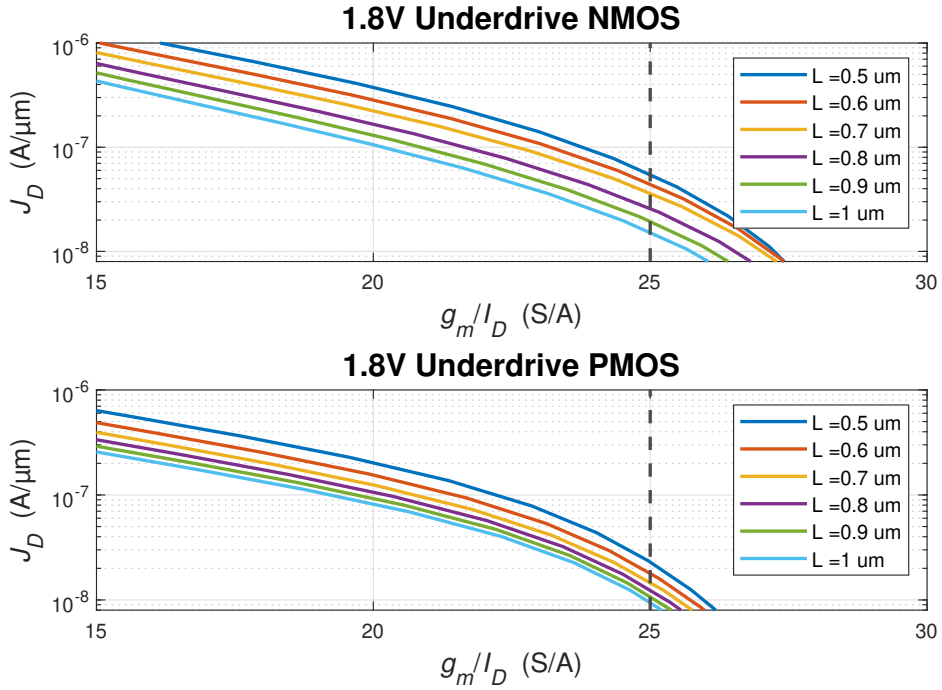


Figure 3.4: J_D vs g_m/I_D for 1.8 V nmos and pmos devices computed using pre-generated LUT.

Table 3.1 shows the design parameters and the OTA sizing according to the g_m/I_D design methodology and the actual sizing after fine-tuning.

Table 3.1: Inverter OTA sizing using pre-computed LUT

Device	**L [µm]**	**W [µm]**	$\mathbf{g_m}$[S]	$\mathbf{g_m/I_D}$[S A^{-1}]
M1p	1	3.5	3.13	24.7
M1n	1	3	3.19	24.7

OTA Performance

Figure. 3.5 illustrates the voltage transfer curve of the OTA. With the common mode set at 850 mV, the OTA achieves a linear input range of $\pm$200 mV.

The AC magnitude plot is illustrated in Fig. 3.6. As shown, the open loop gain of the OTA exceeds the system specification of 40 dB due to the W/L of the devices. However, the gain

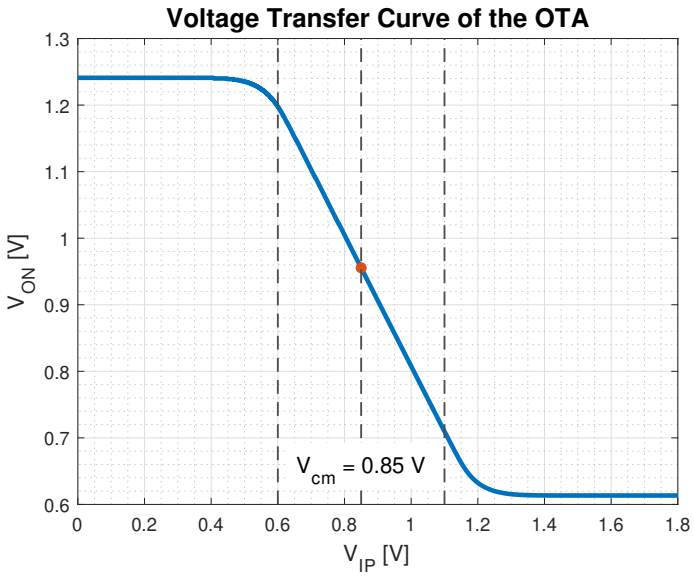


Figure 3.5: Voltage transfer curve of the inverter-based OTA.

of the boxcar sampler will be lower due to time-limited integration. The high-pass pole is achieved by using C_{in} of 1.1 pF and R_f of 75 GΩ using pseudo-resistors. The -3 dB bandwidth of the OTA is located at 1 MHz.

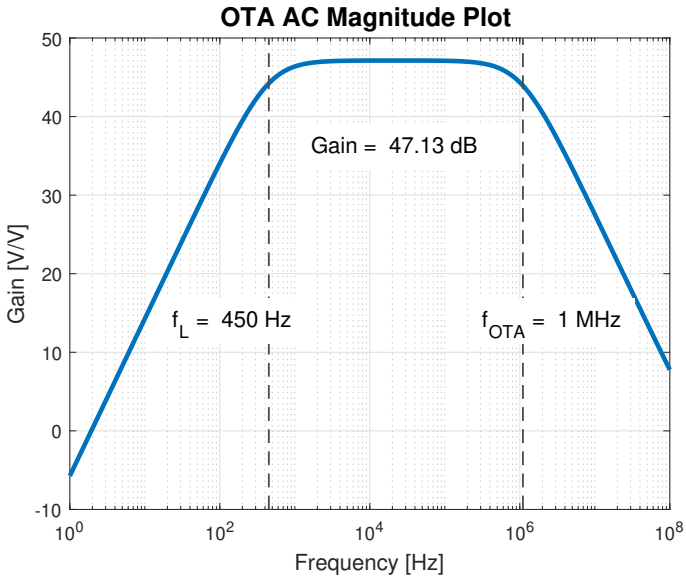


Figure 3.6: AC magnitude plot of the inverter-based OTA.

Figure 3.7 illustrates the transient simulation of the OTA with sine wave input at V_{IP}. After complete settling, the gain of the OTA corresponds to the AC simulation.

The output noise performance of the OTA without filtering is illustrated in Fig. 3.8. As expected, the flicker noise is dominant in the bandwidth of interest. The noise integral of the OTA is illustrated in 3.9. Without filtering, the noise introduced by the OTA cannot meet the desired noise specifications.

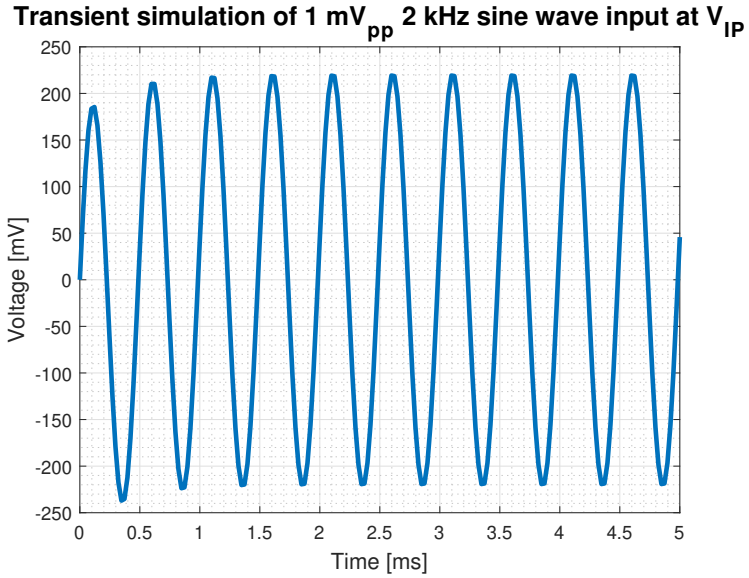
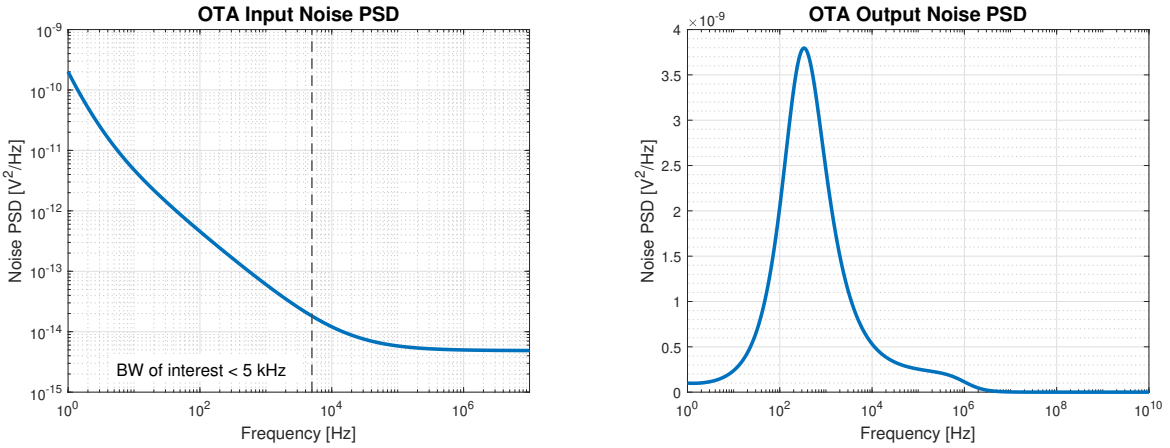


Figure 3.7: Transient simulation of the inverter-based OTA with initial settling from 0 to 1 ms.



(a) Input-referred noise PSD **(b)** Output-referred noise PSD

Figure 3.8: Noise PSD of the inverter-based OTA with high-pass filter.

Figure 3.10 illustrates the noise performance after filtering using the boxcar sampler and the SC-LPF. Due to the discrete-time components, a transient noise analysis is performed over a time interval of 10 ms and the RMS value of the noise at node V_{INT} is calculated [2]. Hence, the input-referred noise of the OTA after filtering is calculated as:

$$V_{n,in,rms} = \frac{V_{n,int,rms}}{A_v} = 10.22\,\mu V_{rms}$$

[2]The SC-LPF samples and holds the noise for a certain period, which would require a very long transient simulation to increase the randomness to obtain an accurate representation of the actual RMS noise. Since the sampling noise of the CDAC is negligible compared to the OTA noise, the RMS noise at V_{INT} is calculated

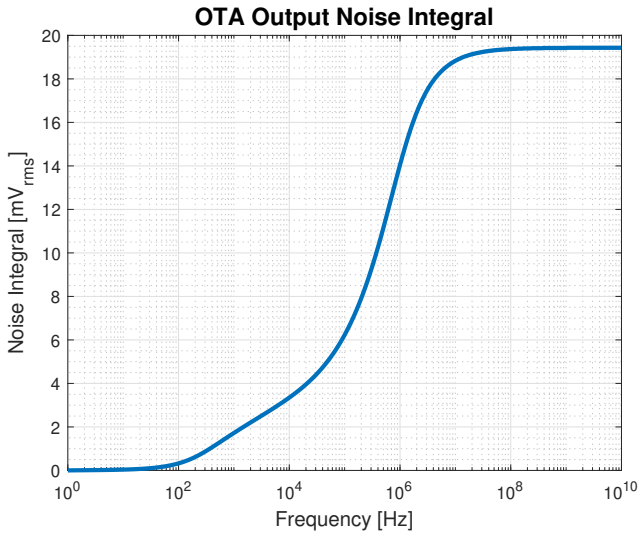


Figure 3.9: Noise integral of the inverter-based OTA.

The obtained RMS noise is within the margin of the required noise specification.

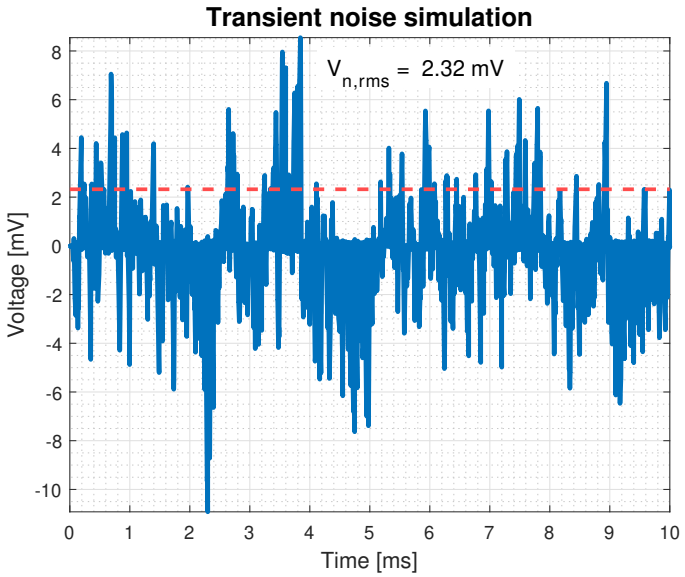


Figure 3.10: Transient noise simulation of the inverter-based OTA with boxcar sampler and SC-LPF.

3.2. Level-Crossing Comparator

The level-crossing comparator is used to generate an out-of-range flag for the clock generator to stop the integration. Therefore, the differential voltage V_{INT} must be continuously monitored and compared to a reference voltage. Two comparators are required to account for both positive and negative voltages. The differential architecture of the system requires a

continuous-time comparator that compares the differential input with a reference voltage. An architecture used in [46] meets this criteria and is illustrated in Fig. 3.11. The continuous-time

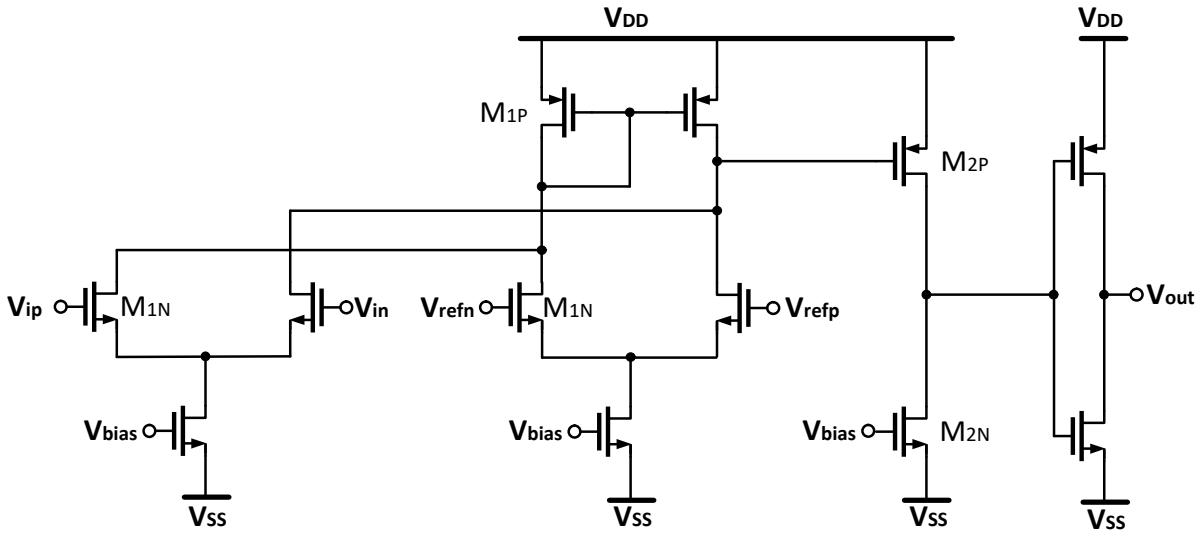


Figure 3.11: Schematic of the continuous-time comparator used for the level-cross detection.

comparator consists of a two-stage open-loop amplifier followed by an inverter. This is similar to a conventional two stage open-loop comparator. However, the two extra current branches are introduced to compare the differential reference voltage to the differential input. The clock generator reads the OOR flag every $\mathrm{T_{cycle}}$ = 100 ns. Therefore, the delay of the comparator $\mathrm{T_d}$ should be designed such that $\mathrm{T_d} << \mathrm{T_{cycle}}$.

To achieve low-latency, small lengths should be used for the all the input transistors of both stages. To achieve sufficient amplification, the input pairs should be sized for large widths. The mismatch of the input pairs will introduce an input-referred offset which will leads to an inaccuracy when comparing the voltage levels. This creates a trade-off between the settling speed and the input-pair offset.

The effect of random variations in the device area mismatch should be accounted for. Therefore, a local Monte-Carlo simulation is performed to verify the offset performance of the comparator. Illustrated in Fig. 3.12, the design is shown to be relative robust against random mismatch variations as at 3σ, the offset is still 5x smaller than the reference voltage, which is set to $\pm$100 mV. Additional fingers in combination with switches can be connected at the input pairs to introduce an imbalance at the input pairs to compensate for the mismatch-induced offset or the comparator can be auto-zeroed to minimize the offset [46].

Figure 3.13 illustrates the delay of the comparator when different input voltages are applied. For large amplitudes, the comparator delay is within the margin of requirements. However, when small amplitudes are applied, the decision time of the comparator can cause the clock generator to miss an OOR flag when the actual voltage already crossed the threshold. Nevertheless, it is only necessary for the comparator to generates an OOR flag in case of stimulation artifacts with large amplitudes. Since the input signal is continuous-time and either ramping up or down in amplitude rapidly, the speed of the comparator is sufficient for the clock generator.

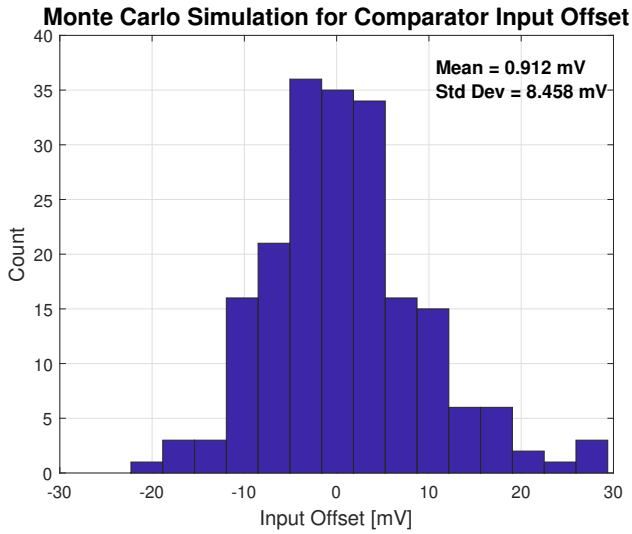


Figure 3.12: Monte Carlo simulation to simulate the effect of mismatch on the comparator offset.

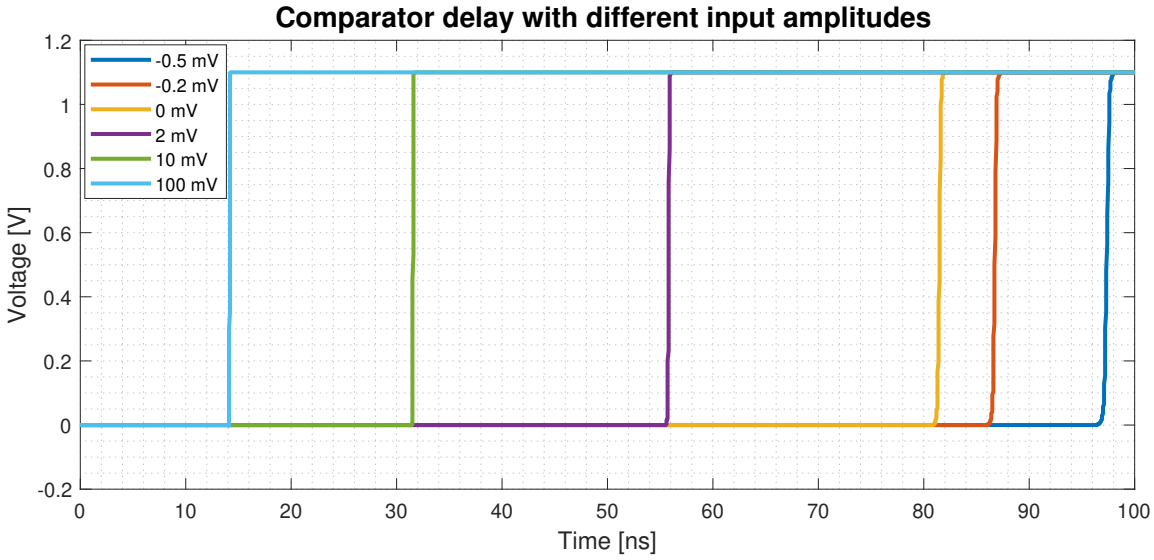


Figure 3.13: Comparator delay simulated using step input with varying amplitudes. The step input is applied at 200 ns

3.3. Clock Generator

The clock generator is used to generate all the clock signals for the switches and operates with a master clock at 10 MHz. The flowchart of the clock generator is illustrated in Fig. 3.14.

As mentioned in chapter 2, the clock generator iterates through a look-up table to determine the

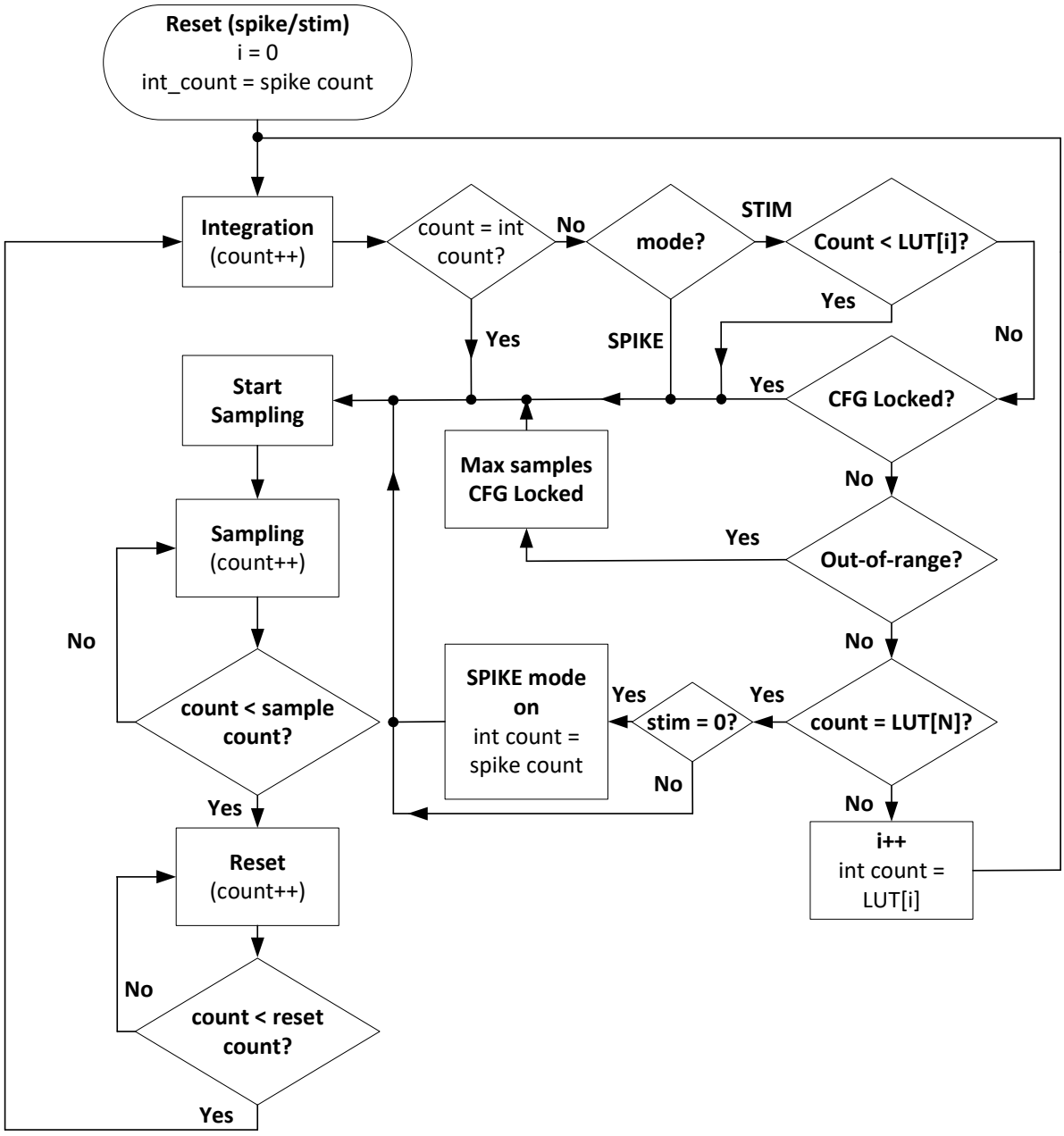


Figure 3.14: Flowchart of the clock generator

integration time. The clock generator starts the integration after reset and increases the counter every clock cycle. If there is no stimulation, the clock generator is set in spike mode with $\mathrm{T_{INT}} = 48\,\mu\mathrm{s}$ as the system output rate is 20 kHz. If there is stimulation, the clock generator checks iterates through the LUT. When the counter reaches the corresponding integration time, the sampling clock is activated for $\mathrm{T_S} = 1\,\mu\mathrm{s}$. After sampling, reset is activated for $\mathrm{T_R} = 1\,\mu\mathrm{s}$.

During stimulation, the integration time configuration is locked for every $10\,\mu\mathrm{s}$ as the output rate of the system during stimulation is 100 kHz, which is required to properly reproduce the stimulation artifact. The configuration is locked when the level-cross comparator generates an

OOR flag. Furthermore, the number of samples taken every 10 µs is also locked. Table 3.2 shows the number of samples corresponding to the different integration times. If OOR is not flagged, integration is continued until the last iteration of the LUT is reached. Note that during stimulation, the last iteration LUT[N] corresponds to 8 µs due to the higher system output rate. When this configuration is reached, the clock generator will only be set in spike mode if the stimulation flag is off. This is necessary to account for the positive to negative transition of the stimulation artifact, as during the transition, the amplitude of the artifact crosses zero, if the integration only comprise of low amplitude signals, the system assumes that there is no artifact present anymore.

Furthermore, the spike mode is not immediately activated after stimulation, as the residual artifact could saturate the front-end when using a high-gain configuration. From the flowchart, it can be derived that the OOR flag should not be triggered after stimulation, before going into spike mode. This indicates that the residual artifact has decreased to a sufficient low level, before the highest gain configuration can be used. Hence, the overall implementation of this clock generator improves the robustness of the system.

Table 3.2: Integration time configurations with the corresponding samples taken every 10 µs.

Tint (us)	0.2	0.4	0.8	1.4	3.8	9	49
Samples	8	4	4	4	2	1	1
A_v **[V/V]**	2.64	5.12	10.41	18.03	48	91	202

4

System Implementation

This chapter focuses on the implementation of the system architecture illustrated in Fig. 3.1. A simplified black-box diagram of the system is illustrated in Fig. 4.1. The circuits designed in chapter 3 are integrated in the system. To verify whether the system meets the specifications listed in Table 2.1, different tests are performed. Section 4.1 presents the input dynamic range of the system. Section 4.2 presents the step response of the system under different input conditions. In section 4.3, sine waves with varying input amplitudes are reconstructed. Furthermore, an artificial stimulation artifact and a neural spike is generated at the positive input of the system to show the reconstructed signal.

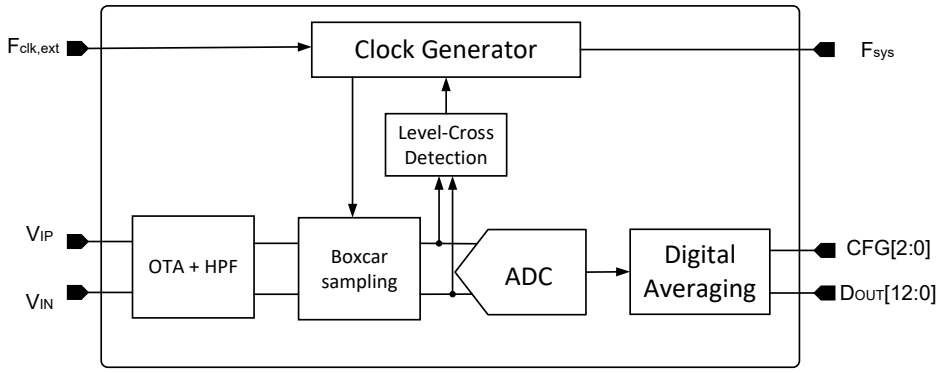


Figure 4.1: Simplified black-box representation of the system architecture

4.1. System input range

The input range of the system is limited by the ADC input range and the boxcar gain configurations. The reference voltage of the ADC is set to $\mathrm{V_{REF}} = 200\,\mathrm{mV}$. Therefore, the input range of the ADC is defined as:

$$-\mathrm{V_{REF}} \leq \mathrm{ADC_{IN}} \leq \mathrm{V_{REF}}$$

The lowest achievable gain: $\mathrm{A_{v,min}} = 2.64\,\mathrm{V\,V^{-1}}$ is obtained at $\mathrm{T_{INT}} = 200\,\mathrm{ns}$. Due to charge sharing properties of the SC-LPF, the sample on $\mathrm{V_{INT}}$ is attenuated after sampling on the CDAC, by approximately:

$$\mathrm{A_{v,SC}} = 1 - \frac{\mathrm{C_{DAC}}}{\mathrm{C_{INT}} + \mathrm{C_{DAC}}} = 0.85$$

Therefore, the largest input signal that will saturate the ADC is defined as:

$$\mathrm{V_{IN,PP}} = 2 \cdot \frac{\mathrm{V_{REF}}}{\mathrm{A_{v,min}A_{v,SC}}} = 89.1\,\mathrm{mV}$$

To verify the dynamic range of the system, multiple 2 kHz sine-waves with varying amplitudes are applied to the positive input of the system, the negative input is not used and kept at a steady DC reference voltage [1]. Figure 4.2 illustrates the frequency response with the signal-to-noise and distortion ratio (SNDR) of the system output when 2 kHz sine-waves with multiple amplitudes are applied to the input.

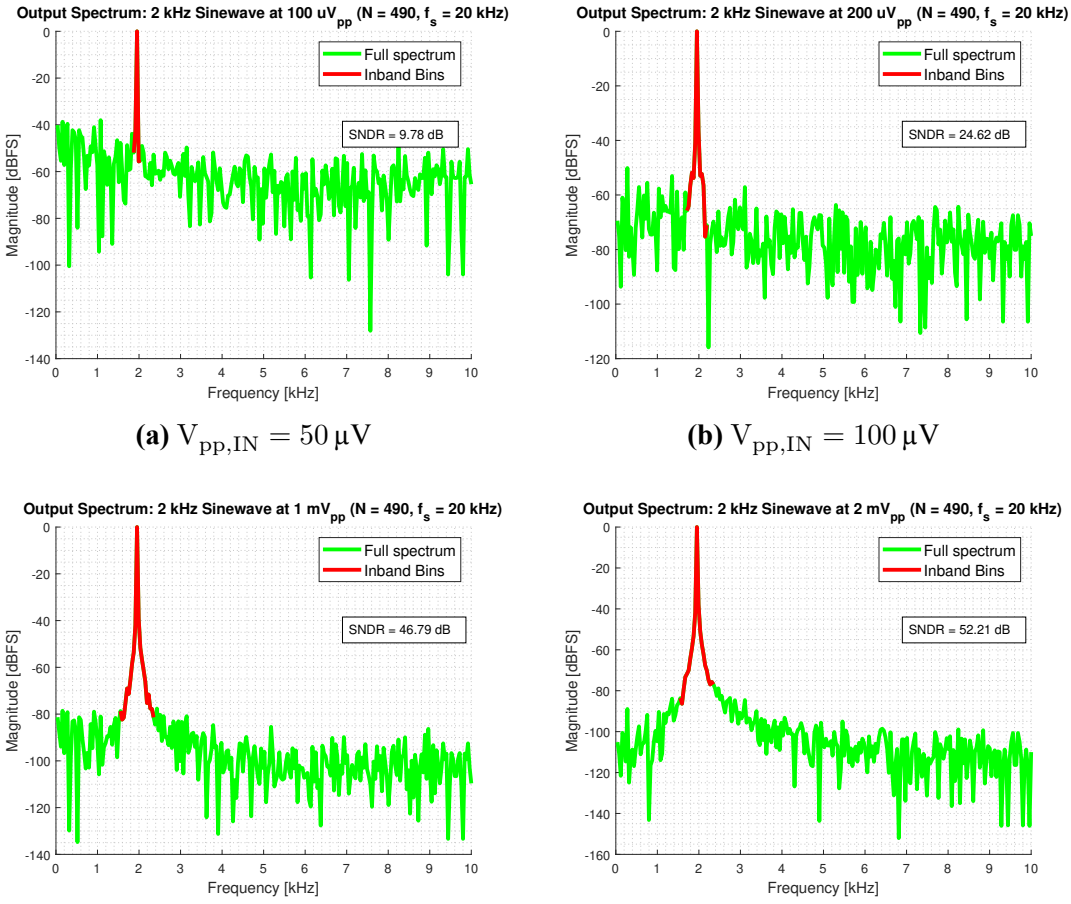
For this system, the frequency response of a full-scale input sine wave is illustrated in Fig. 4.2d. The noise introduced by the system degrades the signal-to-noise ratio (SNR) by approximately 10 dB as an ideal 10-bit ADC with quantization noise only results in an SNR of ∼63 dB when a full-scale sine-wave input is applied. The SNR is defined as:

$$\mathrm{SNR} = 20\log_{10}\left(\frac{\mathrm{A}}{\sqrt{2}\mathrm{V_{n,rms}}}\right)$$

where A is the peak amplitude of a sine-wave and $\mathrm{V_{n,rms}}$ the RMS noise voltage, both at the input of the ADC.

Figure 4.3 illustrates the frequency response when large amplitude sine waves are applied at the input. Due to the adaptive gain implementation, the signal level at the ADC input is within the full scale, thus avoiding saturation. However, the frequency responses for Fig. 4.3c and 4.3d show harmonic distortions, which could be caused by the relative gain error between the gain configurations. Even though the distortion results in a degradation in the SFDR, the

[1] The targeted application of this system uses one working electrode and one reference electrode for each channel



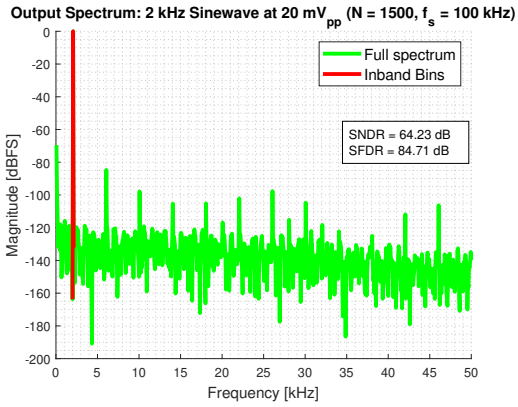
(a) $V_{pp,IN} = 50\,\mu V$ **(b)** $V_{pp,IN} = 100\,\mu V$

(c) $V_{pp,IN} = 500\,\mu V$ **(d)** $V_{pp,IN} = 1\,mV$

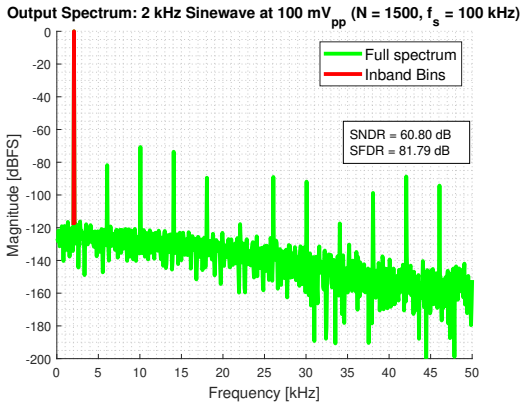
Figure 4.2: Frequency response of the total system with 2 kHz sine-wave input sampled at 20 kHz.

overall SNDR actually improves. This is due to the fact that the large input amplitude leads to a lower gain configuration, resulting in a lower noise at the input of the ADC. This is illustrated in Fig. 4.4, where the difference in the RMS noise voltage can be seen. Hence, as the signal amplitude at the input of the ADC is close to full scale, while the RMS noise voltage is reduced, the SNR improves. Furthermore, at lower gain configurations, the ADC is oversampled, which also increases the SNR slightly. When reaching the limit of the linear input range of the OTA (Fig.4.3c and 4.3d), the distortion becomes more dominant and visible, leading to a degradation in the SNDR.

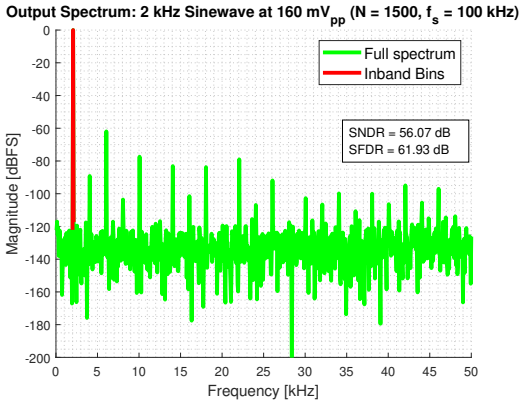
Figure 4.5 illustrates the SNDR versus multiple input amplitudes. The upper-limit of the dynamic range is calculated from the input signal range with a SNDR > 50 dB. This results in an overall dynamic range of 69.5 dB.



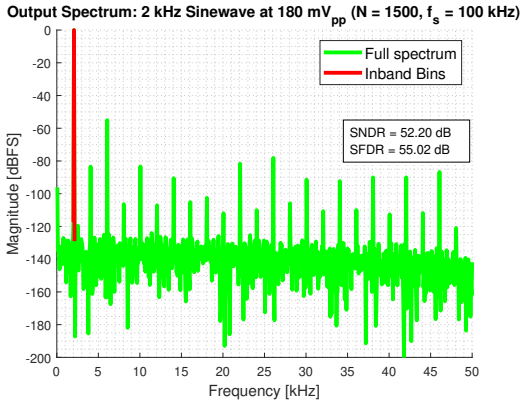
(a) $V_{pp,IN} = 20\,mV$



(b) $V_{pp,IN} = 50\,mV$

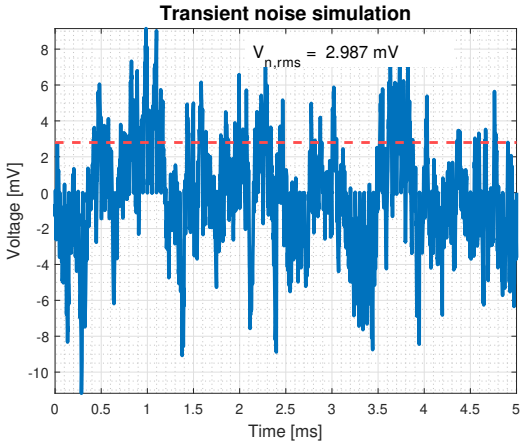


(c) $V_{pp,IN} = 80\,mV$

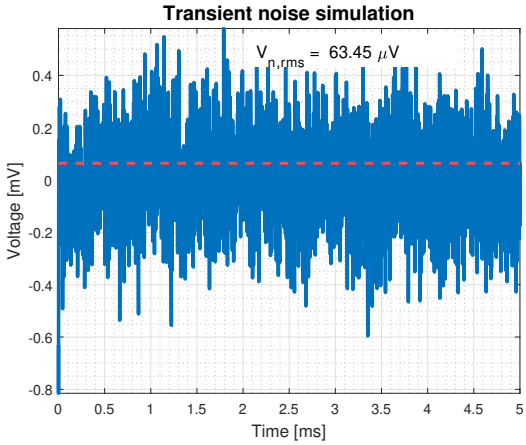


(d) $V_{pp,IN} = 90\,mV$

Figure 4.3: Frequency response of the total system with 2 kHz sine-wave input sampled at 100 kHz.



(a) Highest gain configuration with$T_{INT} = 49\,\mu s$



(b) Lowest gain configuration with $T_{INT} = 200\,ns$

Figure 4.4: Transient noise measured at the output of the boxcar sampler.

4.2. System step response

The dynamic behaviour of the system results in the necessity of verifying its step-response. To verify this, unit-step signals with varying amplitudes are applied at the positive input. Figure

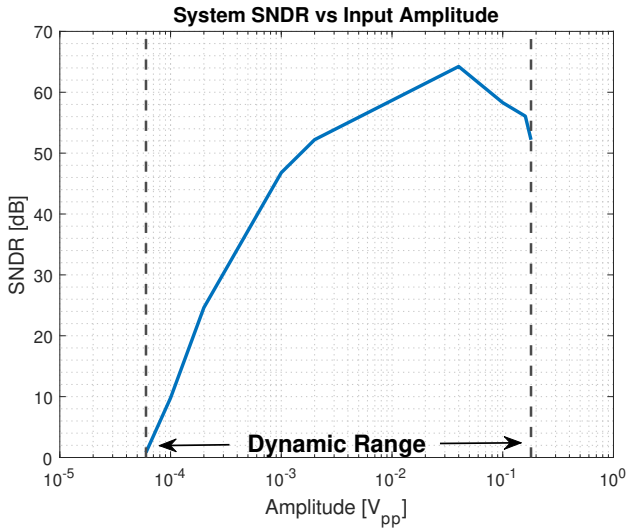
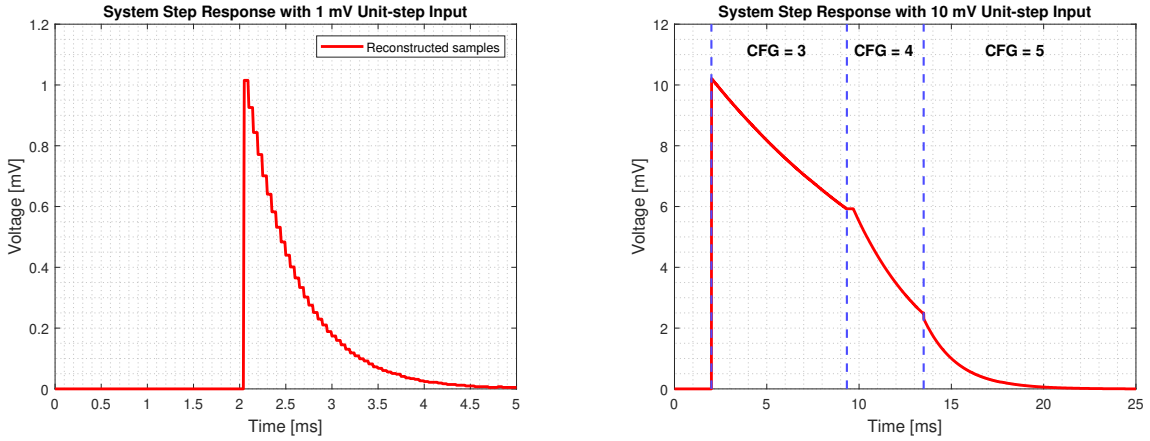


Figure 4.5: System SNDR vs input amplitude

4.6a illustrates the step response of the system when a 1 mV step function is applied at the input at $t = 2$ ms. Due to the small amplitude, the system uses the largest gain configuration. After $\sim$3 ms, the system reaches steady state. When a 10 mV step input is applied, the system uses three different gain configurations as illustrated in Fig. 4.6b. For lower gain configurations, the system settles slower compared to higher gain configurations.

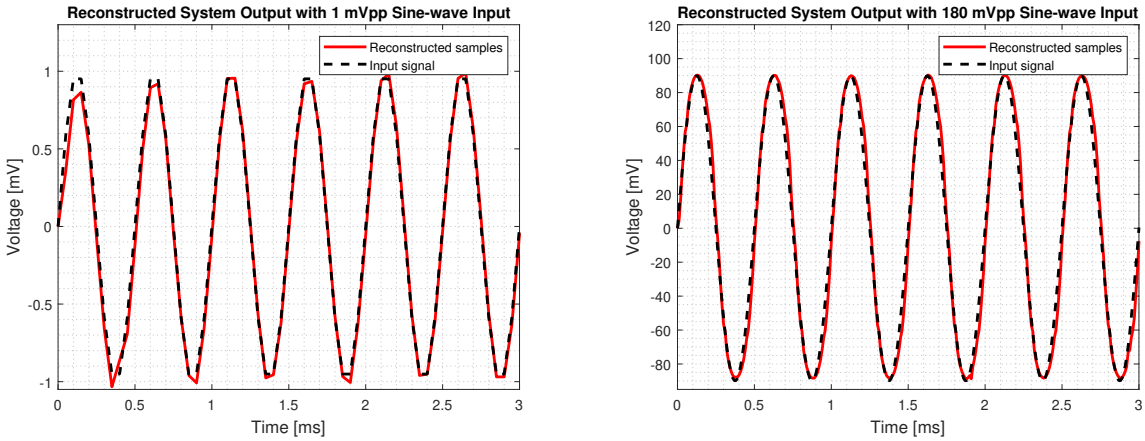


(a) 1 mV **(b)** 10 mV

Figure 4.6: Step response of the total system with 1 mV input step.

4.3. System recording

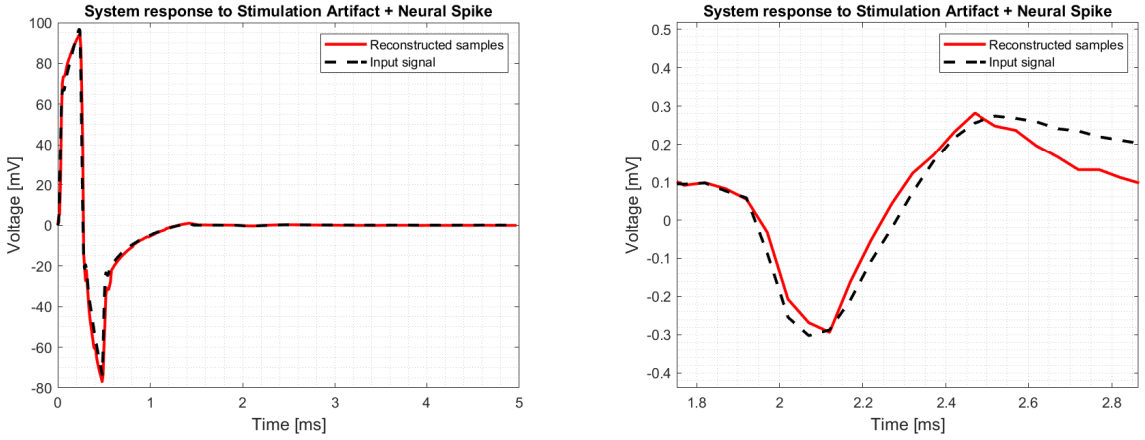
Figure 4.7 illustrates the reconstructed signal when a 2 kHz sine-wave of 1 mV_{pp} and 180 mV_{pp} is applied to the input. It is visible that at the extremes of the 180 mV sine wave, the signal is slightly distorted, which corresponds to the frequency response illustrated in Fig. 4.3d.



(a) 1 mV_{pp} input sine wave sampled at 20 kHz **(b)** 180 mV_{pp} input sine wave sampled at 100 kHz

Figure 4.7: Reconstructed input vs original input for 2 kHz sine waves.

The implemented system is targeted to record during and after stimulation. Therefore, an artificial data-set has been generated which includes the direct stimulation artifact with peak amplitude of ∼100 mV, the residual artifact and the neural spike. Figure 4.8 illustrates the reconstructed input compared to the original input signal. The system adapts the gain during stimulation and is therefore able to record the stimulation artifact without saturating the front-end. After stimulation, the system automatically adapts the gain to the persisting residual artifact. After the integration time reaches the highest gain configuration, the system remains in this configuration such that the neural action potential can be recorded with the largest amplification. It must be noticed that the implemented high-pass pole attenuates the low-frequency part of the AP. The effect of this can be seen in Fig.4.8b after 2.4 ms.



(a) Artifact + spike **(b)** Zoomed on spike

Figure 4.8: Reconstructed input of a artificial stimulation and neural spike recording

4.3.1. Power consumption

The power consumption of the OTA can be calculated by multiplying the OTA supply voltage with its bias current:

$$P_{OTA} = V_{DD,2.5V} \cdot I_{bias,OTA} = 450\,nW$$

The power consumption of the LCD, which consists of two comparators is calculated as:

$$P_{LCD} = 2P_{comp} = 2V_{DD,1.1V} \cdot (2I_{bias,comp1} + I_{bias,comp2}) = 1.12\,\mu W$$

Here, P_{comp} is the power consumption of one comparator of the LCD, $I_{bias,comp1}$ is the bias current of two differential input pairs, $I_{bias,comp2}$ is the bias current of the second gain stage of the comparator.

For the unimplemented blocks, an estimation can be performed. The SAR ADC proposed in [37] achieves a Walden figure-of-merit (FoM) of $4.1\,fJ/c.step$. The Walden FoM is calculated as:

$$FOM = \frac{P_{ADC}}{2^{ENOB} \cdot f_s}$$

Here, P_{ADC} is the total power consumption of the ADC, ENOB is the equivalent number of bits and f_s is the sampling rate of the ADC. For this system, the ADC can be configured to operate at 20 kHz during spike mode and at 1 MHz when in stimulation mode. This results in a power consumption of $43\,nW$ during spike recording and $2.2\,\mu W$ when in stimulation mode.

As for digital blocks, which consists of the clock generator, digital averager (accumulator + logic shifter) and the divider, it can be assumed that their power consumptions are not dominant compared to the analog blocks.

5

Discussions and Conclusions

5.1. Future Work and recommendations

5.1.1. Power and area savings

The system should be implemented in transistor level to verify the power-saving and area-reducing claim in this work. The architecture avoids capacitevely-coupled amplifier and a programmable-gain amplifier as proposed in [22] to reduce the capacitor area budget. The digital averaging filter, in constrast to a sigma-delta modulator, only consists of an accumulator and a binary shifter. The area can therefore be significantly reduced by avoiding a moving average filter. The CDAC of the SAR ADC can be implemented with the unit-length capacitors approach proposed in [37]. By using an asynchronous ADC, power can be minimized during neural spike recording [38].

5.1.2. Tuning design parameters

Different design parameters used in this work can be changed depending on the target specifications of the system. The capacitance of the integration capacitor C_{INT} can be increased to obtain a lower gain at the output of the boxcar sampler at the cost of additional area. The same can be achieved by decreasing the shortest integration time, which in turn result in a smaller gain with the penalty of additional noise folding, to be compensated by oversampling. Assuming that the OTA maintains linearity, the input range of the system can be increased without

saturating the ADC, resulting in a higher DR.

5.2. Conclusions

The aim of this work was to propose a novel system architecture that can record during and after stimulation, without saturating the front-end in presence of the stimulation artifacts. The proposed system architecture automatically adapts the gain of the boxcar sampler by adapting the integration time according to the input amplitude and slew-rate by using continuous-time comparators that generate an out-of-range signal for the clock generator to stop the integration at the boxcar sampler. To avoid complex digital processing blocks, a LUT with fixed gain configurations is implemented and remains fixed during the interval of time at which the output of the system is updated. The ADC oversamples during lower gain configurations to minimize the noise penalty introduced by the boxcar sampler. The output of the ADC is then accumulated. The system outputs a 3-bit signal corresponding to the gain configuration and a 13-bit data correspnding to the output of the accumulator. The output of the system can be reconstructed by averaging the data and recomputing the gain.

The system recording performance is verified in presence of large amplitude input sine waves, large stimulation artifacts and neural spikes. By achieving a dynamic range of $69.5\,\mathrm{dB}$, the system is able to capture input amplitudes up to $180\,\mathrm{mV_{PP}}$ with an ENOB of 8.01 bits.

Bibliography

[1] M. J. Morrell, "Responsive cortical stimulation for the treatment of medically intractable partial epilepsy," *Neurology*, vol. 77, no. 13, pp. 1295–1304, 2011, ISSN: 0028-3878. DOI: 10.1212/WNL.0b013e3182302056.

[2] Stanford Medicine, *Stanford Artificial Retina Project*, URL: https://med.stanford.edu/artificial-retina/research.html, Last accessed on 08-11-2022, 2022.

[3] D. G. Muratore and E. J. Chichilnisky, "Artificial Retina: A Future Cellular-Resolution Brain-Machine Interface," in *NANO-CHIPS 2030: On-Chip AI for an Efficient Data-Driven World*. Springer International Publishing, 2020, pp. 443–465, ISBN: 978-3-030-18338-7. DOI: 10.1007/978-3-030-18338-7_24.

[4] J.-H. Jung, D. Aloni, Y. Yitzhaky, and E. Peli, "Active confocal imaging for visual prostheses," *Vision Research*, vol. 111, pp. 182–196, 2015, Sight restoration: prosthetics, optogenetics and gene therapy, ISSN: 0042-6989. DOI: https://doi.org/10.1016/j.visres.2014.10.023. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0042698914002569.

[5] R. Brash, " Artifact-Free Stimulation for Next-Generation Single-Cell Resolution Epiretinal Implants," M.S. thesis, Delft University of Technology, 2021.

[6] H. Jung, J. Kim, and Y. Nam, "Recovery of early neural spikes from stimulation electrodes using a dc-coupled low gain high resolution data acquisition system," *Journal of Neuroscience Methods*, vol. 304, pp. 118–125, 2018, ISSN: 0165-0270. DOI: https://doi.org/10.1016/j.jneumeth.2018.04.014. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0165027018301171.

[7] K. Joseph, S. Mottaghi, O. Christ, T. J. Feuerstein, and U. G. Hofmann, "When the ostrich-algorithm fails: Blanking method affects spike train statistics," *Frontiers in Neuroscience*, vol. 12, 2018, ISSN: 1662-453X. DOI: 10.3389/fnins.2018.00293. [On-

line]. Available: https://www.frontiersin.org/articles/10.3389/fnins.2018.00293.

[8] J. M. Weiss, S. N. Flesher, R. Franklin, J. L. Collinger, and R. A. Gaunt, "Artifact-free recordings in human bidirectional brain–computer interfaces," *Journal of Neural Engineering*, vol. 16, no. 1, p. 016 002, Nov. 2018. DOI: 10.1088/1741-2552/aae748. [Online]. Available: https://dx.doi.org/10.1088/1741-2552/aae748.

[9] R. Brash, W. Serdijn, and D. G. Muratore, "Fara: A fast artifact recovery algorithm with optimum stimulation waveform for single-cell resolution massively parallel neural interfaces," in *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2022, pp. 190–194. DOI: 10.1109/ISCAS48785.2022.9937814.

[10] A. Zhou, B. C. Johnson, and R. Muller, "Toward true closed-loop neuromodulation: Artifact-free recording during stimulation," *Current Opinion in Neurobiology*, vol. 50, pp. 119–127, 2018, Neurotechnologies, ISSN: 0959-4388. DOI: https://doi.org/10.1016/j.conb.2018.01.012. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S095943881730243X.

[11] M. Dongen and W. Serdijn, "Does a coupling capacitor enhance the charge balance during neural stimulation? an empirical study," *Medical & biological engineering & computing*, vol. 54, May 2015. DOI: 10.1007/s11517-015-1312-9.

[12] C. Hartmann, S. Došen, S. Amsuess, and D. Farina, "Closed-loop control of myoelectric prostheses with electrotactile feedback: Influence of stimulation artifact and blanking," *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, vol. 23, no. 5, pp. 807–816, 2015. DOI: 10.1109/TNSRE.2014.2357175.

[13] S. Culaclii, B. Kim, Y.-K. Lo, and W. Liu, "A hybrid hardware and software approach for cancelling stimulus artifacts during same-electrode neural stimulation and recording," in *2016 38th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, 2016, pp. 6190–6193. DOI: 10.1109/EMBC.2016.7592142.

[14] G. Buzsáki, C. Anastassiou, and C. Koch, "The origin of extracellular fields and currents—eeg, ecog, lfp and spikes," *Nature reviews. Neuroscience*, vol. 13, pp. 407–20, May 2012. DOI: 10.1038/nrn3241.

[15] N. Pérez-Prieto, M. Delgado-Restituto, and Á. Rodríguez-Vázquez, "Artifact-aware analogue/mixed-signal front-ends for neural recording applications," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019, pp. 1–5. DOI: 10.1109/ISCAS.2019.8702656.

[16] U. Hoffmann, W. Cho, A. Ramos-Murguialday, and T. Keller, "Detection and removal of stimulation artifacts in electroencephalogram recordings," in *2011 Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, 2011, pp. 7159–7162. DOI: 10.1109/IEMBS.2011.6091809.

[17] A. Zhou, S. R. Santacruz, B. C. Johnson, *et al.*, *Wand: A 128-channel, closed-loop, wireless artifact-free neuromodulation device*, 2018. arXiv: 1708.00556 [q-bio.NC].

[18] X. Qian, Y. Chen, Y. Feng, B. Ma, H. Hao, and L. Li, "A method for removal of deep brain stimulation artifact from local field potentials," *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, vol. 25, no. 12, pp. 2217–2226, 2017. DOI: 10.1109/TNSRE.2016.2613412.

[19] K. Zeng, D. Chen, G. Ouyang, L. Wang, X. Liu, and X. Li, "An eemd-ica approach to enhancing artifact rejection for noisy multivariate neural data," *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, vol. 24, pp. 630–638, Jun. 2016. DOI: 10.1109/TNSRE.2015.2496334.

[20] M. Zamani, Y. Rezaeiyan, H. A. Huynh, M. Ronchini, H. Farkhani, and F. Moradi, "A 2.3-μw capacitively coupled chopper-stabilized neural amplifier with input impedance of 6.7 gΩ," *IEEE Solid-State Circuits Letters*, vol. 4, pp. 133–136, 2021. DOI: 10.1109/LSSC.2021.3094237.

[21] A. Uran, Y. Leblebici, A. Emami, and V. Cevher, "An ac-coupled wideband neural recording front-end with sub-1 mm^2×fj/conv-step efficiency and 0.97 nef," *IEEE Solid-State Circuits Letters*, vol. 3, pp. 258–261, 2020. DOI: 10.1109/LSSC.2020.3013993.

[22] Y. Jung, S.-J. Kweon, H. Jeon, *et al.*, "A Wide-Dynamic-Range Neural-Recording IC With Automatic-Gain-Controlled AFE and CT Dynamic-Zoom ΔΣ ADC for Saturation-Free Closed-Loop Neural Interfaces," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 10, pp. 3071–3082, 2022. DOI: 10.1109/JSSC.2022.3188626.

[23] E. Greenwald, E. So, Q. Wang, *et al.*, "A bidirectional neural interface ic with chopper stabilized bioadc array and charge balanced stimulator," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 10, no. 5, pp. 990–1002, 2016. DOI: 10.1109/TBCAS.2016.2614845.

[24] M. R. Pazhouhandeh, H. Kassiri, A. Shoukry, I. Weisspapir, P. L. Carlen, and R. Genov, "Opamp-less sub-μw/channel Δ-modulated neural-adc with super-gΩ input impedance," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 5, pp. 1565–1575, 2021. DOI: 10.1109/JSSC.2020.3041289.

[25] C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs, "Sub- μ vrms-noise sub- μ w/channel adc-direct neural recording with 200-mv/ms transient recovery through predictive digital autoranging," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 11, pp. 3101–3110, 2018. DOI: 10.1109/JSSC.2018.2870555.

[26] M. R. Pazhouhandeh, A. Amirsoleimani, I. Weisspapir, P. Carlen, and R. Genov, "Adaptively clock-boosted auto-ranging neural-interface for emerging neuromodulation applications," *IEEE Transactions on Biomedical Circuits and Systems*, pp. 1–16, 2022. DOI: 10.1109/TBCAS.2022.3223988.

[27] K. A. Ng and Y. P. Xu, "A low-power, high cmrr neural amplifier system employing cmos inverter-based otas with cmfb through supply rails," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 724–737, 2016. DOI: 10.1109/JSSC.2015.2512935.

[28] R. Harrison and C. Charles, "A low-power low-noise cmos amplifier for neural recording applications," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, 2003. DOI: 10.1109/JSSC.2003.811979.

[29] M. H. Perrott, S. Pamarti, E. G. Hoffman, *et al.*, "A low area, switched-resistor based fractional-n synthesizer applied to a mems-based programmable oscillator," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2566–2581, 2010. DOI: 10.1109/JSSC.2010.2076570.

[30] H. Chandrakumar and D. Marković, "A high dynamic-range neural recording chopper amplifier for simultaneous neural recording and stimulation," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 3, pp. 645–656, 2017. DOI: 10.1109/JSSC.2016.2645611.

[31] Z. Tang, R. Zamparette, Y. Furuta, T. Nezuka, and K. A. A. Makinwa, "A Versatile ±25-A Shunt-Based Current Sensor With ±0.25% Gain Error From -40 °C to 85 °C," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 12, pp. 3716–3725, 2022. DOI: 10.1109/JSSC.2022.3204520.

[32] A. Mirzaei, S. Chehrazi, R. Bagheri, and A. A. Abidi, "Analysis of first-order anti-aliasing integration sampler," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 10, pp. 2994–3005, 2008. DOI: 10.1109/TCSI.2008.924127.

[33] H. Chandrakumar and D. Marković, "A 15.2-enob 5-khz bw 4.5- μ w chopped ct ΔΣ -adc for artifact-tolerant neural recording front ends," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 12, pp. 3470–3483, 2018. DOI: 10.1109/JSSC.2018.2876468.

[34] A. Nikas, S. Jambunathan, L. Klein, M. Voelker, and M. Ortmanns, "A continuous-time delta-sigma modulator using a modified instrumentation amplifier and current reuse dac for neural recording," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 10, pp. 2879–2891, 2019. DOI: 10.1109/JSSC.2019.2931811.

[35] D.-Y. Yoon, S. Pinto, S. Chung, P. Merolla, T.-W. Koh, and D. Seo, "A 1024-channel simultaneous recording neural soc with stimulation and real-time spike detection," in *2021 Symposium on VLSI Circuits*, 2021, pp. 1–2. DOI: 10.23919/VLSICircuits52068.2021.9492480.

[36] Y. Zhang, C. Yang, J. Sun, *et al.*, "A wireless headstage system based on neural-recording chip featuring 315 nw kickback-reduction sar adc," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 17, no. 1, pp. 105–115, 2023. DOI: 10.1109/TBCAS.2022.3224387.

[37] P. Harpe, "A compact 10-b sar adc with unit-length capacitors and a passive fir filter," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 3, pp. 636–645, 2019. DOI: 10.1109/JSSC.2018.2878830.

[38] P. J. A. Harpe, C. Zhou, Y. Bi, *et al.*, "A 26 μ w 8 bit 10 ms/s asynchronous sar adc for low energy radios," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, 2011. DOI: 10.1109/JSSC.2011.2143870.

[39] H. Kassiri, A. Bagheri, N. Soltani, *et al.*, "Battery-less tri-band-radio neuro-monitor and responsive neurostimulator for diagnostics and treatment of neurological disorders," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 5, pp. 1274–1289, 2016. DOI: 10.1109/JSSC.2016.2528999.

[40] A. Samiei and H. Hashemi, "A bidirectional neural interface soc with adaptive iir stimulation artifact cancelers," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 7, pp. 2142–2157, 2021. DOI: 10.1109/JSSC.2021.3056040.

[41] J. P. Uehlin, W. A. Smith, V. R. Pamula, *et al.*, "A single-chip bidirectional neural interface with high-voltage stimulation and adaptive artifact cancellation in standard cmos," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 7, pp. 1749–1761, 2020. DOI: 10.1109/JSSC.2020.2991524.

[42] R. Sharma and K. Sharma, "Design considerations for effective neural signal sensing and amplification: A review," vol. 5, Apr. 2019. DOI: 10.1088/2057-1976/ab1674.

[43] A. Williams, *Analog Filter and Circuit Design Handbook* (McGraw-Hill's AccessEngineering). McGraw-Hill Education, 2013, ISBN: 9780071816717. [Online]. Available: https://books.google.nl/books?id=WcV8AQAAQBAJ.

[44] D. A. Hall, K. A. Makinwa, and T. Jang, "Quantifying biomedical amplifier efficiency: The noise efficiency factor," *IEEE Solid-State Circuits Magazine*, vol. 15, no. 2, pp. 28–33, 2023. DOI: 10.1109/MSSC.2023.3256353.

[45] P. Jespers and B. Murmann, *Systematic Design of Analog CMOS Circuits*. Cambridge University Press, 2017, ISBN: 9781107192256. [Online]. Available: https://books.google.com/books?id=PhsODwAAQBAJ.

[46] M. Jang, W.-H. Yu, C. Lee, *et al.*, "A 1024-channel 268 nw/pixel 36x36 μm2/ch data-compressive neural recording ic for high-bandwidth brain-computer interfaces," in *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 2023, pp. 1–2. DOI: 10.23919/VLSITechnologyandCir57934.2023.10185288.