Strong doping reduction on wafer-scale CVD graphene devices via Al_2O_3 ALD encapsulation

Dockx, K.; Barnes, M. D.; Wehenkel, D. J.; van Rijn, R.; van der Zant, H. S.J.; Buscema, M.

DOI
10.1088/1361-6528/ad5dbb

Publication date
2024

Document Version
Final published version

Published in
Nanotechnology

PAPER

Strong doping reduction on wafer-scale CVD graphene devices via Al_2O_3 ALD encapsulation

To cite this article: K Dockx *et al* 2024 *Nanotechnology* **35** 395202

IOP Publishing Nanotechnology

Nanotechnology **35** (2024) 395202 (8pp) https://doi.org/10.1088/1361-6528/ad5dbb

Strong doping reduction on wafer-scale CVD graphene devices via Al_2O_3 ALD encapsulation

K Dockx[1,2,*], M D Barnes[1], D J Wehenkel[1], R van Rijn[1], H S J van der Zant[2,*] and M Buscema[1,*]

[1] Applied Nanolayers B.V., Feldmannweg 17, 2628 CT Delft, The Netherlands
[2] Kavli Institute of Nanoscience, Delft University of Technology, Lorentzweg 1, 2628 CJ Delft, The Netherlands

E-mail: k.dockx@appliednanolayers.com, h.s.j.vanderzant@tudelft.nl and m.buscema@appliednanolayers.com

Received 3 May 2024, revised 30 May 2024
Accepted for publication 2 July 2024
Published 11 July 2024

Abstract

We present the electrical characterization of wafer-scale graphene devices fabricated with an industrially-relevant, contact-first integration scheme combined with Al_2O_3 encapsulation via atomic layer deposition. All the devices show a statistically significant reduction in the Dirac point position, V_{cnp}, from around +47 V to between −5 and 5 V (on 285 nm SiO_2), while maintaining the mobility values. The data and methods presented are relevant for further integration of graphene devices, specifically sensors, at the back-end-of-line of a standard CMOS flow.

Supplementary material for this article is available online

Keywords: graphene, atomic layer deposition, electronics

1. Introduction

Two-dimensional materials are the subject of a large volume of research in recent years [1–3]. The interest in these materials stems from their peculiar properties, especially at the single-layer level [4, 5]. Since its discovery, [6] graphene has attracted the largest research effort to date and holds promise for sensor applications, where devices with micron-sized graphene channels are used to sense gas, [7, 8] (bio)molecules, [9] photons, [10–12] magnetic fields, [13–15] pressure [16], or sound [17, 18]. From an industrial perspective, graphene-based sensors are best integrated at the back-end-of-line of a CMOS fabrication flow: the underlying CMOS circuitry can be used to multiplex, amplify and digitize the signal coming from the graphene device [11, 19–21]. This entails that graphene needs to be transferred onto already-present metal electrodes. Bottom contacts are, at first glance, easier to integrate industrially and can provide benefits over top contacts [22]. Encapsulation and contact passivation are also common steps of the fabrication flow for sensors [20].

The effect of encapsulation of graphene via atomic layer deposition (ALD) has been the subject of many reports [23–27]. However, several of these reports focus on single or few devices fabricated via mechanical exfoliation or a handful of devices fabricated with chemical vapor deposition (CVD) grown graphene. Only a few reports consider wafer-scale fabrication of encapsulated graphene field-effect transistors (gFETs) [28–30]. Mzali *et al* [28] have fabricated and measured about 500 gFETs (contact-last integration scheme). They show the importance of protecting the graphene layer during the fabrication process with a thin aluminum layer and

* Authors to whom any correspondence should be addressed.

then fully passivating the devices with Al_2O_3 after contact deposition and lift-off. Smith *et al* [29, 30] report on the fabrication and electrical characterization of double-gated, bottom contacted, graphene devices on a wafer scale. Double-gated gFETS are not suited for sensing applications where the graphene channel needs to be exposed to the stimulus (e.g. photons, charged particles) or where the presence of a metallic electrodes above the channel may alter the signal (e.g. Hall sensors).

In this article, we present wafer-scale data on 2000 graphene devices fabricated with a contact-first approach and encapsulated with ALD. We show that ALD deposition strongly reduces the doping of the whole wafer-scale set of devices, while preserving mobility values. The ability to transfer on already-present metal contacts, the reduction in doping and the negligible change in mobility are desirable and necessary properties for integration of graphene at industrially relevant scales.

2. Materials and methods

Graphene is grown in a home-built CVD reactor and dry transferred onto the target wafer. Both the growth and transfer processes are proprietary and will not be disclosed. For the fabrication of the CVD graphene field-effect transistors (gFETs), we follow a contact-first integration scheme, briefly: the source and drain electrodes are pre-patterned on a SiO_2/Si wafer before the graphene is transferred onto them. Then, the graphene is patterned into channels and finally, the ALD layer is deposited through a thermal process. This flow is very similar to the one used by Mzali *et al* [28] and by Smith *et al* [29, 30], without the top gate. In detail, the fabrication begins by growing a layer of dry, thermal SiO_2 with 285 nm thickness in a CMOS-compatible furnace. An array of devices is patterned on the wafer using maskless optical lithography (μMLA 150, Heidelberg Instruments) and standard photolithography resists.

Once the resist is patterned, metals are evaporated in a high-vacuum evaporator (Temescal). Lift-off is carried out in standard warm solvents (e.g. acetone or NMP) with gentle sonication. After transfer, graphene device channels are defined by standard photolithography and O_2 reactive ion etching (RIE). At this stage, the wafer is characterized with optical microscopy and electrical measurements. Following this inspection, an Al_2O_3 ALD layer of approximately 40 nm is grown on the wafer with a standard TMA-based thermal process leveraging an evaporated metal seed less than 5 nm thick, as described in various references (see [23, 28–30]). The thickness is chosen to maximize the certainty of a closed layer (see AFM data in supplementary information figure S5) and optimize the usage of the ALD tool. After deposition, the ALD layer is chemically removed (through a lithographically defined mask) at the pads for electrical contact. After this step, the wafer is once more electrically characterized.

Optical inspection is carried out on an automated 200 mm-wafer-capable microscope (Zeiss); a full-wafer map can be seen in figure S1, alongside two die-level images, before and after ALD. Wafer-scale electrical measurements are performed in a dry nitrogen environment on a Cascade Microtech Summit 1200-Series Probe Station with an Agilent 4156C Precision Semiconductor Parameter Analyzer. The dry N_2 environment allows us to run measurements before and after encapsulation in the same conditions and to focus solely on the electrical effects of the ALD process, as we eliminate the potential effects of water vapor and oxygen. The electrical measurement circuit is drawn in the inset of figure 1(b).

3. Results and discussion

We have studied the effect of Al_2O_3 encapsulation on the electrical properties of CVD grown gFETs on a wafer scale. To collect statistically relevant data, we fabricate more than 2000 devices on a wafer, following the procedures highlighted in the Materials and Methods section. Figure 1(a) shows the array of devices after the fabrication flow has been completed. The 4-inch wafer is subdivided in 240 identical dies, each contains 10 gFETs of 5 different geometries. These dies are indexed in the x and y direction according to arrows in the inset of figure 1(a). The device cross section and measurement circuit schematic are sketched in the inset figure 1(b). The highly-doped Si wafer body serves as global back-gate (gate voltage, V_g), while the source and drain electrodes allow for current injection (I_s) and bias voltage measurement (V_{sd}). The array of devices covers a large part of the graphene wafer and thus allows for referencing of the location information with the measured graphene or device properties. The inset in figure 1(a) shows a zoomed in micrograph of a single die after encapsulation. The devices have a common-drain layout and the geometry of the graphene channels varies from top to bottom: the lengths and widths of graphene channels range from 50 to 300 μm and 30 to 150 μm respectively, see table S1 for the exact channel geometries. The common-drain geometry allows for flexibility during the subsequent packaging steps and the various channel geometries are intended to elucidate geometry-related effects in the electrical properties.

Two-terminal electrical measurements are performed before and after Al_2O_3 encapsulation. A gFET is characterized by measuring its output (V_{sd} *vs.* I_s at constant V_g) and transfer curve (V_{sd} *vs* V_g at constant I_s). A linear output characteristic indicates relatively clean contact of the Ti/Au leads to the graphene channel, with only small (or negligible) energy barriers, at least at room temperature. From the transfer curve, usually plotted as $R_{sd} = \frac{V_{sd}}{I_{sd}}$ for varying V_g, we extract the residual doping and the field effect mobility of the device. We use a simple parallel-plate capacitor model and define gate capacitance per unit area as $C_g = \frac{\epsilon_0 \epsilon_r}{t_{ox}}$ where ε_0 is the vacuum permittivity and ϵ_r is the relative permittivity of the gate material (SiO_2) and t_{ox} is the thickness of the SiO_2 gate oxide. The residual doping is expressed using one of two parameters: (i) V_{cnp}, the gate voltage at which the charge neutrality point (cnp) is located or (ii) n_0, the carrier concentration at zero gate voltage in cm^{-2}, assuming $n_0 = 0\ cm^{-2}$ at the V_{cnp}. The

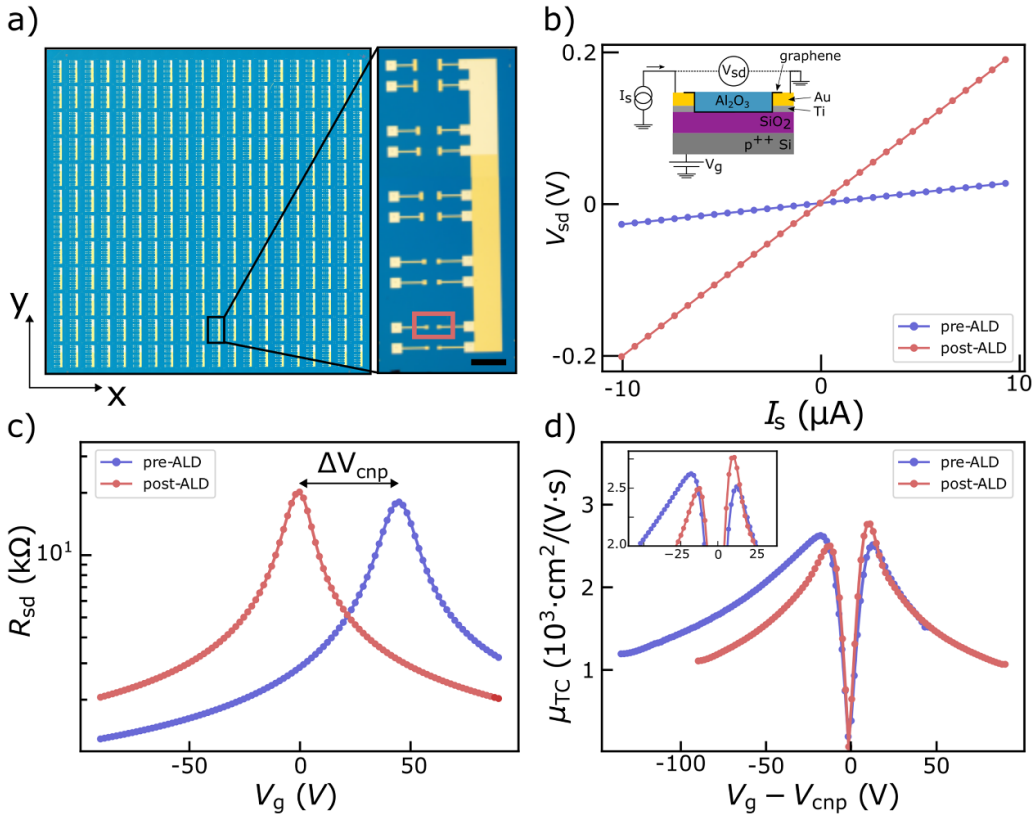

Figure 1. (a) Image of the device array after ALD encapsulation with Al_2O_3, obtained by stitching several images taken at 2.5x magnification. The *x* and *y* arrows indicate the frame of reference for device indexing. Inset: Zoom in on a die-level micrographs after Al_2O_3 ALD. The die design, entailing both a common-drain and varying channel dimensions, is clearly visible. The difference in the yellow shade is due the ALD encapsulation layer being removed for electrical contact. The red box highlights the device whose electrical behavior is shown in panels B, C and D. Scalebar is 500 μm. (b, c and (d) Electrical measurements of the highlighted device before (blue traces) and after Al_2O_3 ALD encapsulation (red traces).(b) Two-terminal output characteristic (V_{sd} *vs.* I_s); both traces measured at $V_g = 0$ V by sweeping I_s while measuring V_{sd}. Inset: Schematic of gFET cross-section and electrical circuit used for measurements. A contact-first integration-scheme is followed: the contacts are patterned first, then graphene is transferred (dry process) and lastly, the device channel is defined. A constant current, I_s, is applied to the device while the source-drain voltage, V_{sd}, is monitored as a function of gate voltage, V_g. (c) Two-terminal resistance versus applied gate voltage (R_{sd} *vs.* V_g measured at $I_s = 10$ μA). ΔV_{cnp} is the difference in the gate voltage at the maximum R_{sd} (i.e. V_{cnp}) before and after the ALD process. Data in log scale. (d) Transconductance mobility versus gate voltage shifted by ΔV_{cnp}. Inset: zoom-in near the DTM mobility peaks.

electron and hole field-effect mobilities are extracted from the transconductance (direct transconductance method—DTM), g_m [31]:

$$\mu_{TC} = g_m \frac{L}{WV_{sd}C_g} = \frac{\partial I_{sd}}{\partial V_g}\frac{L}{WV_{sd}C_g}, \quad (1)$$

where L and W are the length and width of the graphene strip. The transconductance mobility equals zero at the Dirac point; this is because $\frac{\partial I_{sd}}{\partial V_g} = 0$. As the doping increases (i.e. the gate voltage moves away from V_{cnp} with $|V_g - V_{cnp}| > 0$), the mobility increases and reaches a maximum on either side of the charge neutrality point before decreasing again at progressively higher doping. The local maxima (briefly called 'DTM peaks') coincide with the inflection points of the transfer characteristic (where $\frac{\partial^2 I_{sd}}{\partial V_g{}^2} = 0$). In the following, we quote the mobilities in the electron (μ_e^{DTM}) and hole (μ_h^{DTM}) regime calculated at the DTM peaks.

Figures 1(b)–(d) show data from the highlighted gFET before and after Al_2O_3 encapsulation. Figure 1(b) displays the corresponding output characteristics. Both curves in this figure show a linear behavior, indicating that the intrinsic nature of the graphene to metal contacts is not affected by the encapsulation procedure, at least within the bias window used in this study. The ALD encapsulation clearly increases the two-terminal resistance of the device at zero gate bias (see the transfer characteristics in figure 1(c). This jump in resistance at zero gate bias is due to a large shift after encapsulation in V_{cnp} of about -46 V. Before encapsulation, the gFET had a residual hole doping of $n_0 = +3.3 \times 10^{12}$ cm^{-2} which reduced by more than an order of magnitude to a residual electron doping of $n_0 = -1.5 \times 10^{11}$ cm^{-2} after encapsulation. The large hole doping after device fabrication is a well known issue in graphene device integration and it is likely due photoresist residues [28, 32]. The resistance at $V_g = V_{cnp}$ also slightly increases after encapsulation. This small increase is

indicative of negligible damage to the graphene lattice after the ALD process.

Looking at the high doping regime, one can note that the resistance in the hole regime increases after encapsulation whereas it reduces in the electron regime. We also measure the hysteresis (i.e. difference in V_{cnp} for upward and downward gate sweep) of the transfer characteristics (see figure S3a in the supplementary information). The hysteresis values are low both before and after the ALD process, indicating a negligible amount of mobile charges (possibly induced by adsorbates) in both the thermally grown SiO_2 and the deposited ALD layer in close proximity to the graphene layer.

Figure 1(d) shows the transconductance mobility before and after ALD. Note, that a simple parallel plate capacitor model has been used to calculate the gate capacitance both for the pre- and post-encapsulation data. The inset highlights the data around the DTM peaks for both the hole and electron regime and clearly reveals how close the values are before and after ALD encapsulation (less than 15% change), corroborating the idea that the encapsulation process induces limited damage in the graphene lattice. Moreover, it is possible to see that before encapsulation the peak DTM mobility for holes is higher compared to the one for electrons and the reverse is true after encapsulation.

Following the DTM mobility traces towards higher doping values shows that the ALD encapsulation reduces the hole mobility, while not affecting the electron mobility. More generally, the pre-ALD data in figure 1 depicts the expected asymmetry between the electron (higher R_{sd}) and hole regime (lower R_{sd}), consistent with literature findings [33–36]. However, the after-ALD data presented in figures 1(c) and (d) (and later in figure 4) shows the reverse effect: higher conductivity and mobility in the electron regime.

The measured changes in V_{cnp}, resistance and mobility between holes and electrons doping regimes can all be related to the interaction between the dielectric environment and the contact regions. Considering the dielectric environment, a possible cause is the specific alignment of the defect band in the Al_2O_3 layer with respect to the graphene Fermi level [37]. One possible cause is surface reactions between the ALD oxidant (e.g. H_2O) and the graphene surface (or the residues on its surface) [32]. Another possible cause can be related to the simple desorption of contaminants from the graphene surface at the ALD process temperature. A more specific, surface-sensitive, investigation will be required to clearly distinguish between these possible mechanisms, effecting the dielectric environment of the graphene. Looking at the contact regions, two main effects usually occur: band bending and Fermi-level pinning. Band bending is the result of charge transfer at the graphene/metal interface driven by the mismatch between metal work function and graphene Fermi energy. Fermi-level pinning describes the insensitivity of the graphene Fermi-level to the gate electric field (near the contact region) [33–36, 38].

The two effects described above are known to induce p-n junctions near the contact, leading to an asymmetry in the measured 2-terminal resistance between the hole and electron doping regime. The measured output characteristics are still

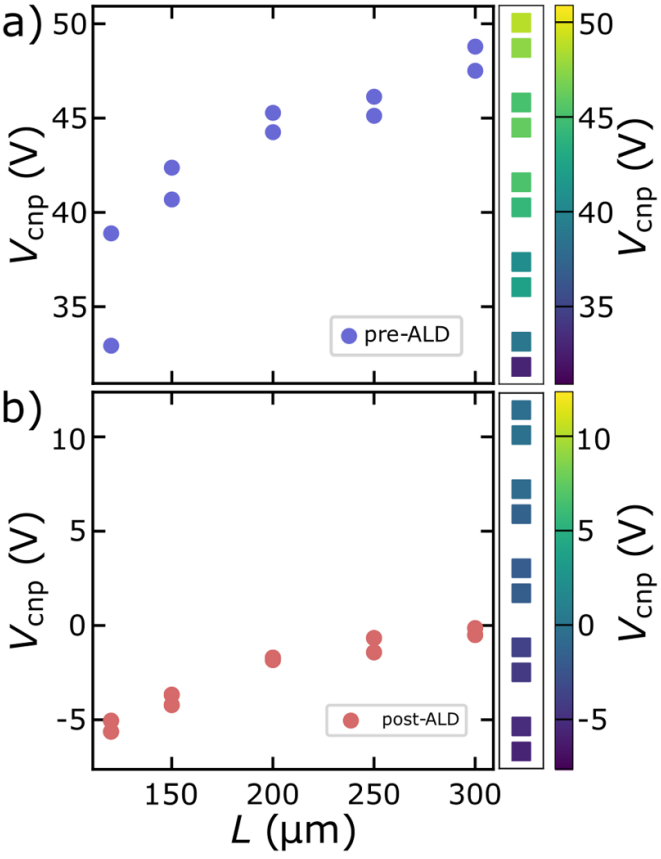

Figure 2. Die-level characterization. (a) V_{cnp} against device length before ALD, (b) V_{cnp} against device length after ALD encapsulation. Insets: false color map of the V_{cnp} for a die before ALD (inset of panel (a) and after ALD (inset of panel (b). The squares represent the five pairs of devices a depicted in the inset of figure 1(a).

linear and the mobility values shift only slightly, therefore the p-n junctions at the contact regions represent a small energy barrier. The data shown in figures 1(c) and (d) indicates that the ALD encapsulation strongly reduces doping. In turn, the doping reduction alters the band alignment, leading to a partial reversal of the direction of the p-n junction at the contacts (see figure S2) and, therefore, higher mobility in the electron regime. Further studies to separate the relative effect of the ALD encapsulation on the intrinsic graphene channel conductivity and on the contact region need to rely on multi-terminal measurements.

Taking advantage of our reliable wafer-scale transfer, we have fabricated 240 dies with several device geometries, enabling us to investigate the relationship between device geometry and the ALD process. From the single devices shown in figure 1, we move on to characterize the single die, looking at the V_{cnp} in particular. Figure 2 displays the V_{cnp} values against the length of the graphene channels in a single die: figure 2(a) shows V_{cnp} before ALD encapsulation and figure 2(b) after the ALD process. Both insets show die-level false color maps of V_{cnp} extracted from each graphene device composing the die. After ALD encapsulation, all the devices in the single die, irrespective of the channel geometry, show a strong reduction in

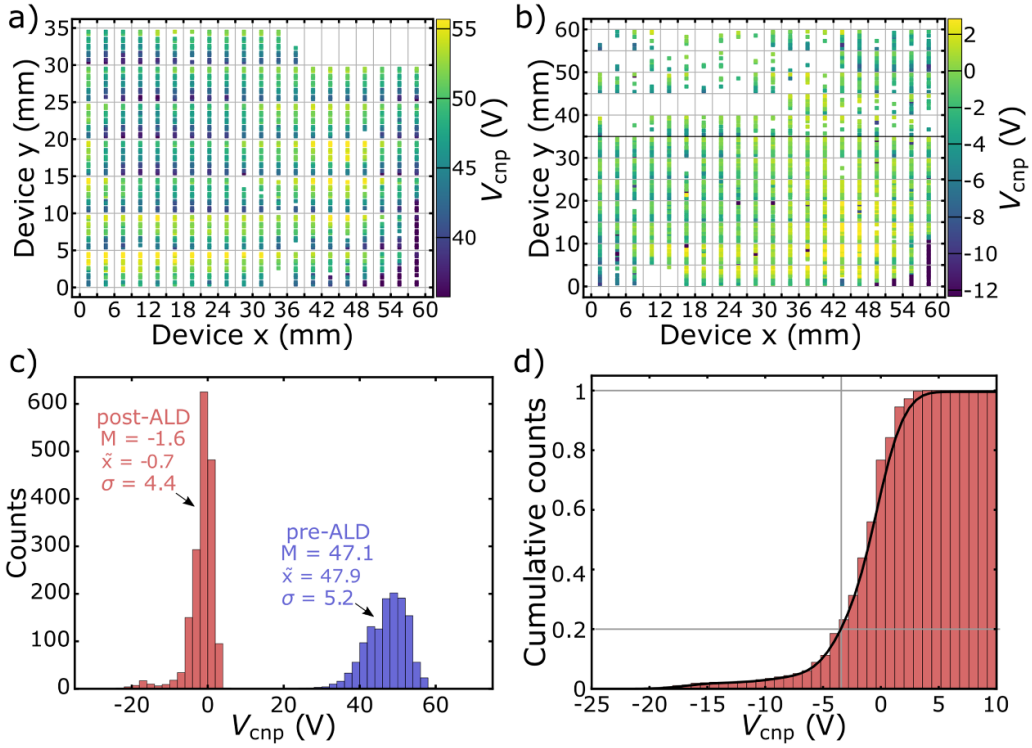

Figure 3. Wafer-scale electrical measurement results of the doping of the gFET devices: (a), (b) false-color images where the x- and y-axis correspond to the device position on the wafer and the color indicates the measured V_{cnp} value before ALD (a) and after ALD (b). The black line at $y = 35$ mm in panel (b) indicates the limit of the devices measured before ALD. The colorscale in panels A and B is cropped between 2.5% and 97.5% of the full distribution to avoid saturation and clearly display the pattern on the wafer.(c) Histogram showing the V_{cnp} values before ALD (blue) and after ALD (red) with the corresponding average (M), median ($\tilde{\chi}$) and standard deviation (σ) values. (d) Cumulative histogram of V_{cnp} values after Al_2O_3 ALD.

V_{cnp}, confirming the behavior of the single device depicted in figure 1. Looking in more detail, there is a trend of increasing V_{cnp} for increasing device length which is stronger before ALD encapsulation. As the geometry of the devices varies from the bottom to the top of the die, as indicated in table S1, the increase in V_{cnp} is likely linked to the geometry of the graphene channel. The variation of V_{cnp} with graphene channel length has been reported before in literature [39, 40] and it has been ascribed to effects at the contacts regions, either doping or changes in the contact transfer length, consistent with the explanation of the behavior of the single device. Thus, for all the devices in a single die, the ALD process strongly reduces V_{cnp} and weakens its dependency with device length, homogenizing device performance; both are beneficial characteristics from an application perspective.

The wafer scale transfer, fabrication process and measurements allow us to confidently prove that the effects shown in figures 1 and 2 for a single device and die are representative for the full wafer-scale dataset. Figure 3 portrays the behavior of the charge neutrality point of all measured devices on one wafer. Figures 3(a) (before encapsulation) and (b) (after encapsulation) show false color maps of the wafer-level collection of the V_{cnp} on each die arranged with respect to the x and y indices shown in figure 1(a).

The absence of a data-point on the color maps indicates that the device is broken (i.e. the measured $R_{sd} > 100$ kΩ). Due to limited measurement time, data points above $y = 35$ mm in figure 3(a) are absent and these are not taken into account in the analysis. When comparing the data from the same devices before and after encapsulation, we find that the device yield decreased only slightly: from 97.7% prior to encapsulation to 93.0% after encapsulation. The small decrease in yield of working devices corroborates that ALD encapsulation introduces a negligible amount of defects in the graphene channel.

The overall wafer-scale pattern of V_{cnp} appears consistent before and after the ALD process: the bottom right region ($x > 54$, $y < 10$) shows the overall lowest V_{cnp}, the center region ($36 < x < 54$, $10 < y < 35$) shows the highest V_{cnp} whereas the top-left region ($3 < x < 20$, $y > 15$) shows the lowest doping. The measured wafer-scale pattern is likely due to slight in-homogeneity in the various processes composing the whole device fabrication chain: from slight differences in the graphene grain sizes (growth), to slight differences in strain introduced by the transfer process, to the variability in the density of residues on the graphene channel due to the fabrication steps. The interplay between these processes is a fascinating research topic, outside of the scope of this publication. The overall significance of the pattern can be better visualized by looking at the numerical spread in the distributions of V_{cnp}, presented in the following paragraphs.

We now turn to the statistical distribution and properties of V_{cnp}. Figure 3(c) plots the histograms of the doping distribution before (blue) and after (red) encapsulation. These distributions are calculated from the full dataset, without selecting

on geometry or device location. Before encapsulation, the V_{cnp} distribution is centered around $V_{cnp} = +47.1 \pm 5.2$ V whereas after encapsulation it shifts to $V_{cnp} = -1.6 \pm 4.4$ V. Note, that the value of the standard deviation after encapsulation is effected by the very small tail of points with $V_{cnp} < -10$ V. Thus, after encapsulation, the V_{cnp} distribution shifts to considerably lower gate voltages, close to zero, and sharpens around the median value.

To verify the statistical significance of the shift, we use the 3-sigma approach to calculate the left (right) edge of the distribution before (after) encapsulation. The left edge of the V_{cnp} distribution before encapsulation is 31.5 V and the right edge after encapsulation is 11.6 V. The calculated edges are well separated, confirming that the distributions are statistically different: all the measured devices show a statistically significant reduction in V_{cnp} after encapsulation.

In figure 3(d), a cumulative histogram of the V_{cnp} distribution after Al_2O_3 encapsulation is shown. As indicated by the grey lines at 0.2 and 1 cumulative counts, the majority of V_{cnp} values is situated around zero. Specifically, the Dirac point of 90.1% of devices is situated between -5 and $+5$ V after encapsulation, further highlighting the narrow distribution after the ALD process. Before the ALD process, less than 70% of the devices has their V_{cnp} in a narrow 10 V range (see figure S4). The ALD process clearly shifts and narrows the entire V_{cnp} distribution around 0 V which is beneficial from an application perspective, where the supply voltages are likely limited to ± 3.3 V or ± 5 V.

With respect to the hysteresis in the V_{cnp} values, by performing a similar analysis (see figure S3(b)), we see that ALD process further reduces the already tiny hysteresis: before ALD, the hysteresis is -1.81 ± 0.48 V whereas, after ALD, it is -0.63 ± 0.39 V. The hysteresis is therefore about three times less pronounced after ALD process, at least in absolute V_g values.

The wafer-scale of the growth, transfer, fabrication and measurement processes have allowed us to confidently determine both the statistically relevant shift to lower V_{cnp} and the reduction in variance in device performance, irrespective of the geometry of the graphene channel. The demonstrated improved performance and higher consistency of the electrical characteristics after the ALD process are important for the industrial application of graphene devices. They ensure consistent electrical behavior of the fabricated devices and the possibility to explore both the hole and electron regime and, therefore, finely adjust the operation point of the sensor, essential in the case of e.g. Hall sensors [13].

After analyzing the behavior of V_{cnp}, we now shift our attention to the extracted DTM-mobilities. Figure 4 shows the DTM peak mobilities before (blue) and after encapsulation (red) in both the hole (figure 4(a)) and electron (figure 4(b)) regimes. The histograms highlight the opposite effect of the ALD encapsulation on the mobility values: in the hole (electron) regime, the encapsulation process results in a small reduction (increase) of the average and median mobility. These observations are also captured by the behavior of the single gFET device already depicted in figure 1.

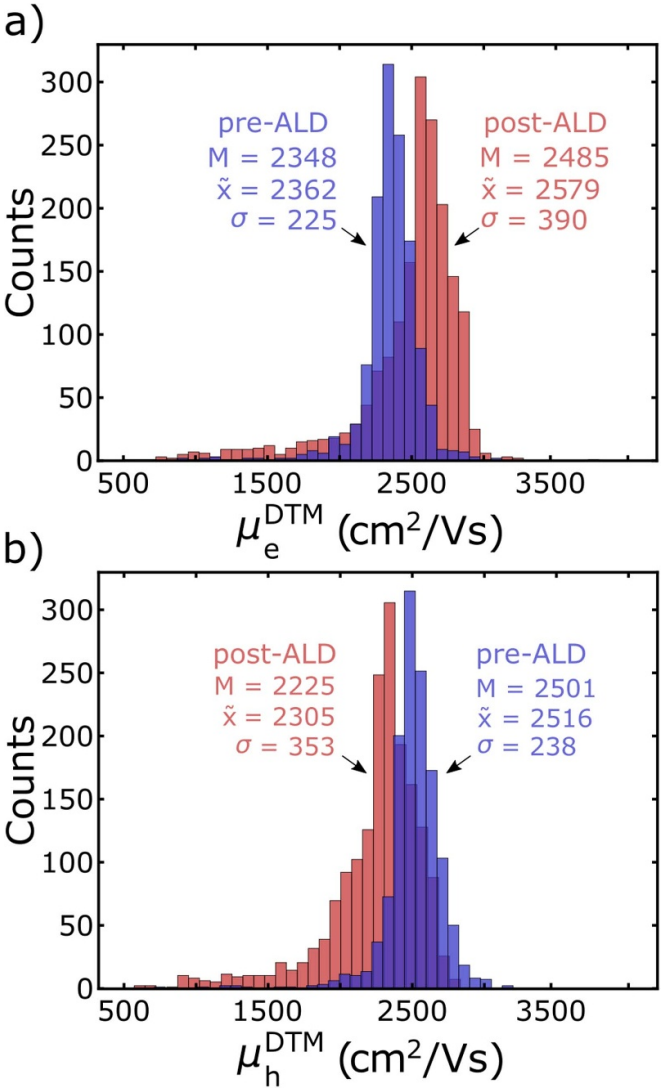

Figure 4. (a) Histograms of the peak value of the hole DTM-mobility before (blue) and after (red) Al_2O_3 ALD encapsulation. (b) Histograms of the peak value of the electron DTM-mobility before (blue) and after (red) ALD. For each distribution, the corresponding average (M), median ($\tilde{\chi}$) and standard deviation (σ) values are indicated.

For the standard deviation the effect is also opposite: post-encapsulation, the hole (electron) regime shows an increased (reduced) standard deviation. Also noteworthy, the ALD-encapsulation makes the distributions for both regimes skew to lower mobility values; in other words, the low-value tails of both distributions increase after the ALD process. This could be an artifact due to the fact that more devices have been measured post-ALD, increasing the chance of measuring slightly lower-performing devices. Another effect to consider is the screening of charged impurities scattering that can be afforded by the ALD layer.

Importantly, there is considerable overlap between the pre- and post-ALD mobility values for both regimes: the mean and median peak mobility values in both regimes change less than 15% after Al_2O_3 encapsulation and are well within one

standard deviation from each other. The large overlap indicates that the ALD has limited effect on the mobility values, in either regimes, and this negligible change in mobility indicates very minimal damage to the graphene layer during the ALD process.

4. Conclusions

In summary, we report on the study of the effect of ALD encapsulation on wafer-scale two-terminal graphene FETs. The devices have been fabricated with a contact-first integration scheme which is similar to the integration of graphene on the back-end-of-line of the CMOS fabrication flow. Wafer-scale electrical characterization shows that the ALD process strongly reduces the V_{cnp} of the fabricated devices and narrows its distribution, allowing for exploring both the electron and hole regime by applying gate voltages of just 5 V or less. The DTM mobilities after ALD are within 15% of the original values before ALD, indicating that minimum (or possibly no) damage has been induced on the graphene channel during the ALD process. Mobilities in the electron and hole regimes change in opposite direction after the ALD encapsulation, possibly hinting to the ALD process affecting the dielectric environment nearest to the contact regions. The observed low graphene doping on a wafer scale removes the need for local gates on thin-high-k dielectrics. This enables access to both the electron and hole regime in devices where it is not possible to integrate local gates; the results thus clearly showcase the benefit of ALD encapsulation for future device integration in e.g. commercial sensors based on a FET geometry.

Data availability statement

The data contains partially commercially sensitive information. It can be shared on request. The data that support the findings of this study are available upon reasonable request from the authors.

Acknowledgment

We thank Prof. S Vollebregt and F Simjanoski for granting access and support to the automated electrical measurement setup. K Dockx, M D Barnes, D J Wehenkel, R van Rijn and M Buscema acknowledge funding from the European Union (Horizon 2020, research and innovation programme under grant agreement SPRING No. 881273).

ORCID iD

M Buscema https://orcid.org/0009-0008-1132-0815

References

[1] Zeng M, Xiao Y, Liu J, Yang K and Fu L 2018 Exploring two-dimensional materials toward the next-generation circuits: from monomer design to assembly control *Chem. Rev.* **118** 6236–96

[2] Novoselov K S, Mishchenko A, Carvalho A and Neto A H C 2016 2D Materials and van der Waals heterostructures *Science* **353** aac9439

[3] Sun B *et al* 2021 Synthesis of wafer-scale graphene with chemical vapor deposition for electronic device applications *Adv. Mater. Technol.* **6** 2000744

[4] Zhan D, Yan J, Lai L, Ni Z, Liu L and Shen Z 2012 Engineering the electronic structure of graphene *Adv. Mater.* **24** 4055–69

[5] Scarpa F, Adhikari S and Phani A S 2009 Effective elastic mechanical properties of single layer graphene sheets *Nanotechnology* **20** 065709

[6] Novoselov K S, Geim A K, Morozov S V, Jiang D, Zhang Y, Dubonos S V, Grigorieva I V and Firsov A 2004 A electric field effect in atomically thin carbon films *Science* **306** 666–9

[7] Wang T, Huang D, Yang Z, Xu S, He G, Li X, Hu N, Yin G, He D and Zhang L 2015 A review on graphene-based gas/vapor sensors with unique properties and potential applications *Nano-Micro Lett.* **8** 95–119

[8] Schedin F, Geim A K, Morozov S V, Hill E W, Blake P, Katsnelson M I and Novoselov K S 2007 Detection of individual gas molecules adsorbed on graphene *Nat. Mater.* **6** 652–5

[9] Szunerits S, Rodrigues T, Bagale R, Happy H, Boukherroub R and Knoll W 2023 Graphene-based field-effect transistors for biosensing: where is the field heading to? *Anal. Bioanal. Chem.* **416** 2137–50

[10] Xia F, Mueller T, Golizadeh-Mojarad R, Freitag M, ming Lin Y, Tsang J, Perebeinos V and Avouris P 2009 Photocurrent imaging and efficient photon detection in a graphene transistor *Nano Lett.* **9** 1039–44

[11] Goossens S *et al* 2017 Broadband image sensor array based on graphene-CMOS integration *Nat. Photon.* **11** 366–71

[12] Vicarelli L, Vitiello M S, Coquillat D, Lombardo A, Ferrari A C, Knap W, Polini M, Pellegrini V and Tredicucci A 2012 Graphene field-effect transistors as room-temperature terahertz detectors *Nat. Mater.* **11** 865–71

[13] Schaefer B T, Wang L, Jarjour A, Watanabe K, Taniguchi T, McEuen P L and Nowack K C 2020 Magnetic field detection limits for ultraclean graphene Hall sensors *Nat. Commun.* **11** 4163

[14] Dankert A, Karpiak B and Dash S P 2017 Hall sensors batch-fabricated on all-CVD h-BN/graphene/h-BN heterostructures *Sci. Rep.* **7** 15231

[15] Lyon T J, Sichau J, Dorn A, Zurutuza A, Pesquera A, Centeno A and Blick R H 2017 Upscaling high-quality CVD graphene devices to 100 micron-scale and beyond *Appl. Phys. Lett.* **110** 113502

[16] Šiškins M *et al* Sensitive capacitive pressure sensors based on graphene membrane arrays 2020 *Microsyst. Nanoeng.* **6** 102

[17] Pezone R, Baglioni G, Sarro P M, Steeneken P G and Vollebregt S 2022 Sensitive transfer-free wafer-scale graphene microphones *ACS Appl. Mater. Interfaces* **14** 21705–12

[18] Baglioni G, Pezone R, Vollebregt S, Cvetanović Zobenica K, Spasenović M, Todorović D, Liu H, Verbiest G J, van der Zant H S J and Steeneken P G 2023 Ultra-sensitive graphene membranes for microphone applications *Nanoscale* **15** 6343–52

[19] Soikkeli M *et al* 2023 Wafer-scale graphene field-effect transistor biosensor arrays with monolithic CMOS readout *ACS Appl. Electr. Mater.* **5** 4925–32

[20] Shah N, Iyer V, Zhang Z, Gao Z, Park J, Yelleswarapu V, Aflatouni F, Charlie Johnson A T and Issadore D 2023 Highly stable integration of graphene Hall sensors on a microfluidic platform for magnetic sensing in whole blood *Microsyst. Nanoeng.* **9** 71

[21] Mortazavi Zanjani S M, Holt M, Sadeghi M M, Rahimi S and Akinwande D 2017 3D integrated monolayer graphene-Si CMOS RF gas sensor platform *npj 2D Mater. Appl.* **1** 36
[22] Cha J, Son J and Hong J 2022 A bottom-electrode contact: the most suitable structure for graphene electronics *Adv. Mater. Interfaces* **9** 2102207
[23] Vervuurt R 2017 Atomic layer deposition on graphene : towards graphene device integration *PhD Thesis* Applied Physics Proefschrift
[24] Zhang Y, Qiu Z, Cheng X, Xie H, Wang H and Xie X 2014 Yu Y and Liu R Direct growth of high-quality Al_2O_3 dielectric on graphene layers by low-temperature H_2O-based ALD *J. Phys. D: Appl. Phys.* **47** 055106
[25] Sagade A A, Neumaier D, Schall D, Otto M, Pesquera A, Centeno A, Elorza A Z and Kurz H 2015 Highly air stable passivation of graphene based field effect devices *Nanoscale* **7** 3558–64
[26] Alexander-Webber J A *et al* 2016 Encapsulation of graphene transistors and vertical device integration by interface engineering with atomic layer deposited oxide *2D Mater.* **4** 011008
[27] Canto B, Otto M, Powell M J, Babenko V, O'Mahony A, Knoops H C M, Sundaram R S, Hofmann S, Lemme M C and Neumaier D 2021 Plasma-enhanced atomic layer deposition of Al_2O_3 on graphene using monolayer hBN as interfacial layer *Adv. Mater. Technol.* **6** 2100489
[28] Mzali S *et al* 2016 Stabilizing a graphene platform toward discrete components *Appl. Phys. Lett.* **109** 253110
[29] Smith A D, Wagner S, Kataria S, Malm B G, Lemme M C and Östling M 2017 Wafer-scale statistical analysis of graphene FETs-part I: wafer-scale fabrication and yield analysis *IEEE Trans. Electron Devices* **64** 3919–26
[30] Smith A D, Wagner S, Kataria S, Malm B G, Lemme M C and Östling M 2017 Wafer-scale statistical analysis of graphene field-effect transistors-part II: analysis of device properties *IEEE Trans. Electron Devices* **64** 3927–33
[31] Zhong H, Zhang Z, Xu H, Qiu C and Peng L-M 2015 Comparison of mobility extraction methods based on field-effect measurements for graphene *AIP Adv.* **5** 057136
[32] Zheng L, Cheng X, Cao D, Wang Z, Xia C, Yu Y and Shen D 2014 Property transformation of graphene with Al_2O_3 films deposited directly by atomic layer deposition *Appl. Phys. Lett.* **104** 023112
[33] Nouchi R and Tanigaki K 2010 Charge-density depinning at metal contacts of graphene field-effect transistors *Appl. Phys. Lett.* **96** 253503
[34] Nagashio K and Toriumi A 2011 Density-of-states limited contact resistance in graphene field-effect transistors *Japan. J. Appl. Phys.* **50** 070108
[35] Huard B, Stander N, Sulpizio J A and Goldhaber-Gordon D 2008 Evidence of the role of contacts on the observed electron-hole asymmetry in graphene *Phys. Rev.* B **78** 121402
[36] Lee E J H, Balasubramanian K, Weitz R T, Burghard M and Kern K 2008 Contact and edge effects in graphene devices *Nat. Nanotechnol.* **3** 486
[37] Knobloch T, Uzlu B, Illarionov Y Y, Wang Z, Otto M, Filipovic L, Waltl M, Neumaier D, Lemme M C and Grasser T 2022 Improving stability in two-dimensional transistors with amorphous gate oxides by Fermi-level tuning *Nat. Electr.* **5** 356–66
[38] Chaves F A, Jiménez D, Santos J E, Bøggild P and Caridad J M 2019 Electrostatics of metal-graphene interfaces: sharp p-n junctions for electron-optical applications *Nanoscale* **11** 10273–81
[39] Ifuku R, Nagashio K, Nishimura T and Toriumi A 2013 The density of states of graphene underneath a metal electrode and its correlation with the contact resistivity *Appl. Phys. Lett.* **103** 033514
[40] Thissen N F W, Vervuurt R H J, Mackus A J M, Mulders J J L, Weber J W, Kessels W M M and Bol A 2017 A Graphene devices with bottom-up contacts by area-selective atomic layer deposition *2D Mater.* **4** 025046