A 6.78 MHz Dual-output Reconfigurable Rectifier with Hysteretic Output Regulation for Wireless Power Transfer Systems

Lu, Tianqi; Du, Sijun

DOI
10.1109/ICECS202256217.2022.9971112

Publication date
2022

Document Version
Final published version

Published in
Proceedings of the 2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS)

A 6.78 MHz Dual-output Reconfigurable Rectifier with Hysteretic Output Regulation for Wireless Power Transfer Systems

Tianqi Lu, Sijun Du
Department of Microelectronics, Delft University of Technology, Delft, the Netherlands
Email: t.lu-4@tudelft.nl; sijun.du@tudelft.nl

2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS) | 978-1-6654-8823-5/22/$31.00 ©2022 IEEE | DOI: 10.1109/ICECS202256217.2022.9971112

***Abstract*—A 6.78 MHz dual-output reconfigurable rectifier for wireless power transfer is presented. The proposed rectifier integrates AC-DC rectification and DC-DC regulation into a single-stage topology, alleviating received power loss and reducing system volume cost. By adding a switch matrix after rectifying bridge, a dual output can be realized and regulated by a hysteretic control unit. The proposed rectifier can work in six operation modes by reconfiguring, and each output can be regulated in three modes. As a result, fine output regulation and large output-driving capability can be achieved. Designed in a 180-nm BCD process using standard 5-V devices, the dual-output rectifier provides two output voltages at 3 V and 5 V, and delivers a maximum power of 1.6 W. The peak post-layout simulated power conversion efficiency reaches 80.1% when both load currents are 0.2 A.**

***Index Terms*—wireless power transfer, 6.78 MHz, dual-output rectifier, reconfigurable rectifier, regulating rectifier, single-stage receiver, hysteretic control, biomedical implants**

I. Introduction

Recently, wireless power transfer (WPT) technology is widely used for portable/wearable electronics, like wireless phone chargers, and biomedical implantable devices such as pacemakers, retinal prostheses and neural recording systems. Typically, a WPT system contains three parts: a power transmitter, a wireless link (L_1, L_2) and a power receiver, as shown in Fig. 1. Conventionally, a wireless power receiver is composed by a rectifier for AC-DC rectification and a post DC-DC converter for DC-DC regulation. However, a two-stage topology degrades the power conversion efficiency (PCE) due to the multiplicative power loss. On the other hand, two or more power supplies are generally required from a WPT system, in highly-functional electronics. For example, a portable solid-state driver needs a high voltage (3.3 V) for the NAND array power supply and a low voltage (1.8 V) for the core logic circuits [1]; a retinal prosthesis requires a high voltage (>5 V) for the neurostimulator and a low voltage (1.8 V) for signal-processing circuits [2]. Conventionally, a power receiver with two output voltages is implemented either by using two rectifiers cascaded by two DC-DC converters or using one rectifier followed by two DC-DC converters, as shown in Fig. 1 (a) and (b). Both ways consume a lot of power and chip area. Therefore, single-stage dual-output rectifiers have been developed to improve system efficiency and reduce system volume [1, 3-5].

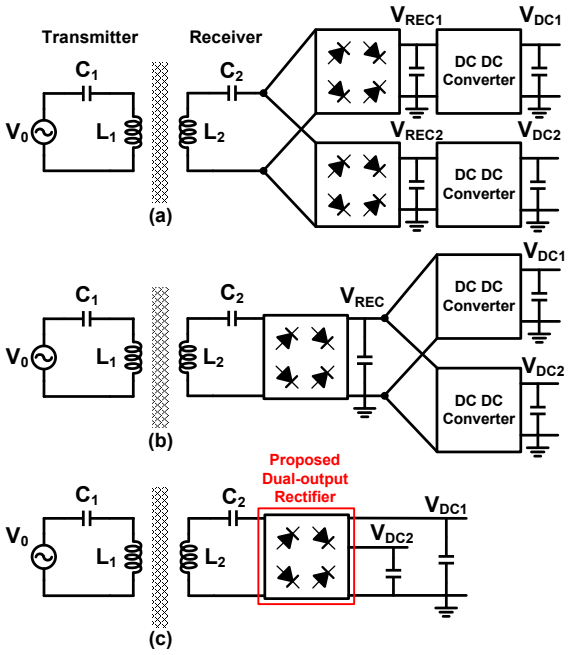

Fig. 1. Dual-output wireless power transfer systems with: (a) two rectifiers and two DC-DC converters; (b) one rectifier and two DC-DC converters; (c) one single-stage dual-output rectifier.

To date, diverse topologies are used to achieve a single-stage dual-output rectifier. By putting a switch between the rectifying bridge and each output node, a single-stage dual-output rectifier can be intuitively realized without evident cross-regulation issue [3]. However, this topology hardly regulates both outputs in one operation period because a part of power path is shared by two outputs. Another topology is using four PMOS diodes (upper side) and two NMOS diodes (down side), with each two PMOS diodes used for one output [4]. While this topology can easily handle two outputs in one operation cycle due to the branching power paths, it raises potential cross-regulation concerns. The topology presented in [1] splits one full-bridge rectifier into two half-bridge rectifiers, and each half-bridge rectifier is responsible for one output. In this case, two outputs can be managed simultaneously and independently. However, with this topology, an output can only be charged by a half-bridge rectifier instead of a full-bridge

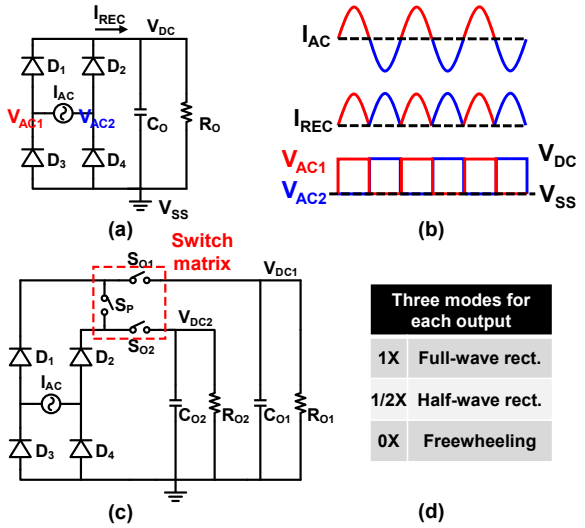

Fig. 2. (a) typical full-bridge rectifier; (b) the working waveform of the typical rectifier; (c) proposed dual-output rectifier; (d) three operation modes for each output in the proposed rectifier.

one, which means a limited driving capability.

In this paper, a single-stage dual-output rectifier is proposed with fine output regulation and full-wave operation. The proposed rectifier can work as either a full-bridge rectifier for one output (full-wave operation) or two parallel half-bridge rectifiers for two outputs (fine output regulation). By using hysteretic control, the rectifier can work in six different modes so that smooth output regulation can be achieved and cross-regulation issue can be eliminated. Section II presents the proposed topology and related working principle. Section III shows the system architecture of the proposed rectifier, as well as key circuit implementations. Section IV provides post-layout simulation results including transient performances and efficiencies. A conclusion is given in Section V.

II. Proposed Dual-Output Rectifier

At the receiving side of a WPT system, two kinds of resonance can be implemented to improve WPT performance: parallel resonance and series resonance. In this work, the series resonance topology is selected for a target power in the range of 200 - 800 mW, which is usually the case for wireless sensors and some biomedical implants. To reduce the volume of LC tanks, an industrial, scientific and medical (ISM) band frequency of 6.78 MHz is selected. Typically, a series-resonance LC tank can be regarded as an AC current source [6].

A typical full-bridge rectifier is shown in Fig. 2 (a), and its operation waveform is shown in Fig. 2 (b). The rectifier has a full-wave operation while supporting one output. By adding a switch matrix, including S_{O1}, S_{O2} and S_P, connected at the output stage, the rectifier becomes capable to generate two outputs, as shown in Fig. 2 (c). Due to the existence of S_P, either a full-wave operation or two half-wave operations can be achieved; S_{O1} and S_{O2} are used to form two conduction

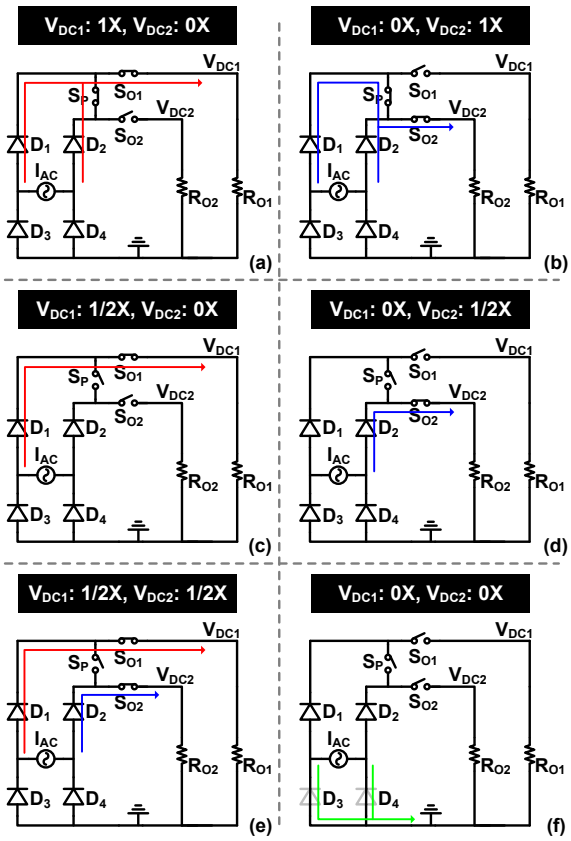

Fig. 3. Reconfiguration of the proposed rectifier with two outputs, V_{DC1} and V_{DC2}, working in: (a) 1X, 0X mode, (b) 0X, 1X mode, (c) 1/2X, 0X mode, (d) 0X, 1/2X mode, (e) 1/2X, 1/2X mode, and (f) 0X, 0X mode, respectively.

paths for two outputs. Thus, the proposed rectifier can regulate each of its outputs in three modes: full-wave (1X), half-wave (1/2X) and freewheeling (0X), as shown in Fig.2 (d).

The proposed rectifier can operate in six different modes in total. When V_{DC1} requires a large driving capability from the rectifier, S_P and S_{O1} will be ON with S_{O2} OFF to form a full-bridge rectifier for V_{DC1} (1X) while V_{DC2} is freewheeling (0X), as shown in Fig. 3 (a). The same way applies to V_{DC2} in heavy load, with S_P and S_{O2} ON and S_{O1} OFF (Fig. 3 (b)). For both 1X case, V_{DC1} has a higher priority to ensure proper operations of critical circuits. When V_{DC1} only requires a moderate driving capability, S_P will be OFF and S_{O1} will be ON to form a half-bridge rectifier for V_{DC1} (1/2X). Meanwhile, S_{O2} can be either ON or OFF to let V_{DC2} be regulated in 1/2X or 0X mode, as depicted in Fig. 3 (c) and (e). When V_{DC1} is high enough and needs no input from the rectifier, S_{O1} will be OFF to disconnect V_{DC1} (0X), while V_{DC2} can be regulated in 1X, 1/2X or 0X mode, as shown in Fig. 3 (b), (d), (f), respectively. Moreover, to guarantee proper circuit operations to the largest extent, a 1X mode is set to have a higher priority than a 1/2X mode. The detailed implementation of the controller will be discussed in Section III.

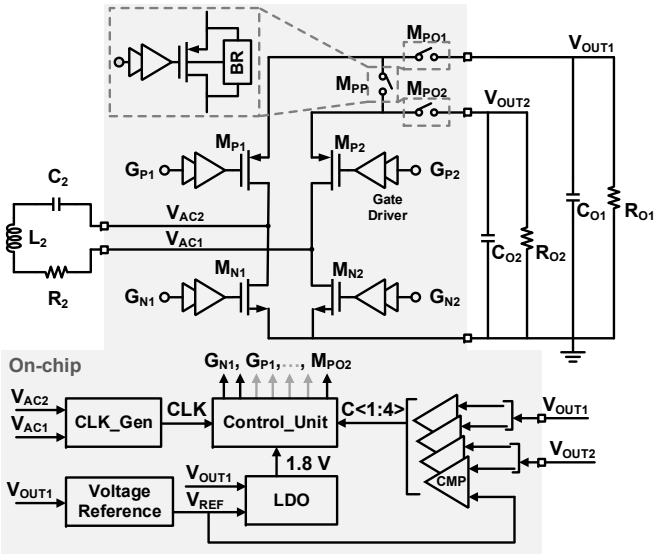

Fig. 4. System architecture of the proposed dual-output rectifier.

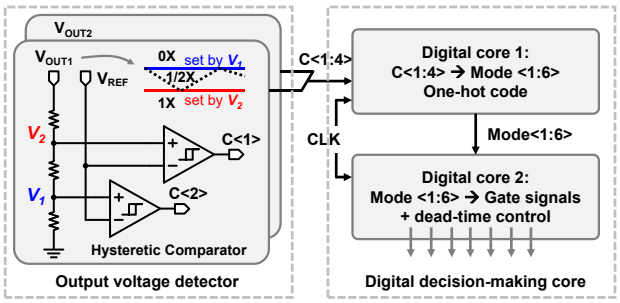

Fig. 5. Schematic of the proposed hysteretic control unit.

III. System Architecture and Circuit Implementations

A. System architecture of the proposed rectifier

Fig. 4 shows the system architecture of the proposed dual-output rectifier. M_{P1}, M_{P2}, M_{N1} and M_{N2} form a conventional rectifying bridge, and the proposed switch matrix is composed by M_{PP}, M_{PO1} and M_{PO2}. Bulk regulation (BR) is used to bias the body terminal of M_{PP}, M_{PO1} and M_{PO2} to the highest voltage in the system. The gate driving signals of the above power switches are generated by a hysteretic control unit involving an output voltage detector and a digital decision-making core. By comparing the AC input V_{AC1} and V_{AC2} versus ground, a 6.78 MHz CLK signal is generated for the hysteretic control unit. A reference voltage and a low power supply (1.8 V) are also realized on chip by a Bandgap and a low dropout regulator (LDO), respectively, for the hysteretic control unit.

B. Hysteretic control unit

Fig. 5 shows the schematic of the proposed hysteretic control unit. Output voltages V_{OUT1} and V_{OUT2} are firstly attenuated by voltage dividers and then detected by hysteretic comparators, with a preset threshold window. If an output voltage goes lower than the bottom threshold, a 1X mode request will be sent to digital core for this output. Similarly, an output voltage inside the threshold window corresponds to a 1/2X mode request, while an output voltage higher than the top threshold means no input is needed (0X). After the output voltage detector, digital core 1 is used to transfer the detection information C<1:4> to a 6-bit one-hot code Mode<1:6> in order to clarify which mode the rectifier should switch to. With mode information, the gate driving signals for the power switches are generated in digital core 2. To eliminate undesired short paths between outputs and ground, dead-time control is also integrated into the digital core 2 for gate driving signal generations.

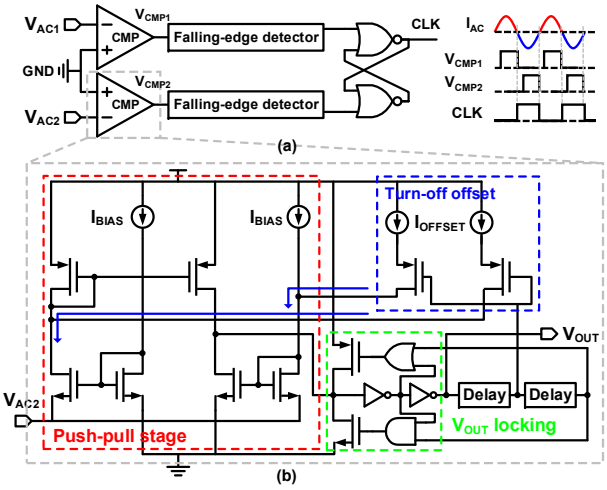

Fig. 6. (a) Schematic and operation waveform of the CLK generator; (b) circuit implementation of the delay-compensated comparator in the CLK generator.

C. Clock generator

Since the AC input works like a current source, the rectifier is always conducting, so the moment to turn on/off the power switches should be properly indicated through the CLK signal. To grab the zero-crossing moment of the AC input, two comparators with turn-off delay compensation are used to compare V_{AC1} and V_{AC2} versus ground. Then, by detecting the falling edge of the outputs of the delay-compensated comparator, a CLK signal can be generated through a SR latch without evident delay. The schematic and working waveform of the CLK generator are shown in Fig. 6 (a).

The detailed implementation of the delay-compensated comparator is shown in Fig. 6 (b). The comparator uses a push-pull stage to compare voltage signals to ground, with a fast slewing response. A pair of switched offset currents are introduced around the turn-off moment to enhance the pull-down ability and diminish the pull-up ability at the output node, in order to compensate the turn-off delay. Moreover, to avoid possible multiple-pulsing problems, a voltage locking block is also implemented at the output node.

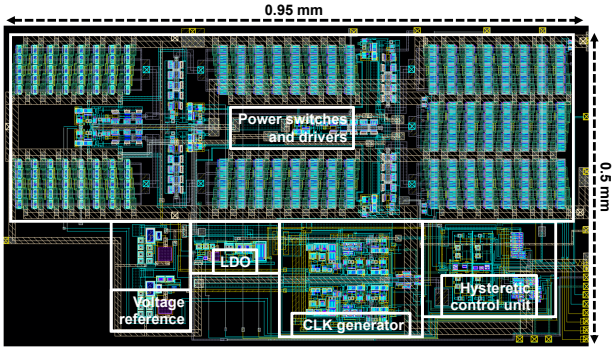

Fig. 7. Layout of the proposed dual-output rectifier.

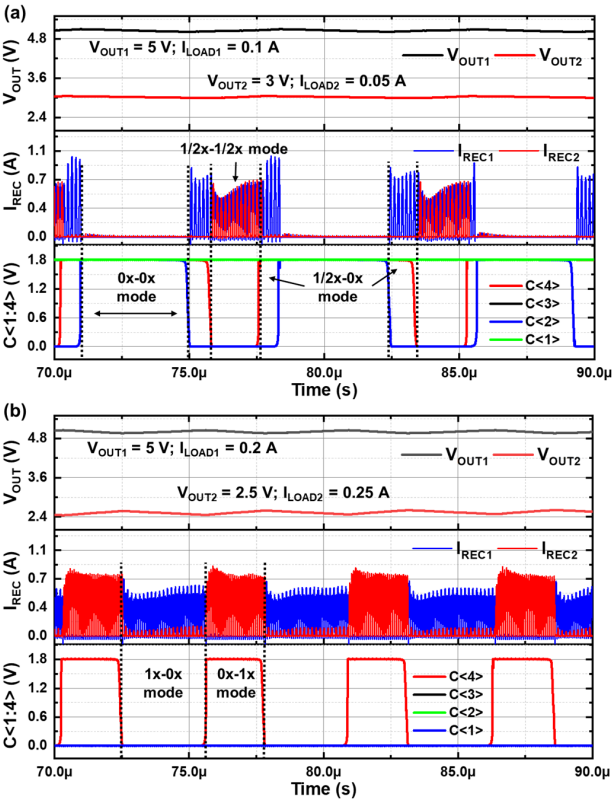

Fig. 8. Post-layout simulated transient waveforms with (a) I_{LOAD1} = 0.1 A and I_{LOAD2} = 0.05 A, (b) I_{LOAD1} = 0.2 A and I_{LOAD2} = 0.25 A. $I_{REC1/2}$ represents the current flowing through the rectifier when charging $V_{OUT1/2}$; $I_{LOAD1/2}$ is the load current induced by $R_{O1/2}$ in Fig. 4.

IV. Post-Layout Simulation Results

The proposed dual-output rectifier was designed in a 180-nm BCD process using standard 5-V devices. Fig. 7 shows the layout of the rectifier occupying an active area of 0.475 mm^2. Three off-chip capacitors are utilized to filter two rectifier outputs and compensate the LDO, respectively.

Fig. 8 shows the post-layout simulated steady-state waveforms of the proposed rectifier in different load conditions. Two output voltages are designed to be 3 V and 5 V, respectively. A modeled WPT frontend is used to provide the AC input, and preset to ensure the rectifier is capable to drive two 0.2 A loads. The post-layout simulations show that the rectifier can regulate each output in three different modes regarding three different driving capabilities. When the load for V_{OUT1} (I_{LOAD1}) is 0.1 A and I_{LOAD2} is 0.05 A, the rectifier works alternatively in 1/2X and 0X modes, equivalent to two parallel half-bridge rectifiers achieving a fine regulation for each output (Fig. 8 (a)). With I_{LOAD1} = 0.2 A and I_{LOAD2} = 0.25 A, the rectifier always works in 1X mode for each output to provide a large driving capability in the heavy load condition (the given load is too heavy for V_{OUT2} to maintain 3 V), as shown in Fig. 8 (b). Fig. 9 depicts the post-layout simulated PCE of the proposed rectifier with both loads in the range of 0.1 - 0.22 A. A peak efficiency of 80.1% is obtained when I_{LOAD1} = I_{LOAD2} = 0.2 A and the output power is 1.6 W in total. The efficiency drops when the rectifier works in light load conditions, mainly due to the freewheeling conduction losses.

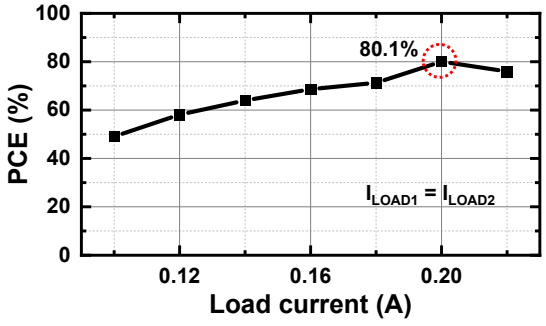

Fig. 9. Post-layout simulated PCE of the proposed dual-output rectifier.

V. Conclusion

A 6.78 MHz single-stage dual-output reconfigurable rectifier is presented in this paper. With a reconfigurable switch matrix and a hysteretic control unit, the proposed rectifier can operate as either a full-bridge rectifier or two parallel half-bridge rectifiers, to achieve either a large driving capability or fine output regulations. A peak efficiency of 80.1% is obtained, and the maximum total output power reaches 1.6 W.

References

[1] J. Lin, Y. Lu et al., "A Single-Stage Dual-Output Regulating Rectifier With Hysteretic Current-Wave Modulation," in IEEE Journal of Solid-State Circuits, vol. 56, no. 9, pp. 2770-2780, Sept. 2021.

[2] Guoxing Wang, Wentai Liu, M. Sivaprakasam and G. A. Kendir, "Design and analysis of an adaptive transcutaneous power telemetry for biomedical implants," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 52, no. 10, pp. 2109-2117, Oct. 2005.

[3] F. -B. Yang, J. Fuh and P. -H. Chen, "A 13.56MHz Wireless Power Transfer System with Dual-Output Regulated Active Rectifier for Implantable Medical Devices," 2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS), 2018, pp. 440-443.

[4] Q. W. Low and L. Siek, "A Single-Stage Dual-Output Tri-Mode AC-DC Regulator for Inductively Powered Application," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 9, Sept. 2019.

[5] Z. Xue et al., "Single-stage dual-output AC-DC converter for wireless power transmission," 2018 IEEE Custom Integrated Circuits Conference (CICC), 2018, pp. 1-4.

[6] Y. Lu and W. -H. Ki, CMOS Integrated Circuit Design for Wireless Power Transfer. Springer, 2018.