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23.3 A 2.6-to-4.1GHz Fractional-N Digital PLL Based on a Time-Mode Arithmetic Unit Achieving -249.4dB FoM and -59dBc Fractional Spurs

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In a fractional-N PLL, it is beneficial to minimize the input range of its phase detector (PD) as it promotes better linearity and higher PD gain for suppressing noise contributions of the following loop components. This can be done by canceling the predicted instantaneous time offset between the frequency reference (FREF) and the variable oscillator-clock (CKV) edges prior to the PD. There are currently two main cancellation strategies. The first is to align FREF and CKV by inserting a digital-to-time converter (DTC) on either path. However, due to the DTC nonlinearity and its susceptibility to PVT variations, the PLL can suffer from large fractional spurs. Although system-level techniques, e.g., background calibration [1], supply ripple reduction [2], and DTC code randomization [3], can partially alleviate these DTC issues, the overall system complexity worsens. The second method is to convert and cancel the predicted time offset in the voltage domain [4]. This arrangement is less sensitive to PVT variations. However, the accuracy of the time-to-voltage conversion relies on the strict trade-offs between the power consumption, noise, and linearity of a current source. In this work, we introduce a third solution based on a time-mode arithmetic unit (TAU), which outputs a weighted sum of time delays between the (falling) edges of FREF and CKV, as well as between two consecutive CKV edges. Compared with DTC-based solutions, it is less sensitive to PVT variations, as its output merely varies by the ratio of RC time constants, thus ensuring low fractional spurs with no extra system complexity. Compared to the voltage-domain solutions, the absence of a current source is beneficial for phase-noise optimization and migration to more advanced technology nodes. Moreover, TAU can implicitly provide a time-amplification (TA) gain, thus further suppressing the noise of subsequent blocks.

Figure 23.3.1 shows the proposed digital PLL based on TAU, which performs three fundamental tasks: instantaneous time-offset prediction, time-offset cancellation, and residue-time-error amplification. First, TAU extracts the DCO period (T_{CKV}), scales it by $1-\Phi_{R,frac}$, where $\Phi_{R,frac}$ is the fractional part of the accumulated frequency-control word (FCW), then time-registers the properly scaled prediction. Second, TAU samples the delay (Δt_s) between the falling edges of FREF and subsequent CKV, and then subtracts it from the stored prediction. Third, TAU amplifies the residue time error by a factor of G_{TA} and launches CMP_P and CMP_N edges separated by the time-domain output (Δt_{out}). The basis of realizing such a system lies in the TAU processor, whose output is $\Delta t_{out} = \sum_{i=1}^{n} w_i \cdot \Delta t_i$, where Δt_i and w_i are, respectively, the i^{th} input time difference and its allocated weight. In the implemented PLL, n=4, so the three tasks for the TAU can be achieved by adjusting the 4 weights in this function.

Figure 23.3.2 depicts the evolution of the proposed TAU. We start from the simplified RC model of a time register (TR) [5], which sums and holds the input pulse widths. First, a capacitor C is charged to an initial voltage V_{init} above the threshold voltage, V_{th}, of the crossing comparator. When the active-low input pulses (SWD) are asserted, the corresponding switch is turned ON to discharge the capacitor C through a resistor R. Each pulse width is accumulated as a voltage drop on C. After all input pulses have been processed, SWD is pulled down to completely discharge the capacitor. The crossing comparator output (CMP) is triggered when V_C falls below V_{th}. The TR output is the delay between the last falling edge of SWD and the asserted CMP, which equals to an offset minus all input pulse widths. Nevertheless, this TR does not fulfill the TAU tasks as all w_is are 1, owing to the fixed RC time constant ($\tau=\tau_0$) for all input pulses. This is solved by the weighted time register (WTR), as the variable resistor and capacitor are used to change across the input pulses. The proposed WTR still has two issues. First, its output has a voltage-dependent offset, causing PVT susceptibility. Second, the intended TAU inputs are time differences, whereas WTR processes only pulse widths. To resolve those, we use two differential WTRs operating in parallel and employ a conventional phase/frequency detector (PFD) prior to the WTRs to perform a "time-difference to pulse-width-difference" (T→PW) conversion, as shown in Fig. 23.3.2 (right). However, during the final discharge, this conversion is unwanted as it prevents the complete discharge of WTRs, so a second mode is added to the PFD to disable it (via $\overline{READ}$).

As revealed in Fig. 23.3.3, a few auxiliary blocks, such as snapshot and predischarge finite-state machines (FSMs), are added to generate TAU time-domain inputs and its weighting factors, thereby facilitating its incorporation into the proposed PLL. The three aforementioned tasks of the TAU (i.e., time-offset prediction, time-offset cancellation and residue-time-error amplifications) are mapped into 3 consecutive states: predischarge, snapshot, and TA. Accordingly, the dual-mode PFD is extended to a tri-mode version to support these states. Moreover, the variable components in the WTRs are realized with the switched-resistor bank (R-bank) and switched-capacitor bank (C-bank) consisting of 223-unit capacitors, C_U, along with a fixed C_0. To avoid any inaccuracy caused by charge sharing with subsequently connected units, the C-bank can only disengage its unit cells in one complete TAU conversion cycle. The cross comparator is gated, awaiting the TA state to reduce the crowbar current.

Figure 23.3.3 also includes the timing diagram of one TAU conversion cycle. It starts with the FREF rising edge, which disconnects the WTRs capacitors from V_{init}. This triggers the predischarge state in which T_{CKV} is scaled by the ratio of $1-\Phi_{R,frac}$ and then time-registered. To achieve this, the predischarge FSM, resembling asynchronous SAR-ADC logic, interacts with the tri-mode PFD to sample CKV for generating 3 discharging pulse pairs with a width difference of T_{CKV} (see $SWD_{P,N}$ within the blue dashed rectangle). For each pulse pair, the FSM also adjusts R&C tuning codes (CT and RT) to achieve the desired scaling ratio with a 10b accuracy, i.e., 7b fine tuning in the 1st pulse pair by CT (with corresponding value N_C), and 3b coarse tuning in the 3rd pulse pair by RT (with corresponding value N_R). Such a tuning strategy reduces the required range of the nonlinear capacitive tuning to improve the overall linearity of the TAU. The 2nd pulse pair is used to add an extra offset, which collaborates with the delay selection logic (red block in Fig. 23.3.1) to address the metastability issue in the snapshot circuit. Next, the TAU enters the snapshot state, in which Δt_s is sampled and subtracted from the registered time. At the FREF falling edge, a differential snapshot circuit captures Δt_s and outputs it as a delay between the rising edges of $CKRG_P$ and $CKRG_N$. By utilizing $CKRG_{P,N}$ instead of CKV, the tri-mode PFD generates the pulse pair to discharge WTRs capacitors accordingly. After the Δt_s subtraction, the WTRs contain only a tiny residue due to the DCO phase noise, which is amplified and output in the next state (TA state). This state corresponds to the final discharge of the conceptual TAU in Fig. 23.3.2. Here, the TA FSM, clocked by CKV, disables the T→PW conversion of the PFD and adjusts the RT to set the TA gain through the ratio between the time constants of the TA and snapshot states. The FSM also triggers the simultaneous falling of SWD_P and SWD_N in the tri-mode PFD to discharge the WTRs remaining capacitors and output the amplified residue (Δt_{out}). Once the TDC quantizes Δt_{out} (indicating by $\overline{TDC_{done}}$), the TAU resets itself and charges the WTRs internal capacitors to prepare for the next FREF cycle.

The proposed PLL was fabricated in 40nm CMOS (Fig. 23.3.7) with an active area of 0.31mm^2. The PLL operates from 2.56 to 4.1GHz (46% tuning range) with a 40MHz FREF. According to Fig. 23.3.4, at the fractional channel of 2668.2MHz, the measured rms jitter (integrated from 10kHz to 40MHz and including all spurs) is 182fs. With the power consumption of 3.48mW, it corresponds to an FoM of -249.4dB. Figure 23.3.5 reveals the spurs in a near-integer channel of 2680.04MHz. The reference spur is -73.5dBc. Without applying any calibration, the worst fractional spur is -44.5dBc at a 10kHz offset. Considering the fractional spurs are dominated by the TAU nonlinearity, mainly attributed to the mismatch of the R-bank and the C-tuning gain error, a piecewise LMS calibration similar to [6] is performed for spur compensation. As a result, the worst fractional spur reduces to -59.3dBc (at a 50kHz offset). While sweeping the PLL fractional frequency near 2680MHz, the worst-case fractional spur remains <-59dBc. Moreover, while keeping all PLL settings (including the calibration codes) the same, the worst-case fractional spur only increases to -54dBc when the TAU supply voltage is raised by 10%. This is a remarkable improvement compared with the DTC-based counterparts, as they would generate substantial spurs if their transfer-function drift could not be compensated. The PLL performance is summarized in Fig. 23.3.6 and compared with prior-art PLLs. Considering the stricter trade-offs between power and performance in low-power wideband designs, the spur and FoMs of this work are very competitive.

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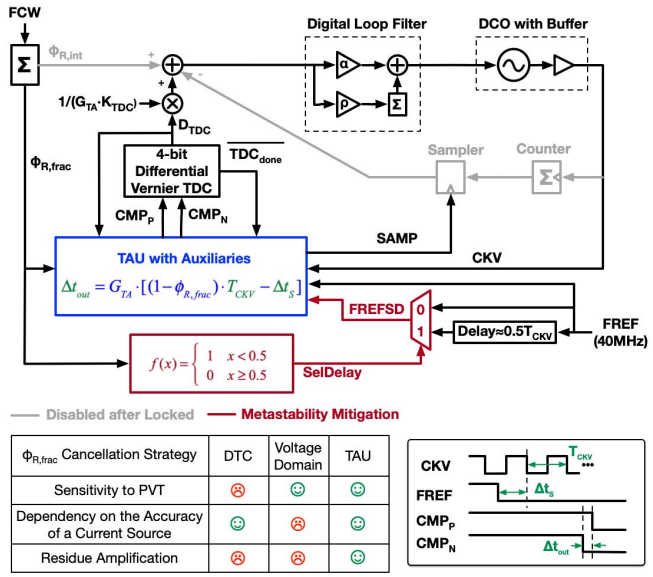


$\Phi_{R,frac}$ Cancellation Strategy	DTC	Voltage Domain	TAU
Sensitivity to PVT	☹	☺	☺
Dependency on the Accuracy of a Current Source	☺	☹	☺
Residue Amplification	☹	☹	☺

Figure 23.3.1: System overview of the proposed time-mode arithmetic-unit (TAU)-based PLL.

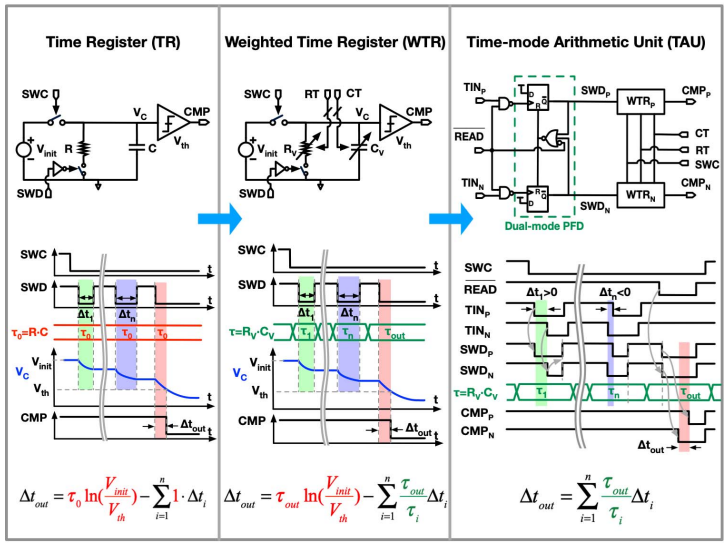
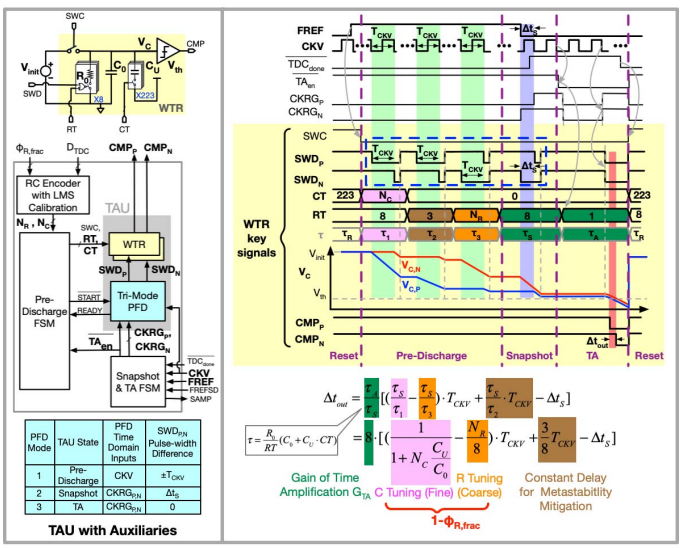


Figure 23.3.2: Conceptual implementation of the proposed TAU: evolution from the TR to the WTR and finally to the TAU.



PFD Mode	TAU State	PFD Time Domain Inputs	SWD$_{P,N}$ Pulse-width Difference
1	Pre-Discharge	CKV	$\pm T_{CKV}$
2	Snapshot	CKRG$_{P,N}$	Δt_S
3	TA	CKRG$_{P,N}$	0

TAU with Auxiliaries

Figure 23.3.3: Block diagram of the proposed TAU with auxiliary circuits (left), the timing diagram of the TAU in a locked state (upper-right), and the TAU output expression (lower-right).

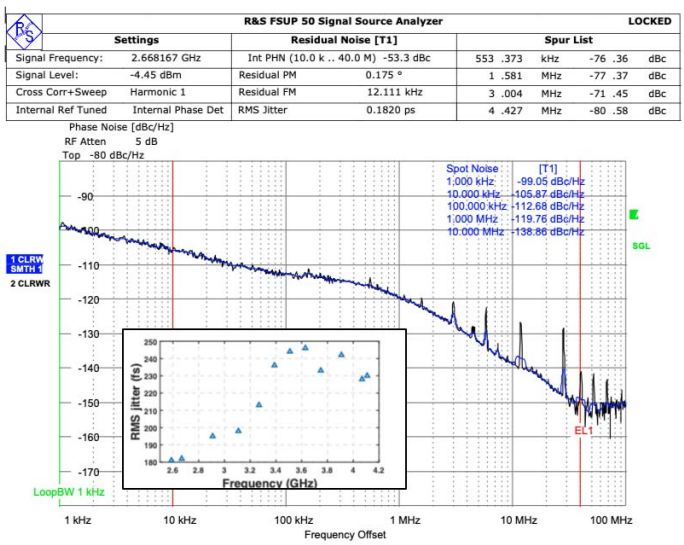


Figure 23.3.4: Measured phase noise and jitter (with spurs) in the fractional-N mode. The jitter degradation at higher frequencies is due to worse DCO phase noise caused by its very wide tuning range.

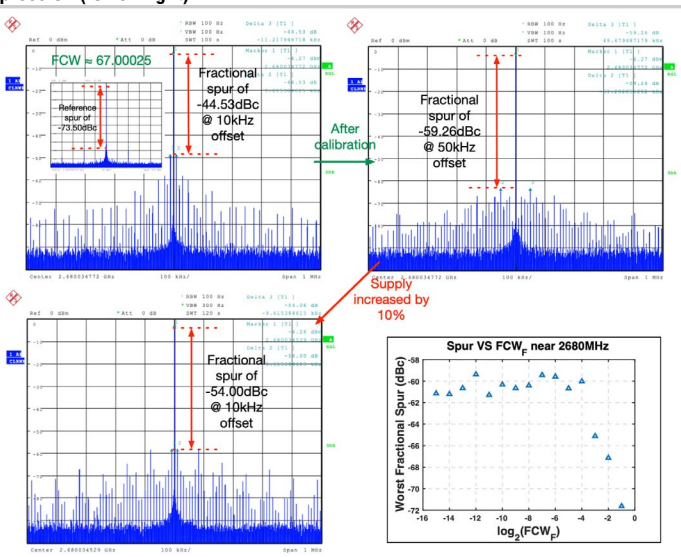


Figure 23.3.5: Measured reference and fractional spurs at a near-integer fractional-N channel (2680.04MHz), and the worst fractional spur versus the fractional part of the frequency-control word (FCW_F) near 2680MHz.

	this work	X. GAO ISSCC'16	H. Liu ISSCC'18	A. Santiccioli ISSCC'20	L. Wu JSSC'21	Z. Xu VLSI'21	W. Wu ISSCC'21	M. Mercandelli ISSCC'21	J. Kim ISSCC'21
Process (nm)	40	28	65	28	130	65	14	28	65
PLL Type & Architecture	Type-II Fractional-N Digital	Type-II Fractional-N Digital	Type-II Fractional-N Digital	Type-II Fractional-N Digital	Type-II Fractional-N Digital	Type-II Fractional-N Hybrid	Type-II Fractional-N Analog	Type-II Fractional-N Digital	Type-II Fractional-N Digital
Phase Detection Strategy	TAU + TDC	DTC + SPD[1]	DTC + TA + TDC	DTC + Bang-Bang PD	Voltage Domain	DTC + SPD[1]	DTC + SPD[1]	DTC + Bang-Bang PD	Voltage Domain
Reference (MHz)	40	40	26×2	500	80	50	76.8×2	250	150
DCO/VCO Freq. (GHz)	2.68	3.88	2.44	13.5	3.36	3.3	6.2	NA	7.3
Tuning Range (GHz)	2.56 to 4.1 (46%)	2.7 to 4.33 (46%)	2.0 to 2.8 (33%)	12.8 to 15.2 (17%)	2.99 to 3.5 (16%)	NA	5 to 7 (33%)	12.9 to 15.1 (16%)	14.0 to 16.0 (13%)
Int. RMS Jitter (fs) & Integ. BW (Hz)	182 (10k to 40M)	159 (10k to 40M)	530 (10k to 10M)	66.2 (1k to 100M)	101 (10k to 40M)	263 (10k to 10M)	91.5 (10k to 40M)	107.6 (1k to 100M)	104 (10k to 30M)
Worst Frac Spur (dBc)	-59	-57.5[2]	-56	-61	-56	-53	-66.4[2]	-50.4	-61
Ref. Spur (dBc)	-73.5	-81.5[2]	-72	-80.1	-79	-80	-66[2]	-73.2	NA
Built-in Resilience to Supply Change	Yes	No	No	No	Yes	No	No	No	No
Power (mW)	3.48[3]	8.2	0.98	19.8	9.2	4.6	8.2	10.8	7.3
FoM[4] (dB)	-249.4	-246.8	-246	-250.6	-250.3	-246	-251.6	-249	-251
FoM$_N$[5] (dB)	-267.7	-266.7	-262.7[6]	-264.9	-266.5	-264.2	-267.7[6]	NA	-271
Active Area (mm^2)	0.31[7]	0.3	0.23	0.17	0.27	0.48	0.31	0.21	0.21

1. Sampling Phase Detector
2. Normalized to DCO/VCO frequency
3. Supplied by 1.0V except for DCO, which is supplied by 1.1V to compensate for the inductor Q degradation, possibly due to metal dummy filling inside the coil.
4. FoM=10·log$_{10}$[(Jitter/1s)^2·Power/1mW)
5. FoM$_N$=10·log$_{10}$[(Jitter/1s)^2·Power/1mW/(f_{osc}/f_{ref})]
6. Calculated with the PLL input reference frequency (after doubler).
7. Excluding output drivers and debugging SRAMs

Figure 23.3.6: Performance comparison with prior-art fractional-N PLLs.

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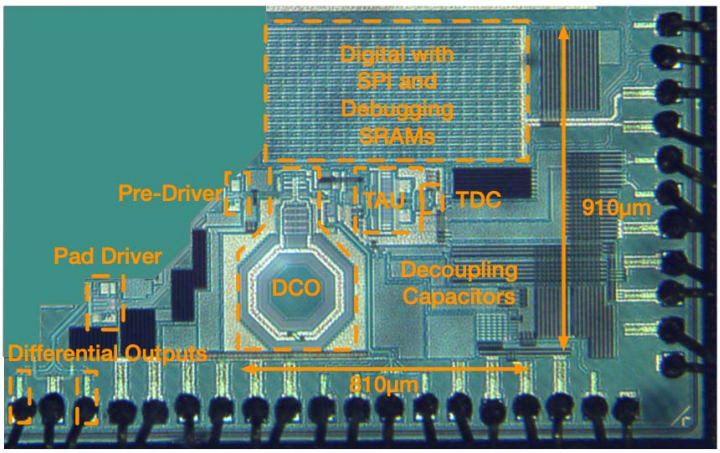

Figure 23.3.7: Die micrograph.

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