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A Chopper Class-D Amplifier for PSRR Improvement Over the Entire Audio Band

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***Abstract*— The power supply rejection ratio (PSRR) of conventional differential closed-loop Class-D amplifiers is limited by the feedback and input resistor mismatch and finite common-mode rejection ratio (CMRR) of the operational transconductance amplifier (OTA) in the first integrator. This article presents a 14.4-V Class-D amplifier employing chopping to tackle the mismatch, thereby improving the PSRR. However, chopping-induced intermodulation (IM) within a pulsewidth modulation (PWM)-based Class-D amplifier can severely degrade PSRR and linearity. Techniques to mitigate such IM are proposed and analyzed. To chop the 14.4-V PWM output signal, a high-voltage (HV) chopper employing double-diffused MOS (DMOS) transistors is developed. Its timing is carefully aligned with that of the low-voltage (LV) choppers to avoid further linearity degradation. The prototype, fabricated in a 180-nm BCD process, achieves a PSRR of >110 dB at low frequencies, which remains above 79 dB up to 20 kHz. It achieves a total harmonic distortion (THD) of −109.1 dB and can deliver a maximum of 14 W into an 8-Ω load with 93% efficiency while occupying a silicon area of 5 mm^2.**

***Index Terms*— Audio power amplifier, Class-D amplifier, intermodulation (IM), power supply rejection ratio (PSRR), total harmonic distortion (THD).**

I. Introduction

CLASS-D amplifiers achieve high power efficiency by switching the output directly to the supply or ground, making them popular in audio applications. However, this inevitably leads to supply sensitivity. To reduce the supply sensitivity, a straightforward solution is to employ a well-regulated supply, but this increases cost. Alternatively, a supply filter can be used. However, for sufficient filtering within the audio band, bulky filter components are required. Hence, most monolithic Class-D amplifiers employ a closed-loop architecture, where the supply-induced error is suppressed by the loop gain [1]–[3], along with the distortion introduced in the output stage.

However, many closed-loop Class-D amplifiers, including [1]–[3], employ the bridge-tied load (BTL) configuration (Fig. 1), where the power supply rejection ratio (PSRR) of the Class-D amplifier not only depends on the loop gain but is also limited by the matching between the R_{IN} and R_{FB} pairs [4], [5]. Therefore, these components should be laid out carefully to minimize their mismatch [6]. However, as will be explained in Section II, to achieve a PSRR of more than 100 dB, the R_{IN} and R_{FB} pairs must match within 10 ppm, requiring excessive area or expensive trimming for high yield. The pseudo-differential structure can alleviate this tradeoff at the expense of increased noise, silicon area, and a loss in the output signal swing due to common-mode offset and its drift [5], which is exacerbated in Class-D amplifiers with a high closed-loop gain.

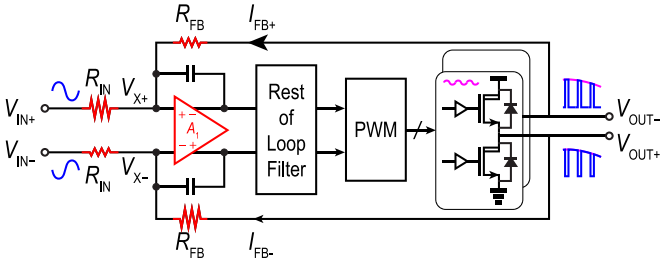

Fig. 1. Conventional closed-loop Class-D amplifier in a BTL configuration and sources of limited PSRR: feedback resistor mismatch, input resistor mismatch, and finite CMRR of the OTA in the first integrator.

In [7] and [8], this problem is addressed by closed-loop control of the Class-D amplifier's output common mode, which significantly improves the PSRR at low frequencies. However, the efficacy of this technique diminishes at high frequencies toward 20 kHz as the loop gain rolls off and the effects of mismatch re-emerge. Although chopping is a well-known technique for tackling mismatch [9], it has not been applied to the main signal path in Class-D amplifiers due to the presence of chopping-induced intermodulation (IM), which could demodulate high-frequency pulsewidth modulation (PWM) components at the switching output node into the audio band and degrade linearity [10].

This article improves the PSRR of a closed-loop Class-D amplifier in the BTL configuration by addressing the mismatch through chopping. Analysis shows that by choosing the chopping frequency (f_{CH}) to be an odd subharmonic of the PWM switching frequency (f_{SW}), even-order nonlinearity and PSRR degradation due to chopping-induced IM can be largely avoided. Furthermore, timing skew between the choppers reduces the linear output swing and thus should be

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minimized. A 14.4-V Class-D amplifier prototype is designed in a 180-nm BCD process, which achieves a total harmonic distortion (THD) of −109.1 dB. The minimum PSRR across eight samples is >110 dB at low frequencies and remains above 79 dB at 20 kHz, which improves over the previous high-voltage (HV) Class-D amplifiers [8], [11]–[13] by 17 dB.

This article is an extension of [14] and is organized as follows. Section II analyzes the causes of PSRR limitations in conventional Class-D amplifiers. Section III introduces the architecture of the proposed chopper Class-D amplifier, analyzes the effects of chopping-induced IM on PSRR and THD, and presents methods to minimize its impact. Section IV presents the circuit design to implement chopping in the 14.4-V Class-D amplifier. Section V presents the measurement results, followed by a conclusion in Section VI.

II. Effect of Mismatches on PSRR

This section discusses how PSRR is limited by various sources of mismatch in conventional Class-D amplifiers employing the BTL configuration switching in AD mode (i.e., fully differential switching [15]).

For the Class-D amplifier shown in Fig. 1, the in-band component of the output common mode equals half the supply, which also modulates the common mode at the virtual ground (V_X) of A_1

$$\Delta V_{X1,\mathrm{CM}} = \frac{R_{\mathrm{IN}}}{R_{\mathrm{FB}}+R_{\mathrm{IN}}}\Delta V_{\mathrm{OUT,CM}} = \frac{R_{\mathrm{IN}}}{2(R_{\mathrm{FB}}+R_{\mathrm{IN}})}\Delta V_{\mathrm{PVDD}}. \tag{1}$$

Resistor mismatch and finite common-mode rejection ratio (CMRR) of A_1 will then limit the Class-D amplifier's PSRR.

A. Resistor Mismatch

A straightforward analysis of Fig. 1 shows that the PSRR due to R_{FB} mismatch is given by [5]

$$\mathrm{PSRR}_{\Delta R_{\mathrm{FB}}} = \frac{R_{\mathrm{FB}}}{\Delta R_{\mathrm{FB}}}\frac{2A+2}{2A+1} \tag{2}$$

where $A = R_{\mathrm{FB}}/R_{\mathrm{IN}}$ is the closed-loop gain of the Class-D amplifier. For an HV Class-D amplifier, $A \gg 1$, thus, the PSRR is approximately $R_{\mathrm{FB}}/\Delta R_{\mathrm{FB}}$.

Similarly, the PSRR limit due to ΔR_{IN} is given by

$$\mathrm{PSRR}_{\Delta R_{\mathrm{IN}}} = \frac{R_{\mathrm{IN}}}{\Delta R_{\mathrm{IN}}}\frac{2A+2}{A}. \tag{3}$$

Compared with (2), for HV Class-D amplifiers, PSRR is less sensitive to R_{IN} mismatch only by about a factor of 2 compared to R_{FB} mismatch.

B. Finite CMRR of A_1

Due to $\Delta V_{X1,\mathrm{CM}}$ and the finite CMRR of A_1, the A_1's virtual ground will be offset by

$$\left|\Delta V_{X1,\mathrm{DM}}\right| = \left|\frac{\Delta V_{X1,\mathrm{CM}}}{\mathrm{CMRR}_{A1}}\right|. \tag{4}$$

Following the definition of CMRR [16], therefore, the Class-D amplifier's output will vary by

$$\Delta V_{\mathrm{OUT}} = \frac{R_{\mathrm{IN}}+R_{\mathrm{FB}}}{R_{\mathrm{IN}}}\Delta V_{X1,\mathrm{DM}} = \frac{R_{\mathrm{IN}}+R_{\mathrm{FB}}}{R_{\mathrm{IN}}}\frac{\Delta V_{X1,\mathrm{CM}}}{\mathrm{CMRR}_{A1}}. \tag{5}$$

Substituting $\Delta V_{X1,\mathrm{CM}}$ with (1), the PSRR due to the finite CMRR of A_1 is given by

$$\begin{aligned}\mathrm{PSRR}_{A1} &= \frac{R_{\mathrm{IN}}}{R_{\mathrm{IN}}+R_{\mathrm{FB}}}\frac{2(R_{\mathrm{FB}}+R_{\mathrm{IN}})}{R_{\mathrm{IN}}}\mathrm{CMRR}_{A1}\\ &= 2\mathrm{CMRR}_{A1}.\end{aligned} \tag{6}$$

III. Chopper Class-D Amplifier Architecture

This work aims to improve the PSRR by tackling the mismatch through chopping. Fig. 2 shows the architecture of the proposed Class-D amplifier, which employs AD mode fixed-frequency PWM. The R_{IN} and R_{FB} pairs are swapped periodically with choppers $\mathrm{CH_{in}}$, $\mathrm{CH_{fb}}$, and $\mathrm{CH_{vir}}$ such that they contribute equally to the two differential halves over time. The operational transconductance amplifier (OTA) A_1 is also chopped to improve its CMRR. Intuitively, with chopping, ΔR_{FB} and ΔR_{IN} in (2) and (3) are now set by the ON-resistance mismatch of the chopper switches, which can be made much smaller with reasonable sizing.

Conventionally, in continuous-time circuitry, chopping has been primarily applied to low-frequency small analog signals. In this work, however, significant HV high-frequency PWM components are present, and thus, the IM products between PWM and chopping should be carefully considered. It should be noted that no IM would occur when any signals pass through only two ideal choppers with perfect timing, if the circuit in between has no delay and infinite bandwidth. In practice, timing skew between the input and output choppers leads to IM. This is shown in Fig. 3, where two resistors are chopped, as is the case for, e.g., R_{FB}. When the chopping clocks are skewed by Δt, $I_{\mathrm{OUT}}(t)$ contains an additional component equal to $v_{\mathrm{IN}}(t)p(t)$, where $p(t)$ is a pulse train with a period of $1/(2f_{\mathrm{CH}})$, a width of Δt, and a height of 2. Such a scenario must be considered in HV Class-D amplifiers since the HV and low-voltage (LV) choppers are implemented differently and, therefore, can exhibit significant timing skew.

In a PWM-based Class-D amplifier, the output state (high/low) of V_{SW} is determined by comparing the loop filter output V_{LF} with a triangle carrier V_{TRI}. Therefore, by aligning the chopping transitions with the peaks of V_{TRI}, sampling of the signal-dependent transitions in V_{OUT} by $p(t)$ can be avoided, which would otherwise lead to signal-dependent IM products. This can be ensured by chopping at the peaks of the triangle wave used for PWM operation, as shown in Fig. 4(a). To the first order, this makes the IM products signal-independent. However, the output waveform of a practical Class-D amplifier includes the supply noise and *IR* drop components. By choosing f_{CH} as an even or odd subharmonic of f_{SW}, $p(t)$ would sample either $V_{\mathrm{PVDD}} - I_{\mathrm{out}}(t)R_{\mathrm{on}}$ at $2f_{\mathrm{CH}}$ or sample $V_{\mathrm{PVDD}} - I_{\mathrm{out}}(t)R_{\mathrm{on}}$ and $-V_{\mathrm{PVDD}} - I_{\mathrm{out}}(t)R_{\mathrm{on}}$ in an alternating fashion at $2f_{\mathrm{CH}}$, as shown in Fig. 4(a), where $I_{\mathrm{out}}(t)$ is the audio band signal current plus high-frequency

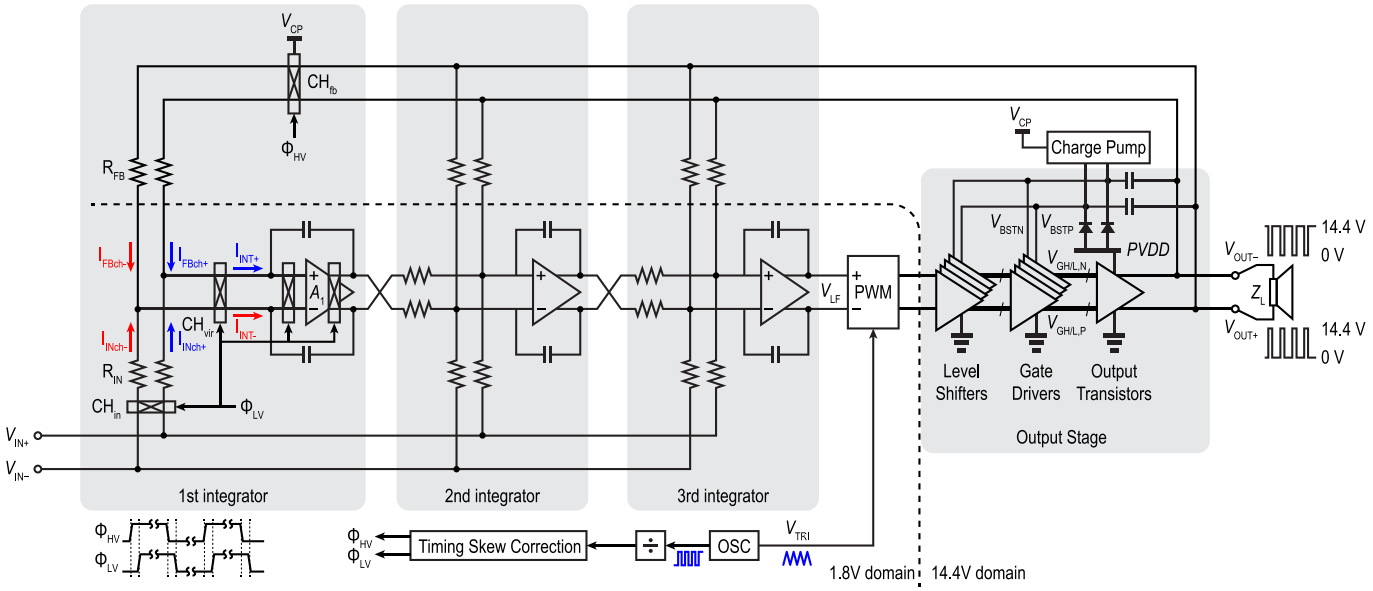

Fig. 2. Top-level block diagram of the proposed chopper Class-D amplifier.

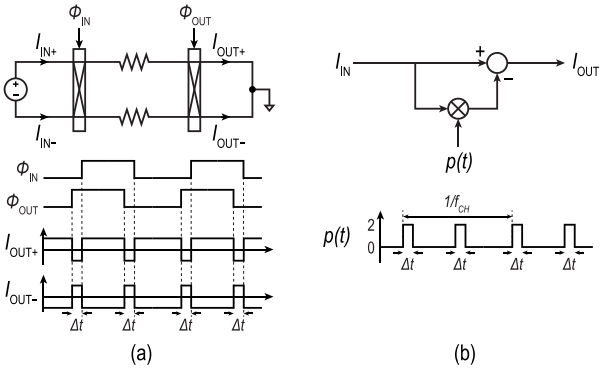

Fig. 3. Effect of chopper timing skew in the time domain. (a) Circuit model and (b) block diagram, and their respective waveform.

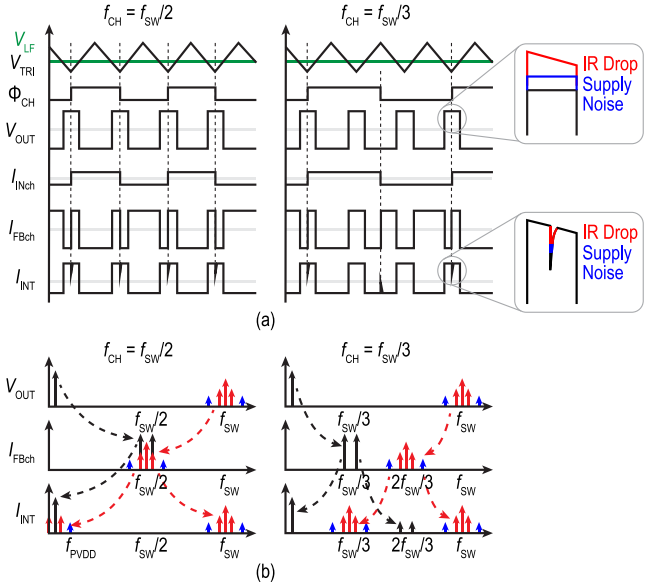

Fig. 4. (a) Time- and (b) frequency-domain behaviors of chopping a PWM signal.

ripple current and R_{on} is the ON-resistance of the output transistors. Sampling V_{PVDD} could affect the PSRR, while sampling $I_{out}(t)R_{on}$ could affect the THD. These will be analyzed in detail in the following.

A. Impact of IM on PSRR

By definition of the Class-D operation, the PWM output waveform is amplitude-modulated by V_{PVDD}. Assuming that V_{PVDD} is modulated by a sinusoid at frequency f_{PVDD}, in the frequency domain, sidebands appear in the spectrum of V_{SW} at $(2n+1)f_{SW} \pm f_{PVDD}$, where n is an integer, as shown (in blue) in Fig. 4(b).

When f_{CH} is an even subharmonic of f_{SW}, these sidebands are demodulated to f_{PVDD}, which becomes the limiting factor of the PSRR. This effect can be easily quantified in the time domain since $p(t)$ effectively samples V_{PVDD} with the same polarity at each chopping transition, as shown in Fig. 4(a). Therefore, the IM product is given in the time domain by $V_{PVDD}(t)p(t)$. In the frequency domain, the component at f_{PVDD} is proportional to the dc component of $p(t)$, which equals $4f_{CH}\Delta t$ (Fig. 3). Hence, the PSRR due to the chopping-induced IM is given by

$$\mathrm{PSRR}_{\mathrm{IM,even}} = 20\log_{10}\left(\frac{1}{4f_{CH}\Delta t}\right). \tag{7}$$

On the other hand, when f_{CH} is an odd subharmonic of f_{SW}, the IM product's polarity alternates for each chopping transition and, in the spectrum, appears at $f_{CH} \pm f_{PVDD}$. Therefore, by choosing f_{CH} sufficiently higher than 20 kHz, the IM products can be kept out of the audio band, as shown in Fig. 4(b).

Fig. 5 shows the simulated PSRR of the system shown in Fig. 2. The PWM switching frequency $f_{SW} = 2.1$ MHz. Except for a timing skew Δt introduced in CH_{fb} with respect

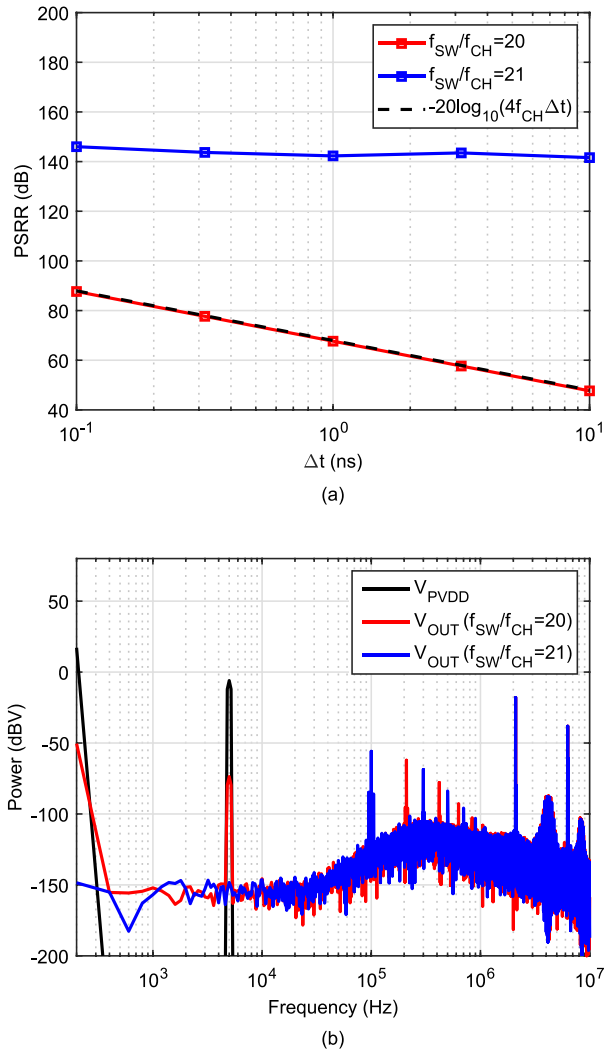

Fig. 5. (a) PSRR due to timing skew of CH_{fb} for $f_{CH} = 100$ kHz and $f_{CH} = 105$ kHz, from system-level simulations. (b) Spectra of the Class-D amplifier output V_{OUT} and supply voltage V_{PVDD} when $\Delta t = 1$ ns.

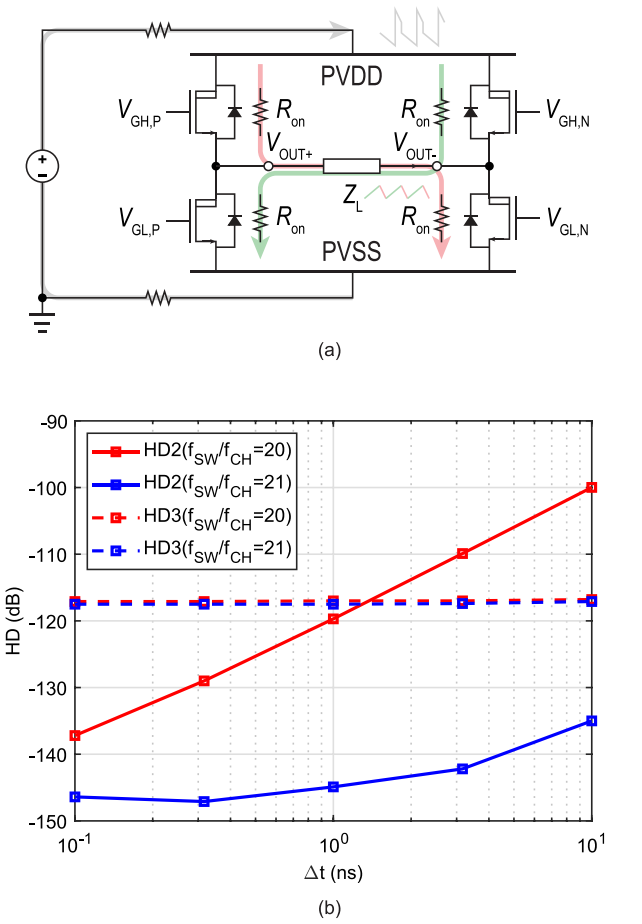

Fig. 6. (a) *IR* drop due to the parasitic resistance in the supply routing and ON-resistance of the output transistors. (b) HD due to timing skew of CH_{fb} for $f_{CH} = 100$ kHz and $f_{CH} = 105$ kHz, from system-level simulations.

to all other choppers, all blocks are ideal. The PSRR is plotted versus Δt for $f_{CH} = 100$ kHz and $f_{CH} = 105$ kHz. When $f_{CH} = 105$ kHz, the PSRR suffers as predicted by (7), whereas when $f_{CH} = 100$ kHz, the PSRR remains high regardless of Δt.

B. Impact of IM on Linearity

Aside from supply voltage variations, V_{SW} also deviates from the ideal levels due to the *IR* drop in the output transistors and supply routing, as shown in Fig. 6(a). The load current consists of both audio band signal current and high-frequency PWM ripple current. For a sinusoidal input, it contains sidebands around multiples of f_{SW} besides the audio signal. The sideband spacing around odd multiples of f_{SW} is $2Nf_{IN}$, whereas the sideband spacing around even multiples of f_{SW} is $(2N-1)f_{IN}$ [17], [18], where N is a positive integer. The strongest sidebands are located around f_{SW}.

If f_{CH} is chosen as an even subharmonic of f_{SW}, the strongest sideband components are demodulated to base-band and contribute to even-order harmonic distortion (HD) [Fig. 4(b) red]. This is avoided if f_{CH} is chosen as an odd subharmonic of f_{SW}. Nevertheless, in both cases, the sidebands around even multiples of f_{SW} are demodulated into odd-order HD. Fortunately, these sidebands located at higher frequencies are lower in amplitude than those around f_{SW}. The *IR* drop induced by these sidebands components is further reduced by the increasing inductive impedance of the speaker [19], leading to less IM distortion.

An analytical derivation for the HD involving the Fourier series expansion of the PWM waveform of V_{OUT} [17] would be lengthy. For brevity, Fig. 6(b) shows the simulated HD due to chopping-induced IM for $f_{CH} = 100$ kHz and $f_{CH} = 105$ kHz. All circuit blocks are ideal except for a timing skew Δt that is introduced in CH_{fb} with respect to other choppers. The load impedance Z_L is 8 Ω in series with 44 μH to represent a realistic speaker model. The supply routing resistance adds additional *IR* drop and therefore is modeled and assumed to be 50 mΩ and $R_{on} = 150$ mΩ [Fig. 6(a)] is assumed, to balance gate charging loss and conduction loss in the output stage. As discussed above, choosing $f_{CH} = 100$ kHz avoids even-order HD even with excessive Δt. Moreover, since the *IR* drop induced by the PWM components is attributed to the ripple current, the relatively large inductance exhibited in a

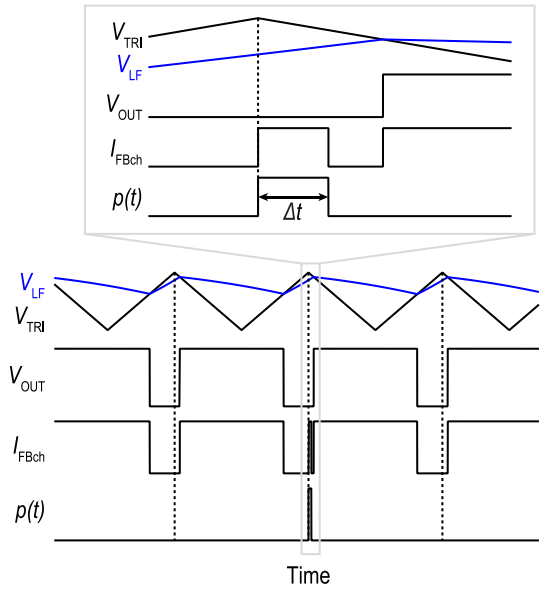

Fig. 7. Transient waveform in the closed-loop chopper Class-D amplifier ($f_{SW}/f_{CH} > 1$).

loudspeaker helps keep this distortion below −100 dB. The constant HD3, on the other hand, is attributed to the inherent PWM residual aliasing distortion and therefore is independent of Δt [20].

Although minimizing Δt does not seem to improve HD once f_{CH} is chosen to be the odd subharmonic of f_{SW}, it is only true when $p(t)$ does not sample the transitions of V_{SW}. Minimizing Δt is still essential for maximizing the linear output swing of the chopper Class-D amplifier. This is because in a closed-loop Class-D amplifier, the output of the loop filter V_{LF} (Fig. 2) contains residual PWM ripple, which skews the center of the PWM pulses away from the triangle wave peaks [20], as shown in Fig. 7. As the Class-D feedback loop's unity-gain frequency (f_U) is increased toward the maximum of f_{PWM}/π for maximal loop gain [21], the interval between a triangle wave peak and the next PWM transition is further reduced. Once this interval reduces below Δt, which is likely to happen under a large input, distortion due to IM drastically increases.

C. Other Sources of IM

So far, only IM due to the timing skew between choppers is analyzed. In addition, two other circuit nonidealities can contribute to IM. First, when the circuit between the two choppers delays or filters the signal, glitches appear in the output waveform. This is the case when a pair of chopped resistors (e.g., R_{FB}) exhibit nonnegligible parasitic capacitance or when a chopped transconductor (e.g., in the OTA of the first integrator) has finite bandwidth. The resulting IM can be described by a model similar to Fig. 3(b), where the pulse shape of $p(t)$ is modified to capture the settling transient [22]. Second, when the OTA in the first integrator is chopped, the parasitic capacitors at the input and internal nodes inject charge packets into the integrator at each chopping transition. Effectively, chopping samples the voltage on these parasitic capacitors at $2f_{CH}$ [23].

Since both abovementioned IM mechanisms occur between the PWM signal and even harmonics of f_{CH}, they can be largely mitigated by choosing f_{CH} to be an odd subharmonic of f_{SW}. Extra measures, such as compensating the resistor delay in the chopper clock generator and increasing the bandwidth and gain of the OTA [24], can further help minimize the residual IM effect, which will be explained in detail in Section IV.

IV. Circuit Implementation

A. Overview

The Class-D amplifier in this work uses a 14.4-V supply for the output stage and switches at $f_{SW} = 2.1$ MHz to avoid interfering with the AM band and achieve high loop gain [11], [13]. A fully differential third-order loop filter based on active *RC* integrators is employed (Fig. 2) for high loop gain [13], [25], with $f_U = 570$ kHz. The first stage of A_1 is chopped to boost its CMRR and eliminate its $1/f$ noise. In a 200-run Monte Carlo simulation, chopping improves the worst case CMRR of A_1 from 87 to 108 dB. The OTAs in the loop filter are designed in a two-stage feedforward compensated topology for high gain-bandwidth product (GBW), which helps to suppress IM at the virtual ground of the first integrator OTA due to chopping, as mentioned in Section III-C. To perform PWM, a differential triangle wave produced by an *RC* oscillator is compared with the loop filter output [25]. The input chopper employs conventional bootstrapping for high linearity.

Based on the analysis in Section II, f_{CH} is chosen to be $f_{SW}/21 = 100$ kHz to avoid PSRR degradation and even-order HD, while it is high enough to avoid IM around f_{CH} from folding back into the audio band. If a higher f_{CH} is used, more nonlinear glitches will be introduced by CH_{in}, which must process an audio waveform, unlike the mostly two-level waveform in CH_{fb}.

B. HV Chopper

CH_{fb} must handle the 14.4-V PWM output. As shown in Fig. 8, each switch consists of two back-to-back *n*-channel lateral DMOS (LDMOS) devices so that they can be completely turned off despite the presence of their body diodes. Level shifters are employed to translate the chopping clock to the floating gate drivers powered from floating regulators bootstrapped to the source nodes of each LDMOS switch. They are supplied by a charge pump that provides a dc voltage V_{CP} near 28 V.

Fig. 9(a) shows the regulator, in which a source follower buffers a Zener-based reference. The charge pump is shown in Fig. 9(b), which reuses the circuitry and takes advantage of the switching operation in the Class-D amplifier's output stage. Two off-chip bootstrap capacitors are employed to supply the high-side gate driver of the output stage [13]. They are charged to V_{PVDD} due to the switching operation. Through Schottky diodes D_1 and D_2, they charge V_{CP} to $\sim 2V_{PVDD}$ [Fig. 9(c)], which is buffered by a small output capacitor C_{CP} on-chip. Fig. 10(a) shows the level shifter, which is based on [25]. During each chopping transition, a current pulse pulls down one of the set-reset (SR)-latch inputs through

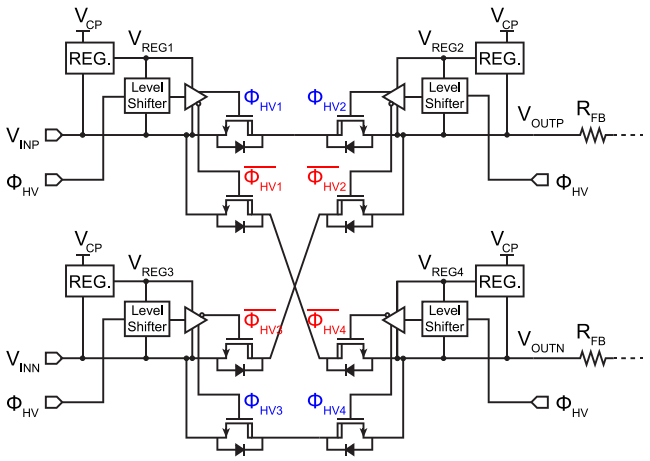

Fig. 8. Schematic of the HV chopper.

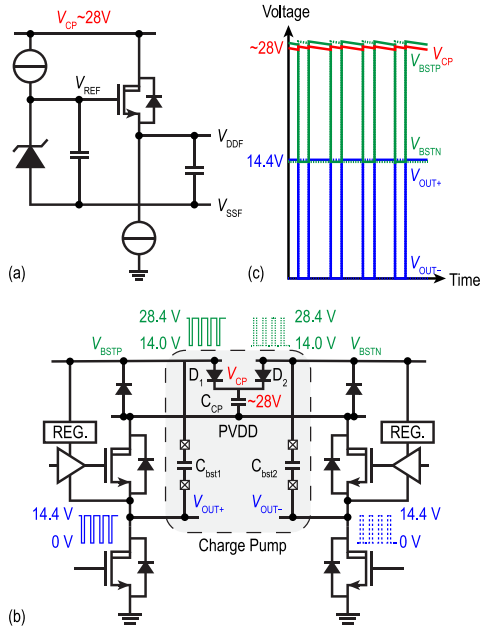

Fig. 9. (a) Floating regulator. (b) Charge pump. (c) Its timing diagram.

the corresponding pull-up resistors, thereby updating the level shifter's output.

C. Timing Skew Correction

As mentioned in Section III, the timing skew between CH_{fb} and the other choppers reduces the linear output swing. The main source of timing skew comes from the level shifter, whose delay is the sum of a fixed and a signal-dependent component. The latter is due to the V_{DS} modulation of the current source M_1 by the signal level at the corresponding terminal of CH_{fb}. To compensate for the signal-dependent delay, the voltage level (high/low) at each input and output terminal of CH_{fb} (i.e., V_{INN}, V_{INP}, V_{OUTN}, and V_{OUTP} in Fig. 8) is detected using a resistive voltage divider from V_{REG}, and a compensation delay is switched in/out. Fig. 10(b) shows the effect of the signal-dependent delay. Without compensation, the resulting timing skew leads to asymmetry in the output

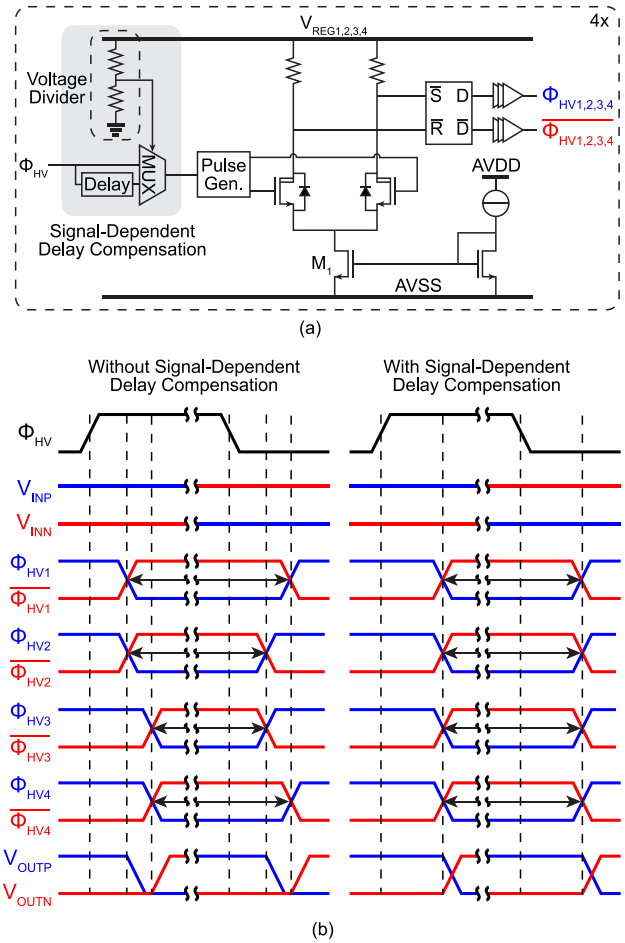

Fig. 10. (a) Level shifter with added signal-dependent delay compensation circuit. (b) Input–output and switch control signals in the HV chopper with and without compensation for the signal-dependent delay.

waveform, whose differential component can also be modeled using Fig. 3(b) with the pulse height modified to 1 for $p(t)$. The compensation delay minimizes the asymmetry and the pulsewidth of the resulting $p(t)$.

The fixed component of the level-shifter delay and the delay due to the parasitic capacitance of R_{FB} is compensated by a replica-based delay line to ensure good tracking over process, voltage, and temperature (PVT) variations. Fig. 11(a) shows the clock paths for all the choppers. The 2.1-MHz oscillator produces a triangle wave and a digital clock signal that toggles whenever the triangle wave changes its ramp direction [25]. The latter is divided by 21, to 100 kHz to drive the choppers. The chopping clock's duty cycle error compromises the efficacy of chopping. The design of the oscillator and divider ensures an accurate duty cycle for the chopping clock. Fig. 11(b) shows the current waveform with and without the replica. The mismatch between the level shifters and the replica results in a residual timing skew. Nevertheless, Monte Carlo simulation[1] shows that the replica-based timing skew correction reduces Δt from about 3.2 ns to

[1]The process design kit (PDK) does not include a mismatch model for the two LDMOS devices in the level shifter, so their mismatch contribution is not included.

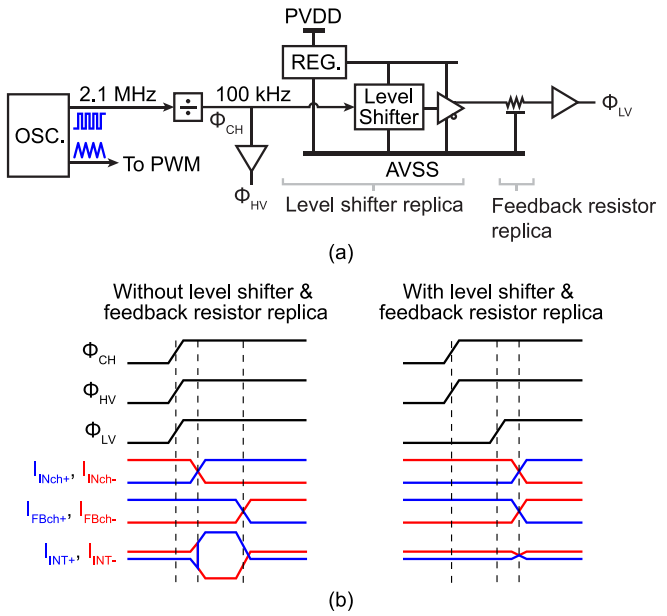

Fig. 11. (a) Replica delay circuit to align chopping transitions of HV and LV choppers. (b) HV and LV chopper clock signals and resulting input, feedback, and integrator current (annotated in Fig. 2) with and without the replica delay circuit.

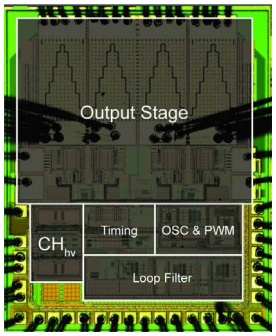

Fig. 12. Die micrograph.

within 200 ps. The input signal range with $p(t)$ and transitions of V_{SW} colliding is reduced from 12% to well below 1% of the full scale.

V. Measurement Results

A prototype of the proposed chopper Class-D amplifier is fabricated in a 180-nm BCD process,[2] and the die occupies 5 mm^2. Fig. 12 shows the die micrograph. The HV chopper and timing skew correction circuitry occupy 0.37 mm^2. For testability, the divide ratio between f_{SW} and f_{CH} is made programmable. The amplifier is loaded with 8 Ω in series with 44 μH, and its output is measured by an Audio Precision APx555 audio signal analyzer. The output stage supply is generated using a Keysight N6705C and also monitored by the APx555.

Fig. 13 shows the measured PSRR across the entire audio band, where V_{PVDD} is modulated by a $2V_{PP}$ sinusoid.

[2]The results reported here are obtained from a silicon revision of [14], which fixes a bond pad issue in [14] that caused the THD to degrade at large-signal levels.

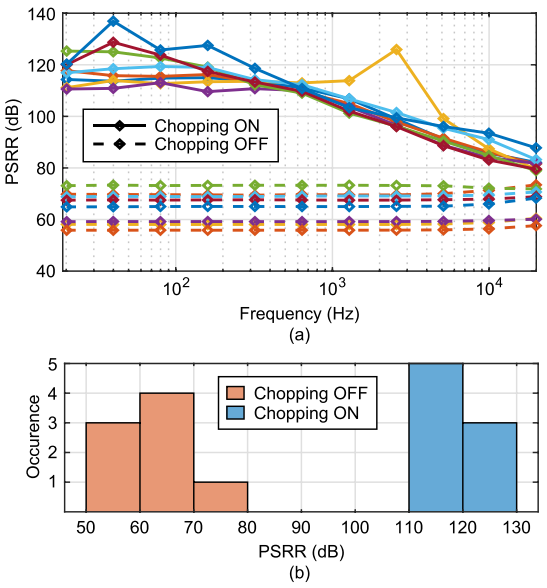

Fig. 13. (a) Measured PSRR versus f_{PVDD} of eight samples with chopping ON (solid) and OFF (dashed). (b) Histogram at 20 Hz.

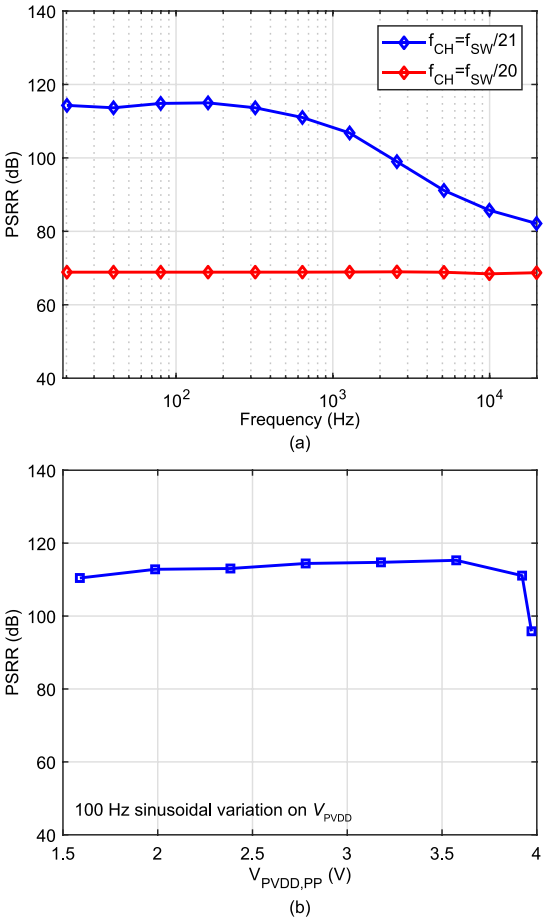

Fig. 14. (a) PSRR comparison between odd (f_{CH} = 100 kHz) and even (f_{CH} = 105 kHz) ratios between f_{CH} and f_{SW}. (b) Measured PSRR as the magnitude of the sinusoidal supply variation is increased.

The PSRR when chopping is turned off is shown in the dashed lines, showing a spread due to random mismatch of the resistors in the feedback network, with an average of

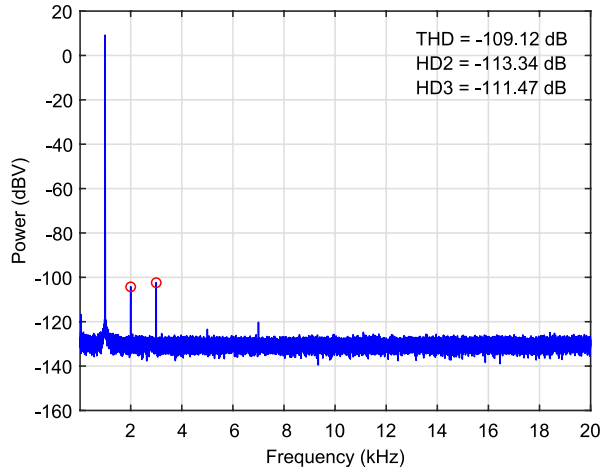

Fig. 15. Measured output spectrum at an output power of 1 W.

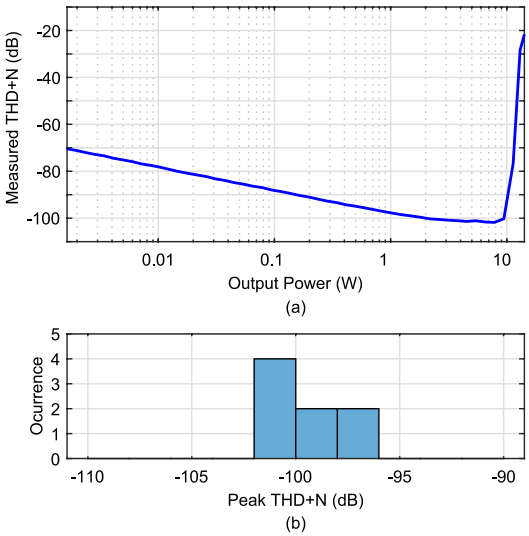

Fig. 16. (a) Measured THD+N across output power. (b) Peak THD+N for eight samples.

about 65 dB. When chopping is enabled, the worst case PSRR is improved by over 20 dB over the entire audio band, reaching a minimum of 110 dB at 20 Hz and 79 dB at 20 kHz. The worst case PSRR without chopping is below 60 dB. Achieving a PSRR of more than 100 dB through brute-force sizing would thus require the feedback resistors' width and length to be increased by more than 100 times [26], and their area would increase from 0.00016 mm^2 of this work to above 1.6 mm^2, which is more than four times larger than the area of the HV chopper and timing skew correction circuitry. Fig. 14(a) compares the PSRR performance when f_{CH} is programmed to $f_{SW}/21$ and $f_{SW}/20$ for the same sample. The PSRR is severely degraded when $f_{CH} = f_{SW}/20$, as mentioned in Section III. Fig. 14(b) shows the measured PSRR when the magnitude of the sinusoidal variation on V_{PVDD} is increased. The PSRR stays consistently high until the magnitude reaches about $4V_{PP}$, at which point the virtual ground of A_1 goes beyond 1.8 V, causing its input pair to operate in triode.

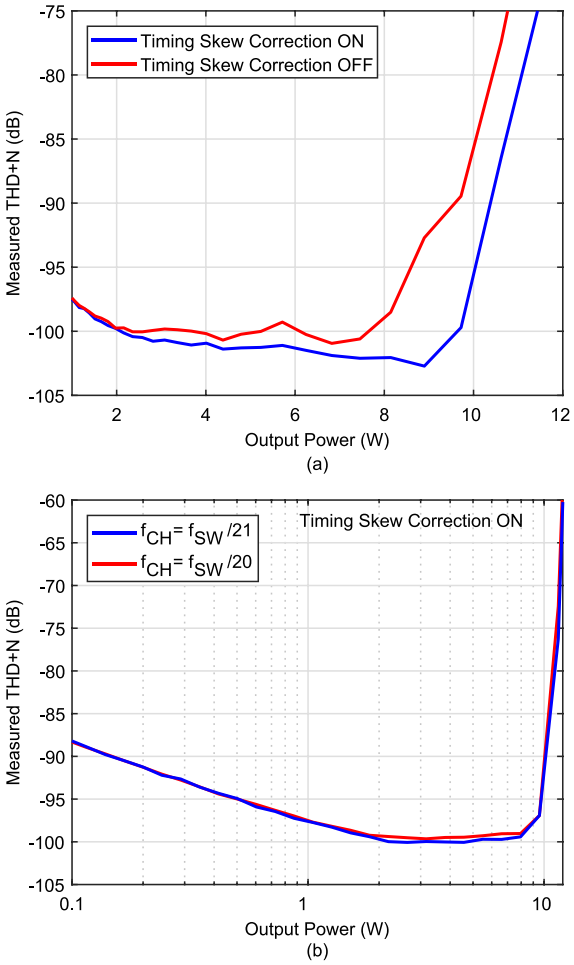

Fig. 17. THD+N comparison (a) with and without timing skew correction and (b) for $f_{CH} = f_{SW}/21$ and $f_{CH} = f_{SW}/20$.

Fig. 15 shows the measured output spectrum when the amplifier delivers 1 W into the load, in which a THD of −109.1 dB is achieved. Fig. 16 shows the measured THD plus noise (THD+N). The prototype reaches a typical peak THD+N of −100 dB, and it can deliver a maximum of 13 W into an 8-Ω load at 10% THD. Fig. 17(a) plots the THD+N of a sample when the timing skew correction circuitry is intentionally bypassed and compares it with that during normal operation. As expected, timing skew correction significantly improves the linearity above 8 W. Fig. 17(b) compares the THD+N for $f_{CH} = f_{SW}/21$ and $f_{CH} = f_{SW}/20$, which is similar and agrees with the prediction of Fig. 6(b) for a small Δt.

Fig. 18 compares the output spectrum with the input shorted when chopping is turned on and off. Flicker noise is clearly suppressed by chopping, and the A-weighted integrated output noise is reduced from 43.7 to 32.7 μV.

Fig. 19 shows the measured power efficiency across output power. The prototype achieves a peak efficiency of 93%. The slight improvement from that reported in [14] is likely due to the improved thermal conductivity of the test assembly.

Table I summarizes the performance of this work and compares it with other state-of-the-art Class-D amplifiers with output power above 10 W. This work achieves >17 dB higher

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work	D. Schinkel [8] JSSC 2017	TAS6424 [11]	E. Cope [12] ISSCC 2018	S. Karmakar [13] ISSCC 2020
Input	Analog	Digital	Digital	Digital	Analog
Area (mm^2)	5	-	-	4.3	4.8
Supply (V)	14.4	25	14.4	8~20	14.4
f_{SW} (kHz)	2100	500	2100	400	2000
Quiescent Current (mA)	21	-	180	20.5	17
Idle Power (mW)	300	-	-	-	245
Output Power (W)	14	80	75	20	28
Efficiency	93%	>90%	86%	90%	91%
Peak THD+N @ 1kHz	0.001%	0.004%	0.02%	0.0013%	0.0008%
SNR (A-weighted)	108.7 dB	-	-	116 dB	-
DR (A-weighted)	110.2 dB	115 dB	-	115.5 dB	109 dB
PSRR (Frequency Range)	110 dB~79 dB (20 Hz~20 kHz)	88 dB~60 dB (100Hz~20kHz)	75 dB~57 dB (20 Hz~20 kHz)	80 dB~50 dB (20 Hz~20 kHz)	70 dB ~ 62 dB (20 Hz~20 kHz)
# Samples	8	-	-	-	-

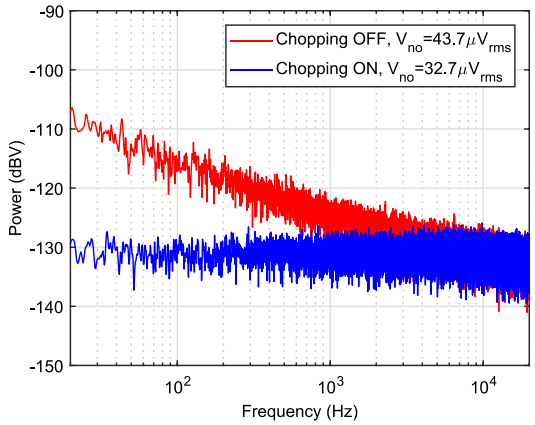

Fig. 18. Measured output spectrum with chopping ON and OFF when the input is shorted.

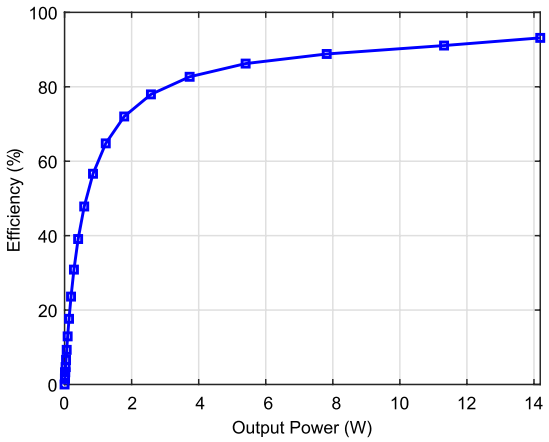

Fig. 19. Power efficiency across output power.

PSRR at both the low end and the high end of the audio band, due to the chopping technique. In the meantime, it achieves a competitive THD+N compared to [8], [11], [12]. Compared to [13], which is also an analog-input design with similar supply voltage and switching frequency, this works significantly improves the PSRR while achieving similar THD+N and dynamic range, at the expense of a slight increase in the idle power, consumed in the HV chopper.

VI. CONCLUSION

A 14.4-V Class-D amplifier using chopping to improve PSRR is presented. The timing of chopping and PWM is co-designed to avoid degrading PSRR and THD due to chopping-induced IM. An HV chopper design and timing skew correction circuits are applied to enable chopping in a 14.4-V amplifier. Measurement results of a 180-nm prototype show >17 dB of PSRR improvement across the entire audio band compared to prior works while achieving a competitive THD+N.

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