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DOI
10.1016/j.ijepes.2018.05.017

Publication date
2018

Document Version
Final published version

Published in
International Journal of Electrical Power and Energy Systems

Electrical Power and Energy Systems 103 (2018) 159–167

Contents lists available at ScienceDirect

Electrical Power and Energy Systems

journal homepage: www.elsevier.com/locate/ijepes

Development of HVDC system-level mechanical circuit breaker model

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ARTICLE INFO

Keywords:
HVDC mechanical circuit breaker
HVDC grid
Circuit breaker performance
Reclosing
PSCAD modelling

ABSTRACT

The main goal of the paper is the modelling of the mechanical direct current circuit breaker (DC CB) with active current injection that includes different circuit breaker characteristics. System level models provide adequate representation of the circuit breakers for system analysis studies. The performance characteristics of the DC CB in those proposed models replicate the ones of the devices in practice. The developed mechanical circuit breaker model is realized for a 320 kV demonstration circuit in PSCAD environment and its limitations and robustness are analyzed. The performance of the model is investigated by different cases. The obtained results show that the DC CB model can be used with full success for both to simulate DC fault interruptions and to be used for different protection studies.

1. Introduction

The growth of renewable energy resources significantly affects the topology of the future transmission systems. Significant progress has been made on the development of Voltage Source Converter (VSC) based HVDC grids in the last few years, which enable meshed HVDC grid to provide a promising technological solution for the connection of offshore wind farms. In order to utilize the potential of offshore resources, meshed networks are urgently needed. There have been several point-to-point VSC HVDC networks in operation, connecting offshore wind resource to mainland. Meshed HVDC offshore grids will provide additional flexibility, security and sustainability to the energy supplies. The development of meshed HVDC offshore grids is hindered by a few technical barriers. One of the main barriers is the lack of reliable, fast, low loss and cost effective HVDC circuit breakers, which can allow isolation of fault segments of the HVDC grid and keep the healthy areas operating continuously [1].

HVDC CBs development is different from that of AC CBs. HVDC CBs cannot interrupt DC faults because of the absence of a natural current zero. An artificial current zero is needed to be created by adding an active current injection circuit. Due to the absence of practical testing platform of HVDC circuit breakers [2], HVDC CBs transient are investigated by simulations performed within PSCAD environment.

Several mechanical DC circuit breaker prototypes have been proposed and developed by manufactures. The performance of these circuit breakers have been studied through system level modelling. The system level model must provide adequate representation of the circuit breaker for system analysis, as it will be implemented for large and multi-terminal grids. The key circuit breaker characteristics for these studies are the transient interruption voltage (TIV), maximum interruption current and the operating time.

Several mechanical DC circuit breaker models have been presented in the literature. The level of complexity of such models changes according to their applications. More simplistic models, like the one presented in [3–5], are conceived to be applied for system-level studies. Models proposed in [6,7] are used to understand the physical performance as well as the interactions and stresses between internal components.

The DC circuit breaker model presented in [5] consists of a series of modularized vacuum switches to achieve the required system voltage level. The layout of a single module consists of three parallel branches: the vacuum interrupter, the metal oxide arrester and a RC snubber. To achieve a high voltage DC interruption, the modules are placed in parallel with a commutation branch. In this model, a triggered sphere gap is adopted as a commutation switch to obtain bidirectional DC interruption. After the commutation process, an oscillating residual current can appear due to the low arc extinguishing capability of the triggered sphere gap. The residual current is usually interrupted by the back-up switches. The model is quite detailed, which takes into account most of the significant system-level features of the breaker. Nevertheless, a number of relevant aspects for system-level studies, such as the charging time for the secondary interruption operation and reclosing logic, are not included in the model.

In [4], an EMTP (electromagnetic transient program) based model of the mechanical DCCB for transmission applications is presented. The model includes the main hardware components (ideal switches with

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https://doi.org/10.1016/j.ijepes.2018.05.017
Received 26 January 2018; Received in revised form 15 March 2018; Accepted 13 May 2018
Available online 26 May 2018

delay, resonant circuit, surge arrester), the control logic and interlocks between sub-components, and self-protection feature in case of failure of the DC protection scheme. The model proved to be robust to a large range of operating conditions (DC fault clearing, reclosing operation, self-protection, reclosing into a DC fault). Despite being a valuable starting point for developing a system level model of the mechanical DCCB with active current injection, the model results too detailed for system-level studies and it is not compatible for RTDS applications as it would require a very fast time sample.

In [6,7], a vacuum circuit breaker was modelled in detail using electromagnetic transient simulation program (PSCAD). It including: (i) the nature of arcing time, (ii) current chopping ability, (iii) characteristic recovery dielectric strength between contacts during opening and (iv) quenching capability of high frequency current at zero crossing.

The main contribution of this paper is to propose a model of the mechanical circuit breaker (MCB) with an active current injection that replicates the breaker characteristics. The performance of the reclosing operation and bidirectional interruption are included. The influence of simulation time-step and robustness are also studied.

2. Design of mechanical DC CB

2.1. Model structure

The general structure of the mechanical HVDC circuit breaker with active current injection is given in Fig. 1 [3]. The breaker consists of three principal branches, namely, the main branch, the current injection branch, and the energy absorption branch. A high speed mechanical vacuum interrupter (S_1) and a residual breaker (S_2) make up the main branch; two switchable parallel resonant circuits which are comprised of inductor (L_p), capacitor ($C_{p\_a/b}$) and injection switch ($S_{3\_a/b}$) are the current injection branches; and a surge arrester (SA) is connected in parallel with the capacitors as the energy absorption branch. A DC current limiting reactor (L_{dc}) is connected in series with the S_2 to limit the rising rate of the fault current. The model has only one external trip signal: K_{grid}, which is a logic signal ($K_{grid} = 1$ is close; $K_{grid} = 0$ is open). The trip signal comes from the system relay and the DC CB acts accordingly. Moreover, the reclosing signal is supposed to arrive from the protective relay. The DC CB model is tested in the circuit with rated voltage of 320 kV and rated current of 16 kA based on [3]. Key components are listed in Table 1.

2.2. Mechanical circuit breaker components

2.2.1. High speed mechanical vacuum interrupter (S_1)

The main interrupter (S_1) contacts need to separate a sufficient distance to ensure adequate dielectric strength. For mechanical DC CBs, a high-speed electro-mechanical actuator can be used to reduce the actuation time. This actuator topology reduces the time delay

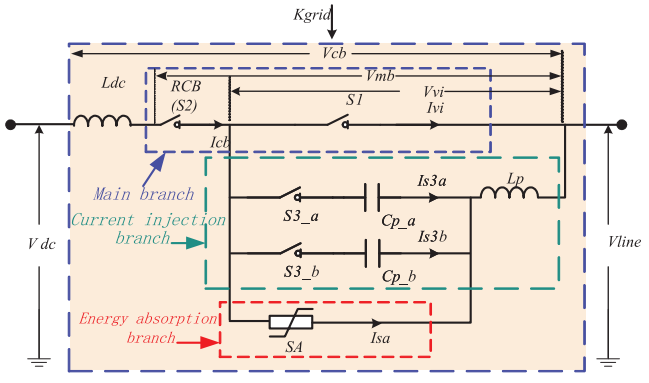

Fig. 1. General topology of the mechanical DC CB with current injection.

significantly. High speed operation of the interrupter contacts allows the resonant circuit to be operated faster, and to extinguish the arc in a shorter period of time. This configuration can allow the mechanical DC CB to withstand a counter voltage within approximately 8 ms from the trip order being given. The mechanical vacuum interrupter is modelled as a resistive switch, which closing state resistance is 0.1 mΩ and open state resistance is 1E10 Ω based upon [5]. The chopping current of vacuum interrupter with the contact material CuCr55 is obtained from [8], which is 0.01 kA as shown in Table 1.

2.2.2. Residual breaker (S_2)

The system inductance and circuit breaker capacitance results in an oscillation after current interruption. The residual current switch (S_2) clears this when a current zero is created. For the purpose of modelling, a same breaker model (as S_1) with a low chopping current (0.01 kA) is used.

2.2.3. Selection of L and C parameters

The capacitance and inductance in the resonant circuit and the precharge voltage affect the profile of the discharged current, in both magnitude and frequency (1) and (2). For the purpose of generating an artificial current zero, the amplitude of LC oscillation current (I_{LC}) should be higher than $K*I_{fault}$ (3), K is a safety margin ensuring successful interruption and DC CB reliability. The safety margin K in this paper is chosen as 2 based on [9].

$$I_{LC} = V_{c(0)}\sqrt{\frac{C_p}{L_p}}\sin(\omega t) \tag{1}$$

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{2}$$

$$I_{LC,max} = V_{c(0)}\sqrt{\frac{C_p}{L_p}} = K*I_{fault} \tag{3}$$

The balance of frequency, current magnitude and component sizes must be a traded-off against one another to optimize the circuit breaker functionality and cost. A higher frequency is desirable as it reduces the cost and the volume of the components in the resonant circuit. However, it also places additional stress on the vacuum interrupter (VI) in the form of a higher di/dt. This can make it challenging for the VI to interrupt successfully upon a current zero. The parameters are chosen as shown in Table 1 considering above factors.

2.2.4. Surge arrester

The voltage generated across the DCCB is governed by the characteristic of the surge arrester (SA) placed in parallel with the resonant circuit capacitors $C_{p\_a/b}$. When the circuit breaker commutates current from the resonant circuit into the SA, the voltage rapidly rises to a level determined by the SA characteristic. In practice, sufficient number of SA elements are added in parallel to absorb the required energy, which influences the clamping voltage of the DCCB. Fig. 2 represents the aggregated I-V curve for a number of parallel columns used with a clamping voltage of approximately 1.5 pu nominal dc voltage at 16 kA.

2.3. Principles of operation and time sequence

Fig. 3 illustrates the process of fault current interruption with a mechanical DCCB, relevant voltages in the circuit breaker and the switching states of the switches. V_{vi} is the voltage across the main interrupter (S_1). V_{mb} is the voltage across the main interrupter (S_1) and the residual current switch (S_2). U_{sys} is the system voltage whilst V_{cb} is the voltage across the inductor L_{dc}, residual current switch (S_2) and main interrupter (S_1). During fault current interruption, when the current (I_{cb}) rises to its peak value, high-speed making switch (S_3) closes and injects a counter current in the main interrupter (S_1) that eliminates the current in the main interrupter. At the same instant, S_1

Table 1
Main components of the mechanical breaker with current injection.

Variable	Default value	Variable	Default value
Capacitor pre-charge voltage	V_{dc} (320 kV)	I_{res3} (residual current for $S_{3\_a/b}$)	0.03 kA
Rated voltage (clamping voltage) of surge arrester SA	320 kV (480 kV)	T_{O12} (S_1, S_2 open mechanical delay)	8 ms
Capacitor $C_{p\_a/b}$	5 μF	T_{C12} (S_1 and S_2 close mechanical delay)	50 ms
Inductor L_p	500 μH	T_{O3} ($S_{3\_a/b}$ open mechanical delay)	30 ms
I_{res12} (residual current for S_1 and S_2)	0.01 kA	T_{C3} ($S_{3\_a/b}$ close mechanical delay)	8 ms

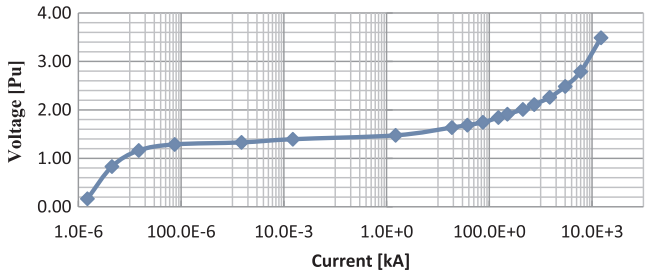

Fig. 2. Aggregated surge arrester current-voltage characteristics.

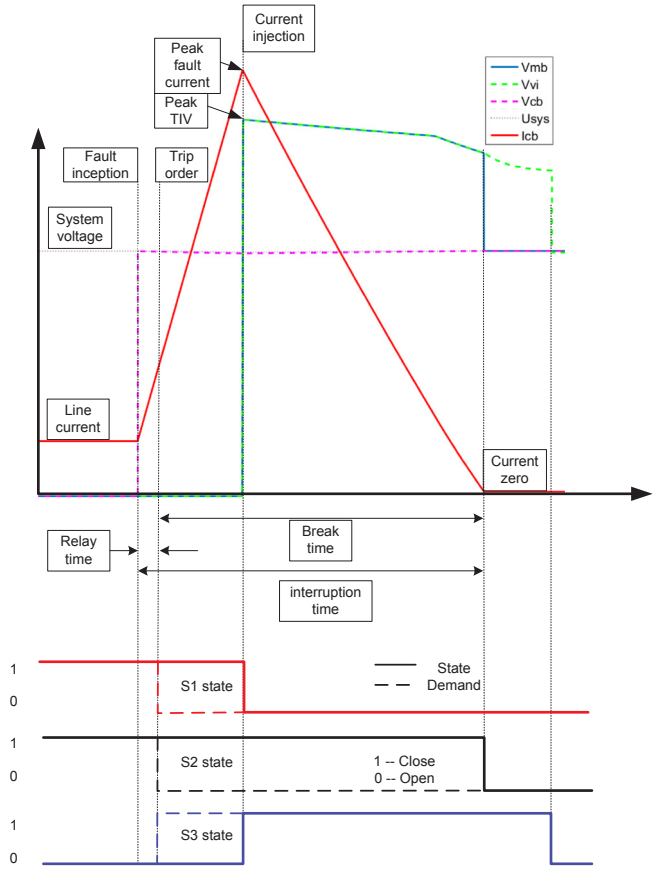

Fig. 3. Relevant voltages and a circuit breaker current as well as associated switching states of the switches S_1, S_2 and S_3 during fault current interruption.

changes its state from closed to open. Voltages V_{mb} and V_{vi} rise and reach their peak values. The current through the residual current switch (S_2) is absorbed by the surge arrester (SA) and gradually decreases toward zero. When the current reaches zero, the state of the residual current interrupter S_2 changes from closed to open. At that instant, the voltage V_{mb} drops to the value of the system voltage. The voltage across the main interrupter V_{vi} gradually decreases and at the instant when S_3 changes its state from closed to open, V_{vi} drops to the system voltage (see Tables 2–4).

3. Implementation of HVDC MCB model

The circuit used to test the validity of the model developed is shown in Fig. 4. The MCB is connected to an ideal DC supply and a resistive load through a cable. The value of the fault resistance R_f is variable. The parameters of the studied cable are shown in Fig. 5.

All possible cases are studied to validate the MCB model performance. Only some of the validation results are shown for brevity. Namely opening operation, bi-direction current interruption and repeated operation.

3.1. Opening operation

3.1.1. Rated current interruption

Fig. 6 shows the simulation results of the DC CB rated current interruption on receiving the system trip signal. Switch signal positions are shown in Fig. 6a, the top figure shows the trip command (K_{grid}) from the relay and the bottom figure shows the state of switches; circuit breaker currents are shown in Fig. 6b; circuit breaker and line voltage are shown in Fig. 6c, the voltage across S_1 and S_2 which is the V_{mb} in is shown in Fig. 1, the V_{mb} overlaps with V_{vi} before I_{cb} crosses zero. At the instant I_{cb} crosses zero, V_{mb} drop to system voltage. Meanwhile the V_{vi} maintains the same as the main interrupter is in parallel with the current injection branch, the V_{vi} drops to system voltage when S_{3_a} is open; and energy dissipation in Fig. 6d. Simulation results show that the breaker successfully interrupts 16 kA within 8 ms from the trip signal being applied. High-frequency oscillation is present due to the interaction between the line and series inductance. A current impulse (I_{s3}) is generated at trip +8 ms when the high-speed making switch (S_3) is closed, which forces a current zero in the main interrupter (I_{vi}). Subsequently, the current is then commutated into the energy absorption branch (I_{sa}), resulting in TIV (Transient Interruption Voltage) generation of approximately 500 kV. Thereafter the current decays, as energy is absorbed in the surge arresters.

3.1.2. Reverse current direction interruption

This case is used to demonstrate the reverse current interruption capability of the circuit breaker. Simulation results are shown in Fig. 7. To demonstrate this functionality, the breaker direction is reversed, so that fault current flows in the opposite direction. The DCCB experiences a pre-fault current of −2 kA. After the high-speed making switch (S_3) closes, a current is injected and superimposed on the line current. However, in this case, the current directions are the same, so the total current increases in the first half cycle. This causes a current peak in the order of 30 kA through the main interrupter (I_{vi}), as shown in Fig. 7b. The natural oscillation of the current injection circuit causes a current zero half a cycle later. At this point, the breaker interrupts the fault current in the typical manner; commutating the current in the surge arrester. However, counter-voltage (TIV) generation is of the opposite

Table 2
Interruption sequence of mechanical circuit breaker with current injection.

Time	Definition and Operation	Default Value
Fault inception	Current and voltage wave fronts arrive at the circuit breaker location: ● DC side voltage starts to decay and current increase.	0 ms
Relay time	Time required for fault detection and discrimination: ● Breaker receives trip signal sent from relay	2 ms
Break time	Delays associated with physical movement of circuit breaker components. At the end of the period: ● Switch S_1 has opened; ● Switch S_3 has closed; ● A current zero is generated in S_1 from the resonant circuit; ● Capacitor voltage rises until the SA clamping voltage is reached. Current is then commutated into the SA; ● Circuit breaker voltage (V_{CB}) is equal to clamping voltage	8 ms
Fault interruption time	Combination of relay time and breaker operation time: ● Breaker has been tripped; ● Current zero and counter voltage generated.	10 ms
Fault current suppression time	Time for stored magnetic energy to be dissipated in the SA: ● The time is determined by the system configuration. For example, cable length, SA characteristic	–
Residual current switch open	Residual switch (S_2) opens ● Current has reached leakage level (several mA), determined by the SA V-I characteristic; ● Residual current is removed by S_2	–

Table 3
Test circuit parameters.

Parameter	Value
Vdc	320 kV
Rdc	0.1 Ω
Ldc	220 mH
DC cable 1	10 km distributed parameter model
DC cable 2	100 km distributed parameter model
Rf (low impedance)	0.01 Ω
Rf (high impedance)	50 Ω
Rload (rated load)	320 Ω
Rload (low load)	500 Ω

Table 4
Repeated Operation upon External Trip Simulation Conditions (Mechanical Breaker).

Parameter		Value	
Fault impedance	R_f	0.1	[Ω]
Fault time	T_f	0.1	[s]
Trip Time (1st)	T_{trip1}	0.102	[s]
Close Time	T_{close}	0.05	[s]
Dead Time	T_{dead}	250	[ms]
Trip Time (2nd)	T_{trip2}	$=T_{trip1}+T_{dead}+T_{close}+2$ ms	
DC Inductance	L_{dc}	220	[mH]

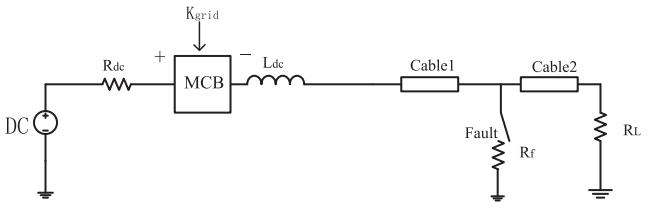

Fig. 4. DC MCB verification circuit.

polarity.

A half-cycle delay results in a slightly longer period between trip-order until TIV is generated. However, due to the high-frequency nature of the current injection circuit, this period is very short and it is in the order of < 100 μs. In this short period the line current can rise marginally. However, current margin is built into the design of the breaker to ensure several current zeroes can be achieved across all cases, ensuring interruption success.

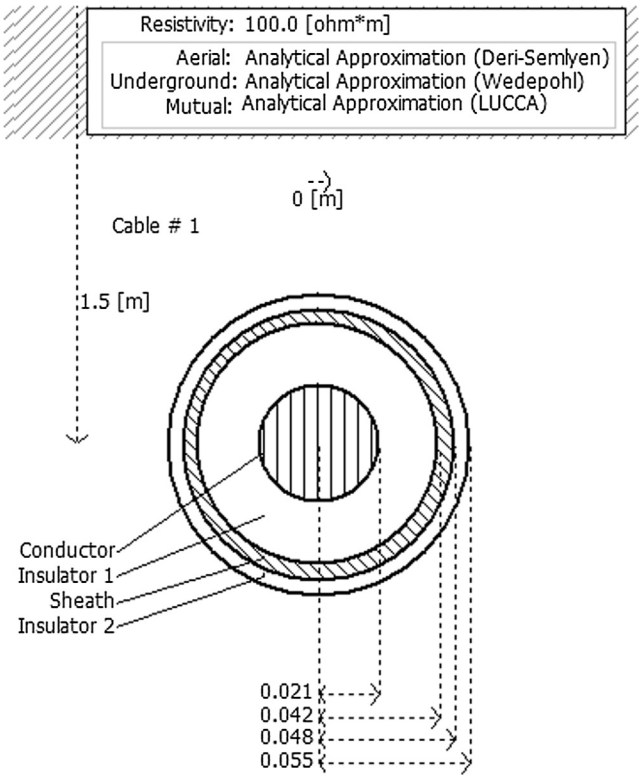

Fig. 5. Dimension of studied cable.

3.2. Repeated interruption operation

To enable multiple opening operations in rapid succession, a secondary current injection circuit is used, as shown in Fig. 1. The time sequence is shown in Fig. 8. DCCB model parameters can be found in Table 1. After the first operation, the second branch is used to inject counter-current through the main interrupter after receiving a second trip signal.

The DC CB operation flow chart is shown in Fig. 9, the DC CB initial state can be set at the beginning of simulation. When the CB initial state is set as closed, then S_1 and S_2 is closed while $S_{3\_a/b}$ is open. On the other hand, when CB initial state is set as open, then S_1, S_2, $S_{3\_a/b}$ is open. N_{op} is the number of operations, the initial value of N_{op} is set to 0.

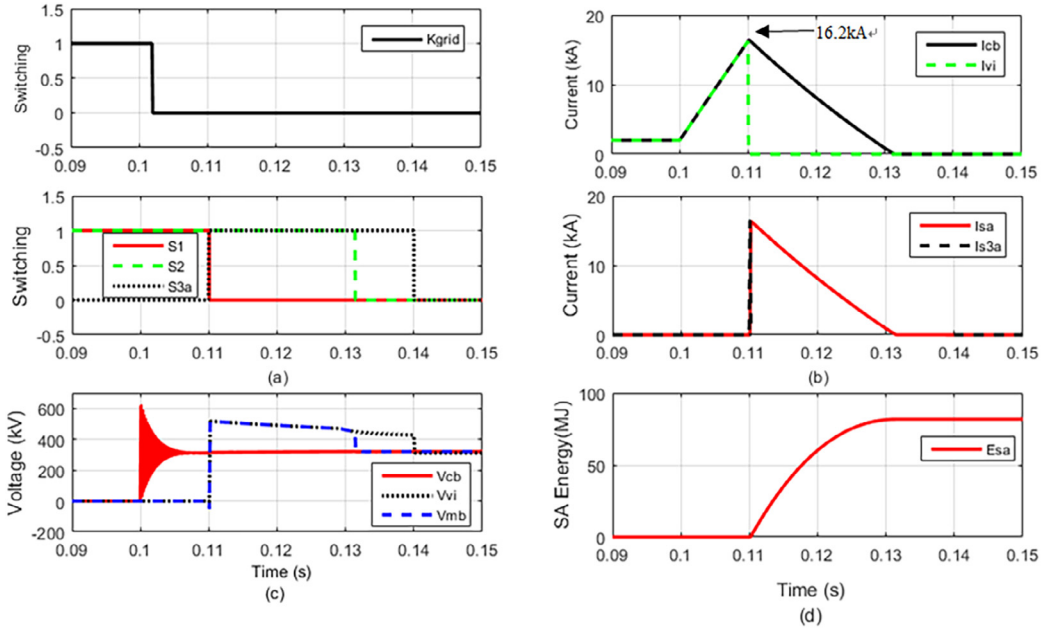

Fig. 6. Rated Current Interruption on External Order (Mechanical DC CB) based on PSCAD.

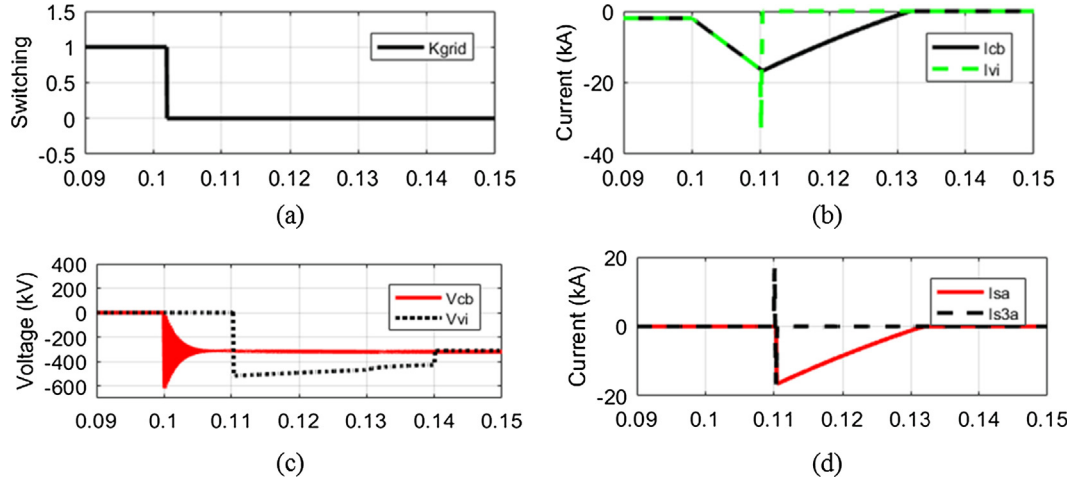

Fig. 7. DC CB Reverse high current interruption performance on receiving grid order.

Users can set the initial state of CB (open/close) at the beginning. When the CB is in open state, it will closed as soon as it receives a close signal. During the closing operation, open trip signal cannot interrupt the operation. After the close operation the CB is closed and it will not open until CB receive an open trip signal. After the opening operation, the CB is opened and $N'_{op} = N_{op} + 1$. If N_{op} is less than 2 then CB can still wait for close signal and perform closing operation. Otherwise, the CB remains open and it cannot operate any longer until the CB is reset by the user.

3.2.1. *Repeated open-close cycle operation with dead time 250 ms*

The dead time T_{dead} is the period between the first trip signal and the closing signal, during this period the DC CB do not respond to any other trip signals. The dead time is assumed to be 250 ms as shown in Fig. 8. The close time T_{close} is the time from DC CB receives a closing signal to it turns to the closed state, it is 50 ms as shown in Fig. 8.

The simulation results are shown in Fig. 10. The simulation starts with rated line current at 2 kA. And the fault occurs at $T_f = 0.1$ s, 2 ms later the first trip signal is sent to the DC CB at $T_{trip1} = 0.102$ s. After the first trip order, the breaker opens and performs the first current interruption (16 kA). The reclosing signal is sent to the DC CB 250 ms after the first trip, and the breaker reconnects the source to the line after 50 ms. As the fault is not cleared from the system, fault current rises as soon as the breaker is closed. The second trip signal is sent to the DC CB 2 ms after the breaker is closed, and then performs the second current interruption. Then the DC CB remains open to insulate the fault. For the first operation, the first current injection circuit (C_{p_a}, S_{3_a} and SA) is used. For the second operation, current injection circuit elements C_{p_b},

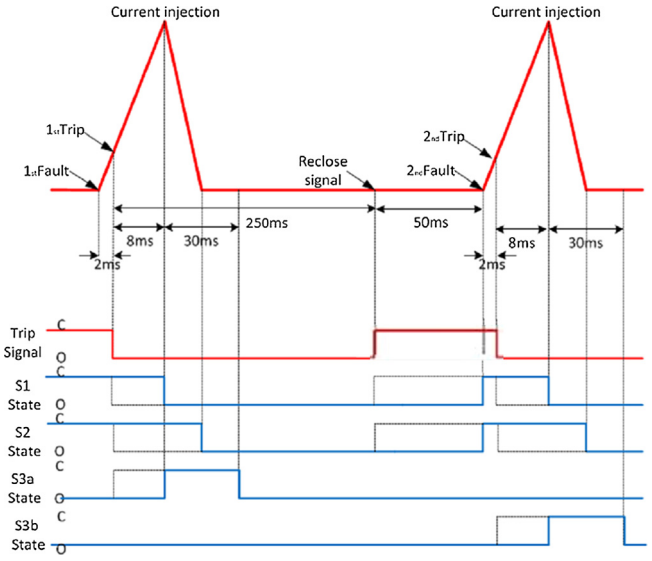

Fig. 8. Sequence of repeat operation Mechanical DC CB.

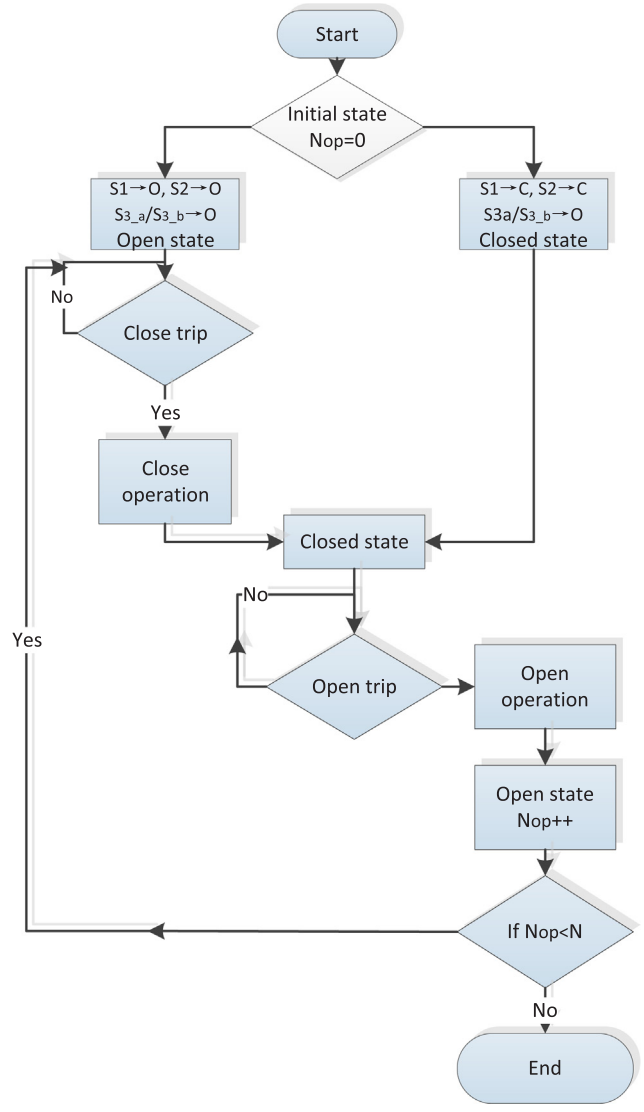

Fig. 9. Flow chart of DC CB control sequence.

S_{3_b} and SA are utilized. We have to point out that the reclosing delay is an external parameter following from the relay and does not depend on the DCCB; The reclosing timer starts at a relay trip instant and should take into account the longest interruption time that comes from the system studies (worst case scenario). As such, the study case in this chapter considers reclosing delay of 250 ms corresponding to existing AC relays, as we do not know how the DC protection will behave. Anyhow, the reclosing delay is an external user-defined parameter and the user can run study cases with different reclosing delays based on his wish and relay algorithm. It is important to point out that the closing time (T_{close}) is fixed and for the DCCB is 50 ms.

3.2.2. Repeated open-close cycle operation with dead time 100 ms

It has to be pointed out that the repeated operation trip signal are sent by system relay. As the total time of interruption and closing is in the order of several tens milliseconds, the dead time should be longer than the total time to ensure the successful interruption. The minimum dead time is set at least 100 ms here. As shown in Fig. 11, the dead time is user defined and the DC CB can successfully interrupt the fault twice with the dead time of 100 ms.

In the case considered, the fault is assumed to be permanent and thus current rises again. A two millisecond period is assumed for the relay detection, after which the breaker is tripped for a second time. As the initial current of second interruption is zero, after 2 ms relay delay time and 8 ms operation time the second fault current peak is less than that of the first interruption. Furthermore, the different current interruption peak leads to the different spikes stress on the vacuum interrupter. Fig. 12 shows the difference of the spikes. The peak value of the first fault current is higher than the peak value of the second fault, the first spike voltage is lower than the second one. Moreover, a zoom in figure is used to show the variation of V_{cb} during the second close and open operation. More details will be discussed in Section 4.

4. Discussion

4.1. Model demonstration responses with different L_{dc}

This scenario demonstrates DC CB model responses with different L_{dc} values. For a given DC CB, different L_{dc} can be used to adjust different protection strategies and grid topology changes at all times.

4.1.1. Comparison of Icb with different L_{dc}

Fig. 13, a short circuit fault current occurs at 0.1 s, the fault current begins to rise and the rising rate is $\frac{V_{DC}}{L}$. The trip signal is sent 2 ms after the fault inception. As soon as DC CB receives the trip signal, the contacts begin to separate. 8 ms later the fault current reaches the peak value which is (4), at this instant the high speed making switch is closed and counter current is injected. The arc in vacuum interrupter is extinguished and Vvi rises quickly, when Vvi reaches the clamping voltage of SA, the current commutates to energy absorption branch and begins to decrease. At this moment, the equivalent circuit can be seen as a DC source connect in series with Ldc and SA, the voltage equation is (5). Then the decrease rate of I_{cb} is (6). The current during the energy absorption period can be calculated as (7). The peak value of the fault current and absorption time are listed in Table 5.

$$I_{fpk} = I_{dcN} + \frac{V_{DC}}{L}(T_{trip} + T_{ope}) \tag{4}$$

$$V_{DC} = L\frac{di_{(t)}}{dt} + V_{SA} \tag{5}$$

$$S = \frac{di_{(t)}}{dt} = \frac{V_{DC} - V_{SA}}{L} \tag{6}$$

$$I(t) = I_{fpk} + \int_{t_{inj}}^{t} S\,dt \tag{7}$$

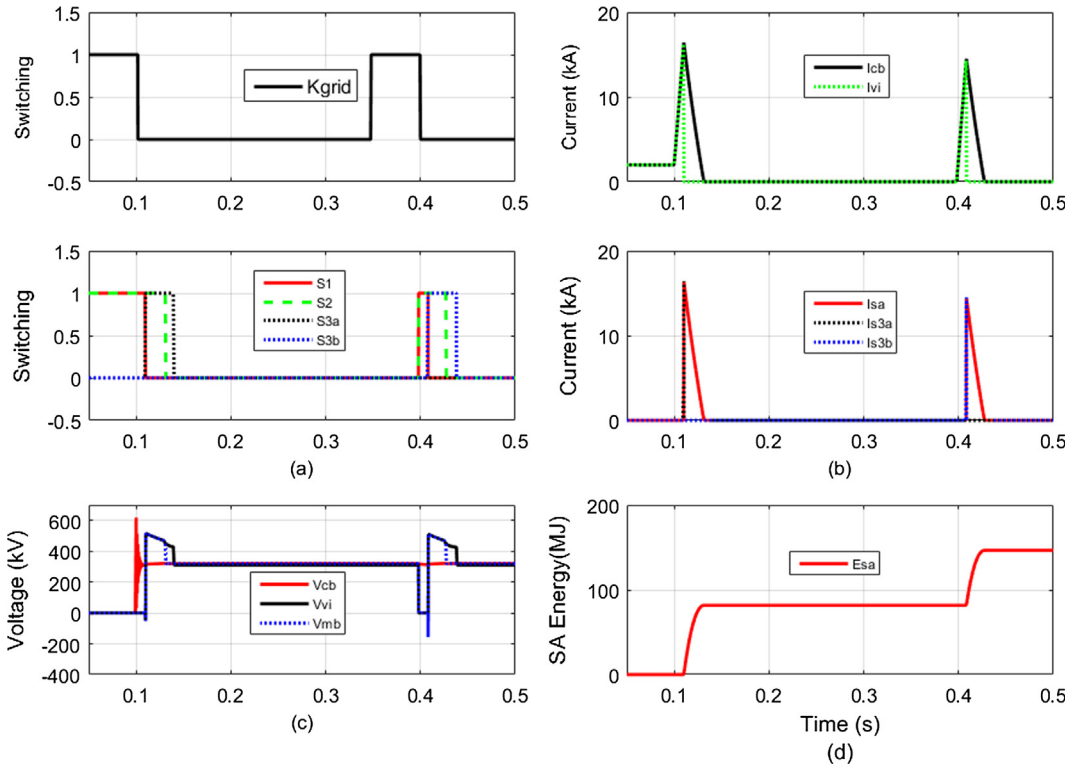

Fig. 10. Repeated open-close cycle operation with dead time 250 ms.

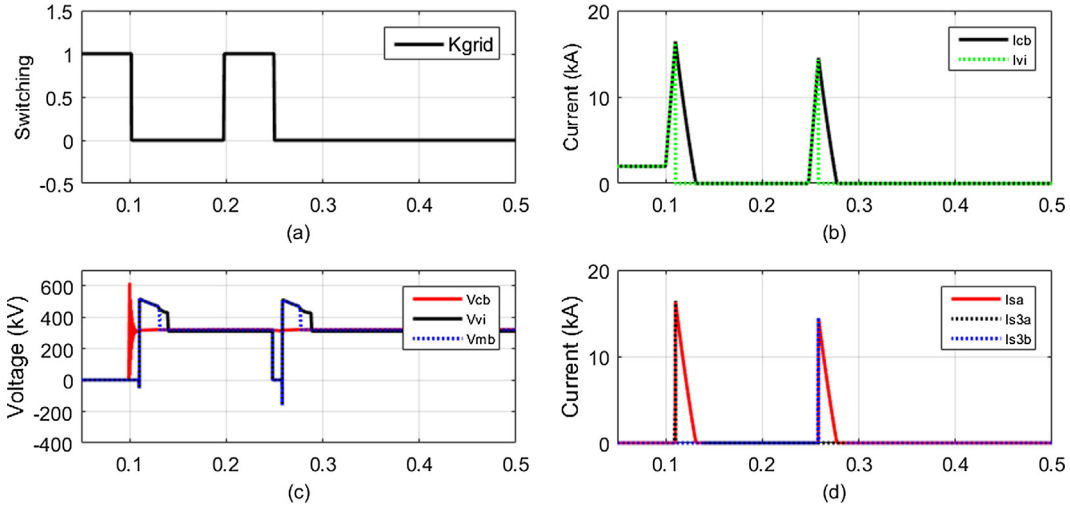

Fig. 11. Repeated open-close cycle operation with dead time 100 ms.

At the intersection point where $I_{L1}(t) = I_{L2}(t)$, combine Eqs. (4)–(7). During the energy absorption procedure, V_{SA} is approximately the SA clamping voltage, which is 1.6–1.5 times V_{DC}. As a result, at the instant t after the current injection time, current curve with different Ldc will have an intersection point.

$$t = \frac{V_{DC}}{V_{SA} - V_{DC}}(T_{trip} + T_{ope}) \tag{8}$$

As the clamping voltage in the model is 524 kV, which is 1.647 V_{dcN}, then the intersection time should be $t = [1/(1.647 - 1)] * (2 + 8) = 15.46$ ms. From Fig. 12, one can see that point X is 125.5 ms, while the time instant when the injection takes place is 110 ms. This energy absorption period is 125.5–110 = 15.5 ms, which verifies that (8) is correct.

Moreover, the energy absorption time t_{abs} can be estimated according to (9).

$$t_{abs} = \frac{I_{dcN}L + V_{DC}(T_{trip} + T_{ope})}{V_{SA} - V_{DC}} \tag{9}$$

4.1.2. Comparison of E_{SA} with different L_{dc}

The energy dissipated in SA varies with the different L_{dc}. As the inductance of the cable is far less than that of L_{dc} in this demonstration, the energy stored in the cable are neglected. However, in the simple verification circuit shown in Fig. 4, the inductance of cables is far lower than that of current limiter Ldc. As a result, when we approximately estimate the energy absorbed by SA, the energy in the cable can be neglected. Meanwhile, the results shown in Fig. 14 take into

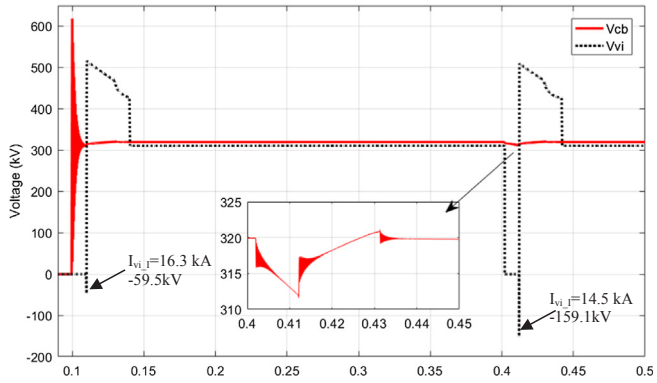

Fig. 12. V_{cb} variation during second close- open based on PSCAD.

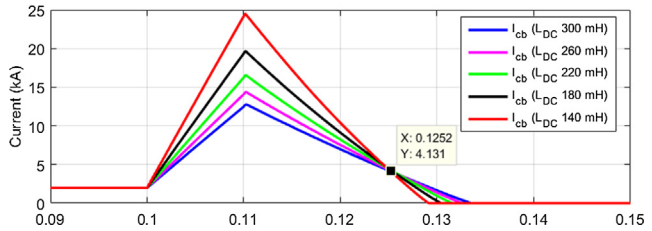

Fig. 13. Comparison of Icb with different L_{dc}.

Table 5
Fault current peak and absorption time.

L_{dc} (mH)	300	260	220	180	140
I_{fpk} (kA)	12.8	14.3	16.3	19.7	24.4
t_{abs} (ms)	23.4	22.5	21.5	20.3	19.1
E_{SA} (MJ)	69.0	74.8	82.4	93.2	109.8

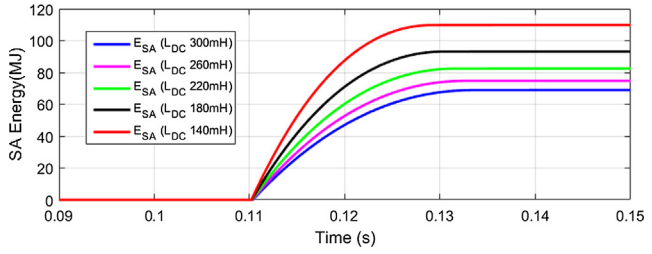

Fig. 14. Comparison of E_{SA} with different Ldc.

consideration the energy stored in the cable as well.

It has to be pointed out that the energy absorption of the surge arrester in present case, corresponds only to this studied circuit configuration, and in practice the results depend on actual circuit topology. The simulation results are shown in Table 5. The energy absorption can also be simply verified by $\frac{1}{2} I_{fpk} V_{clamp} t_{abs}$. For instance, for the case when L_{dc} is 220 mH, the energy is 84 MJ which close to the actual value computed by (10)

$$E_{SA} = \int_{t_{inj}}^{t} V_{SA} * I_{SA} dt \tag{10}$$

4.1.3. Comparison of TIV with different L_{dc}

At the instant of current zero, the TIV is generated across the main interrupter. The main interrupter is subjected to severe stress by the TIV. Different L_{dc} leads to the different interruption current, and the different interruption current result in different stress (TIV) on main vacuum interrupter (see Fig. 15). At the moment of injection, the vacuum interrupter turns to an open circuit and is connected in parallel with the capacitor. The voltage across the capacitor can be determined by (11). The peak value of LC oscillation current is (12). $I_{vi,I}$ is the interrupted current. The time period for current reach zero t_I can be estimated by (13). By solving these three equations the relationship between $I_{vi,I}$ and V_{c_I} can be established. As we can see, the higher the interrupted current is, the lower the TIV spike stresses vacuum interrupter.

$$V_{c_I} = \cos(\omega t_I) \tag{11}$$

$$I_{c,p} = U_{dc} \sqrt{C/L} \tag{12}$$

$$t_I = \sin^{-1}(I_{vi,I}/I_{c,p}) \tag{13}$$

4.2. Wrong trip signal

4.2.1. Superfluous trip signal

When the DC CB is under operating, the DC CB cannot respond to any new trip signal. As a result, the control should be blocked to any trip sent to the DC CB. Especially in repeated operation scenarios, the open and close signals are sent in sequence. If the DC CB responds to a new trip before the last operation is finished, the DC CB may get stuck and cannot react to a new trip. A dead time becomes essential in the logic control, as soon as the DC CB receives a trip signal, the control will block any other new trips until the end of the dead time. The dead time is the period between the system relay sends the first trip signal and the next closing signal, during which time the fault interruption is proceed. The dead time should be longer than the open/close operation time, which will ensure the reliability of the DC CB. The model can ignore wrong trip and react to the new trip signals in this way. The default value of dead time is 250 ms and the minimum dead time is 100 ms, and both scenarios are demonstrated in Section 3.2. Regarding the different dead time, we can point out that it shows the robustness of the model that can be used for protection studies. The dead time is defined by the protection algorithm.

4.2.2. Delayed trip signal

An unwanted case that deserve attention is the case when the DC CB receives a delayed trip command given from the protection system (relay failure). When a fault occurs at some instant, the fault current begins to rise. System protection is supposed to detect the fault and to send a trip signal within 2 ms. A possible relay failure may result in not sending a trip signal or sending a delayed trip signal. During the delayed period, the fault current is beyond the maximum interruption capability of CB. To demonstrate this character, the safety margin factor K is set as 1, and the capacitance and the inductance of resonant circuit is chosen as 3 μF and 1100 μH, respectively. In practice, the safety margin factor K is always selected to be greater than 1 in order to provide some margin, and in other demonstration cases the K is 2 based upon [9]. In case of a delayed trip signal, the CB operates as soon as it receives a trip signal. After 8 ms operation time, S_1 and S_2 switches open and the high-speed making switch (S_3) closes. The commutation current is injected and superimposed to the fault current. As shown in Fig. 16, no current zero is generated and arc cannot be extinguished by the main interrupter (S_1). As a result, the state of S_1 and S_2 remain closed. The high-speed making switch (S_3) opens 30 ms after it is closed, and the commutation current is interrupted. Then the voltage that remains on the commutation capacitor is determined by the capacitor oscillation voltage at the instant when the commutation current crosses zero. The fault current is still present in the system and continuous to rise. In such case, there should be a backup protection available that will clear the fault. The backup protection is beyond the scope of this paper and will not considered here. The results are given in Fig. 16.

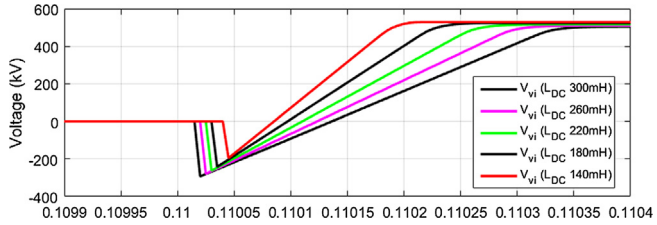

Fig. 15. Comparison of TIV with different L_{dc}.

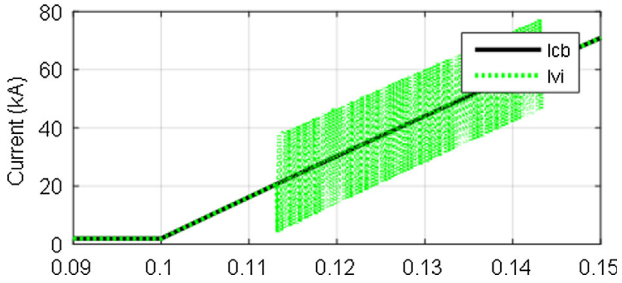

Fig. 16. Current interruption with delayed trip signal.

5. Conclusion

The paper presents a robust model that is capable of simulating different system conditions. The DC CB model with active current injection uses a generic representative structure that replicates the performance characteristics for system studies.

And it replicates the CB characteristics for system analysis studies and is illustrated on a 320 kV demonstration system with 16 kA interrupting current. The DC CB is modelled on PSCAD including DC CB controller for opening operation, bi-direction current interruption and repeated operation.

The studies show that there is an important trade-off between the L and C parameters selection.

It is considered the repeated operations in a short period, a secondary current injection circuit is used and the relevant control logic and sequence are designed. The dead time is defined ensuring the reliability of DC CB.

Meanwhile, the negative spike on main vacuum interrupter during operation are studied, and accurate evaluation of TIV spike is given. It indicates that the higher the interrupted current is, the lower the TIV spike stresses vacuum interrupter.

Furthermore, this generic model can be reproduced in different cad software and the control sequence can be transferred. Especially in repeated interruptions in a short period, the secondary LC branch as well as its control logic becomes essential. The model can be updated by taking into account parasitic elements, etc.

Acknowledgement

The author gratefully acknowledge the financial support from the funding from the European Union's Horizon 2020 research and innovation program under grant agreement No 691714.

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