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25.4 A 5GS/s 360MHz-BW 68dB-DR Continuous-Time 1-1-1 Filtering MASH ΔΣ ADC in 40nm CMOS

Qilong Liu[1,2], Lucien Breems[1,2], Chenming Zhang[1,2], Shagun Bajoria[1,2], Muhammed Bolatkale[2,3], Robert Rutten[2], Georgi Radulov[1]

[1]Eindhoven University of Technology, Eindhoven, The Netherlands
[2]NXP Semiconductors, Eindhoven, The Netherlands
[3]Delft University of Technology, Delft, The Netherlands

In the pursuit of ever larger bandwidths, in recent years GHz-rate continuous-time (CT) oversampled ADCs have been reported in literature that achieve bandwidths of hundreds of MHz and have even exceeded the GHz barrier [1-3]. As impressive as these bandwidths are for CT ADCs, the required ADC architectures are complex, are sensitive to layout parasitics due to the high sampling rates, and most important of all, are power hungry, consuming several hundreds of mW. In this paper, we propose a filtering multi-stage noise-shaping (MASH) ΔΣ ADC architecture that overcomes the abovementioned drawbacks. Passive delay compensating filters [4] are used to realize broadband and deep suppression of the input signal component at the internal filter nodes of the ADC. As a result, no interstage DACs are needed, which are commonly required to generate the quantization error replicas in a MASH ΔΣ ADC, saving substantial power and greatly reducing the parasitic load of the high-speed critical nodes. Moreover, because of the absence of signal content at the internal filter nodes, the backend stages of the MASH architecture have relaxed linearity requirements and can be implemented with simple low-power G_m-C filters. Precise excess loop delay and excess phase compensation are accomplished with a partly resistive and capacitive stabilization DAC, enabling very-high-speed operation of the ΔΣ loops. The realized MASH ADC is sampled at 5GHz and achieves 68dB/65dB DR/peak SNDR over a 360MHz bandwidth, -78dBc THD at -1dBFS for a 115MHz input signal, and consumes 158mW. Implemented in a mature 40nm CMOS technology, the ADC occupies only 0.21mm^2 core area, achieves 2× lower power, 5dB higher Schreier FOM and 2× lower Walden FOM compared to state-of-the-art broadband CT ADCs in advanced 16nm-28nm nodes [1-3].

Figure 25.4.1 shows the architecture of the CT 1-1-1 filtering MASH ADC. The ADC consists of three 1st-order stages and achieves 75dB SQNR in 360MHz at a 5GHz sampling rate. Stage 1 is implemented as a first-order modulator and consists of an active-RC integrator, a 3b flash ADC (ADC1), a main feedback DAC (DAC1), and a stabilization DAC2 that compensates for the excess loop delay (ELD) and excess phase shift. The output of the integrator is directly coupled to the input of stage 2. Stage 2 consists of a G_m-C filter, a 3b flash ADC (ADC2) and a combined main/ELD DAC (DAC3). The output current of DAC3 of stage 2 is scaled down with respect to G_{m2} to provide an interstage gain (IG2) of 3×. A two-path G_m×R residue amplifier (RA) extracts the quantization error of stage 2 that is directly connected to the input of stage 3 without the need for an interstage DAC. Stage 3 is a replica of stage 2 and also employs an interstage gain of 3×. The digital outputs of all stages (OUT1, OUT2, OUT3) are fed to off-chip digital noise cancellation filters (DNCF1, DNCF2, DNCF3) for further processing. DNCF1 is implemented as a fixed delay (z^{-n}) without any filtering, and DNCF2 and DNCF3 are implemented as 12-tap programmable FIR filters. The DNCF coefficients are calibrated using an off-chip frequency-domain least-square algorithm [5] during start-up of the chip.

Figure 25.4.2 illustrates the implementation of the proposed stage 1 of the CT MASH ΔΣ ADC. The loop filter consists of a single RC integrator R_S/C_{INT}. The integrator output V1 is connected to the input node (Vsum) of a 3b quantizer (ADC1) via summing resistor R_{LF}. The quantizer input gate load and routing capacitance are modeled with C_P that forms an undesired pole at ~4GHz with R_{LF}. The quantizer has 1 clock period latency and its output is connected to a current steering main DAC (DAC1) and a passive R//C DAC (DAC2), which is directly connected to the summing node Vsum. The main loop formed by DAC1-RC integrator-summing pole R_{LF}/C_P-quantizer delay is stabilized by the compensation DAC (DAC2). DAC2 comprises a resistive part (RDAC2) that forms the low-frequency compensation loop, and a capacitive part (CDAC2) to realize the high-speed first-order loop. This way, the complete ΔΣ loop is stabilized and can be mapped to a nearly perfect 1st-order NTF while operating at a very high sampling frequency.

To replicate the quantization error that is fed to the subsequent stage in a MASH ADC, the input of the quantizer Vsum and the output of the quantizer are commonly subtracted with an additional interstage DAC [1], removing the input signal component (IN) from Vsum. The interstage DAC is power hungry and significantly increases capacitive loading of the high-speed ELD compensation loop, severely limiting the maximum possible sampling frequency. In [5], the loop filter output (V1) is used to replicate the quantizer error, instead of the quantizer input (Vsum). The signal component in V1 is suppressed by adding a signal feedforward path to V1. Consequently, node V1 can be directly connected to the next stage without the need of the interstage DAC. The technique in [5] gives a narrowband suppression of the signal component, which is very suitable for audio applications, but does not provide a wideband solution. In [4], all-pass filters (APFs) are introduced in both the input and the feedforward path of a ΔΣ modulator to create wideband suppression of the signal component at all nodes of the loop filter, to relax linearity requirements of the filter stages. In this paper, the filtering of [4] and interstage connection of [5] are combined to realize a wideband MASH ADC without the need of interstage DACs. The APF is implemented as a cross-coupled R-RC branch [4] and the low-pass filter (LPF) is a passive T-network that implements both the direct and delayed signal feedforward paths. The division factor (k) in LPF is chosen to be asymmetric (0.2) in order to reduce the loading of C_{FF} on Vsum. LPF resistor R_{FF} is matched with RDAC2 for good signal suppression. The input signal suppression at V1 is more than 30dB within the signal band. DAC2 is driven by a pass-gate latch (L1) in order to provide well-defined timing with the minimum clk-to-Q delay. L1 is clocked with CLK_{ADC1} but uses its rising edge to latch ADC1 output and drive DAC2. ADC1 consists of 7 unit comparators and a 7-tap resistive ladder. Each comparator has a preamplifier, a regeneration core and a dynamic latch (not shown).

Figure 25.4.3 shows the schematic implementation of stage 2 of the CT MASH ADC. The G_m cell (G_{m2}) is implemented as a resistively-degenerated folded-cascode amplifier (R_{DG}, M1-M6). The parasitic pole inside the G_m cell (at Vxp and Vxn) is outside the feedback loop of stage 2 and helps to filter high-frequency quantization errors without compromising the loop stability. The biasing current (Ibp) of the folded-cascode amplifier is reused by the current-steering DAC (IDAC3). A common-mode feedback circuit (CMFB) senses the common-mode voltage of V2p and V2n and compares it with an external voltage reference (Vcm2). All biasing current sources IG_m, Ibp and $IDAC3_u$ use cascoding. IG_m and Ibp have constant-G_m biasing, and $IDAC3_u$ has 1/R biasing. Ibp is implemented using thick-oxide transistor Mp and thin-oxide cascode transistor Mpc, and is supplied with 1.8V. ADC2 (as well as ADC3) is implemented similarly as ADC1. A capacitive DAC (CDAC3) is implemented to compensate for the excess loop delay [6]. The latch L3 that drives $CDAC3_u$ uses the same structure as L1 in Fig. 25.4.2. The latch L2 is a clocked S-R latch that drives the switching pair M7, M8 with a high crossing point (1V) to minimize the glitches at Vt.

The CT 1-1-1 MASH ΔΣ modulator is fabricated in a 40nm CMOS process and the core occupies 0.21mm^2 including modulator, clocking, 1/R biasing and constant-G_m biasing (Fig. 25.4.7). Figure 25.4.4 shows the measured single-tone output spectrum (RBW 89kHz) with a 980mV peak differential (-1dBFS) input signal at 115MHz. The measured THD is -78dBc, which is limited by second order distortion. Figure 25.4.5 shows the measured SNR/SNDR versus input amplitude of 115MHz input signal. The dynamic range is 68dB and the peak SNDR is 65dB at -1dBFS input in 360MHz bandwidth. The measured signal transfer function (STF) does not exhibit peaking up to 2GHz. The ADC (including modulator, clocking and biasing) consumes 158mW from 1.8V/1.1V/1V supplies. Stage1 consumes 78mW, stages 2 and 3 combined consume 44mW and the clocking and other auxiliary circuits consume 36mW. The measured performance is summarized and compared to the state-of-the-art CT ADCs with BW greater than 250MHz in Fig. 25.4.6. Thanks to the filtering MASH architecture achieving wideband signal suppression without interstage DACs, the designs of the substages and interstage connections of the MASH ADC are greatly simplified, resulting in a core area of 0.21mm^2, a 5dB better Schreier FoM and 2× lower Walden FoM when compared to state-of-the-art CT ADCs in more advanced technology nodes.

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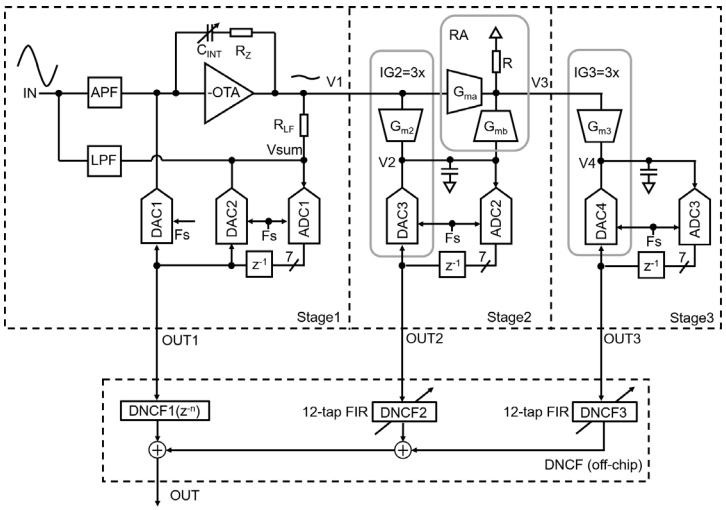

Figure 25.4.1: CT 1-1-1 filtering MASH ADC architecture (drawn single ended).

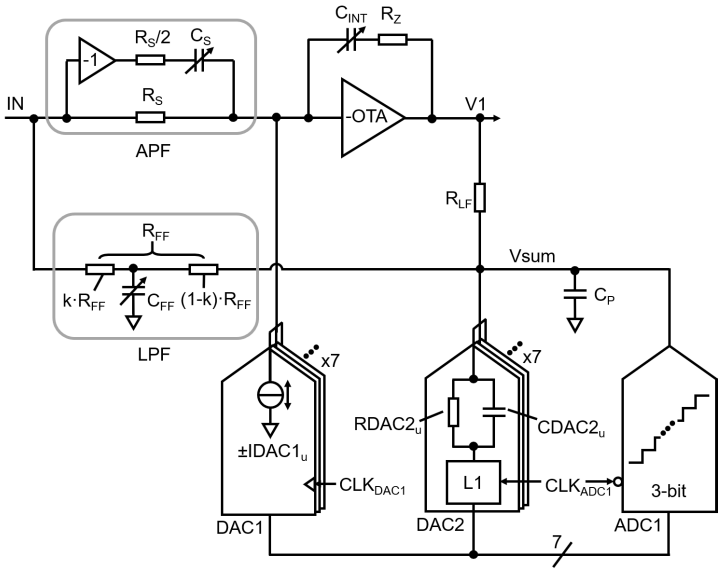

Figure 25.4.2: Block diagram of stage 1 of the CT MASH ADC.

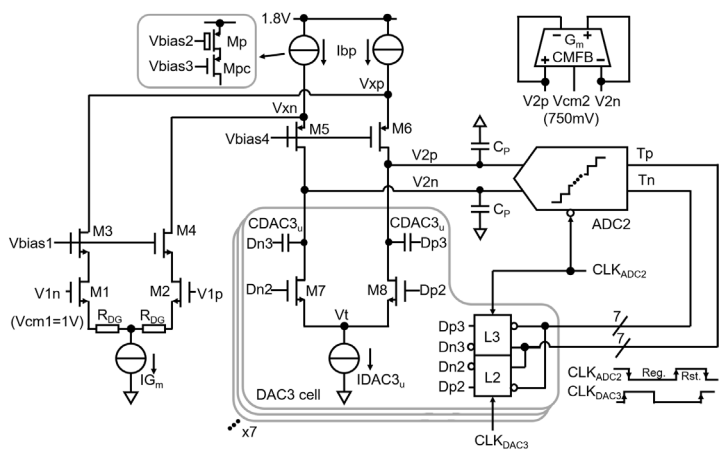

Figure 25.4.3: Schematics of G_{m2} and DAC3 in the second stage of the CT MASH ADC.

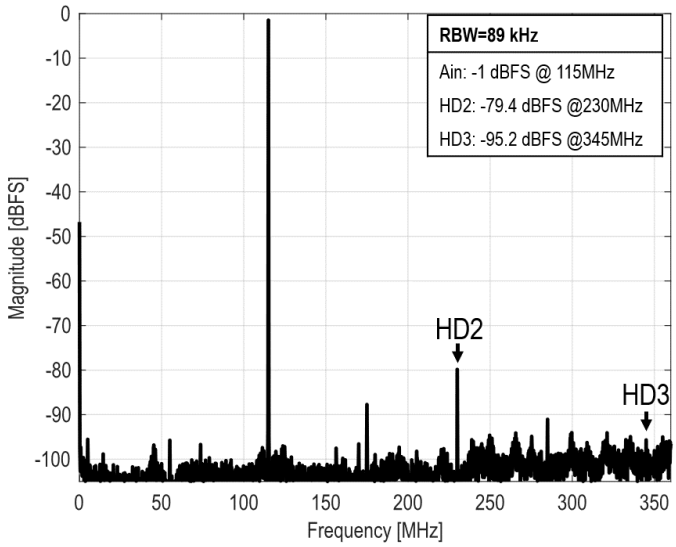

Figure 25.4.4: Measured output spectrum with a single-tone at 115MHz (DC-360MHz).

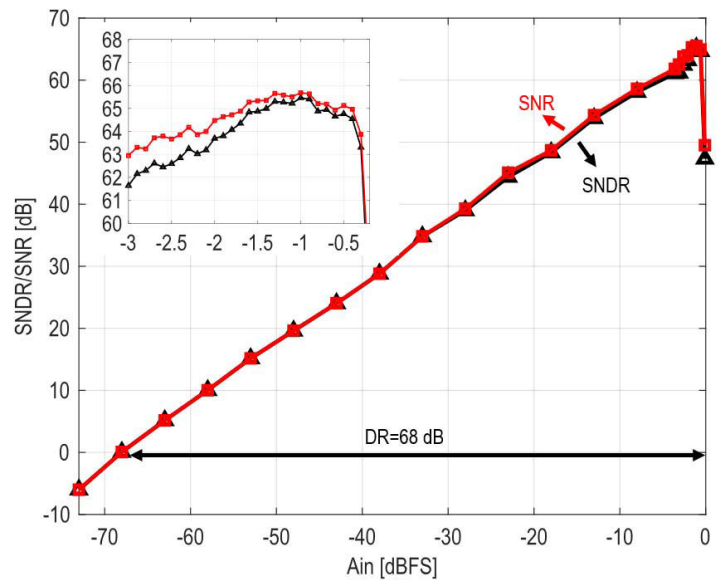

Figure 25.4.5: SNDR/SNR versus input level for F_{in}=115MHz.

	This work	JSSC 2016 Y. Dong [1]	JSSC 2017 H. Shibata [2]	ISSCC 2020 H. Shibata [3]
Technology (nm)	40	28	28	16
Architecture	CT ΔΣ MASH 1-1-1	CT ΔΣ MASH 1-2	CT pipeline	CT pipeline
Vdd (V)	1.8 / 1.1 /1	1.8 / 1.0 / -1.0	1.8 / 1.1/-1.0	1.8 / 1.0 / 0.8
OSR	7	8.6	4	4
Area (mm^2)	0.21	1.4	5.1	0.34*
Fs (GHz)	5	8	9	6.4
Bandwidth (MHz)	360	465	1125	800
Peak SNR (dB)	65	68	66	58
Peak SNDR (dB)	65	67	66	58
DR (dB)	68	72	73	60
THD (dBc)	-78	n.a.	n.a.	-82
Power (mW)	158	890	2330	280*
FoM_S (dB)	159	154	153	153
FoM_W (fJ/Conv.)	151	523	635	270

FoM_S = SNDR+10*log10(BW/P), FoM_W = P/(2^{ENOB}*2*BW). *Both analog and digital power/area included.

Figure 25.4.6: Performance summary and comparison to the state-of-the-art CT ADC with BW ≥ 250MHz and DR ≥ 60dB.

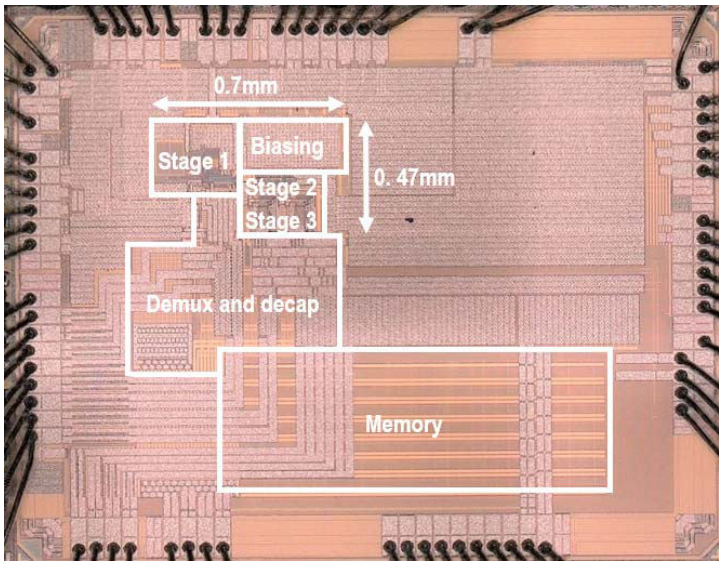

Figure 25.4.7: Chip micrograph.

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