The Zoom ADC

An Energy Efficient ADC for High Resolution

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Summary

Analog-to-digital converters (ADCs) are an indispensable part of the digital age we are living in, as they form the interface between physical reality and virtual reality. Higher ADC energy efficiency is the dominant focus of ADC design research due to the high impact of ADC energy consumption to total energy consumption of the systems they are employed in. The energy consumption of an ADC increases with its resolution within a given signal bandwidth, which makes the efficiency of high-resolution ADCs even more important. Although the average energy efficiency of ADCs improved orders of magnitude in the last two decades, the high energy consumption of high-resolution ADCs was still restrictive for a large range of applications. This thesis investigates how the zoom ADC architecture can achieve both high resolution and high energy efficiency.

In Chapter 1, an introduction to the thesis is given and the importance of ADC energy efficiency is discussed. First an overview of the developments in ADC energy efficiency in the past two decades is presented. The zoom ADC, which was in its infancy when this thesis work started, is then identified as a suitable architecture for improving high-resolution ADC energy efficiency. This is followed by a detailed motivation of this thesis work.

Delta-sigma modulators (DSM) are the backbone of most high-resolution ADCs. For this reason, the fundamentals of their energy efficiency are analyzed in Chapter 2. In this deep dive into the lower limits of DSM energy consumption, the impact of noise and nonlinearity on both discrete-time (DT) and continuous-time (CT) DSMs are considered. This analysis yielded several interesting findings. Firstly, it is found that efficient amplifiers should be used to reduce the impact of thermal noise, especially for the first integrator of the DSMs. When efficient amplifiers are used, the circuit nonlinearity is found to be more dominant than thermal noise for both DTDSMs and CTDSMs but this is more severe for CTDSMs. Reducing the input swing of the loop-filter is shown to be the best way to reduce the impact of circuit nonlinearity. Energy efficient architectures, such as multi-bit DSMs, FIR-DAC DSMs and the zoom ADC, are observed to be doing exactly this. The properties of these architectures and a brief comparison of them are given.

Chapter 3 presents the system-level design of zoom ADCs. Firstly, the zoom ADC architecture is explained. This is followed by an in-depth analysis of the static and dynamic error sources. The static error sources are mostly related to the unit element mismatch of the DAC of a zoom ADC, the use of over-ranging in combination with dynamic element matching (DEM) techniques is proposed. Furthermore, the quantization noise leakage of the coarse ADC into the output of a zoom ADC is discussed and digital and analog methods to alleviate this are proposed. The dynamic errors mainly result from the delay between the coarse and fine ADC sampling moments, the dynamic zoom ADC architecture making use of a coarse ADC running in tandem with its fine DSM is introduced. The impact of the sampling rate of the coarse ADC in a dynamic zoom ADC is investigated.

Chapter 4 discusses the design of dynamic zoom ADCs for audio applications. The input signal bandwidth of the incremental zoom ADCs before this implementation were limited to Hz range because of the sequential operation of their coarse ADC and fine DSM. The coarse and fine converters of the dynamic zoom ADC introduced in this thesis work in tandem, making it possible to achieve kHz input signal bandwidth required for audio applications. The coarse ADC of the designs is a 5-bit synchronous successive-approximation register (SAR) ADC. This is followed by a 3^{rd}-order feed-forward compensated 1-bit fine DTDSM. The amplifiers used in the integrators of the loop-filter are based on a dynamically biased inverter which combines auto-zeroing with biasing of the amplifier. Since this amplifier is pseudo-differential, it is prone to high common-mode signals at its input. A differential sampling scheme with high common-mode rejection is used to boost the common-mode rejection ratio (CMRR) of the ADC. A first prototype achieved 98.3 dB signal-to-distortion ratio (SNDR) and 107.5 dB dynamic range (DR) in a 20 kHz bandwidth while consuming 1.65 mW corresponding to a figure-of-merit (FOM) of 178.3 dB. A revised version of this, the second prototype, achieved 103 dB SNDR and 109 dB DR, while its power consumption dropped to 1.12 mW and its FOM increased to 181.5 dB. In terms of bandwidth, this represents a 1000-fold improvement on incremental zoom ADCs, while maintaining their state-of-the-art energy efficiency.

Chapter 5 describes a dynamic zoom ADC for instrumentation applications. Based on an asynchronous SAR, which allows the DSM references to be updated after every clock cycle, this zoom ADC is more robust to out-of-band interferers, and has relaxed loop filter requirements and, hence, increased overall energy efficiency. The use of the 5-bit asynchronous SAR ADC made it possible to reduce the over-ranging factor to its minimum. This resulted in not only increased signal-to-quantization-noise ratio (SQNR) but also a reduced loop-filter input swing. The reduced swing made it possible to use fully-differential current-starved inverter

amplifiers in the loop-filter, which are much simpler compared to the dynamically-biased amplifiers in the previous applications. $1/f$ noise and offset are reduced by use of correlated double-sampling (CDS) in the first integrator. The non-unity STF of the loop-filter is found to be the reason behind imperfect cancellation of the SAR ADC quantization error giving rise to the spectral "fuzz" seen at the previous dynamic zoom ADC implementations. This is addressed in digital, similar to multi-stage noise-shaping (MASH) ADCs. The ADC achieves a peak signal-to-noise ratio (SNR), SNDR and total harmonic distortion (THD) of 119.1, 118.1 and -125.9 dB respectively. The measured DR of the ADC is 120.3 dB and its power consumption is 280 μW resulting in 185.8 dB FOM.

Chapter 6 presents the design of a CT zoom ADC for audio applications. It combines an asynchronous 5-bit SAR ADC with a 3^{rd}-order 1-bit CTDSM. As found in Chapter 2, the amplifier linearity has a larger impact on the energy efficiency of CTDSMs. For improved energy-efficiency and linearity, its first integrator is based on a capacitively-coupled pseudo-differential inverter-based amplifier, which is more linear compared to a fully-differential amplifier. The amplifier is chopped at the sampling frequency to mitigate its $1/f$ noise while not resulting in chopping related artifacts. Inter-symbol-interference (ISI) in the DAC of a CTDSM is an important nonlinear error source. This is addressed by a novel ISI reduction technique based on a matched-pair layout in the resistive non-return-to-zero (NRZ) DAC. The ADC achieves 108.1 dB peak SNR, 106.4 dB peak SNDR and 108.5 dB DR in a 20 kHz bandwidth while dissipating only 618 μW, and its FOM is 185.8 dB.

Chapter 7 summarizes the main findings of this thesis, discusses other applications of the developed techniques, and includes some proposals for future work. The circuit nonlinearity of the 1st-integrator of a high-resolution DSM is the main factor determining the energy consumption. This resulted in the observation that the key to improve the energy efficiency of a high-resolution DSM is to reduce its loop-filter's input swing. The zoom ADC is a competitive architecture achieving this while not complicating the circuit design. Unlike prior zoom ADCs based on sequential two-step conversion, which were too slow for audio applications, the dynamic zoom ADCs proposed in this thesis are suitable for digitization of kHz range audio signals by employing concurrent coarse and fine conversions.

Samenvatting

Analoog-digitaalomzetters (ADCs) zijn een onmisbaar onderdeel van het digitale tijdperk waarin we leven, omdat zij de verbinding vormen tussen de fysieke en virtuele realiteit. In onderzoek naar ADC ontwerpen overheerst de focus op grotere ADC energie-efficiëntie, vanwege de grote impact van het energieverbruik van de ADC op het totale energieverbruik van de systemen waarin zij gebruikt worden. Het energieverbruik van een ADC groeit parallel aan zijn resolutie binnen een bepaalde signaal bandbreedte. Dit maakt de efficiëntie van hoge resolutie ADCs éxtra belangrijk. Hoewel de gemiddelde energie-efficiëntie van ADCs tientallen orders verbeterd is in de afgelopen twee decennia, bleef het hoge energieverbruik van hoge resolutie ADCs limiterend voor een grote reeks aan toepassingen. Dit proefschrift onderzoekt hoe de zoom ADC architectuur zowel hoge resolutie als hoge energie-efficiëntie kan bereiken.

Hoofdstuk 1 geeft een introductie van het proefschrift en bespreekt het belang van ADC energie-efficiëntie. Allereerst wordt een overzicht gegeven van de ontwikkelingen in ADC energie-efficiëntie in de afgelopen twee decennia. De zoom ADC, die nog in de kinderschoenen stond op het moment dat het werk aan dit proefschrift begon, wordt vervolgens benoemd als een passende architectuur om de energie-efficiëntie van hoge resolutie ADCs te verbeteren. Hierop volgt een gedetailleerde motivatie voor dit proefschrift.

Delta-sigma modulators (DSM) zijn de basis van de meeste hoge resolutie ADCs. Daarom worden de grondbeginselen van hun energie-efficiëntie geanalyseerd in Hoofdstuk 2. In dit diepgravend onderzoek naar de lagere limieten van DSM energieverbruik wordt de impact van ruis en niet-lineariteit op zowel tijdsdiscrete (DT) en tijdscontinue (CT) DSMs beschouwd. Deze analyse resulteerde in verschillende interessante bevindingen. Allereerst wordt ontdekt dat efficiënte versterkers gebruikt moeten worden om de impact van thermische ruis te reduceren, vooral in de eerste integrator van de DSMs. Het blijkt dat bij gebruik van efficiënte versterkers de niet-lineariteit van het circuit dominanter is dan de thermische ruis. Dit geldt voor zowel DT DSMs en CT DSMs, maar het meest voor CT DSMs. Het reduceren van de signaalzwaai van het lusfilter wordt gepresenteerd als de beste manier om de impact van de niet-lineariteit van het circuit te reduceren. Energie-efficiënte architecturen, zoals meerdere-

bits DSMs, FIR-DAC DSMs en de zoom ADC, laten precies ditzelfde zien. Daarom volgt een uiteenzetting van de eigenschappen van deze architecturen en een korte vergelijking ervan.

Hoofdstuk 3 presenteert het ontwerp van zoom ADCs op systeemniveau. Allereerst wordt de zoom ADC architectuur uitgelegd. Dit wordt gevolgd door een diepgaande analyse van de statische en dynamische foutbronnen. De statische foutbronnen zijn vooral gerelateerd aan de mismatch in het eenheidselement van de digitaal-analogomzetter (DAC) van een zoom ADC; het gebruik van over-ranging in combinatie met dynamische matching van de elementen (DEM) wordt daarom voorgesteld. Voorts wordt de lekkage van de kwantisatieruis van de grove ADC naar de uitgang van een zoom ADC besproken en worden zowel digitale als analoge methodes voorgesteld om dit te verlichten. De dynamische fouten resulteren vooral uit de vertraging tussen de sample momenten van de grove en fijne ADC. Daarom wordt de dynamische zoom ADC architectuur geïntroduceerd, gebruikmakend van een grove ADC die in tandem loopt met zijn fijne DSM. De impact van de samplefrequentie van de grove ADC op een dynamische zoom ADC wordt onderzocht.

Hoofdstuk 4 behandelt het ontwerp van dynamische zoom ADCs voor audiotoepassingen. De bandbreedte van het ingangssignaal van de incrementele zoom ADCs vóór deze implementatie was gelimiteerd tot het hertz bereik vanwege de sequentiële operatie van hun grove ADC en fijne DSM. De grove en fijne omzetters van de dynamische zoom ADC worden in dit proefschrift in tandem geïntroduceerd, waardoor het mogelijk is om een kilohertz ingangssignaal bandbreedte te bereiken, die nodig is voor audiotoepassingen. De grove ADC in deze ontwerpen is een 5-bit synchrone successive-approximation register (SAR) ADC. Dit wordt gevolgd door een derde orde voorwaartsgekoppeld gecompenseerde 1-bit fijne DT DSM. De versterkers die worden gebruikt in de integrators van het lusfilter zijn gebaseerd op een dynamisch gevoede inverter die auto-zeroing combineert met het instellen van de versterker. Omdat de versterker pseudo-differentieel is, is het gevoelig voor hoge common-mode signalen aan zijn ingang. Een differentieel sample schema met hoge common-mode onderdrukking wordt gebruikt om de common-mode rejection ratio (CMRR) van de ADC te boosten. Een eerste prototype bereikte 98.3 dB signal-to-distortion ratio (SNDR) en 107.5 dB dynamisch bereik (DR) in een 20 kHz bandbreedte, en verbruikte 1.65 mW. Dit komt overeen met een figure-of-merit (FOM) van 178.3 dB. Een aangepaste versie hiervan, het tweede prototype, bereikte 103 dB SNDR en 109 dB DR, terwijl het vermogensverbruik daalde naar 1.12 mW en zijn FOM verhoogde naar 181.5 dB. Wat betreft bandbreedte vertaalt dit zich in een 1000-maal verbetering op incrementele zoom ADCs, en tegelijkertijd behoudt het zijn 'state-of-the-art' energie-efficiëntie.

Hoofdstuk 5 beschrijft een dynamische zoom ADC voor instrumentatie toepassingen.

Gebaseerd op een asynchrone SAR, die het toestaat dat de DSM referenties vernieuwd worden na elke klok periode, is deze zoom ADC robuuster dan out-of-band omvormers, en het heeft toegeeflijke lusfilter vereisten; waardoor de totale energie-efficiëntie groter is. Het gebruik van de 5-bit asynchrone SAR ADC maakte het mogelijk om de over-ranging factor te reduceren tot zijn minimum. Dit resulteerde niet alleen in een vergroot signal-to-quantization-noise ration (SQNR), maar ook in een verminderde signaalzwaai in het lusfilter. Deze verminderde zwaai maakte het mogelijk om volledig differentiële stroom-gelimiteerde inverter-gebaseerde versterkers in het lusfilter te gebruiken. Deze zijn eenvoudiger in vergelijking met de dynamisch ingestelde versterkers in de eerdere toepassingen. $1/f$ ruis en offset zijn verminderd door het gebruik van gecorreleerde dubbele sampling (CDS) in de eerste integrator. De signaal transferfunctie van het lusfilter is ongelijk aan 1 en blijkt daardoor de reden te zijn voor de imperfecte onderdrukking van de kwantisatiefout in de SAR ADC, die de oorzaak blijkt voor de spectrale 'fuzz' die wordt gevonden in voorgaande dynamische zoom ADC implementaties. Dit wordt behandeld in het digitale domein, op een soortgelijke manier als multi-stage noise-shaping (MASH) ADCs. De ADC bereikt een piek signal-to-noise ratio (SNR), SNDR en total harmonische vervorming (THD) van respectievelijk 119.1, 118.1 en -125.9 dB. Het gemeten dynamische bereik van de ADC is 120.3 dB en het vermogensverbruik is 280 μW, resulterend in 185.8 dB FOM.

Hoofdstuk 6 presenteert het ontwerp van een CT zoom ADC voor audiotoepassingen. Het combineert een asynchrone 5-bit SAR ADC met een 3^e orde 1-bit CT DSM. Zoals aangetoond in Hoofdstuk 2, heeft de lineariteit van de versterkers een grotere impact op de energie-efficiëntie van CT DSMs. Voor verbeterde energie-efficiëntie en lineariteit, is zijn eerste integrator gebaseerd op een capacitief gekoppelde pseudo-differentiele inverter-gebasseerde versterker, die lineairder is dan een volledig differentiele versterker. De versterker is gechopt op de sample frequentie om zijn $1/f$ ruis op te verwijderen, zonder te resulteren in artefacten gerelateerd aan het choppen. Inter-symbool-interferentie (ISI) in de DAC van een CTDSM is een belangrijke foutbron van niet-lineaireit. Dit wordt behandeld met een vernieuwende ISI verminderingstechniek gebaseerd op een matched-pair layout in de op weerstanden gebaseerde non-return-to-zero (NRZ) DAC. De ADC bereikt 108.1 dB piek SNR, 106.4 piek SNDR en 108.5 dB DR in een 20 kHz bandbreedte, terwijl het slechts 618 μW verbruikt, en zijn FOM is 185.8 dB.

Hoofdstuk 7 vat de hoofdbevindingen van dit proefschrift samen, bespreekt mogelijke andere toepassingen van de ontwikkelde technieken, en bevat enkele voorstellen voor toekomstig werk. De niet-lineariteit van het circuit van de 1^e integrator van een hoge resolutie DSM is de belangrijkste factor voor het vaststellen van het energieverbruik. Dit resulteerde in de ob-

servatie dat het reduceren van de signaalzwaai van het lusfilter de sleutel is tot het verbeteren van energie-efficiëntie van een hoge resolutie DSM. De zoom ADC is een competitieve architectuur die dit bereikt zonder het circuit ontwerp te compliceren. Anders dan eerdere zoom ADCs gebaseerd op sequentiële conversie in twee stappen, die te langzaam waren voor audiotoepassingen, is de dynamische zoom ADC zoals aangedragen in dit proefschrift wél geschikt voor digitalisering van kilohertz bereik audiosignalen, door opeenvolgend grove en fijne omzettingen te gebruiken.

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Chapter 1

Introduction

We are living in a digital age. But since the real world remains stubbornly analog, techniques to efficiently digitize physical quantities such as sound, color, light intensity, temperature, and humidity are essential. This usually involves the use of a sensor that performs a first conversion of such quantities into analog signals such as voltage, current, and charge. This is then followed by an analog to digital conversion. Analog-to-digital converters (ADCs) are thus an indispensable part of our digital age, as they form the interface between physical reality and virtual reality.

Over the last few decades, there has been an enormous improvement in ADC energy efficiency. Based on the data presented in [1], the energy-per-conversion (E_{conv}) vs signal-to-noise and distortion ratio (SNDR) of ADCs published in the last two decades is shown in Fig. 1.1. The lines representing the lowest E_{conv} for each decade are also shown, showing that it has improved 16-fold between 2000 and 2010, and 90-fold between 2010 and 2020. This represents a total improvement of more than three orders-of-magnitude in only two decades. This has made many new applications possible, from digital cameras and high-bandwidth internet to smartphones and wearables. The popularity of these applications, in turn, has only increased the demand for ADCs with even better performance.

Although CMOS technology scaling has helped fuel this impressive progress, the biggest contributor, especially in the last decade, has been a better understanding of the architectural trade-offs inherent to ADC design. Successive-approximation (SAR) ADCs have experienced a revival, with new architectures that leverage the improved digital performance provided by CMOS scaling while minimizing hardware complexity. The result has been a rapid improvement in the energy efficiency of low to medium resolution ADCs, i.e. 30 to 70 dB SNDR, whose E_{conv} is mainly dominated by the energy associated with amplitude quantization. How-

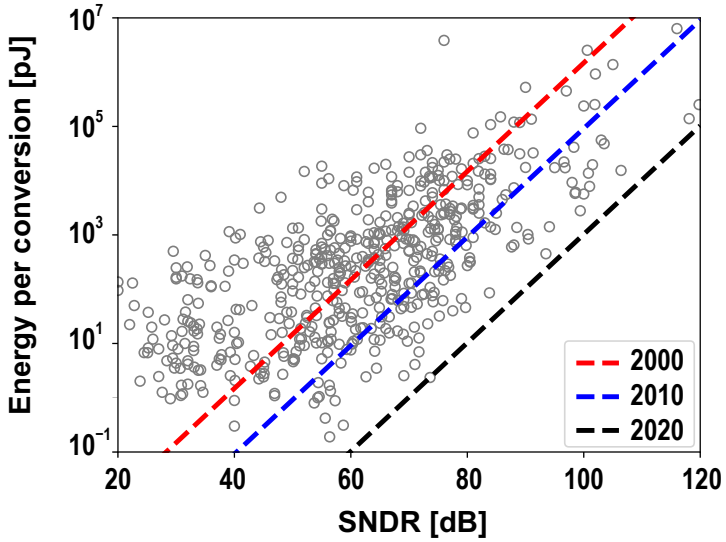

Figure 1.1: Energy-per-conversion vs SNDR for the ADCs published in last two decades [1].

ever, designing SAR ADCs with higher resolution (> 70 dB SNDR) becomes harder due to component mismatch, which requires extensive calibration, and low thermal noise requirements, which increases the energy consumption of their capacitive digital-to-analog converters (DAC) and comparators. The high resolution design space (> 70 dB SNDR) has been traditionally dominated by delta-sigma-modulators (DSMs), due to their ability to trade-off resolution for speed and thus decouple the energy associated with quantization from that required to reduce thermal noise. Although an immense amount of progress has been made in understanding DSMs, improvements in the energy efficiency of very high resolution (> 100 dB SNDR) designs has been comparatively slow. The work described in this thesis represents an attempt to investigate how a new architecture, the zoom ADC, can achieve both high resolution and high energy efficiency.

1.1 Previous Work

In 2010, Souri et al. described a high-resolution ADC that used a SAR ADC to perform an initial coarse conversion, followed by a DSM for a fine fine conversion as shown in Fig. 1.2 [2]. Intended for use in a temperature sensor, it exploited the fact that temperature changes are slow, and so the input signals (V_{BE} and ΔV_{BE}) were essentially constant during a conversion. The key idea behind this "zoom" ADC was to use the information obtained during the coarse conversion to zoom in and narrow the conversion range of the DSM. This reduces the ADC's

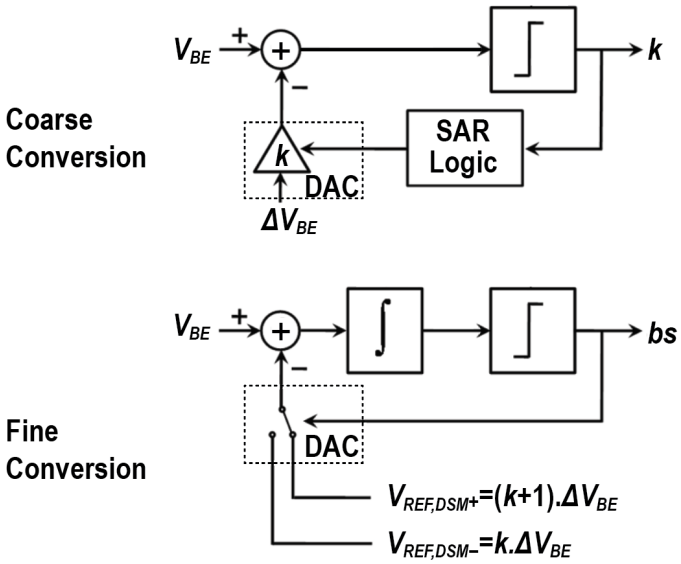

Figure 1.2: The first zoom ADC implementation [2].

overall energy consumption, and as such the resulting temperature sensor had state-of-the-art energy efficiency. In later work by Chae et al. [3], a similarly energy-efficient stand-alone zoom ADC was described, which, at that time, represented a more than 10-fold improvement in the state-of-the-art. Shortly thereafter, a capacitance-to-digital converter (CDC) also achieved high energy efficiency by using a similar architecture [4]. Despite their high energy efficiency, however, one drawback of these designs was that they were only suitable for the digitization of quasi-static signals (< 20 Hz bandwidth).

1.2 Motivation

In 2014, when this thesis work started, the main goal was to overcome the bandwidth limitations of zoom ADCs while maintaining their excellent energy efficiency. As a natural first step, the aim was to improve the input signal bandwidth to kHz range. This drove an exploration of the architectural trade-offs inherent to zoom ADCs and resulted in the dynamic zoom ADC architecture (Chapter 3).

Improving the energy efficiency of very high-resolution ADCs represents a challenge due to their low thermal noise and high linearity requirements. At first sight, noise and linearity may seem to be orthogonal specifications. However, ADC designers often observe a trade-off between them, whose exact nature is concealed by architectural complexity. The zoom ADC, due to its architectural simplicity and flexibility, presents an opportunity to understand

the trade-off between noise and linearity. This motivated the choice of very high-resolution applications such as audio and instrumentation for the ADC designs described in this thesis (Chapter 4-6).

1.3 Thesis Organization

In Chapter 2, the energy efficiency limits of high-resolution DSMs, for both discrete-time and continuous-time architectures are analyzed. In Chapter 3, the system-level design trade-offs of zoom ADCs are discussed. The rest of the thesis is divided into two parts. In Chapters 4 and 5, two dynamic zoom ADC designs based on discrete-time delta-sigma modulators (DTDSM) are presented: the former intended for audio applications, and the latter for instrumentation applications. The audio design was the first dynamic zoom ADC, and it allowed the various system-level trade-offs to be explored and proven in silicon. Using the findings from this first design, the second design then achieved both improved energy efficiency and linearity. In Chapter 6, a dynamic zoom ADC based on a continuous-time delta-sigma modulator (CTDSM) is presented. Compared to the previous designs, the use of a continuous-time DSM presents extra design challenges. These are explained and the methods to tackle them are discussed in depth. Chapter 7 then concludes this thesis, underlining its contributions and suggesting some future work.

1.4 References

[1] B. Murmann, *ADC performance survey 1997-2020*. [Online]. Available: `http://web.stanford.edu/~murmann/adcsurvey.html`.

[2] K. Souri, M. Kashmiri, and K. Makinwa, "A CMOS temperature sensor with an energy-efficient zoom ADC and an inaccuracy of ± 0.25°C (3σ) from -40°C to 125," in *Dig. Tech. Papers ISSCC*, Feb. 2010, pp. 310–311.

[3] Y. Chae, K. Souri, and K. A. A. Makinwa, "A 6.3 μW 20 bit incremental zoom-ADC with 6 ppm INL and 1 μV offset," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3019–3027, Dec. 2013.

[4] S. Oh, W. Jung, K. Yang, D. Blaauw, and D. Sylvester, "15.4b incremental sigma-delta capacitance-to-digital converter with zoom-in 9b asynchronous SAR," in *Proc. Symp. VLSI Circuits*, Jun. 2014, pp. 1–2.

Chapter 2

Energy Efficiency of High Resolution Delta-Sigma Modulators

2.1 Introduction

As discussed in Chapter 1, high-resolution ADCs are often thermal noise limited. Thus it is important to understand how the presence of thermal noise limits the amount of energy consumed per conversion. In real circuits, energy is also consumed to overcome other error sources such as settling inaccuracy and circuit nonlinearity. In this chapter, the impact of thermal noise, settling inaccuracy and circuit nonlinearity on ADC energy efficiency will be analyzed.

2.2 Energy Consumption Due to Thermal Noise

Although there is no universally accepted lower limit of ADC energy consumption, a physical lower limit of the required energy to overcome thermal noise can be found. An ADC can be

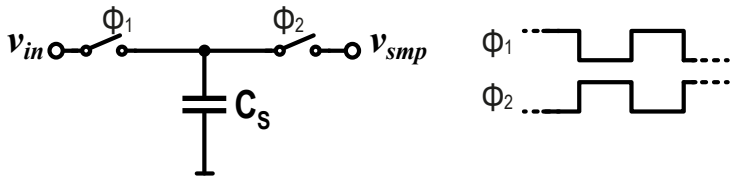

Figure 2.1: A simple sample and hold.

modelled as a simple sample-and-hold, as in Fig. 2.1. Its resolution, expressed as signal-to-noise ratio (SNR), will then be limited by the sampled noise, which is known to be $\frac{kT}{C_s}$. The energy required to drive the sample and hold with a certain SNR can then be considered to be a lower limit for the ADC conversion energy, E_{min}. From the analysis in Appendix A, this is found to be:

$$E_{min} = kT \text{ SNR} \tag{2.1}$$

This result describes the energy required to sample the signal, but does not account for the energy needed to quantize its amplitude.

2.3 Thermal Noise and Linearity Limited Conversion Energy in Discrete-Time Delta-Sigma Modulators

2.3.1 Thermal Noise

The energy consumed per conversion by a typical first stage of a DTDSM in which the sampling capacitor is also used to implement its feedback DAC as shown in Fig. 2.2 is found in Appendix A as:

$$E_{min,DT} = 4kT \text{ SNR}. \tag{2.2}$$

In (2.2), the amplifier was assumed to be noiseless. In reality, all amplifiers exhibit thermal and $1/f$ noise [1]. As found in Appendix A, the energy consumed in one conversion period considering the amplifier thermal noise is:

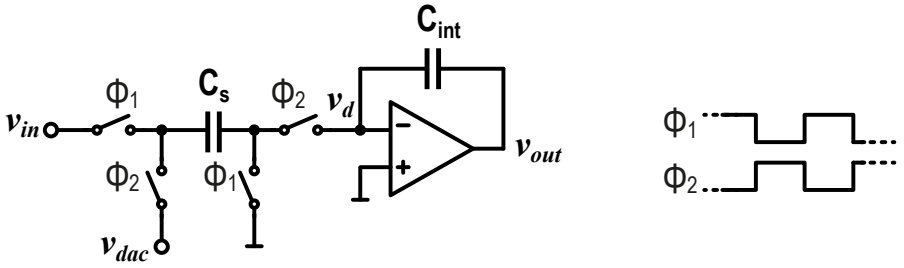

Figure 2.2: DTDSM input stage with single capacitor.

[1] $1/f$ noise may be dominant in low bandwidth high resolution ADCs. This can be alleviated by the use of dynamic techniques such as auto-zeroing or chopping. Thus, $1/f$ noise will be ignored in the noise related analyses.

$$E_{th,DT} = 2\,(1+\Gamma_n)\,kT\ \mathrm{SNR} \tag{2.3}$$

where Γ_n is noise excess factor [2] expressing the efficiency of the amplifier as defined in Appendix A and explained in detail in [1]. In the case of $\Gamma_n = 1$, there will be no excess noise and (2.3) is equal to (2.2). A low Γ_n can be achieved by avoiding current sources, load resistors, and extra current branches as in the case of folded-cascode amplifiers [1]. $\Gamma_n = 1$ is obtained if all the transistors used in the amplifier are input transistors, as is the case in inverter-based amplifiers [3, 4] [3]. Their Γ_n can be reduced further by stacking [7].

2.3.2 Linear and Nonlinear Settling Error

In switched-capacitor (SC) circuits the signal must settle to the level of accuracy necessary to maintain signal integrity. This is directly related to the required resolution because the sampling capacitance of the system is determined by noise requirements, as discussed in Section 2.2. The relative error within the settling time, t_{set}, can be expressed as:

$$\varepsilon_{set} = e^{-n_\tau} \tag{2.4}$$

where n_τ is the ratio of t_{set} and the system time constant τ:

$$n_\tau = \frac{t_{set}}{\tau}. \tag{2.5}$$

Assuming $C_s = C_{int}$, τ is:

$$\tau = \frac{C_s}{g_m} \tag{2.6}$$

where g_m is the transconductance of the amplifier, which is assumed to be single-stage.

The complete settling is achieved when the settling error is smaller than the other contributions such as thermal noise and quantization noise. This condition can be expressed as:

$$\varepsilon_{set} < \frac{1}{\sqrt{\mathrm{SNR}}}. \tag{2.7}$$

Fig. 2.3 is a plot of n_τ vs relative settling error. It can be seen that for high resolution, complete settling requires quite a high value of n_τ. For example, $n_\tau \simeq 14$ is needed to achieve 120 dB SNR. From (2.5) and (2.6), n_τ is proportional to g_m. Since the capacitance value is

[2] Note that the noise excess factor defined in [1] is different than noise efficiency factor defined in [2].

[3] Inverter-based amplifiers using switched-capacitor biasing techniques could exhibit excess noise [5, 6].

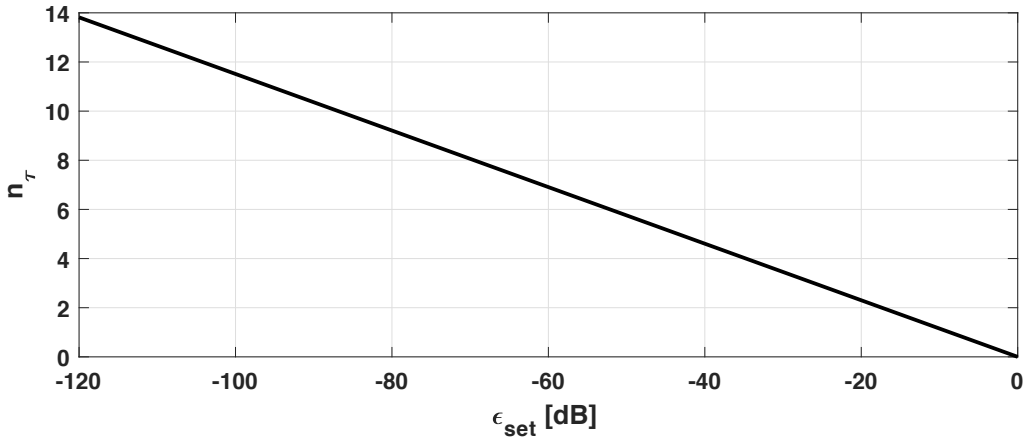

Figure 2.3: n_τ vs relative settling error.

determined by the thermal noise requirements, the only way to increase n_τ is to increase g_m. This will increase the energy consumption.

Considerable energy can be saved by accepting so-called incomplete settling, i.e. using a smaller n_τ than is necessary for complete settling [1, 8, 9]. Although this results in a larger ε_{set}, this will be a linear gain error if n_τ is constant and g_m is linear. An integrator with incomplete settling can then be modeled as a leaky integrator, similar to an integrator with limited DC gain A_0. The gain error due to incomplete settling is given as:

$$\varepsilon_{set} \approx \frac{1}{A_0}. \tag{2.8}$$

As a rule of thumb, DC gain of each amplifier in a single-loop DSMs should be [10]:

$$A_0 \gtrsim \mathrm{OSR}. \tag{2.9}$$

From (2.8) and (2.9)

$$\varepsilon_{set} < \frac{1}{\mathrm{OSR}}. \tag{2.10}$$

Required n_τ can be found by using (2.4)

$$n_\tau > \ln(\mathrm{OSR}). \tag{2.11}$$

For example, a modulator with OSR $= 128$ would only need $n_\tau = 5$ as it is seen in Fig. 2.3. This can be reduced even further if the loss of gain is compensated by adjusting the feedback factor.

Another lower limit on n_τ results from amplifier nonlinearity, which is mainly due to the nonlinear g_m of the input transistors. This causes both harmonic distortion and quantization noise folding and is an important limitation on SNDR [11]. Since most high-resolution DSMs are fully-differential, the most dominant nonlinearity is often third-order g_m nonlinearity, usually expressed by their third-order distortion-to-signal-ratio (HD3). The HD3 of a DTDSM with an $N-$bit DAC is analyzed in Appendix B and found to be:

$$\text{HD3} = \frac{\lambda}{2} e^{-n_\tau} \frac{\hat{V}_{in}^2}{2^{3N-2}} \tag{2.12}$$

where λ is a third-order nonlinearity factor, and $\hat{V}_{in}$ is the peak-to-peak amplitude of the maximum input signal. Note that a lower HD3 indicates less nonlinearity. The latter can be expressed as a fraction of the ADC's full-scale voltage reference range V_{FS}:

$$2\hat{V}_{in} = \eta_v V_{FS}. \tag{2.13}$$

Combining (2.12) and (2.13), the n_τ for a desired HD3 level for a DTDSM with an N-bit DAC is found as

$$n_{\tau,\text{HD3}} = \ln\left(\frac{\lambda\, \eta_v^2 V_{FS}^2}{\text{HD3}}\right) - (3N+1)\ln 2. \tag{2.14}$$

Note that lowering n_τ below 2 does not improve energy efficiency because of the increase in thermal noise explained in [9]. Thus, $n_\tau = 2$ the optimum settling factor for highest energy efficiency when only thermal noise is considered.

2.3.3 Thermal Noise and Amplifier Nonlinearity Limited Energy Efficiency

Appendix C reports the results of an analysis performed to understand the effect of n_τ on the energy efficiency of DTDSM input stages implemented with a single stage-amplifier[4] as shown in Fig. 2.4. Assuming the settling time is half a clock period ($t_{set} = \frac{0.5}{f_S}$), the energy consumed by the amplifier is found to be:

$$E_{amp,DT} = 8kT\ \text{SNR}\ (1+\Gamma_n)\frac{V_{gt}}{\eta_v^2\, \eta_c\, V_{dd}} n_\tau \tag{2.15}$$

where η_v is voltage efficiency factor, which defines how efficiently the voltage headroom is used, η_c is the current efficiency factor, which defines how much of the amplifier's supply cur-

[4] A similar analysis of switched-capacitor amplifiers is presented in [1].

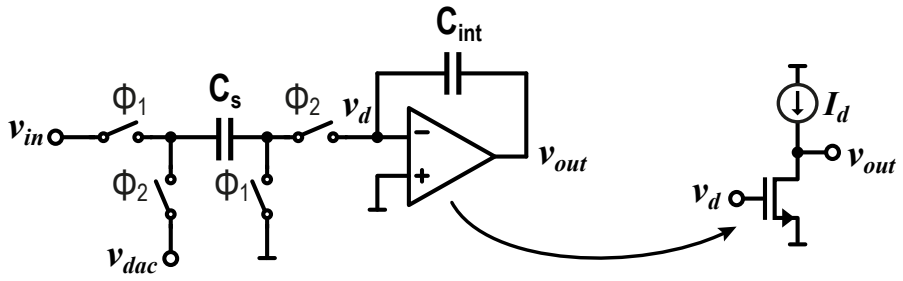

Figure 2.4: SC integrator with single stage amplifier.

rent is contributing to the transconductance, and V_{gt} is the overdrive voltage of the transistor. Note that V_{gt} is equal to difference of the gate bias voltage (V_g) and the threshold voltage (V_{th}) for strong inversion, but constant and equal to roughly 80 mV for weak inversion [1]. More detailed definitions of η_v and η_c are given in Appendix C.

The total energy per conversion is given by the sum of the energy consumed to drive the input and the reference given in (2.3) and the energy consumed by the amplifier given in (2.15):

$$E_{tot,DT} = 2kT \text{ SNR } (1+\Gamma_n)\left(1+\frac{4V_{gt}}{\eta_v^2\,\eta_c V_{dd}}n_\tau\right). \tag{2.16}$$

As expected, the Γ_n is quite dominant. An important observation is that η_v has a significant impact on the energy consumption. In other words, the input stage should use its voltage swing efficiently. η_c is also important, making current re-use structures such as inverter-based amplifiers ($n_c = 2$), single current branch structures such as telescopic amplifier ($\eta_c = 1$), and stacked amplifiers desirable, but amplifiers with extra current branches such as folded-cascode amplifier ($\eta_c = 0.5$) undesirable.

If an inverter-based amplifier is used, and the input voltage swing is maximized ($\eta_c = 2$, $\eta_v = 1$), and the excess noise is minimized ($\Gamma_n = 1$) (2.16) will become:

$$E_{tot,DT} = 4kT \text{ SNR } \left(1+\frac{2V_{gt}}{V_{dd}}n_\tau\right). \tag{2.17}$$

As can be seen from (2.17), V_{gt} should be as small as possible, while the highest possible V_{dd} should be used. V_{gt} has its lowest and constant value, roughly 80 mV at room temperature, in weak-inversion [1, 12]. Hence, a weak-inversion operation is desired. However, this may not be possible for high clock frequencies depending on the adopted technology node [1, 12]. Furthermore, n_τ should be minimized for high energy efficiency. This can be achieved by using incomplete settling and reducing n_τ to the lowest possible for level required for achieving the required HD3 level as given in (2.14). Using (2.14) in (2.17) and assuming

$V_{FS} = V_{dd}$, the total energy consumption can be expressed when n_τ is determined by the HD3 requirement as:

$$E_{tot,DT} = \begin{cases} 4kT\ \text{SNR}\ \left(1+\frac{2V_{gt}}{V_{dd}}\left(\ln\left(\frac{\lambda\,\eta_v^2 V_{dd}^2}{\text{HD3}}\right)-(3N+1)\ln 2\right)\right) & n_{\tau,\text{HD3}} > 2 \\ 4kT\ \text{SNR}\ \left(1+\frac{4V_{gt}}{V_{dd}}\right) & n_{\tau,\text{HD3}} \leq 2. \end{cases} \tag{2.18}$$

Note that $n_\tau = 2$ is assumed as a lower limit for an optimum efficiency. Considering $\frac{4V_{gt}}{V_{dd}} \ll 1$ when an amplifier in weak-inversion is used, the minimum energy required by the input stage of a DTDSM is found to be again:

$$E_{min,DT} = 4kT\ \text{SNR}. \tag{2.19}$$

2.4 Thermal Noise and Linearity Limited Conversion Energy in Continuous-Time Delta-Sigma Modulators

2.4.1 Thermal Noise

An example of a CTDSM input stage based on an ideal amplifier and a resistive DAC (R-DAC)[5] is shown in Fig. 2.5. The total energy consumed in one conversion period is found in Appendix A to be:

$$E_{min,CT} = 8kT\ \text{SNR}. \tag{2.20}$$

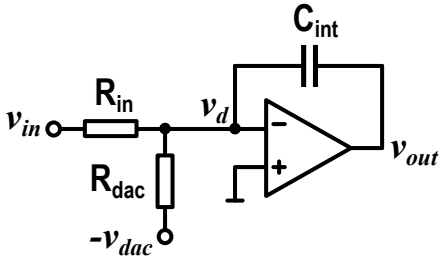

Figure 2.5: CTDSM input stage with R-DAC.

[5]Current DACs (I-DAC) are also used in CTDSMs. However, I-DACs exhibit more thermal and $1/f$ noise [13] compared to R-DACs, making them unsuitable for high resolution DSMs. For this reason, the analysis in this thesis is limited to CTDSMs employing R-DACs.

This assumes a noiseless amplifier. In reality, the amplifier in Fig. 2.5 will exhibit thermal noise. Assuming $R_{in} = R_{dac}$, the total energy consumed in one conversion period to drive the input and DAC resistors is found to be:

$$E_{th,CT} = \eta_P \, 8kT \ \text{SNR}. \tag{2.21}$$

where η_P is an excess power consumption factor defined in Appendix A to accommodate the increased power consumption due to amplifier noise. This result does not include the energy consumed by the amplifier itself. The energy consumed by an amplifier is strongly related to its g_m, which is often chosen considering linearity requirements. Thus, in order to find the amplifier energy consumption, the relationship of g_m and the linearity should be defined.

2.4.2 Amplifier Nonlinearity

Amplifier nonlinearity affects the SNDR of CTDSMs in a similar way to their DT counterparts by causing distortion and quantization noise fold-back [11]. The impact of the third-order g_m nonlinearity on the HD3 level for a CTDSM with an N-bit quantizer is found in Appendix B as:

$$\text{HD3} = \frac{\lambda}{2^{3N-1}\,(2+g_m R_{in})^3}\,\eta_v^2\,V_{FS}^2 \tag{2.22}$$

where λ is a third-order nonlinearity factor, η_v is voltage efficiency factor, and $g_m R_{in}$ is an important design parameter that defines the linearity of the input stage shown in Fig. 2.5 similar to n_τ for an SC input stage. For a given HD3 level, $g_m R_{in}$ can be found by using (2.22) as:

$$g_m R_{in} = \frac{1}{2^N}\sqrt[3]{\frac{2\,\lambda\,\eta_v^2\,V_{FS}^2}{\text{HD3}}} - 2. \tag{2.23}$$

2.4.3 Impact of Circuit Nonlinearity on Energy Efficiency

The power consumption of the single-stage OTA in Fig. 2.5 is dependent on g_m, which is often determined by linearity requirements for high resolution designs. The energy consumed by the amplifier in Fig. 2.5 found in Appendix C to be:

$$E_{amp,CT} = \frac{16kT \ \text{SNR}\ V_{gt}(g_m R_{in} + 2\Gamma_n)}{\eta_v^2\,\eta_c\,V_{dd}}. \tag{2.24}$$

The total energy consumption $E_{tot,CT}$ is the sum of $E_{th,CT}$ from (2.21) and $E_{amp,CT}$ from (2.24):

$$E_{tot,CT} = 8kT\ \text{SNR}\left(\eta_P + \frac{2V_{gt}}{\eta_v^2\,\eta_c\,V_{dd}}(g_m R_{in} + 2\,\Gamma_n)\right). \tag{2.25}$$

η_P is defined in Appendix A as:

$$\eta_P = 1 + \frac{2\Gamma_n}{g_m R_{in}} \tag{2.26}$$

Using (2.26) in (2.25):

$$E_{tot,CT} = 8kT\ \text{SNR}\left(1 + \frac{2\Gamma_n}{g_m R_{in}} + \frac{2V_{gt}}{\eta_v^2\,\eta_c\,V_{dd}}(g_m R_{in} + 2\Gamma_n)\right). \tag{2.27}$$

It can be seen from (2.27) that there is an optimum $g_m R_{in}$ which result in minimum $E_{tot,CT}$. The Γ_n is quite dominant as expected. The $\frac{V_{gt}}{\eta_v^2\,\eta_c\,V_{dd}}$ part again appears, similar to (2.16).

If an inverter-based amplifier is used ($\eta_c = 2$), and the input voltage swing is maximized ($\eta_v = 1$), and the excess noise is minimized ($\Gamma_n = 1$), (2.25) becomes:

$$E_{tot,CT} = 8kT\ \text{SNR}\,(g_m R_{in} + 2)\left(\frac{1}{g_m R_{in}} + \frac{V_{gt}}{V_{dd}}\right) \tag{2.28}$$

The optimum $g_m R_{in}$ is then found as:

$$g_m R_{in} = \sqrt{\frac{2V_{dd}}{V_{gt}}}. \tag{2.29}$$

$g_m R_{in}$ should be chosen according to (2.29) for the lowest $E_{tot,CT}$. However, $g_m R_{in}$ is often defined by linearity requirements as expressed in (2.23) for high resolution and high linearity CTDSMs as determined in Section 2.4.2. This is the main source of excess energy consumption in such CTDSMs.

The minimum energy required for a CTDSM can then be found by using (2.29) in (2.28) and assuming $\frac{V_{gt}}{V_{dd}} \ll 1$. The result is again:

$$E_{min,CT} = 8kT\ \text{SNR} \tag{2.30}$$

which is equal to (2.21) for $\eta_P = 1$. The energy consumption when $g_m R_{in}$ is determined by linearity requirements, which can be defined by a certain HD3 level, is found by using (2.23) in (2.28), and assuming $V_{FS} = V_{dd}$ to be:

$$E_{tot,CT} = 8kT\ \text{SNR}\left(1 + \frac{1}{2^N}\sqrt[3]{\frac{2\lambda\,V_{dd}^2}{\text{HD3}}}\,\frac{V_{gt}}{V_{dd}}\right). \tag{2.31}$$

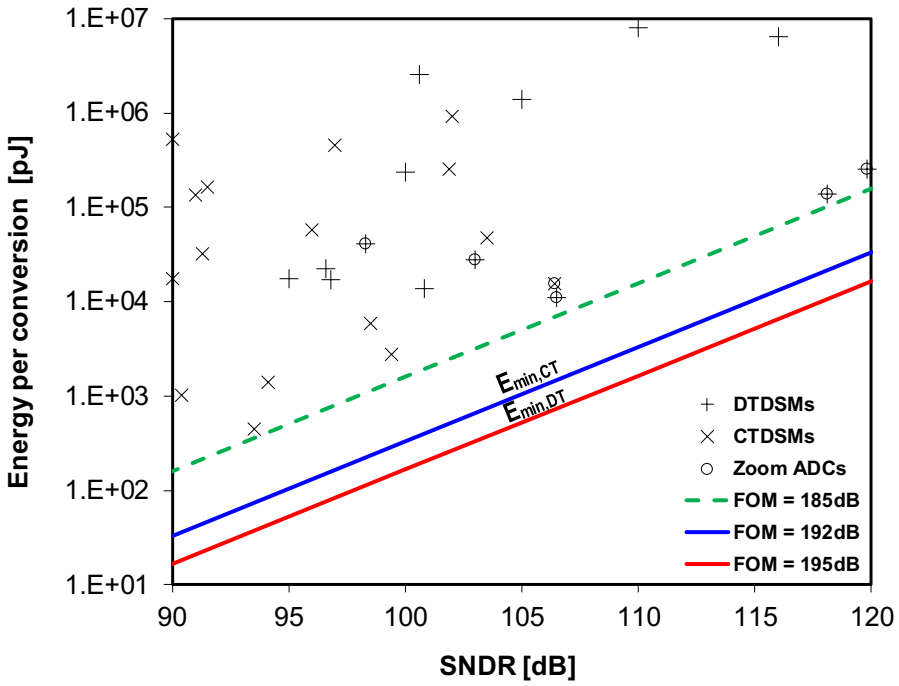

Figure 2.6: SNDR vs Energy per conversion for state-of-the-art high resolution ADCs and low energy bounds found for DTDSMs and CTDSMs in (2.19) and (2.30) respectively [14].

2.5 Energy Efficiency of the State-of-the-Art DSMs and Zoom ADCs

In the analysis above it is found that the thermal-noise limited energy per conversion for DTDSMs and CTDSMs in (2.3) and (2.21), respectively. It is shown that the power consumption of a single-stage OTA is dependent on several factors related to amplifier efficiency such as Γ_n, voltage efficiency (η_v), current efficiency (η_c), and also g_m nonlinearity. It is observed that, even though the amplifier can be optimized at the circuit level to have high efficiency, its nonlinearity would result in excess energy consumption for high SNDR designs. When amplifier nonliearity is taken into account, the total energy per conversion of DTDSMs and CTDSMs is given by (2.18) and (2.31), respectively. These are related to HD3, which is often the dominating error source for high SNDR ADCs.

When efficient amplifiers are used, and nonlinearity is negligible, i.e. when the input swing of the loop filter is very small, the lower limits of energy consumption of DTDSMs and CTDSMs are given in (2.19) and (2.30) respectively. These lower limits, corresponding to 195 dB and 192 dB figure-of-merit (FOM)[6] respectively, are plotted in Fig. 2.6 together with

[6]FOM $=$ DR $+ 10\log($Signal bandwidth $/$ Power$)$ is defined in [10].

the energy consumption of state-of-the-art high resolution DTDSMs and CTDSMs published between 1997-2020 [14]. Note that in Fig. 2.6, SNR is assumed to be equal to SNDR, which assumes that the distortion is negligible. In practice though, this is not the case, resulting in excess energy consumption. The trend-line of the current state of the art is equivalent to 185 dB FOM[7]. This means that state-of-the-art designs consume almost 10 times more energy than the theoretical minimum.

It is seen from Fig. 2.6 that zoom ADCs are at the current state-of-the-art. However, their energy consumption is still far from the theoretical minimum. As it is proposed above, this gap for a large part can be explained when taking the circuit nonlinearity into account. Since the necessary data about their design details are readily available, it to would be intresting to compare their actual energy consumption to the predicted energy consumption by using (2.18) and (2.31).

All of these state-of-the-art zoom ADCs use inverter-based current-reuse amplifiers [4–6, 15, 16], which means $\Gamma_n = 1$ and $\eta_c = 2$. Most of the designs use 5-bit quantization ($N = 5$) and their input voltage range is optimized ($\eta_v = 1$). The input transistors of the amplifiers are in weak inversion ($V_{gt} = 80\ mV$), and the V_{dd} of the process is $1.8\ V$. The g_m nonlinearity of amplifier input stages is analyzed in Appendix D. From this, $\lambda = 50$ is found for an inverter-based pseudo-differential amplifier design in weak inversion for the process technology used in this thesis. By using these parameters, and assuming the noise and the harmonic distortion powers to be equal, the energy consumption can be estimated from (2.18) and (2.31) for zoom ADCs with DT and CT DSMs respectively. These are shown in Fig. 2.7 together with the actual energy consumption of the designs. Our analysis captures an important part of excess energy consumption due to nonlinearity and makes a more accurate estimation of energy consumption in spite of being limited to the energy consumed by the first stage only. This helps the designer to identify the system and circuit level trade-offs, minimize the energy consumption while not compromising the performance.

[7] 185 dB FOM is roughly equal to $38kT$ SNR.

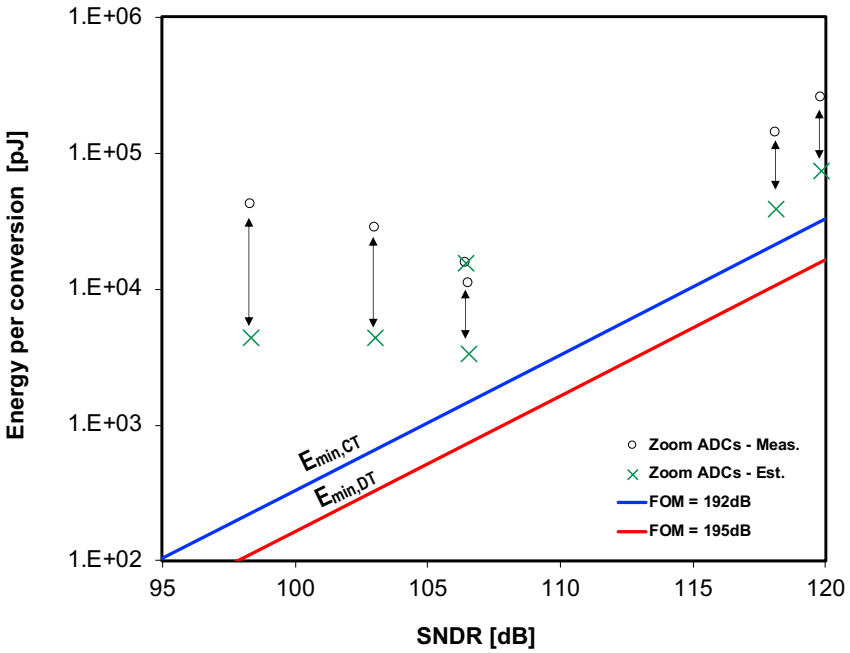

Figure 2.7: SNDR vs measured and estimated energy consumption for published zoom ADCs.

2.6 Comparison of the Energy Efficiency of High Linearity DTDSMs and CTDSMs

When considering the excess energy consumption due to nonlinearity, the interesting observation can be made that the effect of g_m on linearity for DTDSMs and CTDSMs is considerably different. To demonstrate this, let us find the g_m necessary for a certain HD3 by rewriting (2.14) by using $n_\tau = \frac{g_m}{2 f_s C_s}$:

$$g_m = 2 f_s C_s \left(\ln \left(\frac{\lambda \, \eta_v^2 V_{FS}^2}{\mathrm{HD3}} \right) - (3N+1) \ln 2 \right). \tag{2.32}$$

The same can be achieved for a CTDSM by using (2.23), resulting in:

$$g_m = \frac{1}{R_{in}} \left(\frac{1}{2^N} \sqrt[3]{\frac{2 \lambda \, \eta_v^2 \, V_{FS}^2}{\mathrm{HD3}}} - 2 \right). \tag{2.33}$$

As seen from (2.32) and (2.33) the relation of g_m and HD3 is logarithmic for a DTDSM while it is cubic for a CTDSM. As will be demonstrated later, this means that for high linearity requirements, a DTDSM is more energy-efficient than a CTDSM.

To demonstrate this, 3^{rd}-order 1-bit DT and CT modulators with the input stages shown

in Fig. 2.2 and Fig. 2.5 were simulated. They were designed to have the SNR of 108 dB, and OSR = 128. The g_m of their first stage amplifier, which had a nonlinearity factor $\lambda = 0.1$[8], was then swept[9]. The input resistor of the CTDSM (R_{in}) is found to be 8 kΩ for the full-scale input range of 1.8 V by assuming $\frac{1}{g_m} \ll R_{in}$, and $\Gamma_n = 1$ by using the analysis in Appendix A. The sampling capacitance of the DTDSM (C_s) is found to be 12.2 pF, which is chosen by using the same analysis with the same assumptions. The integration capacitances were 24.4 pF and 12.2 pF for the CT and the DT modulators respectively.

A single-tone sinusoidal input with 0.35 V amplitude at 1 kHz is applied to both modulators and the simulated HD3 results are shown in Fig. 2.8 together with the estimated values obtained from (2.12) and (2.22) for different g_m values. Note that for the same g_m, the given R_{in} and C_s values result in the same $g_m R_{in}$ and n_τ shown in Fig. 2.8, making it easy to compare (2.12) and (2.22). It is expected from (2.32) that the HD3 of the DTDSM will improve exponentially with increased g_m. Similarly, the HD3 of the CTDSM will improve cubically with increased g_m for a fixed R_{in} according to (2.33). From Fig. 2.8 it is clear that for high linearity levels (HD3 < -90 dB) the DTDSM requires much less g_m, hence its first stage amplifier consumes much less energy, which is in line with our prediction. The saturation of the HD3 below -140 dB for the DTDSM is due to quantization noise level at the harmonic frequency.

The n_τ and $g_m R_{in}$ values for a certain HD3 level can be extracted from Fig. 2.8 and used in (2.17) and (2.25) to calculate the energy per conversion for each modulator. This is illustrated in Fig. 2.9 for the simulated modulators in terms of E_{min} given in (2.1). Note that for HD3 > -110 dB the CTDSM's E_{tot} is limited to its minimum value determined in (2.29). Below this level (HD3 < -110 dB), $g_m R_{in}$ is increased further than its optimum value due to higher linearity requirements, hence E_{tot} is increased. The same can be seen for the DTDSM, where its n_τ is limited to 2 higher than -70 dB HD3 due to increased noise below this point as given in (2.18).

It is noted that the DTDSM always consumes less energy per conversion than the CTDSM. There are two reasons for this. Firstly, reusing the sampling capacitance as the DAC results in a much smaller loading to the amplifier to achieve the same thermal noise. This establishes the difference in E_{tot} for a high HD3 (> -110 dB). Secondly, the HD3 $\propto e^{-g_m}$ for the DTDSM, and HD3 $\propto \frac{1}{g_m^3}$ for the CTDSM where the former is much stronger function than the latter. This is the reason behind the difference for low HD3 levels (< -110 dB). In practice, however, the DTDSM will require much stronger input and reference drivers. Although these often

[8]Since the simulation setup uses ideal circuit components, a small λ had to be chosen to avoid convergence errors during the simulation.

[9]The loop-filter order, SNR and OSR values are chosen to be compatible the implementations presented in Chapter 4 and Chapter 6.

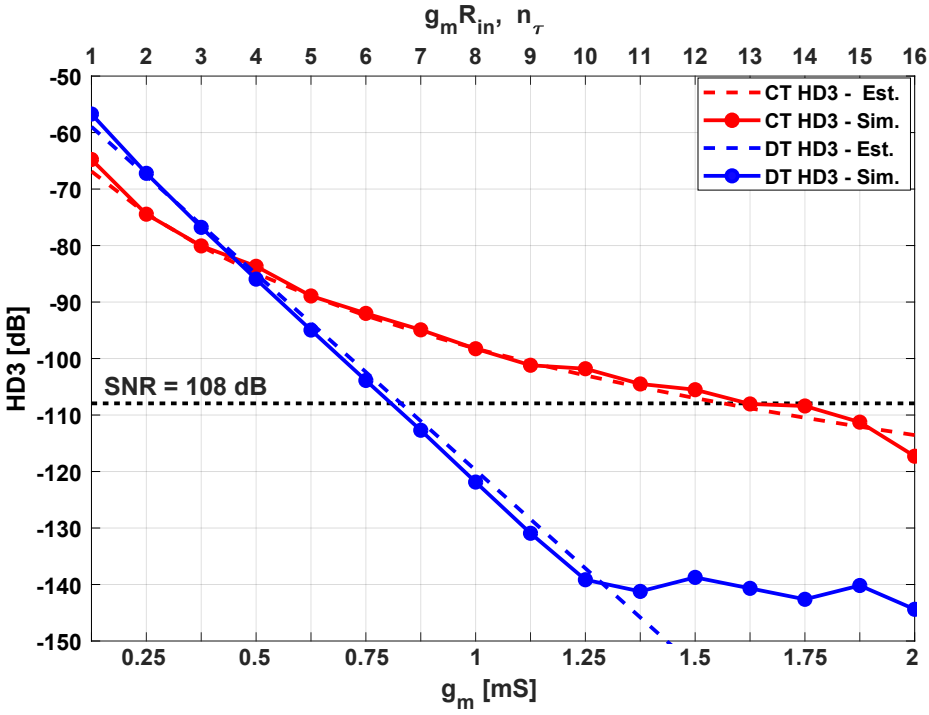

Figure 2.8: g_m vs HD3 for the simulated DT and CT modulators. $g_m R_{in}$ and n_τ values are also given.

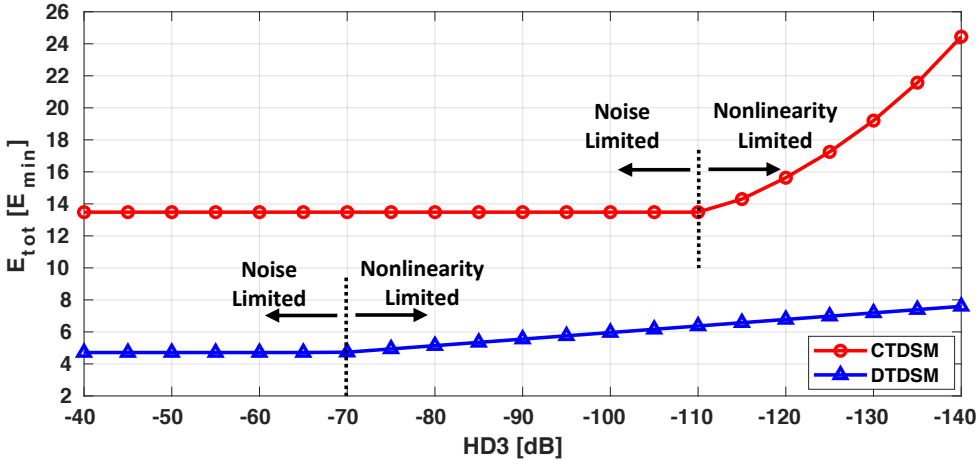

Figure 2.9: Estimated E_{tot} of the simulated DT and the CT modulators.

consume more energy than the first stage of a DTDSM [17], they are usually not reported [14].

2.7 Loop Filter Input Swing Reduction

It is found in Section 2.3.2 and Section 2.4.2 that increasing N helps to reduce the amplifier nonlinearity related distortion $\left(\text{HD3} \propto \frac{1}{2^{3N}}\right)$ due to the reduced loop-filter input swing. Thus, increasing N not only helps to mitigate HD3, but also reduces the quantization noise fold-back due to amplifier nonlinearity by reducing both the distortion and the quantization noise themselves [10]. Since increasing N would reduce quantization noise, f_s can be lowered to achieve the same performance. Both the DT and CT modulators benefit from a reduced f_s as the switching energy of the digital circuits, comparators, and switches are linearly related to f_s. Increasing N can be achieved through multi-bit quantization [12], by filtering the DAC feedback signal [18], or by zooming [5].

Multi-bit quantization is the most conventional approach to reach a higher N. Each bit added to the quantizer will reduce the loop-filter input swing by $2\times$. Reduced quantization noise will also result in the additional benefits of better loop stability, increased stable input range, and a more relaxed decimation filter implementation [10]. The biggest drawback of this approach is that the linearity of the modulator is now limited by the unit element matching of the multi-bit DAC. This can be solved by utilizing a dynamic element matching (DEM) scheme. This, on the other hand, comes at the cost of additional digital power consumption and delay in the feedback loop. A multi-bit quantizer in the loop must also meet stringent requirements, since its non-linearity can degrade performance, and its delay will cause excess loop-delay (ELD) [10]. The latter is especially problematic for CTDSMs. For these reasons, the multi-bit quantizer is often implemented as a flash ADC. However, a flash ADC is not an efficient quantizer because of the exponential rise in the number of comparators with N. Using a SAR ADC together with ELD compensation is a promising way to improve the efficiency of the multi-bit DSMs [19–21].

Filtering the quantization noise in the feedback signal is another architectural solution to reduce the input error swing. This can be accomplished with an finite-impulse-response (FIR) filter as shown in Fig. 2.10 [18, 22, 23]. Filtering the quantization noise will make the loop filter input swing smaller by effectively filtering the shaped quantization noise. It will also reduce the modulator's jitter sensitivity due to the reduced amount of quantization noise in the feedback. Thus, the swing and jitter performance will be similar to that of a multi-bit modulator without using a multi-bit quantizer or DEM. The FIR filter can be implemented

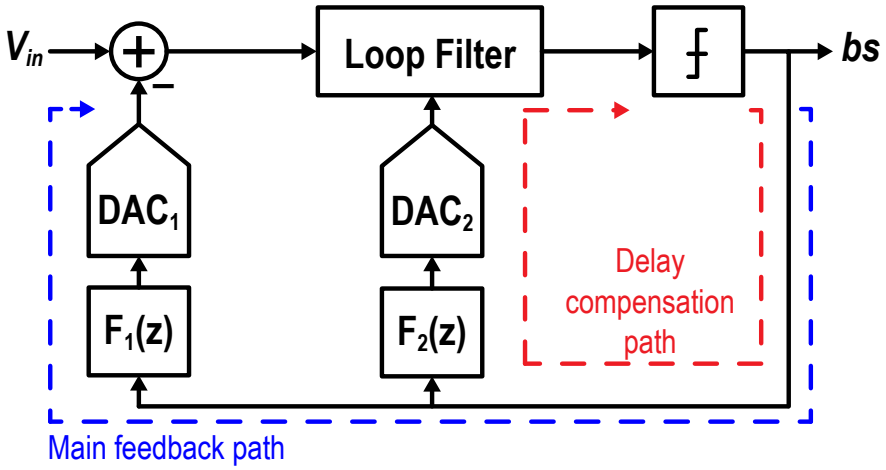

Figure 2.10: A DSM with an FIR filter incorporated in its feedback.

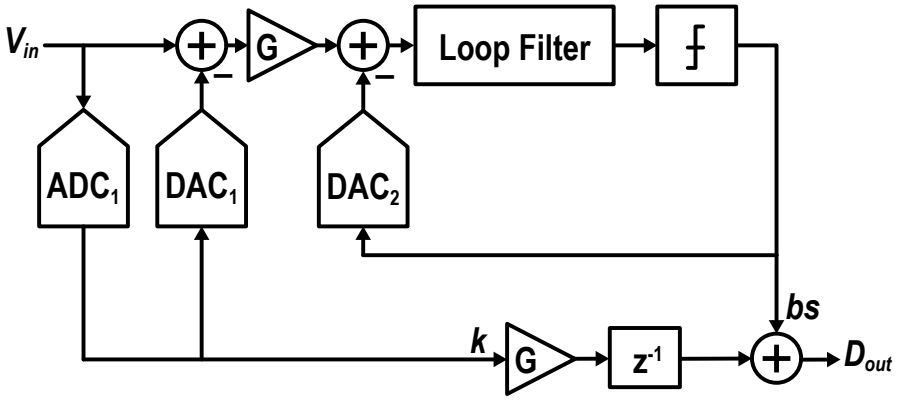

Figure 2.11: Simplified block diagram of a $0-N$ MASH ADC.

fully in digital, which requires a multi-bit DAC in the feedback, or integrated in the DAC by using multiple 1-bit DAC units to implement each coefficient of the FIR filter. The latter, dubbed as FIR-DAC, does not have stringent DAC unit matching problems that multi-bit DACs have. Although these properties make feedback filtering architectures very attractive, they still require a faster path to compensate for the delay induced by the FIR filter as shown in Fig. 2.10. Furthermore, the increased delay in the FIR filter means that their swing reduction saturates at around 12-taps [18]. A recently reported combination of multi-level quantization and FIR filtering relaxes this limitation with added complexity of DEM [24].

A possible way to avoid the problems of incorporating a multi-bit quantizer or filtering the quantization noise in the loop is to have a multi-bit quantizer outside the DSM loop. This is achieved by the so-called $0-N$ multistage noise shaping (MASH) architecture proposed

in [25], which uses a two-step structure with a coarse multi-bit quantizer and a fine DSM as shown in Fig. 2.11. However, as in any two-step ADC, the matching between the fine and coarse ADCs needs to be better than the desired overall accuracy of the ADC. If no over-ranging is used, ADC1, DAC1 and DAC2 will have very strict matching requirements. Similarly, the gain between the coarse quantizer, and the fine DSM (G) must be accurate. This architecture has been used in wide-band CTDSMs later in [26, 27]. These implementations needed calibration to achieve maximum accuracy.

2.8 Zoom ADC

The zoom ADC architecture has been proposed for high resolution and high linearity applications, for which it achieves excellent energy efficiency [4–6, 15, 16]. A system block diagram of a zoom ADC is shown in Fig. 2.12. It consists of a coarse ADC and a fine DSM. The coarse ADC's output (k) corresponds to an analog range $k \cdot V_{LSB,C} < V_{in} < (k+1) \cdot V_{LSB,C}$ where $V_{LSB,C}$ is the quantization step or the least significant bit (LSB) of the coarse ADC. The digital value k is then used to adjust, i.e., "zoom in," the references of the DSM's DAC such that $V_{REF-} = k \cdot V_{LSB,C}$ and $V_{REF+} = (k+1) \cdot V_{LSB,C}$. These reference voltages straddle the input signal V_{in}, thus ensuring that it lies in the input range of the fine DSM. By using a wider fine input range, similar to over-ranging in two-step ADCs [28], the coarse converter's linearity and accuracy is considerably relaxed. The overall linearity is determined by the fine DSM, in particular by its DAC, the linearity of which is then improved by DEM. Compared to multi-bit and the 0-N MASH DSMs, the zoom ADC improves efficiency by relaxing the specifications of both its coarse ADC and fine DSM. The coarse ADC can be implemented as an efficient SAR ADC, as its matching requirements are more relaxed than the quantizer of a multi-bit DSM due to over-ranging. The input swing of the DSM is reduced such that its power consumption can be minimized. Compared to the FIR-DAC based DSMs it does not require an ELD compensation path.

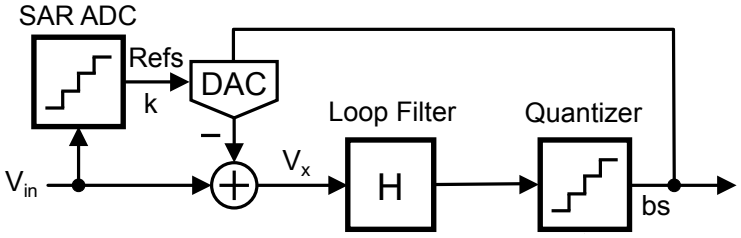

Figure 2.12: Block diagram of a zoom ADC

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Chapter 3

The Zoom ADC

In Chapter 2, reducing the loop filter's input swing was found to be the most important way to improve the energy efficiency of a high-resolution ADC. Conventionally, this has been achieved by the use of multi-bit DSMs, but, as will be shown, the use of a zoom ADC is an even better approach. When compared at the system-level, both architectures use the same building blocks: a loop filter, a multi-bit ADC, and a multi-bit DAC with dynamic element matching (DEM). However, the critical difference is that in a multi-bit DSM the multi-bit (coarse) ADC is in the loop, while in a zoom ADC it is outside the loop.

Putting the coarse ADC inside the loop of a multi-bit DSM places more stringent demands on its performance. First, it must be fast enough to avoid adding additional delay in the loop. This often requires the use of a power-hungry flash ADC [1, 2]. Even when a more efficient ADC is used, it must still be designed for speed. Secondly, its mismatch requirements are quite stringent, and can significantly degrade the performance of the overall DSM [2, 3].

In a zoom ADC, the use of over-ranging greatly relaxes the requirements on the coarse ADC. This comes at a cost of a slightly reduced SQNR when a 1-bit fine DSM is used. This can be compensated for by a slight increase in sampling frequency or by employing a 2-bit ADC [4]. As a result, the design of the coarse ADC is quite relaxed, leading to significant improvements in its area and energy efficiency.

One disadvantage of the first zoom ADCs was that they had a severe limit on the maximum input signal frequency [5]. This shortcoming is resolved by the dynamic zoom ADC proposed in this thesis [4, 6–8]. Another problem faced by zoom ADCs is leakage of the coarse ADC quantization noise due to the non-unity STF of the DSM [4, 7]. This is also addressed in this thesis.

In this chapter, the system-level design of zoom ADCs is explored. In Section 3.1, the

zoom ADC architecture is explained. Section 3.2 describes the static error sources in a zoom ADC and some methods to alleviate their impact. In Section 3.3, the dynamic errors are discussed.

3.1 Zoom ADC Architecture

A block diagram of a dynamic zoom ADC is shown in Fig. 3.1. It consists of a coarse ADC and a fine DSM working concurrently. A schematic representation of the coarse ADC's quantization levels and their relation to the zoomed-in references of the DSM's DAC is shown in Fig. 3.2.a. The output of the coarse ADC (k) is found such that:

$$d_{C,k}V_{LSB,C} < V_{in} < d_{C,k+1}V_{LSB,C} \tag{3.1}$$

where $d_{C,i}$ is the i^{th} coarse quantization step (from 1 to 2^{N-1}), and $V_{LSB,C}$ is the quantization step, or the least significant bit (LSB) of the coarse ADC expressed as:

$$V_{LSB,C} = \frac{V_{REF}}{2^{N-1}}. \tag{3.2}$$

The digital value k is then processed to dynamically adjust the references of the fine DAC such that:

$$V_{REF,DSM-} = d_{F,k}V_{LSB,C} \tag{3.3}$$

$$V_{REF,DSM+} = d_{F,k+1}V_{LSB,C} \tag{3.4}$$

where $d_{F,i}$ is the i^{th} DAC step. Note that, ideally $d_{C,i} = d_{F,i}$. These reference voltages straddle V_{in}, ensuring that it lies within the input range of the fine DSM. Due to zooming, the input of the loop filter (V_x in Fig. 3.1) is much smaller than V_{in}, and so its first stage linearity requirements are relaxed.

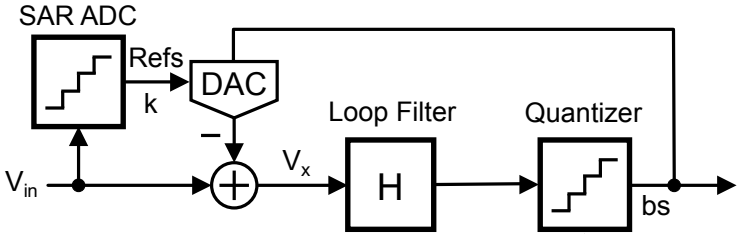

Figure 3.1: The system level block diagram of a zoom ADC.

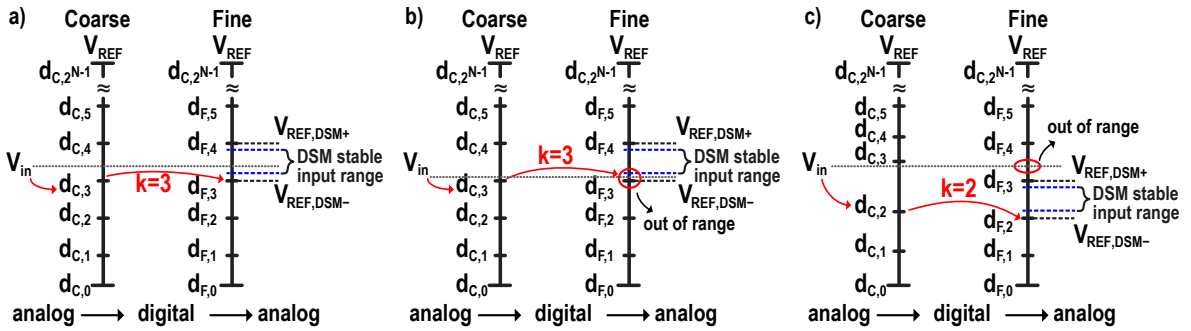

Figure 3.2: Chosen quantization levels and references of the fine DSM when the coarse ADC outputs $k = 3$. a) Ideal situation. b) V_{in} is close to one of the coarse quantization levels, and outside the stable input range of the DSM. c) Different coarse ADC quantization levels cause errors in the chosen references ($k = 2$) of the DSM.

3.2 Static Errors

As shown in Fig. 3.2.b, if V_{in} is very close to one of the chosen references, i.e. $V_{in} \approx V_{REF,DSM+}$ or $V_{in} \approx V_{REF,DSM-}$, then it might be outside the DSM's stable input range. Moreover, the coarse and fine quantization levels will not be equal in practice, i.e. $d_{C,i} \neq d_{F,i}$. As shown in Fig. 3.2.c, such differences may also cause V_{in} to fall outside the DSM's stable input range. With no loss of generality, we can assume that the fine quantization levels ($d_{F,i}$) are ideal, and only the coarse quantization levels ($d_{C,i}$) exhibit error. In Fig. 3.2.c, $d_{C,i}$ are shifted with respect to $d_{F,i}$, resulting in a large error due to the invalid fine conversion. This can be seen in more detail in Fig. 3.3.a and Fig. 3.3.b , which show the input of the loop filter (V_x) for ideal and mismatched coarse quantization levels, respectively. Even if the coarse ADC is ideal, the fine conversion might still be invalid due to the DSM's limited stable-input range (Fig. 3.3.a). Additional errors will only corrupt the fine conversion further, as can be seen in Fig. 3.3.b.

3.2.1 Over-ranging

The DSM's input range can be widened by using over-ranging, as is often done in traditional two-step ADCs [9], by choosing the following DAC references:

$$V_{REF,DSM-} = (d_{F,k} - M)V_{LSB,C} \tag{3.5}$$

$$V_{REF,DSM+} = (d_{F,k+1} + M)V_{LSB,C} \tag{3.6}$$

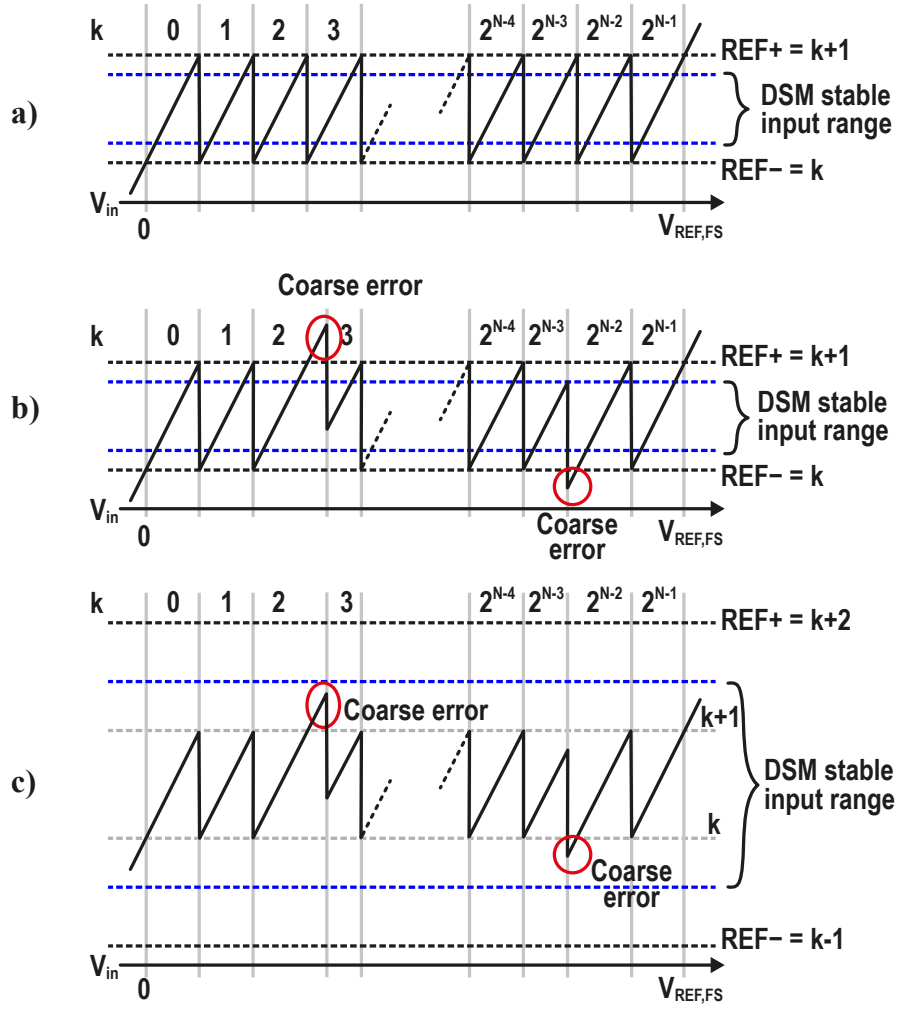

Figure 3.3: Input of the DSM for various input voltages V_{in} with a) an ideal coarse ADC and references chosen by the DAC, b) non-ideal coarse quantization levels yielding an error in the chosen references, c) over-ranging ($M = 1$) causing the input value to be within the range of the chosen references.

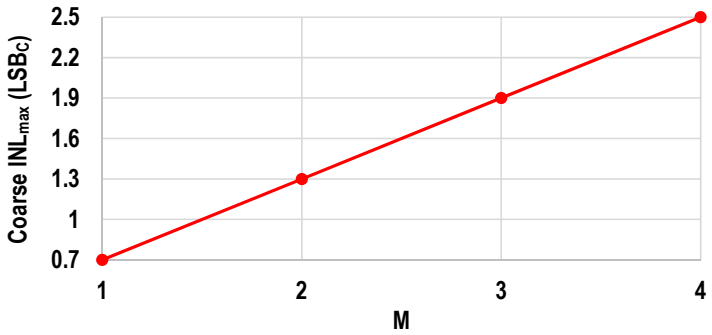

Figure 3.4: Maximum INL of the coarse ADC which results in less than 10 dB SQNR degradation for different M values.

where M is the over-ranging factor. This can be easily implemented by simply adding and subtracting an integer value, i.e. $\pm M$ to the output of the coarse ADC before adjusting the references of the fine ADC. Fig. 3.3.c gives an example of over-ranging with $M = 1$ in the presence of the same mismatch as in Fig. 3.3.b. The chosen references now correctly straddle V_{in} even in the presence of coarse conversion errors. Furthermore, over-ranging also prevents errors due to the limited stable input range of the DSM.

With over-ranging, the coarse ADC can be simply realized as a SAR ADC[1]. These are both area and power efficient and so are used in the zoom ADC implementations presented in Chapters 4 - 6. For design purposes, it is then of interest to understand the trade-off between the integral non-linearity (INL) of the coarse ADC and the over-ranging factor. Fig. 3.4 shows the maximum acceptable INL for different M values for zoom ADCs with 4- to 6-bit coarse ADCs. Each design employs a 3^{rd}-order 1-bit DSM with out-of-band gain (OBG) = 1.5 and oversampling ratio (OSR) = 128. Each data point represents a 100-point Monte Carlo simulation, and the INL that degrades the SNR by 10 dB was noted. The 10 dB criterion is chosen because it is large enough to allow the impact of coarse ADC INL to be reliably estimated. The maximum tolerable INL in Fig. 3.4 is normalized to the coarse LSB ($\mathrm{LSB_C}$). Note that the relative matching of the unit elements increases quadratically for each coarse bit, i.e. from 5- to 6-bit, due to the smaller size of their $\mathrm{LSB_C}$. As seen in Fig. 3.4, the maximum acceptable INL error increases proportionally with M, thus allowing the coarse ADC's accuracy requirements to be relaxed.

3.2.2 Gain Error and STF

The errors in a zoom ADC are similar to those in the $0-N$ MASH ADC shown in Fig. 3.5 , thus this model can be used for analysis. The quantization error of the coarse converter is q_C, and its other errors are represented by e_C. These errors will be digitized and will affect the coarse output code such that:

$$k = V_{in} + q_C + e_C. \tag{3.7}$$

Assuming $M = 0$, the output of the fine ADC then becomes:

$$bs' = -(1+\Delta g)\,(q_C + e_C + e_{D1})\,\mathrm{STF} - (\mathrm{e_{D2}\ STF}) + (e_F\ \mathrm{STF}) + (q_F\ \mathrm{NTF}) \tag{3.8}$$

[1] In a static zoom ADC, the coarse conversion could be done using the DSM in an incremental ADC fashion. This would save area due to hardware sharing [10, 11]. Another way to save area is to use the DAC and the comparator of the DSM to implement the coarse SAR ADC [5].

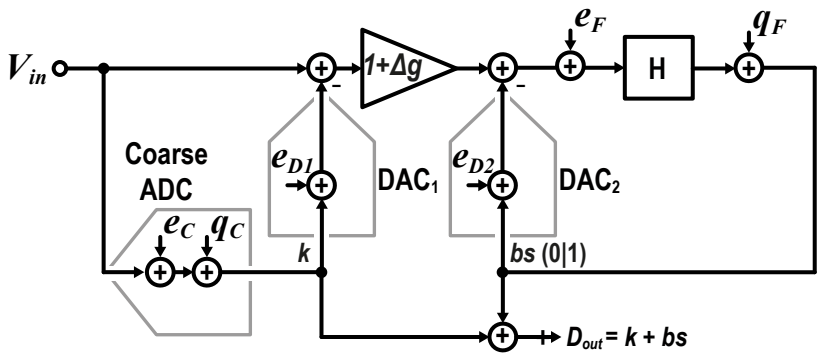

Figure 3.5: System level block diagram of a $0-N$ MASH ADC.

where Δg is the gain error between the coarse and the fine DACs, q_F is the quantization error of the DSM, e_F represents its other input-referred errors, $\text{STF} = \frac{H}{1+H}$ is the signal transfer function of the DSM, $\text{NTF} = \frac{1}{1+H}$ is the noise transfer function of the DSM, and e_{D1} and e_{D2} are the errors introduced by DAC_1 and DAC_2, respectively. The combined digital output of the zoom ADC can be found by adding (3.7) and (3.8):

$$D_{out} = V_{in} + (q_C + e_C)(1 - \text{STF} - \Delta g) + (q_F\ \text{NTF}) - ((1+\Delta g)e_{D1} + e_{D2} - e_F)\,\text{STF}. \quad (3.9)$$

As (3.9) indicates, any gain error between the coarse and fine paths will cause the coarse ADC errors to leak into the output, including quantization error. Since a low-resolution coarse converter is used, its quantization error will be much larger than the desired resolution of the zoom ADC. Thus, even a small gain error will significantly degrade the overall performance.

There are two types of gain error in a zoom ADC: the mismatch between DAC_1 and DAC_2 (Δg), and the non-unity STF of the fine DSM. These will be investigated in the following sections. If there is no gain error ($\Delta g = 0$ and $\text{STF} = 1$), (3.9) simplifies to:

$$D_{out} = V_{in} + q_F\,\text{NTF} - e_{D2} - e_{D1} \quad (3.10)$$

It can be seen that if the fine conversion is valid, and there is no gain error, the overall ADC will be tolerant to errors in the coarse ADC, but the errors introduced by DAC_1 and DAC_2 will appear at the output.

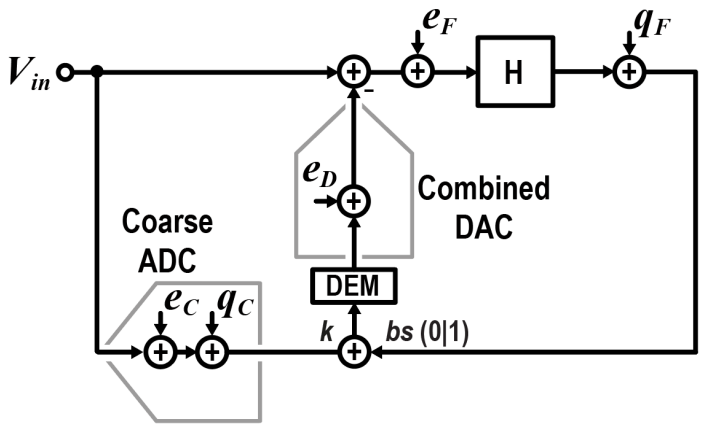

Figure 3.6: System level block diagram of a zoom ADC.

3.2.3 DAC Mismatch Errors and Dynamic Element Matching

The gain error between DAC_1 and DAC_2 (Δg in Fig. 3.5) is conventionally addressed by trimming or calibration [12–14]. These either complicate the system when high resolution is desired. In a zoom ADC, however, none of these approaches is used. Instead, as shown in Fig. 3.6, these two DACs are merged into one, thus eliminating their mismatch and the resulting gain error. The output of the zoom ADC still includes the error introduced by the combined DAC's unit mismatch (e_D), the shaped DSM quantization noise, and the other input-referred errors of the DSM (e_F):

$$D_{out} = V_{in} + q_F \mathrm{NTF} - e_D + e_F. \tag{3.11}$$

DAC unit mismatch would make e_D a significant error source. Once more, this can be corrected by calibration or trimming, e.g. by employing wafer-level laser trimming [15]. However, laser-trimmed DACs still suffer from post-trim errors due to aging, drift, or packaging stress. Background or foreground analog calibration techniques can circumvent such errors, but both require calibration circuits and analog redundancy, usually resulting in an area penalty [15]. Digital look-up tables (LUTs) can be used instead of analog calibration circuitry to correct for static DAC errors [16]. Such errors corrupt the feedback signal going into the loop filter, hence the DSM's output (D_{out}) includes these errors (e_D) as given in (3.11). If the unit DAC errors are measured and added to D_{out}, the error term e_D can be removed. The DAC errors need to be accurately measured for both analog and digital calibration schemes, and this needs to be repeated often in case the error changes over time. The required measurement accuracy is quite high; hence it adds a lot of extra complexity, making calibration undesirable for most applications.

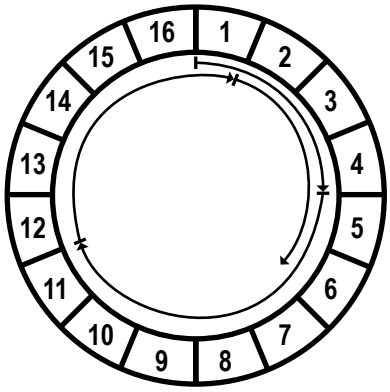

Figure 3.7: Rotational unit selection of DWA for the sequence $\{4,7,6,5\}$

Dynamic element matching (DEM) is a better option. It involves swapping DAC unit elements so as to modulate DAC unit mismatch errors to higher frequencies such that they can be filtered out later [17, 18]. The advantage of DEM is that it requires no prior knowledge, or measurement, of mismatch error to correct for it. Different DEM algorithms have been invented such as randomization [19], individual level averaging [20], and data weighted averaging (DWA) [21]. DWA is widely used in high resolution DSMs because of its simple algorithm, which is well suited for digital implementation, and its efficacy in converting static mismatch errors into a high-pass shaped noise-like signal.

DWA is based on a unary DAC with rotational unit selection, as shown in Fig. 3.7 for the case of an 8-unit DAC and an output sequence of $\{4,7,6,5\}$. Here, the elements to be used at the current clock cycle are selected by starting from the first unused element of the previous clock cycle. When the end of the array is reached, the selected units wrap around. In this way, a difference of the DAC mismatch error of the consecutive cycles is achieved such that the error after DWA has a high-pass spectral shape. However, DWA can cause tones due to its rotational operation, especially for small input signals [3]. This can be solved with dithering, i.e. adding randomization into the selection scheme.

DWA introduces 1^{st}-order shaped in-band noise as shown in Fig. 3.8 for a zoom ADC with a 5-bit coarse ADC and a 3^{rd}-order 1-bit DSM with an OSR of 128 and 1% DAC unit mismatch. Due to the residual errors of DWA, the in-band SNR of the ADC degrades from an ideal value of about 122 dB to 118 dB. Thus, DWA limits SNR, which is more severe for higher OSRs, especially for DSM's with higher-order noise shaping. Thus, it is important to understand the parameters which determined the residual errors of DWA.

A simple estimation of the in-band error due to DWA is derived in [18], which can be used to estimate the resulting SNR_{DWA}:

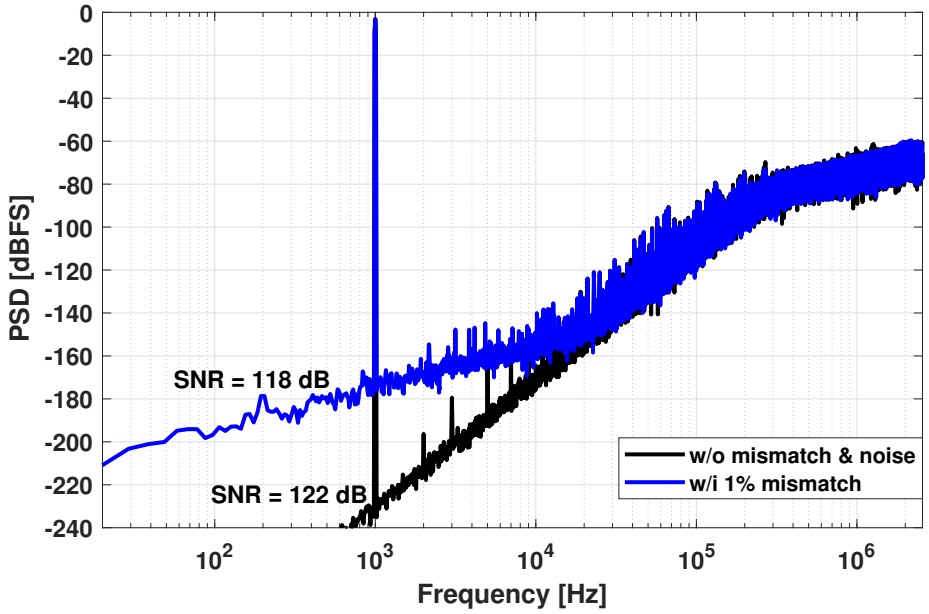

Figure 3.8: Output spectrum of a zoom ADC showing the effect of the DWA induced noise.

$$\mathrm{SNR}_{\mathrm{DWA}} = \frac{9\,(2^N-1)\,\mathrm{OSR}^3}{8\pi^2\sigma_u^2} \tag{3.12}$$

where N is the number of DAC bits, and σ_u is the standard deviation of the DAC unit mismatch. Note that (3.12) is not very accurate as demonstrated in [3], but it reveals the relative importance of the design parameters. The actual value of $\mathrm{SNR}_{\mathrm{DWA}}$ must to be verified by simulation.

3.2.4 Non-unity STF

The gain error due to the non-unity STF of the fine DSM is a well-known problem in MASH converters [3]. In a DSM, a non-unity STF can be caused by limited open-loop gain, or by the choice of the loop filter. The former is often not a significant problem since the in-band open-loop gain of a high-order DSM can be quite high (> 120 dB), while the latter is a design choice. For example, in the case of a 2nd-order feed-forward compensated loop filter (Fig. 3.9.a), the resulting STF will exhibit some peaking, as is shown in Fig. 3.9.b. As discussed above, combining the two DACs and using DEM removes Δg in (3.9). The digital output of the zoom ADC then can be written as:

$$D_{out} = V_{in} + (q_C + e_C)(1 - \mathrm{STF}) + q_F\,\mathrm{NTF} + (e_F - e_D)\mathrm{STF}. \tag{3.13}$$

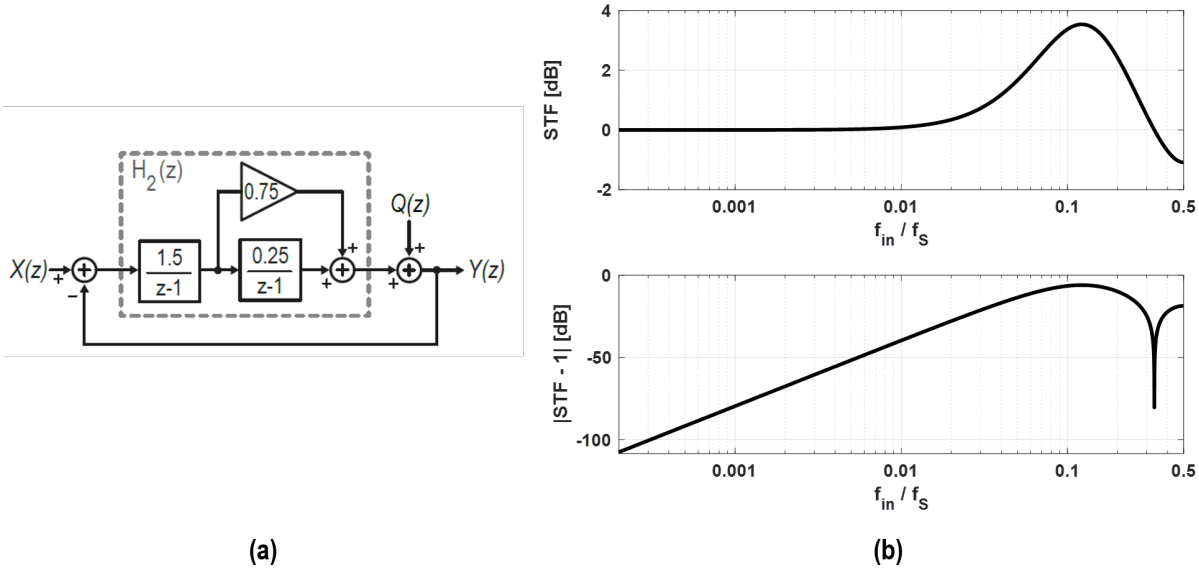

Figure 3.9: a) Example of a feed-forward compensated loop filter. b) Resulting STF and NTF.

It can be seen from (3.13) that a non-unity STF results in the leakage of both the quantization error (q_C) and the unit mismatch related errors (e_C) of the coarse ADC. Fig. 3.9.b shows this effect for the $2^{nd}-$order DSM shown in Fig. 3.9.a. Below the peaking frequency, i.e. $f_{in}/f_S < 0.1$, $|\text{STF}-1|$ rolls off with the order of the loop-filter, i.e. $40\,\text{dB}/\text{decade}$. This means that the error leakage will be highest at the signal band edge, and that low OSR and low order loop-filter implementations will suffer more.

For low resolution coarse ADCs, q_C is much larger than e_C. At less than 7-bit resolution, the energy of q_C will be concentrated at the harmonics of the input signal [14]. The result is some residual "fuzz" in the output spectrum of a zoom ADC. This is shown in Fig. 3.10.b for the zoom ADC of Fig. 3.10.a [7], whose coarse ADC is a 5-bit SAR ADC. Its peaking STF causes imperfect cancellation of q_C, resulting in the fuzz shown in Fig. 3.10.b. As in MASH architectures, this can be tackled with the help of a reconstruction filter in the digital domain [3]. As shown in Fig. 3.11.a, this involves passing the output code of the SAR ADC (k) through a digital filter matched to the STF before combining it with the bit-stream output. The result is almost perfect fuzz suppression, as shown in Fig. 3.11.b, although any mismatch between the analog STF and the reconstruction filter will degrade the fuzz suppression performance.

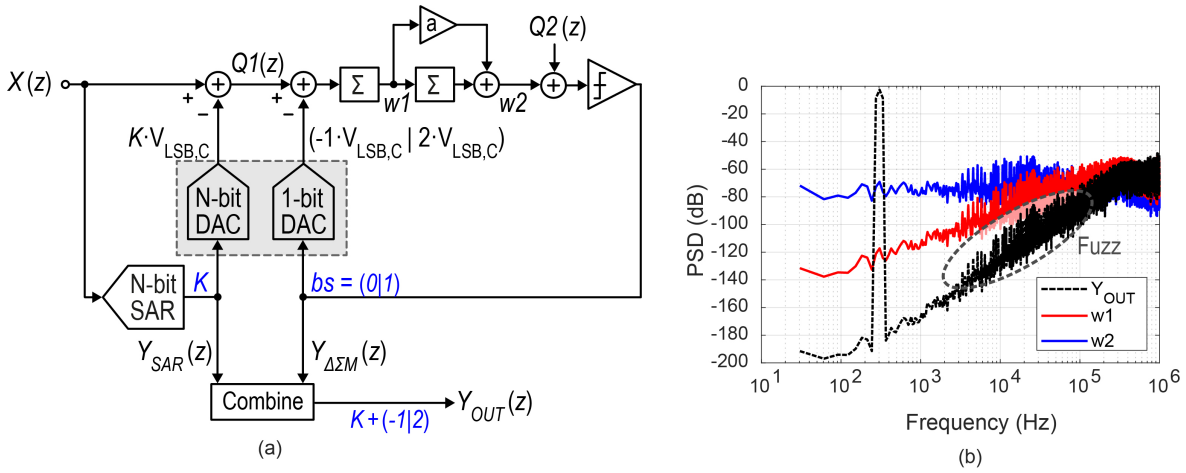

Figure 3.10: a) Intuitive block diagram of the zoom ADC described in [7] ($N = 5$ and $M = 1$). b) Spectrum at internal nodes of the loop filter and the zoom ADC's output.

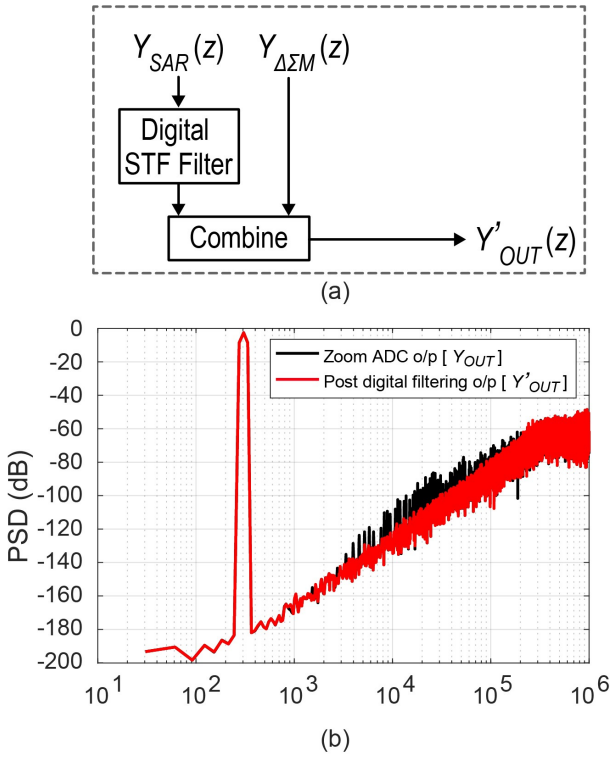

Figure 3.11: a) Fuzz filtering using a digitally matched STF filter. b) The resulting zoom ADC output spectrum.

Another way to address the non-unity STF issue is to design a loop filter with a unity STF. This can be achieved by using a loop filter with feed-back compensation, or by adding a direct feed-forward path from the input of the modulator to the input of the quantizer [3, 22, 23]. The

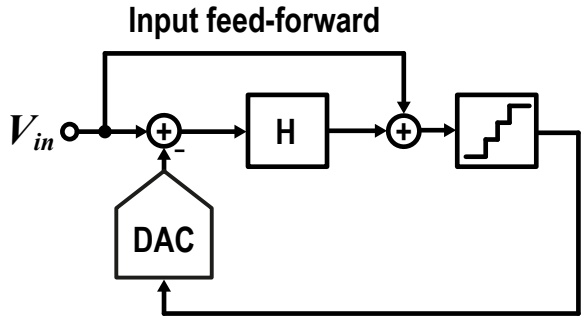

Figure 3.12: General input feed-forward DSM.

former results in large signal swings at the internal nodes of the loop-filter, which exacerbate the need for loop-filter linearity. The latter, shown in Fig. 3.12, also removes the signal related component in the loop, thus relaxing the need for loop-filter linearity. As shown in Fig. 3.6, assuming $q_C \gg e_C$, and $\Delta g = 0$, the input of the DSM in a zoom ADC is the quantization error of the coarse ADC (q_C). Thus, if q_C is fed-forward to the quantizer input, a unity STF will result and the out-of-band fuzz will be canceled completely.

In [4], the proposed coarse quantization noise feed-forward is implemented. The zoom ADC consists of a 5-bit coarse ADC and a 3^{rd}-order DSM with 2-bit quantizer. A replica of q_C is generated by subtracting an analog version of the output of the coarse ADC output (k) from the input (V_{in}), as shown in Fig. 3.13. The former is created by using a DAC, while the latter is established by a direct connection. This replica coarse quantization noise ($q_{C,replica}$) is then scaled down by the quantizer gain ($\frac{1}{G_q}$) in order to cancel the out-of-band fuzz. The simulated improvement achieved by this replica quantization noise feed-forward scheme can be seen in Fig. 3.14.a which corresponds to more than 10 dB improvement in in-band total harmonic distortion (THD). Measured improvement in THD, however, is limited to 7.4dB as shown in Fig. 3.14.b [4]. Compared to the results of simulations, the actual results are limited by the mismatch between the DAC of the SAR ADC and the DAC used to generate the replica quantization noise, and the gain inaccuracy of the feed-forward path.

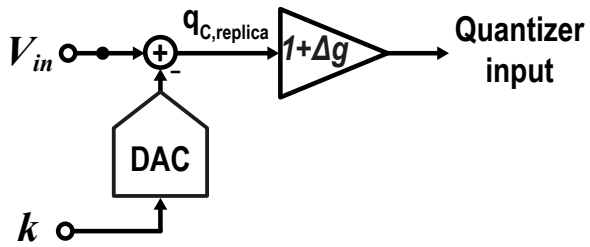

Figure 3.13: Replica coarse quantization noise feed-forward path.

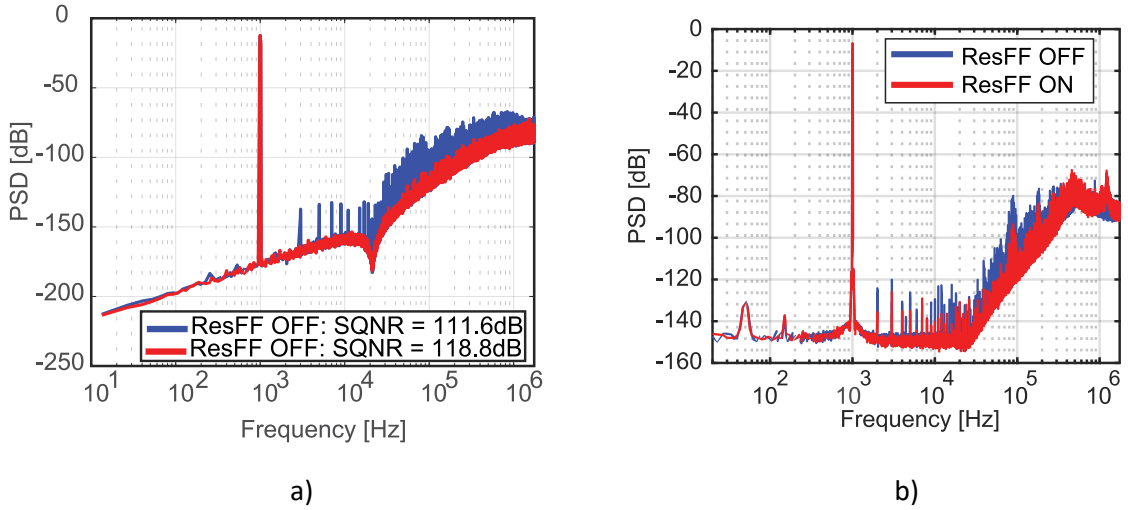

Figure 3.14: The out-of-band cancellation achieved by q_C feed-forward in a) simulation, b) measurement.

3.3 Dynamic Errors

In a zoom ADC, the references of the DSM are updated by the digital output of the coarse ADC, and remain fixed till the next update of the references. If the input is changing slowly, as in the case of a temperature sensor [24], then the reference update can also be slow. The first generation of zoom ADCs were intended for such signals [5, 25] and thus employed sequential coarse and fine conversions. In [5], for example, the coarse conversion took 6 clock cycles while the succeeding fine conversion took 128 clock cycles, as shown in Fig. 3.15.a. As shown in Fig. 3.15.b, dynamic signals may then move outside the chosen reference range during the fine conversion.

In many applications, e.g. biomedical sensor read-out, audio, and instrumentation, high resolution is required together with several kHz of bandwidth. In order to satisfy the latter requirement, a *dynamic* zoom ADC architecture is proposed, which utilizes concurrent coarse and fine conversions [6]. A dynamic zoom ADC utilizes concurrent coarse and fine conversions. The coarse converter then updates the references of the DSM continuously at its output rate.

The time domain operation of a dynamic zoom ADC is shown in Fig. 3.16.a and Fig. 3.16.b. The coarse ADC is an N-bit SAR ADC, whose conversion time takes N clock cycles of the DTDSM ($N = 5$ in Fig. 3.16). Although more robust to dynamic signals, the duration of the coarse conversion still puts a limit on the maximum full-scale input frequency ($f_{in,max}$), as

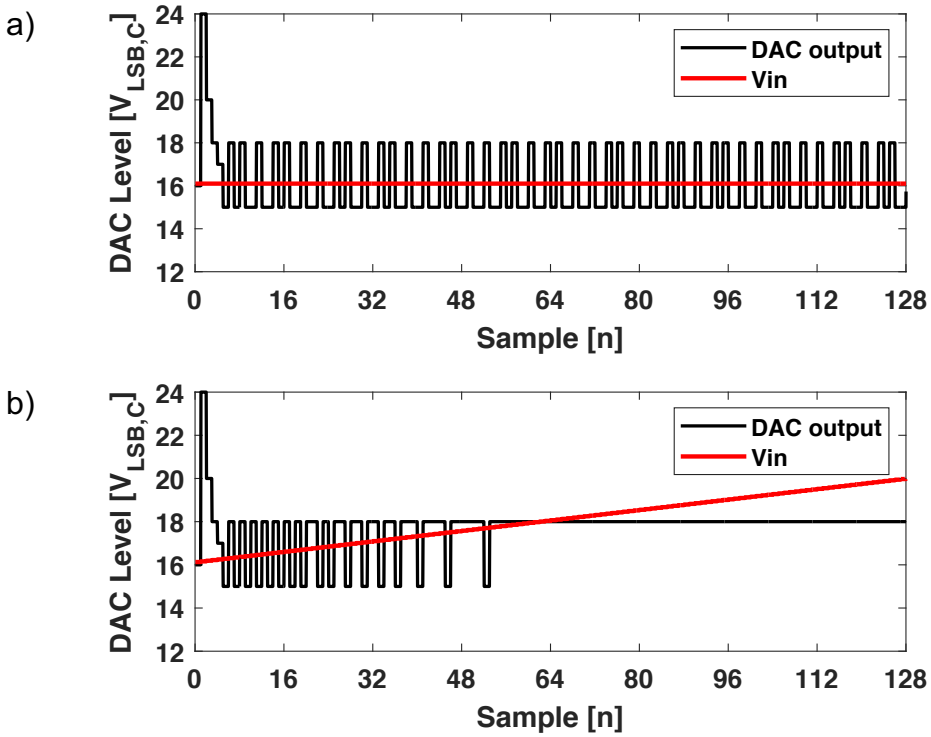

Figure 3.15: Sequential zoom ADC operation in the time domain. a) Static inputs. b) Dynamic inputs.

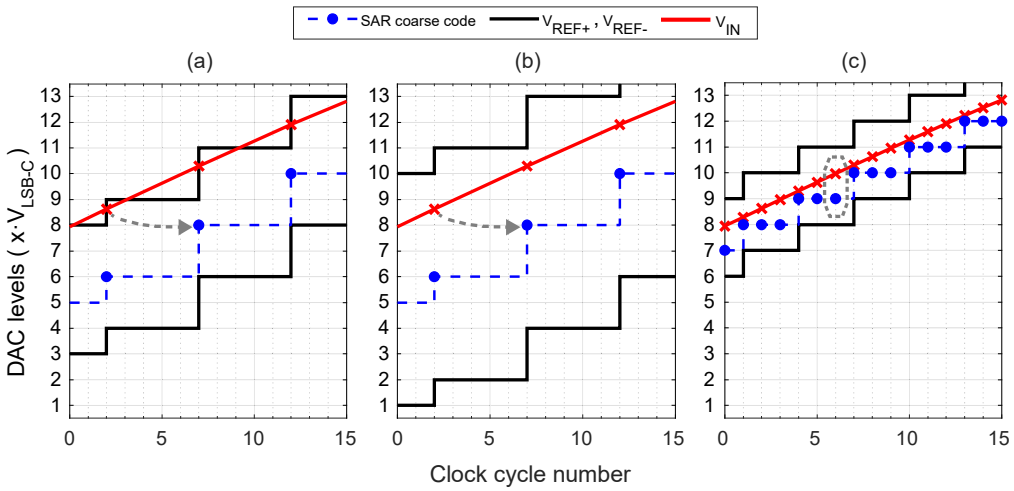

Figure 3.16: Time domain operation of the dynamic zoom ADC for a fast changing input. a) Coarse code and corresponding fine-reference are updated at every 5 cycles by an 5-bit SAR ADC for a) $M = 2$, for b) $M = 4$. c) Fine-reference is updated every cycle by an 5-bit asynchronous SAR, with an over-ranging of $M = 1$ [7].

shown in Fig. 3.16.a. This is because the references of the DTDSM are only updated once every N clock cycles, while the DSM assumes that the signal rests in between these set reference levels between two reference update moments. The references are set by k, which represents the signal's value at the moment of the coarse ADC's sampling $V_{in}(t_{s,C})$. This is used to compare it with the sampled input of the DTDSM at its samlping moment ($t_{s,F}$), which is $V_{in}(t_{s,F})$. In case of an N-bit coarse SAR ADC, the input is sampled at $t_{s,C}$ and the corresponding k is present N cycles later. Assuming k sets the references immediately, minimum difference $\Delta t = t_{s,F} - t_{s,C}$ ise N clock periods. However, this k value will be used for the next N cycles. Thus, the maximum Δt would be $2N$ clock cycles. This requires more over-ranging, i.e. higher M, to achieve proper operation, as shown in Fig. 3.16.b.

A higher N is desirable to reduce the DSM input range and increase the energy efficiency as discussed in Chapter 2. However, it raises Δt. As shown in Fig. 3.16.a, when the input signal changes too fast to be tracked by the coarse SAR ADC, the input can extend beyond the modulator's stable input range. The stable input range of DSM can be expressed as:

$$V_{DSM,max} = \alpha(V_{REF,DSM+} - V_{REF,DSM-}) = \frac{\alpha\,(2M+1)\,V_{REF,FS}}{2^N - 1} \tag{3.14}$$

where $V_{REF,FS}$ is the full-scale of the zoom ADC, and $\alpha \leq 1$ defines the topology-dependent stable input range of the DSM. The maximum input signal slope ΔV_{in} for a sinusoidal input with frequency f_{in} in a time period Δt (assuming $\Delta t \ll 1/f_{in}$) occurs at its zero-crossings, and can be approximated for a full-scale signal amplitude ($A_{max} = 0.5\,V_{REF,FS}$) as:

$$\Delta V_{in} \simeq A_{max} 2\pi f_{in} \Delta t = V_{REF,FS}\ \pi\ f_{in}\ \Delta t. \tag{3.15}$$

The input signal stays within the stable input range of the DSM if the signal variation (ΔV_{in}) does not exceed this range during one coarse conversion period:

$$\Delta V_{in} < V_{DSM,max}. \tag{3.16}$$

By using (3.14), (3.15), and (3.16), the maximum input signal frequency of the zoom ADC is found as:

$$f_{in,max} < \frac{\alpha\,(2M+1)}{\Delta t\,(2^N - 1)\,\pi}. \tag{3.17}$$

When a synchronous SAR ADC is used as in [6], Δt would be equal to $\frac{2N}{f_s}$. In this case, $f_{in,max}$ can be expressed as:

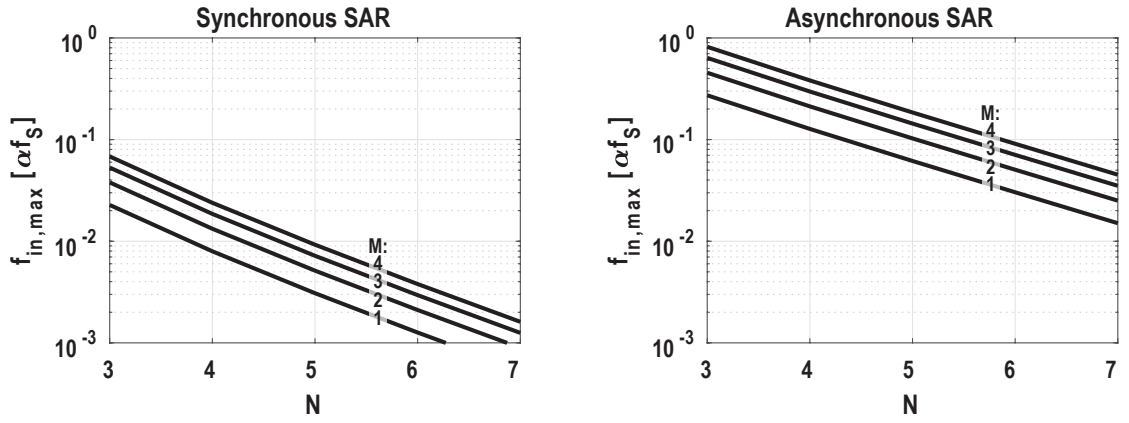

Figure 3.17: $f_{in,max}$ $[\alpha\, f_S]$ vs N for synchronous and asynchronous SAR ADCs with different M values.

$$f_{in,max} < \alpha \frac{2M+1}{2N\,(2^N-1)\,\pi} f_s. \tag{3.18}$$

The first part of (3.18) represents the relation of $f_{in,max}$ to M and N, which are parameters about the coarse conversion. The second part gives the effect of α and f_s, which are DSM related parameters. It can be seen that a higher N, or a lower f_s reduce $f_{in,max}$.

Compared to a synchronous SAR ADC, an asynchronous one is a better choice [7]. An asynchronous SAR ADC is triggered by a clock edge, synchronous to f_s, but its internal execution of the binary search algorithm is self-timed. In [7], the asynchronous SAR ADC's total conversion time was much less than half a clock cycle. This allowed the update of the DSM references half a clock cycle after the coarse sampling moment as shown in Fig. 3.16.c, hence Δt was $\frac{0.5}{f_s}$. We can express $f_{in,max}$ in this case as:

$$f_{in,max} < 2\,\alpha \frac{2M+1}{(2^N-1)\,\pi} f_s. \tag{3.19}$$

The dependency of $f_{in,max}$ to N is less dramatic in (3.19) compared to (3.18). Fig. 3.17 depicts $f_{in,max}$ in terms of $\alpha\, f_s$ for N-bit synchronous and asynchronous SAR ADCs with different M values. It is seen that a synchronous SAR ADC limits $f_{in,max}$ dramatically. This can be alleviated by increasing M, or reducing N. Both would result in increased DSM input swing, and therefore degraded energy efficiency. An asynchronous SAR ADC, however, has a minimal penalty on $f_{in,max}$ even for higher N values. This allows the use of $M = 1$, as reported in [4, 7, 8] and shown in Fig. 3.16.c. This directly reduces the input swing of the DSM and improves the energy efficiency of the DSM, which is limited by its linearity specifications as discussed in Chapter 2.

3.4 References

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Chapter 4

A Discrete-Time Dynamic Zoom ADC for Audio Applications

This chapter presents the design of a dynamic zoom ADC in which the coarse and fine ADCs operate concurrently[1]. Aimed for use in audio codecs for automotive applications, a first prototype achieved 98.3 dB SNDR in a 20 kHz bandwidth while consuming 1.65 mW [1]. A revised version of this, the second prototype, achieved 103 dB SNDR while its power consumption dropped to 1.12 mW [2]. In terms of bandwidth, this represents a 1000-fold improvement on incremental zoom ADCs [3, 4], while maintaining their state-of-the-art energy efficiency.

4.1 Dynamic Zoom ADC

The block diagram of the proposed dynamic zoom ADC is shown in Fig. 5.1. As explained in Chapter 3, it consists of a coarse SAR ADC and a fine DSM working concurrently. Over-ranging is used to accommodate static and dynamic mismatch errors between the coarse and the fine sections. Since over-ranging increases the DSM's input range, it also increases its quantization noise, resulting in a trade-off between resolution, linearity, and the offset requirements of the SAR ADC.

Because the input signal V_{in} is directly fed to the fine DSM, the linearity of the overall zoom ADC is only determined by the fine DAC and the loop filter, as long as the SAR ADC's INL error is small enough to keep the DSM stable. Achieving the required loop filter linearity is greatly eased by zooming, since it ensures a low swing at the input of the loop filter. At the same time, data weighted averaging (DWA) can be used to meet the high linearity requirements

[1] This chapter is based on [1] and [2].

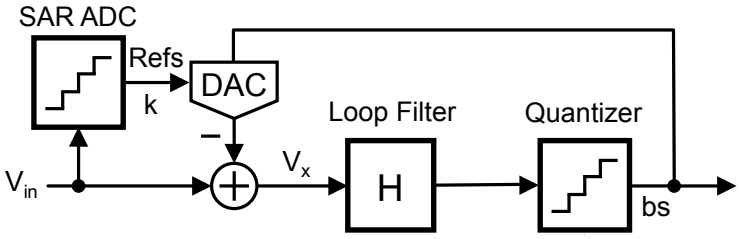

Figure 4.1: The system-level block diagram of the dynamic zoom ADC.

in the fine DAC. In this way, zooming enables an energy-efficient two-step conversion without stringent linearity requirements on the coarse ADC, which can then be easily realized.

4.2 System Level Design

4.2.1 Coarse Resolution, Bandwidth, and Over-ranging

It is desirable to increase the resolution of the coarse ADC to reduce the DSM's input swing. However, the limited conversion speed of the coarse ADC means that the update of the DSM's references is subject to a delay, during which the input signal can move out of the DSM's stable input range, as discussed in Chapter 3. Assuming that the SAR ADC and the DSM are clocked at the same frequency f_s, and that the SAR ADC requires N clock periods to complete its $N-$bit conversion,, i.e., $f_{s,coarse} = f_s/N$, the maximum input signal frequency of the zoom ADC is found in Chapter 3 as:

$$f_{in,max} < \alpha \frac{2M+1}{2N\left(2^N-1\right)\pi} f_s. \tag{4.1}$$

It is clear that the signal bandwidth of the zoom ADC is limited by the coarse ADC's resolution, but that it can be improved by increasing f_s or M. Increasing the former would degrade energy efficiency by increasing the energy consumption of the clock circuitry, sampling and DAC switches and digital logic, which are all proportional to f_s. Increasing M, however, is more difficult due to the stricter nonlinearity requirements as discussed in Chapter 2.

In the chosen 0.16 μm CMOS technology, $f_s = 11.29$ MHz (OSR $= 282$) is chosen as a compromise between bandwidth optimization and power consumption in the digital circuits. Fig. 4.2 shows $f_{in,max}$ as a function of M for $f_S = 11.29\,MHz$, $\alpha = 0.6$, and for different SAR ADC resolutions. Both a 4-bit SAR ADC with $M = 1$, and a 5-bit SAR ADC and $M = 2$ are suitable. The latter is chosen, since its quantization error will be lower, resulting in better predictions of the fine ADC's input range.

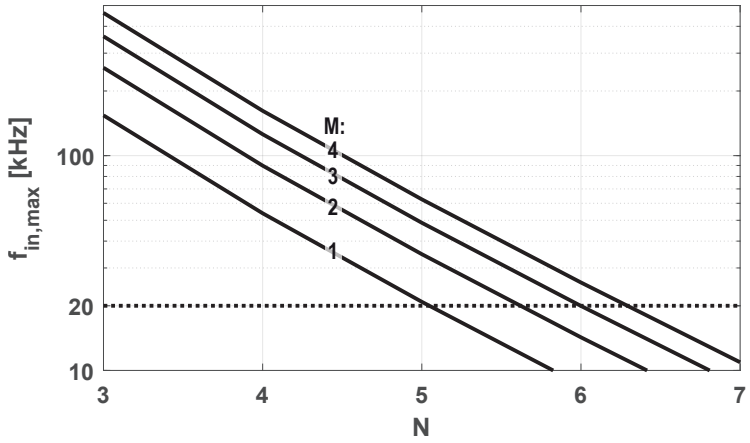

Figure 4.2: $f_{in,max}$ vs N for $f_s = 11.29\ MHz$ and different M values.

4.2.2 DSM

The signal-to-quantization-noise ratio (SQNR) of the zoom ADC depends on the DSM's SQNR, the SAR ADC's resolution, and the over-ranging factor M. In order to have a thermal noise limited SNR, the quantization noise should be much less than the thermal noise, i.e., SQNR $\geq$ 130 dB for SNR = 110 dB. The DSM's SQNR is determined by the loop filter order, the quantizer resolution, and OSR. Since the out-of-band quantization noise is already low enough, due to the zoom-induced reduction in the DSM's input range, multi-bit quantization is not required.

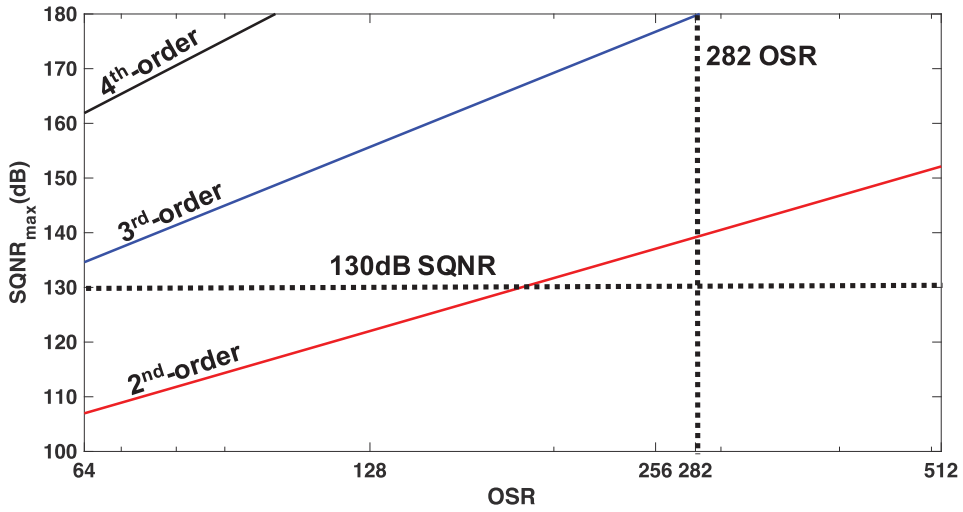

Figure 4.3: SQNR_{max} of a zoom ADC with 5-bit SAR ADC, and a first-, second-, and third-order DSM versus OSR.

The theoretical SQNR_{max} for a zoom ADC with 1-bit quantizer, 5-bit SAR ADC, and $M = 4$ is shown in for different loop filter orders Fig. 4.3. This indicates that, for the chosen $\text{OSR} = 282$, a second-order loop filter would be sufficient. However, in practice, a second-order loop filter will not have enough margin. For a robust design, the third-order DSM shown in Fig. 4.4 is chosen. The switched-capacitor loop filter is implemented as a cascade of integrators with feed-forward compensation (CIFF) for its superior linearity and energy efficiency.

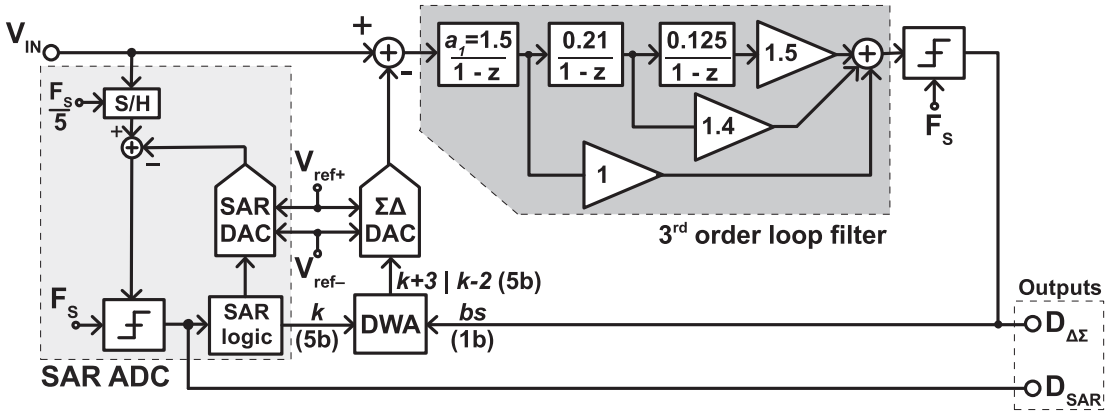

Figure 4.4: System level block diagram of the implemented dynamic zoom ADC.

System-level simulations revealed that the required SQNR performance is met for a DC gain of 65 dB in the first integrator, and a 40 dB DC gain for both the second and the third integrators. The first integrator's gain coefficient a_1 in conventional DSMs is usually less than 1 to realize a large stable input range. However, since zooming allows for an input range much smaller than the zoom ADC's full-scale input, $a_1 = 1.5$ is chosen. This corresponds to a first-integrator output swing of up to 27% of the full-scale. The area of a DTDSM is mostly dominated by the sampling and the integration capacitors of the first integrator due to the noise requirements. As a result of the increased a_1, the integration capacitor of the first integrator can be much smaller.

4.3 Circuit Design

A simplified circuit schematic of the proposed dynamic zoom ADC is shown in Fig. 4.5. The unary capacitance DAC is also used as a sampling capacitor. The reduced swing of the DSM enables the use of low-gain amplifiers for the realization of the integrators, such as simple energy-efficient CMOS inverters [3]. However, pseudo-differential inverter-based

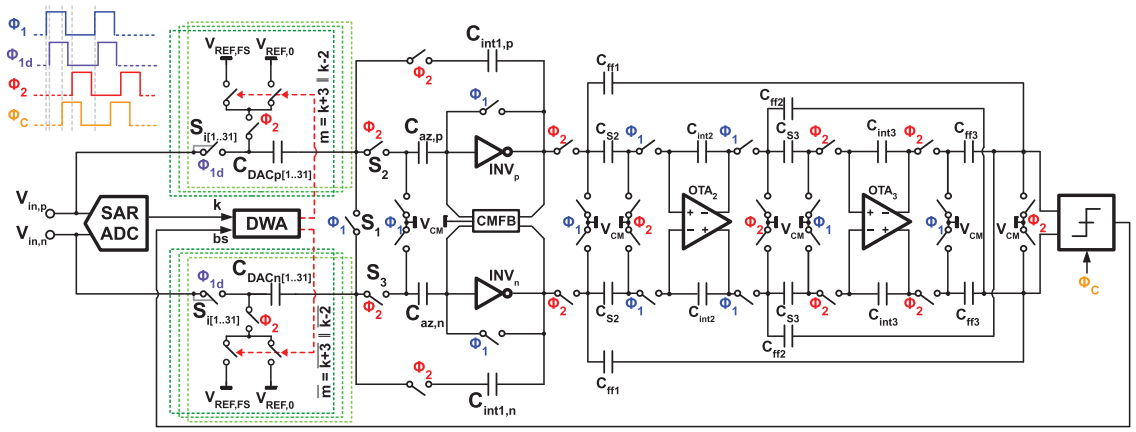

Figure 4.5: Simplified schematic of the implemented dynamic zoom ADC,

amplifiers exhibit a poor common-mode rejection ratio (CMRR) [5]. This is improved by an input sampling circuit that utilizes switches S_{1-3} to reject input common-mode signals. At the end of the sampling phase Φ_1, S_1 opens and the differential input signal V_{in} is sampled on all 31 DAC units $C_{DACp,n[1..31]}$, while the input common-mode is cancelled. The CMRR is limited by the matching of the two sampling capacitors, and is simulated to be higher than 60 dB. Because they see rail-to-rail signals, the input switches $S_{i[1..31]}$ are bootstrapped to improve their linearity [6]. The level shifting capacitors in the bootstrap circuit are implemented by using MOS capacitors and their value is 5 pF. The area of the bootstrapped switches are less than 10% of the capacitive DAC. In the integration phase Φ_2, m DAC elements ($m = k-2$ or $m = k+3$) are connected to $V_{ref,p}$ in the positive branch (to $V_{ref,n}$ in the negative branch), while the others are connected to $V_{ref,n}$ ($V_{ref,p}$). Thus, a differential charge equal to $(31\,C_{DACp}\,V_{in}) - m\,C_{DACp}\,(V_{ref,p} - V_{ref,n})$ is transferred to the integration capacitors $C_{int1p,n}$, effectively performing reference zooming in charge domain. Since the units used in each period are scrambled by the DWA algorithm, a high-accuracy reference zooming is achieved. The quantizer is implemented as a clocked latch proceeded by a single stage static preamplifier.

4.3.1 DAC

Since linearity is a critical specification for audio applications, the total harmonic distortion (THD) of the zoom ADC should be less than −100 dB. The linearity is mainly limited by the fine DAC, even after the application of DWA. Moreover, DWA could increase the in-band noise and limit SNR as discussed in Chapter 3. Thus, the DAC unit elements should be designed for low mismatch. In the chosen process, a unary capacitive DAC using lateral metal-

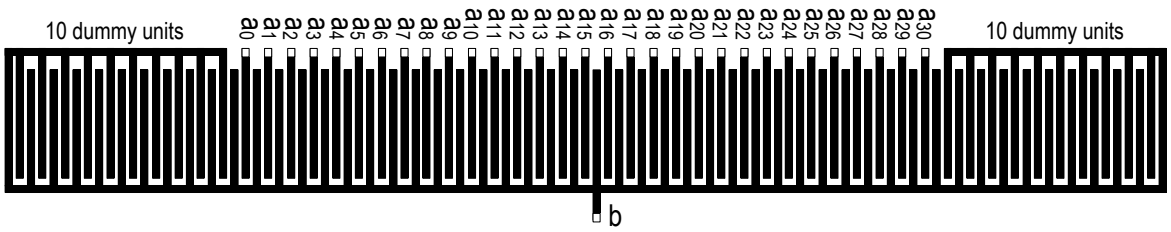

Figure 4.6: Layout of the implemented capacitive DAC.

metal capacitors has achieved 0.1% maximum relative mismatch [3]. A 5-bit version of this DAC with 160 fF units $C_{DACp,n[1..31]}$ as shown in Fig. 4.6 is used in combination with DWA. This results in a total 5 pF sampling capacitor that meets the thermal noise requirements. 10 dummy units are used on each side to overcome edge effects degrading the unit matching. Recalling from Chapter 3, the SNR after DWA can be estimated as [7]:

$$\mathrm{SNR}_{\mathrm{DWA}} = \frac{9\,(2^N-1)\,\mathrm{OSR}^3}{8\pi^2\sigma_u^2}. \tag{4.2}$$

With $N = 5$, and OSR $= 282$ the resulting $\mathrm{SNR}_{\mathrm{DWA}} > 145$ dB indicates that the extra "noise" due to shaped mismatch-errors will not limit the overall SNR. The expected worst case THD is verified to be less than than -110 dB by system level simulations.

4.3.2 Loop Filter Integrators

Inverter-based integrators have been used in DSMs for their excellent energy efficiency [3, 5, 8, 9]. However, a simple CMOS inverter's quiescent current is strongly dependent on its input voltage and is prone to process supply voltage and temperature (PVT) variations. An energy-efficient pseudo-differential inverter-based operational trans-conductance amplifier (OTA) is shown in Fig. 4.7.a. In [3], a dynamic biasing scheme is proposed to address its PVT sensitivity. The proposed topology, however, is not suitable for high sampling frequencies, as explained in the following. During the sampling phase Φ_1, the input is sampled on C_s and the input transistors M_1 and M_2 are diode-connected and biased by a floating current source via cascode transistors M_{3b} and M_{4b}, while M_{3a} and M_{4a} are in off state. The bias voltages V_{OP} and V_{ON} are sampled on the auto-zeroing capacitors C_{az} while simultaneously sampling the offset and $1/f$ noise of the OTA to implement auto-zeroing. Since the floating current source needs to be removed from the circuit in the following integration phase Φ_2, M_{3b} and M_{4b} are driven off and M_{3a} and M_{4a} are turned on by biasing their gates with $V_{b,n1}$ and $V_{b,p1}$, respectively. Because of the large current flowing in the OTA, the switching gates of cascode transistors $M_{3a,b}$ and $M_{4a,b}$ are large enough to significantly load the biasing circuit generating $V_{b,n1}$ and

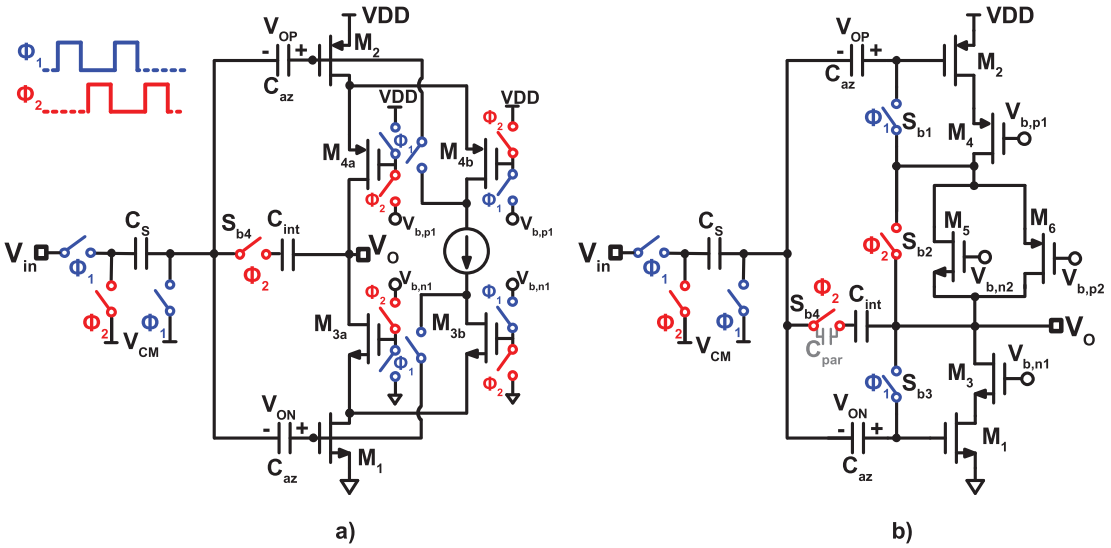

Figure 4.7: a) Inverter-based integrator used in [3]. b) Proposed inverter-based integrator.

$V_{b,p1}$. For $f_s = 11.29$ MHz, settling to the correct biasing voltages within each period would require the biasing circuit to consume about the same amount of power as the OTA itself, which would significantly degrade energy efficiency.

A dynamic biasing scheme for inverter-based OTAs is proposed in this work and shown in Fig. 4.7.b. Instead of switching the floating current source by means of cascode transistors, switches S_{b1-3} are introduced. During the sampling phase Φ_1, diode connections are established around the input transistors (M_{1-2}) via S_{b1} and S_{b3}, and the floating current source (M_{5-6}) forces the same bias current ($125\,\mu A$) through the input and cascode (M_{3-4}) transistors. At the same time, the bias voltages as well as the offset and the $1/f$ noise are sampled on the auto-zeroing capacitors C_{az} (2 pF each). In the integration phase Φ_2, diode connections are broken by opening the switches S_{b1} and S_{b3}, and the floating current source consisting of M_{5-6} is simply bypassed by S_{b2}. Since there is no switching capacitive load to the biasing circuit, its power consumption can be minimized. Furthermore, the proposed biasing scheme results in a much more compact design by eliminating two large cascode transistors. A simple SC common-mode feedback (CMFB) circuit as in [3] is adequate to avoid output common-mode drift in the pseudo-differential implementation.

Integration capacitors $C_{int} = 3.3$ pF are realized by using lateral metal-metal capacitors. The parasitic capacitance across S_{b4} (C_{par}) may limit the DC gain of the integrator if particular care is not taken. During the integration phase Φ_2, the sampled charge is transferred to the integration capacitor C_{int}. In the following sampling phase Φ_1, S_{b4} is off and C_{par} is in series with C_{int}. Thus, some of the integrated charge leaks into C_{par}, and is discharged in the

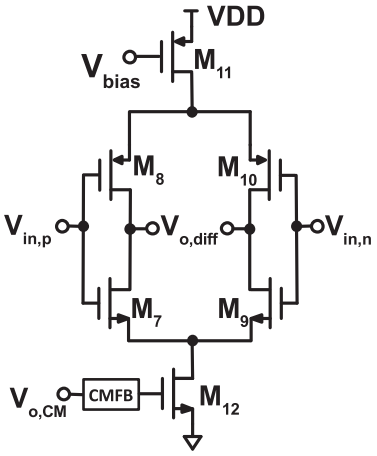

Figure 4.8: Simplified schematic of OTA_2 and OTA_3.

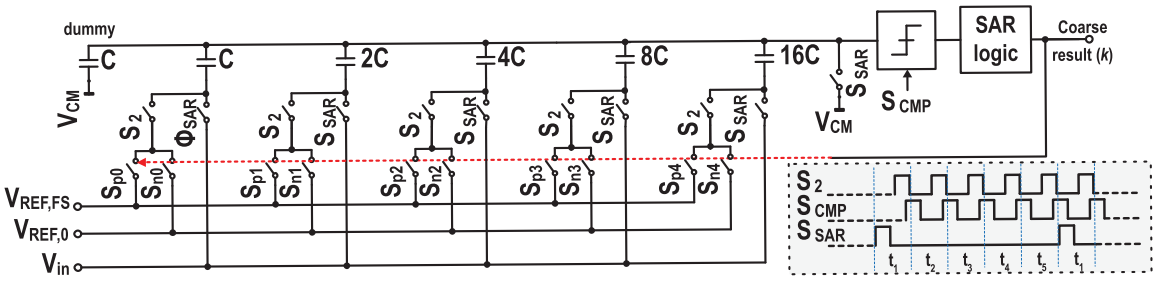

Figure 4.9: Simplified schematic of the SAR ADC.

following phase Φ_2, thus limiting the integrator DC gain. Hence, the ratio between C_{int} and C_{par} should be much higher than the intended DC gain of 65 dB, meaning less than $C_{par} < 1$ fF for the $C_{int} = 3.3$ pF. This is achieved by increasing the distance of the source and drain nodes as much as possible and using a shield between source and drain routing.

Due to their more relaxed requirements, a fully differential current-starved inverter-based OTA with SC CMFB is used to implement OTA_2 and OTA_3, as shown in Fig. 4.8. Because of the relaxed noise and linearity requirements due to the first integrator gain, they were biased at five times lower current levels compared with the first OTA (50 μA each) and their capacitors were also scaled accordingly.

4.3.3 SAR ADC

The simplified schematic of the SAR ADC with its timings is shown in Fig. 4.9. The 11 fF unit capacitors are sized to ensure that coarse conversion errors due to noise and mismatch are less than 1 LSB_C. As shown in Fig. 4.9, the SAR ADC samples the input once every five

clock cycles. At the end of each five-cycle conversion, the result k is provided to the DAC of the zoom ADC. The same quantizer as in the DSM is used to implement the comparator of the SAR ADC.

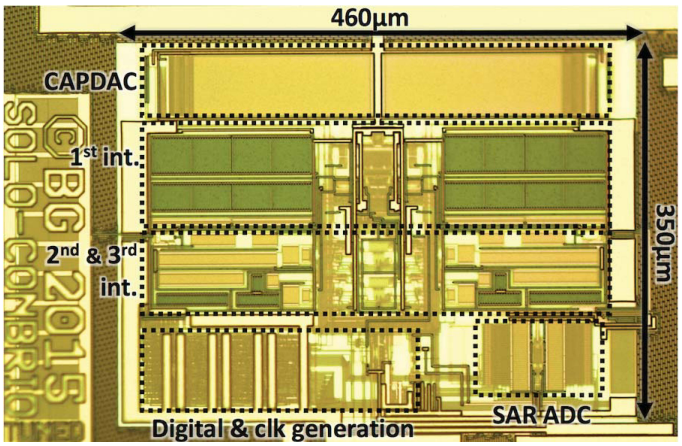

Figure 4.10: Chip micrograph of prototype 1.

4.4 Measurement Results of Prototype 1

The $0.16\,\mathrm{mm}^2$ zoom ADC shown in Fig. 4.10 is fabricated in a $0.16\,\mu$m CMOS process. It draws 0.92 mA from a 1.8 V supply, with the digital circuitry consuming 25% of the power (DWA, SAR logic and the non-overlapping clock generator). The analog power consumption is dominated by the first integrator. The SAR ADC's analog section draws only 11 μW (simulated). As shown in Fig. 4.11 and Fig. 4.12, the peak SNR and peak SNDR are 104.4 dB and 98.3 dB, respectively, in a 20 kHz bandwidth, with DWA on and for input frequencies up to 20 kHz and input voltages of $\pm 1.75\,\mathrm{V}$ (differential, $V_{ref,p} = 1.8\,\mathrm{V}, V_{ref,n} = 0\,\mathrm{V}$). The measured DR is then 107.5 dB. With DWA off, the DAC mismatch limits the peak SNDR to 73 dB.

The ADC's measured CMRR is greater than 62 dB from DC up to 1 kHz, demonstrating the effectiveness of the proposed common-mode cancellation scheme. As it can be seen from Fig. 4.12 its $1/f$ corner is below 10 Hz, which demonstrates the effectiveness of the auto-zeroing scheme.

Table 4.1 presents a summary of the ADC's performance in comparison with state-of-the-art ADCs[2] with similar resolution (> 90 dB SNDR) and bandwidth. By achieving a competitive $\mathrm{FOM_{DR}}$ of 178.3 dB and using significantly less area than the state-of-the-art, this work demonstrated that zoom ADCs can also achieve high energy efficiency for dynamic

[2] At the time of publication of [1].

signals. Note that [10] outperforms this design in energy efficiency while having a similar performance.

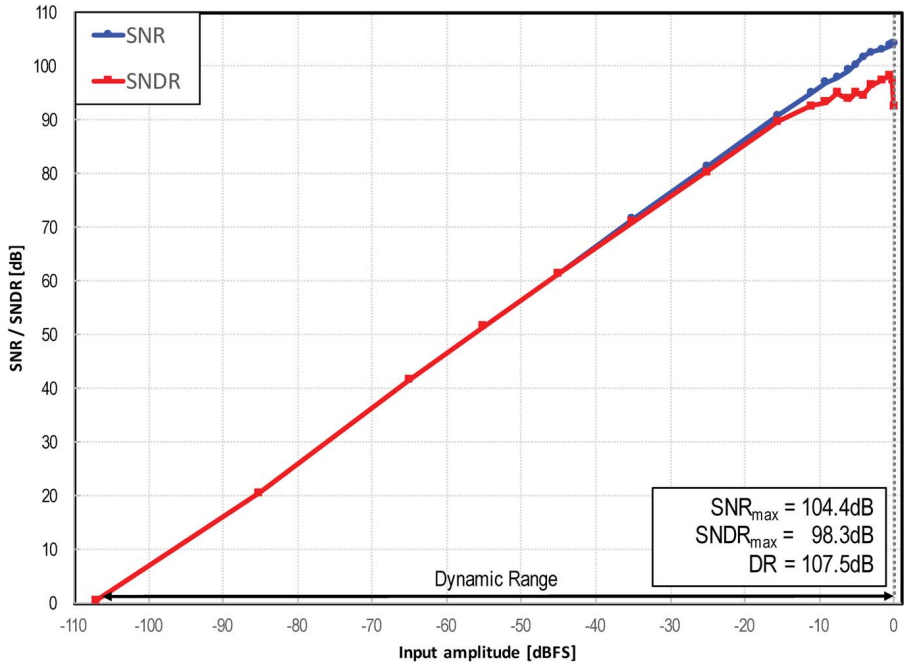

Figure 4.11: SNR and SNDR versus input signal amplitude (1 kHz).

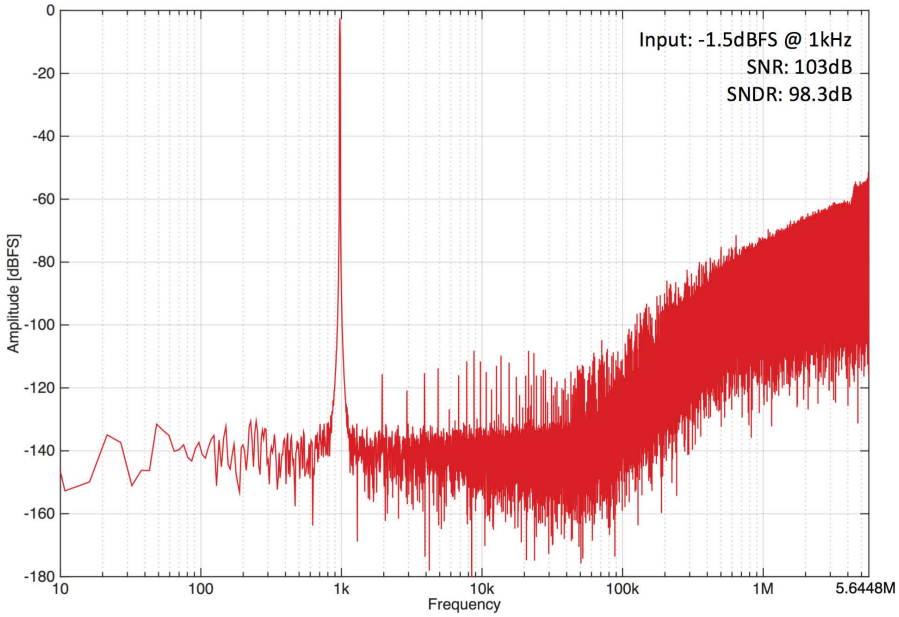

Figure 4.12: Measured output spectrum of the zoom ADC.

Table 4.1: Performance summary and comparison for prototype 1.

	Unit	This Work	Wang [11]	Sukumaran [10]	Park [6]	Yang [12]	Nguyen [13]
Year	-	2016	2015	2014	2009	2008	2005
Technology	μm	0.16	0.028	0.18	0.18	0.35	0.35
Die area	mm^2	0.16	0.022	1.25	2.16	7.4	0.82
Power consumption	mW	1.65	1.13	0.28	0.87	165	18
Sampling frequency	MHz	11.29	24	6.144	5	6.144	5.12
Signal bandwidth	kHz	20	24	24	25	20	20
Peak SNR	dB	104.4	100.6	98.9	100	-	106‡
Peak SNDR	dB	98.3	98.5	98.2	95	111	99
DR	dB	107.5	100.6	103	100	124‡	106‡
†FOM$_{\text{SNDR}}$	dB	169.1	171.8	177.5	169.6	161.8	159.5
††FOM$_{\text{DR}}$	dB	178.3	173.8	182.3	174.6	174.8‡	166‡

†FOM$_{\text{SNDR}}$ = SNDR + 10log(Signal bandwidth / Power)
††FOM$_{\text{DR}}$ = DR + 10log(Signal bandwidth / Power).
‡ A-weighted.

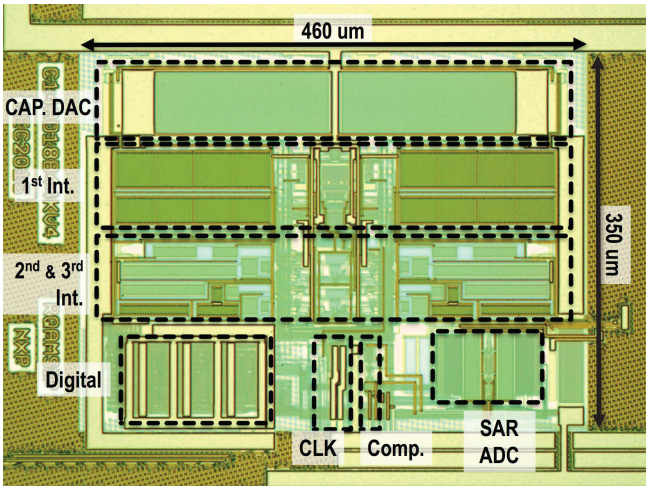

Figure 4.13: Chip micrograph of prototype 2.

4.5 Measurement Results of Prototype 2

The first prototype's digital outputs are the DSM bit-stream, the SAR ADC's comparator output, and a clock at f_s synchronized to the data. On- and off-chip (PCB-coupled) interference from these 1.8 V CMOS level single-ended outputs to the ADC's references limited the measured SNR and SNDR. Moreover, the drivers of these signals were powered from the same supply pad on-chip. This not only caused on-chip interference, but also corrupted the ADC's core power consumption measurement significantly. Another issue discovered in prototype 1 was that the biasing currents were much higher than the designed levels, due to the post-layout stress effects which were not taken into account. This resulted in increased analog power consumption. The second prototype is designed to fix these, together with some minor layout errors.

The second prototype dynamic zoom ADC, which is a modified version of the first prototype, has been realized in a $0.16\,\mu$m CMOS technology [2]. The prototype ADC occupies an area of 0.16 mm^2, as shown in Fig. 4.13. It consumes 1.12 mW from a 1.8 V supply, with the digital circuitry consuming 29% of the power (DWA, SAR logic, and the non-overlapping clock generator). The first integrator with its 56% share dominates the analog power consumption. In contrast, the SAR ADC's analog section draws only 7 μW (measured).

The supply of the digital output drivers is lowered from 1.8 V to 0.9 V to reduce the PCB-coupled interference (Fig. 4.14). The ADC's peak SNR, SNDR, and DR were then measured to be 106, 103, and 109 dB, respectively, with DWA on (Fig. 4.15). With DWA off, DAC mismatch limits the peak SNDR to 72 dB. The ADC's measured CMRR is greater than 62 dB from DC up to 1 MHz for full-scale common-mode inputs, demonstrating the effectiveness of the common-mode cancellation scheme. Also, its $1/f$ corner is below 20 Hz, which demonstrates the effectiveness of the auto-zeroing scheme used in the first integrator.

As discussed before, full-scale out-of-band signals may overload the DSM. This will typically degrade its in-band DR and noise floor. To test this, Fig. 4.16 shows the measured DR in 20 kHz bandwidth in the presence of full-scale in- and out-of-band differential signals. A full-scale sine wave is applied to the prototype ADC's input and its frequency is swept from 10 to 100 kHz. In-band noise is measured to predict the achievable DR. The ADC's DR starts to degrade with full-scale inputs above 27 kHz, which is in line with the results of system-level simulations. Inserting a first-order RC low-pass filter (LPF) with a 30 kHz corner frequency in series with the ADC ensures that its DR remains constant for full-scale inputs up to at least 100 kHz (the maximum output frequency of the used low-noise signal generator Rohde & Schwarz UPD).

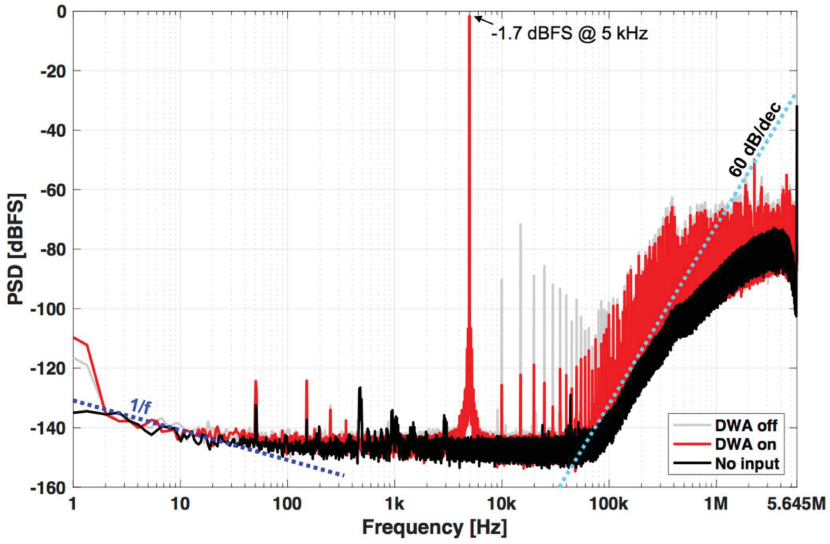

Figure 4.14: Measured output spectrum of the zoom ADC with 0.9V output drivers.

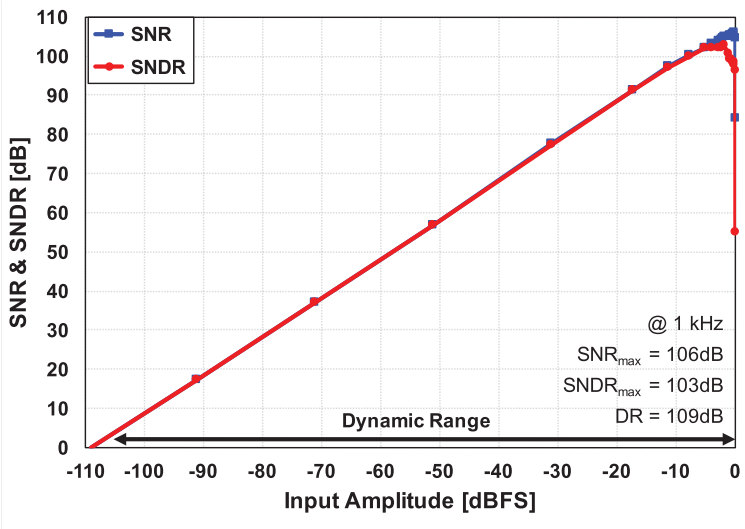

Figure 4.15: Measured SNR and SNDR versus input amplitude (DWA on).

Table 4.2 presents a summary of the ADC's performance in comparison with the state-of-the-art ADCs with similar resolution (> 100-dB DR) and bandwidth[3]. A key observation is that it is significantly more area-efficient than previous designs in similar technology nodes. A large part of the ADC's area consists of capacitors, which, in turn, is defined by the kT/C noise required to obtain a given DR and sampling frequency. The proposed zoom ADC shows good area efficiency, even compared to designs implemented in advanced technology nodes with high-density capacitors.

[3] At the time of publication of [2].

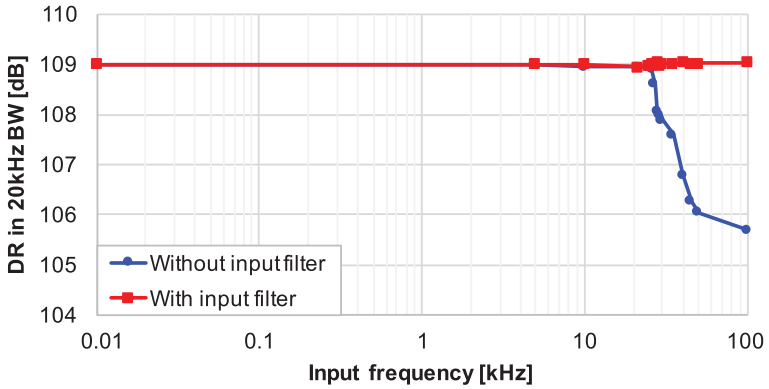

Figure 4.16: DR in 20 kHz BW in the presence of in- and out-of-band full-scale inputs with and without an LPF at the input with 30 kHz corner frequency (DWA on).

Table 4.2: Performance summary and comparison for prototype 2.

	Unit	This Work	de Berti [14]	Billa [15]	Leow [16]	Wang [11]	Sukumaran [10]
Year	-	2016	2016	2016	2016	2015	2014
Technology	nm	160	160	180	65	28	180
Die area	mm^2	0.16	0.21	1.33	0.256	0.022	1.25
Power	mW	1.12	0.39	0.28	0.8	1.13	0.28
Sampling frequency	MHz	11.29	3	6.144	6.4	24	6.144
Signal bandwidth	kHz	20	20	24	25	24	24
Peak SNR	dB	106	93.4	99.3	100.1	100.6	98.9
Peak SNDR	dB	103	91.3	98.5	95.2	98.5	98.2
DR	dB	109	103.1	103.6	103	100.6	103
$^{\dagger}FOM_{SNDR}$	dB	175.5	168.4	177.8	170.1	171.8	177.5
$^{\dagger\dagger}FOM_{DR}$	dB	181.5	180.2	182.9	177.9	173.8	182.3

$^{\dagger}FOM_{SNDR} = SNDR + 10\log(\text{Signal bandwidth} \,/\, \text{Power})$
$^{\dagger\dagger}FOM_{DR} = DR + 10\log(\text{Signal bandwidth} \,/\, \text{Power})$.

4.6 References

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Chapter 5

A Discrete-Time Zoom ADC for Instrumentation Applications

Slowly changing signals, with bandwidths below 1-2 kHz, are often encountered in several applications, such as sensor interfaces, biomedical signal processing, and industrial instrumentation. The amplitude of such signals may vary considerably, ranging from a few μV to a few Volts, and so ADCs intended for such applications require higher than 120 dB DR, and high linearity. Since many of these applications involve battery powered systems, such as wearable medical devices and portable instruments, such ADCs should also be extremely energy-efficient with a power consumption less than a milliwatt. Linearity requirements in such applications also necessitate an INL within a few parts-per-million (ppm), translating into a SNDR similar to the DR.

This chapter describes a dynamic zoom ADC based on an asynchronous SAR, which allows the DSM references to be updated after every clock cycle[1]. This makes the zoom ADC more robust to out-of-band interferes, while at the same time relaxing the loop filter requirements and, hence, increasing its overall energy efficiency.

5.1 Zoom ADC with Asynchronous SAR ADC

The proposed zoom ADC, as shown in Fig. 5.1.a, consists of an N-bit asynchronous SAR ADC, which performs a coarse conversion and outputs an N-bit code k. This digital value k is used to determine the high and low references for the DSM, respectively, as:

[1]This chapter is based on [1]

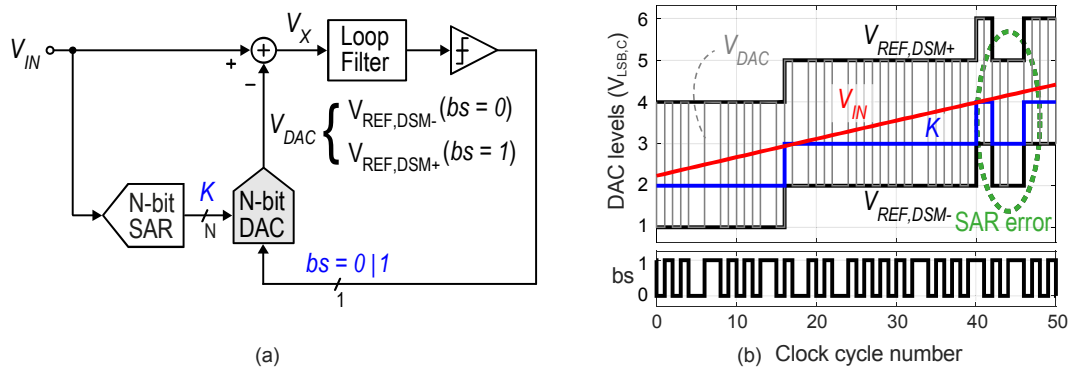

Figure 5.1: a) Simplified block diagram of the dynamic zoom ADC. b) Time domain waveforms of different signals in the zoom ADC with an over-ranging of $M = 1$.

$$\mathrm{V_{REF,DSM+}} = (k+1+M)\ \mathrm{V_{LSB,C}} \tag{5.1}$$

$$\mathrm{V_{REF,DSM-}} = (k-M)\ \mathrm{V_{LSB,C}} \tag{5.2}$$

where, $\mathrm{V_{LSB,C}}$ is the quantization step size corresponding to the N-bit SAR and M is the over-ranging factor. An N-bit DAC is used to generate these fine references. The DSM DAC toggles between these references depending on the bitstream output of the comparator (bs), as in a conventional DSM, essentially zooming-in on the signal and achieving an SQNR significantly higher than a conventional 1-bit DSM. Fig. 5.1.b shows the resulting signals for the case when $M = 1$.

The relaxed requirements on the SAR ADC due to over-ranging, greatly simplifies its design. Furthermore, zooming reduces the swing at the input of the loop filter, relaxing the linearity and driving requirements of the DSM integrators, thus allowing the use of simple and energy-efficient inverter-based operational transconductance amplifiers (OTAs).

5.1.1 Maximum Input Frequency and Over-ranging

Over-ranging also plays a role in defining the maximum input signal frequency that a dynamic zoom ADC can tolerate. In [2], a conventional synchronous N-bit SAR ADC is constantly running in the background. Since it takes N cycles to calculate and update the coarse code k, and as this is then used for the next N cycles before it is updated again, an input signal is not allowed to swing beyond the fine-references determined by k for $2N$ cycles. The N cycle delay between every input sampled by the SAR ADC and the corresponding update in k makes it difficult for the dynamic zoom ADC to track such signals as discussed in Chapter 3. This

inability to track high-frequency signals or interferers deteriorates its in-band performance, limiting its use to applications where out-of-band inputs are not expected, or requiring the use of a low-pass filter to attenuate them [2]. Tracking limitations can be improved by increasing the over-ranging. However, a higher over-ranging also means an increased swing at the inputs of the DSM loop filter (V_x in Fig. 5.1.a).

In a switched-capacitor circuit, an amount of charge proportional to the swing V_x is transferred to the loop filter input capacitors. The OTAs used to implement the integrators in the loop filter must provide this charge with a certain settling accuracy and linearity. If the swing at the loop filter input is smaller, this can be achieved with less current, hence with less total power consumption. For high energy efficiency, it is therefore necessary to keep the over-ranging as low as possible. For this reason, an asynchronous SAR ADC is used instead of the conventional N-cycle SAR ADC in this work. An asynchronous SAR ADC calculates the N-bit output code in a fraction of the clock period, updating the fine-references and allowing it to be used in the same cycle. This cycle-by-cycle update of the fine-references implies that the input must stay within the bounds of the fine-reference for only one cycle. The maximum tolerable input frequency for a zoom ADC with asynchronous SAR ADC is found in Chapter 3 as:

$$f_{in,max} < 2\,\alpha\,\frac{2M+1}{(2^N-1)\,\pi}\,f_s \tag{5.3}$$

where $\alpha \leq 1$ defines the topology-dependent stable input range of the DSM. (5.3) is $2N$ times higher compared to a zoom ADC with a synchronous SAR ADC. This change also makes it possible to reduce M to the bare minimum required to tolerate the inaccuracies of the SAR ADC. Although, the power required by an asynchronous SAR will be N times that of a synchronous design, it is negligible compared to the power dissipated in the loop filter and the digital back-end. Furthermore, the lower swing requirements on the integrators, allows the use of simpler amplifiers, thus reducing the power consumption of the loop filter.

5.1.2 Loop Filter Order, Coarse Resolution and OSR

To ensure a thermal noise limited SNR, the target for SQNR is set above 140 dB. Fig. 2 shows the variation of peak SQNR with different combinations of loop filter order and coarse resolution with increasing sampling frequency. Since this work targets precision applications, a discrete-time loop filter is chosen over its continuous-time counterpart for the inherent advantages it offers, mainly in terms of process spread and jitter immunity. However, a discrete-time loop filter suffers from sampled thermal noise, mainly dominated by the input stage sampling

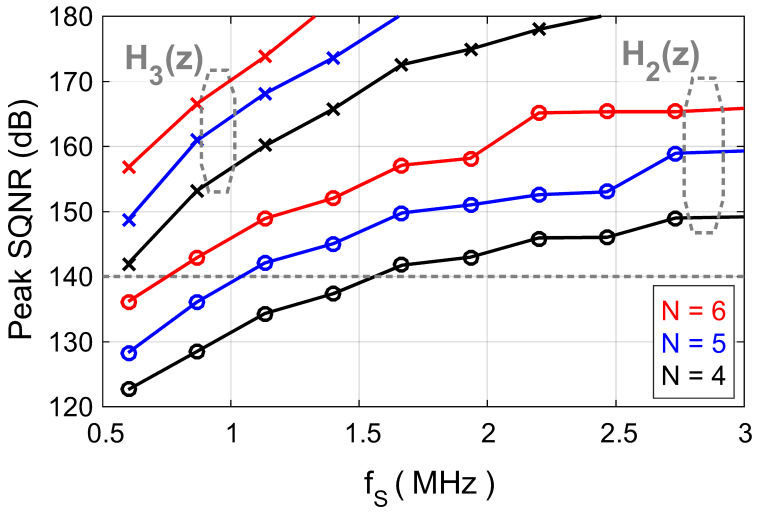

Figure 5.2: SQNR vs sampling frequency f_S for a 2^{nd} and 3^{rd} order loop filter employing a 4,5,or 6-bit asynchronous SAR ADC as the coarse quantizer with an over-ranging of $M = 1$ on the fine-references.

capacitors. The strict linearity requirement necessitates the use of metal capacitors, which have the drawback of low density. Thus, they can be quite large at low OSR. An OSR of 1000 (f_s = 2 MHz for f_{bw}= 1 kHz) is chosen to achieve a 120 dB DR while using reasonably sized capacitors. As seen in the plot, every configuration exceeds the target SQNR of 140 dB at f_s = 2 MHz, so that a 3^{rd}-order loop filter is unnecessary. With a 2^{nd}-order loop filter, coarse resolutions above $N = 4$ offes sufficient SQNR when an over-ranging of $M = 1$ is used. Using $M = 1$, the loop filter input swing for $N = 4$ is approximately twice that of $N = 5$, leading to a proportional increase in loop filter power consumption to maintain linearity. While the loop filter can achieve even lower swing for $N = 6$, the maximum tolerable input frequency of the zoom ADC decreases and the accuracy requirements of the SAR ADC increase, requiring an increase in over-ranging. Furthermore, since a DEM algorithm is used in the digital backend for the DAC (on-chip), its power consumption for $N = 6$ will be approximately double that for $N = 5$, which is quite significant in the chosen 0.16 μm technology. For these reasons, a coarse resolution of $N = 5$ is used in this design, for an optimum trade-off between power consumption, tracking capability and SAR ADC requirements.

5.1.3 Linearity Relaxation and Out-of-Band Fuzz

The zoom ADC can be modeled as shown in Fig. 5.3.a, where the SAR ADC serves as a direct input feed-forward to the digital output. The DSM DAC can be split into two ideal DACs: one N-bit DAC that tracks the input using the coarse code k and another 1-bit DAC with levels

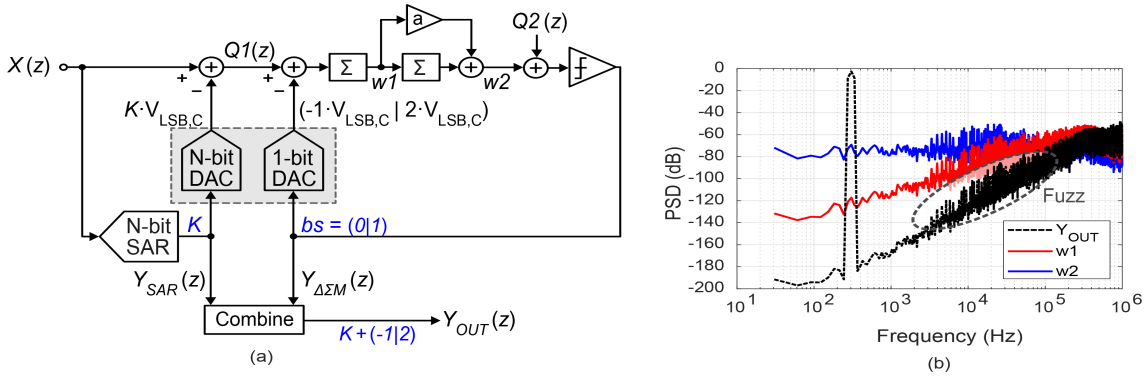

Figure 5.3: a) Intuitive block diagram of the coarse-fine operation of the N-bit DAC. b) Spectrum at internal nodes of the loop filter and the zoom ADC's output when $N = 5$ and $M = 1$.

$-1 \cdot V_{(LSB,C)}$ and $2 \cdot V_{(LSB,C)}$. Since the input to the loop filter $Q1(z)$ is basically the quantization error of the SAR ADC, the loop filter does not process the signal, as shown in the spectrum in Fig. 5.3.b, relaxing the linearity requirements of its integrators to a significant extent. It should be noted that splitting the N-bit DAC into two separate DACs is purely conceptual, the actual implementation consists of a single N-bit DAC.

Due to the way the digital logic processes the outputs of the SAR ADC and the DSM, some residual out-of-band *fuzz* is visible in Fig. 5.3.b. Observing Fig. 5.3.a, one can write the outputs of the SAR ADC and the DSM in the z-domain as:

$$Y_{SAR}(z) = X(z) - Q1(z) \tag{5.4}$$

$$Y_{\Delta\Sigma M} = Q1(z) \cdot \mathrm{STF} + Q2(z) \cdot \mathrm{NTF} \tag{5.5}$$

$$Y_{OUT}(z) = X(z) + Q1(z) \cdot (\mathrm{STF} - 1) + Q2(z) \cdot \mathrm{NTF} \tag{5.6}$$

where $Q1(z)$ is the quantization noise of the coarse SAR ADC, $Q2(z)$ is the quantization noise of the 1-bit comparator in the DSM, and STF and NTF are the signal and noise transfer functions of the DSM, respectively. Due to the feed-forward nature of the loop filter, the STF exhibits some peaking and deviates from 1, which causes an imperfect cancellation of the SAR ADC quantization noise $Q1(z)$ out-of-band. The fuzz shown in Fig. 5.3.b is a result of the imperfect cancellation of the SAR ADC's quantization error, which is characterized by high frequency tonal content. As in MASH architectures, this can be tackled in the digital domain. The SAR ADC's output code k can be passed through a digital filter matched to the STF before combining it with the bitstream output, as shown in Fig. 5.4.a. The combined

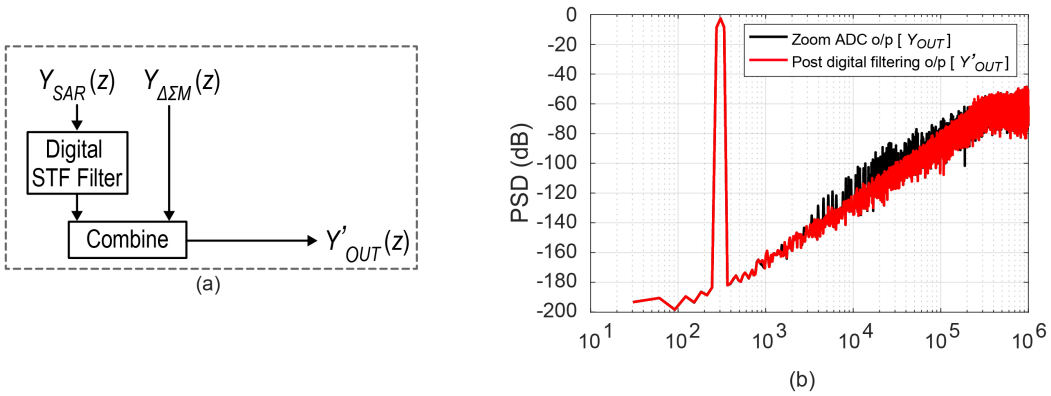

Figure 5.4: a) Fuzz filtering using a digitally matched STF filter. b) Its effect on the zoom ADC output spectrum.

output spectrum before and after digital processing to remove the fuzz is shown in Fig. 5.4.b.

5.1.4 SAR ADC Requirements

As explained earlier, over-ranging helps mitigate the errors of the SAR ADC and relaxes its accuracy requirements. A systematic coarse quantization error simply reduces the residual over-ranging and consequently lower the maximum tolerable frequency. This changes (5.3) to:

$$f_{in,max} < 2\,\alpha\,\frac{(2M+1-\varepsilon)}{(2^N-1)\,\pi}\,f_s \tag{5.7}$$

where ε is the maximum error in the SAR ADC's quantization levels. For this design, although the SAR ADC is 5-bit, a 7-bit accuracy is chosen so as not to deteriorate the overall performance of the zoom ADC, while not requiring excessive power and area in the SAR ADC.

5.1.5 DAC

The SNDR of the zoom ADC needs to be above 120 dB and it is limited by the fine-references generated by the N-bit DAC. While the unit capacitors used to implement the DAC are much larger than the SAR DAC's, their mismatch limits resolution to the 13-bit level. This issue is resolved using data weighted averaging (DWA) [3]. For an expected spread of $\sigma_C/C = 0.3\%$ in the unit elements, simulations indicate that an OSR of 1000 provides a sufficiently low DWA noise.

5.2 Implementation Details

Fig. 5.5 shows a simplified system level diagram of the dynamic zoom ADC, comprising of a 5-bit asynchronous SAR, a 5-bit DAC, a 2^{nd}-order feed-forward loop filter. The zoom ADC operates with $M = 1$ and OSR $= 1000$. A feed-forward loop filter is chosen to avoid the power consumption of a second DAC in the case of a feed-back loop filter [4]. The coefficients were optimized considering the stability of the loop filter, output swing of the integrators, and corresponding capacitor sizes.

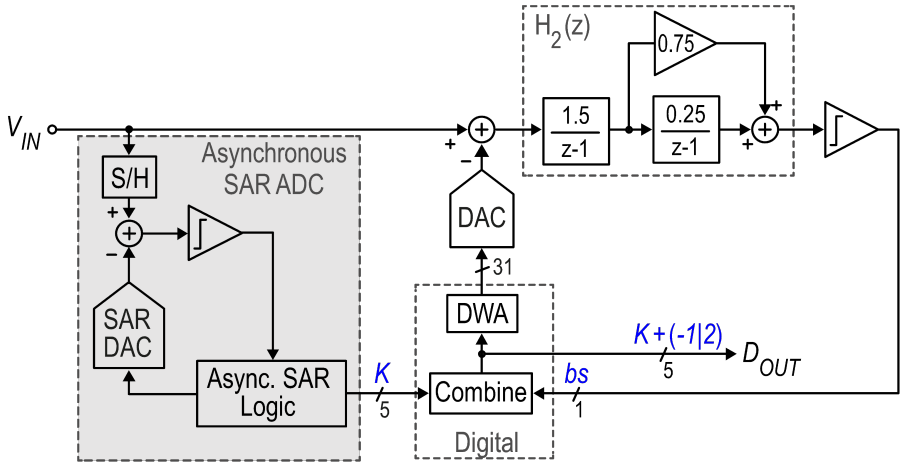

Figure 5.5: A dynamic zoom ADC employing 1-bit 2^{nd}-order modulator with a coarse 5-bit asynchronous SAR quantizer.

5.2.1 DSM

Fig. 5.6.a shows the circuit level implementation of the fully-differential discrete-time 2^{nd}-order DSM. The input sampling capacitors also serve as the feedback DAC. It is built from 31 unit elements with a value $C_{DAC[J]} \approx 438$ fF ($J = 1..31$) to form an overall sampling capacitance $C_S \approx 13.6$ pF. This value, together with the OSR, determines the thermal noise level of the zoom ADC. Metal fringe capacitors have been used to implement the unit elements due to their high linearity and good matching. The integration capacitor of the first stage is sized to have a tolerable swing at that output of OTA1, and has a value $C_{INT,1} \approx 9$ pF. During sampling phase $\Phi 1$, all the units are shorted, and the input is effectively sampled on C_S; during $\Phi 2$, the digital back-end converts the 5-bit DAC code to a 31-bit thermometer code, which is presented to the DAC switches after DWA to generate the appropriate feedback voltage. Fig. 5.6.b shows the timing diagram of the zoom ADC. The sampling instants of the SAR ADC and the DSM

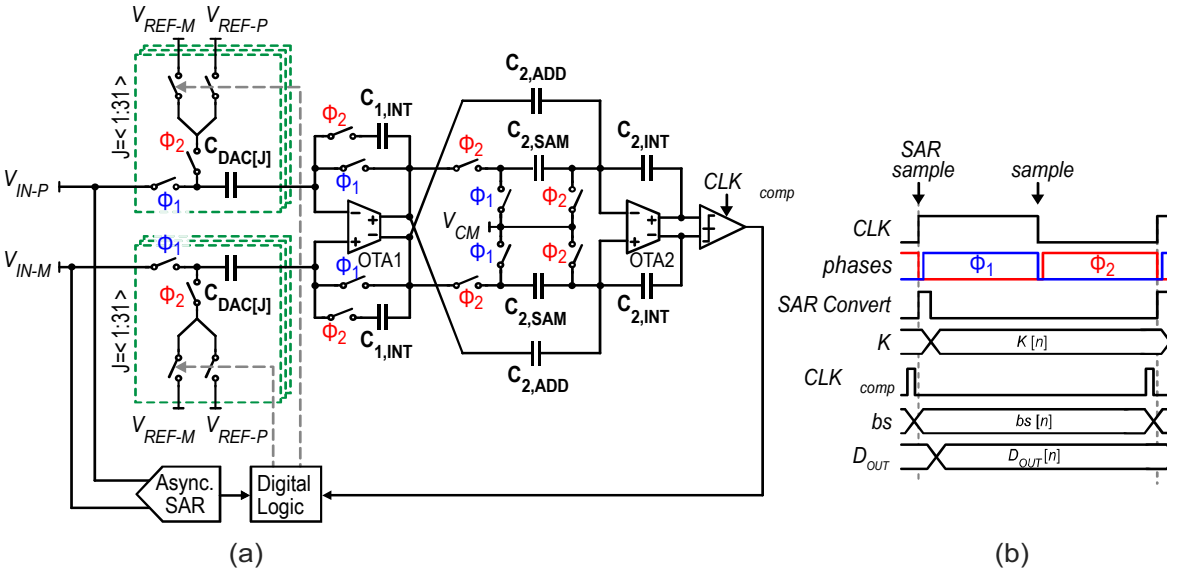

Figure 5.6: a) Simplified schematic of the dynamic zoom ADC. b) Timing diagram of the zoom ADC.

are kept half clock cycle apart to minimize the coupling between them via the input terminal.

A correlated double sampling scheme (CDS) is implemented to suppress the offset of OTA1 [5]. While the input is shorted to the outer plate of C_S during phase $\Phi 1$, OTA1 is connected in unity feedback and samples its own offset and $1/f$ noise on the other plate. During $\Phi 2$, this offset is effectively canceled while the input gets integrated. Due to the finite DC gain of OTA1, the offset sampled at the virtual ground node due to unity feedback is $V_{OFF} \cdot A/(1+A)$. As a result, an input referred offset of approximately V_{OFF}/A remains. A typical offset of a few millivolts gets suppressed to microvolts if the OTA gain is around 60 dB.

The size of the capacitors of the second stage can be very relaxed due to the high gain of the first stage. 100x smaller capacitors would mean that the corrspoinging thermal noise is 20 dB worse. However, due to the 60 dB gain of OTA1, the resulting input-referred noise floor is still 40 dB below the dominant thermal noise. In this case, the capacitance values are mainly limited by matching. $C_{SAM,2}$, $C_{ADD,2}$ and $C_{INT,2}$ are 150 fF, 450 fF and 600 fF respectively. On a similar note, the offset and $1/f$ noise of OTA2 and the comparator are also suppressed by the gain of their preceding stages. $C_{ADD,2}$ and $C_{INT,2}$ together form a continuous time proportional path in parallel to the discrete time integral path ($C_{SAM,2}$ and $C_{INT,2}$) and is used to implement the feed-forward coefficient without additional capacitors or switches.

The digital logic consists of a binary-to-unary converter followed by the DWA logic to generate the signals for each of the 31×2 unit elements from a 5-bit binary value. These two blocks together make up the dominant source of power consumption in the digital backend.

5.2.2 Current-Starved Inverter OTAs

Due to the reduced swing and current requirements, inverter-based OTAs are an ideal choice due to their high energy efficiency. The OTAs described in [2, 6] are dynamically biased, resulting in switching losses and hence degradation their energy efficiency. The reduced output swing in this design, allows the use of a simple class-A biasing scheme as shown in Fig. 5.7. The head and tail current sources M_{B0-2}, biased with 40 μA mirrored from a constant-g_m reference, suppress unwanted signal and noise from the supply lines. Cascodes are used to achieve a 60 dB DC gain. Diode-configured transistors $M_{CP,N}$ are used to track the threshold voltage spread and bias the OTA cascode transistors, ensuring that both P/NMOS input pair remain in saturation across to PVT variations.

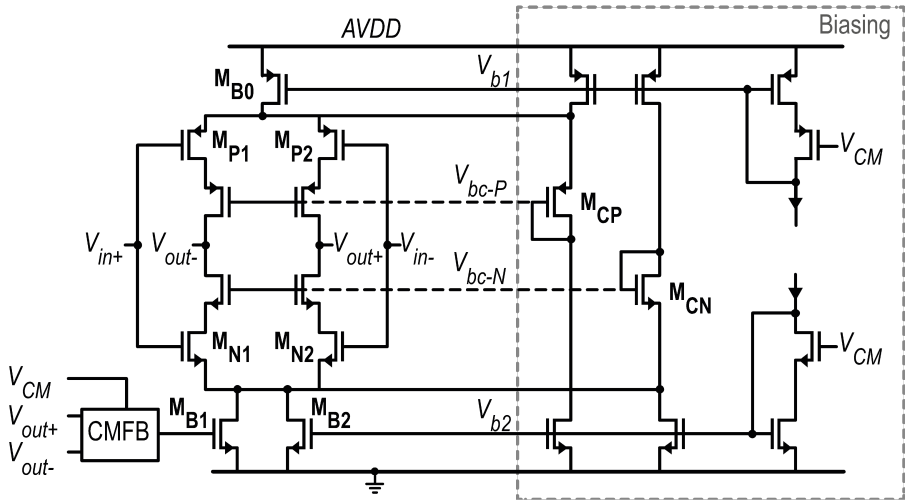

Figure 5.7: Schematic of the current-starved inverter OTAs.

The CDS sampling operation described above is also associated with the sampling of uncorrelated white noise of OTA1, adding to the kT/C sampling noise. This effect is much less pronounced in inverter based OTAs compared to other topologies. Assuming negligible noise contribution from head and tail current sources, and cascodes, the transconductance and noise are contributed only by the input PMOS and NMOS pairs, $M_{P1,2}$ and $M_{N1,2}$ respectively, without any excess noise contribution from additional transistors, typical in other topologies such as telescopic or folded cascode OTAs as discussed in Chapter 2.

OTA2 is an 8$\times$ scaled down version of OTA1 consuming 6 μA. A conventional switched-capacitor common-mode feedback circuit is used to regulate the common-mode voltage of the OTA [7].

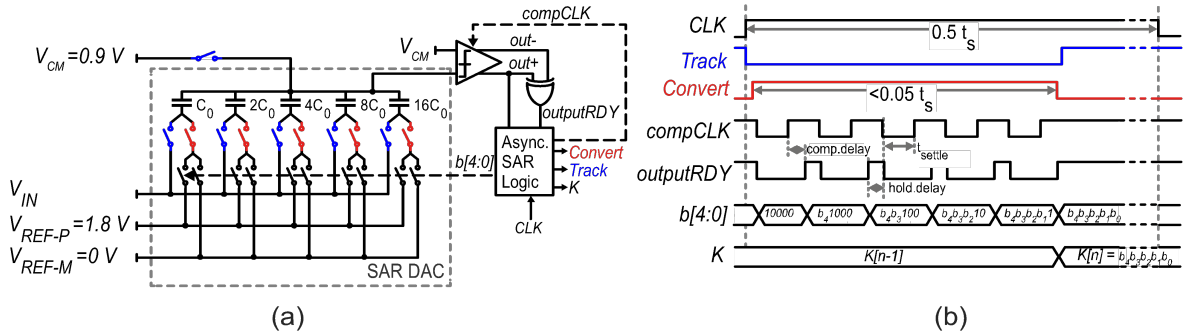

Figure 5.8: a) Simplified schematic of the asynchronous SAR ADC. b) Timing diagram of the SAR ADC.

5.2.3 5-bit Asynchronous SAR ADC

An asynchronous SAR ADC relies on internal states and logic to carry out the binary search algorithm [8, 9]. Fig. 5.8.a shows the simplified schematic of the single-ended equivalent circuit of the asynchronous SAR ADC and Fig. 5.8.b illustrates the timing of the logic signals associated with it. It consists of an asynchronous digital logic, a binary weighted capacitor DAC (SAR DAC) and a comparator. Built as an asynchronous state machine, it uses the outputRDY signal to progress from one state to the next. The SAR ADC silently tracks the input till the rising edge of CLK, when it is sampled. Each bit-conversion starts by setting the DAC inputs and then resetting the comparator with compCLK = 0. After a delay (t_{settle}) to allow the DAC to settle, the comparator is clocked (compCLK = 1) to make a comparison. An XOR gate is used to monitor the comparator output and generate the outputRDY = 1 signal once a decision is made. The decision is saved in the SAR register and a new cycle is started after a hold delay for the digital logic. After 5 such asynchronous cycles, the SAR ADC returns to tracking the input.

The unit capacitors of the SAR DAC are around 5 fF and have more than 8-bit accuracy. The SAR ADC finishes the conversion in less than 5% of the zoom ADC sampling period (across PVT variations). To mitigate kick-back on the small sampling capacitance due to the fast asynchronous operation, a dynamic comparator with a constant current biased preamplifier is used [10]. The power consumption of the preamplifier is minimized by keeping it off during the tracking phase.

5.3 Experimental Results

The prototype dynamic zoom ADC is realized in a standard 0.16 μm CMOS process and occupies an active area of 0.25 mm^2 as shown in Fig. 5.9. The input sampling capacitors, loop filter, SAR ADC, digital logic occupies 22%, 39%, 4% and 10% of the total area, respectively, with the remaining area taken up by secondary blocks such as bias and clock-phases generation, routing and de-coupling capacitors.

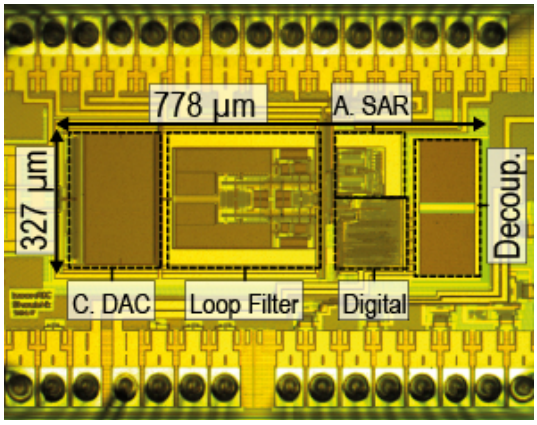

Figure 5.9: Die-micrograph of the prototype dynamic zoom ADC.

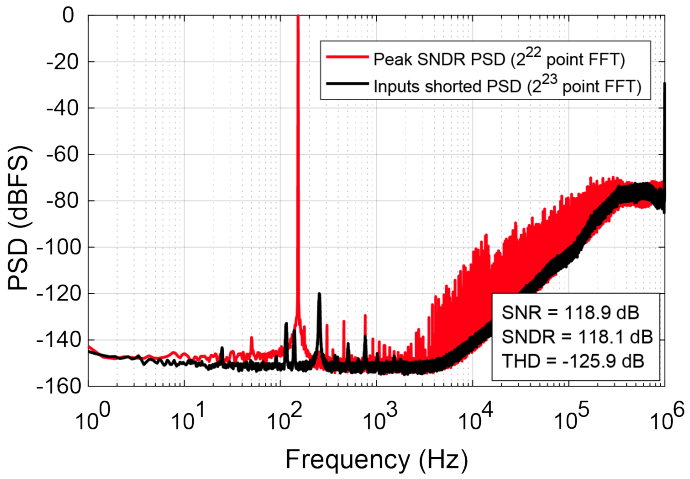

Figure 5.10: Measured output spectrum of the zoom ADC at peak SNDR (with a –0.5 dBFS sine-wave input signal) and with inputs shorted.

The ADC is powered from off-chip 1.8 V regulators for the analog and digital supply domains and a dedicated off-chip 1.8 V low noise buffered voltage reference serves as the reference source for the ADC. The ADC draws 154.5 μA (88 μA for the analog section, 42 μA for the digital section, and 24.5 μA for the references) and achieves a peak SNDR of

118.1 dB with a 0.95 V_{FS} input signal. The output spectrum is shown in Fig. 5.10. Off-chip buffers were used to drive the ADC inputs, and to limit the fold back of its wideband noise, a first-order filter with -3dB bandwidth of 2.3MHz was inserted between the signal buffers and the ADC inputs. However, this filter causes incomplete settling, and hence introduces some distortion. The tone at $f_s/2$, and others at lower frequencies, when the inputs are shorted, are due to the lack of randomization in the DWA logic and DSM. The $1/f$ noise corner is at 7 Hz and is measured by taking multiple ($32\times$) averages of a 2^{23}-point FFT with the inputs shorted.

To demonstrate the efficacy of the out-of-band fuzz cancellation, a digital post-processing filter mimicking the response of the DSM STF was implemented in MATLAB and used to evaluate the output. Fig. 5.11 shows a comparison of the output spectrum before and after using the digital filter designed to reproduce the STF response obtained in circuit simulations. The slight residual fuzz is indicative of a mismatch between the ideal STF and the actual STF. A significant reduction in out-of-band fuzz is visible, and when implemented, this filter can be used to relax the decimation filter requirements or gain back the slight loss in bandwidth due to the presence of the fuzz.

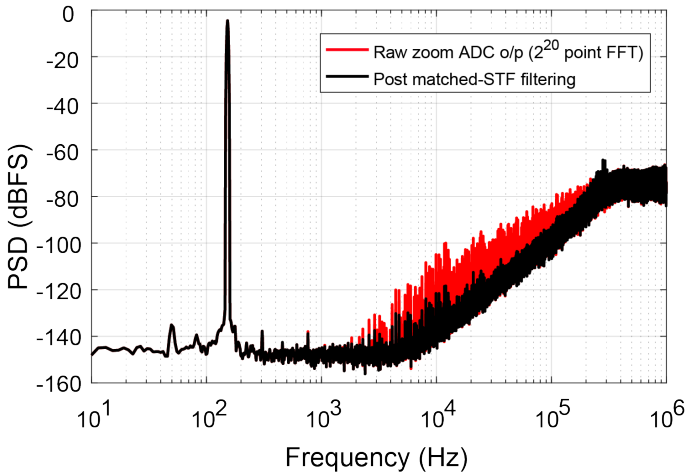

Figure 5.11: Fuzz filtering of the output spectrum using a digital matched STF filter.

A maximum offset of 30 μV from 10 different samples suggests that the CDS scheme is effective in suppressing the offset. The measured power-supply rejection ratio (PSRR) of the ADC is greater than 96 dB up to 5 kHz, demonstrating the current-starved OTA's ability to reject noise from the supply.

To assess the asynchronous SAR ADC's signal tracking capability, a -1.5 dBFS input signal is applied and its effect on the ADC's noise floor is monitored while varying the input signal frequency. Fig. 5.12 shows that the integrated in-band noise power within a 1 kHz BW (0-1 kHz) across different input frequencies. The noise floor remains unperturbed for

input frequencies as high as 48 kHz, making the dynamic zoom ADC immune to out-of-band interferers. This advancement in the zoom ADC, to track signals 48× the signal bandwidth, is a drastic improvement over [2], which could only handle signals up to 1.5× its bandwidth before its in-band noise degrades.

Fig. 5.13 shows the measured INL of the dynamic zoom ADC. Without DWA, the linearity is dominated by the mismatch of unit elements in the capacitive DAC, resulting in an INL of 400 ppm. With DWA on, the INL is within ±2 ppm.

Fig. 5.14 shows the measured SNR and SNDR of the dynamic zoom ADC across input amplitudes. The ADC achieves a peak SNR, SNDR and THD of 119.1, 118.1 and -125.9 dB respectively. The measured dynamic range of the ADC is 120.3 dB. Based on these results, FOM_{DR} is 185.8 dB. Table 5.1 summarizes the performance and compares it to other state-of-the-art ADCs with similar resolution and bandwidth (SNDR > 95 dB, bandwidth < 2 kHz) at the time of publication. The proposed ADC outperforms all other designs in terms of peak SNDR and FOM, while achieving a 120.3 dB DR.

Table 5.1: Performance summary and comparison with previous work.

	Unit	This Work	Li [11]	Shu [12]	Zhang [13]	Steiner [14]	Chae [6]
Year	-	2017	2017	2016	2017	2016	2013
Technology	nm	160	180	55	180	350	160
Die area	mm^2	0.25	4	0.072	0.27	11.5	0.375
Power consumption	µW	280	1970	15.7	33.2	12700	6.3
Sampling frequency	MHz	2	1	1	0.64	0.64	0.05
Signal bandwidth	kHz	1	500	1	1.2	1	0.013
Peak SNR	dB	119.1	-	104	97.1	-	119.8
Peak SNDR	dB	118.1	101.5	101	96.6	-	-
THD	dB	-125.6	-	-	-	-116	-
DR	dB	120.3	102.7	101.7	100.2	136.3	119.8
$^{\dagger}\text{FOM}_{\text{SNDR}}$	dB	183.6	175.5	179.0	172.2	-	-
$^{\dagger\dagger}\text{FOM}_{\text{DR}}$	dB	185.8	176.7	179.7	175.8	185.3	182.7

$^{\dagger}\text{FOM}_{\text{SNDR}} = \text{SNDR} + 10\log(\text{Signal bandwidth} \,/\, \text{Power})$
$^{\dagger\dagger}\text{FOM}_{\text{DR}} = \text{DR} + 10\log(\text{Signal bandwidth} \,/\, \text{Power})$.

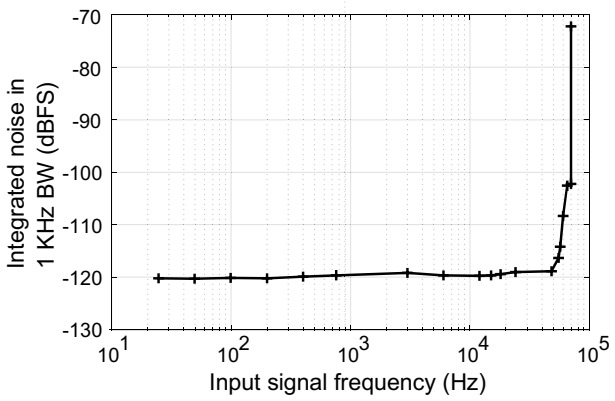

Figure 5.12: Integrated noise floor across different input frequencies with a -1.5 dBFS amplitude.

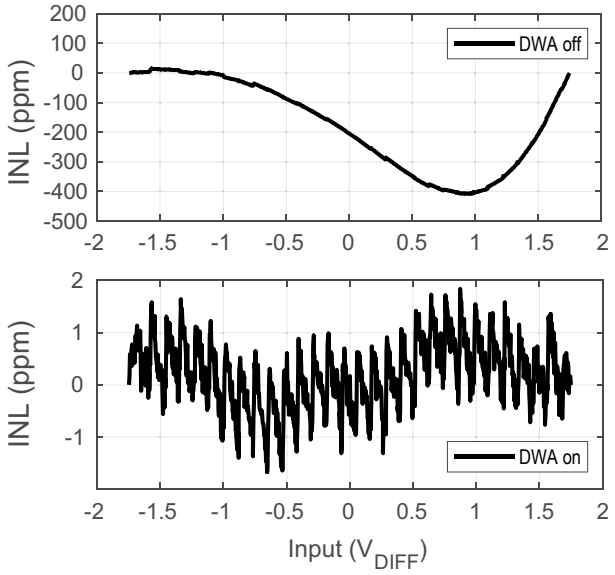

Figure 5.13: Measured INL with and without DWA.

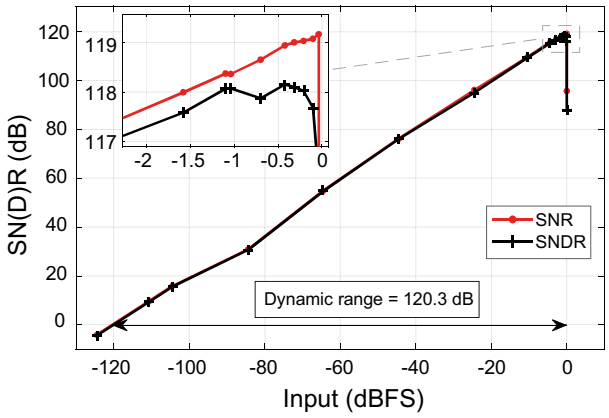

Figure 5.14: Measured SN(D)R across input amplitude.

5.4 References

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Chapter 6

A Continuous-Time Zoom ADC for Low Power Audio Applications

Audio ADCs used in battery-powered devices are required to have high linearity and high dynamic range (DR), while also being energy-efficient. These requirements can be met by zoom ADCs. However, previous designs employed switched-capacitor (SC) front-ends that required input and reference drivers capable of delivering large signal-dependent peak currents [1, 2]. For high linearity applications (> 90dB), the power dissipation of these drivers will be higher than that of the ADC itself, in some cases necessitating on-chip buffers, at the expense of chip area [3]. Previous zoom ADCs also required a 1^{st}-order input filter to prevent aliasing, and also to prevent them from overloading in the presence of large out-of-band signals [1, 2].

It is well known that ADCs based on continuous-time (CT) delta-sigma modulators (DSMs) generally do not require anti-aliasing filters, while their resistive input impedance is easy to drive [3]. However, their design can be quite challenging. First, the linearity of the amplifiers used to realize their first integrators is quite critical as discussed in Chapter 2. Furthermore, CT DACs suffer from inter-symbol-interference (ISI), which manifests itself as distortion. Calibration [4, 5], dual return-to-zero (RTZ) switching [6], or digital ISI shaping techniques [7] have been proposed to mitigate ISI-induced distortion. These techniques considerably increase system complexity and degrade energy efficiency. Also, $1/f$ noise is a dominant noise source in audio CTDSMs. Chopping could be used to suppress $1/f$ noise, but this requires care due to chopping related artifacts in CTDSMs [4, 8].

This chapter[1] describes a CT zoom ADC which achieves 108.1 dB peak SNR, 106.4 dB peak SNDR and 108.5 dB DR in a 20 kHz bandwidth while dissipating only 618 μW. This

[1]This chapter is based on [9].

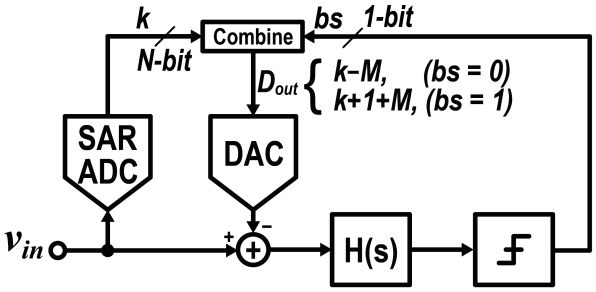


Figure 6.1: Block diagram of the CT zoom ADC.

performance is achieved by combining an asynchronous 5-bit SAR ADC with a 3^{rd}-order single-bit CTDSM. For improved energy-efficiency and linearity, its first integrator is based on a capacitively-coupled inverter-based OTA, which is chopped to mitigate its $1/f$ noise. The DAC employs a novel ISI reduction technique based on a matched-pair layout.

6.1 Continuous-Time Zoom ADC

The block diagram of the proposed CT zoom ADC is depicted in Fig. 6.1. It consists of an N-bit coarse SAR ADC and a 1-bit fine CTDSM that operate concurrently. The digital output of the coarse ADC, k, satisfies $k \cdot V_{LSB,C} < V_{in} < (k+1) \cdot V_{LSB,C}$, where V_{in} is the input signal, and $V_{LSB,C}$ is the coarse quantization step, or least-significant bit (LSB). Via the multi-bit DAC shown in Fig. 6.1, the digital value k is used to dynamically adjust the references of the CTDSM such that:

$$V_{REF,DSM+} = (k+1+M) \cdot V_{LSB,C} \tag{6.1}$$

$$V_{REF,DSM-} = (k-M) \cdot V_{LSB,C} \tag{6.2}$$

where M is an over-ranging factor as defined in Chapter 3. Driven by the modulator's bitstream (bs), the DAC then toggles between these references, effectively zooming in on V_{in}. It can be seen that as M increases the linearity requirement on the coarse ADC become increasingly relaxed. In the implementation in Chapter 5, the delay introduced by the coarse conversion path was minimized by using an asynchronous SAR ADC, and by ensuring that its output was transferred to the DAC within half a sampling-clock period. In this work, the same approach is used. By using the analysis in Chapter 3 and assuming an ideal SAR ADC, the maximum input frequency ($f_{in,max}$) that the zoom ADC driven by a full-scale input signal can handle can

then be expressed as:

$$f_{in,max} = 2\,\alpha\,\frac{(2M+1)}{(2^N-1)\,\pi}\,f_{bw}\,\mathrm{OSR} \tag{6.3}$$

where α is a coefficient that defines the maximum stable input range, f_{bw} is the signal bandwidth, and OSR is the oversampling ratio ($= f_s/2f_{bw}$). The minimum OSR ($\mathrm{OSR_{min}}$) required to ensure that $f_{in,max} > f_{bw}$ for different values of M and N is shown in Fig. 6.2. It can be seen that for a given M, increasing N also increases $\mathrm{OSR_{min}}$. Fig. 6.2 also shows the simulated INL of the coarse ADC that results in less than 10 dB SQNR degradation is for different values of M. It can be seen that as M increases the linearity requirement on the coarse ADC become increasingly relaxed as discussed in Chapter 3.

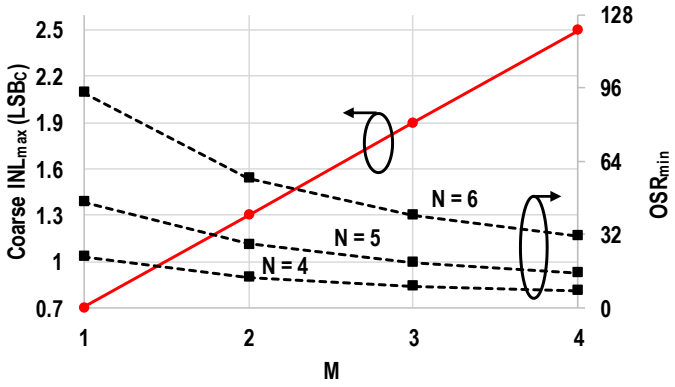


Figure 6.2: Acceptable coarse ADC INL level and minimum OSR vs over-ranging factor (M).

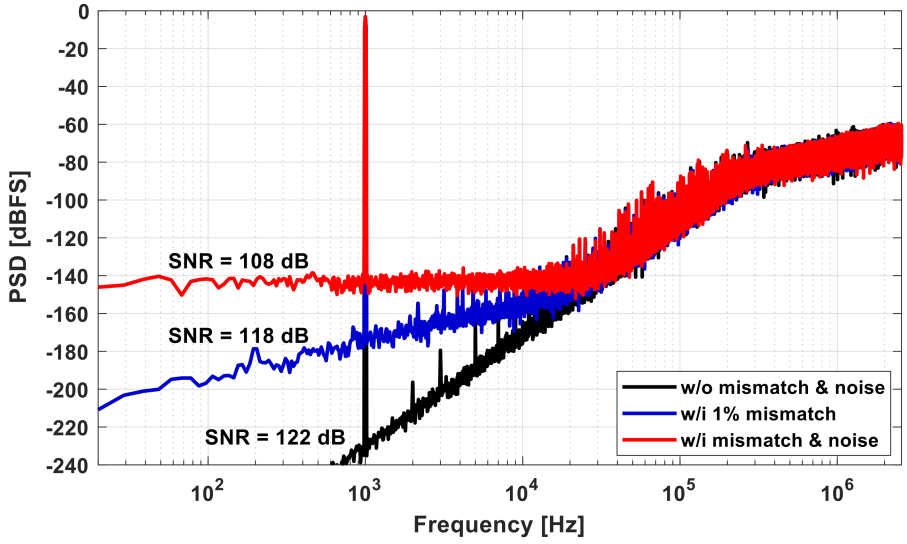


Figure 6.3: Output spectra of the CT zoom ADC with different error sources.

From Fig. 6.2, OSR_{min} is found to be roughly 40 for $N = 5$ and $M = 1$, while simulations show that an OSR of ~64 is commensurate with a target SNDR of 108 dB (the same as in the implementation presented in Chapter 4). As discussed in Chapter 3, the use of data weighted averaging (DWA) to linearize the zoom ADC's multi-bit DAC puts a higher limit on OSR because it only provides 1^{st}-order mismatch shaping while the CTDSM has a higher-order noise shaping. It also puts a lower limit on OSR due to the level of unit mismatch, below which the shaped mismatch error is too high for the targeted SNDR. Thus, in order to find the optimum OSR, first an acceptable unit mismatch should be chosen depending on the technology and area restrictions. Assuming a 3^{rd}-order loop filter, $M = 1, N = 5$, and 1% unit mismatch, OSR= 128 is found to be the optimum where the contributions of shaped quantization noise and shaped mismatch error are equal at the signal band-edge. This is shown in the output spectra obtained from simulations shown in Fig. 6.3 for three different scenarios: no mismatch and thermal noise, 1% unit mismatch and no thermal noise, and both 1% mismatch and thermal noise. The resulting in-band SNR is 122 dB, 118 dB, and 108 dB respectively. From Fig. 6.2, these parameters also ensure that the criterion $f_{in,max} > f_{bw}$ is satisfied with adequate margin.

6.2 Circuit Implementation

A simplified schematic of the implemented CT zoom ADC is shown in Fig. 6.4. It consists of a 5-bit asynchronous SAR ADC, a 3^{rd}-order feed-forward compensated loop filter, a 1-bit quantizer, and a 5-bit unary resistive DAC (R-DAC).

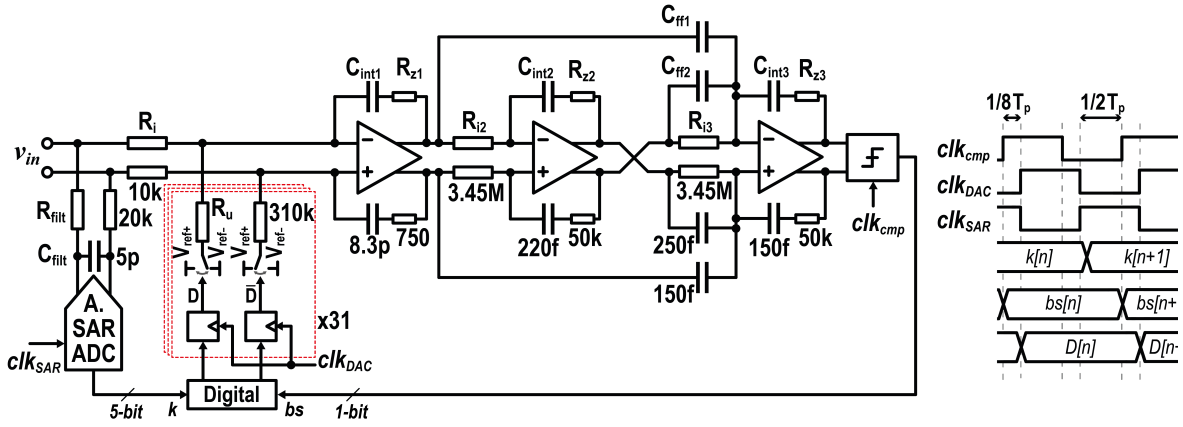


Figure 6.4: Simplified schematic of the proposed CT zoom ADC. The units for the resistors are ohms, and for the capacitors are farads.

6.2.1 Loop filter

As shown in Fig. 6.4, the feed-forward compensated loop filter used in the proposed CT zoom ADC is implemented with active-RC integrators. With a 1/8 sampling-clock delay in the loop, as shown in the timing diagram in Fig. 6.4, the modulator is stable and its in-band quantization noise power is at least 10 dB lower than the thermal noise power, even in the case of $\pm$15% RC spread. The input resistors (R = 10 kΩ) define the ADC's thermal noise, as discussed in Chapter 2, and are sized to ensure that self-heating-induced distortion is below -120 dB. The integration capacitors are adjustable, making the modulator robust to $\pm$30% RC spread.

Compared to other loop filter architectures, a feed-forward compensated loop filter has superior distortion and noise performance [10]. However, it requires a summing operation in the fast path around the quantizer. This can be implemented with a separate summing amplifier, or with capacitive feed-forward paths to the last (3^{rd}) integrator. The former often degrades energy efficiency due to the need for an additional wide-bandwidth amplifier. For the latter, the speed of the last integrator's amplifier will limit the speed of the loop filter's fast path and thus compromise stability. Preventing this would require a faster amplifier, which would consume more power [11]. A more efficient approach is to insert resistors R_{z1-3} in series with the integration capacitors C_{int1-3}, so as to reduce their phase shift around f_s as shown in Fig. 6.5 for the 1^{st}-integrator with $g_m = 2.5$ mS and $C_{int1} = 8.3$ pF. $R_{z1} = 750\ \Omega$ is chosen for the optimal improvement of the phase shift around f_s. The capacitors C_{ff1-3} and C_{int3} also need to be small to ensure that their parasitics do not impact the summing bandwidth. This is achieved by implementing the 2^{nd} and 3^{rd} integrators with large input resistances ($R_{i2-3} = 3.45$ MΩ), and small integration capacitors ($C_{int2} = 220$ fF, $C_{int3} = 150$ fF) in order to reduce the loading of their respective amplifiers and, simultaneously, optimize area. The small value of C_{int3} allows the use of small feed-forward capacitors ($C_{ff1} = 150$ fF, $C_{ff2} = 250$ fF), and hence further reduces the capacitive loading of their respective amplifiers. These techniques make it possible to reuse the 3^{rd} integrator as a summing block without compromising its power efficiency.

6.2.2 Capacitively Coupled Pseudo-Differential Amplifier

As discussed in Chapter 2, the linearity of the CIFF loop filter is mostly determined by the first integrator's linearity. This is often realized with a fully-differential amplifier (Fig. 6.6.a) [3, 12, 13]. As discussed in [14], the linearity of a fully-differential amplifier, however, is worse than that of its pseudo-differential counterpart (Fig. 6.6.b). This is because the fixed tail current makes the amplifier's transconductance (g_m) compressive while the g_m of a pseudo-differential amplifier is expansive. The dynamic biasing techniques proposed for switched-

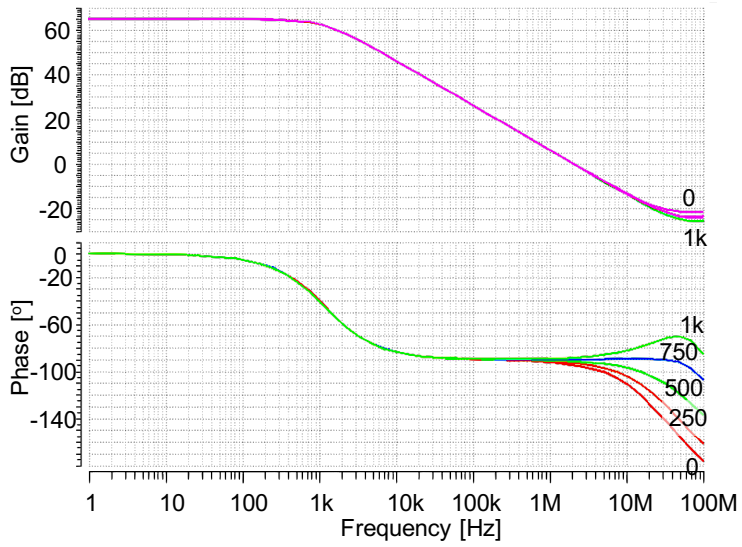
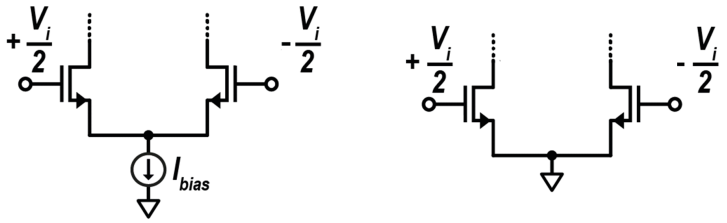


Figure 6.5: Gain and phase of the 1^{st}-integrator with $g_m = 2.5$ mS and $C_{int1} = 8.3$ pF for various R_{z1} values (0 Ω to 1 kΩ).

capacitor designs [1, 14, 15], are not suitable for continuous-time operation.

Simulations were made to compare the linearity of the a pseudo-differential amplifier with that of its fully-differential counterpart designed in the used 0.16 μm technology. Both the amplifiers are biased in weak inversion, have the same I_{bias} and device sizing, and thus have the same power consumption and g_m. In Fig. 6.7, the nonlinear components of their differential output currents are shown after being normalized to I_{bias}. It can be seen that the proposed capacitively-coupled pseudo-differential amplifier is much more linear than its fully-differential counterpart. In fact, it requires $2\times$ less g_m, hence less power, for the same linearity. A detailed analysis of the linearity of both amplifiers is given in Appendix D. These results show that a pseudo-differential amplifier can improve the energy efficiency considerable. However, removing the tail current source makes a pseudo-differential amplifier difficult to bias robustly. Furthermore, pseudo-differential amplifiers usually suffer from poor power supply and common mode rejection [1]. Thus a pseudo-differential amplifier with a robust biasing scheme and good power supply and common mode rejection is needed.

Chopping is often employed to reduce $1/f$ noise in audio CTDSMs. In this work, we propose a capacitively-coupled inverter-based pseudo-differential amplifier incorporating chopping. As shown in Fig. 6.8, it uses AC coupling capacitances (C_c) and large resistors (R_b) to bias its input transistors at the desired current levels, and simultaneously block input common-mode variations. The biasing voltages (V_{bni}, V_{bpi}, V_{bnc}, and V_{bpc}) are generated by a constant-g_m biasing circuit.



(a) Fully-differential (b) Pseudo-differential

Figure 6.6: Fully-differential (a) and pseudo-differential (b) amplifiers.

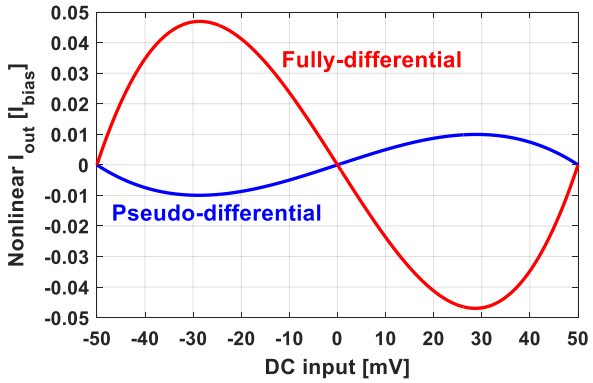


Figure 6.7: Nonlinear components of I_{out} for fully-differential and pseudo-differential amplifiers.

The combination of R_b and C_c behaves like a high-pass input filter. Setting its corner frequency below the audio band (< 20 Hz) would require extremely large resistors and/or capacitors making this approach impossible to integrate. Instead, choppers are used to up-modulate audio signals to f_{chop} before this filter, and then to demodulate them back into an output DC current. In this way, the high-pass filter's corner frequency only has to be lower than f_{chop}. To avoid down-converting the quantization noise present at the virtual ground node, the choppers are driven at the sampling frequency ($f_{chop} = f_s$) [8]. Since the output choppers are placed in a high bandwidth node, between the input devices and the cascodes, the DC gain reduction due to these is negligible.

For linearity, the coupling capacitors ($C_c = 2$ pF) are implemented as metal fringe capacitors and designed to be much larger than the gate capacitances of the input transistors to minimize signal attenuation and excess noise. The polysilicon biasing resistors ($R_b = 3$ MΩ) are chosen to ensure that the high-pass corner frequency is much less than f_s. In the layout, R_b is placed under C_c to reduce the total area of the four R_b-C_c pairs to 0.01 mm^2.

The NMOS input transistors are split in a 6:1 ratio, with the smaller branch being used for common-mode feedback (CMFB). A continuous-time CMFB circuit is used to sense and

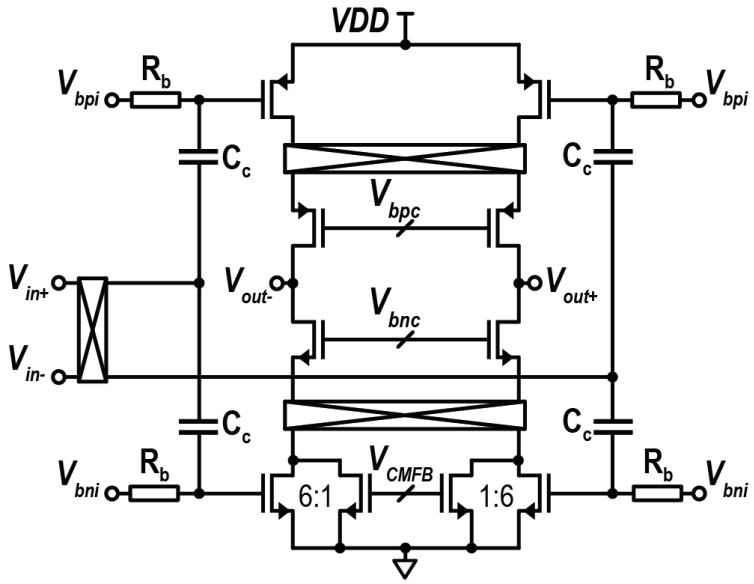


Figure 6.8: Simplified schematic of the proposed amplifier.

stabilize the amplifier's output common-mode voltage [16]. The input and output choppers also chop the offset and low-frequency noise contributed by the CMFB loop itself.

The total power consumption of the amplifier is 205 μW including the chopper drivers, biasing and CMFB circuits. Its nominal and minimum DC gains are 60 dB and 55 dB respectively over process, voltage, and temprature corners (-55 °C to 150 °C, 1.6 V to 2 V). The amplifier's simulated CMRR is greater than 70 dB up to 1 kHz. Its simulated PSRR is greater than 100 dB up to 1 kHz, and greater than 50 dB for higher frequencies due to chopping.

The noise and distortion specifications of the 2^{nd} and 3^{rd} integrators are relaxed by the gain preceding them. They are implemented with current-starved inverters similar to the ones used in the implementation in Chapter 4, each consuming 15 μW while providing 45 dB DC gain.

6.2.3 DAC

The DAC of the zoom ADC is one of its most critical blocks, as it directly impacts its total input-referred noise, total harmonic distortion (THD), and clock jitter sensitivity. An non-return-to-zero (NRZ) DAC is preferred for high energy efficiency and low jitter sensitivity. The input voltage is converted to a current (I_{in}) via R_{in} as shown in Fig. 6.9. After subtracting the DAC current (I_{DAC}), their difference (I_{OTA}) is then integrated. The maximum value of I_{OTA} defines the output current requirements of the OTA, and hence its power consumption. The maximum input current ($I_{in,max}$) for a sinusoidal input with amplitude $V_{in,max}$ is:

$$I_{in,max} = \frac{V_{in,max}}{\mathrm{R_{in}}}. \tag{6.4}$$

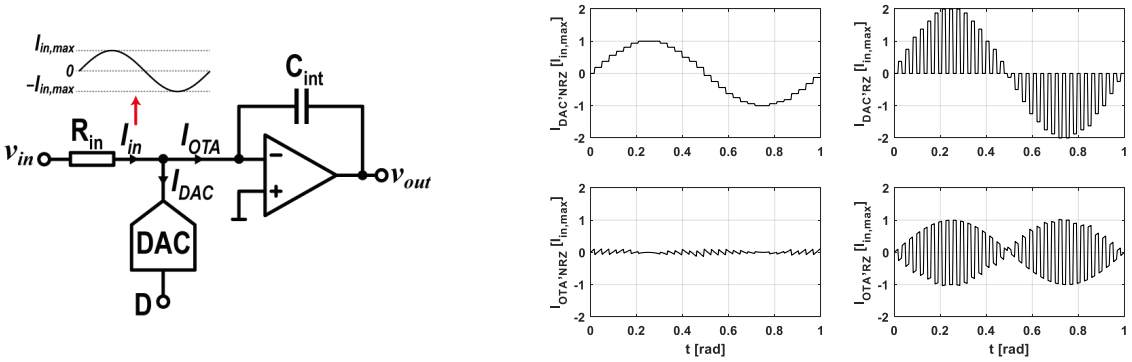


Figure 6.9: I_{DAC} and I_{OTA} for NRZ and RZ DACs.

Time-domain waveforms of I_{DAC} and I_{OTA} for NRZ and return-to-zero (RZ) DACs for a zoom ADC based on a 3-bit coarse ADC are given in Fig. 6.9. For an NRZ DAC, the difference between I_{in} and I_{DAC} is constant, and decreases as the resolution of the coarse DAC is increased. For an RZ DAC, however, this difference is much larger. When I_{DAC} is zero I_{OTA} should be as large as $I_{in,max}$. Moreover, the jitter sensitivity of an NRZ DAC is considerably better than that of an RZ DAC. Thus, an NRZ DAC is used in this work. There are two ways to implement a 2-level NRZ DAC: as a current DAC (I-DAC), or as a resistive DAC (R-DAC). Due to the its higher linearity and lower noise, an R-DAC is used in this work.

ISI refers to the signal-dependent errors that occur at code transitions due to the finite rise/fall times of the currents generated by the unit elements of the R-DAC. The use of DWA makes this problem even worse because it increases the number of unit-element transitions in the DAC and introduces even-order distortion [7]. In this work, a novel ISI reduction technique is proposed to solve this problem. In the output of the differential R-DAC unit element shown in Fig. 6.10, there are four different transition edges: t_{rp}, t_{rn}, t_{fp}, and t_{fn}. If the total amount of positive and negative DAC output currents within one period would match, there would be no nonlinear ISI error [7]. One approach to achieve this is to match a rising edge with its corresponding falling edge (match t_{rp} and t_{fn}, and match t_{rn} and t_{fp}) [4, 5]. However, this is hard to guarantee in practice, since the speed of the rising edges is set by PMOS drivers, while the speed of the falling edges is set by NMOS drivers. Thus, background calibration is often necessary for this approach [4, 5].

Alternatively, we note that to avoid ISI it is only necessary to match the rising and falling edges of the positive and the negative half DACs (match t_{rp} and t_{rn}, and match t_{fn} and t_{fp}).

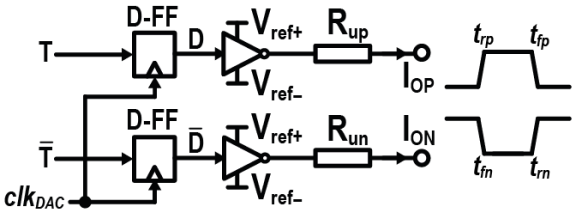


Figure 6.10: Simplified schematic of an R-DAC cell.

This is comparatively easy to achieve because the edges that need to be matched are generated by the same type of devices. However, the positive and the negative DAC unit resistors also need to match, as they also influence the resulting rise and fall times. Simulations indicated that the 1% matching needed for low DWA in-band noise, is also more than enough to achieve < -120 dB HD2. The positive and negative half DACs should then be laid out next to each other. Noting that the on-resistances of the DAC switches are much smaller than R_{up} and R_{un}, the matching requirements on the driver inverters can be relaxed to 5%. The switch driving signal (D and $\overline{D}$) asymmetry, which is also a source of ISI error, is reduced by using two separate flip-flops to drive D and $\overline{D}$ as shown in Fig. 6.10.

6.2.4 Asynchronous SAR ADC and Alias Rejection

The asynchronous SAR ADC used in this work is similar to the one in Chapter 5, but with smaller DAC unit capacitors (1.8 fF) to reduce the peak currents drawn from the input, resulting in a total sampling capacitance of 55 fF. Due to its input sampler, the asynchronous SAR ADC could alias the signals around f_s back to DC. This could be prevented by utilizing an all-pass filter [17]. However, the passive elements required to implement an all-pass filter for the chosen f_s would occupy a large area. In this work, we propose to use a simple 1^{st}-order RC low-pass filter as shown in Fig. 6.4 to suppress the signal components around f_s instead. Simulations showed that $R_{filt} = 20\,k\Omega, C_{filt} = 5$ pF is enough to achieve better than 65 dB alias rejection around f_s.

6.3 Measurement Results

As shown in Fig. 6.11, the prototype CT zoom ADC occupies 0.27 mm^2 in 0.16 μm CMOS technology. The input resistors, R-DAC, loop filter, SAR ADC, and digital logic occupy 18%, 18%, 53%, 4% and 7% of the total area, respectively. The ADC consumes 618 μW from a 1.8 V supply. The analog, reference, clock, and digital circuitry consume 45%, 28%, 13%, and

14%, respectively, of this total power as shown in Fig. 6.11. The first integrator dominates the analog power consumption. The voltage references are externally generated (V_{ref+} = 1.8 V and V_{ref-} = 0 V).

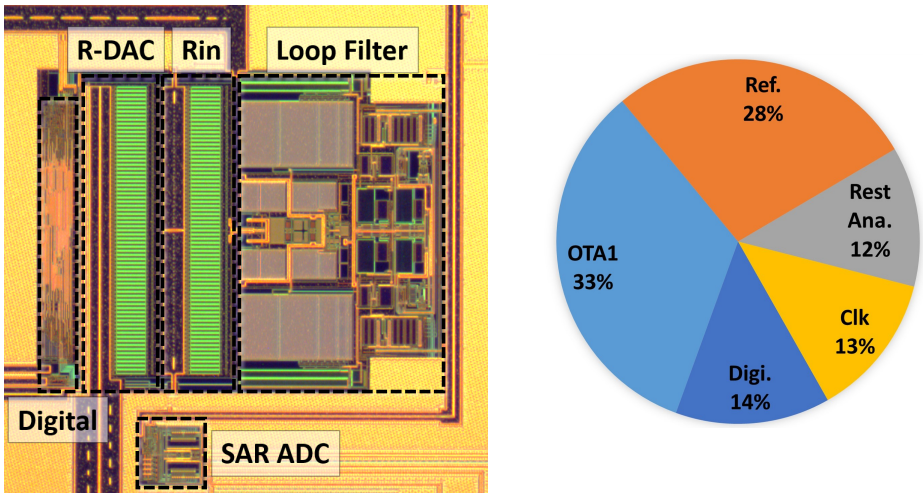


Figure 6.11: Chip photograph and power breakdown.

The measured output spectrum of the ADC is shown in Fig. 6.12. When no input signal applied (V_{in} = 0), the ADC effectively operates like a 3^{rd}-order 1-bit DSM. The in-band tones seen in this case are due to DWA. Peak SNDR is achieved with an input of -0.15 dBFS. HD3 is the dominant distortion component at -113 dB, and all other harmonic components are below -120 dB. The tones at 50 Hz and 150 Hz are due to the signal generator. The measured peak SNR, SNDR, and DR are 108.1 dB, 106.5 dB, and 108.5 dB, respectively (Fig. 6.13).

Fig. 6.14 shows HD2 and HD3 levels for -1 dBFS single-tone in-band input signals. HD3 is lower than -113 dB and HD2 is lower than -125 dB for all frequencies. Low HD2 levels prove the efficacy of the proposed ISI mitigation technique. The apparent increase in HD2 and HD3 at higher frequencies is due to the increased quantization noise at these frequencies. The signal-dependent unit transitions caused by DWA makes the current drawn from the reference signal-dependent [7]. To illustrate this, the current drawn from V_{ref+}, I_{ref}, is measured with an audio analyzer. The measured power spectrum of I_{ref} is shown in Fig. 6.15 for f_{in} = 1 kHz and for DWA "on" and "off." It can be seen that DWA causes even-order tones in I_{ref}. The mixing of these even-order components with the input signal via the finite output impedance of the reference is thus the main reason for the odd-order harmonic components (HD3-9) seen in Fig. 6.12.

The measured INL of the SAR ADC is 0.15 LSB. The ADC's measured CMRR and PSRR at 50 Hz are greater than 70 dB and 100 dB respectively, and its $1/f$ corner is lower than 20

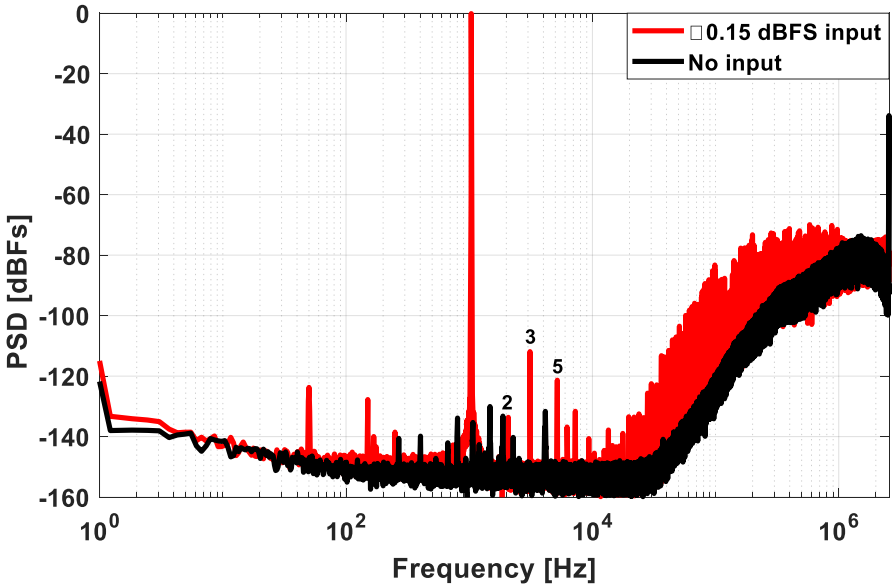


Figure 6.12: Measured output spectrum (-0.15 dBFS input signal at 1 kHz, and no signal. 2^{23} points 8 average with Hanning window)

Hz, demonstrating the performance benefits of the capacitively-coupled chopped OTA. The measured alias rejection of the ADC is then higher than -72 dB for -6 dBFS input signals as shown in Fig. 6.16.

Table 6.1 summarizes the performance of the proposed CT zoom ADC and compares it with that of other state-of-the-art audio ADCs at the time of publication of [9]. The proposed ADC outperforms all the others in terms of peak SNDR and FOM. Although the DT zoom ADC presented in Chapter 4 achieves similar peak DR and SNR, it requires much stronger input drivers. The input impedance of the proposed CT zoom ADC is essentially resistive, and so can be easily driven.

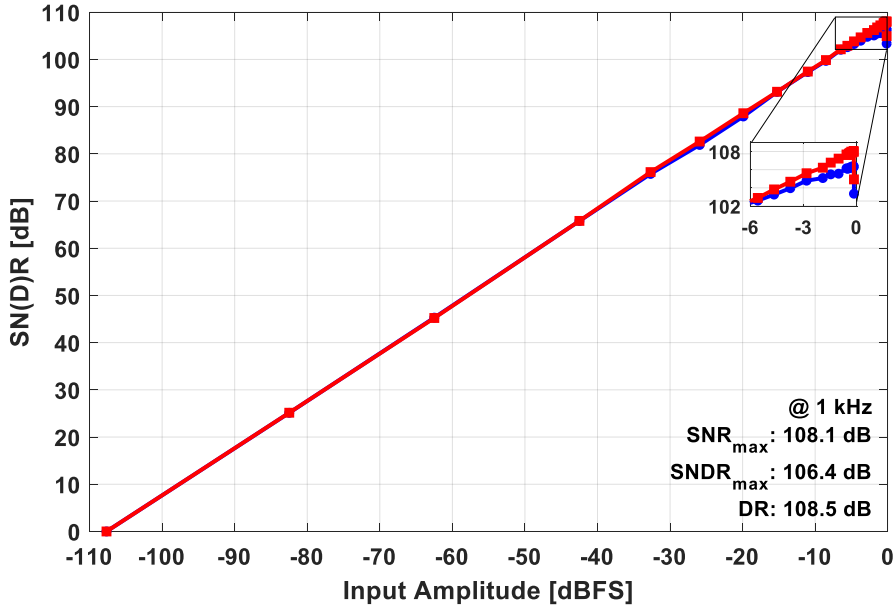


Figure 6.13: Measured SNR and SNDR across input amplitude.

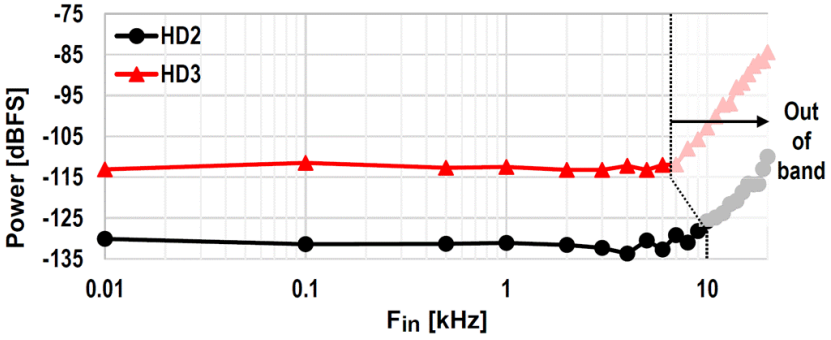


Figure 6.14: HD2 and HD3 across input frequency.

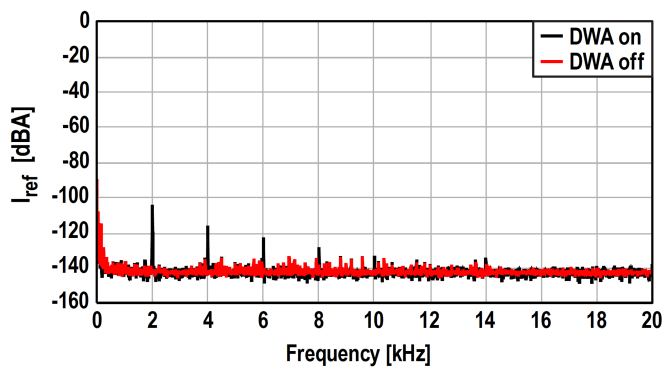


Figure 6.15: Measured I_{ref} power spectrum for DWA on and off.

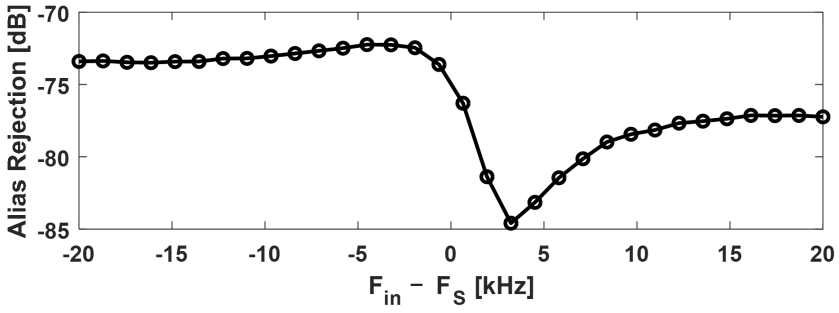


Figure 6.16: Measured alias rejection of the CT zoom ADC around f_s.

Table 6.1: Performance summary and comparison with previous work.

	Unit	This Work	Jang [18]	Karmakar [2]	Gönen [1]	de Berti [19]	Billa [4]
Year	-	2019	2019	2017	2016	2016	2016
Technology	nm	160	65	160	160	160	180
Die area	mm^2	0.27	0.14	0.25	0.16	0.21	1.33
Power consumption	µW	618	68	280	1.12	0.39	0.28
Sampling frequency	MHz	5.12	6.144	2	11.29	3	6.144
Signal bandwidth	kHz	20	24	1	20	20	24
Peak SNR	dB	108.1	94.8	119.1	106	93.4	99.3
Peak SNDR	dB	106.4	94.1	118.1	103	91.3	98.5
DR	dB	108.5	98.2	120.3	109	103.1	103.6
$^{\dagger}FOM_{SNDR}$	dB	181.5	179.5	183.6	175.5	170.5	177.8
$^{\dagger\dagger}FOM_{DR}$	dB	183.6	183.6	185.8	181.5	180.2	182.9

$^{\dagger}FOM_{SNDR} = SNDR + 10\log(\text{Signal bandwidth} \,/\, \text{Power})$
$^{\dagger\dagger}FOM_{DR} = DR + 10\log(\text{Signal bandwidth} \,/\, \text{Power})$.

6.4 References

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Chapter 7

Conclusions

In this thesis, the development of energy-efficient zoom ADCs for audio and instrumentation applications has been investigated. This chapter summarizes the main findings of this research, discusses other applications of the developed techniques, and includes some proposals for future work.

7.1 Main Findings

The main findings of this thesis can be summarized as follows:

- The key way to improve the energy efficiency of a high-resolution delta-sigma modulator (DSM) is by lowering the input swing of its loop-filter. Low input swing reduces the effects of amplifier nonlinearity, making it possible to reduce amplifier energy consumption (Chapter 2).

- The energy consumption of the critical first integrator of a high-resolution DSM is determined by the requirements on its nonlinearity rather than on its thermal noise (Chapter 2).

- In high-resolution and low-bandwidth applications, discrete-time DSMs (DTDSM) can be more energyefficient than their continuous-time (CT) counterparts. Due to the exponential settling behavior of switched-capacitor integrators, amplifier nonlinearity, and hence energy efficiency, can be readily improved by allowing more time for settling. In contrast, continuous-time integrators are considerably more sensitive to amplifier nonlinearity (Chapter 2).

- Zoom ADCs are inherently energy-efficient. This is because their two-step architecture drastically reduces the input swing of the loop filter. The in-band matching between their coarse and fine DACs, often a problem with two-step architectures, is achieved in a simple and compact manner by using a single DAC together with over-ranging and dynamic element matching (DEM) (Chapter 3).

- Unlike prior zoom ADCs based on sequential two-step conversion, which were too slow for audio applications, the dynamic zoom ADCs proposed in this thesis solve this problem by employing concurrent coarse and fine conversions. This makes the signal bandwidth of zoom ADCs comparable to that of conventional multi-bit DSMs (Chapter 3).

- The extra tones or "fuzz" often seen in the output spectrum of a zoom ADC are due to the non-unity signal transfer function (STF) of its fine DSM which results in leakage of the coarse SAR ADC quantization error. This can be reduced considerably by using digital filtering of the coarse SAR ADC output, or analog techniques to achieve a unity STF (Chapter 3).

- Data weighted averaging (DWA) shapes static DAC unit-mismatch errors to higher frequencies. However, its 1^{st}-order shaping characteristic often limits the minimum oversampling ratio (OSR) that can be used in higher-order DSMs. This, in turn, also limits the minimum digital power consumption (Chapter 3).

- The fine converter of a zoom ADC can be implemented either as a discrete-time or as a continuous-time DSMs. However, discrete-time modulators can achieve some $2\times$ better energy efficiency. A discrete-time design achieves a FOM of 185.8 dB, while a continuous-time design with similar specifications, achieved 183.6 dB (Chapter 4-6).

- Due to the reduced loop-filter swing of a zoom ADC, the area of the associated integration capacitors can be reduced significantly (Chapter 4). Due to their relatively short conversion time, using an asynchronous SAR ADC as the coarse ADC of a zoom ADC results in much better robustness to large out-of-band signals. It also minimizes the amount of over-ranging required, resulting in lower loop-filter swing, and higher overall energy efficiency (Chapter 5).

- The increased DAC switching activity associated with DWA may limit the linearity of a CTDSM. The associated DAC currents create voltage drops on the parasitic resistances in series with the DAC's voltage reference, thus modulating the reference voltage and creating odd-order harmonic tones (Chapter 6).

These findings emerged during the implementation of the designs presented in Chapters 4 – 6 [1–3] as given in . As shown in Fig. 7.1, these designs (the red dots in the plot) improved the energy efficiency of high-resolution ADCs by an order of magnitude compared to the state-of-the-art at the beginning of this thesis (2014). In the meantime, several other designs have also achieved similar energy efficiency [4–14]. Closer inspection reveals that they do this by using architectural and circuit techniques to reduce the signal swing in their loop filters, which is one of the key findings of this thesis. A comparison of the state-of-the-art high-resolution ADCs is presented in Table 7.1.

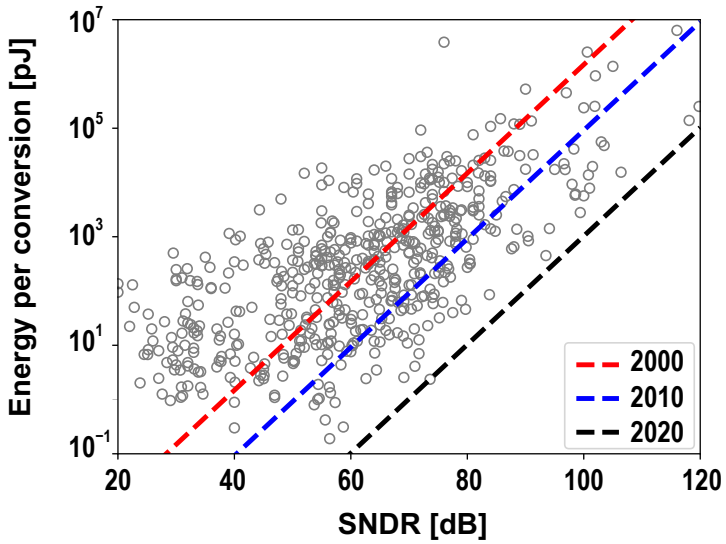

Figure 7.1: Energy-per-conversion vs SNDR for the ADCs published in last two decades (Based on the data presented in [15]).

The DSMs presented in [6] and [5] use multi-bit DACs to reduce the loop filter swing and achieve 180.2 dB and 177.9 dB FOM[1] respectively. The energy efficiency of a multi-bit DSM is further improved in [8] by utilizing an asnychronous SAR ADC as a quantizer and using a gain stage preceding the first integrator. These techniques, combined with the low input swing of the ADC (200 mV peak-to-peak) helped it to achieve a FOM of 187 dB.

The designs presented in [4] and [7] use a finite-impulse-response DAC (FIR-DAC) to filter the quantizer's output, thus reducing loop-filter swing and achieving 182.3 dB and 182.9 dB FOM respectively. In [4], it was shown that the signal swing reduction achieved by a FIR-DAC alone is limited and is equivalent to the use of a 12-level quantizer. For further loop filter swing reduction, a FIR-DAC is combined with a multi-bit quantizer [10] to achieve 105.3 dB

[1]FOM based on DR is chosen to compare the designs presented in Table 7.1.

Table 7.1: Comparison of state-of-the-art high resolution ADCs.

	Year	Arch.	Area	P	BW	SNR	SNDR	DR	FOM (SNDR)	FOM (DR)
	-	-	mm^2	µW	kHz	dB	dB	dB	dB	dB
Ch. 4 [1]	**2016**	**DT-zoom**	**0.16**	**1120**	**20**	**106**	**103**	**109**	**175.5**	**181.5**
Ch. 5 [3]	**2017**	**DT-zoom**	**0.25**	**280**	**1**	**119.1**	**118.1**	**120.3**	**183.6**	**185.8**
Ch. 6 [2]	**2019**	**CT-zoom**	**0.27**	**618**	**20**	**108.1**	**106.4**	**108.5**	**181.5**	**183.6**
Mondal [14]	2021	CT FIR-DAC	0.39	139	24	102	100.9	104.8	183.3	187.2
Eland [13]	2021	DT-zoom	0.27	440	20	107.5	106.5	109.8	183.1	186.4
Jang [12]	2021	CT 3-lvl FIR & -R	0.28	134	24	101	99.4	103.5	181.9	186
Billa [11]	2020	CT FIR-DAC MASH	0.64	550	24	101.7	100.9	104	179.6	182.7
Theertham [10]	2020	CT N-bit FIR-DAC	2.85	24e3	250	108.2	105.3	107.5	175.5	177.7
Jang [12]	2019	CT 3-lvl & -R	0.14	68	24	94.8	94.1	98.2	179.5	183.6
Chandra. [8]	2018	CT N-bit & gain	0.05	4.5	5	94.3	93.5	96.5	184	187
Billa [7]	2017	CT FIR-DAC	1.33	280	24	99.3	98.5	103.6	177.8	182.9
de Berti [6]	2016	CT N-bit	0.21	390	20	93.4	91.3	103.1	170.5	180.2
Leow [5]	2016	CT N-bit	0.25	800	25	100.1	95.2	103	175	177.9
Sukumaran [4]	2016	CT FIR-DAC	1.25	280	24	98.9	98.2	103	178.2	182.3

$\text{FOM (SNDR)} = \text{SNDR} + 10\log(\text{Signal bandwidth / Power})$
$\text{FOM (DR)} = \text{DR} + 10\log(\text{Signal bandwidth / Power})$.

SNDR in 250 kHz bandwidth, resulting in 177.7 dB FOM. The design presented in [11] uses a 1-N MASH architecture combined with FIR-DAC. While 1-bit 1^{st}-order coarse DSM achieves close to full scale maximum stable input amplitude, the FIR-DAC helps to reduce the signal swing seen by the fine DSM, similar to a zoom ADC. This design achieves a FOM of 182.7 dB for audio applications.

The designs presented in [9] reduce the input swing of the amplifiers by applying negative-resistance (negative-R) at the virtual ground of these. This technique helps to not only reduce the input swing of the amplifiers but also improve their bandwidth while intorducing thermal noise, which is very suitable for high-resolution ADCs since the linearity is the main problem as discussed in Chapter 2. The design with 1.5-bit quantizer achieves 183.6 dB FOM, proving the strenght of this technique. In [12], the negative-R assistance is combined with a 1.5-bit FIR-DAC to further reduce the input swing if the amplifiers and the design achieved 186 dB FOM.

The DT-zoom ADC design presented in [13] used a 2-bit quantizer in its fine DSM to further reduce the loop filter input-swing compared to previous zoom ADCs and achieved 186.4 dB FOM (DR). A recent design presented in [14] made use of both circuit and architectural techniques to boost the energy efficiency of an audio ADC and achieved 187.2 dB FOM. This design stacked 3 amplifiers similar to the one used in [2] combined with a FIR-DAC.

7.2 Other Applications of This Work

The analysis of the impact of noise and nonlinearity on the energy-efficiency of high-resolution DSMs presented in Chapter 2 can be used as a framework to analyze the energy efficiency limits of other analog circuits and systems. It can be extended to noise-shaping or Nyquist-rate SAR ADCs, whose energy consumption is typically dominated by their reference buffers and comparators. DSMs based on Gm-C integrators, or VCO-based quantizers can also be analyzed by using similar principles. Although quite area-efficient, implementations of the latter are often less efficient than conventional DSMs, and to the best knowledge of the author, the fundamental reasons behind this are not yet fully understood.

The system and circuit level design techniques introduced in this thesis can be applied to capacitance-to-digital converters (CDCs). For example, the signal bandwidth of the zoom CDC presented in [16, 17] could probably be improved by adopting a dynamic zoom ADC architecture. The conversion speed of zoom CDCs can then be improved by orders of magnitude, making them suitable for high-speed capacitive sensing applications, e.g., when capacitive displacement sensors are to be used in a control loop [18].

The impact of amplifier nonlinearity, which is analyzed in detail in this thesis, also affects analog front-ends for sensor readout, as discussed in [19]. An improved version of the pseudo-differential amplifier presented in Chapter 6 has been used for high-resolution Wheatstone-bridge readout [20]. Noting that the loop-filter swing of a zoom ADC is quite small, the capacitively-coupled input of this amplifier lends itself to amplifier stacking, which leads to even higher efficiency [14]. Similarly, the switched-capacitor amplifier described in Chapter 4 can be used in conventional DSMs [21], and can potentially also be stacked.

Although the work described in this thesis has focused on audio applications, the zoom ADC architecture can be extended to larger bandwidths. A recent work investigates this possibility and shows that the zoom ADC can be implemented with input signal bandwidths required for wireless communication applications [22].

7.3 Future Work

While this work represents a significant step in improving the energy efficiency of high-resolution ADCs, it does not represent the end of this quest. Future work will undoubtedly aspire to reach the theoretical energy efficiency levels presented in Chapter 2.

A logical way to reduce the energy efficiency of the analog circuits of a zoom ADC would be to further reduce the input swing of its loop-filter. Using a 2-bit quantizer in the fine DSM [13], indeed reduced loop-filter input swing, and hence improved energy-efficiency considerably (from 181.5 dB [1] to 186.4 dB [13] FOM). In principle, a FIR-DAC and a 1-bit quantizer could be used to achieve the same result. Further amplitude reduction by increasing the coarse ADC resolution could also be investigated. In the adopted technology node, this was avoided to keep the digital power consumption low.

The digital circuits of the designs presented in this thesis had a large share on the total power consumption: 29% (Chapter 4), 27% (Chapter 5), and 27% (Chapter 6). The power consumption of the digital circuits is a linear function of the sampling frequency (f_s), which needs to be reduced to its lowest possible for low power consumption. In the implementations presented in this thesis, the use of DWA was the main constraint on reducing f_s. As discussed in Chapter 3, DWA only provides 1^{st}-order shaping of the DAC mismatch error while consuming considerable power. For a given DAC unit mismatch and desired in-band SNDR specification, the use of DWA results in a minimum OSR requirement. One way to reduce this is to use higher-order mismatch noise shaping techniques. Unfortunately, these are too complicated to be implemented with low power consumption in mature technology nodes [23]. Adopting advanced technology nodes such as 28 nm will be necessary to investigate the

efficacy of such techniques. The possibility of using thick-oxide devices for analog blocks while using core devices for low power digital will allow the overall partitioning of the design to be optimized for the highest energy efficiency. For the more mature technology nodes, such as the 0.16 μm process adopted in this thesis, accurate calibration methods can be a potential solution. Since background calibration methods will most likely consume a considerable amount of power, and considering the DAC unit mismatch is often static, a fast and accurate foreground calibration method would be the best solution.

A surprising finding of the analysis presented in Chapter 2 was that DTDSMs are potentially more efficient than CTDSMs for the same performance specifications. This is confirmed by the excellent efficiency of recent discrete-time zoom ADCs [1, 3, 13], which outperform similar continuous-time designs. Discrete-time ADCs, however, are known to require power-hungry input and reference drivers. DTDSM input impedance boosting techniques by using low-power coarse buffers [24], and recent work done in reducing SAR ADC reference buffer power consumption [25], shows that discrete-time designs can potentially also achieve excellent efficiency including their input and reference drivers. Further investigation into how the power consumption of these blocks can be reduced would therefore be a promising line of future research.

The zoom ADC architecture could also be used to improve the linearity of VCO-based or Gm-C based DSMs, which are known to suffer from poor linearity. The former can be very compact, and so they are under active investigation [26, 27]. The latter can potentially reduce the energy consumption of the loop-filter since the amplifier does not need to drive a feedback network. So far, Gm-C-based DSMs have not been able to deliver on this promise due to their rather limited (a few hundred millivolts) linear input range. Incorporating them in a zoom ADC architecture might be a promising way to drastically reduce their input swings, and potentially achieve better performance than the use of multi-bit DACs alone [28].

7.4 References

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Appendix A

Thermal Noise Limited Energy Consumption in Integrators

A.1 Switched-Capacitor Integrator

The simplest switched-capacitor circuit is a sample and hold circuit shown in Fig. A.1. Energy required to drive a sample and hold with a certain SNR could be used as a lower limit for the ADC conversion energy. If a simple sample and hold circuit is driven by a signal $\hat{V_{in}}cos(\omega t)$ the signal power is:

$$P_{signal} = \frac{\hat{V_{in}^2}}{2} \tag{A.1}$$

Let's assume the sampling frequency is equal to the Nyquist bandwidth, i.e. $f_s = 2\,f_{bw}$, and a complete sampling is achieved. The integrated noise power in $0 - f_{bw}$ bandwidth is:

$$P_{noise} = \bar{v}_n^2 = \frac{kT}{C_s}. \tag{A.2}$$

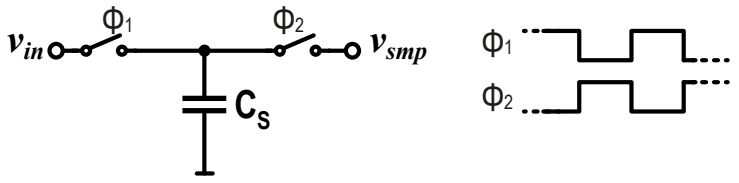

Figure A.1: A simple sample and hold.

The resulting SNR is then found as:

$$\text{SNR} = \frac{P_{signal}}{P_{noise}}. \tag{A.3}$$

The sampling capacitance could be defined in terms of SNR and $\hat{V}_{in}$ as:

$$C_s = \frac{2kT\,\text{SNR}}{\hat{V}_{in}^2}. \tag{A.4}$$

The energy stored on a capacitor is given as:

$$E = CV^2. \tag{A.5}$$

Assuming the sampling capacitor is discharged at each cycle, the root-mean-square (RMS) power required to drive the signal into C_s is found from (A.5) as:

$$P = E\,f_s = \frac{\hat{V}_{in}^2}{2} f_s C_s \tag{A.6}$$

which could be rewritten by substituting (A.4) into (A.6) as:

$$P = f_s kT\ \text{SNR}. \tag{A.7}$$

The consumed energy is found to be:

$$E_{min} = kT\ \text{SNR} \tag{A.8}$$

Fig. A.2 shows a typical switched-capacitor first stage of a discrete-time delta-sigma modulator (DTDSM) in which the sampling capacitor is also used to implement its feedback DAC. This means that the capacitance is sampled twice, thus doubling the total sampled noise. C_s must then be doubled to maintain the same SNR:

$$C_s = \frac{4kT\,\text{SNR}}{\hat{V}_{in}^2} \tag{A.9}$$

The charge transfer activity happens twice in the integrator shown in Fig. A.2 compared to the sample and hold shown in Fig. A.1, thus the power consumption is now:

$$P_{min,DT} = \hat{V}_{in}^2 f_s C_s \tag{A.10}$$

which can be rewritten by using (A.9) as:

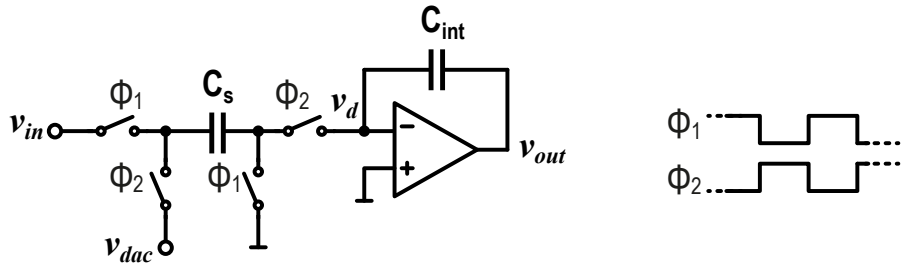

Figure A.2: DTDSM input stage with single capacitor.

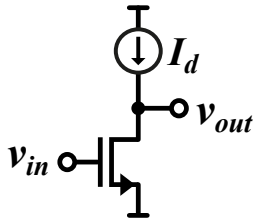

Figure A.3: Single transistor amplifier

$$P_{min,DT} = 4kT\,\mathrm{SNR}\,f_s. \tag{A.11}$$

The energy consumed per conversion then found as:

$$E_{min,DT} = 4kT\ \mathrm{SNR}. \tag{A.12}$$

A.1.1 Amplifier Noise

In the analysis above, the amplifiers were assumed to be noiseless. The single transistor amplifier shown in Fig. A.3 is the simplest possible building block used as the input stage of amplifiers. Ignoring $1/f$ noise, its integrated thermal noise in a given bandwidth, f_{bw}, can be expressed as [1]:

$$\bar{v}_{n,in}^2 = \frac{4kT\,f_{bw}}{g_m} \tag{A.13}$$

where g_m is the transconductance of the transistor. However, amplifiers often use more devices than a single transistor, and each of them contribute to noise. Thus, a noise excess factor (Γ_n) can be defined to account for this [1]:

$$\Gamma_n = \frac{\bar{v}_{n,amp}^2}{\bar{v}_{n,in}^2} \tag{A.14}$$

where $\bar{v}_{n,amp}^2$ is the total input-referred noise of the amplifier in the given bandwidth. The total input-referred noise of the SC input stage shown in Fig. A.2, including the amplifier thermal noise, can be divided into two parts as:

$$\bar{v}_n^2 = \bar{v}_{n,sw}^2 + \bar{v}_{n,amp}^2 \tag{A.15}$$

where $\bar{v}_{n,sw}^2$ is due to the switch related noise and $\bar{v}_{n,amp}^2$ is the amplifier related noise. Switch related noise can be expressed as [2]:

$$\bar{v}_{n,sw}^2 = \left(1 + \frac{2R_{on}g_m}{2R_{on}g_m + 1}\right) \frac{kT}{\mathrm{OSR}\, C_s} \tag{A.16}$$

where R_{on} is the series switch resistance during integration phase, and OSR is the oversampling ratio. Assuming $g_m R_{on} \ll 1$, which is often the case for integrator, and $\mathrm{OSR} = 1$ without loss of generality, (A.16) simplifies into:

$$\bar{v}_{n,sw}^2 = \frac{kT}{C_s}. \tag{A.17}$$

The amplifier related noise is given in [2] can be expressed by using by using (A.13) and (A.14) as:

$$\bar{v}_{n,amp}^2 = \left(\frac{\Gamma_n}{1 + 2R_{on}g_m}\right) \frac{kT}{\mathrm{OSR}\, C_s}. \tag{A.18}$$

Using A.17 and A.18 which for $g_m R_{on} \ll 1$, and $\mathrm{OSR} = 1$ simplifies into:

$$\bar{v}_{n,amp}^2 = \Gamma_n \frac{kT}{C_s}. \tag{A.19}$$

(A.15) can then be rewritting by using (A.17) and (A.19) as:

$$\bar{v}_n^2 = \frac{(1 + \Gamma_n)\, kT}{C_s} \tag{A.20}$$

from which we can find C_s as:

$$C_s = \frac{(1 + \Gamma_n)\, kT}{\bar{v}_n^2}. \tag{A.21}$$

By using (A.1) and (A.3) we can rewrite (A.21) for $P_{noise} = \bar{v}_n^2$ as:

$$C_s = \frac{2\,(\Gamma_n + 1)\, kT\ \mathrm{SNR}}{\hat{V}_{in}^2}. \tag{A.22}$$

The power consumption of the integrator is then found by using (A.10) as:

$$P_{th,DT} = 2\,(\Gamma_n + 1)\,kT\ \mathrm{SNR}\ f_s. \tag{A.23}$$

The energy consumed in one conversion period is then given by:

$$E_{th,DT} = 2\,(1 + \Gamma_n)\,kT\ \mathrm{SNR} \tag{A.24}$$

which is equal to (A.12) for $\Gamma_n = 1$.

A.2 Continuous-Time Integrator

The total input referred noise for this input stage shown in Fig. A.4 is:

$$v_{n,in}^2 = 4\,kT\,R_{in}\,f_{bw}(1 + \frac{R_{in}}{R_{dac}}). \tag{A.25}$$

For $R_{in} = R_{dac}$, it will be:

$$v_{n,in}^2 = 8\,kT\,R_{in}\,f_{bw}. \tag{A.26}$$

The SNR is then found as:

$$\mathrm{SNR} = \frac{\hat{V}_{in}^2}{16\,kT\,R_{in}\,f_{bw}}. \tag{A.27}$$

The input resistance $R_{in,0}$ can be expressed as:

$$R_{in,0} = \frac{\hat{V}_{in}^2}{16\,kT\,\mathrm{SNR}\,f_{bw}}. \tag{A.28}$$

Power consumed to drive the input resistance is then:

$$P_{in} = \frac{\hat{V}_{in}^2}{2R_{in}}. \tag{A.29}$$

Using (A.27) we can rewrite (A.29) as:

$$P_{in} = 8\,kT\,\mathrm{SNR}\,f_{bw} \tag{A.30}$$

Assuming infinitely small quantization error, the power consumed to drive R_{dac} is equal to the one for R_{in}, so that the total power consumption is doubled:

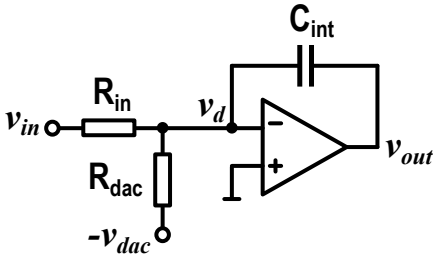

Figure A.4: CTDSM input stage with R-DAC.

$$P_{min,CT} = 16kT\,\mathrm{SNR}\,f_{bw}. \tag{A.31}$$

The total energy consumed in one conversion period $\left(f_s = \frac{1}{2f_{bw}}\right)$ is found then as:

$$E_{min,CT} = 8kT\,\mathrm{SNR}. \tag{A.32}$$

A.2.1 Amplifier Noise

Analysis above assumes a noiseless amplifier. In reality, the amplifier in Fig. A.4 will exhibit thermal noise. Assuming $R_{in} = R_{dac}$, the input-referred noise of Fig. A.4 can be written as:

$$\bar{v}^2_{n,in} = 2\bar{v}^2_{n,R} + 4\bar{v}^2_{n,amp} \tag{A.33}$$

where $\bar{v}^2_{n,amp}$ is the input-referred thermal noise of the amplifier, and $\bar{v}^2_{n,R}$ is the resistor noise. Ignoring $1/f$ noise, $\bar{v}^2_{n,amp}$ could be written from (A.13) and (A.14) as [1]:

$$\bar{v}^2_{n,amp} = \frac{4kT\,\Gamma_n\,f_{bw}}{g_m}. \tag{A.34}$$

The resistor noise $\bar{v}^2_{n,R}$ is:

$$\bar{v}^2_{n,R} = 4kT\,R_{in}\,f_{bw}. \tag{A.35}$$

By substituting (A.34) and (A.35) in (A.33):

$$\bar{v}^2_{n,in} = 8kT\,f_{bw}(R_{in} + \frac{2\,\Gamma_n}{g_m}). \tag{A.36}$$

The SNR of the CT input stage then is:

$$\mathrm{SNR} = \frac{\hat{V}_{in}^2}{16kT\, f_{bw}\left(R_{in} + \frac{2\Gamma_n}{g_m}\right)}. \tag{A.37}$$

From (A.37) R_{in} could be expressed as:

$$R_{in} = \frac{V_{in}^2}{16kT\,\mathrm{SNR}\, f_{bw}} - \frac{2\Gamma_n}{g_m}. \tag{A.38}$$

The first part of (A.38) is equal to $R_{in,0}$, which is the input resistance determined by SNR for an integrator with a noiseless amplifier given by (A.28). The second part of (A.38) represents the amplifier noise, which could be expressed as an equivalent resistor as:

$$R_{amp} = \frac{2\Gamma_n}{g_m}. \tag{A.39}$$

(A.38) then becomes:

$$R_{in} = R_{in,0} - R_{amp} \tag{A.40}$$

The power consumed by the input and the reference could be found by using (A.29) and (A.31) as:

$$P_{in,ref} = \frac{\hat{V}_{in}^2}{R_{in}} = \frac{\hat{V}_{in}^2}{R_{in,0} - R_{amp}}. \tag{A.41}$$

(A.41) is higher than (A.31), because R_{in} is lower than $R_{in,0}$ due to the thermal noise of the amplifier. This could be defined as excess power consumption factor (η_P):

$$\eta_P = \frac{P_{min,CT}}{P_{in,ref}} = \frac{R_{in,0}}{R_{in,0} - R_{amp}} = \frac{1}{1 - \frac{2\Gamma_n}{g_m R_{in,0}}} \tag{A.42}$$

which can be rewritten by using (A.39) and (A.40) in a more intuitive form as:

$$\eta_P = 1 + \frac{2\Gamma_n}{g_m R_{in}}. \tag{A.43}$$

η_P becomes unity for $g_m R_{in} \gg 2\Gamma_n$.

Power consumed to drive the input and the reference is calculated by using η_P as:

$$P_{th,CT} = \eta_P\, 8kT\,\mathrm{SNR}\, f_{bw}. \tag{A.44}$$

Energy consumed per conversion to drive the input and the reference is then found as:

$$E_{th,CT} = \eta_P \, 8 \, kT \, \mathrm{SNR} \tag{A.45}$$

which is equal to (A.32) for $\eta_P = 1$.

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Appendix B

Impact of Amplifier Nonlinearity in Integrators

B.1 Continuous-Time Integrator

Effect of first stage's g_m nonlinearity in the integrator shown in Fig. B.1 which is often used as the first stage of a continuous-time delta-sigma modulator (CTDSM) will be analyzed. The third order nonlinearity will be assumed as the most dominant error source. The output current of the amplifier, which is assumed to be a single-stage amplifier, could be expressed as:

$$i_{out} = g_m v_d - g_{m3} v_d^3 \tag{B.1}$$

where g_m and g_{m3} are the linear transconductance of the amplifier and its third order component respectively, and v_d is the virtual ground voltage. (B.1) can be re-written as:

$$i_{out} = g_m v_d - \lambda\, g_m v_d^3 \tag{B.2}$$

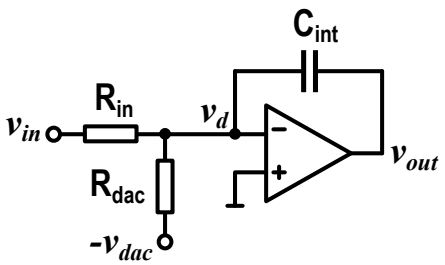


Figure B.1: The CT integrator.

where

$$\lambda = \frac{g_{m3}}{g_m} \tag{B.3}$$

is a nonlinearity coefficient. The the resulting third order nonlinearity error is found in [1] as:

$$\varepsilon_{D3} = \frac{2\lambda}{(2+g_m R_{in})^3}(v_{in} - v_{dac})^3. \tag{B.4}$$

where v_{in} is the input signal defined as:

$$v_{in} = \hat{V_{in}} cos(\omega t). \tag{B.5}$$

Considering the v_{dac} will be a good representation of the v_{in} for $f_{in} \ll f_s$ and assuming a non-return-to-zero (NRZ) DAC switching, the approximate value of $(v_{in} - v_{dac})^3$ and for a 1-bit modulator is found in [2] as:

$$\left|(v_{in} - v_{dac})^3\right| \approx \frac{\hat{V_{in}^3}}{2} cos(\omega t). \tag{B.6}$$

$v_{in} - v_{dac}$ in (B.19) would be reduced by $2\times$ for each increased number of bits (N) of the DAC[1]. Thus, $(v_{in} - v_{dac})^3$ could be rewritten as:

$$\left|(v_{in} - v_{dac})^3\right| = \frac{\hat{V_{in}^3}}{2^{3N-2}} cos(\omega t) \tag{B.7}$$

By using (B.7) we can rewrite (B.19) as:

$$\varepsilon_{D3} = \frac{\lambda}{(2+g_m R_{in})^3} \frac{\hat{V_{in}^3}}{2^{3N-3}} cos(\omega t). \tag{B.8}$$

The third order harmonic distortion (HD3) is defined as:

$$\text{HD3} = \frac{\varepsilon_{D3}}{v_{in}}. \tag{B.9}$$

The HD3 for a N-bit CTDSM can then be found by using (B.5), (B.8) and (B.9) as:

$$\text{HD3} = \frac{\lambda}{2^{3N-3}(2+g_m R_{in})^3} \hat{V_{in}^2}. \tag{B.10}$$

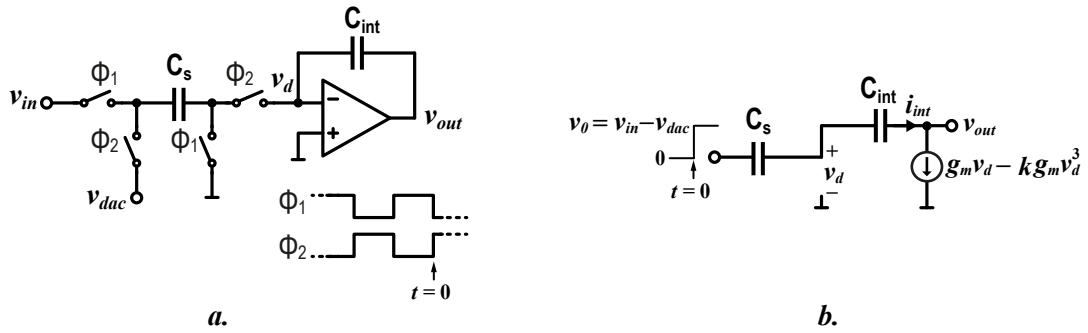


Figure B.2: a) The SC integrator. b) The small signal equivalent during the integration phase (Φ_2).

B.2 Switched-Capacitor Integrator

Fig. B.2.a shows the switched-capacitor (SC) integrator with a single stage amplifier which is often used in discrete-time DSMs (DTDSM). Its small signal equivalent during the integration phase is shown in Fig. B.2.b. The input voltage is a step function which has an amplitude of $v_0 = v_{in} - v_{dac}$ at $t = 0$. This means the voltage at the input of the amplifier at $t = 0$ is:

$$v_d(0) = v_{in} - v_{dac} \tag{B.11}$$

The output current of the amplifier in Fig. B.2 could be expressed as:

$$i_{out} = g_m v_d - \lambda\, g_m v_d^3. \tag{B.12}$$

The Kirchhoff's current law equation for the virtual ground node is:

$$g_m v_d\,(1 - \lambda v_d^2) = -C_s \frac{dv_d}{dt}. \tag{B.13}$$

(B.13) can be analytically solved by using the initial condition given in (B.11). The result at the end of the settling time t_{set} is:

$$v_d = \frac{1}{\sqrt{\lambda + \left(\frac{1}{(v_{in}-v_{dac})^2} - \lambda\right) e^{2n_\tau}}} \tag{B.14}$$

where n_τ is the settling time constant of the integrator expressed as:

$$n_\tau = \frac{g_m t_{set}}{C_s}. \tag{B.15}$$

[1] Verified in simulation.

Note that (B.14) will give the linear settling equation for $\lambda = 0$:

$$v_d = (v_{in} - v_{dac})\, e^{-n_\tau}. \tag{B.16}$$

For $n_\tau > 1$ and $g_m v_d \ll 1$ (B.14) could be approximated as:

$$v_d \approx e^{-n_\tau}\,(v_{in} - v_{dac}) + \frac{\lambda}{2}\, e^{-n_\tau}\,(v_{in} - v_{dac})^3. \tag{B.17}$$

The error on the integrated charge is expressed as:

$$Q_{int} = C_s\, v_d. \tag{B.18}$$

Thus, v_d in (B.17) directly gives the error at the end of the integration period. The nonlinear error at the end of the settling period could be found as:

$$\varepsilon_{D3} = \frac{\lambda}{2}\, e^{-n_\tau}\,(v_{in} - v_{dac})^3 \tag{B.19}$$

By using (B.6) we can rewrite (B.19) as:

$$\varepsilon_{D3} = \frac{\lambda\, e^{-n_\tau}}{4} \hat{V}_{in}^3 cos(\omega t). \tag{B.20}$$

The HD3 for a N-bit DTDSM can then be found by using (B.5), (B.9) and (B.20) as:

$$\mathrm{HD3} = \frac{\lambda\, e^{-n_\tau}}{2^{3N-1}} \hat{V}_{in}^2 \tag{B.21}$$

B.3 References

[1] P. Sankar and S. Pavan, "Analysis of integrator nonlinearity in a class of continuous-time delta-sigma modulators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 12, pp. 1125–1129, Dec. 2007.

[2] L. Breems and J. H. Huijsing, *Continuous-Time Sigma-Delta Modulation for A/D Conversion in Radio Receivers*. Springer, Boston, MA, 2001.

Appendix C

Amplifier Energy Consumption

C.1 Amplifiers in Switched-Capacitor Integrators

A detailed analysis of the energy efficiency of switched-capacitor amplifiers is done in [1]. In this section, we will take a similar approach to analyze the effect of amplifier energy efficiency in switched-capacitor (SC) integrators. It is shown in [1] that settling time constant n_τ a very important design parameter for defining amplifier energy efficiency. Assuming the switch resistances are negligable, n_τ is defined for the integrator with a single stage amplifier shown in Fig. C.1 as:

$$n_\tau = \frac{g_m t_{set}}{C_s} \tag{C.1}$$

where t_{set} is the total settling time during the integration period, and g_m is the transconductance of the single stage amplifier which can be expressed as [1]:

$$g_m = 2 I_d V_{gt} \tag{C.2}$$

where I_d is the bias current, and V_{gt} is the overdrive voltage of the amplifier. Note that V_{gt} is constant and equal to roughly 80 mV for weak inversion [1]. The current (I_d) required to have n_τ settling in half a clock period ($t_{set} = 0.5T_s$) could be found from (C.1) and (C.2) as:

$$I_d = n_\tau f_s C_s V_{gt} \tag{C.3}$$

C_s is found in Appendix A as:

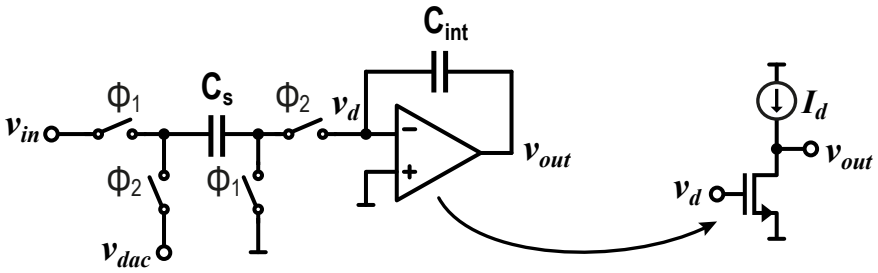


Figure C.1: SC integrator with single stage amplifier.

$$C_s = \frac{2\,(\Gamma_n + 1)\,kT\ \mathrm{SNR}}{\hat{V}_{in}^2} \tag{C.4}$$

where $\hat{V_{in}}$ is the amplitude of the input signal, Γ_n is the noise excess factor of the amplifier defined in Appendix A, and SNR is the desired signal-to-noise ratio. By substituting (C.4) in (C.3) we arrive at:

$$I_d = \frac{2\,kT\,(1+\Gamma_n)\,n_\tau V_{gt}\,f_s\,\mathrm{SNR}}{\hat{V}_{in}^2} \tag{C.5}$$

The input signal swing could be expressed as a fraction of the supply voltage (V_{dd}) as:

$$2\hat{V}_{in} = \eta_v V_{dd}. \tag{C.6}$$

In most of the amplifiers there are more than one current branch. To account for this excess current, we can define a current efficiency factor as the ratio of a single transistor amplifier to the actual circuit current

$$\eta_c = \frac{I_{single}}{I_{circuit}} \tag{C.7}$$

From (C.6) and (C.7), the total current of a single-stage amplifier is:

$$I_{amp} = \frac{8\,kT\,(1+\Gamma_n)\,n_\tau V_{gt}\,f_s\,\mathrm{SNR}\,(1+\Gamma_n)}{\eta_v^2\,\eta_c\,V_{dd}^2} \tag{C.8}$$

and its power consumption is:

$$P_{amp} = \frac{8\,kT\,(1+\Gamma_n)\,n_\tau V_{gt}\,f_s\,\mathrm{SNR}\,(1+\Gamma_n)}{\eta_v^2\,\eta_c\,V_{dd}} \tag{C.9}$$

The energy consumption of the amplifier per conversion is then found as:

$$E_{amp} = \frac{8kT\,(1+\Gamma_n)\,n_\tau V_{gt}\,\mathrm{SNR}\,(1+\Gamma_n)}{\eta_v^2\,\eta_c V_{dd}} \tag{C.10}$$

which can be rewritten by using $E_{min} = kT$ SNR which is derived in Appendix A as:

$$E_{amp} = 8\,E_{min}\,(1+\Gamma_n)\,\frac{V_{gt}}{\eta_v^2\,\eta_c V_{dd}}\,n_\tau \tag{C.11}$$

C.2 Amplifiers in Continuous-Time Integrators

The same analysis will be performed for an amplifier used in a continuous-time (CT) integrator. The current required for a single transistor amplifier for a given g_m is found via (C.2) as:

$$I_d = \frac{g_m V_{gt}}{2} \tag{C.12}$$

The SNR of a CT integrator is found in Appendix A as:

$$\mathrm{SNR} = \frac{\hat{V}_{in}^2}{16kT\,f_{bw}\left(R_{in} + \frac{2\Gamma_n}{g_m}\right)} \tag{C.13}$$

from which g_m can be found for $f_s = 2\,f_{bw}$ as:

$$g_m = \frac{8kT\,\mathrm{SNR}\,f_s\,(g_m R_{in} + 2\Gamma_n)}{\hat{V}_{in}^2} \tag{C.14}$$

where $g_m R_{in}$ is a design parameter which plays a role in the linearity and the noise performance of the integrator as found in Appendix B, similar to n_τ in a SC integrator. The current required for a single transistor amplifier is then found via (C.2):

$$I_d = \frac{4kT\,\mathrm{SNR}\,V_{gt}\,f_s\,(g_m R_{in} + 2\Gamma_n)}{\hat{V}_{in}^2} \tag{C.15}$$

By using η_v and η_c defined by (C.6) and (C.7), the power consumption of the amplifier is found as:

$$P_{amp} = \frac{16kT\,\mathrm{SNR}\,V_{gt}\,f_s\,(g_m R_{in} + 2\Gamma_n)}{\eta_v^2\,\eta_c V_{dd}} \tag{C.16}$$

Energy consumption of the amplifier per conversion is then:

$$E_{amp} = \frac{16\,kT\,\mathrm{SNR}\,V_{gt}\,f_s\,(g_m R_{in} + 2\Gamma_n)}{\eta_v^2\,\eta_c\,V_{dd}} \tag{C.17}$$

C.3 References

[1] K. Bult, M. S. Akter, and R. Sehgal, "High-efficiency residue amplifiers," in *Low-Power Analog Techniques, Sensors for Mobile Devices, and Energy Efficient Amplifiers : Advances in Analog Circuit Design 2018*, Springer, 2019, pp. 253–296.

Appendix D

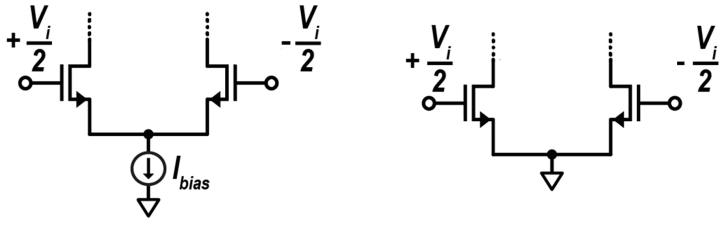
Linearity Analysis of Fully-Differential and Pseudo-Differential Amplifiers

In this Appendix, an analysis of the input pairs shown in Fig. D.1 is performed to compare their linearity. In order to not limit the analysis to only one operation region, i.e. weak, moderate, or strong inversion, the transconductance-to-current ratio (g_m/I_D) based method in conjunction with EKV model proposed in [1] is used. The drain current of a transistor in saturation

$$I_D = 2nV_T^2 \mu C_{ox} \frac{W}{L}(q^2 + q) \tag{D.1}$$

where q is the normalized mobile charge density at the source, n is the subthreshold slope, and V_T is the thermal voltage. The relation between the gate drive voltage and q is given as:

$$V_{GS} - V_{TH} = nV_T[2(q-1) + \log(q)] \tag{D.2}$$



(a) Fully-differential (b) Pseudo-differential

Figure D.1: Fully-differential (a) and pseudo-differential (b) amplifiers.

where V_{TH} is the threshold voltage. g_m/I_D could be then found as [1]:

$$\frac{g_m}{I_D} = \frac{1}{nV_T(q+1)}. \tag{D.3}$$

By using (D.3) q can be expressed as:

$$q = \frac{1}{(nV_T \frac{g_m}{I_D})} - 1. \tag{D.4}$$

Due to the differential operation, even order nonlinearity components will be zero. For this analysis, we will take only the third-order distortion into account. The output current then be written by using the power series expansion:

$$i_d = g_m v_{gs} + \frac{1}{6} g_{m3} v_{gs}^3. \tag{D.5}$$

Linear and the third-order components of the transconductance, g_m and g_{m3}, are given in [1] for a pseudo-differential stage as:

$$g_{m,PD} = \frac{I_s q}{nV_T}, \tag{D.6}$$

$$g_{m3,PD} = \frac{I_s q}{(nV_T)^3(2q+1)^3}. \tag{D.7}$$

HD3 could be found for the pseudo-differential input pair shown in Fig. D.1 by using (D.1)-(D.7) for a differential sinusoidal input signal with $v_{i,pk}$ amplitude:

$$\mathrm{HD3_{PD}} \approx \frac{1}{16}\left|\frac{g_{m3}}{6g_m}\right| v_{i,pk}^2 = \frac{1}{96}\left(\frac{1}{nV_T}\right)^2 \frac{1}{(2q+1)^3} v_{i,pk}^2 \tag{D.8}$$

g_m and g_{m3} are given in [1] for a fully-differential input stage as:

$$g_{m,FD} = \frac{I_s q}{nV_T}, \tag{D.9}$$

$$g_{m3,FD} = -\frac{I_s q(3q+1)}{2(nV_T)^3(2q+1)^3}. \tag{D.10}$$

HD3 of the fully-differential input pair is found in [1] as:

$$\mathrm{HD3_{FD}} = \frac{1}{48}\left(\frac{1}{nV_T}\right)^2 \frac{(3q+1)}{(2q+1)^3} v_{i,pk}^2. \tag{D.11}$$

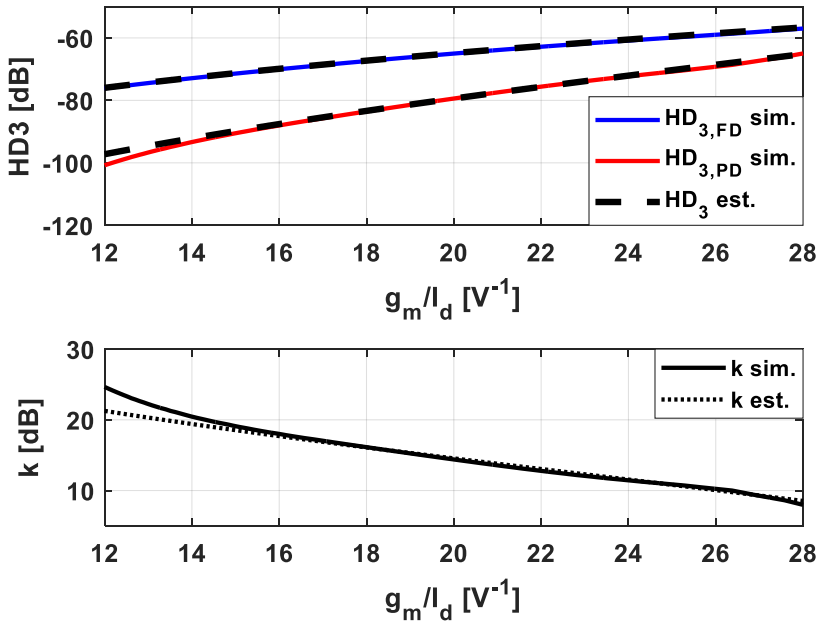


Figure D.2: HD3 and k vs g_m/I_D for pseudo-differential and fully-differential input pairs (L = 0.7μm).

The ratio of HD3_{FD} to HD3_{PD}, k, is then found from (D.8) and (D.11) as:

$$k = \frac{\text{HD3}_{\text{FD}}}{\text{HD3}_{\text{PD}}} = 6q + 2. \tag{D.12}$$

Using (D.1) - (D.4) we can find k in terms of g_m/I_D, n and V_T as:

$$k = \frac{6}{\frac{g_m}{I_D} n V_T} - 4. \tag{D.13}$$

The only one process technology related parameter required for (D.13) is n. g_m/I_D is a very useful design parameter that determines the achievable g_m for a given bias current I_D. Fig. D.2 shows simulated HD3 and k for the fully-differential and pseudo-differential NMOS input pairs for different g_m/I_D values, both driven by a sinusoidal input with $v_{i,pk} = 10$ mV. The HD3 and k values estimated after extracting $n = 1.25$ from the used 0.16 μm process are also shown in dashed lines. The simulated and estimated results are in good agreement, and they show that for all operation regions the pseudo-differential pair is more linear than its fully-differential counterpart. k is at least 8 dB for weak inversion (high g_m/I_D), it increases to more than 20 dB for strong inversion (lower g_m/I_D). Note that the above analysis and simulations do not include the output impedance nonlinearity.

The nonlinearity coefficient λ which is defined in Appendix B can be derived from (D.5)

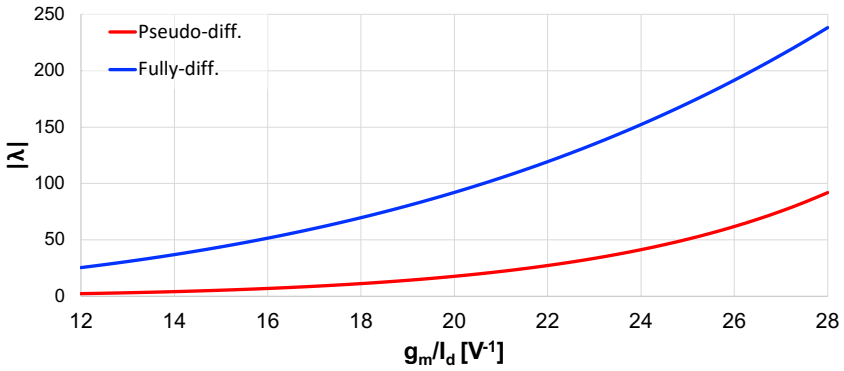


Figure D.3: Calculated $|\lambda|$ vs g_m/I_D for pseudo-differential and fully-differential input pairs (L = 0.7μm).

as:

$$\lambda = \frac{g_{m3}}{6g_m} \tag{D.14}$$

which can be found for the pseudo-differential input pair by using (D.6), (D.7) and (D.14) as:

$$\lambda_{PD} = \frac{1}{6(nV_T)^2(2q+1)^3}, \tag{D.15}$$

and for the fully-differential input pair as:

$$\lambda_{FD} = -\frac{3q+1}{3(nV_T)^2(2q+1)^3}. \tag{D.16}$$

Fig. D.3 shows the calculated absolute values of λ_{PD} and λ_{FD} versus g_m/I_D for the 0.16 μm process.

D.1 References

[1] P. G. A. Jespers and B. Murmann, "Calculation of MOSFET distortion using the transconductance-to-current ratio (gm/ID)," in *Proc. IEEE Int. Symp. Circuits and Systems*, Lisbon, Portugal, 2015, pp. 529–532.

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List of Publications

Journal Papers

- E. Eland, S. Karmakar, **B. Gönen**, R. van Veldhoven, and K. A. A. Makinwa, "A 440-μW, 109.8-dB DR, 106.5-dB SNDR discrete-time zoom ADC with a 20 kHz BW," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 4, pp. 1207–1215, Apr. 2021.
- **B. Gönen**, S. Karmakar, and R. van Veldhoven K. A. A. Makinwa, "A continuous-time zoom ADC for low-power audio applications," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, pp. 1023–1031, Apr. 2020.
- S. Karmakar, **B. Gönen**, F. Sebastiano, R. V. Veldhoven, and K. A. A. Makinwa, "A 280 μW dynamic zoom ADC with 120dB DR and 118dB SNDR in 1kHz BW," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 12, pp. 3497–3507, Dec. 2018.
- **B. Gönen**, F. Sebastiano, R. Quan, R. van Veldhoven, and K. A. A. Makinwa, "A dynamic zoom ADC with 109-dB DR for audio applications," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 6, pp. 1542–1550, Jun. 2017.

Conference Papers

- E. Eland, S. Karmakar, **B. Gönen**, R. van Veldhoven, and K. A. A. Makinwa, , "A 440μW, 109.8dB DR, 106.5dB SNDR discrete-time zoom ADC with a 20 kHz BW," in *Proc. Symp. VLSI Circuits*, Jun. 2020, pp. 1–2.
- **B. Gönen**, S. Karmakar, and R. van Veldhoven K. A. A. Makinwa, "A low power continuous-time zoom ADC for audio applications," in *Proc. Symp. VLSI Circuits*, Jun. 2019, pp. 1–2.
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- **B. Gönen**, F. Sebastiano, R. van Veldhoven, and K. A. A. Makinwa, "A 1.65mW 0.16mm^2 dynamic zoom-ADC with 107.5dB DR in 20kHz BW," in *Dig. Tech. Papers ISSCC*, Jan. 2016, pp. 282–283.

- L. Xu, **B. Gönen**, Q. Fan, J. H. Huijsing and K. A. A. Makinwa, "A 110dB SNR ADC with ±30V input common-mode range and 8μV Offset for current sensing applications," in *Dig. Tech. Papers ISSCC*, Feb. 2015, pp. 1–3.

Book Chapters

- **B. Gönen**, F. Sebastiano, R. van Veldhoven, and K. A. A. Makinwa, "A Hybrid ADC for High Resolution: The Zoom ADC" in *Hybrid ADCs, Smart Sensors for the IoT, and Sub-1V & Advanced Node Analog Circuit Design*. Springer, 2018, pp. 99–117.

Patents

- **B. Gönen**, F. Sebastiano, R. van Veldhoven, and K. A. A. Makinwa, "Efficient Analog to Digital Converter", US Patent US9325340, Apr. 2016

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Burak Gönen received the B.Sc. degree in electronics from Istanbul Technical University, Istanbul, Turkey, in 2012, and the M.Sc. degree (cum laude) in microelectronics from the Delft University of Technology, Delft, The Netherlands, in 2014, where he has pursued the Ph.D. degree, with a focus on the design of energy- and area-efficient analog-to-digital converters for digital audio and sensor interfaces, in collaboration with NXP Semiconductors, Eindhoven, The Netherlands. From 2011 to 2012, he was an Intern with Mikroelektronik Ar-Ge Ltd., Istanbul. From 2013 to 2014, he was an Intern with NXP Semiconductors. From 2012 to 2019, he was with Electronic Instrumentation Laboratory, Delft University of Technology. In 2019, he was a Senior Analog IC Design Engineer with Broadcom, Bunnik, The Netherlands. Recently, he joined Ethernovia, Zeist, The Netherlands, as a Senior Member of Technical Staff.

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