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ZVS Turn-on integrated Triangular Current Mode Three-phase PFC for EV On-board Chargers

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***Abstract*—An efficient, compact and lightweight three-phase AC-DC power factor correction (PFC) converter becomes a necessity for electric vehicles (EVs) On-board chargers (OBCs) in conventional grid-to-vehicle (G2V) and vehicle-to-grid (V2G) charging methods. The commercially available OBCs have very limited power density despite the moderate efficiency under specific power levels. In this paper, the integrated triangular current mode (iTCM) control is implemented to improve the power density (kW/L) and specific power (kW/kg) of the three-phase PFC converter stage while maintaining high efficiency. Zero voltage switching (ZVS) turn-on is realized in the iTCM control with a higher switching frequency to reduce the LCL filter size without sacrificing efficiency. By adding an LC branch between the bridge leg and mid-point of the DC link, the high-frequency and low-frequency currents are split to minimize the inductor loss and to derive a better inductor design. Analytical modeling and simulation in PLECS are conducted to verify the idea of iTCM. The capacitor-current feedback active damping method is implemented to prevent instability from the LC and LCL filters. The design of an 11kW three-phase AC-DC PFC converter, including the input LCL filter, achieves an efficiency of 98.81%, a power density of 12.46 kW/L and a specific power per weight of 1.87 kW/kg. The proposed three-phase iTCM control is benchmarked in a 3 kW SiC MOSFET-based AC-DC converter.**

***Index Terms*—On-board chargers, power factor correction, integrated triangular current mode, zero voltage switching**

I. Introduction

Due to the increasing concern of global warming and the rapid development of renewable energy resources, switching to Electric Vehicles (EVs) has become highly attractive. The on-board charger (OBC) plays an important role in charging at home or the workplace on the daily basis because of its flexibility and convenience. Moreover, the bidirectional OBCs ensure the possibility of future vehicle-to-grid (V2G) charging, which is defined as feeding or storing electric energy to the grid by using the EVs battery to provide ancillary services to the grid, such as peak shaving and/or frequency regulation [1].

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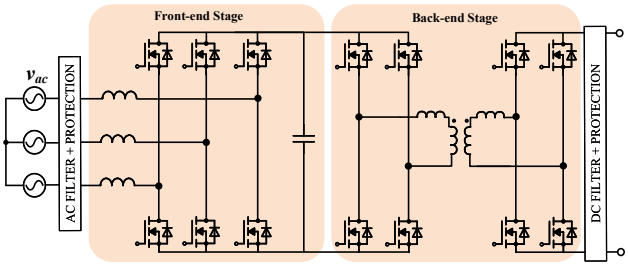


Fig. 1. Example of a two-stage high power OBC configuration suitable to G2V and V2G charging

The two-stage bidirectional OBCs are the mostly used configuration in commercial EVs, as shown in Fig.1 [2]. The front-end stage is an AC-DC power factor correction (PFC) converter connected to the power grid via an AC filter. The PFC converter provides a controllable DC voltage for the back-end stage DC-DC converter, and it also regulates the current to meet the grid standards and codes, and provides a high power factor operation ($\geq$0.99). An efficiency of up to 99% can be achieved for PFC converters which employ GaN or SiC MOSFET switches operating at the hard-switching continuous current mode (CCM) [2]. However, due to the thermal management and cost restrictions, the hard-switching operation will pose a limit to the maximum switching frequency, and thus will affect the maximal achievable power density of the system. In most commercial cases, the PFC systems used in OBCs have a power density of around 3 kW/L, mainly because a large AC filter is needed to meet the grid-connected current harmonics requirement [2]. The volume and weight of the typical LCL-based current harmonic filter commonly take up the largest part of the converter, sometimes more than 80% [3]. Therefore, PFC converters operating at CCM with low switching frequency often lead to a low power density (kW/L) and low specific power (kW/kg) merits.

To improve the power density and specific power of the PFC converter stage, a high switching frequency can be selected to optimize the size of the LCL input filter. Meanwhile, an increment in switching frequency will lead to a higher switching loss of the semiconductors and penalize not only power efficiency but also the thermal management system. Therefore, a clear trade-off between efficiency and power density or specific power is necessary for designing the PFC converter. When operating at relatively high frequencies, the soft turn-on switching is of great necessity to improve the efficiency of the

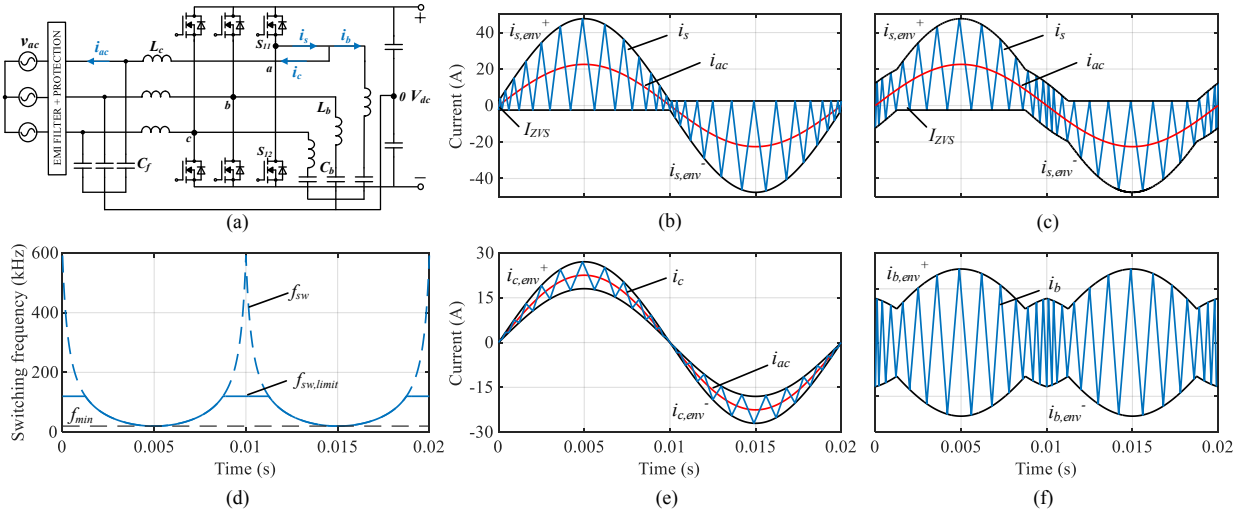


Fig. 2. (a) Three-phase AC-DC PFC converter with an additional LC branch allowing the usage of iTCM control for OBCs; (b) The semiconductor current i_s in TCM or iTCM with constant reversal current I_{zvs}; (c) The semiconductor current i_s with a maximum 120 kHz switching frequency limitation; (d) The switching frequency (f_{sw}) of the TCM or iTCM (the dash line) and the switching frequency with a maximum 120 kHz limitation (the solid line); (e) The L_c current with a small ripple r; (f) The LC branch current i_b with most high-frequency component (Taking one converter phase and few switching periods in one main-frequency period as illustration)

converter as the turn-on loss can take expressively high values, e.g., more than 70% of the total loss even in wide-bandgap (WBG) semiconductors like SiC MOSFET [4].

There are multiple ways to achieve soft switching turn-on. The addition of extra components is sometimes explored, but this will increase the physical complexity and most likely will also impair the gain of power density and specific power [3]. The state-of-art control methods like the triangular current mode (TCM) control and boundary current control (BCM) are good alternatives to achieve soft switching by zero-voltage-switching (ZVS) turn-on [5].

In the TCM control method, the semiconductor current reaches a certain value in the opposite direction in each switching period, which makes the voltage of the parasitic capacitance drop to zero during the resonance period. It ensures that the anti-parallel diode conducts before turning on the switch so that fully ZVS turn-on is achieved [3]. However, in the PFC application, the filter inductor current in TCM has an intrinsic large ripple, containing both the low-frequency and high-frequency components, which could cause higher inductor and semiconductor conduction losses.

To minimize the inductor loss and to achieve a simplified inductor design, the integrated triangular current mode (iTCM) control is proposed in [6], [7]. The basic idea is to split the high- and low-frequency components of the current by adding an extra LC branch between the bridge-leg and DC-link. Because of the high-pass characteristic of the LC branch, most of the high-frequency current flows through the LC branch, which stays circulating within the PFC circuit, while the low-frequency current with relatively small ripple flows into the converter-side line inductor L_c in the direction of the AC grid. The current flowing into the semiconductors remains similar to in TCM so that the ZVS turn-on is safeguarded. The iTCM strategy can outweigh the TCM one in terms of AC filter power density. The inductor with low-frequency current can be designed by powder iron core, while the inductor with high-frequency current can be designed by ferrite core with litz wire to minimize the losses. Another advantage is that only the low-frequency current with a small ripple flows to the grid so that a small input filter can be used for the grid-connection. Furthermore, simple pulse width modulation (PWM) method can be implemented, and extra wide-band current measurement devices which are necessary for an accurate zero cross detection are not needed [5].

However, based on the knowledge of the authors in all research found in the literature, the iTCM control method is only used in DC-DC converters or single-phase AC-DC PFC applications [6] [7]. Moreover, the close-loop control is not implemented in the previous research [6]. Resonance of the added LC branch would cause an instability problem when merged with the LCL input filter. In [6], only the passive damping method is applied to suppress the LCL and LC branch resonances. This method is simple and reliable but at the cost of extra losses [8]. In this paper, an iTCM modulated three-phase grid-connected AC-DC PFC converter is proposed, and the active damping method is developed to stabilize the system.

The rest of this paper is structured as follows. In Section II, the basic concept of the three-phase grid-connected AC-DC PFC converter with iTCM control for OBCs is presented. In Section III, semiconductor and inductor loss are modeled. Besides, an inductor design procedure is introduced. Section IV presents the comparative analysis of three-phase PFC rectifiers operating with CCM, TCM and iTCM based on

TABLE I
SYSTEM SPECIFICATIONS

PARAMETER	$v_{\rm ac}$	P	f_0	$V_{\rm dc}$	M
VALUE	230 V RMS	11 kW	50 Hz	800 V	0.8132

TABLE II
POLYNOMIAL COEFFICIENT OF SWITCHING ENERGY FOR SIC MOSFET C3M0120090J (PER DEVICE) TESTED UNDER V_b = 600 V

Coefficient	Turn-on Energy (E_{on}+E_{rr})	Turn-off Energy (E_{off})
a (μJ/A^2)	0.074	0.53
b (μJ/A)	10.43	5.36
c (μJ)	18.84	1.18

the derived analytical modeling results. Finally, in Section V, control with capacitor-current feedback for the iTCM is implemented, and the waveform of the iTCM is verified by simulation.

II. THERE-PHASE INTEGRATED TRIANGULAR CURRENT MODE AC-DC PFC CONVERTER

The iTCM three-phase AC-DC PFC topology proposed in this work is shown in Fig. 2(a). The DC midpoint and AC capacitor neutral point are connected to ensure three phases are decoupled and each phase can operate independently. Independent operation must be guaranteed in the three-phase TCM or iTCM since the switching frequency ($f_{\rm sw}$) of each phase has a 120° phase shift [5]. Simple sinusoidal PWM (SPWM) method can also be used in this topology, and it can be extended to space vector PWM (SVPWM) or third harmonic injection PWM (THIPWM) [5].

The current $i_{\rm s}$ flowing into the semiconductors in iTCM is a triangle wave with large ripple as shown in Fig. 2(b). The upper and lower envelope are denoted as $i^{+}_{\rm s,env}$ and $i^{-}_{\rm s,env}$ respectively. The current is in phase with the grid voltage, so the input current $i_{\rm ac}$ can be expressed as $i_{\rm ac}(t) = \hat{i}_{\rm ac}\sin(\omega_0 t)$, where $\hat{i}_{\rm ac}$ is the input peak current and ω_0 is the grid angular frequency. The current $i_{\rm s}$ goes to the reversal direction at a certain value during each switching period, which is indicated by $|I_{\rm zvs}|$. Then, the anti-parallel diode of the semiconductor can conduct before the control turns on the switch so that fully ZVS turn-on is achieved. Taking one phase-leg as an example, when S_{11} is turned off, the resonance occurs between the two parasitic capacitances of S_{11}, S_{12} and the inductors $L_{\rm c}$, $L_{\rm b}$ before turning on S_{12}. $I_{\rm zvs}$ is the desired turn-off current of S_{11} to fully discharge the parasitic capacitance of S_{12} so that the anti-parallel diode can conduct before turning on S_{12}.

In [4], u-Zi diagram has been proposed to analyze the minimum turn-off current needed to fully discharge the parasitic capacitance of the switch which will turn on. The characteristic impedance is:

$$Z = \sqrt{\frac{L}{2C_{\rm oss}}} \tag{1}$$

where $C_{\rm oss}$ is the equivalent output capacitance of each half-bridge semiconductors (assuming that the upper and bottom switches are the same), the equivalent boost inductor L is calculated by:

$$L = 1/(\frac{1}{L_{\rm c}} + \frac{1}{L_{\rm b}}) \tag{2}$$

In rectifier mode, the minimum current needed to fully discharge the parasitic capacitance when the modulation index $M > 0.5$ is [9]:

$$I_{\rm min} = \frac{V_{\rm dc}}{Z}\cdot\sqrt{|2M-1|} \tag{3}$$

where $V_{\rm dc}$ is the DC link voltage.

In both iTCM and TCM, the switching frequency ($f_{\rm sw}$) as shown in Fig. 2(d) varies with time to achieve a constant reverse current, which is expressed as:

$$f_{\rm sw} = \frac{\hat{v}^2_{\rm ac}\ (1/M - Msin^2(\omega_0 t))}{4I_{\rm zvs}\hat{v}_{\rm ac} + 8P/3\ |\sin(\omega_0 t)|}(\frac{1}{L_{\rm c}} + \frac{1}{L_{\rm b}}) \tag{4}$$

where P is the three-phase input power, $\hat{v}_{\rm ac}$ is the peak value of the AC input voltage. Note that for full power factor operation the minimum switching frequency occurs at the peak current time, which is set to be 20 kHz in this paper.

However, the switching frequency $f_{\rm sw}$ varies from 20 kHz to 591.48 kHz (effective mean switching frequency is 97.6 kHz), which poses a great challenge to practical implementation as well as to the design of the EMI filter [5]. Therefore, the switching frequency is limited to a maximum of 120 kHz in this paper as the solid line shown in Fig. 2(d). ZVS turn-on is still achieved but the reversal current is not constant due to the frequency limitation as the $i_{\rm s}$ waveform shown in Fig. 2(c). This causes a larger current ripple, higher turn-off current and turn-off loss compared to the case without frequency limitation. Since the turn-off loss of the WBG semiconductors is much smaller when compared to turn-on loss, and due to the fact the switched current is naturally smaller close to the zero-crossing of the phase current, the trade-off is acceptable.

The current $i_{\rm s}$ is divided into two parts due to the added LC branch. The capacitance $C_{\rm b}$ in the LC branch blocks DC and low-frequency current so that most of the high-frequency current would flow through the LC branch ($i_{\rm b}$) as shown in Fig. 2(f). As a result, the low-frequency current with small current ripple ($i_{\rm c}$) flows through $L_{\rm c}$ to the grid as shown in Fig. 2(e). The inductance of $L_{\rm c}$ and $L_{\rm b}$ need to be properly designed to guarantee that the average value of $i_{\rm c}$ and $i_{\rm b}$ are $i_{\rm ac}$ and 0 respectively.

The parameter r is introduced as the peak-to-peak current ripple of $i_{\rm c}$ in the percentage of the input peak current ($\hat{i}_{\rm ac}$) to determine the inductance of $L_{\rm c}$ and $L_{\rm b}$ [6]. The coefficient r varies from 0 to 200 %. When $r = 200$ %, the control scheme becomes equivalent to the TCM control since the value of $L_{\rm b}$ becomes 0. The inductance of $L_{\rm c}$ is first determined by:

$$L_{\rm c} = \frac{\hat{v}_{\rm ac}}{2P/3\ f_{\rm min}\ r}\cdot\frac{(V_{\rm dc}/2)^2 - \hat{v}^2_{\rm ac}}{V_{\rm dc}} \tag{5}$$

TABLE III
SEMICONDUCTOR LOSS MODELING RESULTS WITH FOUR HARD-PARALLELED C3M0120090J PER SWITCH UNDER CCM (20KHZ AND 97.6KHZ), TCM AND ITCM WITH SWITCHING FREQUENCY LIMITATION.

P=11kW, I_{zvs}=2.5A		Switching frequency (kHz)	P_{on} (W)	P_{rr} (W)	P_{off} (W)	P_{con} (W)	P_{loss} (W)	Efficiency(%)
	iTCM/TCM	20-591.48	0	0	49.45	36.52	85.97	99.22
C3M0120090J	iTCM_limit	20-120	0	0	47.71	37.31	85.02	99.23
V_{ds}=900V I_d=22A	iTCM_limit	20-60	0	0	47.65	42.19	89.84	99.18
R_{ds}=120mΩ	iTCM_limit	20-20	0	0	51.93	126.74	178.67	98.38
E_{on}=32μJ E_{off}=8μJ	CCM	20	15.78	0.80	7.81	25.16	49.55	99.55
	CCM	97.6	78.05	3.98	37.49	25.13	144.65	98.69

[a]Note that the efficiency calculation shown here only considers the semiconductor losses.

L_b can be subsequently subtracted from (4) and (5) to be expressed as

$$L_b = \frac{1}{f_{min}} \frac{\hat{v}_{ac}^2}{2I_{zvs}\hat{v}_{ac} + 4P/3 - 2P/3\ r} \frac{(V_{dc}/2)^2 - \hat{v}_{ac}^2}{V_{dc}} \quad (6)$$

The capacitor C_b needs to be well-designed to block the low-frequency current. It will draw some reactive power at low frequency so that the value of C_b should desirably be small. By contrast, C_b should be large enough to keep the resonance frequency of the LC branch smaller than the switching frequency to obtain an inductive behaviour, which is a necessity to achieve ZVS [7]. The LC resonant frequency $\omega_{LC,res}$ is chosen as 40000 rad/s in this paper, and hence the value of C_b can be determined by

$$\omega_{LC,res} = 1/\sqrt{L_b C_b} \quad (7)$$

III. SYSTEM MODELING

The three-phase PFC converter specifications used for the simulation and analytical modeling in this paper are shown in Table I. The semiconductors for loss modeling are the Silicon Carbide (SiC) MOSFETs (C3M0120090J [10], where four devices in parallel per switch are selected). The equivalent output capacitance of the four parallel MOSFETs is $C_{oss} \approx 355$ pF [11]. In the following analytical modeling and simulation, the minimum switching frequency is preset to be 20 kHz, and the maximum switching frequency is limited by 120 kHz. By choosing a random r between 0-200%, the equivalent boost inductance L is calculated by (2), which is 67.62 μH. Thus, the minimum turn-off current for ensuring ZVS can be calculated by (3), which is 2.05 A. To maintain a safety margin, I_{zvs} is chosen as 2.5 A. SPWM is adopted in this paper for both analytical modeling and simulation.

A. Semiconductor Loss Modeling

In the semiconductor loss modeling, the voltage in every switching period is assumed to be constant since the switching frequency f_{sw} is larger enough compared to the main frequency f_0 [11]. The switching energy (Turn-on, Turn-off and Diode reverse recovery) of the selected MOSFET is expressed as: $E_{sw}(I_{sw}) = a + b|I_{sw}| + c|I_{sw}|^2$ where E_{sw} is the switching energy, I_{sw} is the switching current. a, b and c are the polynomial coefficients which models the switching energy [11]. For the selected MOSFET, these polynomial coefficients are shown in Table II.

In iTCM, the switching frequency f_{sw} and I_{sw} are both variable, so the switching loss P_{sw} of each paralleled MOSFET can be expressed as [12]:

$$P_{sw} = \frac{V_{dc}}{2\pi V_b} \int_0^{2\pi} f_{sw}(\omega t)\ E_{sw}(I_{sw}(\omega t)/N_p) \mathrm{d}\omega t \quad (8)$$

where V_b is the reference voltage for measuring the switching energy that can be extracted from the device datasheet, and N_p is the number of MOSFETs in parallel used per switch.

The conduction loss P_{con} of each paralleled MOSFET is calculated by [13]:

$$P_{con} = R_{ds}(I_{s,rms}/N_p)^2 \quad (9)$$

where R_{ds} is the equivalent on-state resistance of each paralleled MOSFETs, $I_{s,rms}$ is the RMS value of the current i_s flowing through the active switch. The rms value of the semiconductor current during one switching period $i_{s,rms}$ can be calculated by [9]

$$i_{s,rms}^2(t) = \frac{1}{3}\left[{i_{s,env}^+}^2(t) + i_{s,env}^+(t) i_{s,env}^-(t) + {i_{s,env}^-}^2(t)\right] \quad (10)$$

Thereafter, the RMS current $I_{s,rms}$ can be calculated by integrating (10) in one grid-frequency period [12], resulting in:

$$I_{s,rms} = \sqrt{\frac{1}{3}\left(2\ \hat{i}_{ac}^2 + \frac{4}{\pi}\ \hat{i}_{ac}\ I_{zvs} + I_{zvs}^2\right)} \quad (11)$$

The semiconductor loss modeling results of different cases are summarized in Table III. Limiting the switching frequency can considerably increase the MOSFET conduction loss since the RMS value of i_s will increases because of the larger current ripple. However, the turn-off loss almost remains the same due to the intrinsically low turn-off energy found in the selected SiC MOSFET.

B. Inductor Loss Modeling

The basic approach for core loss modeling is the Steinmetz Equation (SE): $P_v = k f^\alpha B^\beta$, where P_v is the average core loss per unit volume, f is the current frequency, k, α and β are the so-called Steinmetz coefficients which is material

TABLE IV
INDUCTOR MODELING OPTIMIZATION RESULTS FROM PARETO PLOT
FOR CCM (20KHZ AND 97.6KHZ), TCM AND ITCM WITH MAXIMUM SWITCHING FREQUENCY OF 120KHZ

iTCM (20kHz-120kHz)	$L_c(\mu H)$	$L_b(\mu H)$	$C_b(\mu F)$	$L_g(\mu H)$	L_{Total} (μH)	Loss (W)	Weight(kg)	Volume (L)	THD (%)
r=0.1	1502.52	70.81	9.00	0	1573.33	99.73	14.8036	1983.45	0.2
r=0.2	751.26	74.31	8.20	0	825.57	41.23	20.0631	2471.38	0.45
r=0.3	500.84	78.18	8.00	0	579.02	45.48	16.1231	2371.38	0.69
r=0.4	375.63	82.47	7.5	0	458.1	45.34	12.3931	1571.38	0.95
r=0.5	300.50	87.26	7	0	387.76	47.44	9.3097	1359.65	1.24
r=0.6	250.42	92.64	6.80	0	343.06	44.23	9.9297	1359.65	1.56
r=0.7	214.65	98.73	6.30	0	313.38	45.69	6.9497	1008.75	1.78
r=0.8	187.82	105.68	6.00	0	293.50	45.74	5.8897	883.8	2.06
r=0.9	166.95	113.67	5.60	0	280.62	45.85	6.0597	901.72	2.2
r=1	150.25	122.98	5.00	0	273.23	45.14	5.9814	892.97	2.56
TCM (20kHz-120kHz)	67.63	0	0	833	900.63	78.14	19.12	2709	0.69
CCM (20kHz)	699	0	0	649	1348	23.79	40.48	5000	0.62
CCM(97.6kHZ)	159.93	0	0	113.57	273.50	20.08	17.56	2089.00	0.3

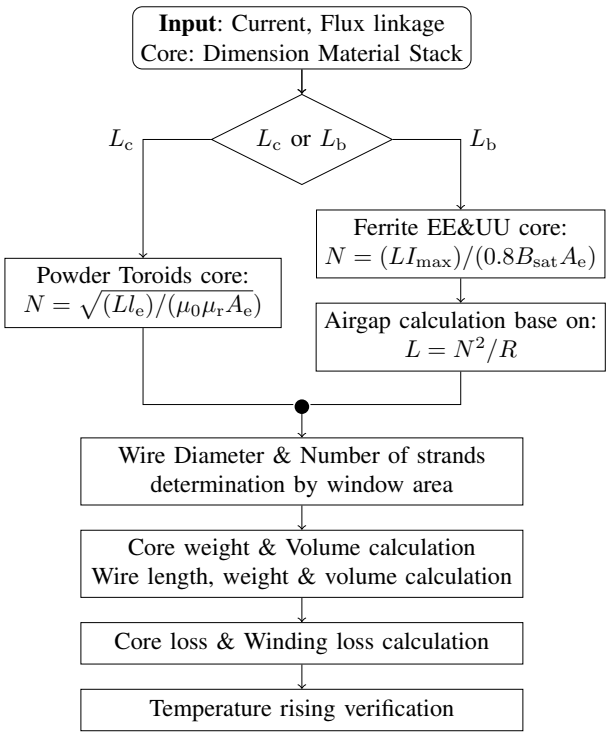


Fig. 3. Inductor design procedure of the three-phase iTCM PFC converter. The core material is chosen from Magnetics. Core dimension, material and number of stacks are swept to get an optimal result

dependent and can be derived from core datasheet [14]. However, the SE method is not accurate for non-sinusoidal flux waveform, and DC bias is not considered. Thus, the improved Generalized Steinmetz Equation (iGSE) is used to calculate any flux waveform, which is expressed as [15]:

$$P_v = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^\alpha (\Delta B)^{\beta-\alpha} dt \tag{12}$$

where

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^\alpha 2^{\beta-\alpha} d\theta} \tag{13}$$

and ΔB denotes the peak-to-peak amplitude flux density, k, α, β are the same parameters in the Steinmetz Equation. Note that ΔB will vary in time according to the evolution of the input voltage which will cause different current ripple values. Thus, the instant loss calculated in each switching period is summed up, and then averaged in a grid time period.

For the winding loss modeling, skin effect loss P_S and proximity effect loss P_P are taken into consideration. In iTCM, litz wire is used to reduce the winding loss. The skin effect loss can be calculated by:

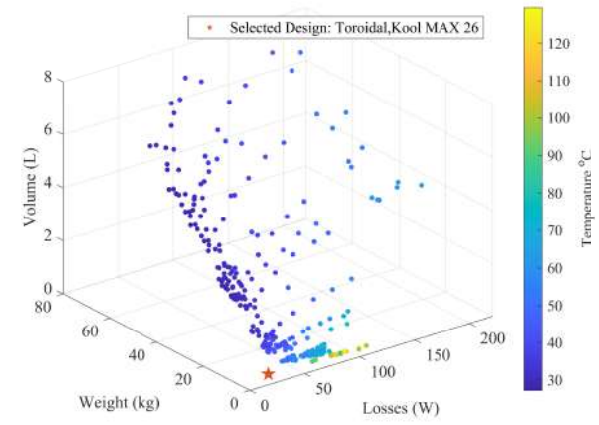
$$P_{S,Litz} = n\ F_{R/S}(f)\ R_{DC}\left(\frac{\hat{I}}{n}\right)^2 \tag{14}$$

where n is the number of strands, R_{DC} is the DC resistance per unit length per strand. Due to several strands in litz wire, the magnetic field consists of external part and internal part. The external magnetic field $\hat{H}_e$ is generated by other neighbouring conductors while the internal magnetic field $\hat{H}_i$ is generated by neighbouring strand within one conductor. The proximity effect loss calculation is adapted to:

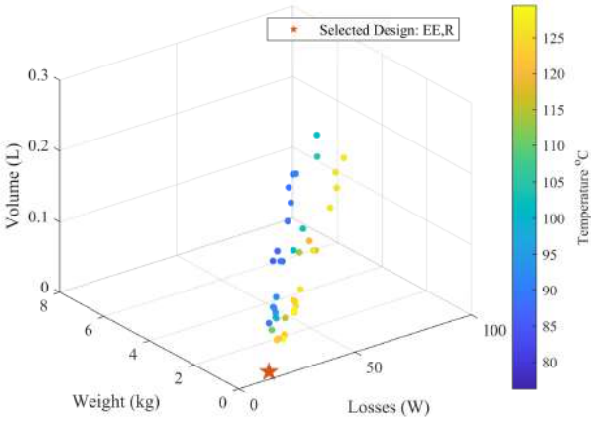
$$P_{P,Litz} = n\ G_{R/S}(f)\ R_{DC}\left(\hat{H}_e^2 + \hat{H}_i^2\right) \tag{15}$$

C. Inductor Design

To obtain a compact, lightweight and high-efficiency PFC converter design for OBCs, the inductor L_c and L_b should be optimally designed for the minimum inductor loss as well as volume and weight. Meanwhile, the maximum temperature



(a)



(b)

Fig. 4. 3D Pareto plots for the merits of volume, weight and loss for the inductor design of the studied three-phase recifier operating with iTCM (r=0.8, $f_{\min}$=20kHz). The magnetic core dimensions, material, stacks from Magnetics are swept to derive an optimal design which is shown as a star symbol. The temperature rising of each design is shown in the color bar. (a) Toroids powder core for the $L_{\rm c}$ design with 36 material, maximum 2 stacks swept; (b) EE&UU ferrite core for the $L_{\rm b}$ design with 3 material (P,R,F), maximum 2 stacks swept

should be limited to an acceptable value, e.g., 80..130 °C. As discussed before, $L_{\rm c}$ is designed with powder iron core, while $L_{\rm b}$ is designed by using ferrite core.

The inductor design procedure is shown in Fig. 3. Powder iron core has a relatively high saturation flux density ($B_{\rm sat}$) of up to 1.2 T so that ungapped Toroid powder core is used for the $L_{\rm c}$ design. The number of turns N is calculated by:

$$N = \sqrt{\frac{L l_{\rm e}}{\mu_0 \mu_{\rm r} A_{\rm e}}} \tag{16}$$

where L is the inductance value, $l_{\rm e}$, $A_{\rm e}$ are the flux path length and cross-sectional area of the core, μ_0 is the air permeability, $\mu_{\rm r}$ is the relative permeability.

TABLE V
OPTIMAL RESULTS FROM PARETO PLOT FOR $L_{\rm c}$ AND $L_{\rm b}$ DESIGNS

$f_{\min}$= 20 kHz, r = 80%	$\mathbf{L_c}$	$\mathbf{L_b}$
Core Material	Kool MAX 26	R
Core Code	'OD55778A2'	'0R44016EC'
Core Type	Toroid	EE
Number of Stacks	2	2
Number of Turns (N)	36	27
Airgap length(mm)	0	1.6
Number of strand (n)	2120	397
Core loss (W)	13.76	9.68
Winding loss (W)	14.58	7.72
Total loss (W)	28.34	17.4
Total weight (kg)	5.54	0.3497
Total volume (L)	0.824	0.0596

Ferrite core has lower saturation flux density ($B_{\rm sat}<$ 0.5 T), so the gapped core (EE&UU) is a necessity for the $L_{\rm b}$ design. The number of turns is determined by the maximum saturation flux density $B_{\rm sat}$ as:

$$N = \frac{L I_{\max}}{0.8 B_{\rm sat} A_{\rm e}} \tag{17}$$

where $I_{\max}$ is the maximum current flowing through L, and 0.8 is the safety coefficient to avoid saturation. For gapped cores the airgap length can be chosen based on the core dimension and number of turns. An accurate airgap calculation is proposed in [16], which is used in this modeling. Since the maximum switching frequency is up to 120 kHz, so litz wire AWG #40 is chosen to minimize the skin effect loss. The number of strands n is calculated based on the window area of the selected core, considering a filling factor of 0.8 for the litz wire bundle. To optimize the inductor design, core dimensions, material characteristics, number of stacks are scaled. The volume/loss and weight/loss optimization result are chosen from the Pareto plot results as summarized in Table IV.

The aforementioned parameter r is also scaled from 0-100% for the optimization. For $r > 100\%$, the total THD is not satisfying the IEEE519 standard anymore with the increase of grid-side current ripple. As shown in Table IV, the inductor loss is not affected too much when $0.2 \leq r \leq 0.8$. When r is small, the value of $L_{\rm c}$ is larger, but the current flowing through it is closer to sinusoidal. Finally, r is selected as 0.8 to obtain a lower weight and volume of the filter. The inductance of $L_{\rm c}$ and $L_{\rm b}$ are 187.82 μH and 105.68 μH respectively.

The Pareto plot for the design of $L_{\rm c}$ and $L_{\rm b}$ with $r = 0.8$ are shown in Fig. 4(a), 4(b) respectively. The optimal inductor core and wire selection is summarized in Table V.

IV. COMPARISON OF CCM TCM AND ITCM

To verify the advantage of the proposed three-phase iTCM control, the same models are also implemented to CCM at

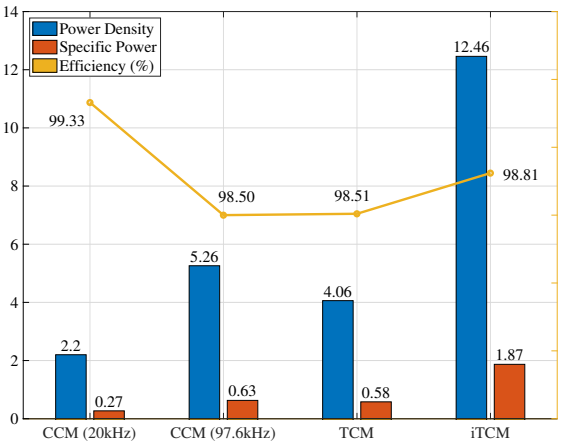


Fig. 5. Efficiency, power density and specific power comparison for the three-phase rectifier operating with CCM at 20kHz, CCM at 97.6kHz, TCM and iTCM with maximum frequency of 120kHz

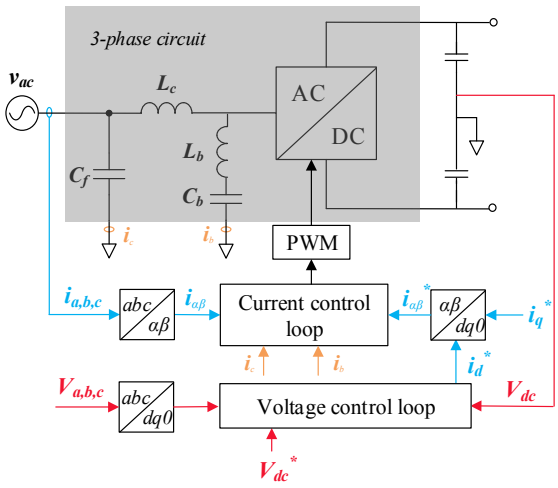


Fig. 6. Control diagram of the iTCM three-phase AC-DC PFC converter

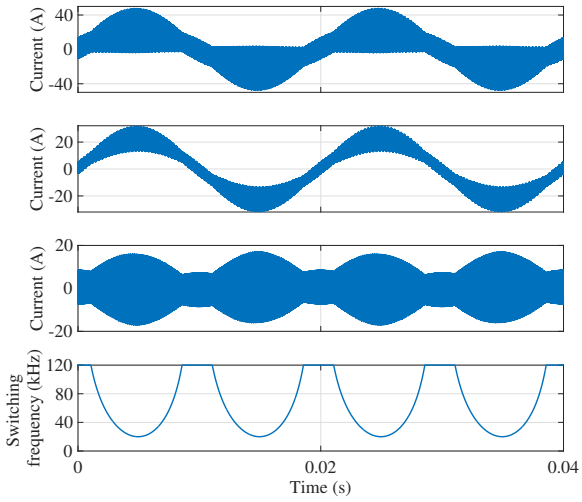


Fig. 7. Simulation results of the iTCM control by PLECS with r=0.8 and maximum frequency limitation of 120 kHz. The waveforms are semiconductor current i_{s}, grid-side current i_{c}, LC branch current i_{b} and f_{sw} from top to bottom, respectively.

20 kHz, CCM at 97.6 kHz and TCM, of which the results are summarized in Table III, IV. The grid-side inductor L_{g} is designed following the requirements from the IEEE519 standard, satisfying that the individual high order current harmonic amplitude is smaller than 0.3% of the maximum grid current [17], [18]. The inductor loss modeling and design uses the method discussed previously, and all the results are extracted from the derived Pareto plots. Fig. 5 shows the benchmark results considering the merits of efficiency, power density and specific power.

The efficiency of the rectifier operating with CCM at 20 kHz is the highest, while CCM at 97.6 kHz leads to the lowest efficiency of 98.5%. The power density and specific power are improved from 2.2 kW/L to 5.26 kW/L and 0.27 kW/kg to 0.63 kW/kg, respectively. It is proved that increasing the switching frequency to reduce the LCL input filter is limited and not practical, since it will lead to extremely high hard switching loss at higher switching frequency.

Surprisingly, the efficiency of TCM are not improved compared to CCM at 97.6 kHz. The main reason is that for the selected MOSFETs (C3M0120090J), the switching energy is already extremely low and the on-state resistance is quite large as shown in Table III. TCM or iTCM would eliminate turn-on loss, but the turn-off loss and conduction loss is increased [9]. Especially for the conduction loss, the RMS value is increased at least 33% by setting I_{zvs} to 0 in (10). Moreover, the large current ripple causes high inductor loss at the converter-side inductor. Thus, the increased loss part is larger than the eliminated turn-on loss. The power density and specific power of the TCM are also slightly reduced compared to the CCM at 97.6 kHz, which is because a larger core is needed for L_{c} due to the triangular current with large ripple.

The iTCM control extraordinarily improved the power density and specific power to 12.46 kW/L and 1.87 kW/kg, respectively. Compared to CCM at 20kHz, the efficiency is sacrificed only by 0.52%, but the power density and specific power improved 5.6 and 6.9 times, respectively. Due to the splitting of the high-frequency and low frequency current, the grid-side inductor L_{g} is not needed. Also, the inductor design minimized the loss, which improved the efficiency of 0.3%. Moreover, ferrite EE or UU core often has a lower volume and material density than powder Toroids core for the same inductor design.

TABLE VI
OPTIMAL RESULTS FROM PARETO PLOT FOR L_c AND L_b DESIGNS

f_{min}= 27 kHz	$\mathbf{L_c}$	$\mathbf{L_b}$
Inductance	945μH	196μH
Core Material	N87	N87
Core Code	'65/32/27'(1.5)	'55/28/21'(2)
Core Type	EE	EE
Number of Stacks	1	1
Number of Turns (N)	56	34
Airgap length(mm)	0.1	0.1
Number of strand (n)	600	600

V. CLOSE-LOOP CONTROL AND SIMULATION VERIFICATION

The close-loop control diagram of the iTCM operated three-phase AC-DC PFC is shown in Fig. 6. Dual-loop control is implemented with an outer voltage loop and an inner current loop. The voltage control loop is used to control the output DC link voltage V_{dc} in dq frame by a PI controller. The grid-side current is controlled in $\alpha\beta$ frame by a PR controller.

Due to the additional LC branch and the large variation of switching frequency, the close-loop control of iTCM becomes more complicated. The resonance of the input LC filter and LC branch could cause control instability. Passive damping is the simplest method but would cause extra loss. Several active damping methods exist to stabilize the system without adding extra components [8].

The capacitor-current-feedback control is one of the active damping methods used for damping the input filter. The capacitor current is fed back to the current loop by a proportional gain, which can be considered as a virtual resistor parallel to the capacitor due to a time delay [8]. Moreover, the current i_b should be fed back to the main loop damping the LC branch resonance as shown in Fig. 6.

The simulation is conducted to verify the idea of iTCM and close-loop control via PLECS. The parameter used for the simulation is the same as the system specification in Table I. The simulation results are shown in Fig. 7. ZVS turn-on is achieved at full period since the current is reversed to 2.5A at each switching period as the current waveform of i_s shows. The low-frequency and high-frequency current are split, while the low-frequency current satisfies the input power and the high-frequency current flows through the LC branch and stay within the circuit by the midpoint.

VI. EXPERIMENT VALIDATION

To validate the feasibility of the proposed three-phase iTCM control, experiment based on the digital signal processor (DSP)-TMS320F28379D has been conducted, as shown in Fig. 8. The prototype that used in the experiment is a three-phase two-level full-bridge AC-DC converter, and the semiconductor device is SiC MOSFET (C3M0120090J, four paralleled as one switch), which is the same as in the analytical modeling.

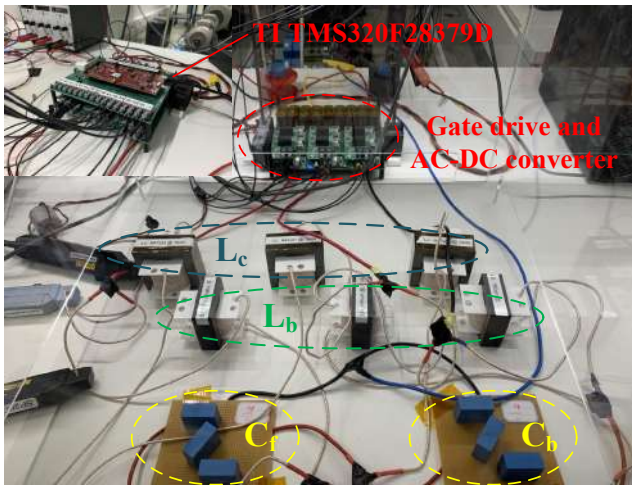


Fig. 8. Experimental setup.

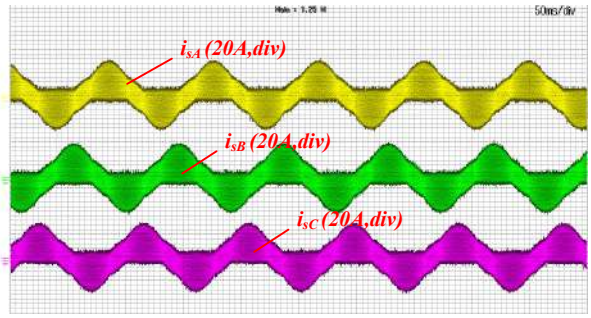
Fig.9 shows the experimental results under the power rating of 3 kW. The AC voltage v_{ac}, the DC-link voltage V_{dc} and the AC frequency f_0 are shown in Table I. The inductor L_c and L_b are designed by the inductor design procedure shown in Fig. 3. Due to the lower power rating, both L_c and L_b use ferrite core and litz wire to optimize the efficiency. The chosen optimal results for L_c and L_b design in this experiment are shown in Table VI. The reversal current I_{zvs} at 3 kW is chosen as 1.5 A based on (3).

Fig. 9(a), 9(c) and 9(d) show the waveform of the semiconductor current i_s, the L_c current i_c and the LC branch current i_b, respectively. It can be seen that L_c and L_b are well-designed so that the current flows to the AC side only has a small ripple while the high-frequency current flows to the LC branch.

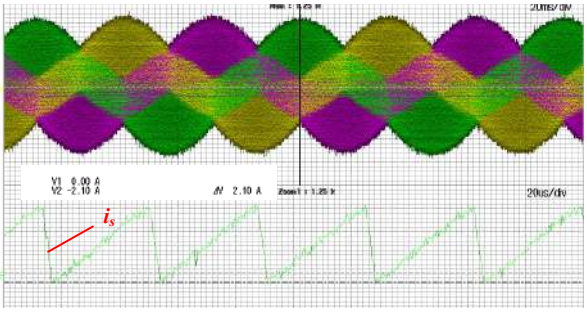
Fig. 9(b) shows the zoomed waveform of the semiconductor current i_s. In each switching cycle, the current reaches around -2 A, which means fully ZVS is achieved in this experiment.

VII. CONCLUSION

The iTCM control method applied to a three-phase AC-DC PFC converter has been proposed in this paper. ZVS operation in the iTCM strategy eliminates the turn-on switching loss but slight increases the turn-off switching and conduction losses. The inductor loss in iTCM is minimized due to the added LC branch, while the grid-side current ripple is highly reduced compared to the conventional TCM. By analytical modeling and simulation, iTCM is proved to be more efficient, highly compact and lightweight than TCM and CCM at the high switching frequency. Compared with CCM at low frequency, the power density and specific power improved around 6 times but sacrificed efficiency by 0.5%, which is acceptable. Dual-loop control with LCL capacitor and LC branch current feedback is proposed and implemented in PLECS to control the PFC converter in iTCM. The feasibility of the three-phase iTCM control is verified by experimental results. In the



(a)



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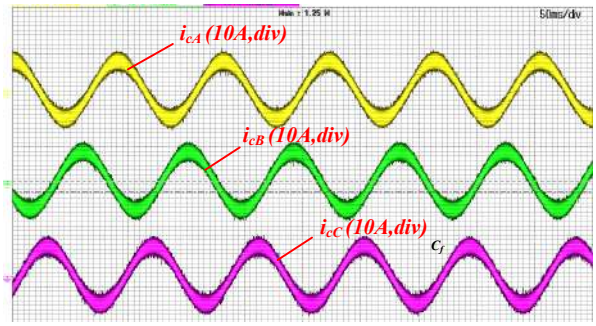
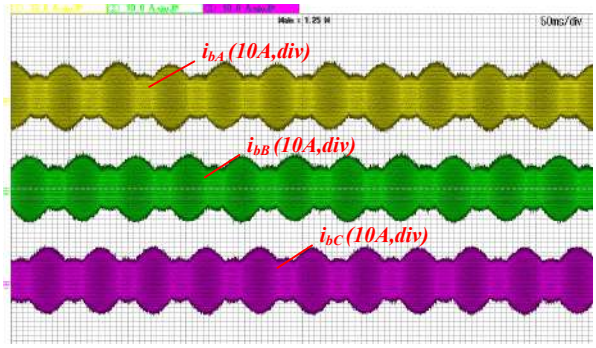


(c)



(d)

Fig. 9. Experimental results of the proposed three-phase iTCM control. (a) The semiconductor current i_s; (b) The zoomed waveform of semiconductor current i_s in several switching cycles;(c) The L_c current i_c; (d) The LC branch current i_b.

future, the complete comparison of iTCM, TCM and CCM will be practically verified, and the iTCM method operating at different load situations will be analyzed and optimized.

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