Wideband Hybrid pipeline ADC

by

Wouter Kragt

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Student number: 4459091
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Thesis committee:

Dr. ir. M. Bolatkale,	TU Delft, NXP Semiconductors, supervisor
Prof. Dr. ir. K. Makinwa,	TU Delft
Prof. Dr. ir. W. Serdijn	TU Delft

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TU Delft

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Abstract

To be able to cope with the demands of next generation radar applications, a bandwidth of 400MHz is required. The SAR assisted CT $\Delta\Sigma$ ADC provides an energy efficient ADC, but needs improvements to cope with the bandwidth enlargement. This thesis examines the front end components and thus initially focuses on resolving the issues in the front end.

Although bandwidth enlargement is possible, the APF limits the performance resulting in an inefficient two-stage architecture. For optimal system efficiency, the APF requirements must be relaxed, which is achieved by decreasing the amount of resolved bits in the coarse ADC. Due to this reduction in bits, more stages must be incorporated into the architecture. To facilitate this, power and error budgets are devised to visualize the effects of adding stages. Hereafter, the 2 bit coarse ADC is compared to a 3 bit coarse ADC. This results in a trade-off between the applicable gain (APF complexity) and the noise requirements of the front end. The five-stage (2-2-2-2-6 bit) architecture proves to be the most promising design to achieve the desired FoM$_s$ of 172dB.

Finally, in an attempt to optimize power efficiency, the APF and LPF filter are revised. The open loop filter implementation is compared to a closed loop filter implementation. It shows that the open loop implementation exhibits very good power efficiency, but lacks in its linearity. The closed loop implementation achieves the requirements, but consumes a lot of power. To optimize power consumption, the first and second stage must be implemented with the closed loop filters, but the third and fourth stage must be implemented with the open loop filters.

Contents

Nomenclature

Abbreviations

Abbreviation	Definition
AAF	Anti-aliasing filter
ADC	Analog-to-digital converter
APF	All-pass filter
BW	Bandwidth
Comp	Comparator
CMRR	Common-Mode Rejection Ratio
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-analog converter
DC	Direct Current
DR	Dynamic range
FoM	Figure of Merit
GBW	Gain-bandwidth product
HD_3	3^{rd} order harmonic distortion
HPF	High-pass filter
LPF	Low-pass filter
LSB	Least significant bit
NMOS	Negative-Channel Metal Oxide Semiconductor
OPAMP	Operational amplifier
OSR	Oversampling ratio
OTA	Operational transconductance amplifier
PLL	Phase-locked loop
PMOS	Positive-Channel Metal Oxide Semiconductor
PPF	Polyphase filter
PSRR	Power Supply Rejection Ratio
RMS	Root-mean-square
SAR	Successive-approximation
SNR	Signal-to-noise ratio
SFDR	Spurious-free dynamic range
SQNR	Signal-to-quantisation noise ratio
SJNR	Signal-to-jitter noise ratio
THD	Total harmonic distortion
UGBW	Unity-gain-bandwidth
ZOH	Zero-order hold

Symbols

C	Capacitance	[F]
C_{ox}	Gate-oxide capacitance per unit area	[F/m^2]
g_m, G_m	Transonductance	[S]
I	Current	[A]
f	Frequency	[Hz]
G	Gain	[V/V]
μ	Mobility of electrons	[m^2/(V·s)]
P	Power	[W]
P_n	Integrated noise power	[V^2]
ω	Radians	[rad/s]
R	Resistance	[Ω]
S	Siemens	[Ω^{-1}]
t	Time	[s]
T	Temperature	[K]
V	Voltage	[V]
W	Transistor width	[m]
Z	Impedance	[Ω]

Constants

Symbol	Definition	Unit
k	Boltzmann $\approx 1.38 \times 10^{-23}$	[J/K]
c	Speed of light	[m/s]

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1 Introduction

1.1. Motivation

The SAR assisted CT $\Delta\Sigma$ ADC provides an energy efficient ADC with a bandwidth of 40MHz [1]. It incorporates inherent anti-aliasing and achieves a large SNDR (77.5dB). Furthermore, it has relaxes driving requirements of CT $\Delta\Sigma$ ADC. However, to be able to cope with the demands of next generation radar applications, the bandwidth needs to be enlarged, up to 400MHz. To achieve this bandwidth adjustments in the architecture have to be made, such as the latency compensation of the APF, SAR ADC and R-DAC. Furthermore, the anti-aliasing and the low-pass filtering of the residue signal are taken into account. In other words, this thesis initially focuses on resolving the issues in the front end. More specifically, it focusses on the problems related with the bandwidth enlargement to 400MHz.

The SAR assisted CT $\Delta\Sigma$ ADC [1] has proven to be power efficient, hence it is taken as the starting point of the analysis. However, it does not mean that this architecture is the best solution for the 400MHz bandwidth. Therefore, it is examined more thoroughly and a power and error budget is made to visualize the effects of different amount of stages on the performance of the architecture. In an attempt at the most power efficient system, the APF and LPF filter are revised. Here, an open loop low-pass filter configuration is compared to a closed loop filter configuration. Subsequently, a conclusion is drawn on the best implementation.

1.2. System requirements

The ADC is meant for automotive radar applications, which brings certain constraints with it. These constraints are listed in 1.1.

System requirements	Unit	Budget
Technology	nm	28
Supply voltage	V	0.9
HDx	dBc	70
DR	dB	70
SNDR	dB	67
SFDR	dBc	104
Power (analog)	mW	12.7

Table 1.1: System specifications

1.3. Constraints

To limit the scope of the thesis, some additional constraints and assumptions are made prematurely to the thesis. On the whole, as much as possible components from The SAR assisted CT $\Delta\Sigma$ ADC [1] are reused. These components consist of the inverter based amplifier, the (coarse) SAR ADC and the resistive DAC (R-DAC).

Furthermore, the following assumptions are made. The coarse ADC is dithered in a later phase of the design. The amplifier is chopped to reduce the flicker noise and the passive components are digitally calibrated to achieve the wanted accuracy. The system blocks are assumed to have an ideal operation, without offset, gain errors etc, unless it is mentioned otherwise.

1.4. Structure

First, a literature study is performed on the SAR assisted CT $\Delta\Sigma$ ADC [1]. To revise whether the architecture is promising for the enlarged bandwidth, other solutions for the wanted bandwidth are examined. Before diving into a thorough analysis of the architecture, Chapter 3 provides a simple explanation of all the blocks in the ADC. Here, the main operation of the ADC and the role of the system blocks become clear. Hereafter, Chapter 4 provides a thorough analysis on the APF and the front end ADC. In Chapter 5 a system study is performed, where the original two-stage architecture of is reviewed [1]. Furthermore, the coarse ADC is examined and its impact on a system level is given. The results are used to conclude on the most promising architecture. In an attempt to increase the power efficiency of the system, Chapter 6 compares the open loop APF and LPF implementation to the closed loop APF and LPF implementation. At last, a conclusion and the recommended future work are presented.

2

Literature study

The SAR-assisted CT $\Delta\Sigma$ ADC [1] is given as a starting point for the system. However, this architecture is not necessarily the best option for the bandwidth. To have an overview of other architecture solutions for the bandwidth, a literature study is done. Here, the trends of other architectures are reviewed and the capability of the SAR-assisted CT $\Delta\Sigma$ ADC for the bandwidth enlargement is examined.

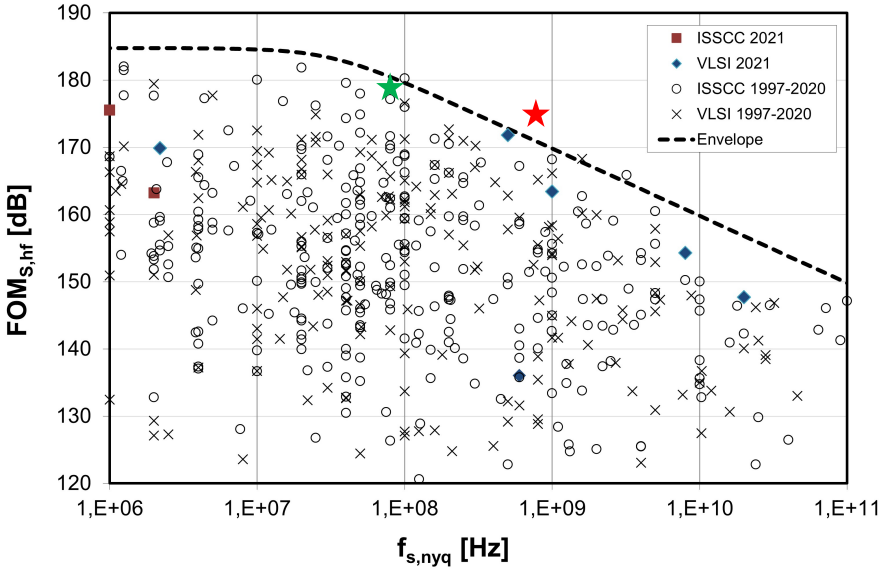

Figure 2.1: Murmann graph, goal of the architecture: ★
the SAR assisted CT $\Delta\Sigma$ ADC [1]: ★

Figure 2.1, shows the Murmann graph, where the green star is the SAR assisted CT $\Delta\Sigma$ ADC [1]. This verifies that the SAR-assisted CT $\Delta\Sigma$ ADC provides an energy efficient ADC with a bandwidth of 40MHz [1]. However, the targeted bandwidth is ten times as large, 400MHz (see red star in Figure 2.1). It is known that SAR ADCs are very power efficient, but they lack in terms of speed [2]. Therefore, it is not straightforward to use a SAR ADC for large bandwidths. In the literature study, the choice of reusing the SAR ADC is validated by examining the most recent research-outcomes and by reviewing their architectures and the trends that are seen. The architectures that are used to obtain a good Schreier Figure of Merit (FoM) for a SNDR > 55dB are given by Figure 2.2.

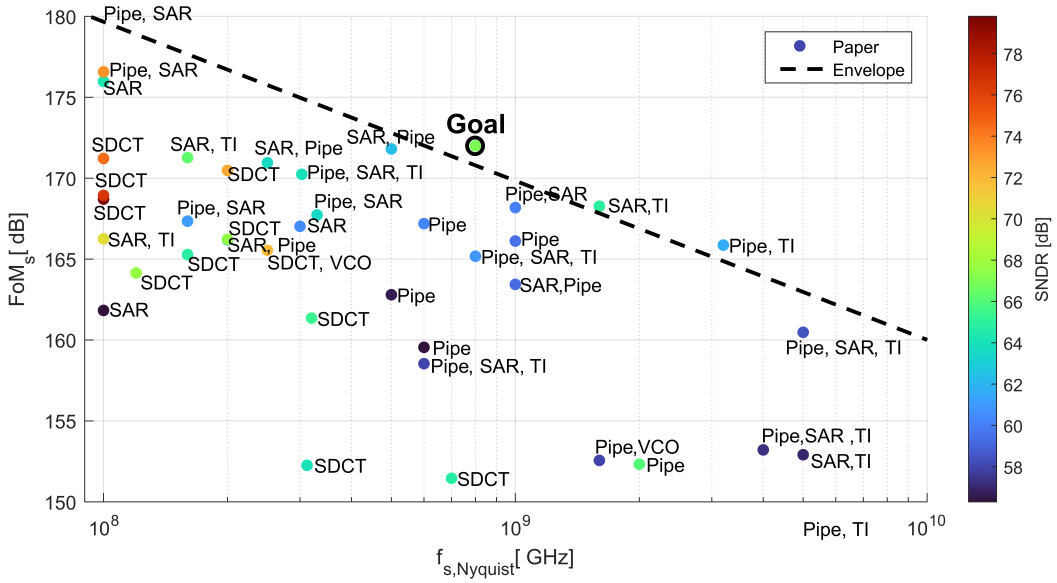

Figure 2.2: Papers from Murmann graph, with trends in the architectures, filtered for SNDR > 55dB

Figure 2.2 shows that for smaller Nyquist bandwidths (200$\leq$MHz) with a large SNDR ($\geq$ 65dB), the continuous time $\Delta\Sigma$ ADC proves to be an efficient architecture. The pipelined SAR and time interleaved (TI) are not so popular for the large SNDR. Nevertheless, they do prove to be power efficient, since the highest FoMs are achieved with the pipelined SAR ADCs. For larger bandwidths, Figure 2.2, shows that pipelined ADCs, TI ADCs and TI pipelined ADCs are the most preferred architecture. More specifically, for the targeted bandwidth, Figure 2.2, shows the preferred architectures are pipelined ADCs [3], [4], [5], [6]. To achieve higher FoMs architectures lead to trends towards the TI SAR ADCs [7], [8], [9] or a combination of TI and pipelined SAR ADCs [10], [11], [12]. The previously mentioned papers, incorporate a (novel) sort of digital calibration. The calibration is to optimize the offsets [8], [9], [11], [12], the timing skews [7], [12], the capacitor mismatches [5], [10], the linearity [4], [6], [10], or gain [4], [6], [8], [9], [10], [12] of the amplifier etc. In the end, all the calibration methods are used to enhance the performance of the system, enabling higher SNDRs (up to an ENOB of 12 bits).

SAR ADCs, (pipelined or not) are limited by their kT/C noise, which can be mitigated by enlargement of the capacitors. However, the capacitor bank of the first stage must settle with sufficient accuracy to reach the wanted SNDR. In order to obtain a faster settling behavior, the capacitors must be made very small. Consequently, there is a trade-off in the capacitor size. A solution is, implementing a buffer before the first stage [13]. Nevertheless, the buffer decreases the FoM with its power consumption because it must comply with all the system requirement as it is at the input of the system. TI techniques can be used to increase the bandwidth of SAR ADCs. However, other TI problems arise. Moreover, this does not completely solve the previous problem, as the input capacitance remains present. The architecture of [1] is not constrained by the input capacitance trade-off, because the kT/C of the coarse SAR ADC is cancelled. A more detailed explanation of this phenomenon is discussed later in this thesis. As a result of the noise cancellation, the input capacitance can be made as small as possible. This enables fast and accurate sampling of the input signal. The used SAR ADC is given by [14]. The SAR ADC of [14] can operate up to 2.4GHz to resolve 5 bits. For the targeted bandwidth, this gives an OSR of 3, which is assumed to be enough. Next to this, the

SAR ADC only dissipates 2.12mW. This is made possible, due to the relieved constraint of the capacitor. Therefore, this coarse ADC is the starting point of the analysis.

The papers in Figure 2.2 that are in the vicinity of the goal, are pipelined architectures. All these architectures use of SAR ADCs for their coarse conversions (ADCs) [15] [16], [17]. However, they reach at most a SNDR of 62.3dB. Moreover, Figure 2.2 shows that for the larger bandwidths the SAR ADCs have a limited SNDR. At these bandwidths the continuous time $\Delta\Sigma$ ADCs achieve a higher SNDR, but their FoMs are between 152 and 162dB. Therefore, it is interesting to investigate the continuous time $\Delta\Sigma$ ADCs. Their power consumption is mainly due to the amplifiers and the quantizers [18], [19], [20]. Nevertheless, the continuous time $\Delta\Sigma$ ADCs benefit from their inherent anti-aliasing.

The SAR assisted CT $\Delta\Sigma$ ADC [1] achieves the needed SNDR and proves to be power efficient. The same architecture composition is used in [21]. However, in [21] more stages are used and all the ADCs are Flash ADCs. This paper reaches a FoM of 152.3dB, for a Nyquist bandwidth of 2GHz with an SNDR of 66dB. The SNDR is high for the bandwidth, but the FoM is relatively low due to the large power consumption. The large power consumption is large due to the Flash ADCs and the clock, which dissipate 34.7% and 33.3% of the total power. Next to this, the power of the amplifiers is 25.7%, which is relatively small. The power of consumption of the coarse ADC in [1] is reduced, because the SAR ADC of [14] is used.

From the previous analysis, it is clear that (TI) SAR ADCs are power efficient ADCs, but with a limited SNDR [7], [8], [9]. The nature of the limited SNDR is due to the dependence on passive components, the capacitors. Nevertheless, this limitation is suppressed by adding a front end stage, which can contribute to the SNDR, such that the requirements on the SAR ADC are relaxed. The wanted SNDR can be obtained in two stages, with 5 bits in the front end and 7 bits in the back end as in [1] and [22]. Although, in [22] the back end resolution is obtained by a VCO. Another option is to divide the SNDR into multiple stages, as in [23] and [21]. In [23], a Nyquist bandwidth of 200MHz is targeted for a SNDR of 70dB. To achieve this, four stages are used as the number of bits resolved per stage is 3-3-3-7 bit, consequently there are 4 bits redundant. [21] has an even larger Nyquist bandwidth of 2GHz; here seven stages are used, in each stage 4 bit are resolved, thus in total 28 bits. However, it only achieves an SNDR of 66dB. The large deviation between the effective number of bits and the resolved number of bits becomes clear in Section 3.2. To achieve the SNDR, there are multiple options, which can be summarized in two main directions. First in a two-stage design, where the front end resolves up to 5 bits and the rest of the bits are resolved in the back end. The second option is to spread the resolved bits into more stages in such a way that the back end resolved a smaller amount of bits. In addition, it seems that the larger bandwidths prefer this configuration.

At last, the (pipelined or TI) SAR ADCs sample at Nyquist rate, which makes them prone to aliasing. The architectures [1], [19], [21], [23] oversample the input signal, which relaxes the anti-aliasing requirements. Furthermore, the inherent anti-aliasing property of the continuous time $\Delta\Sigma$ ADCs is also integrated in the architecture, because the aliases created in the coarse ADC are cancelled. This is done in the same fashion as the quantization error of the coarse ADC. As a result, only the back end ADC causes the aliases of the signal. In addition, the aliases created by the back end ADC are filtered by the digital reconstruction filter (the digital back end) [24]. This digital back end must replicate the continuous time path, thus the LPF and DAC sinc response attenuate the out-of-band-blockers (OOBs). As a result, the architecture exhibits a good anti-aliasing performance. A further analysis on the AAF, is given in Section

4.1.

All in all, it can be concluded that [1] will most likely be able to cope with the bandwidth enlargement, as the architecture, [1] is relieved from the capacitor size trade-off. However, probably more stages must be added to cope with the bandwidth and the SNDR, as in [21], [23]. In addition, the power efficiency increases, because the power consumption of the architectures [21], [23] can be reduced by replacing the Flash ADCs with SAR ADCs from [1], [14] as is seen in the pipelined SAR ADCs [15] [16], [17].

3

Architecture overview

From the literature study, the preferred architecture is given in Figure 3.1, which includes all the sub-blocks. Each sub-block has its own functionality, which are explained in more detail in the next chapter. This chapter will introduce all the sub-blocks, whereafter the main considerations for the dynamic range of the architecture are briefly given. Subsequently, the analyses of the architecture is given, based on the SAR assisted CT $\Delta\Sigma$ ADC [1].

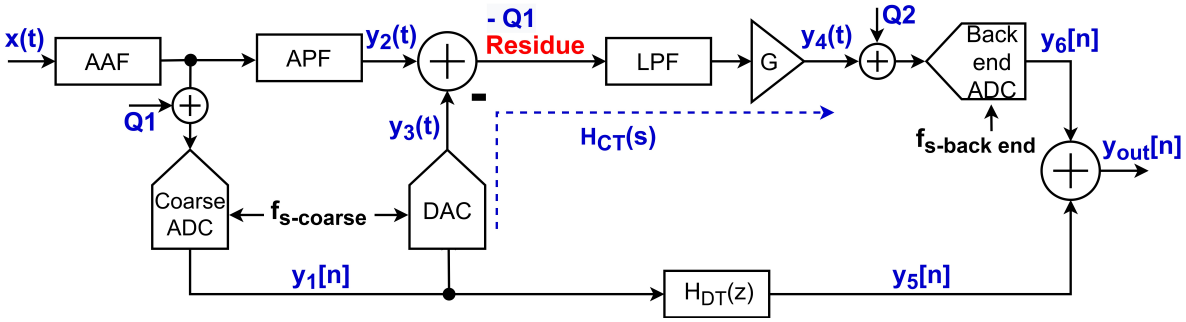

Figure 3.1: Block diagram of the two-stage system architecture

Before explaining the sub-blocks, an overview of the operation of the system is given. This explanation is based on Figure 3.1. The system consists of three parts, the front end stage also known as the coarse stage, the back end stage (or the fine stage) and the digital back end (or the digital reconstruction filter). The front end stage consists of the AAF, APF, coarse ADC, DAC, LPF and G (inter-stage Gain). The back end stage consists of the back end ADC. The digital back end is the noise cancellation filter $H_{DT}(z)$.

The input signal $x(t)$ passes through the AAF, which is used to filter out-of-band signals. Hereafter, the coarse ADC quantizes the signal and introduces a quantization error (Q1), $y_2[n]$ and the DAC converts the digital signal back into an analog signal, $y_3(t)$. Those two conversions cause a latency, which is matched by the APF, $y_2(t)$. The summation node subtracts $y_3(t)$ from $y_2(t)$ and creates the residue signal. Ideally, this residue consists of only the quantization error Q1. The residue signal is low-pass filtered to make sure the amplifier will not saturate, $y_4(t)$. Hereafter $y_4(t)$ is digitized by the back end ADC, which introduces the second quantization error Q2, $y_6[n]$. Furthermore, the digital back end $H_{DT}(z)$ must match the analog

path $H_{CT}(s)$, such that in the output $y_{out}[n]$ the quantization error (Q1) of the coarse ADC is cancelled. This can be expressed as:

$$y_{out}[n] = y_5[n] + y_6[n] \rightarrow y_{out}[n] = H_{DT}(z)(x(t) + Q1) + (-Q1H_{CT}(s) + Q2) \tag{3.1}$$

$$y_{out}[n] = x(t)H_{DT}(z) + Q1(H_{DT}(z) - H_{CT}(s)) + Q2 \tag{3.2}$$

In Equation 3.2 it can be seen that, if the transfer function of the digital back end $H_{DT}(z)$ exactly matches the transfer function of the analog path $H_{CT}(s)$, the quantization error of the coarse ADC is cancelled out. Furthermore, since $H_{DT}(z)$ must match the analog path, the same inter-stage gain of block G must be in the transfer function of $H_{DT}(z)$. Therefore, the output signal $y_{out}[n]$ can be rewritten as:

$$y_{out}[n] = Gx(t) + Q2 \tag{3.3}$$

Note that from Equation 3.3 the SQNR equation can be derived. This is done in Section 3.2.

3.1. The sub-blocks

3.1.1. Anti-aliasing filter

The anti-aliasing filter (AAF) must not attenuate signals that are in the signal-band. However, the AAF must attenuate out-of-band blockers (OOB) that potentially alias back in the signal-band. These aliased signals can degrade the dynamic range of the system. Furthermore, the inter-stage gain (G, see Figure 3.1) that can be applied to the residue signal must be applicable over the frequency span from 0 to f_s Hz. If not, an OOB can saturate an internal node in the system, which will cause degradation in the SNR. Or worse, the system could even malfunction. In other words, this must be taken into account. For an in depth analysis, see Chapter 4.1.

3.1.2. Coarse ADC

The coarse ADC, is a SAR ADC, which is used in [1]. It performs the coarse conversion of the first 5 bits. It generates the first quantization error that is processed by the back end of the system. Furthermore, the coarse ADC determines the sampling rate of the coarse ADC, which sets the latency. For an in depth analysis, see Chapter 4.5.

3.1.3. DAC

The output of the coarse ADC is in the digital domain. However, it is fed back to the input signal at the summation node, see Figure 3.1. Therefore, a DAC is needed to convert the quantized signal back to the analog domain and make the subtraction possible.

3.1.4. All pass filter

The all pass filter (APF) compensates for the latency of the coarse ADC and DAC. The effect of a phase mismatch in the summation node can be seen in Figure 3.2. For a perfect latency compensation, the residue signal has the smallest magnitude. Therefore, the APF must be designed for an as accurate as possible latency compensation.

3.1.5. Low pass filter and gain

The main reason for the implementation of the LPF, is to ensure that a certain amount of gain can be applied to the residue signal. This can easily be shown by the residue signal for non-ideal latency compensations in Figure 3.2. As the phase mismatch is larger, high frequency tones arise. These tones can deteriorate the residue signal or even saturate the node. To circumvent this, the LPF is implemented. Further, the gain is applied to the residue in such a way that the SQNR increases, see the Section 3.2.

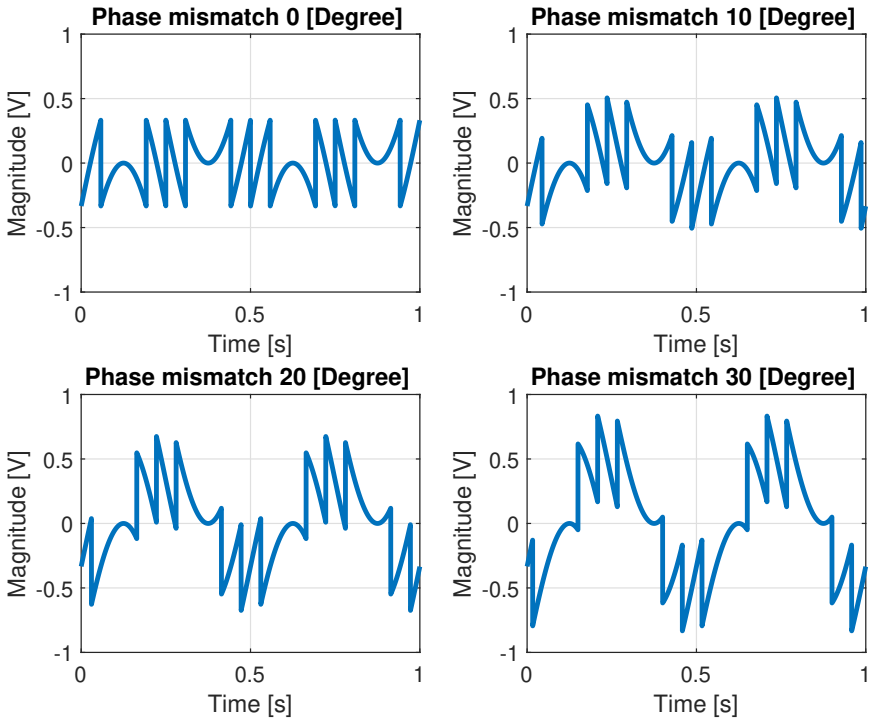

Figure 3.2: Residue output due to phase mismatch

3.1.6. Back end (SAR) ADC

In this architecture, the composition of the dynamic range can be divided into two parts. First, the quantization noise of the front end, which is cancelled and suppressed by the gain. Second, the amount of bits resolved by the back end (SAR) ADC.

3.1.7. Digital back end

The output signal $y_{out}[n]$ is a summation of the quantized residue signal ($y_6[n]$) and the digital back end path ($y_5[n]$). The digital back end is the block $H_{DT}(z)$ in Figure 3.1. It must mimic the transfer function of the continuous time path (see arrow in Figure 3.1). If not, the quantization noise of the coarse ADC will leak and the SNR will drop. Therefore, the matching of the digital back end is an important block for the performance of the ADC. Note that the cancellation of other noise sources, that originate in the same location, are also cancelled at the output.

3.2. The dynamic range

For the design of the system, a dynamic range specification is given. The main concerns of the dynamic range are reviewed in this section. The dynamic range can be broken down into multiple components, the noise sources, where the main concerns are the jitter, digital

matching, thermal noise and the quantization noise. The jitter is a concern because of the large bandwidth. Nevertheless, the jitter is set by the technology and the PLL used by the system. Furthermore, the exact digital matching is unknown and stays out of the scope of the thesis. The thermal noise can be designed for and will be a trade-off between thermal noise and power and area. Hence, the main noise source to design for is the quantization noise.

If all the blocks are assumed to be ideal (in 3.1), Equation 3.3 holds. Moreover, the quantization noise to noise (SQNR) can be determined. The total quantization noise power in the bandwidth of $f_s/2$ can be described by :

$$P_n = \frac{\Delta^2}{12} \tag{3.4}$$

where Δ is the least-significant-bit size (V_{lsb}), which can be expressed as:

$$\Delta = \frac{2V_{ref}}{2^B - 1} \tag{3.5}$$

where B is the amount of converted bits, V_{ref} is the reference voltage. However, if there is an oversampling ratio, a part of the quantization noise falls out of the signal bandwidth (BW). The coarse ADC is dithered in a later phase of the design. Therefore, the assumption can be made that the quantization noise has a white spectrum. Equation 3.4 must be extended to:

$$P_{n-in-band} = \frac{\Delta^2}{12}\frac{2BW}{f_s} \tag{3.6}$$

The signal power is known, thus the SQNR can be expressed by:

$$SQNR = \frac{P_{signal}}{\frac{\Delta^2}{12}\frac{2BW}{f_s}} \tag{3.7}$$

The signal power can also be expressed as [2]:

$$P_{signal} = \frac{2^{2B}\Delta^2}{8} \tag{3.8}$$

Substituting 3.8 in 3.7, results in:

$$SQNR = \frac{3}{2}2^{2B}\frac{2BW}{f_s} \tag{3.9}$$

In a logarithm this becomes:

$$SQNR_{dB} = 6.02B + 1.76 + 10log_{10}(\frac{f_s}{2BW}) \tag{3.10}$$

From Equation 3.3 it can be seen that the quantization error Q2 is from the back end ADC, hence the sampling rate must be taken of the back end ADC. Furthermore, it shows that the input signal is magnified by the gain, G. Hence, Equation 3.3 can be expressed as:

$$SQNR_{dB} = 6.02B + 1.76 + 10log_{10}(\frac{f_{s,BE}}{2BW_{sig}}) + G_{inter-stage} \tag{3.11}$$

From Equation 3.11 it can be seen that in order to increase the SQNR either the back end ADC must resolve more bits or the inter-stage gain must be increased. The inter-stage gain is defined by the amount of gain that can be applied after low-pass filtering the residue signal,

see G in Figure 3.1. There is one more factor to increase the SQNR, namely, the oversampling ratio of the back end ADC. This is the $f_{s,BE}$ in Equation 3.11. However, due to the large bandwidth of the system, an increase of the OSR leads to a large increase of the sampling rate of the back end. As a result, the back end can either convert a smaller amount of bits or it must increase its power consumption.

If the back end ADC is not considered, the SQNR can only be increased by applying a larger inter-stage gain. This can be achieved by optimizing the magnitude of the residue signal. Therefore, the residue signal is examined more thoroughly.

The ideal residue signal, without low-pass filtering, is solely the quantization error as Equations 3.12 and 3.13 describe:

$$V_{residue} = V_{in} - (V_{in} \pm \frac{V_{ref}}{2^B - 1}) \tag{3.12}$$

$$V_{residue} = \pm \frac{V_{ref}}{2^B - 1} \tag{3.13}$$

Ideally, the maximal gain that can be applied to the residue signal is defined by the reference voltage divided by the magnitude of the residue signal, which can be expressed as:

$$\begin{aligned} Gain &= \frac{V_{ref}}{|V_{residue}|} \\ Gain &= 2^B - 1 \end{aligned} \tag{3.14}$$

Amount of bits	Gain [dB]
2	9.5
3	16.9
4	23.5
5	29.8

Table 3.1: The maximum gain applied to the residue signal, without latency mismatch

The amount of gain that can be applied in to the residue signal is given in Table 3.1. Note this is the maximal gain without low-pass filtering, thus it only holds for very low in-band frequencies ($\approx f_{in} < 2MHz$). The AAF and LPF do not affect very low frequencies. Hence, Table 3.1 defines the maximally applicable in-band gain of a stage.

The cancellation of the input signal is not ideal. A more insightful examination of the residue signal, is to consider the residue signal as a signal consisting out of two components; The first component is the quantization error and the second component is the leaked input signal. In order to reduce the magnitude of the residue signal, both components must be minimized. The quantization error consists of harmonics (3^{rd}, 5^{th}, 7^{th} etc) of the input signal [2]. The high frequency components of the quantization error are reduced by low-pass filtering them. However, this only holds for input frequencies where the majority of the quantization error is near or higher than the band-edge. Very low input frequencies are not affected by it. The LPF has a larger impact on the low frequencies if the quantizer is dithered, because the quantization noise power is evenly spread up to $f_{s-coarse}/2$

The leakage of the input signal is suppressed by the implementation of the APF. The APF must compensate for the latency of the coarse ADC and DAC. The leaked input signal is the smallest for the most accurate latency compensation. In other words, both components must be optimized to obtain an as small as possible residue signal, which is needed to implement an as high as possible gain to obtain, in the end, the largest SQNR.

3.3. Summary

In summary, the system behavior can be described as follows; The coarse ADC determines the sampling rate and thereby sets the amount of latency compensation needed by the APF. The DAC makes the subtraction possible such that the residue signal can be generated. The LPF, ensures a certain amount of gain that can be applied to the residue signal. Moreover, the LPF together with the AAF ensure that OOBs do not degrade the performance of the system. To cancel the quantization noise and other noises that originate at the coarse ADC, the digital back end $H_{DT}(z)$ must mimic the continuous time path. The achievable SQNR is set by the inter-stage gain, the OSR and the amount of bits it resolved of the back end ADC (Equation 3.11). The inter-stage gain is a dominant factor in the achievable SQNR, which depends on the latency compensation, the low-pass filtering, the coarse ADC/DAC and on the AAF. The accuracy of the latency compensation of the APF impacts the amount of gain that can be applied to the residue signal. At last, for the low frequencies, the amount of bits resolved in the coarse ADC defines the maximal gain that can be applied to the residue signal.

4

The front end

The front end of the ADC must be redesigned to meet the bandwidth requirement of 400MHz. In order to meet these requirements, the AAF, APF, LPF, DAC and the coarse ADC must be redesigned. The starting point is the SAR assisted CT $\Delta\Sigma$ ADC [1], where a sampling rate of 2.4GHz is used. Hence, this is the starting point of the system and of the analyses within the thesis. If not otherwise mentioned, the circuit level components in these analyses are assumed to be ideal.

4.1. Anti-aliasing filter

The architecture has an inherent anti-aliasing, because the aliased signals are cancelled at the output of the ADC. However, the anti-aliasing only holds if the analog filters do not saturate. For OOBs, the LPF could saturate, in order to prevent this, the AAF is implemented. In other words, the AAF eases the saturation of the residue signal for OOBs. This is explained more thoroughly in the next section.

4.1.1. The impact of the AAF on the residue signal

To analyze the impact of the AAF, Figures 4.1, 4.2 and 4.3 give a good visualization of three regions which define the impact of the filters.

The first region (low frequencies $f_{in} \leq f_{BW}$, see Figure 4.1) is in the signal-band, as the AAF should not impact this region. A maximum in-band ripple of the AAF magnitude response is set. The AAF together with the LPF define the bandwidth of the system, because, at 400MHz the decrease of the SNR must be 3dB compared to low in-band frequencies. The decrease of the SNR is due to the decrease of signal magnitude, causes by the attenuation of the AAF and LPF filters.

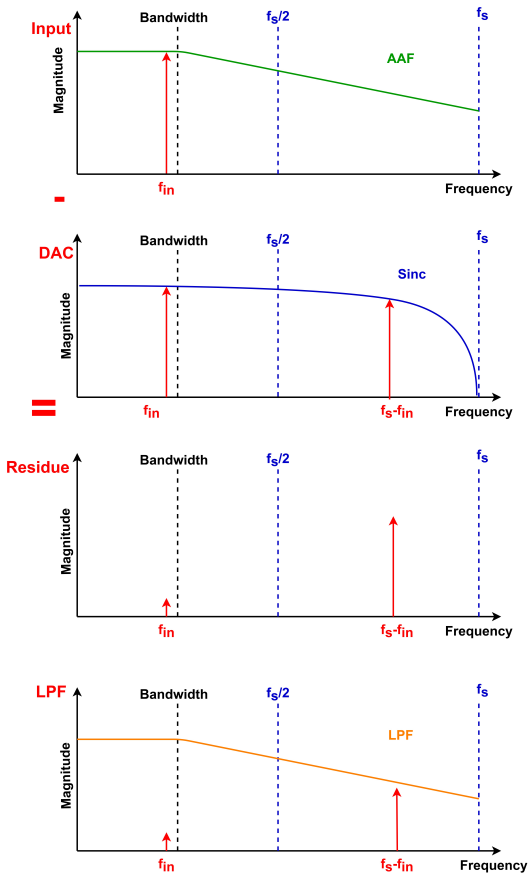

Figure 4.1: Attenuation of an in-band signal

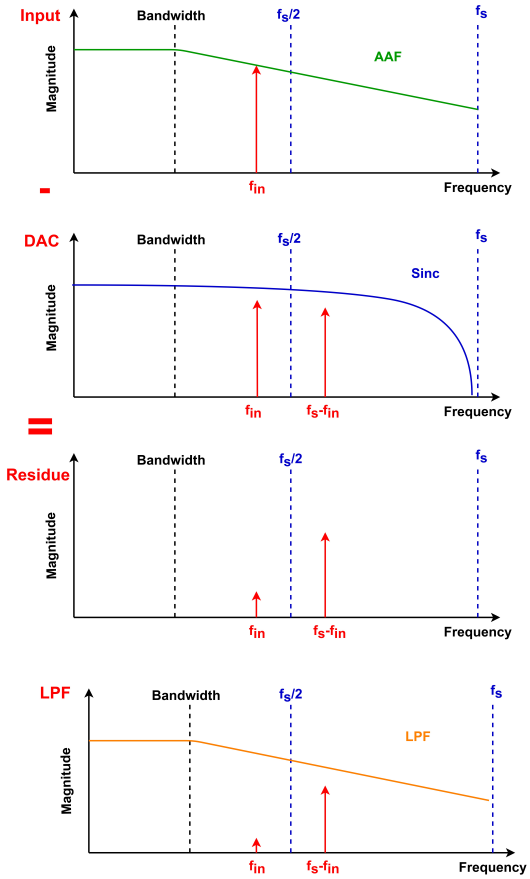

Figure 4.2: Attenuation of an OOB interferer

Second is the OOB region (middle frequencies $f_{BW} < f_{in} \leq f_s - f_{BW}$, see Figure 4.2). Here, a mutual dependence on the AAF and the LPF define the needed attenuation to achieve a certain gain in the LPF. The analysis of this region is complex and needs to be evaluated for each individual situation, since the optimum shifts depending on the sampling rate of the coarse ADC, the APF compensation, the amount of gain that needs to be applied etc. Nevertheless, on the whole, it can be stated that a large attenuation is beneficial for this region. The order of the filter is practically limited to two, thus to achieve the largest attenuation, the roll off from the filter must be as steep as possible.

Third is the far OOB region (high frequencies $f_{in} > f_s - f_{BW}$, see Figure 4.3), which is mainly determined by the AAF. However, this is not entirely the case as the minimum attenuation before the OOB falls in-band is determined by the sampling frequency and the attenuation of the AAF. This is explained next.

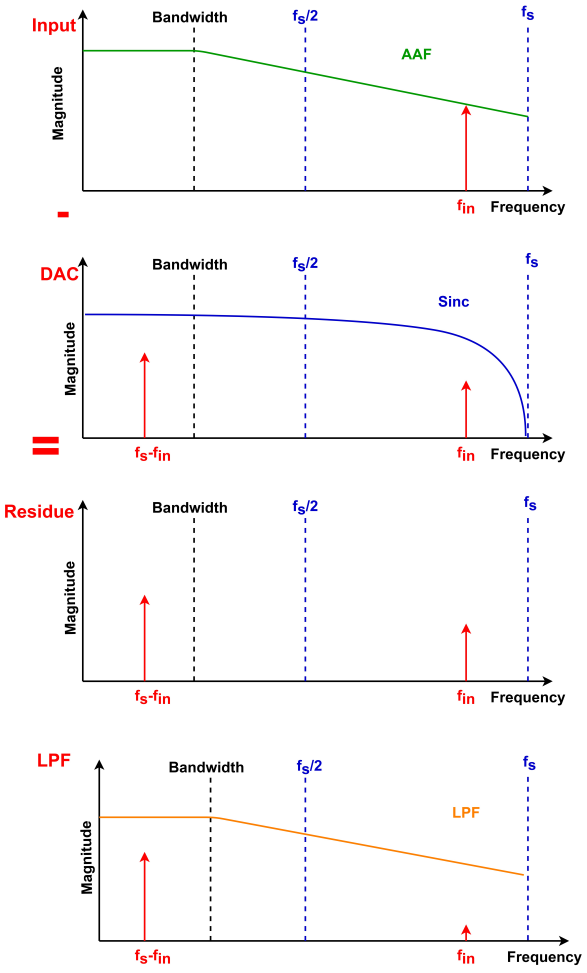

Figure 4.3: Attenuation of a far OOB interferer

$$f_{alias} = f_s - f_{in} \tag{4.1}$$

Filling in the smallest frequency to fall in the signal-band, $f_{alias} = f_{BW}$

$$f_{in} = f_s - f_{BW} \tag{4.2}$$

From 4.2 follows that the minimum attenuation for out-of-band blockers is equal to,

$$H_{AAF}(f = f_s - f_{BW}) \tag{4.3}$$

Equation 4.3 shows that the attenuation for the OOBs can be divided into two segments; first the attenuation of the anti-aliasing filter, second the sampling frequency of the coarse ADC. If it is assumed that the AAF has a low-pass filtering roll off, this means that for a larger OSR, the OOBs have a larger attenuation. In addition, a larger sampling frequency results in an improved the anti-aliasing performance.

4.1.2. AAF options

As a result of the analysis, a 2^{nd} order AAF proved to be sufficient, with a maximum amount of in-band ripple of 0.125dB. Consequently, the AAF options are reviewed based on these requirements.

For an AAF there are multiple ”standard” solutions, such as the regular 2^{nd} order filter, Butterworth, Chebyshev type 1, Chebyshev type 2 (or inverse) and elliptical filter. The elliptical filter is not considered because a 2^{nd} order elliptical filter results in the same as an inverse Chebyshev filter [25]. However, the other filters are evaluated.

From the previous analysis, it is clear that in all the frequency regions, a sharp filter roll off is beneficial for the performance of the AAF. The magnitude response of the different filters is given in Figure 4.4.

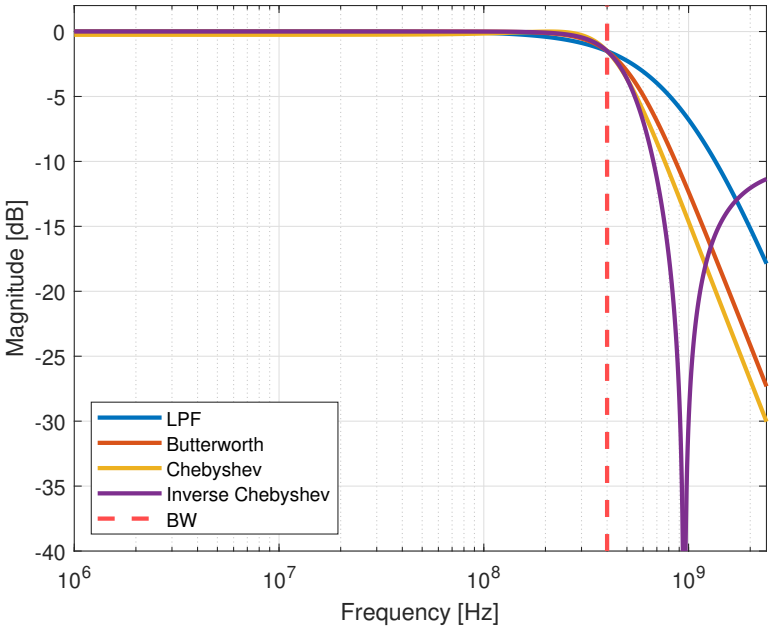

Figure 4.4: Magnitude response of the evaluated AAFs

Figure 4.4 shows that a regular 2^{nd} order filter has the least steep roll off, whereafter the Butterworth comes, and then the most steep roll off is the inverse Chebyshev filter. However, the inverse Chebyshev has a notch and afterwards an attenuation without a roll off, which is not ideal for the far OOBs. Moreover, the placement of the notch depends on the amount of attenuation after the notch (at high frequencies). The closer the notch is to the pass-band, the smaller the attenuation is at high frequencies [25]. This makes the inverse Chebyshev not the ideal implementation. In contrast, the Chebyshev has a less steep roll off, but keeps its roll off. Therefore, the Chebyshev is the best option, despite the fact that it has in-band ripple, but this can be designed to 0.125dB.

As stated before, the exact design of the poles and zeros of the AAF must be done together with the LPF.

4.2. The All Pass Filter

4.2.1. The latency compensation

Before zooming in on the APF design, the reason for the APF implementation must be understood. Hereafter, the effect of the bandwidth enlargement on the APF is considered. The DAC and coarse ADC (this is the SAR ADC), introduce a latency to the incoming signal at the summation node (see the green arrows Figure 4.5). The total latency of the input signal

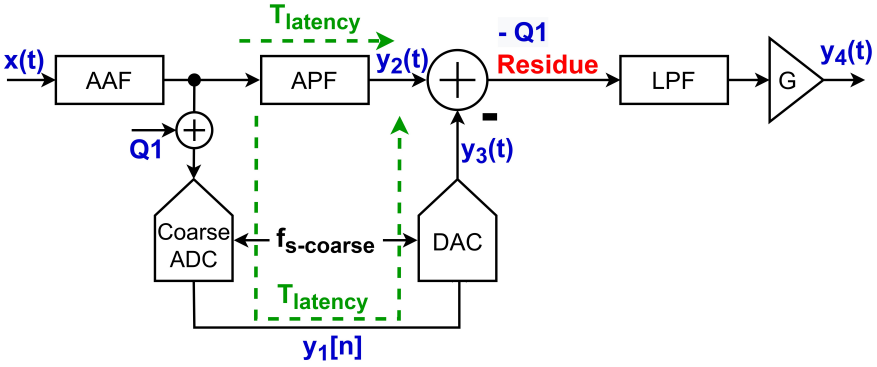

Figure 4.5: Front end of the ADC

in the coarse ADC/DAC path is equal to one-and-a-half times the sampling rate of the coarse ADC/DAC, which can be described as:

$$T_{latency}(s) = \frac{1.5}{T_s} \tag{4.4}$$

where $T_s = \frac{1}{f_s}$. One sampling clock cycle (T_s) of delay arises from the fact that the coarse ADC needs time to do the analog to digital conversion. The extra half sampling clock cycle is due to the pulse shape of the DAC. For low frequency input signals, the latency compensation is not as relevant as for high frequencies. This can be seen from the following example in which for a 1MHz signal, a single the period is takes 1μs, if the sampling frequency is 2.4GHz and the total latency is 625ps. Thus, the latency is just 0.225° of the entire phase of the signal. However, if the signal has a frequency of 400MHz, the latency makes up for 90° of the entire phase, this is 400 times larger. Consequently, the bandwidth enlargement from 40 MHz to 400 MHz, causes a 10 times larger phase shift at the signal band-edge. Moreover, the higher the frequency the larger the phase shift for a certain latency, since ideally the phase shift increases linearly with frequency.

Another important aspect of the latency compensation is the total amount of delay. As the total delay becomes larger, it will incorporate a larger part of the total phase of a certain frequency. Hence, the total latency should be kept at its minimum, since the smallest phase shift will be required, which is the easiest to compensate for. The relative phase shift of two sine waves can be described with the following equivalence:

$$sin(\omega t) - sin(\omega t + \phi(f)) = -2sin(\frac{\phi(f)}{2})cos(\omega t + \frac{\phi(f)}{2}) \tag{4.5}$$

In Equation 4.5, it can be seen that the residue mismatch does not depend on the frequency of the input signal. However, it does depend on the phase $\phi(f)$, which again depends on the frequency. This dependency is linear, because the latency is constant and only the frequency increases. Therefore, the phase delay is equal to the group delay.

Furthermore, the phase difference of the input signal relative to the phase shift of the coarse path is relevant. As the phase difference increases, the magnitude of the residue signal increases, which is verified in Figure 3.2.

Due to the phase mismatch, sharp peaking behavior arises in the residue signal, as shown in Figure 3.2. These sharp peaks indicate large magnitudes at high frequencies, which is unwanted. The increased magnitude of the residue signal can cause the amplifier to clip. Consequently, the relative phase difference must be reduced as much as possible. In other words,

the latency of the coarse ADC/DAC must be minimized, which is achieved by the latency compensation of the APF and decreasing the total latency; by increasing the sampling rate of the coarse ADC.

In addition, the latency compensation for out-of-band signals must be considered. Assuming a sampling rate of 2.4GHz of the coarse ADC/DAC, then the Nyquist bandwidth is equal to 1.2GHz. Therefore, coarse ADC behaves identical for signals up to 1.2GHz. However, the latency compensation at 1.2GHz incorporates a much larger phase shift than for 400MHz. If this phase shift is incorrectly compensated, this too will exhibit high frequency peaking behavior. The LPF after the summation node, see Figure 4.5 attenuates those frequencies. On top of this, the AAF reduces the input magnitude of these out-of-band frequencies. Both filters reduce the impact of the out-of-band latency compensation. Nevertheless, it should be monitored.

The phase shift must be obtained with a magnitude response that is flat or ”all-pass”. The magnitude transfer function of the APF should match the transfer function of the DAC. The DAC has a sinc response. Therefore, low-pass filtering could be beneficial. However, the sinc response exhibits a very small attenuation at the signal band-edge, depending on the sampling rate of the coarse ADC. Although, the low-pass filtering must not limit the bandwidth of the system, hence the aim is to have a flat magnitude response. A ”high-pass” filtering response is unwanted, since the case of a non-ideal latency compensation the high frequency components that arise are magnified. This could saturate the node at the output of the LPF, in case of a well-designed closed loop filter.

All in all, the APF must have a flat magnitude response with a linear phase response that is valid up to a frequency that is as high as possible. A slight low-pass filtering can be beneficial to mimic the sinc response of the DAC. Nevertheless, the most important property is the phase shift of 90° at the signal-band-edge. Therefore, the analysis is focused on the signal bandwidth of 400MHz.

4.2.2. Overview of latency compensation schemes

To explore the latency compensation described in the previous section, an overview is made with the possible latency compensation schemes. In this overview, the main advantages and disadvantages are reviewed. To achieve a certain latency compensation, multiple solutions are available. Figure diagram 4.6 shows possibilities for a certain phase compensation. All of the possibilities seen in the diagram are briefly reviewed. In order to review the possibilities, a distinction is made between the continuous time and discrete time latency compensation.

First, the continuous time solutions are examined. More precisely, the Radio Frequency (RF) circuit design inspired solutions. The polyphase filter (PPF) has a very accurately defined phase compensation at a single frequency. This technique can be made suitable for wider bandwidths. Nevertheless, it will still perform much better at certain frequencies than others. Furthermore, if the PPF is made more wideband, its area consumption will be much larger, especially because 400MHz is a relatively low frequency [26]. The noise performance is limited to the resistor values, but these can be scaled. Another RF inspired phase compensation are transmission lines, which too can set a certain latency accurately, although it is a narrowband solution. Most importantly, a transmission line designed for a certain phase compensation at 400MHz is very long, since $s = c/f_{BW}$, where c is the speed of light. The speed of light is an overestimation. Nevertheless, a single wavelength is approximately 75cm. In the design of a transmission line, the length is a fraction of the total wavelength. However, even if a tiny

fraction of 75cm is taken, the length is orders of magnitude from a realistic chip size, hence it is not suitable for this ”low” frequency operation [27].

The analog circuit design solutions are active APFs and passive APFs. Active APFs are based on active components, such as a Gm-C, an OPAMP-RC etc. The active APFs are based on an orthonormal filter design. The active APF could give a very well-defined latency compensation. However, the main disadvantage of the active filter implementations is the power consumption. This is ”extra” power that is consumed, which is not the case for passive RC filters. The active continuous time APF has a less accurately defined phase compensation than the discrete time solutions. Furthermore, the active filters have to fulfill the linearity and noise requirements. The other analog circuit design method is a ”simple” passive RC network, which in the previous works [1], [22], gives sufficient latency compensation. This will consume a relatively small area and does neither consume power nor impact the linearity. The main disadvantage is the phase compensation, this is not as accurate as the other solutions. Next to this, noise performance is limited to the resistor values. However, the resistors can be scaled to improve the noise performance.

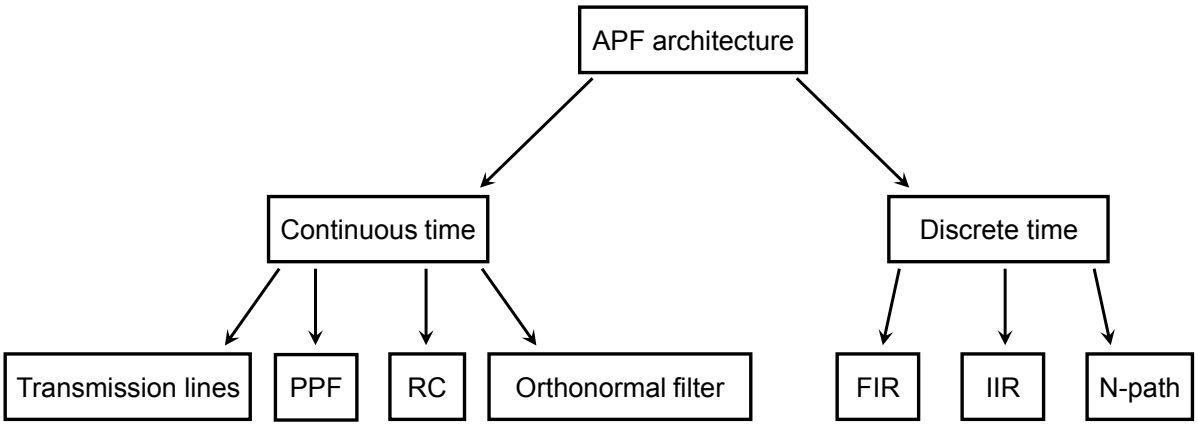

Figure 4.6: Diagram APF implementation possibilities

The discrete time solutions are the finite impulse response (FIR), the infinite impulse response (IIR) filters and the N-path filters. For the FIR and IIR filters, the main advantage is that the phase response can be made linear and can be set very accurately. However, these filters sample the input signal, which adds noise and creates aliases. The aliasing can be suppressed by the scaling of coefficients or by using a windowed integration with a gm-C cell [28], [29]. For the N-path filters, the main disadvantage is the pre-filtering to suppress the folding [30]. To achieve these alias suppressing methods, active components must be used, which increases the power consumption. On top of this, for the FIR and IIR filters, the APF must not attenuate the signal magnitude in the signal bandwidth. Consequently, a larger sampling rate than the sampling rate of the coarse ADC is needed or time interleaving of the filter can be used. However, time interleaving brings its own problems. The N-path filters sample the input, thus in either way, the clock of the system is more heavily loaded. Furthermore, the large bandwidth of the system (400MHz) makes the discrete time filters even more power consuming. On the top of that, the discrete time filters have active components, consequently these will limit the power and or linearity of the filter. All in all, the discrete time filters could be an option if very accurate phase compensation is needed, but aliasing, power consumption and reduced linearity is the trade-off. The N-path filter is recommended looking into.

As a result, a passive RC seems to be the most obvious choice. It has proved to function properly [1], [22]. Moreover, it benefits from the relative small area and does not impact the

linearity and power consumption. However, the phase compensation is not as accurate as the other solutions. Therefore, a very well-defined phase compensation from the design itself is more important. This will be done in the next sections.

4.2.3. Mathematical latency compensation derivation

The goal is to compensate for the latency of the coarse ADC/DAC, which is just a delay in time domain. However, what would it look like in the Fourier domain? A continuous time Fourier transform of a pure delay is equal to

$$f(t-\tau) = e^{-s\tau}F(s) \tag{4.6}$$

The problem arises with the fact that the delay in the Fourier domain cannot be expressed as a rational polynomial. However, approximations can be made such as,

$$e^{-s\tau} \cong 1 - s\tau + \frac{(s\tau)^2}{2} - \frac{(s\tau)^3}{6}... \tag{4.7}$$

$$e^{-s\tau} \cong \frac{1}{1 + s\tau + \frac{(s\tau)^2}{2} + \frac{(s\tau)^3}{6}...} \tag{4.8}$$

$$e^{-s\tau} \cong \frac{1 - \frac{s\tau}{2}}{1 + \frac{s\tau}{2}} \tag{4.9}$$

$$e^{-s\tau} \cong \frac{1}{[1 + \frac{s\tau}{n}]^n} \tag{4.10}$$

As n increases, the accuracy of the polynomials increase too, [31]. Nevertheless, all of the polynomials exhibit different pro's and cons, such as the feasibility regarding their implementation, the magnitude response and the phase error they exhibit at the signal-band-edge. Note that the expressions (4.9) and (4.10) have the form of a common APF and LPF, whereas Equation (4.7) has a high-pass filtering response. First, their accuracy will be revised with their magnitude response. The phase error is examined in the signal bandwidth for different orders of the polynomials, which is done in MATLAB©.

The results are listed in Table 4.1. It can be concluded that for higher order transfer functions, the latency compensation improves. In other words, the latency compensation improves by introducing more poles and zeros, with the exceptions of the odd order transfer functions for (4.7) and (4.8).

From Equation (4.9) and Table 4.1 it can be seen that if the pole and zero compensate each other, a unity gain response is achieved. This is illustrated in Figure 4.7.

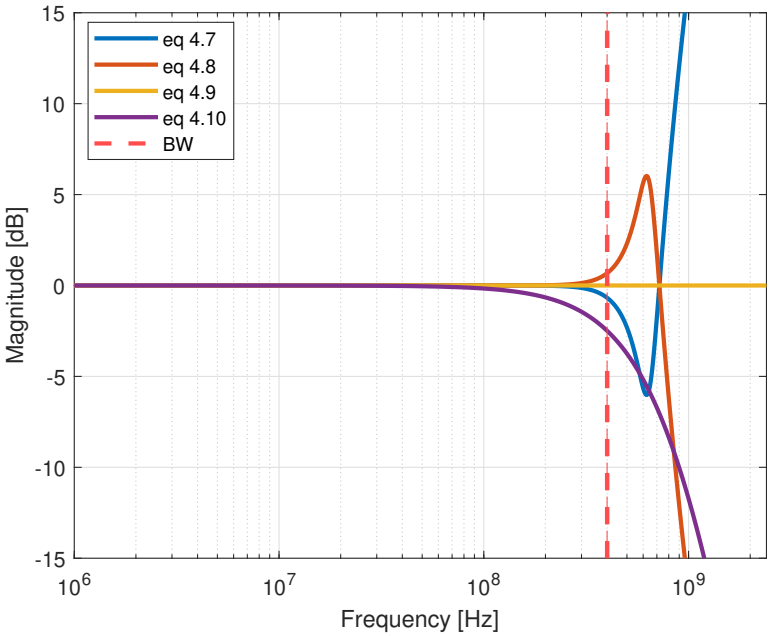

Figure 4.7: Magnitude response of the 4^{th} order transfer functions, $\tau = \frac{1.5}{f_s}$

Transfer functions		Order (n)	Phase error at 400 MHz [°]	Phase error at 1.2GHz [°]	Magnitude at 400MHz [dB]
$1 - s\tau + \frac{(s\tau)^2}{2}...$	4.7	1	32.5	192.0	5.4
		2	-9.0	115.0	4.0
		3	-14.2	38.4	-0.4
		4	1.2	-39.4	-0.7
$\frac{1}{1+s\tau+\frac{(s\tau)^2}{2}...}$	4.8	1	32.5	192.0	-5.4
		2	-9.0	115.0	-4.0
		3	-14.2	38.4	0.4
		4	1.2	-39.4	0.7
$(1 - \frac{s\tau}{2})/(1 + \frac{s\tau}{2})$	4.9	2	13.7	136.0	0.0
		4	1.2	136.0	0.0
$\frac{1}{(1+\frac{s\tau}{n})^n}$	4.10	1	32.5	192.0	-5.4
		2	13.7	136.0	-4.2
		3	7.1	97.4	3.2
		4	4.2	71.3	-2.5

Table 4.1: Simulation results, phase error and magnitude response

Regarding the magnitude response of the derived equations, Equation (4.7) and (4.8) have a largely varying magnitude transfer, which is unwanted. Equation (4.10) behaves as a LPF, with a large attenuation at the signal band-edge. This can compensate for the sinc response of the DAC. However, this is a very small attenuation. Hence, zeros are wanted in the transfer to compensate for this. This is done in Equation (4.9), which exhibits a unity gain response and has the most wideband phase response.

From the previous analysis, increasing the order of Equation (4.9) is a starting point to examine more thoroughly, since it is the only one with a unity gain magnitude response. As

stated before, for a higher order of the transfer function, a better the latency approximation can be achieved. If Equation (4.9) is made 4^{th} order, the phase compensation can be seen in Table 4.1. Note, a higher n^{th} order for (4.9) is not stated in [31], therefore it is not a mathematical derivation of the latency and the τ must be adjusted. The 4^{th} order transfer is the best and the most wideband solution for the latency compensation.

As stated before, the latency compensation improves with a higher order transfer function. Combining this idea with the poles and zeros that compensate each other, the magnitude response is flat. A high-pass magnitude response is unwanted. On the other hand, a small low-pass filtered response is acceptable or even wanted as long as it does not limit the system bandwidth. Applying this idea to a transfer function means that the order of the denominator is always at least as large as the numerator or larger. A generic APF filter achieving the requirement of our ADC can be expressed as:

$$H(s) = \frac{(1 - s/\omega_z)^n}{(1 + s/\omega_p)^d} \quad , \qquad where \;\; d \geq n \tag{4.11}$$

here, ω_p and ω_z are the poles and zeros, d is the order of the denominator and n is the order of the numerator. These transfer functions are examined more thoroughly to confirm the previous analysis and gain more insight. Additionally, the APF filter used in the SAR assisted CT $\Delta\Sigma$ ADC [1] is examined. The transfer function of the APF is [1],

$$H(s) = \frac{(1 - s/\omega_z)^2}{(1 + s/\omega_p)} \tag{4.12}$$

Notice that the transfer function, has a high-pass filtering function. However, since there is a functioning APF circuit implemented in SAR assisted CT $\Delta\Sigma$[1], it is worthwhile to examine the performance.

To reduce the complexity of the analysis, all the different orders for the transfer functions from 4.11 are evaluated with all poles and zeros at the same location. Higher orders of the transfer functions are not investigated, because their implementation will be very complex and probably cannot be done without adding active components. The results are summarized in Table 4.2:

Name	**Transfer functions**	**Phase error at 400 MHz [°]**	**Phase error at 1.2GHz [°]**	**Magnitude at 400MHz [dB]**
2^{nd}	$(1 - s/\omega_z)/(1 + s/\omega_p)$	$5{\cdot}10^{-2}$	127.0	0.0
3^{rd} HPF	$(1 - s/\omega_z)^2/(1 + s/\omega_p)$	$-4{\cdot}10^{-2}$	90.1	1.2
3^{rd} LPF	$(1 - s/\omega_z)/(1 + s/\omega_p)^2$	$-4{\cdot}10^{-2}$	90.1	-1.2
4^{th}	$(1 - s/\omega_z)^2/(1 + s/\omega_p)^2$	$8{\cdot}10^{-2}$	65.4	0.0
5^{th}	$(1 - s/\omega_z)^2/(1 + s/\omega_p)^3$	$3{\cdot}10^{-2}$	48.7	-0.4

Table 4.2: Different orders of a transfer function

From Table 4.2 it can be concluded that higher order APFs achieve better latency compensation. A limitation of the analysis is for the higher order transfer function, where the first pole and zero frequency matches, but the second pole and zero frequency are set at a higher frequency. This could be interesting to improve the out-of-band performance of the APF, which could lead to a larger gain at high out-of-band frequencies.

4.2.4. Residue signal optimization

In this section, the impact of the APF on the residue signal is reviewed. This is done by examining the suppression of the signal content in the residue signal. The transfer functions from

Table 4.2 are examined and are referred to by Figures 4.8, 4.9, 4.10 and 4.11. Furthermore, the transfer function of the DAC is taken into account, which is a sinc response [2]. The overall transfer function of the coarse ADC and DAC introduce the entire latency, which can be expressed as:

$$H_{ADC/DAC}(j\omega) = \frac{sin(\pi f/f_{s-coarse})}{\pi f/f_{s-coarse})} e^{-j\pi(1+0.5)f/f_{s-coarse}} \tag{4.13}$$

The latency consists of two components, the $0.5f_{s-coarse}$ comes from the zero-order hold (ZOH) function of the DAC. The other $f_{s-coarse}$ is caused by the latency of the coarse ADC. For analysis of Figures 4.8, 4.9, 4.10 and 4.11 the residue signal can be expressed as:

$$H_{Residue}(j\omega) = H_{APF}(j\omega) - H_{ADC/DAC}(j\omega) \tag{4.14}$$

Note that in Equation 4.14 the quantization error is not yet taken into account, because no matter what the latency compensation is, the quantization signal will be present in the residue signal. In other words, Figures 4.8, 4.9, 4.10 and 4.11 assume an infinite resolution for the coarse ADC. At last, it must be mentioned that the aliasing of the signal is not taken into account.

First, the residue signal is examined for different APF filter implementations, whereafter the other filters are included one by one. The result is given in Figure 4.8.

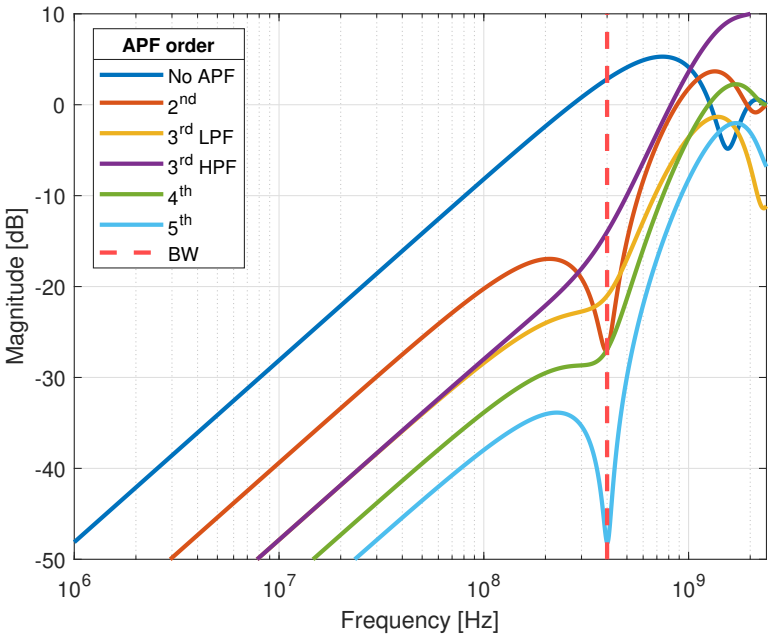

Figure 4.8: Magnitude of residue signal, with only the APFs implemented

From Figure 4.8 it can be seen that the high-pass filtering function of the 3^{rd} order APF from the SAR assisted CT $\Delta\Sigma$ ADC [1] is not the ideal magnitude transfer for the signal suppression. Apart from that, the low-pass filtering seems to suppress the input signal. On top of this, it can be seen that for different orders of the transfer functions the peaking behavior, at high frequencies, is at other frequencies. This can be explained because phase response is at its worst for different frequencies. At last, it can be concluded that for higher order APFs, the residue is suppressed more, thus a larger gain can be applied.

From Section 4.1 of the AAF analysis, it is clear that for the AAF a Chebyshev type 1 filter is wanted. Hence, a non-limiting attenuation of 0.05 dB at the band-edge used for the AAF. The result of the AAF can be seen in Figure 4.9.

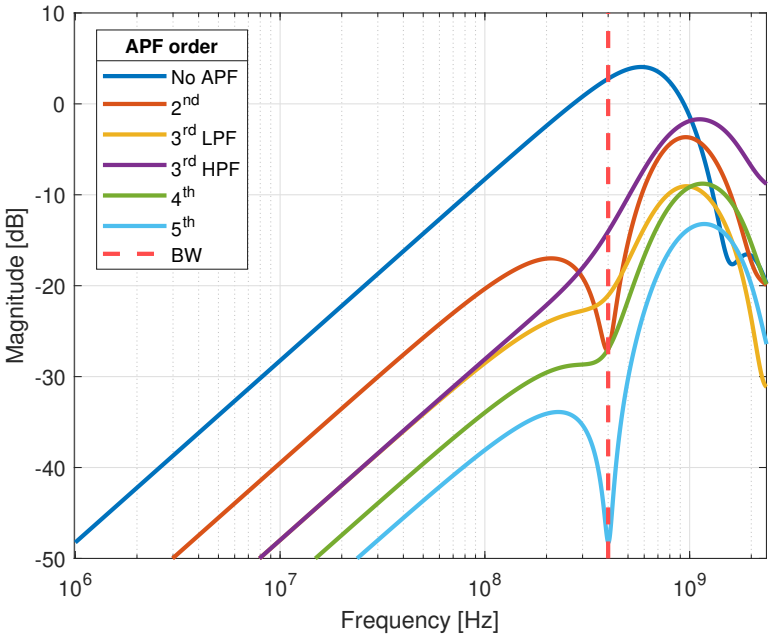

Figure 4.9: Magnitude of residue signal, with an AAF and the APFs implemented

First of all, Figure 4.9 shows that the AAF attenuates the out-of-band and far out-of-band signals, which increases the maximum applied gain to the signal. Secondly, in terms of magnitude, it can be seen that the 4^{th} order transfer function makes a large improvement with regard to Figure 4.8.

Not only an AAF will be applied in the system, but also a LPF. Hence, the combined impact of the LPF and the APF will be examined. To give a good visualization of the impact of the LPF and APF combination, the bandwidth of the LPF is set to 400MHz. The results are shown in Figure 4.10.

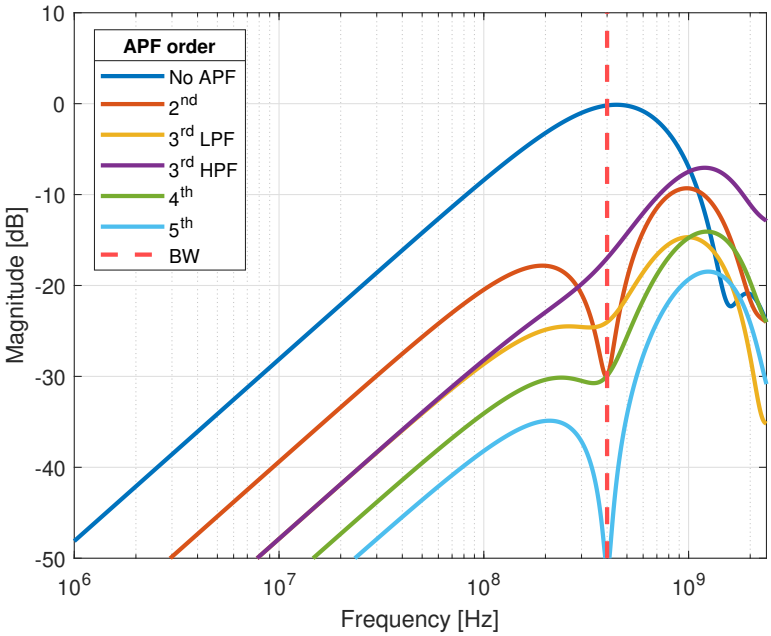

Figure 4.10: Magnitude of residue signal, with a LPF and the APFs implemented

It can be seen that the gain that can be applied, increases. Furthermore, the maximum residue signal magnitude shifts to a lower frequency, hence the low-pass filtering causes the minimum gain to be defined around 1GHz.

Combining the AAF and LPF to examine the influence of the APF, results in Figure 4.11.

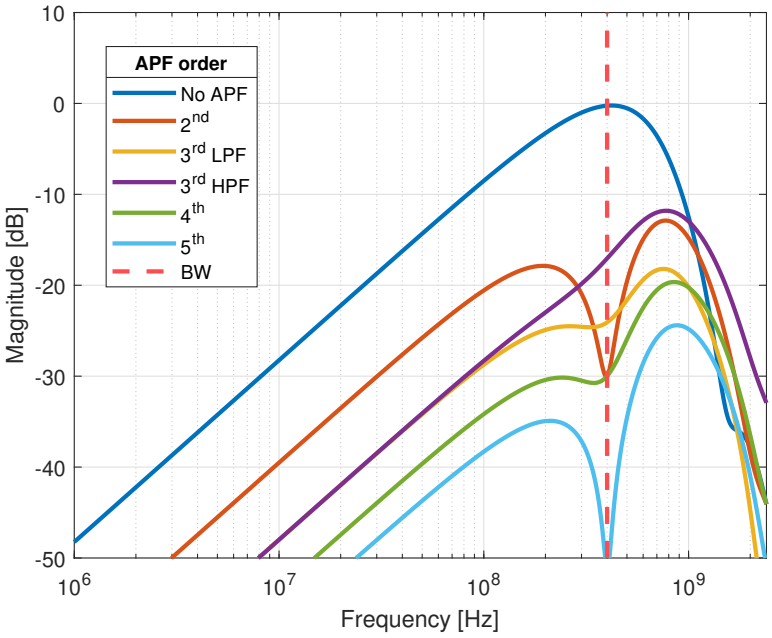

Figure 4.11: Magnitude of residue signal, with all (AAF, LPF and the APFs) the filters implemented

From Figure 4.11, the largest magnitude is defined by the combination of the latency compensation and the amount of filtering. Nevertheless, it can be concluded that as long as Equation 4.11 holds, the latency compensation improves with the order of the APFs. Furthermore,

a high-pass filtering function is unwanted, as can be seen from Figure 4.11. However, a slight low-pass filtering in the APF is also beneficial to suppress the input signal content, because the sinc response of the DAC too has a slight low-pass filtering. The low-pass filtering does limit the bandwidth of the system.

At last, the pole and zero positioning is important to look at. They can shift the gain that can be applied to the residue signal. As before, the AAF is given a 0dB of attenuation at the band-edge and the LPF a 3dB of attenuation at the band-edge. For this, the pole and zero location of the 4^{th} order APF is reviewed. Figure 4.12 shows that the pole and zero location indeed impact the maximal gain that can be applied. Note that the AAF/LPF are not optimized, hence Figure 4.12 is only illustrative.

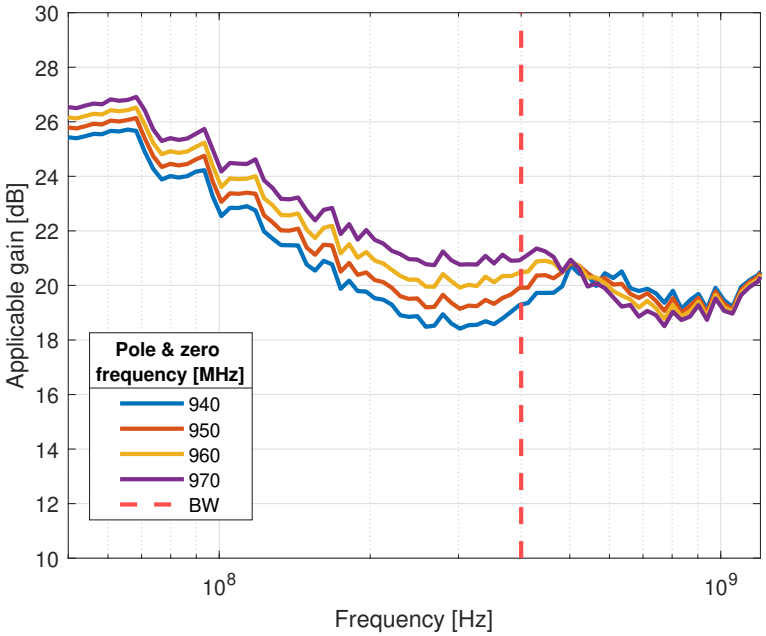

Figure 4.12: Applicable gain after LPF, for different latencies of the 4^{th} order APF

For a lower pole and zero frequency of the APF, the total latency increases. Hence, the latency compensation is not optimized for the band-edge anymore, thus in-band there is a larger phase mismatch. This can be seen by the smaller in-band gain. However, out-of-band the APF latency compensation is better, hence the larger out-of-band gain. Note that in Figure 4.12 a 5 bit coarse ADC is included. Moreover, Figure 4.12 shows the trade-off in the positioning of the poles and zeros of the APF. The exact positioning of the poles and zeros translates to the total of latency of the APF at a certain frequency. For smaller poles and zeros, the in-band gain decreases, but the out-of-band gain increases.

4.2.5. Proposed solution

The analyses of the previous sections show that the APF is a necessary component for an efficient operation of the system. It is concluded that, for a more accurate latency compensation, a larger gain can be applied. Moreover, the APF design has a major role in the gain that can be applied to the residue signal. In other words, the latency compensation improves, and thereby the gain, for a higher order of the APF. However, not only the latency compensation contributes to the performance of the APF, also the magnitude response has its impact. As shown, a high-pass transfer is unwanted, Although, a low-pass transfer function can be beneficial. The low-pass filtering of the APF does limit the bandwidth of the system. Therefore,

the 4^{th} order transfer function is chosen for the current implementation. The exact placement of the poles and zeros must be done together with the AAF and LPF, because this affects the out-of-band behavior of the system.

This APF analysis is limited to a fixed latency compensation of 625ps. However, for a smaller latency, a better compensation can be achieved for the same order of the filter. Hence, a larger sampling rate of the coarse ADC is interesting.

4.3. Low pass filter

The LPF must attenuate the quantization error and other high frequency errors that exist in the summation node. This allows the system to apply a large gain ”after” the filter, which is needed for the dynamic range of the system. Further, the LPF attenuation limits the bandwidth of the system. Hence, the LPF together with the AAF must be designed in such away that the bandwidth is 400MHz.

4.3.1. The impact of the LPF on the residue signal

The residue signal consists of the non-ideal latency compensation and the quantization error itself. The latter will exhibit high frequency components. Especially for signals that are near the signal band-edge, the quantization error has components at uneven multiples of the input signal [2].In Section 4.1, Figures 4.1, 4.2 and 4.3 describe the regions of an incoming signal and the effect of the LPF on it. The three regions will be considered next.

The first region, inside the signal-band, see Figure 4.1, it can be seen that the LPF attenuates the aliased tone of the input signal. The back end stage will benefit from this attenuation, because the back end samples the signal again and another alias is generated.

Second, with regard to the middle frequencies, see Figure 4.2, the input signal and its alias is attenuated by the LPF. It is expected that the APF will have the worst latency compensation around the middle to high frequencies. Consequently, the residue signal will be large, thus require attenuation. As stated in Section 4.1 the middle OOB region is suppressed by the AAF and the LPF, and it requires an analysis in which both the filters are taken into account. This must enable the application of the required gain.

Third, looking at the high frequencies, see Figure 4.3, the LPF has no influence on these frequencies in a two-stage design as the OOB fall back in-band. Here the LPF has no attenuation.

Next to this analysis, it is known that the quantization error consists of odd harmonic components. Moreover, it is known that when the resolution of the quantizer is larger, the power of the quantization error is distributed more evenly over its odd harmonics [2]. Hence, the higher frequencies have a larger portion of the total quantization error power. Therefore, if a larger amount of bits is resolved in the coarse ADC, the residue signal has more high frequency content. Assume that the latency compensation is ideal and that the LPF has a 3dB attenuation at the signal-band-edge. It is expected that the attenuation of the LPF has a larger impact on the magnitude of the residue signal when a larger amount of bits is resolved in the coarse ADC. Note that the for a larger amount of bits resolved, the residue signal is smaller, because the LSB size is smaller. Therefore, the gain that can be applied is larger. However, at the moment this is not the point of interest, thus the DC gains are normalized to zero to highlight the difference of the impact of the LPF. This is shown by Figure 4.13. Furthermore, Figure 4.13 has an ideal latency compensation and an equal sampling rate for all the quantizers. Figure 4.13 verifies the statement that the attenuation of the LPF has a larger impact on the magnitude

of the residue signal when a larger amount of bits is resolved. Apart from this, Figure 4.13 shows that when more bits are resolved, the gain improvement begins at a lower frequency. This phenomenon is can also be explained by the fact that the quantization error is spread out to the higher harmonics if a larger amount of bits is resolved [2].

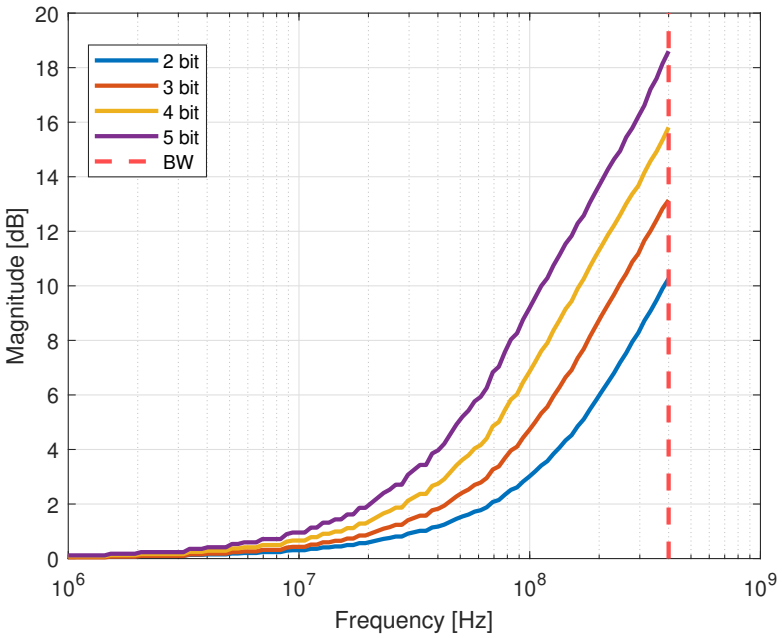

Figure 4.13: Gain after LPF, for different amount of bits, for an ideal latency compensation and the LPF has 3dB attenuation at 400MHz (f_{-3dB} = 622MHz). Note that for a better visualization of the LPF impact, the DC gains are normalized to 0dB

With an APF implemented, the latency compensation is not ideal. The 4^{th} order APF is implemented with the same 3dB attenuation as the LPF. The result is shown by Figure 4.14.

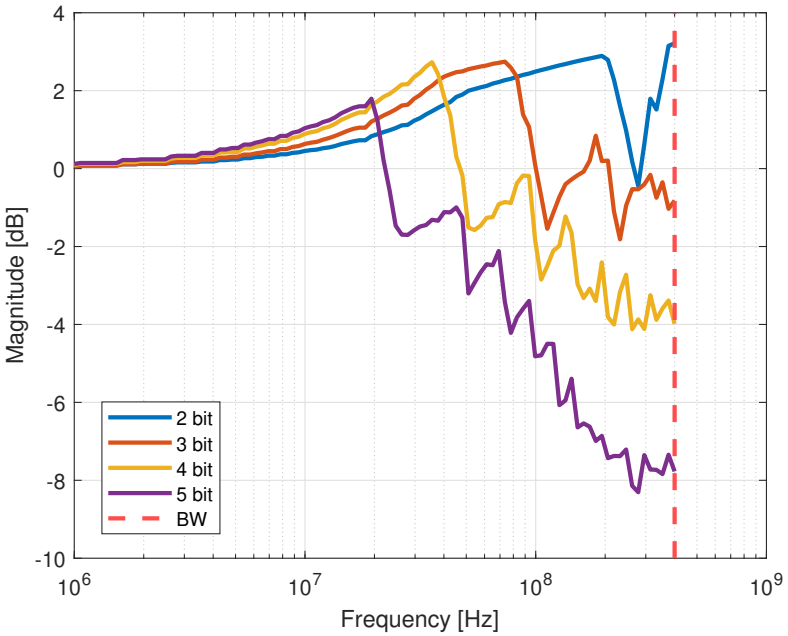

Figure 4.14: Gain after LPF, for different amount of bits, for an 4^{th} order APF, latency of 625ps and the LPF has 3dB attenuation at 400MHz (f_{-3dB}=622MHz). Note that for a better visualization of the LPF impact, the DC gains are normalized to 0dB

Figure 4.14 shows that the increase in gain due to a larger amount of resolved bits, does not outweigh the larger sensitivity to phase mismatch (of the coarse ADC that resolve a larger amount of bits). Again note that in Figure 4.14 the DC gain of all the curves is set to 0 dB.

All in all, on the one hand, the LPF needs a roll off as steep as possible, but on the other hand, the bandwidth of the system must be taken into account. Furthermore, the design of the LPF must be done simultaneously with the AAF.

4.3.2. LPF options

At first sight, the LPF implementation options seem to be the same as for the AAF. However, this is not the case and the Chebyshev and the Butterworth filters are hard to implement. Moreover, a goal of the thesis is to compare a closed loop LPF implementation to an open loop filter implementation. Therefore, it is chosen to limit the LPF to a regular 2^{nd} order filter.

4.4. The filters

As stated in previous sections, the AAF, APF and LPF cannot be designed separately. Therefore, this section briefly examines the eventual implementation when all of them are combined. Again, the maximum gain after the LPF is examined. The AAF is a 2^{nd} order Chebyshev filter, the APF is 4^{th} order with its poles and zeros at 965MHz, and the LPF is a regular 2^{nd} order filter. The attenuation at the band-edge of the AAF and the LPF are reviewed, while the bandwidth constraint is kept, see Figure 4.15.

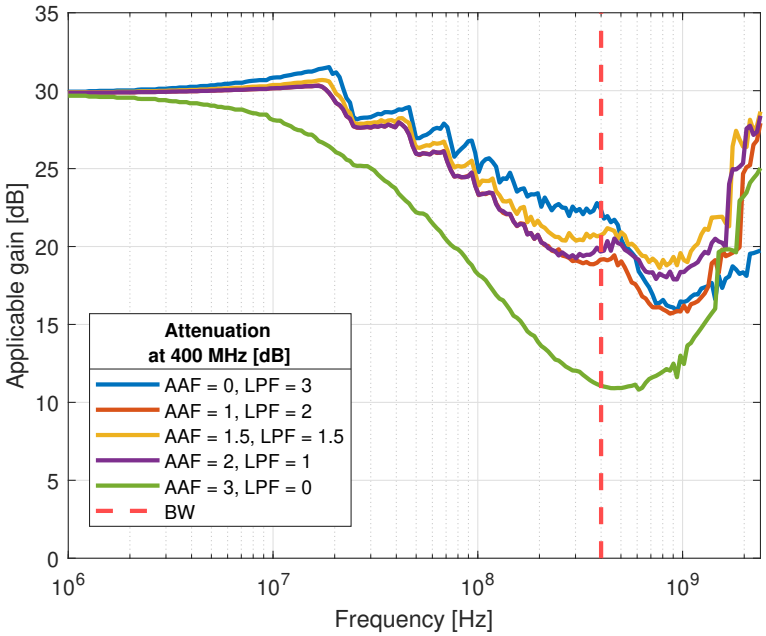

Figure 4.15: Applicable gain versus frequency, for a 4^{th} order APF

In Figure 4.15, it can be seen that the best option is close to an equal separation of the attenuation at the band-edge. Note that, this is for the current implementation. It does not necessarily have to hold for other architecture configurations of Chapter 5.
Next, the pole and zero placement is reviewed with this filter combination.

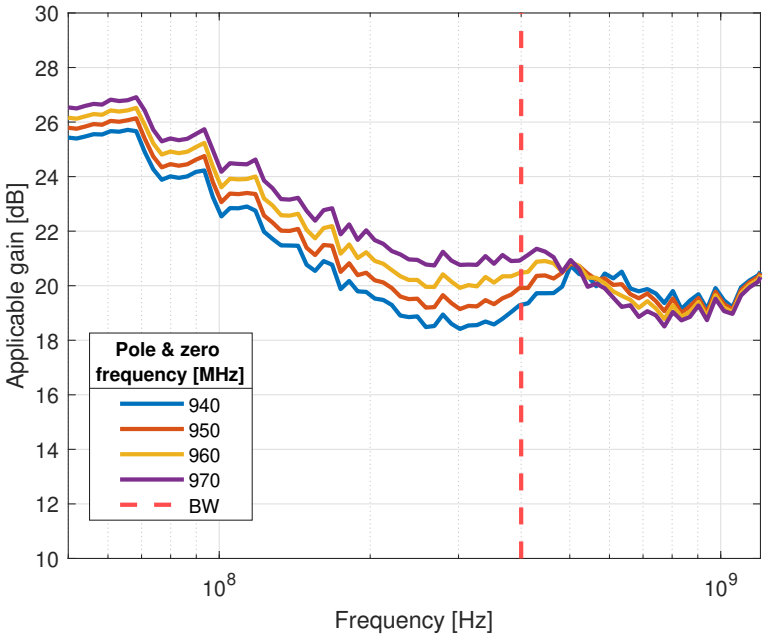

Figure 4.16: Applicable gain versus frequency, for a 4^{th} order APF, AAF and LPF have 1.5dB attenuation at 400MHz

Figure 4.16, shows that the best pole and zero frequency is at 950MHz. The maximum

gain that can be applied is 19.6dB. However, the ideal applicable gain with a perfect latency compensation is 29.8dB for a 5 bit coarse ADC. This is 10dB more than actually can be applied. Consequently, the 4^{th} order APF does not give sufficient latency compensation. Hence, a higher order APF must be used or the APF compensation must be relaxed. To relax the APF compensation, either the LPF must be implemented with a steeper roll of or the latency must be reduced.

4.5. Coarse ADC

In [1], the system architecture uses a coarse ADC that resolves 5 bits, but this can be adjusted. The amount of resolved bits inherently determines the maximum sampling frequency. The coarse ADC that is used, is based on the SAR ADC that is used in the SAR assisted CT $\Delta\Sigma$ ADC [1], which is the SAR ADC from [14].
From the previous sections, it can be concluded that the design benefits from a larger sampling frequency. This means that a smaller latency is easier to compensate for by the APF and it is better for the OOB immunity. If the sampling frequency is increased, the coarse ADC must be able to convert all the bits in one sampling clock cycle. As a result, the coarse ADC must convert fewer bits. Furthermore, when fewer bits are converted, a smaller gain can be applied to the residue signal. This is verified in Figure 4.17 and Table 3.1. Next to this, Figure 4.17 verifies the maximally applied gain of Equation 3.14.

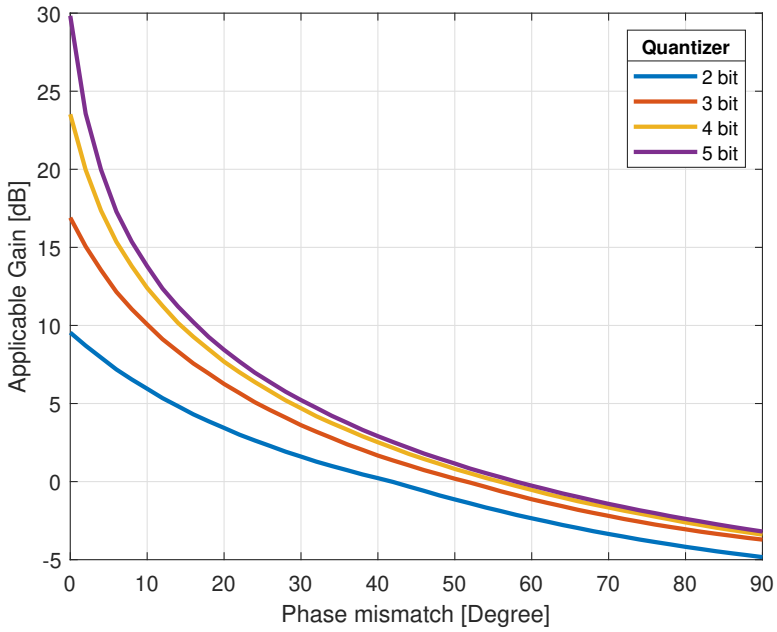

Figure 4.17: Applicable gain versus phase mismatch between the DAC and APF output, for different amount of resolved bits, with an ideal latency compensation and equal sampling rates

Equation 4.5 shows that for an ideal latency compensation, the phase mismatch becomes frequency independent. Hence, for an ideal latency compensation, one can deduce that the gain increases when the number of resolved bits increases. However, for a certain phase mismatch, the gain degradation is larger for a higher amount of resolved bits. Moreover, for phase mismatches up to $\approx 30^{\circ}$, the gain degradation is more sensitive to the phase mismatch. For example, when comparing the phase mismatch between B=5 and B=2, the 2 bit case pro-

vides a larger phase mismatch for the same amount of gain degradation. In other words, the latency mismatch sensitivity is larger for a larger amount of resolved bits in the coarse ADC. Furthermore, Figure 4.17 shows that the gain degradation is larger for smaller phase mismatches than for larger phase mismatches. This can easily seen by the fact that the slope of the curves changes. As a result, the smaller phase mismatches are more sensitive than the larger phase mismatches.

In the coarse ADC, the reference level of the quantizer can be adjusted. Figure 4.18 and Table 3.1 assume a LSB size of $V_{ref}/(2^N - 1)$. Here, the maximum and minimum reference levels of the quantizers are at $\pm$ 1 V_{supply}, see Table 4.3. However, if this is adjusted, the residue signal can benefit from a larger applicable gain. For simplicity, a 2 bit quantizer is examined and the supply voltage is 1V. Furthermore, Figure 4.18 shows that the quantizer levels, that are at 00 and 11 will overestimate the quantized input signal, the sine wave. This causes the reference levels of 00 and 11 to be bigger or equal to the input signal. As a result, the quantizer makes an error in a single direction. If the quantization levels are not scaled to the full reference voltage, but to the scaled quantization levels seen in Figure 4.19, where the error is fluctuating between $\pm$ instead of one direction, then the same signal can be quantized and the LSB can be reduced. This is visualized in Figure 4.19 and the corresponding reference levels are given in Table 4.3.

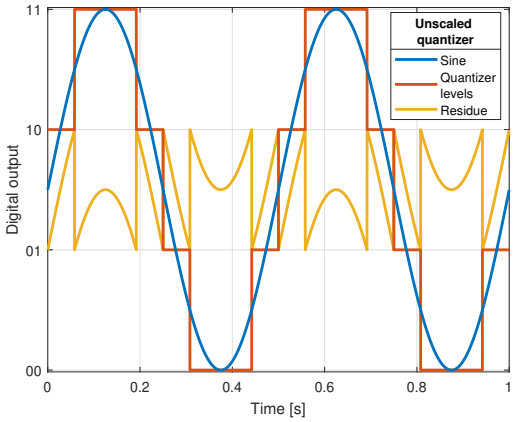

Figure 4.18: Unscaled 2 bit quantizer

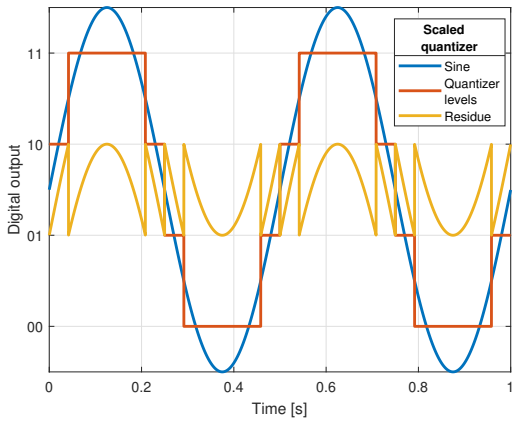

Figure 4.19: Scaled 2 bit quantizer

Digital code	**Unscaled quantizer**	**Scaled quantizer**
	Reference voltage [V]	
00	-1.0	-0.75
01	-0.33	-0.25
10	0.33	0.25
11	1	0.75

Table 4.3: Reference levels unscaled quantizer and scaled quantizer

Note, that the adjusted reference levels from Table 4.3 refer to the quantizer references, not the DAC output. The DAC has a supply voltage of 0.9V, hence the output of the DAC must be scaled to obtain the same output as quantizer reference levels, which is discussed in the next section.

All in all, a smaller amount of converted bits is a good point to examine more thoroughly, especially if the reference levels of the quantizer are shifted. This is because it enlarges the applicable gain, which then enables a larger SQNR.

4.6. DAC

The DAC implementation that will be used, is the same as in the SAR assisted CT $\Delta\Sigma$ ADC [1]. The exact design of the DAC is out of the scope of the thesis. Nevertheless, it must be mentioned that the transfer function of the DAC is in the continuous time path of $H_{CT}(s)$ (see Figure 3.1), consequently it must be taken into account when designing the digital back end.

As mentioned in the previous Section 4.5, the maximum magnitude of the residue signal decreases with a scaled quantizer. However, the signal is fed back by the DAC, not by the quantizer. Therefore, the DAC must be scaled to the same levels as the quantizer, which is examined next. Figure 4.19 shows the wanted output of the DAC. However, the reference voltage of the DAC is assumed to be unaltered. Consequently, a certain scaling factor must be applied to the DAC, as is shown in Figure 4.21. The scaling of the DAC can easily be done by changing the DAC resistance. The scaling factor can be expressed as:

$$Scaling\ factor = \frac{\frac{V_{ref}}{2^B}}{\frac{V_{ref}}{2^B - 1}} \tag{4.15}$$

$$Scaling\ factor = \frac{2^B - 1}{2^B}$$

Equation 4.15 shows that this scaling factor is the smallest for the least amount of bits. For a 2 bit coarse ADC, this is 0.75. Therefore, the quantization error is reduced by this amount. A reduction of 0.75, is -2.5dB and this causes the magnitude of the residue signal to have a reduction of -2.5dB. Hence, a larger gain can be applied to the residue signal. The gain that can be applied is expressed as:

$$Gain = 2^B \tag{4.16}$$

The maximally applied gain with the adjusted reference levels and the DAC scaling is given in Table 4.4.

Amount of bits	Gain [dB]
2	12.0
3	18.1
4	24.1
5	30.1

Table 4.4: The maximum gain applied to the residue signal, with the adjusted quantizer reference and DAC scaling, without latency mismatch

The input output relation of the quantizer and the DAC combined is shown in Figure 4.21. The unscaled version is shown in Figure 4.20.

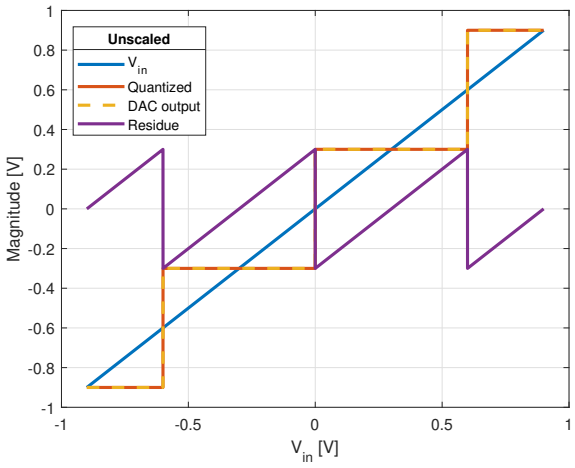

Figure 4.20: Unscaled quantizer levels and DAC, with the residue signal

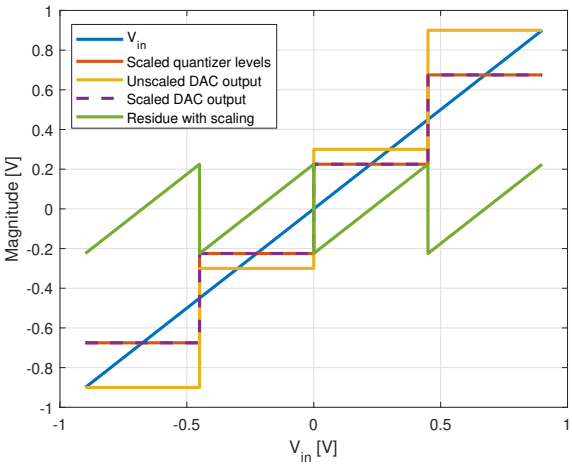

Figure 4.21: Scaled quantizer levels and DAC, with the residue signal

Figures 4.20 and 4.21, show that a larger gain can be applied to the residue signal. However, the residue signal also consists of the input signal, which too has an attenuation. Hence, the residue signal has an increased input signal magnitude, see Figures 4.22 and 4.23.

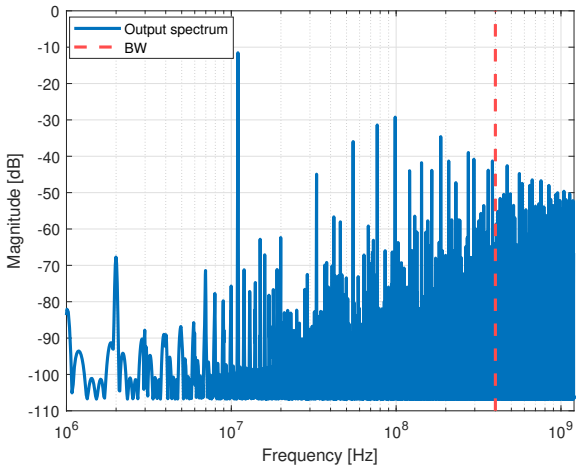

Figure 4.22: Unscaled ADC & DAC spectrum, f_{in}=11MHz

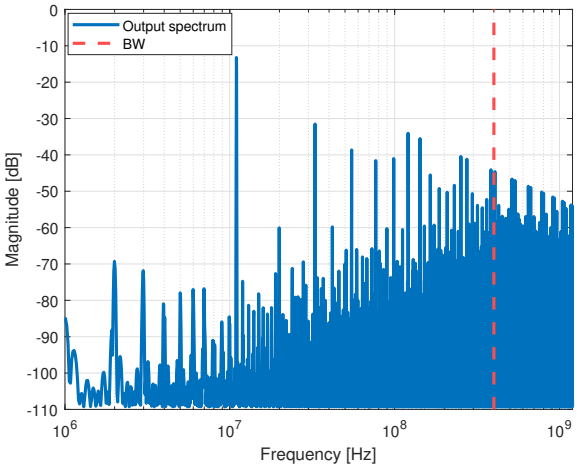

Figure 4.23: Scaled ADC & DACspectrum, f_{in}=11MHz

In Figures 4.22,4.23, it can be seen that the fundamental tone in the residue signal is larger with the scaled ADC/DAC and the 3^{rd} harmonic tone has increased. This makes the design of the linearity of the amplifier more stringent, although, the 5^{th} and 7^{th} harmonic decreased. Therefore, the total impact of the linearity is accepted. Note that the quantizer is not dithered. This is done in a later phase of the design. If the quantizer is dithered, the larger 3^{rd} harmonic tone is not present anymore. In other words, the scaling will not impact the tones at the output of the coarse ADC/DAC.

The intention of the scaling is to obtain a larger applicable gain. To review the effectiveness, the applicable gain is shown in Figure 4.24. Here the AAF and LPF have a 1.5dB of attenuation at the band-edge, together with the 4^{th} order APF is applied.

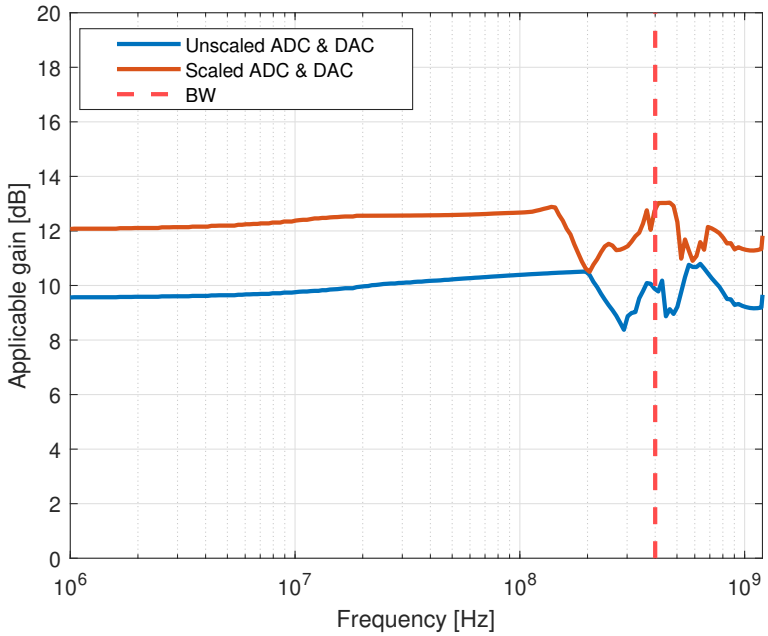

Figure 4.24: Gain improvement due to the scaling of the ADC & DAC

From Figure 4.24 it can be seen that a larger gain can be applied across all frequencies. The improvement is 2.1dB. For a 2 bit quantizer this is a relatively large improvement, which could be beneficial for a multi-stage design.

At last, the quantization error is reduced, which makes the digital mismatch requirements more relaxed. All in all, the scaled quantizer and DAC is beneficial for the performance of the ADC.

4.7. Conclusion

For the implementation of the APF, the passive RC network seems to be the most obvious choice, because it benefits from a small area, noise and no power and linearity requirement. This seems so despite the fact that the trade-off is the phase compensation, which is not as accurate as the other solutions. Therefore, a very well-defined phase compensation from the design itself is very important. On the other hand, the discrete time filters could be an option if very accurate phase compensation is needed, but then aliasing, power consumption and reduced linearity is the trade-off.

In conclusion the previous analyses, the AAF together with the LPF ease the saturation of the residue signal for OOBs. For both filters, it is desirable to have an as steep as possible roll off. To accomplish this, the AAF is implemented with a 2^{nd} order Chebyshev filter and the LPF is implemented with has a regular 2^{nd} order filter. Assuming that the APF has a flat magnitude response, that makes the AAF and the LPF determine the system bandwidth. In addition, a larger sampling frequency of the coarse ADC results in an improved anti-aliasing and OOB performance. The APF must compensate for a total latency of $\frac{1.5}{f_{s-coarse}}$ at the signal-band-edge, in which for the latency the following holds:

- Ideally, the phase shift increases linearly with frequency.
- The total latency must be kept at a minimum, because then the smallest phase shift will be required, which is the easiest to compensate for by the APF.

- The phase difference of the input signal relative to the phase shift of the coarse path is relevant.
- The total phase shift of the coarse ADC/DAC path must be minimized, which is done by increasing the sampling rate of the coarse ADC.

These statements lead to requirements for the APF. Nevertheless, more conclusions on the APF can be drawn from the analysis:

- The APF must have a flat magnitude response with a linear phase response that is valid up to a high as possible frequency. A slight low-pass filtering can be beneficial to mimic the sinc response of the DAC.
- Higher order APFs achieve more accurate latency compensation, by introducing more poles and zeros in the transfer function.
- The exact positioning of the poles and zeros translates to the total of latency of the APF at a certain frequency. With smaller the poles and zeros, the in-band gain decreases, but the out-of-band gain increases.
- The largest magnitude of the residue signal is determined by the combination of the latency compensation and the amount of filtering.
- The exact placement of the poles and zeros must be performed simultaneously with the AAF and LPF, because this affects the out-of-band behavior of the system.
- The APF is implemented to minimize the magnitude of the residue signal, by decreasing the signal amplitude in the residue signal.

The residue signal is a very important signal in the system. Therefore, the system level blocks that impact it are examined thoroughly. Apart from the AAF, APF and LPF, the coarse ADC and DAC impact the residue signal too. Their impact can be summarized as follows. First, in terms of applicable gain, the smaller phase mismatches are more sensitive than the larger phase mismatches. Note that this is independent of the amount of resolved bits. Second, the scaled quantizer levels and scaled DAC result in a larger applicable gain. This is most beneficial for small amounts of converted bits (B$\leq$ 3). The residue signal will exhibit a larger 3^{rd} harmonic, but reduced 5^{th} and 7^{th} harmonics. This can be neglected if the quantizer is dithered. Nevertheless, the residue signal has more signal content. Furthermore, the digital mismatch is relaxed, because the quantization error is smaller.

Apart from this, for a larger amount of resolved bits in the coarse ADC, the larger attenuation of the LPF on the residue signal does not outweigh its larger sensitivity to phase mismatches. As a result, the applicable gain will decrease more due to the larger amount of resolved bits. Note that this holds for a latency compensation with a 4^{th} order APF, for a total latency of 625ps.

It is shown, that for a 5 bit coarse ADC with a sampling frequency of 2.4GHz, the applicable gain after the LPF is 10dB less than the ideal gain. Consequently, the 4^{th} order APF does not supply sufficient latency compensation. Therefore, an interesting direction to examine is the reduction of the amount of bits in the coarse ADC. By decreasing the amount of bits resolved in the coarse ADC, the sampling rate of the coarse ADC can be increased. This will cause a decreased latency, which is easier to compensate for by the APF. Moreover, the gain degradation is less sensitive to the latency mismatch for smaller amount of resolved bits, thereby easing the APF design further. On top of this, the OOB blocker immunity is increased, because the aliased tones are suppressed more by the AAF.

5

System study

The aim is to design an ADC for automotive radar applications, and this entails certain requirements. As listed in Table 1.1, it is given that the ADC must have an as low as possible power consumption. As this power consumption is immeasurable, the power consumption is calculated. It is known that the system must obtain a DR 70dB, to have a competitive design for its bandwidth. The power consumption can be calculated with the Schreier FoM. In Figure 2.1, the Murmann graph is shown. It can be seen that the goal for the FoM is 172dB. The Schreier FoM is expressed as:

$$FoM_s = 10log_{10}(\frac{SNDR \cdot BW_{system}}{P_{diss}}) \rightarrow SNDR_{dB} + 10log_{10}(\frac{BW_{system}}{P_{diss}}) \tag{5.1}$$

Here, the bandwidth is set to 400MHz and the SNDR is set to 70dB. To achieve 172 FoM, the power dissipation of the ADC should be 12.7mW. In the following sections, a detailed analysis of power dissipation breakdown is explained. Whereafter an error-budget is made to distribute the noise sources and check their feasibility.

5.1. Power approximation

The power consumption of the residue amplifier consumes a significant amount of the total power consumption, some even more than 50% of the total power consumption of an ADC [5], [6], [32], [33], [34]. However, it is not straight forward to estimate the power consumption of an amplifier. Therefore, the power approximation is limited to the DAC, coarse ADC and the back end ADC. In Section 5.4.1, a power optimization is done with regard to the power available for the amplifier. For the power approximation there are a few components, which power consumption are known or can relatively easily be approximated. For further study, the DAC and reference voltage presented [1] are adopted. Therefore, it is assumed that the power dissipation of the DAC does not scale. Hence, the power consumption from the SAR assisted CT $\Delta\Sigma$ ADC [1] can be used, which is 777μW. Next to this, the coarse ADC and the back end ADC are based on the coarse SAR ADC of the SAR assisted CT $\Delta\Sigma$ ADC [1]. However, the SAR ADC scales with frequency and the amount of resolved bits. Therefore, a more elaborate examination is done in the next section.

5.1.1. Power approximation: SAR ADC

The power consumption of the coarse ADC and the back end ADC are the main components that consume a different amount of power depending on the amount of bits resolved and the sampling frequency. The paper [14] explains the SAR ADC and contains an overview of its

power distribution. The power in a SAR ADC is mainly from the comparator, clock and the switching of the capacitor bank. Hence, an estimation for different amount of resolved bits can be expressed as:

$$P_{diss} = \frac{1}{2} f_s C_l V_{supply}^2 \tag{5.2}$$

The unit capacitance that is used is 0.7fF [14]. From a standard SAR ADC design and [14], the total load capacitance for different amount of resolved bits can be expressed as:

$$C_{load,N} = 2C_{N-1} + C_{unit} \tag{5.3}$$

This approach is verified with circuit level simulations in Cadence©. Furthermore, it is assumed that for total the power consumption of the SAR ADC, the comparator and the clock do not scale with the sampling frequency and load capacitance. The power consumption for a 5 bit SAR ADC is known and by applying the ratio's of Equations 5.2 and 5.3 the power of the SAR ADC can be approximated. The sampling frequency can be estimated by the time needed per conversion, this can be read from a table in the paper [14]. At last, the power consumption of the SAR ADC can be reduced by optimising the current design, which is a matter of time spent on the design. The results are given in Table 5.1.

Amount of bits SAR ADC	**Sampling frequency**	**Load capacitance**	**Power w/o comp & clock**	**Total power**
Unit	**GHz**	**fF**	**mW**	
1b	10.0	0.7	0.18	0.57
2b	5.0	2.1	0.28	0.67
3b	3.33	4.9	0.43	0.78
4b	2.50	10.5	0.69	1.08
5b	2.0	21.7	1.15	1.54
6b	1.66	44.1	1.96	2.35
7b	1.43	88.9	3.39	3.78
8b	1.25	178.5	5.95	6.34
9b	1.11	357.7	10.53	10.92

Table 5.1: Estimation power consumption SAR ADC

Table 5.1 shows that for a lower amount of converted bits the sampling frequency can be higher. Moreover, the power consumption decreases too. Both can be reasoned with Equation 5.2 and the fact that the load capacitance does not scale linear.

5.2. Error budget

In order to obtain a DR of 70dB, the error sources must be modelled. The main error sources are quantization, thermal, jitter and digital mismatch. To visualize the noise sources, an example is given for a three-stage architecture. Therefore, the dominant noise sources can be it can be seen in Table 5.1. The flicker noise of the amplifier is not taken into account, since it is assumed that in a later phase of the system design, the amplifier is chopped.

To achieve the DR, the error sources and their budgets are given in Table 5.2. The AAF is not taken into account as a noise source, because the AAF is implemented off chip, see Figure 5.1.

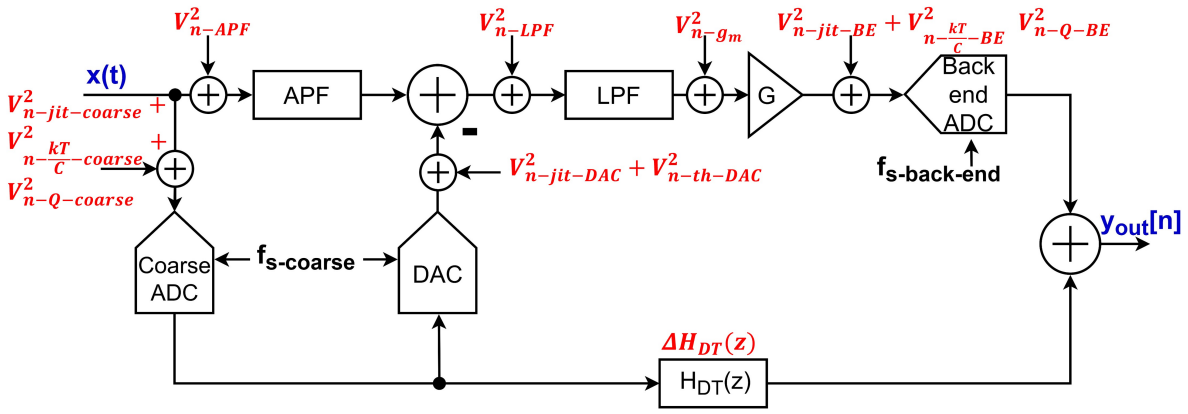

Figure 5.1: The main noise sources for a two-stage architecture

Error source	SNR [dB]
Quantization	77
Thermal	74
Jitter	77
Digital mismatch	+ 77
Dynamic range	70

Table 5.2: Error budget

5.3. Two-stage design

From the previous Section 5.2 it is clear that a SQNR of 77dB is needed to obtain the DR. With the SQNR Equation 3.11, the needed back end ADC can be determined. From Section 4.4 it is known that an inter-stage gain of 19.6dB can be achieved. This leaves $77 - 19.6 = 57.4$ dB for the back end ADC. As a result, the back end ADC would at have to resolve:

$$(57.4 - 1.76 - 10log_{10}(1.11/0.8))/6.02 = 9bits$$

This calculation makes it clear that 9 bits must be resolved in the back end stage. The power consumption of a 9 bit SAR ADC, is 10.9mW, see Table 5.1. After adding the DAC power consumption, it is 11.7mW, and the power budget is 12.7mW. Hence, there is 1mW available for the amplifier, which results in a power budget of approximately 8% of the total power. Literature shows that a power budget of at least 25% of the total power is needed [5], [6], [32], [33], [34]. Therefore, the power for the amplifier will not be sufficient. Moreover, the maximum in-band gain for a 5 bit coarse ADC is 29.8dB, whereas only 19.6dB can be applied. Therefore, the 5 bit resolution is not used efficiently. The large gain degradation is due to the large latency that must be compensated, as well as to the sensitivity of a 5 bit coarse ADC to phase mismatch. All in all, for the given APF, the two-stage architecture is an inefficient solution for a bandwidth of 400MHz. A much more complex APF can be designed, for example a 6^{th} order. However, the implementation will be very challenging, therefore, this direction is not pursued. If the APF provides an accurate latency compensation, the inter-stage gain of 29.8dB can be applied, which decreases the amount of bits resolved by the back end ADC to 8. As a result, the amplifier can dissipate 5.6mW, 44%. On top of this, to reach an SQNR of 77dB, the gain of the amplifier must be 25.1dB. Consequently, the gain can be backed off by 4.7dB. Therefore, it can be concluded that the APF is limiting the performance of the system. To alleviate the APF from the demanding requirements, the total latency must be smaller. Consequently, a

coarse ADC that resolves fewer bits should be investigated. This is done in the next Section 5.4.

5.4. Multi-stage design

To clarify a single-stage design, the definition of a single-stage is given in Figure 4.5. In order to achieve the SQNR, Section 3.2 shows that, either the back end must resolve more bits or the inter-stage gain must be increased. In a multistage design, a larger total inter-stage gain can be achieved, because the gain is divided into multiple stages. As a result, the SQNR Equation 3.11 does not hold anymore. The added stages amplify the residue signals. Hence, these inter-stage gains are added to a larger total gain. The SQNR of the multi-stage pipeline converter can be expressed as:

$$SQNR_{dB} = 6.02B_{BE} + 1.76 + 10log_{10}(\frac{f_{s,BE}}{2BW_{sig}}) + \sum_{i=1}^{N-1} G_{inter-stage} \tag{5.4}$$

Here B_{BE} is the number of bits resolved in the back end stage and $f_{s,BE}$ is the sampling rate of the back end SAR ADC. N is the amount of stages, and the inter-stage gain ($G_{inter-stage}$) is the gain applied in each stage. On the one hand, the smaller applied gain means a lower power consumption of the amplifier. On the other hand, the addition of a stage means a higher power consumption. As a consequence, there is an optimum, which is investigated in the next section.

5.4.1. Power optimization

The power consumption of amplifiers in pipelined architectures have a significant power consumption [5], [6], [32], [33], [34]. On top of this, the approximation of the power consumption of an amplifier is not easily done. Hence, the power budget optimization of multi-stage architectures is done with regard to the power conserved for the amplifier.

In Chapter 4, the benefits of less amount of bits in a stage are discussed, such as a reduced phase mismatch sensitivity. Combining this, together with the increased sampling rate that can be reached (see Table 5.1), this results in a smaller latency and thereby causes a relaxed APF design. As a consequence, the proposed architectures are based on a smaller inter-stage gain. In other words, a smaller inter-stage gain translates to less amount of bits resolved in the front end stages. This causes a smaller latency, an improved phase mismatch sensitivity. A 4 bit coarse ADC, allows a maximum gain of 23.5dB. However, the phase mismatch leads to 4dB of gain cutback, see Figure 4.14. Hence, this makes the coarse ADC relatively inefficient compared to its maximum gain. On top of this, the 4 bit coarse ADC has a sampling frequency of 2.5GHz, which makes the total latency just 25ps less than the evaluated coarse ADC. It is assumed that this slight improvement is not enough to give a considerable improvement in the terms of applicable gain. Furthermore, the 4 bit coarse ADC is sensitive to the phase mismatch, this is less for the 2 and 3 bit cases. If a 1 bit coarse ADC is used, a lot of stages are needed and the components in the stages (DAC and coarse ADCs) will dominate the power consumption. Therefore, only 2 bit and 3 bit coarse ADCs are investigated. The underlying SQNR calculation is discussed in Section 5.2. Furthermore, the calculation of the proposed architectures is based on the power consumptions mentioned in Section 5.4.1. In addition, the amplifier of the first stage is given a twice as large power budget, because the amplifier of the first stage has the most stringent noise, distortion and mismatch requirements, see Table 5.3. At last, to cope with the noise sources and other non-idealities, such as component variability, a gain redundancy of 2dB is used.

Amount of stages	Bits resolved per stage	DAC	Coarse ADC	Back end ADC	Total power w/o amplifiers	Total power for amplifiers	Power breakdown amplifier (2-1-...)	Gain per amplifier
Unit	Bits				mW			dB
3	3-3-7	1.6	1.6	3.8	6.9	5.8	3.9-1.9	15.7
	3-3-8	1.6	1.6	6.3	10.2	2.5	1.6-0.8	12.6
4	3-3-3-5	2.3	2.3	1.5	6.2	6.5	3.2-1.6-1.6	13.8
	3-3-3-6	2.3	2.3	2.4	7.0	5.7	2.8-1.4-1.4	12.0
	2-2-2-7	2.3	2.0	3.8	8.1	4.6	2.3-1.2-1.2	10.2
5	2-2-2-2-4	3.1	2.6	1.1	6.8	5.9	2.3-1.2-1.2-1.2	11.6
	2-2-2-2-6	3.1	2.6	2.4	8.1	4.6	1.8-0.9-0.9-0.9	9.1

Table 5.3: Power breakdown for the architectures

Table 5.3 shows, that the power per amplifier increases for a lower gain. The three-stage architecture (3-3-7) has a gain redundancy of just 1.6dB, which is not enough. The same holds for the four-stage architecture (2-2-2-7) and the five-stage (2-2-2-2-4) architecture. Moreover, the gain per amplifier in Table 5.3 is the theoretically needed gain. The feasibility of this gain is not investigated yet. This is done in Section 5.4.3.

All in all, in order to achieve more power for the amplifier, the system needs more stages. The pro's and cons are discussed in Chapter 4, but the influence on the error sources need to be examined, these are investigated next.

5.4.2. Error sources investigation

The error budget for all the noise sources is known, but the feasibility of all the sources must be examined. This is done in the next sections.

5.4.2.1. Quantization noise

The quantization noise is one of the main components in the noise model. The quantization noise must be designed for a SQNR of 77dB. This can be modelled with Equation 5.4. The reviewed architectures must fulfil the 77dB of SQNR requirement, which is done with a combination of the inter-stage gain and the resolution of the back end. As an example, the four-stage architecture with a 3 bit coarse ADC and a 6 bit back end ADC. From Table 5.1 the back end sampling rate can be obtained. Filling this into Equation 5.4, gives

$$SQNR_{dB} = 6.02 \cdot 6 + 1.76 + 10log_{10}(\frac{1.66}{0.8}) + \sum_{i=1}^{3} G_{inter-stage} \tag{5.5}$$

The SQNR is equal to 77dB, hence the inter-stage gain can be calculated with,

$$77 = 41.05 + \sum_{i=1}^{3} G_{inter-stage} \rightarrow G_{inter-stage} = 12dB \tag{5.6}$$

This procedure is used for all the other architecture calculations.

5.4.2.2. Thermal noise

To have a rough idea of the thermal noise sources in the system, the most dominant noise sources are monitored. Figure 5.1 shows the dominant thermal noise sources. The noise is calculated referred to the input. The kT/C noise of the back end stage is attenuated by the gain of the first stage. Therefore, the noise of the first stage is dominant and the thermal noise of the back end stage can be neglected. Moreover, some of the "regular" thermal noise sources can be neglected, such as the kT/C noise of the coarse ADC. An intuitive explanation for it is that, on a system level, this noise source has the same origin as the quantization noise of the front end stage. The quantization noise of the front end is cancelled at the output, since this sampling noise has the exact same path to the output. This too will be cancelled. The

remaining thermal noise sources are the following:, the thermal noise of the APF, DAC, LPF and the amplifier has g_m noise, see Figure 5.1. Furthermore, the thermal noise sources of the other stages are neglected, because the amplifier will reduce their noise contribution by its gain. The thermal noise requirement is set to 74dB.

5.4.2.3. Jitter noise

Jitter is an unavoidable artifact that occurs in discrete time systems. The jitter performance for a certain implementation can only be improved by using an improved PLL. As jitter is a time related error source, it should not be a surprise that for larger bandwidths, jitter could limit the performance of the system [2]. Overall, there are two main jitter sources, the sample and hold jitter and the jitter in the DAC. The sample and hold jitter of the coarse ADC is cancelled, because it has the same place of origin as the quantization error. However, the sample and hold jitter of the back end ADC is not cancelled, but it is attenuated by the gain of the front end and can be neglected. Therefore, the impact of the DAC jitter must be monitored carefully. Furthermore, the PLL has a rms jitter of 100fs.

The DAC jitter originates in the DAC and is not fed through the digital back end in the same stage, see Figure 5.1. Hence, it is not cancelled. The impact of this jitter is unknown. Therefore, a model in MATLAB© makes a first order approximation of the jitter. Figure 5.2 and Table 5.4 show the results of the approximation.

Jitter specification	**Coarse ADC**		**Unit**
	2 bit	3 bit	
SJNR (77 dB)	0.13	0.17	ps
Minimum rms jitter (100fs)	78.1	79.4	dB

Table 5.4: Coarse ADC and jitter requirement

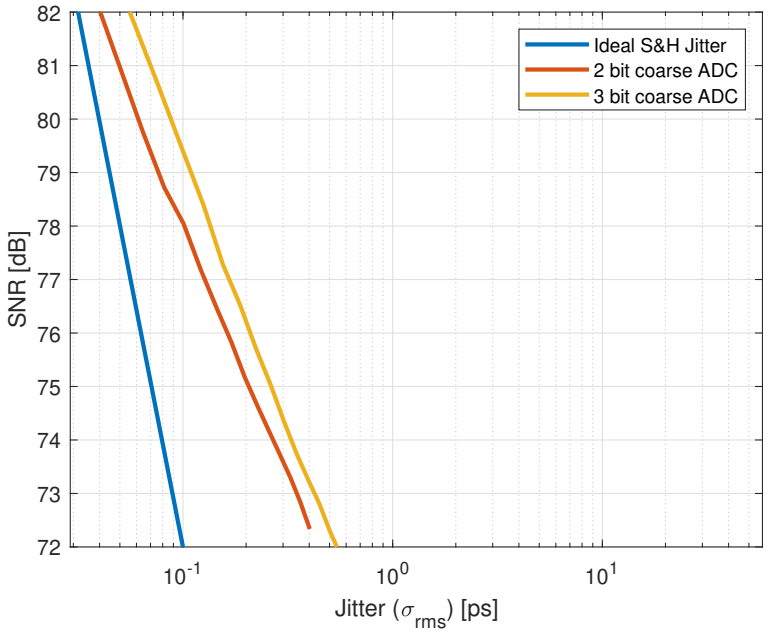

Figure 5.2: DAC jitter for the 2 bit versus 3 bit coarse ADC

Furthermore, the first stage has the most impact on the overall jitter performance, as can be seen in Figure, 5.3. With this rms jitter the specification of the error budget is achieved. Therefore, the DAC jitter is not investigated any further. Note that a limitation of this analysis is that the exact impact of the jitter on architectures with different amount of stages is not quantified. Nevertheless, it can be seen that the amount of stages has a minor impact on the jitter.

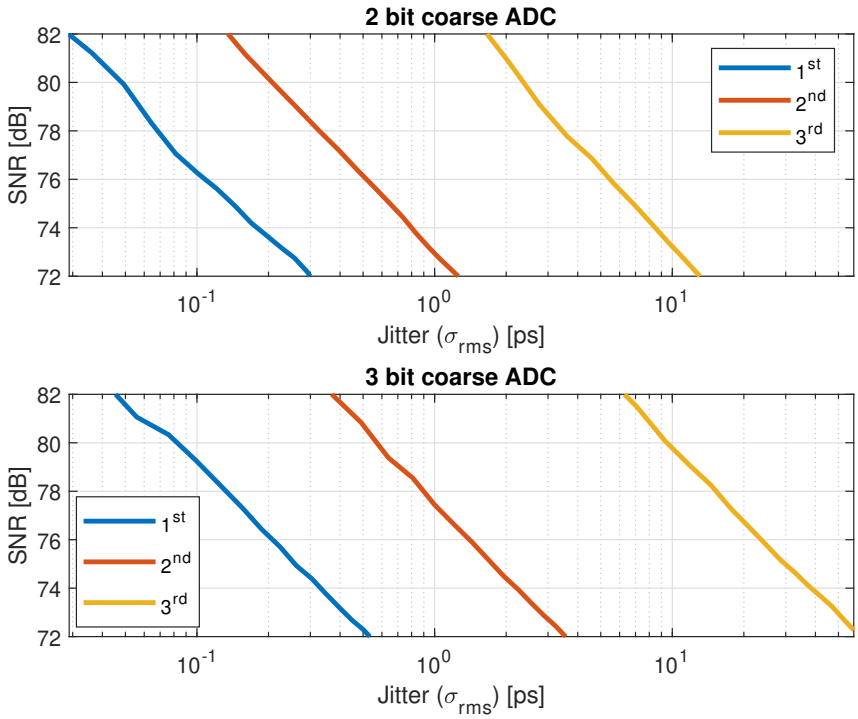

Figure 5.3: DAC jitter of the four-stage architecture, 2 bit versus 3 bit coarse ADC for the different stages

5.4.2.4. Digital mismatch

The noise sources that originate in the coarse ADC, such as the sample and hold jitter, the kT/C noise and the quantization noise cancel at the output of the system. However, the noise cancellation of the coarse stage is based on the digital back end matching exactly to the analog path. If there is a mismatch (ΔH_{DT}) between the digital back end and the analog path, the noise sources will leak to the output. Resulting in a decreased SNR, thus the digital mismatch can be seen as noise leaking at the output.

If the digital back end can mimic the analog path good enough ($\geq$ 77dB), this noise cancellation works. However, it is not straightforward to imitate an analog circuit with a digital one. For instance, the PVT variations too must align and overall digital circuits tend to cope much better with PVT variations than analog circuitry. Consequently, this must be modelled into the digital circuitry in such a way that transfer functions from the coarse ADC to the output of the system output align. A transfer function basically consists of two components, the magnitude response and the phase response, where the phase response can be seen as a time response. Therefore, the digital mismatch is characterized in two components: the gain mismatch and the time mismatch. For both mismatches, a MATLAB© model is created. In this model the back end ADC is removed, and the analog path is summed with the digital path, so that the back end has an infinite resolution. Now, the error can be modelled very accurately.

The results are given in Figures 5.4, 5.5, 5.6, 5.7 and Table 5.5.

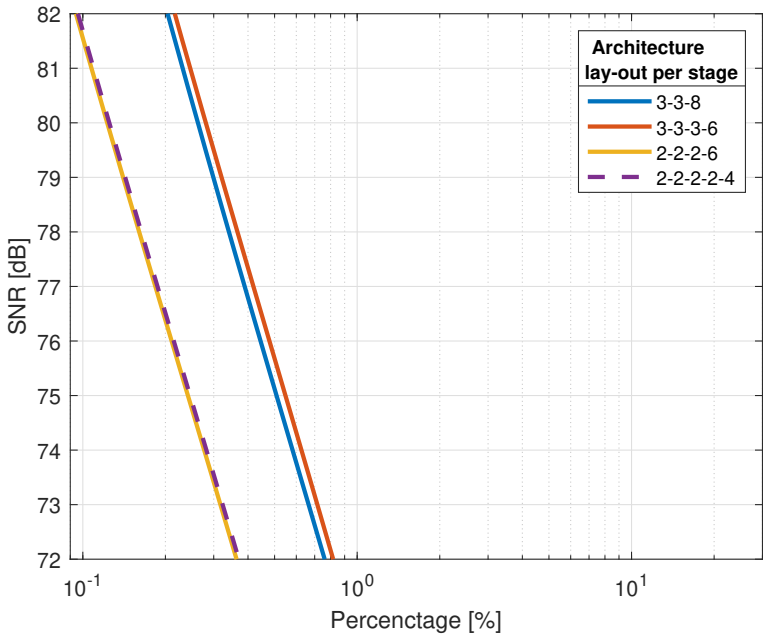

Figure 5.4: Gain mismatch for the architectures

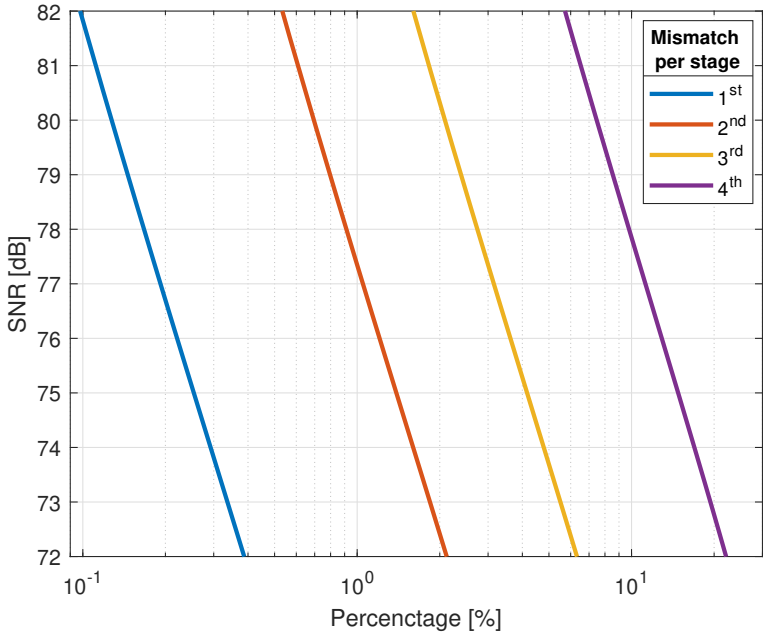

Figure 5.5: Gain mismatch for the five-stage architecture, with 2 bit coarse ADCs

From Figure 5.4 it can be concluded that the 2 bit coarse ADC puts a more stringent requirement on the digital gain mismatch than the 3 bit coarse ADCs. This is substantiated by the quantization error, which is smaller for a 3 bit ADC than for a 2 bit ADC. As a result, the total error leakage is smaller for a certain gain mismatch. Furthermore, Figure 5.4 shows that the amount of stages does not determine the digital mismatch requirement, but the amount of

bits resolved in the coarse ADC does. For a better understanding, the five-stage architecture with 2 bit coarse ADCs is examined. The digital mismatch of each stage is reviewed separately. The result is given in Figure 5.5, which shows that the stage at the front (the first stage) dominates the gain mismatch.

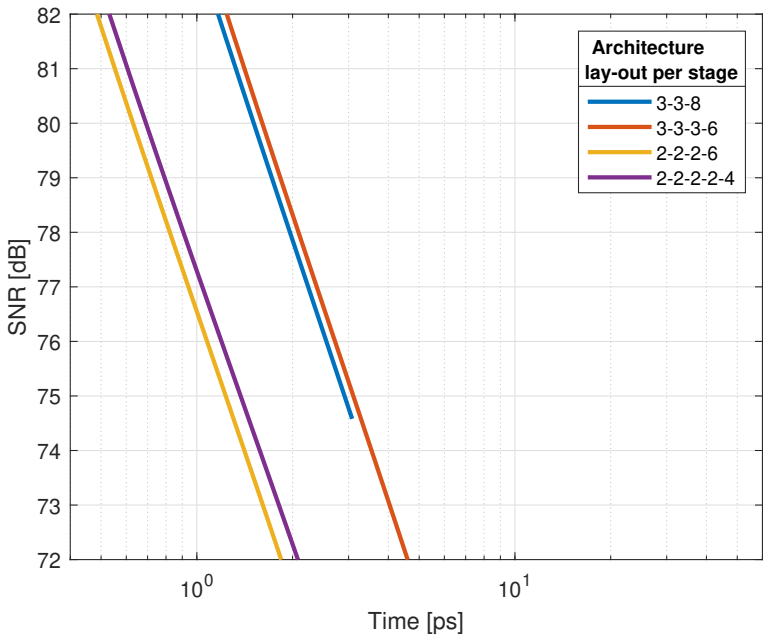

Figure 5.6: Time mismatch for the architectures

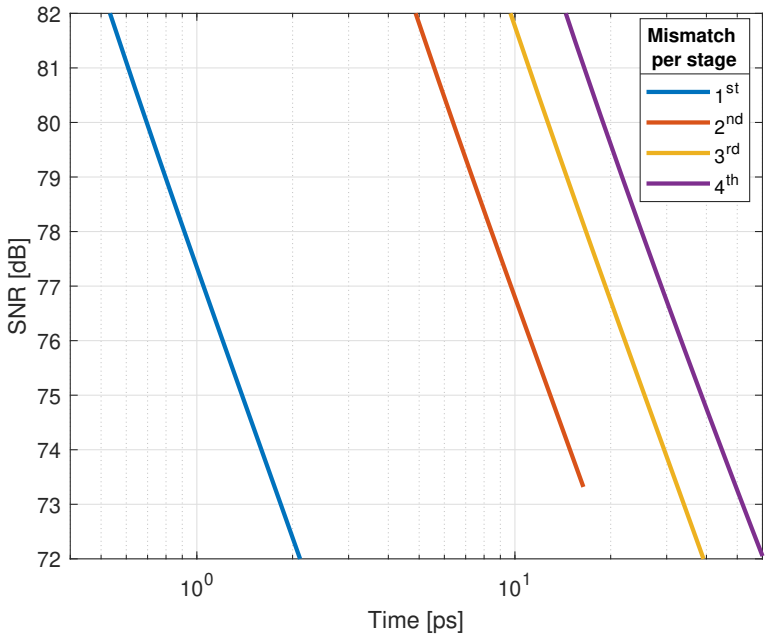

Figure 5.7: Time mismatch for the five-stage architecture, with 2 bit coarse ADCs

The digital time mismatch, which is given in Figure 5.6, conveys the same conclusion as

the conclusion for the gain mismatch.

Coarse ADC bits	Mismatch	
	Gain [%]	Time [ps]
2	0.123	0.63
3	0.263	1.61

Table 5.5: Gain and time error for the digital mismatch requirement of 77dB

The feasibility of the digital mismatches are out of the scope of this thesis. Nevertheless, the gain mismatch is feasible, because this results in the amount of power spent in the amplifier. The time requirement on the other hand could be more stringent. However, there are already systems that can reach such specifications [35], [36].

5.4.3. Proposed architecture

The foregoing analyses show pros and cons for each system architecture. However, the feasibility of the applicable gain after the LPF is not investigated. The applicable gain for the most promising architectures from Table 5.3 is reviewed next. Whereafter, the 2 bit coarse ADC versus the 3 bit coarse ADC are summarized. At last, an architecture is chosen.

For the architectures, it is assumed that the PLL can only give a clock signal which produces sampling rates that are integer multiples of each other. For example, a 6 bit back end ADC that operate on a calculated sampling frequency of 1.66GHz, is assumed to operate on 1.6GHz. Hence, the coarse ADC must operate either on 3.2GHz or on 4.8GHz. The exact coarse and back end ADC sampling rates are given in Table 5.6. The performance of the most promising architectures of Table 5.3 are listed in Table 5.6.

Amount of stages	Bits resolved per stage	Front end $f_{s-coarse}$	Back end $f_{s-back-end}$	Theoretically needed gain	Simulated gain	Gain back off	Power breakdown amplifier (2-1-...)
Unit	Bits	GHz		dB			mW
3	3-3-8	3.3	1.1	12.8	14.3	1.5	1.6-0.8
4	3-3-3-5	3.4	1.7	14.0	12.7	-	3.2-1.6-1.6
	3-3-3-6	3.2	1.6	12.0	10.4	-	2.8-1.4-1.4
5	2-2-2-2-6	4.8	1.6	9.1	11.1	2	1.8-0.9-0.9-0.9

Table 5.6: Resulting proposed architectures

Table 5.6 shows that only the 2-2-2-2-6 architecture complies with the 2dB gain back off. The 3-3-8 architecture is only 1.5 dB off from the specification. These gains are verified by Figures 5.8, 5.9.

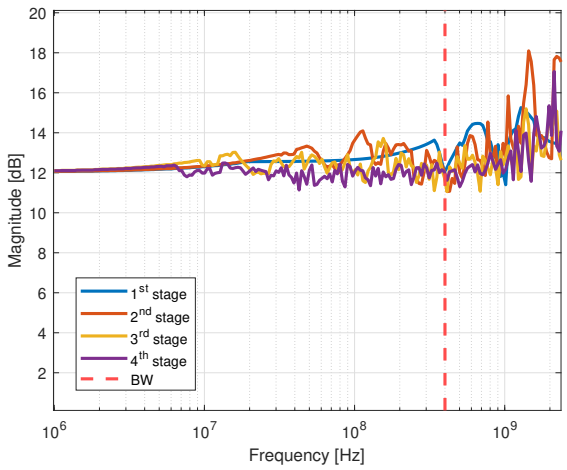

Figure 5.8: Applicable gain after the LPF for the 2-2-2-2-6 architecture

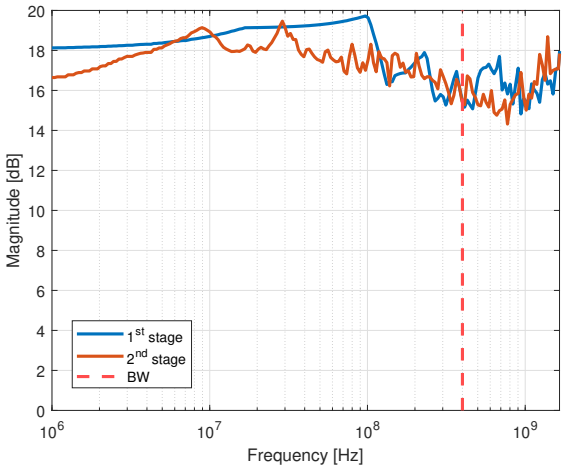

Figure 5.9: Applicable gain after the LPF for the 3-3-8 architecture

From the error source investigation in Section 5.4.2 and Chapter 4. The main advantages of the 2 bit and 3 bit coarse ADCs are summarized. The 2 bit coarse ADC benefits from a smaller latency, due to the larger sampling rate. This has the advantage of a more accurate latency compensation. This, combined with the reduced sensitivity to the phase mismatch, enables the 2 bit coarse ADC to apply a relatively large gain. The applicable gain is only 1dB below the maximum gain, whereas for the 3 bit coarse ADC, this reduction is 3.8dB. Hence, for a 2 bit coarse ADC, the gain can be applied more efficiently than for a 3 bit coarse ADC. The main advantages of the 3 bit coarse ADC over the 2 bit coarse ADC are the relaxed digital mismatches and the jitter performance.

As a side note, if a Butterworth filter is applied to the architectures with a 3 bit coarse ADC, the four-stage architectures become interesting, because a simulated applicable of 15.9dB can be achieved. Hence, the 2dB of back-off is easily reached. The 2-2-2-2-6 architecture with 2^{nd} order APFs and Butterworth filters as LPF can also reach the same specifications. Thus, there is a trade-off between the filter complexity of the APF or the LPF. However, the implementation with the Butterworth filters are out of the scope of the thesis.

All in all, the performance of the amplifier of the 3-3-8 architecture lacks compared to the 2-2-2-2-6 architecture. The 3-3-8 architecture has a smaller gain back off and the power reserved for the amplifiers is smaller. Moreover, the 2 bit coarse ADC has a more relaxed APF network than the 3 bit coarse ADC. The relaxed noise requirements do not compensate for the disadvantages. Consequently, the 2-2-2-2-6 architecture is the best choice. For the system architecture, see Figure 5.10.

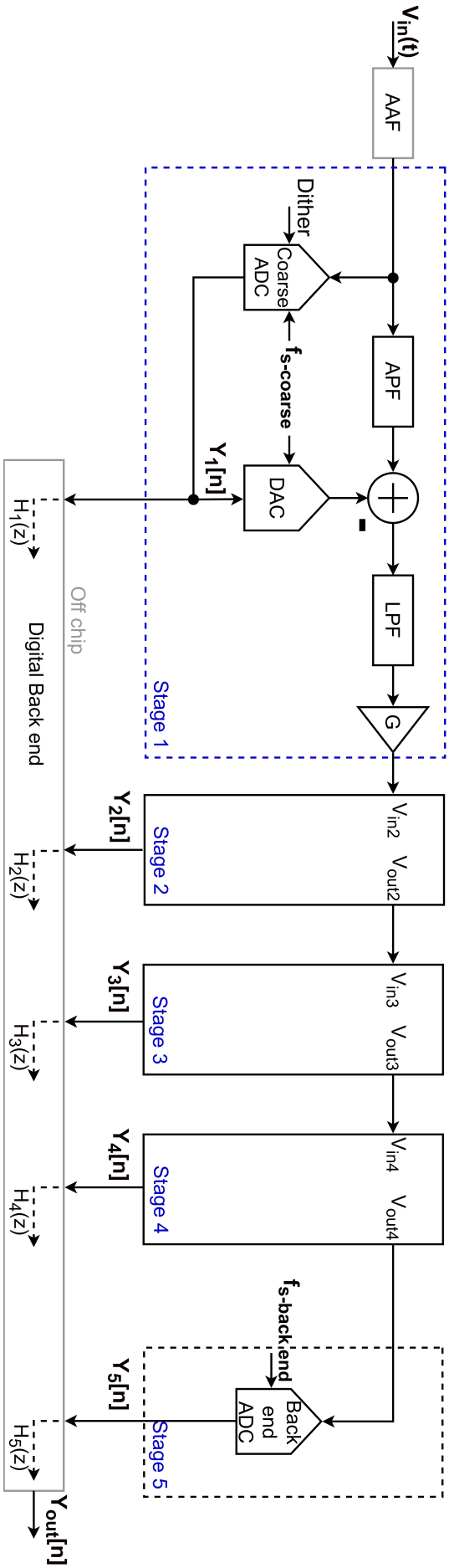

Figure 5.10: System architecture

5.5. Proposed system requirements

The ADC is made for the automotive industry, which brings more requirements with it apart from the ones derived in the previous Chapter 4. Such as the harmonic distortion (HDx) and the spurious free dynamic range (SFDR) specification. The other specifications are given in the previous sections, and are summarized in Table 5.7. First, the HDx specification must be taken care of in the design of the components. It is assumed that the front end has the most impact on the distortion and more specifically, the DAC and the amplifier. The design of the DAC is out of the scope of this thesis, but the design of the amplifier is investigated in Chapter 6. Second, the SFDR specification is important and a brief validation for this specification is given in Section 5.6.1. Next to the system requirements, the amplifier requirements are important. This chapter has given an optimization for the amplifier power consumption. However, the exact specifications of the amplifier are not given yet. The amplifier requirements are merged with the specifications of the APF and LPF, because the APF and LPF implementation are dependent on the implementation of the amplifier. Hence, it is called the filter requirement. The filter requirements are listed in Table 5.8. These requirements are explained next.

For the filter specifications, it is assumed that it has the same specifications as the system specifications, because it is at the input of the architecture. Hence, all the non idealities, such as distortion and noise sources, will directly impact the performance of the system. Furthermore, dither will be applied to the coarse ADC, which relaxes the linearity of the amplifier. However, the dither is applied in a later phase of the design. The dither is applied to reduce the tonal output spectrum of the ADC, thus also the DAC and the residue signal. This will relax the linearity requirements of the amplifier, but this is out of the scope of this thesis. Note that the noise specification of the filters is equal to the system specification. This is done because the thermal noise sources mainly originate from the front end filters (APF and LPF) and from the R-DAC. However, the resistors of the R-DAC must be scaled to the APF resistance, therefore the DAC resistors are incorporated with the filters.

The requirements of the filters, the ADCs and the DAC are given in Tables 5.9 and 5.10.

System specification	Unit	Budget
Technology	nm	28
Power	mW	12.7
$P_{n,in}$	nV^2	16.1
HDx	dBc	70
SFDR	dBc	104
Jitter	ps	0.13
Digital gain mismatch	dB	-58.2
Digital time mismatch	ps	0.63
Dynamic range	dB	70

Table 5.7: System specifications

Specification	Unit	Budget
Current	mA	2.1
$P_{n,in}$	nV^2	16.1
Gain	dB	9.1
HDx	dBc	70
SFDR	dBc	104
Gain mismatch	dB	-58.2

Table 5.8: The filter requirements of the five-stage (2-2-2-2-6) architecture

Requirements	AAF	APF	LPF
Type	Chebyshev	All-pass	Regular low-pass
Order	2^{nd}	4^{th}	2^{nd}
Pole [GHz]	$0.8e^{2.3i}$,$0.8e^{-2.3i}$	2.0, 2.0	1.3, 1.3
Zero [GHz]	-	2.0, 2.0	-

Table 5.9: The filter transfer function requirements of the five-stage (2-2-2-2-6) architecture

Requirements	Coarse ADC	Back end ADC	DAC
Type	SAR	SAR	R-DAC
Bits	2	6	2
Power [mW]	0.67	2.35	0.77

Table 5.10: The ADC and DAC requirements of the five-stage (2-2-2-2-6) architecture

5.6. System verification

To verify the feasibility of the requirements of the system. An estimation of the SFDR specification is calculated. Whereafter the MATLAB© model is verified by a Cadence© implementation. Note that a limitation of the previous error analysis is that not all the errors are added simultaneously. However, it is assumed that this will not pose a problem, because the quantization error of the first coarse ADC can be expressed by:

$$P_{n,Q,coarse} = \frac{\Delta^2}{12}\frac{f_{s-coarse}}{2BW} \tag{5.7}$$

The input signal power is known, hence the SQNR of the first front end stage can be expressed by:

$$SQNR_{coarse-ADC} = 10log_{10}(\frac{P_{signal}}{(\frac{\Delta^2}{12}\frac{f_{s-coarse}}{2BW})}) \tag{5.8}$$

Filling in the variables, results in a SQNR of 21.6dB. Comparing the magnitude of the SQNR of the front end ADC with the thermal noise and sample and hold jitter. The sample and hold jitter is obtained from Figure 5.2, which is approximately 72dB. The thermal noise of the capacitor bank of the SAR ADC can be expressed as:

$$SNR_{kT/C} = 10log_{10}(\frac{P_{signal}}{kT/C}) \tag{5.9}$$

Assume room temperature (T = 300K), k is the Boltzmann constant and the total capacitance can be read from Table 5.1. This results in a SNR of 53.1dB. Consequently, it can be stated that the other error sources that leak to the output have a negligible contribution to the total noise leaked to the output due to the digital mismatches. Nevertheless, a limitation of the preceding analyses is the combined impact of the quantization error, DAC jitter, digital mismatch and the thermal noise on the system.

5.6.1. SFDR validation

In the automotive industry, the spurious free dynamic range (SFDR) is an important requirement. The SFDR definition deviates from the usual definition. The SFDR is defined by the highest tone in the signal-band that is not a harmonic tone of the input signal. For example, harmonic tones that are aliased back in-band, are not considered as harmonics, but are considered for the SFDR.
The specification of the SFDR is demanding (104dBc), thus it must be taken care of. Fortunately, it can quite easily be verified. For this, the assumption that the coarse ADC output has a white noise spectrum must hold. It is expected that the coarse ADC is dithered in a later phase of the design, which is out of the scope of this thesis. Nevertheless, applying dither to the first stage coarse ADC ensures the white noise spectrum. For now assume, the back end ideally quantizes the out of the first stage, hence the continuous time output and the digital output are summed, see Figure 5.11.

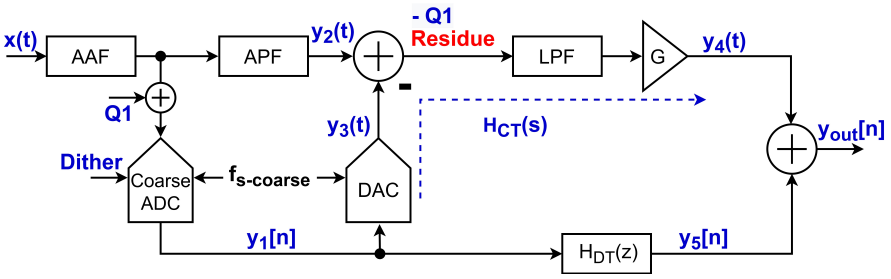

Figure 5.11: Front end stage with an ideal back end

As given by Equation 3.6, the noise power can be derived. The white noise spectrum, ensures that the quantization noise power is spread evenly over the bandwidth of zero to $f_{s-coarse}/2$. The power spectrum density (PSD) $[dB/Hz]$ of the leaked quantization can be calculated. The leaked quantization noise of the front end is equal to the quantization noise of the front end multiplied by the power of the gain mismatch of the continuous time path ($y_4[t]$) and the digital path ($y_5[n]$). This can be expressed as:

$$P_{n,Q,front-end} = \Delta G^2(\frac{\Delta^2}{12}\frac{f_{s-coarse}}{2BW})[dB/Hz] \tag{5.10}$$

Note that, it is assumed that the digital gain mismatch (ΔG) is mainly determined by the gain mismatch and is not due to the distortion of the amplifier. The signal power is known, thus the input referred SFDR can be calculated, which can be expressed by:

$$SFDR_{front-end} = \frac{P_{signal}}{\Delta G^2(\frac{\Delta^2}{12}\frac{f_{s-coarse}}{2BW})}[V^2/Hz] \tag{5.11}$$

where, P_{signal} is the power of the input signal and ΔG the gain mismatch requirement from Table 5.7. Filling in the parameters gives a SFDR of 166dBFS, thus this architecture inherently

makes sure that the SFDR is taken care of. Note that the low-pass filtering is not taken into account. The other noise sources are assumed to have a white noise spectrum. Therefore, the eventual result will improve. The back end quantization error is not yet taken into account, because the quantization noise of the back end does not influence the eventual result. In other words, the assumption of an ideal back end quantization holds, because the fourth stage has a spectrum with a white-noise-like spectrum. The back end ADC resolves 6 bits, which ensures a more spread quantization noise spectrum. Moreover, for a worst case scenario, where a full scale input signal is applied, shown in Figure 5.12, results in a largest tone of -51.6dBc. However, the largest in-band signal magnitude at the input of the back end ADC is -33dB. On top of this, the quantization noise of the back end is attenuated by the gain of the preceding stages.

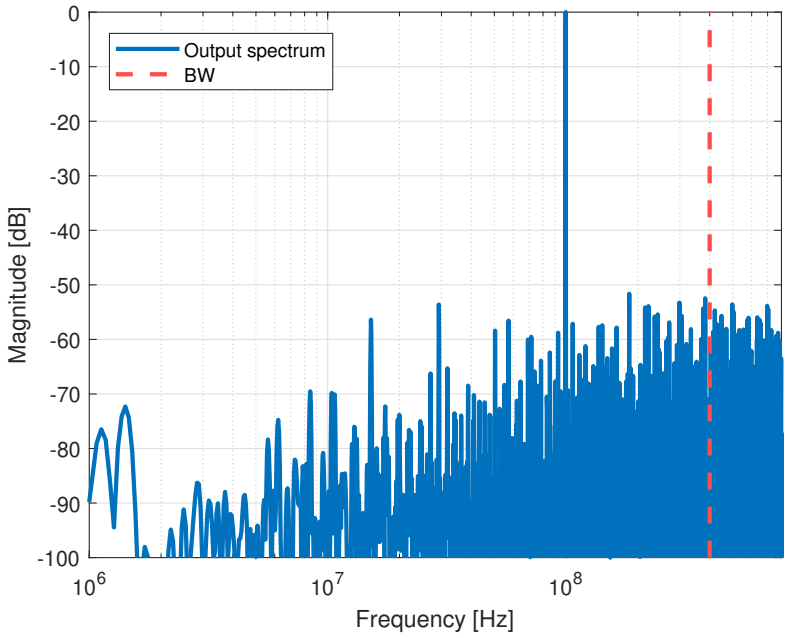

Figure 5.12: Output spectrum of the back end ADC for a full scale input signal

As a result, the largest tone due to the quantization noise of the back end ADC can be expressed by:

$$\begin{aligned} SFDR_{back-end} &= 9.1 \cdot 4 + 33 + 51.6 \ \ [dB/Hz] \\ SFDR_{back-end} &= 121 \ \ [dB/Hz] \end{aligned} \tag{5.12}$$

This outcome verifies that the SFDR specification is inherently satisfied by the architecture.

5.6.2. Verification of the system

To be able to verify the MATLAB© model with the Cadence© model, the implementation of the models must be identical. Therefore, as much as possible ideal blocks are used in Cadence©. The discrepancies between the models can be explained by the fact that components load each other, which is inevitable in a schematic implementation.
In MATLAB© the APF is implemented with a transfer function. However, in Cadence© such a transfer function block is very cumbersome. Therefore, the APF filter implemented in Cadence© is 2^{nd} order instead of the derived 4^{th} order APF, as there is no solution for the 4^{th} order APF

implementation. For the 2^{nd} order transfer function there is a solution from [37]. This APF network is implemented in Cadence©. This limits the applicable gain of 11dB to only in-band signals, which is shown by Figure 5.13.

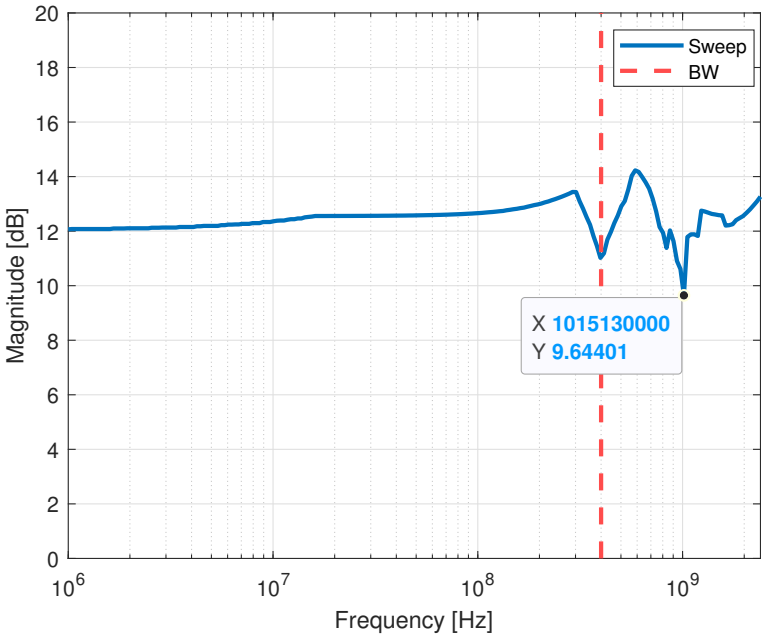

Figure 5.13: The applicable gain after the LPF verses frequency for the first-stage, for a 2^{nd} order APF

Nevertheless, Figure 5.13 shows, that the gain of 9.1dB can be applied over the entire bandwidth, even though, the gain cannot be applied together with the wanted error budget of 2dB. Furthermore, in MATLAB© the digital back end is implemented with transfer functions blocks and gain blocks. In Cadence© this is done with ideal OPAMPs and RC values. This too can cause slight discrepancies between the models.
The jitter and digital mismatch verification is out of the scope of the thesis, because the implementation of a jitter and digital mismatch in an analog environment is a challenge on its own.

To verify the model, the residue signal, the analog output of the first-stage ($y_4(t)$ in Figure 5.11), and the spectrum of the output ($y_{out}[n]$) are examined. The other intermediate signals are harder to judge, since they appear as pseudo-random signals. Figure 5.14 shows the residue signal of the first-stage. Both signals appear to be identical. Although the signal in Cadence© has a slightly less ideal form, which can be due to the fact that resistors and capacitors are used instead of the ideal transfer functions in MATLAB©. On top of this, the ideal OPAMPs in Cadence© have a large, but not infinite gain. The same conclusion can be drawn for the signal at the output of the first-stage, given in Figure 5.15.

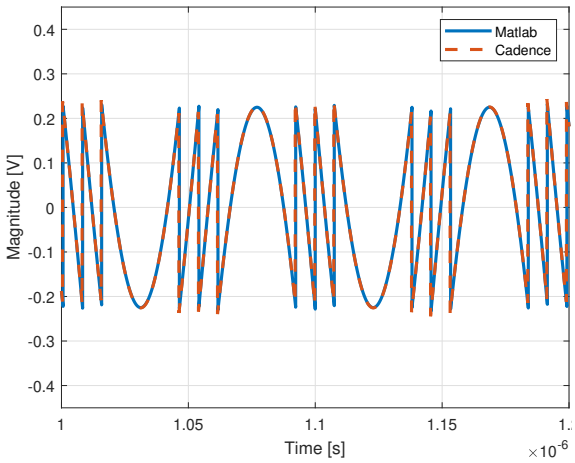

Figure 5.14: Residue signals, f_{in} = 11 MHz

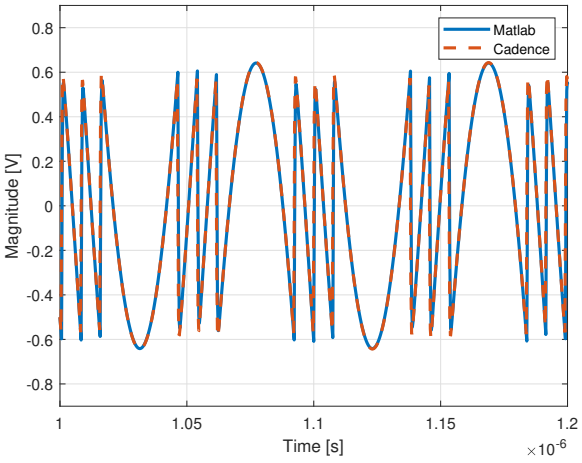

Figure 5.15: Residue signal after the gain and LPF, f_{in} = 11 MHz

At last, the output spectra of both models can be seen in Figures 5.16 and 5.17.

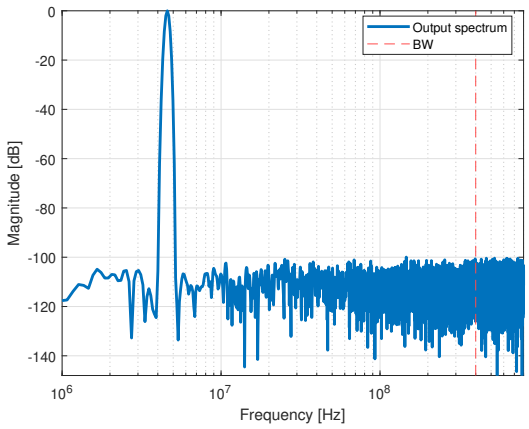

Figure 5.16: Output spectrum Cadence©, f_{in} = 5 MHz

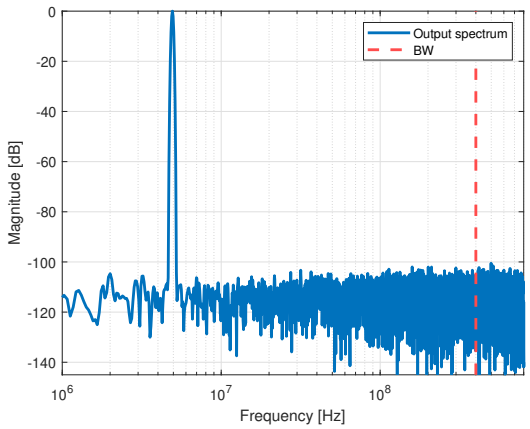

Figure 5.17: Output spectrum MATLAB©, f_{in} = 5 MHz

Figures 5.16 and 5.17 show a similar spectrum. However, the amount of points taken in the MATLAB© is larger than for the Cadence© simulation. This explains the wider input tone in Figure 5.16. Another discrepancy is the slight change in frequency. The MATLAB© has got multiple sampling rates, for which the coherent sampling function is adjusted accordingly. Note that the coarse ADC has no dither implemented, but due to the ideal blocks the tones are not visible in the spectrum.

To finish the comparison of the spectra, the SQNR is calculated. In both cases the SQNR is 77dB. All in all, the crucial aspects of the system are examined and it can be concluded that they match properly.

5.7. Conclusion

The two-stage design has a too small power budget for the amplifier, which is due to the lack of accuracy of the latency compensation from the APF. As a result, the two-stage architecture is an inefficient architecture for the bandwidth of 400MHz. To alleviate the APF from the demanding requirements, the coarse ADC must resolve fewer bits. As a result, the amount of

latency is reduced and the sensitivity to phase mismatch is smaller. In order to resolve fewer bits in the coarse ADC, other architecture configurations are considered. This optimization is focussed on reserving more power for the amplifier.

The rest of the analyses compares the 2 bit to the 3 bit coarse ADC. Before comparing the two, the analysis shows that the first stage is the most sensitive to the digital mismatch and the jitter requirements. Next to this, with a rms jitter of 100fs, it should not pose a problem in the design. However, it is seen that the 2 bit coarse ADC is more sensitive to jitter and digital mismatch than the 3 bit coarse ADC. Therefore, it can be concluded that the 3 bit coarse ADC relaxes the first stage in terms of digital mismatch and jitter performance. On the other hand, the reduced total latency and sensitivity to the phase mismatch enables the 2 bit coarse ADC to apply a relatively large gain. The five-stage (2-2-2-2-6) architecture has an applicable gain is only 1dB below the maximum gain, whereas for the 3 bit coarse ADC (3-3-8 architecture), this reduction is 3.8dB. Hence, a 2 bit coarse ADC the gain can be applied more efficiently than for a 3 bit coarse ADC. Furthermore, the increased sampling rate of the 2 bit coarse ADC causes a better out-of-band blocker immunity.

All in all, the performance of the APF of the 3-3-8 architecture lacks compared to the 2-2-2-2-6 architecture. Consequently, the 3-3-8 architecture has a smaller gain back off. Next to this, the power reserved for the amplifiers is smaller. Furthermore, the 2 bit coarse ADC has a more relaxed APF network than the 3 bit coarse ADC. The relaxed jitter requirement and digital leakage (mismatch) do not compensate for the disadvantages. As a result, the five-stage (2-2-2-2-6) architecture is chosen.

6

Filter implementation

The goal of this chapter is to compare the open loop APF and LPF filter implementation with a closed loop implementation. This chapter provides an implementation for both designs. Hereafter, a recommendation is given which implementation is most promising. In this chapter, the AAF is not taken into account, because it is implemented off chip. In order to give a fair comparison between the two implementations, both cases use an inverter as the active component. Furthermore, to limit the scope of the amplifier design2, the following assumptions are made: In a later phase of the design the amplifier will be chopped, therefore the flicker noise is not taken into account. Sophisticated CMFB, CMRR and PSRR are not considered. The calibration methods are out of the scope of this thesis. Examples of the calibration methods that should be applied are the calibration of components, gain, linearity, PVT variation.

6.1. Derivation of the LPF requirements

The LPF requirements are summarized in Tables 5.8 and 5.9. The magnitude response of the LPF has to be of 2^{nd} order with an attenuation of 0.75dB at 400MHz, see Figure 6.1. Table 5.8 sets the SNR to 74dB. It is assumed that only the first stage contributes to the noise. The main noise contributors can be divided into the APF, DAC and amplifier noise which is the g_m noise. The flicker noise of the transistors is not considered, because this is out of the scope of the thesis. Furthermore, for the design of the LPF the resistors and capacitors have a too large component spread to achieve the gain mismatch requirement. Therefore, it is inevitable to design the LPF without any calibration methods. The component mismatch and the calibration is out of the scope of this thesis. Nevertheless, it must be taken into consideration.

From Table 5.8 it can be seen that the HDx and SFDR specifications are 70 dBc and 104 dBc. For simplicity, the amplifier is optimized for the HDx and not for the SFDR. This can be done, because the SFDR depends on the HDx of the amplifier.

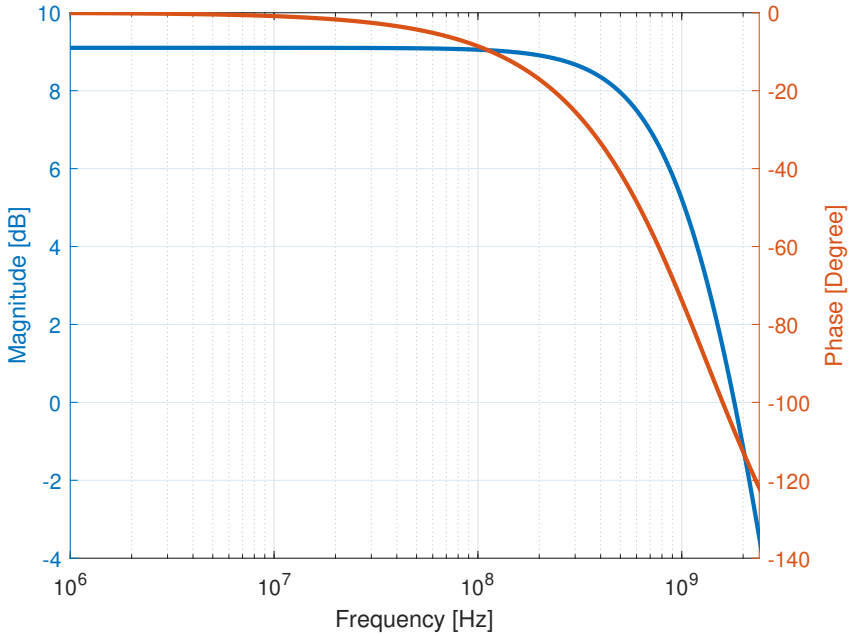

Figure 6.1: Transfer function of the required LPF, 0.75dB at 400MHz

The LPF amplifies the residue signal, which is a very tonal signal due to the presence of the quantization error. Therefore, the signal swing of the residue signal is not representative for a non-linearity optimization. To signify the distortion of the amplifier, the amplitude of the input frequency in the residue signal is needed. In order to know the amplitude of the input signal, the spectrum of the residue signal is consulted. The input signal magnitude can be read from Figures 6.2 and 6.3. Note that a rectangular window is used for the spectrum. Figures 6.2 and 6.3 show that for the closed loop implementation the amplitude is -18.1dB and for the open loop implementation it is -23.5dB. For both implementations it holds that, on the one hand, the small amplitudes relax the linearity requirements and on the other hand, the tonal behavior of the residue signal increases the HDx and the SFDR. These tones at the output of the LPF can mix with signals, which causes the tones popping up at unexpected frequencies. Another effect is that these tones can mix and fold on top of the harmonics. If the coarse ADC is dithered, these tones disappear, which relaxes the HDx and the SFDR. The HDx depends on the performance of the APF and on the amount of dithering that will be applied. The Section 4.2, shows that for an improved latency compensation, the residue signal contains a smaller magnitude of the input signal. As a result, the HDx and the SFDR requirement is relaxed for a better latency compensation. The first stage coarse ADC is dithered in a later phase of the design. This is out of the scope of this thesis. In other words, the tonal spectrum of the residue signal is still variable. Therefore, the HDx of the amplifier is not quantified in a schematic with the coarse ADC and DAC present, instead a simplified test bench is made. In the test bench a single input frequency is given with the magnitude as described before. The 3^{rd} harmonic and 5^{th} harmonic components are measured such that the HD_3 and the HD_5 are derived. It is assumed that the 7^{th}harmonic is negligible.

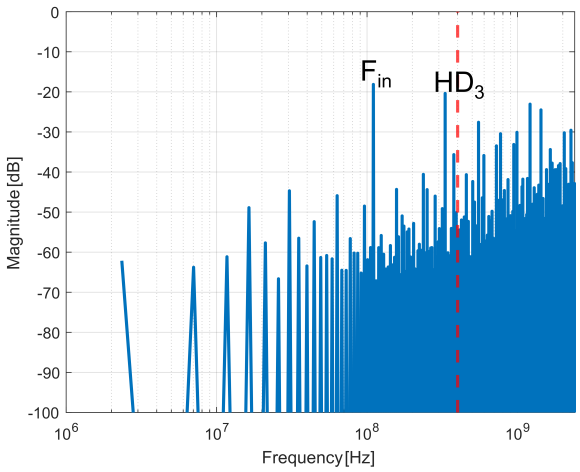

Figure 6.2: Spectrum of residue signal for the closed loop implementation, f_{in} = 110MHz

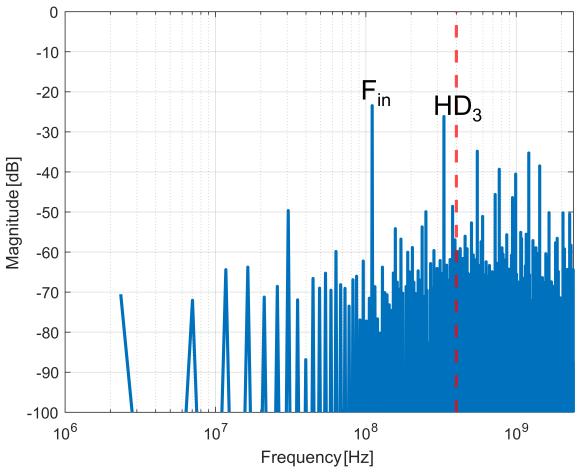

Figure 6.3: Spectrum of residue signal for the open loop implementation, f_{in} = 110MHz

6.2. Open loop implementation

An open loop implementation of the APF network is not designed before. Therefore, it is unknown if an APF network can be made with an open loop amplifier implementation. The scope of this chapter is to compare both implementations of the LPF. Hence, the APF is investigated, but not completely optimized. Further, the LPF realization and the APF filter implementation must be investigated first.

6.2.1. LPF realization

There are multiple possibilities to realize the 2^{nd} order low-pass filtering transfer function. The options are either two cascaded 1^{st} order LPFs, see Figure 6.4, or a single 2^{nd} order LPF, see Figure 6.5.

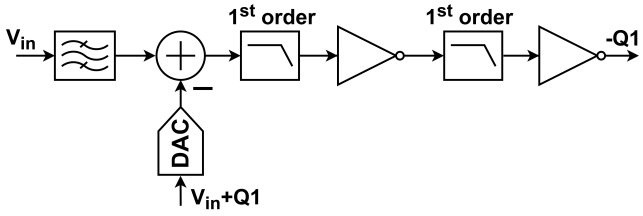

Figure 6.4: Open loop LPF implementation, with two cascaded LPFs

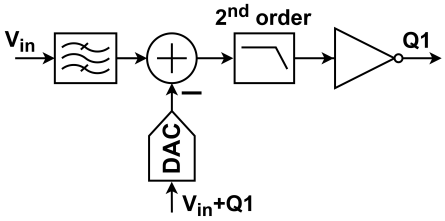

Figure 6.5: Open loop LPF implementation

The former is unwanted, because both LPFs contribute to the distortion. It is assumed that the distortion requirement is a limiting factor of the open loop implementation. The non-linearity of the first LPF is multiplied by the gain of the second LPF. Moreover, the harmonic components due to distortion of both amplifiers will mix and this increases the total non-linearity. Therefore, for each LPF, the non-linearity requirement is more stringent. Consequently, a single LPF is implemented. The 2^{nd} order low-pass filtering transfer function can be achieved by either increasing the circuit complexity at the output of the inverter or the APF circuit can incorporate a 1^{st} order filtering function. The latter is chosen, because the resistor implemented in the APF can be reused for the implementation of the LPF. Hence, it saves area and noise. The resulting implementation is given by Figure 6.6.

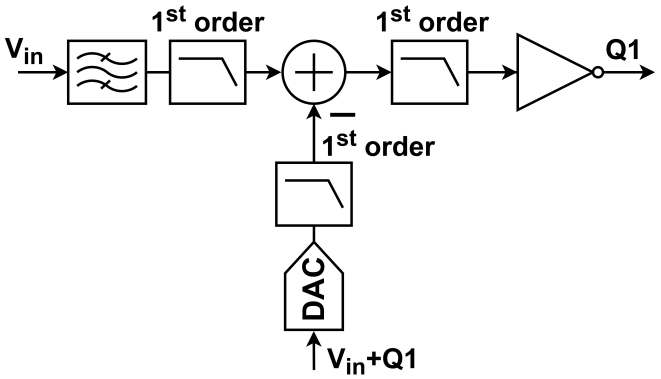

Figure 6.6: Open loop LPF implementation, 1^{st} order in the APF, 2^{nd} order after the inverter

6.2.2. APF circuit

The starting point for the APF is an already working latency compensating APF network from the paper [37]. However, in [37] the APF is implemented with a closed loop amplifier, where the feedback network allows a current to flow through R_3, see Figure 6.7. The intention is to make an open loop amplifier based on an inverter.

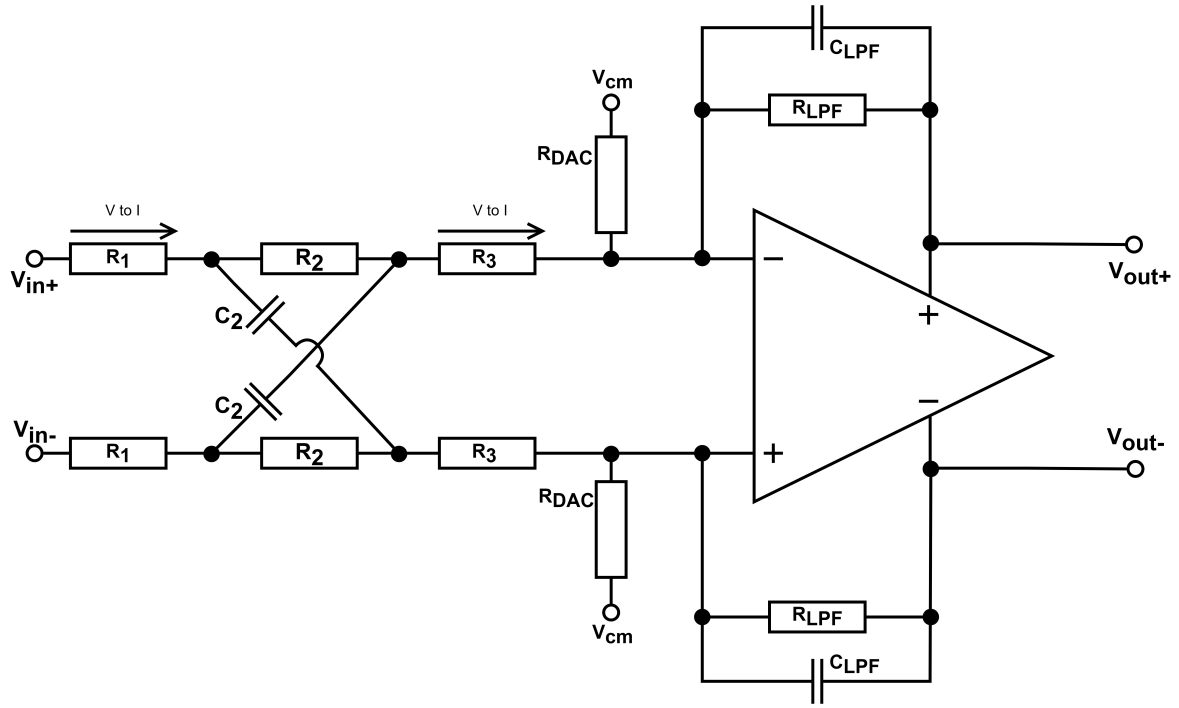

Figure 6.7: Simplified circuit implementation APF

An ideal inverter can be seen as an operational transconductance amplifier (OTA). Figure 6.8 shows an open loop amplifier, where it can be seen that there is no feedback path.

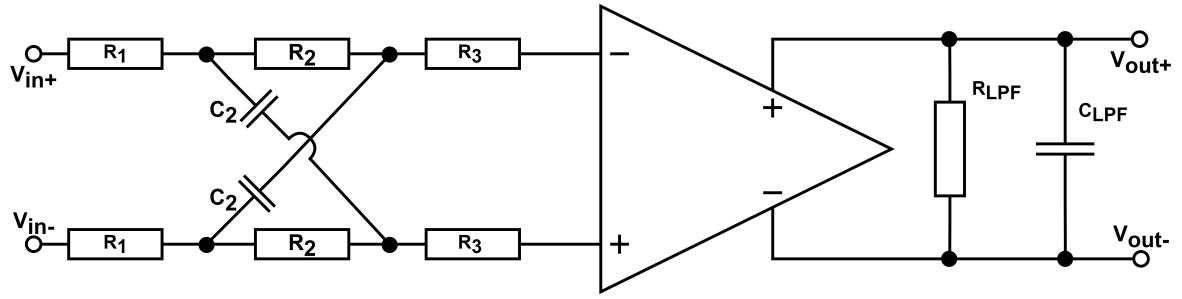

Figure 6.8: Open loop amplifier

Assuming the standard ideal operational transconductance amplifier rules hold, it is clear that no current can flow into the OTA. Thereby, R_3 has no current flowing through it, thus it does not impact the transfer function of the APF. Moreover, the absence of a feedback path causes the virtual ground at input nodes of the OTA to disappear. The open loop gain of the amplifier does not attenuate the voltage swing at its input, and because the DAC is implemented with resistors, there is mutual loading of the APF and the DAC. In other words, the transfer of the DAC signals will "see" the APF network, hence the DAC will have a transfer function. Moreover, the DAC has a certain magnitude and phase response on top of the latency. Consequently, the complexity of the design of the APF circuit increases, due to the added degree of freedom, the DAC transfer function.

The APF circuit in [37] is taken as starting point. However, the resistor R_3 does not influence the transfer function. Therefore, the R_3 is discarded, see Figure 6.9. The circuit that is left exhibits the transfer function 6.1 and 6.2.

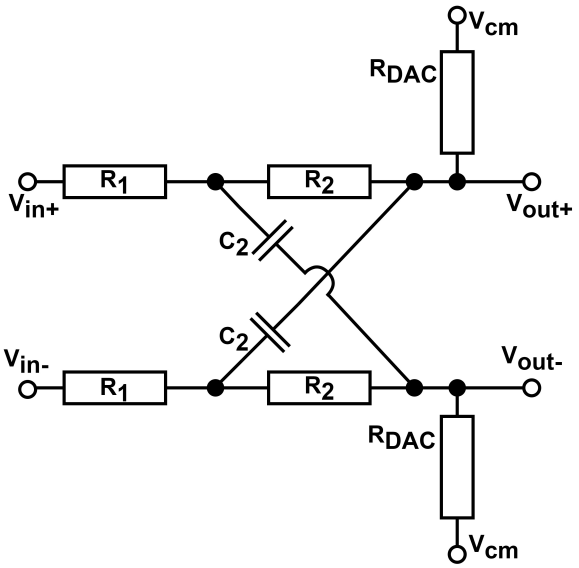

Figure 6.9: APF for the open loop implementation

$$H_{APF}(s) = \frac{(1 - sR_2C_2)R_{DAC}}{R_1 + R_2 + R_{DAC} + sC_2(R_1R_2 + 4R_1R_{DAC} + R_2R_{DAC})} \tag{6.1}$$

$$H_{DAC}(s) = -\frac{R_1 + R_2 + sC_2R_1R_2}{R_1 + R_2 + R_{DAC} + sC_2(R_1R_2 + 4R_1R_{DAC} + R_2R_{DAC})} \tag{6.2}$$

It can be seen that the zeros will differ, but the poles are on the same frequency. This influences the magnitude and phase response. However, a gain deviation between the APF

and DAC transfer function is wanted. To keep the circuit complexity of at a minimum, the reference of the DAC is not down scaled to 675mV, but it is kept at the 900mV of the system. In order to have the same output without an adjusted reference, the DAC must have a magnitude transfer of -2.5dB as derived in Chapter 4.6. Note that the DAC transfer must have this gain reduction relative to the gain of the APF. The numerator shows that at DC, the R_{DAC} must be $4/3$ times larger than R_1 and R_2 combined. Furthermore, it shows that R_{DAC} together with R_1 have the most influence on the pole location. Since the R_{DAC} is set due to the magnitude requirement, R_1 must be kept small. Knowing that R_1 is kept small, the numerator causes the zero of the DAC transfer function to be at a much higher frequency than the zero of the APF transfer function. At last, it can be assumed that the zero of the APF transfer function is at a higher frequency than the pole. As a result, the higher frequencies have less attenuation. This is unwanted. A solution for this is to add a pole at the same frequency as the zero. In order to accomplish this, a capacitor is added after R_1, see Figure 6.10.

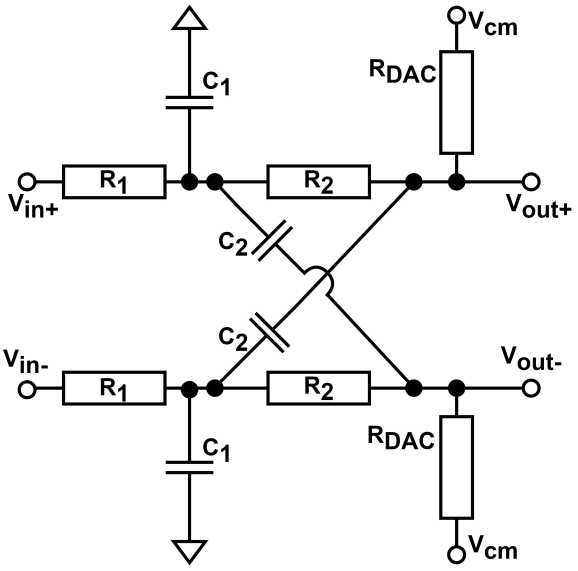

Figure 6.10: APF for the open loop implementation, with the added shunted capacitor

$$H_{APF}(s) = \frac{(1 - sR_2C_2)R_{DAC}}{R_1 + R_2 + R_{DAC} + sC_1(R_1R_2 + R_1R_{DAC}) + sC_2(R_1R_2 + 4R_1R_{DAC} + R_2R_{DAC}) + s^2C_1C_2R_1R_2R_{DAC}} \quad (6.3)$$

$$H_{DAC}(s) = -\frac{R_1 + R_2 + sC_1R_1R_2 + sC_2R_1R_2}{R_1 + R_2 + R_{DAC} + sC_1(R_1R_2 + R_1R_{DAC}) + sC_2(R_1R_2 + 4R_1R_{DAC} + R_2R_{DAC}) + s^2C_1C_2R_1R_2R_{DAC}} \quad (6.4)$$

From the previous analysis, it is clear that the APF has a lot of constraints to comply with, especially due to the mutual loading of the APF and the DAC. It cannot be overcome that the APF has a certain magnitude transfer. This is unwanted, but assumed to be inevitable.

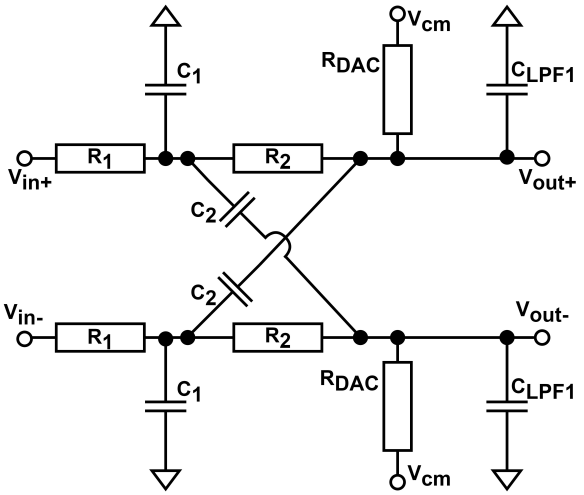

Figure 6.11: APF for the open loop implementation, with the LPF added

Furthermore, the LPF must be of the 2^{nd} order. One order of the filtering can easily be obtained, which can be seen in Figure 6.8 where the RC at the output of the OTA. However, the 2^{nd} order of the filtering must be incorporated too. This can be done by adding another RC at the output, or it can be applied at the input of the amplifier, see Figures 6.5 and 6.6. The latter is implemented in Figure 6.11, this saves some area and thermal noise of the resistor. Moreover, the APF is less sensitive to the input capacitance of the inverter, because there is already a relatively large capacitor at the input of the inverter. Therefore, the deviation of the input capacitance is relatively a small amount of the total capacitance.

From Figure 6.12, it can be seen that the APF transfer function has an attenuation of the input signal to the summation node. This attenuation will magnify the noise of the LPF and the amplifier. Thereby, it makes the requirements more stringent. On top of this, the gain of the amplifier must be increased, since the gain of the input of the stage to its output must be 9.1dB. However, there is an attenuation of 4.9dB. Hence, the amplifier must compensate for this, by applying a gain of 14.0dB ($= 4.9 + 9.1$).

$$H_{APF}(s) = \frac{(1 - sR_2C_2)R_{DAC}}{R_1 + R_2 + R_{DAC} + sC_1(R_1R_2 + R_1R_{DAC}) + sC_2(R_1R_2 + 4R_1R_{DAC} + R_2R_{DAC}) + sC_{LPF}(R_1R_{DAC} + R_2R_{DAC}) + s^2R_1R_2R_{DAC}(C_1C_2 + C_1C_{LPF} + C_2C_{LPF})} \quad (6.5)$$

$$H_{DAC}(s) = -\frac{R_1 + R_2 + sC_1R_1R_2 + sC_2R_1R_2}{R_1 + R_2 + R_{DAC} + sC_1(R_1R_2 + R_1R_{DAC}) + sC_2(R_1R_2 + 4R_1R_{DAC} + R_2R_{DAC}) + sC_{LPF}(R_1R_{DAC} + R_2R_{DAC}) + s^2R_1R_2R_{DAC}(C_1C_2 + C_1C_{LPF} + C_2C_{LPF})} \quad (6.6)$$

The resulting APF and DAC transfer functions are given by Equations 6.5 and 6.6, which are shown in Figures 6.12 and 6.13. Note that the sinc response of the DAC is not incorporated.

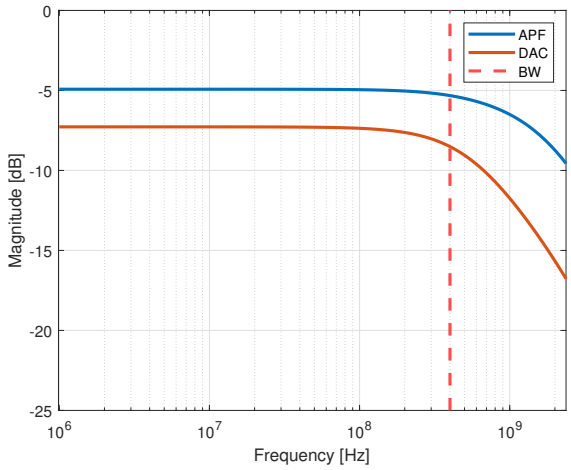

Figure 6.12: Magnitude response of the APF and DAC for the open loop implementation, with the LPF added

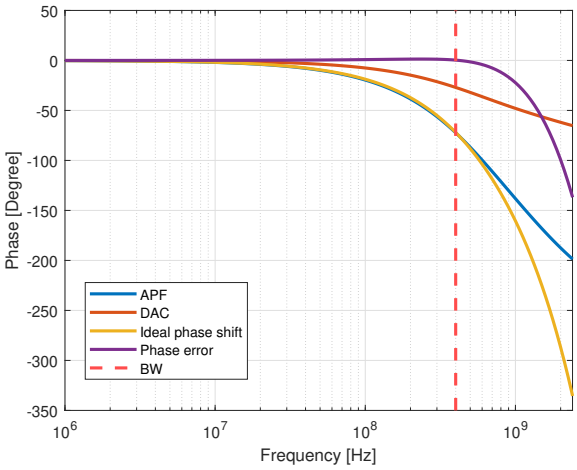

Figure 6.13: Phase response of the APF and DAC for the open loop implementation, with the phase error

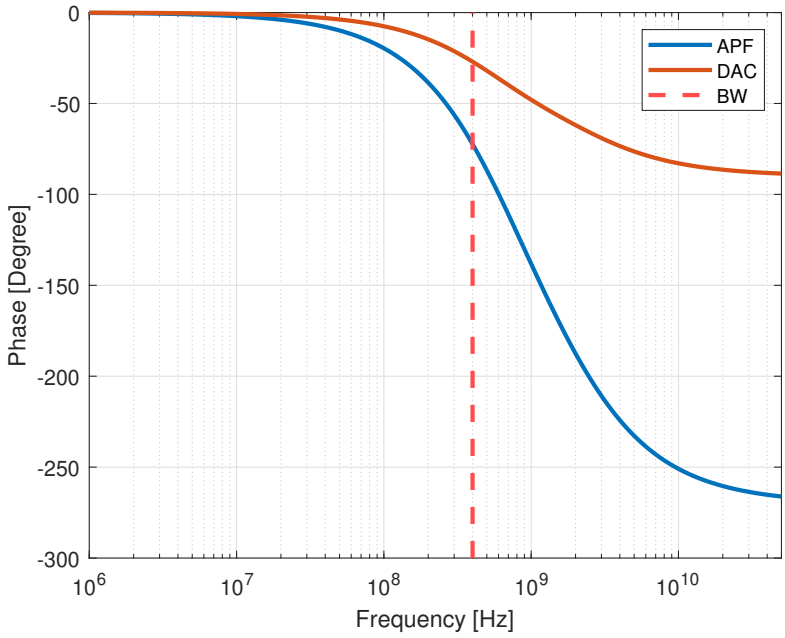

Figure 6.14: Phase response of the APF and DAC, combined with the first LPF for the open loop implementation

Figure 6.14 shows that the phase response of the APF is 3^{rd} order and the response of the DAC is 1^{st} order. Consequently, the phase compensation of the APF is effectively is 2^{nd} order. Next to this, the low-pass filtering of the DAC does improve the out-of-band performance, because the OOBs are suppressed.

At last, the APF implementation attenuates the input signal and generates noise. The attenuation, increases the input referred noise of the amplifier. Furthermore, the noise power of a resistor can be expressed as:

$$\bar{V}^2_{n,in,res} = 4kTRBW \tag{6.7}$$

However, this is not equal to the individual noise contributions of the resistors, because all the resistors have a certain transfer function to the input. This must be taken into account. To be clear on the amplifier specification, its specifications are given in Table 6.1.

Specification	Unit	Budget
Current	mA	2.1
$P_{n,in}$	nV^2	6.1
Gain	dB	14.0
HDx	dBc	70.0

Table 6.1: Specifications of the open loop amplifier

6.2.3. The amplifier

Before analysing the open loop amplifier, the main advantages and disadvantages of an inverter are briefly reviewed. The main advantages arise from the reused current by the NMOS and PMOS, which causes a large g_m/I_d. Consequently, the inverter has a large g_m. As a result, it has a large bandwidth, a good noise performance and a high intrinsic gain. Furthermore, the output signal swing is large [38]. On top of this, the linearity of an inverter is high (if biased in strong inversion saturation) [39]. At last, the drive capability of the inverter is good [40].

The main disadvantage of an inverter is the high PVT sensitivity, since it amplifies the supply voltage variations [40], [41], [42]. In other words, the PSRR is not very good. This causes the system to have a dedicated supply regulator. However, there are techniques to increase the PSRR [38]. Another drawback of an inverter is the CMRR. Both must be calibrated or compensated for, this is out of the scope of the thesis.

For the comparison of the two filter implementations, the inverter is used as the active element. The length is limited to a maximum of 120nm. For the analysis of the inverter, the square law model is used. This model gives a limited understanding of the transistors because the technology size is 28nm. To obtain a better understanding, the length, the width and the input voltage are swept. For a larger width of the inverters, more current is dissipated and a larger g_m is obtained. The latter is beneficial for the intrinsic gain and their noise performance, these statements are verified in Section 6.2.3.1.

The intrinsic gain can be described by:

$$A_v = -(g_{m-NMOS} + g_{m-PMOS})(r_{o-NMOS}||r_{o-PMOS}) \tag{6.8}$$

By increasing the length of the NMOS and PMOS, the output resistance (r_o) increases. Consequently, the intrinsic gain increases. Next to this, simulation results show that the threshold voltages decrease by increasing the length of the transistors. This is logical, because the distance between the drain and the source is larger, hence a larger voltage potential is needed. As a result, the threshold voltage is larger.

Next to this, the amount of inverter configurations is limited due to the low supply voltage. The inverter is used as a gain element, thus it is wanted to operate the transistors in weak inversion saturation, although, in terms of linearity, the strong inversion saturation could be a necessary. Stacking more than two transistors (NMOS + PMOS) on top of each other is unwanted, which can easily be demonstrated with a few Equations [38]. For simplicity, the analysis is focused on the NMOS. The supply voltage is 0.9V, where the threshold voltage of the used technology for the NMOS is 244mV (and for the PMOS is 340mV). For proper operation of the transistors, they must be in the saturation region, thus the following must hold for the NMOS:

$$V_{DS} > V_{Ov} \quad and \quad V_{GS} > V_{Th}, \quad where \quad V_{Ov} = V_{GS} - V_{Th} \tag{6.9}$$

For the PMOS the same Equation with opposite signs holds. To illustrate that there is no room for another transistor, Figure 6.15 shows that the input range is very small for a linear amplification. The inverter has a linear amplification approximately from 200mV to 700mV, and has a maximum output swing of 250mV. This comes down to an input range of approximately 88mV. Furthermore, the transistors have less headroom when another transistor is stacked on top. As a result, there is no headroom for another transistor. Another artifact that can be seen, is that the PMOS is limiting the operation in the saturation region.

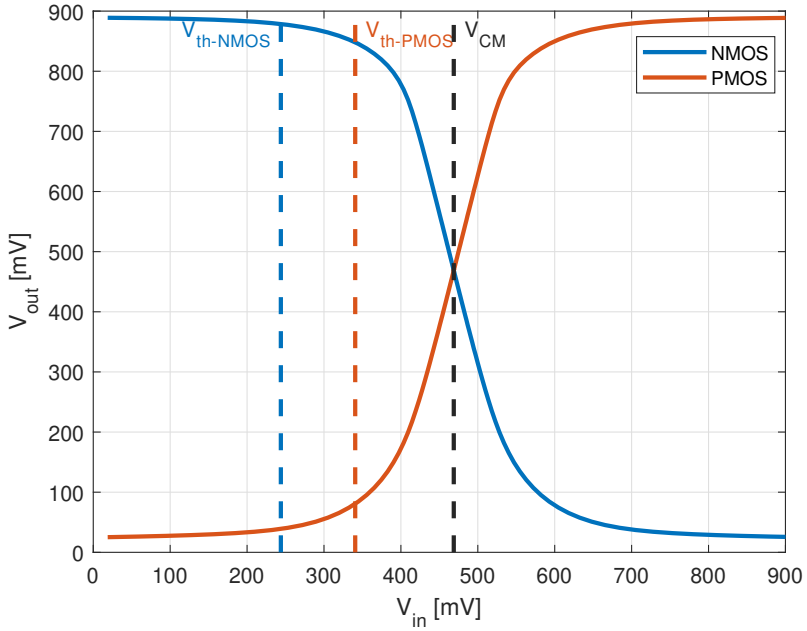

Figure 6.15: Operation region inverter, for a gain of 14dB and gate length = 30nm

6.2.3.1. Noise optimization

The main noise sources of a transistor are the thermal, flicker and shot noise. However, the latter is neglected, because the contribution is very small [43]. Furthermore, in a later stage the amplifier will be chopped, hence the flicker noise is not considered. Consequently, the thermal noise remains and its input-referred thermal noise voltage contribution is described by [38], [41]:

$$\bar{V}_{n,in}^2 = \frac{8kT\gamma}{g_{m-NMOS} + g_{m-PMOS}} \tag{6.10}$$

Equation 6.10 shows that a large g_m is beneficial for the noise contribution. In order to obtain a large g_m, either the current can be increased by increasing the number of fingers of a transistor or the inverter must be set further into weak inversion. The latter increases the g_m efficiency. Figure 6.16 shows that for a larger current, the noise decreases. On top of this, the g_m can be increased by decreasing the overdrive voltage, see Equation 6.11. The V_{TH} increases with larger lengths of a transistor.

$$g_m = \frac{2I_D}{V_{Ov}}, \quad where \quad V_{Ov} = V_{GS} - V_{Th} \tag{6.11}$$

Hence, increasing the length of the transistor increases the noise performance of the inverter, which is illustrated in Figure 6.16.

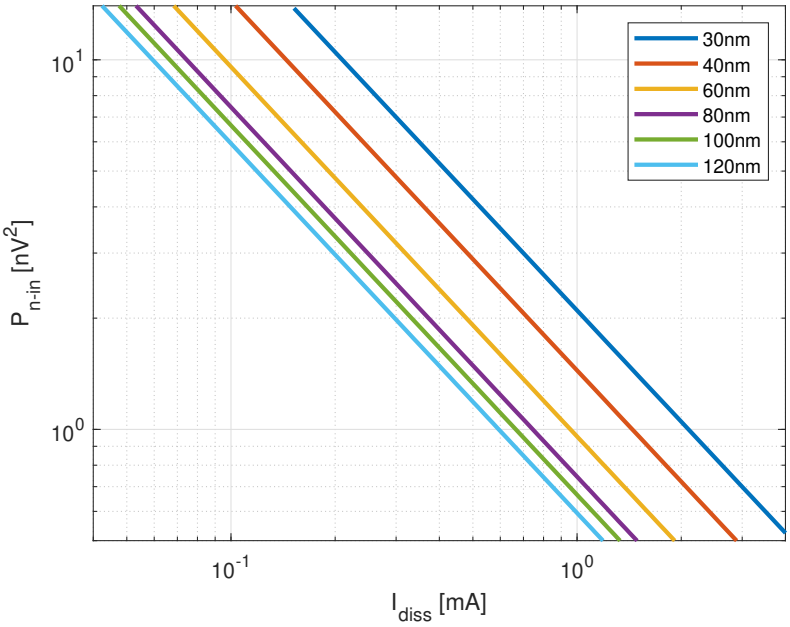

Figure 6.16: Input referred integrated noise voltage versus current dissipation, for different transistor lengths of the inverter

Even though it is out of the scope of this thesis, a larger gate size, due to larger transistor length, causes a smaller flicker noise contribution [41].

From the analysis, it can be concluded that an inverter with a length of 120nm is wanted in terms of the noise performance. To determine the current for which the noise budget is reached, the gain is set to 14dB and the LPF resistor at the output of the inverter is scaled accordingly. This results in a current consumption of 303μA.

6.2.3.2. Distortion optimization

In an open loop configuration, the non-linearity of the amplifier is a crucial requirement. The non-linearity of the amplifier can be divided in a small signal and a large signal distortion. As the inverter essentially is a transconductor it has two main factors that contribute to the small signal distortion, namely, the non-linear g_m and the output impedance [44]. For the large signal distortion, the output swing will limit its performance. In CMOS the non-linearity is dominated by 2^{nd} order distortion, which easily can be seen from the square law models. Fortunately, the implementation is differential, which causes the 2^{nd} order distortion terms to cancel itself [41], [44]. Moreover, the distortion in the output current is mainly due to the short channel effects, which are verified by Equations from [44].

Figure 6.15 shows that the inverter has a limited input voltage for which it linearly amplifies. It starts to clip before the threshold voltages. Hence, it seems that the distortion is dominantly set by the large signal distortion, the output signal swing. This is confirmed by Figures 6.17 and 6.18. In Figure 6.17, it is assumed that the HD_3 is the largest harmonic.

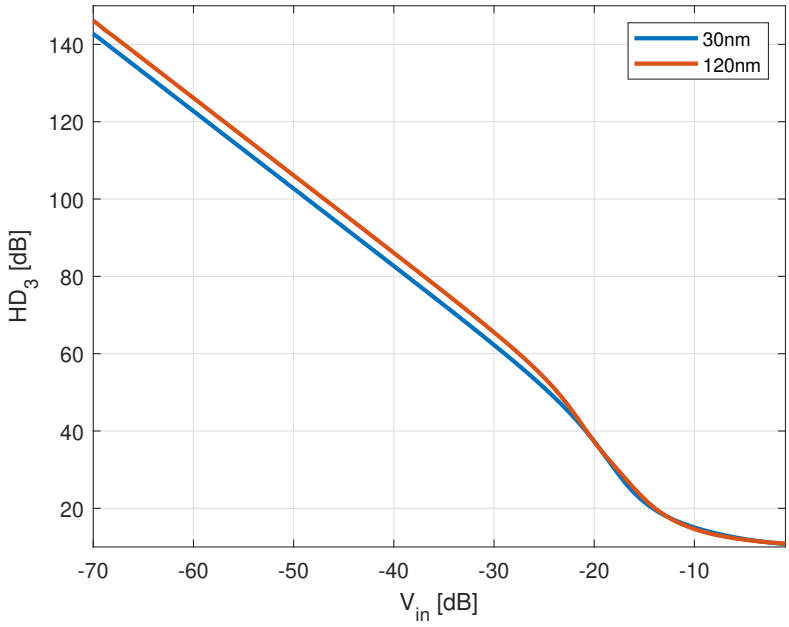

Figure 6.17: HD_3 versus V_{in} for transistor lengths of 30nm and 120nm, for the same current

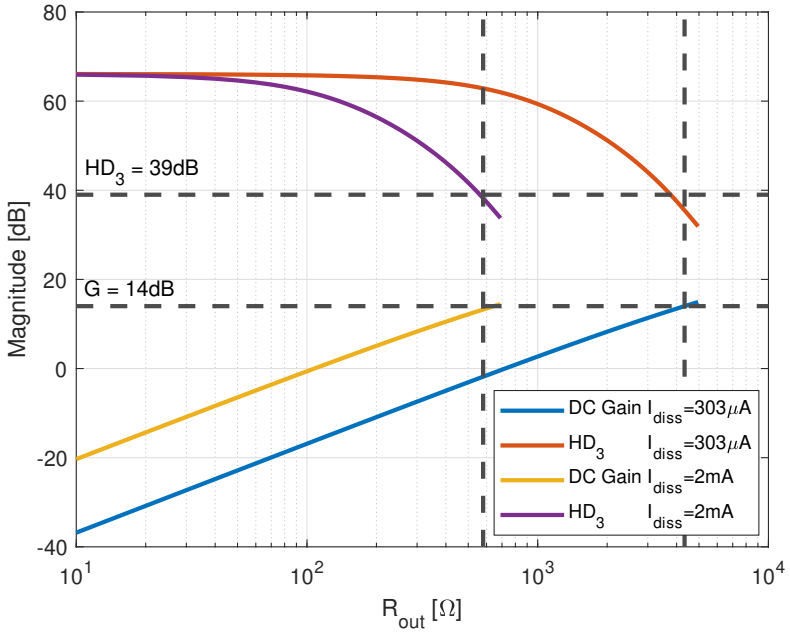

Figure 6.18: HD_3 versus resistance of the LPF, for different currents, for a length of 120nm

Another artifact that Figure 6.17 shows is that the distortion is larger for smaller gate lengths. This can be explained by the output impedance of the inverter. For a larger the deviation of the output impedance, the gain will be more non-linear. This is confirmed by Figure 6.19.

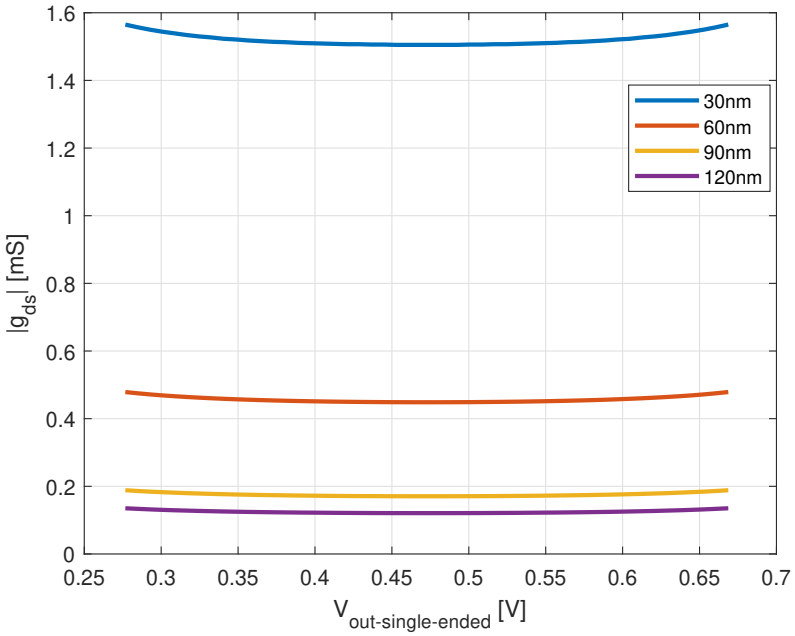

Figure 6.19: The output resistance versus the single ended output swing

Furthermore, assuming that the overdrive voltage is constant, Equation 6.11 shows that the g_m increases for a larger current. Combining this with the results from Figure 6.18, shows that for the wanted DC gain a similar distortion is achieved. Consequently, for this gain the g_m does not dominate the distortion.

At last, the book [44], shows that for large signal operation, where the NMOS is in saturation and the PMOS is pushed into weak inversion, the 3^{rd} order harmonic coefficient can be expressed as:

$$c_3 = \theta_n \beta_n - I_0 \tag{6.12}$$

Here, θ_n is the short channel parameter, $\beta_n = \mu_n C_{ox} \frac{W_n}{L_n}$ and I_0 is the minimum current in the saturation region of the PMOS transistor. Note that Equation 6.12 must hold for the case where the PMOS is in saturation and the NMOS is in weak inversion. The Equation 6.12 has to be adjusted accordingly. All in all, the distortion is better for larger gate lengths, which is supported by Equations from [44]. For a gain of 14dB, the g_m of the inverter does not dominate the distortion. The distortion is dominated by the large output signal swing, which modulates the output resistance of the inverter. Increasing the gate lengths decreases the variation in the output resistance of the inverter. Hence, the large signal distortion can be improved by correctly sizing the NMOS and PMOS such that Equation 6.12 is minimal.

The previous analysis, shows that in the analog domain, the linearity can be optimized by correct sizing of the inverter. Furthermore, resistive degeneration could be an option [45]. However, it is expected that it does not improve the linearity a lot, because the degeneration resistor linearizes the g_m and not the large signal distortion. Therefore, the impact will be minor. However, this is not investigated in depth and is recommended looking into. Another method to improve the linearity is in the digital domain. There are multiple possibilities to digitally calibrate the inverter. A digital calibration method could be employed in the analog path of the inverter, which counteracts the distortion [4], [45], [46]. The digital calibration method can also

be performed in the digital back end. The idea behind this is that the generated distortion of the inverter captured, and fed to the output of the system, therefore, it cancels at the output. Theoretically, this could lead to an infinite linearity of the system. However, this is out of the scope of this thesis and is strongly recommended to look into. At last, the inverter is optimized for the distortion such that c_3 in Equation 6.12 is as small as possible. The results are in given in Table 6.2. The resulting transfer function is given in Figure 6.20.

Specification	Unit	Obtained
Current	μA	321.0
$P_{n,in}$	nV^2	15.9
Gain	dB	14.0
HDx	dBc	55.1

Table 6.2: A summary of simulations results of the open loop filter

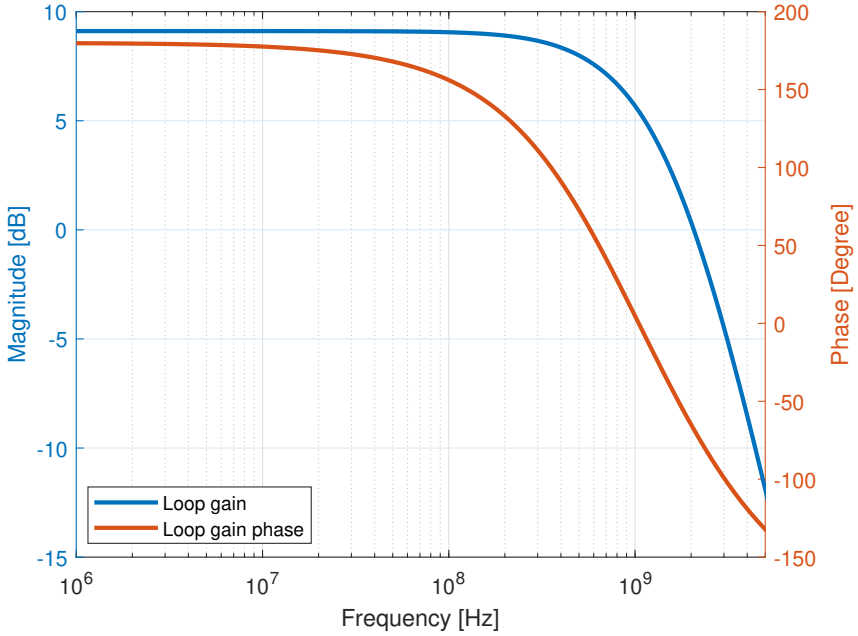

Figure 6.20: The open loop amplifier transfer function

Table 6.2 shows that the HDx specification is not obtained. There is another other option to increase the linearity, namely, the coarse ADC could resolve more bits, causing a smaller magnitude of the residue signal assuming the gain to remain the same. This will cause a decreased output swing of the amplifier. As a result, the linearity increases. However, the latency will also be larger. Thus, a more complex APF is needed, which is unwanted. Finally, other open loop amplifier configurations should be investigated, such as a common source stage combined with a regeneration resistor and calibration techniques [45].

6.3. Closed loop implementation

6.3.1. LPF implementation

The LPF must have a 2^{nd} order roll off, which can be realized in multiple ways. For instance, a Sallen-Key filter can be used, but it needs two inputs, one for the plus and minus input at the positive and negative side of the amplifier [47]. However, this increases circuit complexity,

which is unwanted. The other options are a cascade of two 1^{st} order LPFs or a single 1^{st} order LPF. A 2^{nd} order LPF can be made from only a 1^{st} order LPF, by making use of the intrinsic pole of the amplifier. The former can easily be realized, but it requires a larger power consumption. This can easily be reasoned by the fact that the LPF will have to be made twice. The second LPF will have some relaxed requirements, but nevertheless it will consume power. Furthermore, the distortion requirement is more stringent for two cascaded LPFs than for a single LPF. Therefore, the single 1^{st} order LPF is the most promising solution, see Figure 6.21.

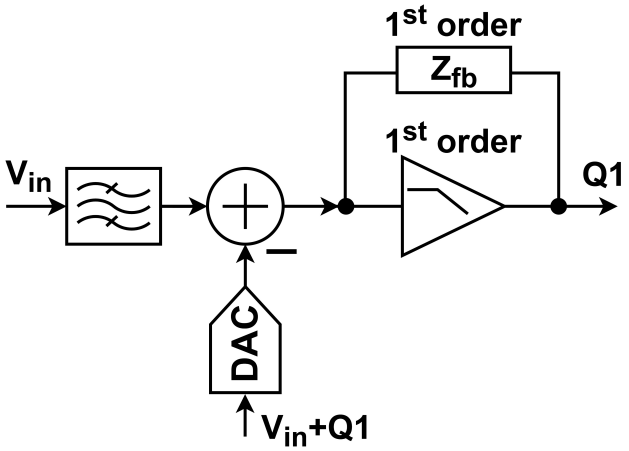

Figure 6.21: Closed loop 2^{nd} order LPF realization

6.3.2. APF circuit

The APF of the open loop LPF implementation effectively achieves a latency compensation that is 2^{nd} order. To maintain a fair comparison, the closed loop implementation also uses a 2^{nd} order APF. Therefore, the 2^{nd} order APF of [37] is taken. In the paper [37], it is assumed that, $2R_1 = 2R_3 = R_2$. The transfer function of the APF can be expressed as:

$$\frac{I_{out}(s)}{V_{in}(s)} = \frac{1 - sR_2C_2}{4R_2(1 + sR_2C_2)} \tag{6.13}$$

No further optimization are done for this APF, because for in-band signals the wanted gain of 9.1dB can be achieved. Out-of-band this is not the case, because then it comes 1.4dB short around 1GHz, see Figure 5.13. Nevertheless, better latency compensations are available, such as the APF implementation with inductors [21]. Another option is a higher order APF as is given in [48]. From Chapter 4, it is clear that the residue signal contains a smaller input signal magnitude for a better latency compensation. Consequently, the distortion requirement is easier to achieve. Figure 6.7, shows the implementation of the APF and LPF. Note that the summation of the signals is in the current domain, whereas for the open loop implementation, the summation is in the voltage domain. At last, the APF does not attenuate the input signal. Furthermore, the R-DAC has a noise contribution. The noise generation of the resistors is equal to Equation 6.7. However, the APF does not attenuate the ingoing signals. Therefore, the noise budget for the LPF for the closed loop implementation is larger than for the open loop implementation. The rest of the specifications for the closed loop implementation remain as it is derived in Chapter 5, see Table 6.3.

Specification	Unit	Budget
Current	mA	2.1
$P_{n,in}$	nV^2	11.7
Gain	dB	9.1
HDx	dBc	70.0

Table 6.3: Specifications of the closed loop amplifier

6.3.3. The amplifier

A three inverter based amplifier is chosen for this design, because with two inverters the amplifier will not have enough open loop gain. Simulation results show that the gain of an inverter with a length of 120nm is approximately 30dB. Hence, the loop gain will maximally be 48.3dB, where β = 11.7dB for a closed loop gain of 9.1dB. This is probably less, which is assumed not to be enough for the implementation. A four inverter based amplifier could potentially achieve a loop gain of 108.3dB, which is quite an overkill. Therefore, the power consumption will be unnecessarily large. Moreover, the CMFB is probably hard to implement, because of the needed negative feedback loop.

The amplifier has to consist of inverters, this will require a common mode and a stabilization circuitry. The stabilization network is executed with Miller compensation [41], [49]. The common mode is set by a basic network, because it is not the main component that determines the power consumption of the LPF. However, it can pose an issue for the eventual implementation. Therefore, a more sophisticated solution for the CMRR is recommended looking into [44].

In order to design the LPF, a current budget and an optimization distribution are made, see Figure 6.22. The current budget is based on previous three inverter based on amplifier design [1].

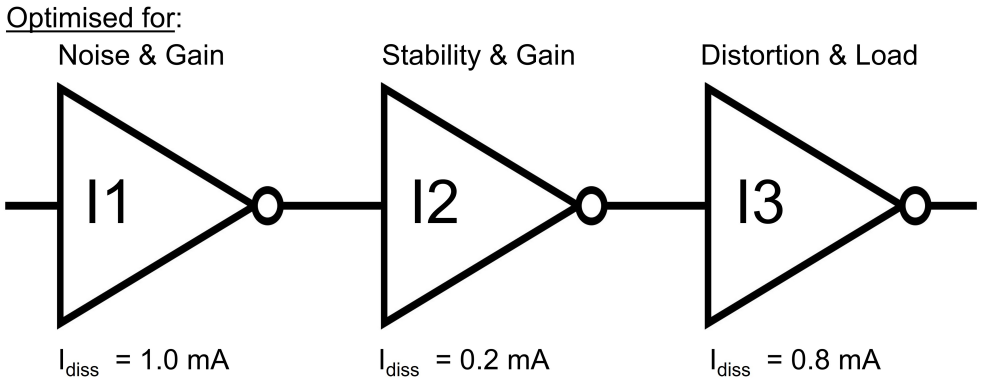

Figure 6.22: Inverter budget closed loop amplifier

The current budget and the optimization distribution, see Figure 6.22, is based on the following assumptions. The first inverter dissipates the most current, because it dominates the noise performance. Hence, the first inverter must have a large g_m, which can be obtained by increasing the current, which is described by Equation 6.11. The noise contribution of the other inverters is attenuated by the gain of the first inverter. Therefore, the first inverter needs a large gain. Hereafter, it is optimized for its current dissipation. As a result, the first inverter can dissipate the most current. The second inverter is optimized for the gain and the stability. It does not drive a large load or need a large g_m. Hence, the current budget is small. The

third inverter is optimized for the distortion, which does not necessarily demand a large current consumption. However, the third inverter must drive load. Therefore, the current budget of the third inverter is larger than the second inverter. The large intrinsic gain of the inverter is achieved by increasing the r_{out}, see Equation 6.8. A large r_{out} is obtained by increasing the length of the inverter, which is verified by simulation results. Another consequence of a larger length is a slower inverter, because for long channel devices, it holds that $f_t \propto 1/L$, where f_t is the transit frequency and L is the transistor length. However, it is assumed to be acceptable, because an inverter has a large bandwidth.

The optimization of the LPF, is performed as follows: The first inverter is given a large length such that it has a large gain, then it is optimized for its noise and current consumption. Hereafter, the first and second inverter are replaced by an ideal OPAMP, and the third inverter is optimized for its distortion. At last, the second inverter is optimized for stability and gain. The Miller compensation is used to stabilize the LPF. The Miller compensation is executed with a resistor and capacitor that form the feedback path on the first and the last inverter and the overall feedback network, see Figure 6.23. A proper optimization of all the things at once will result in a better LPF performance, but for the time being this optimization is expected to be good enough.

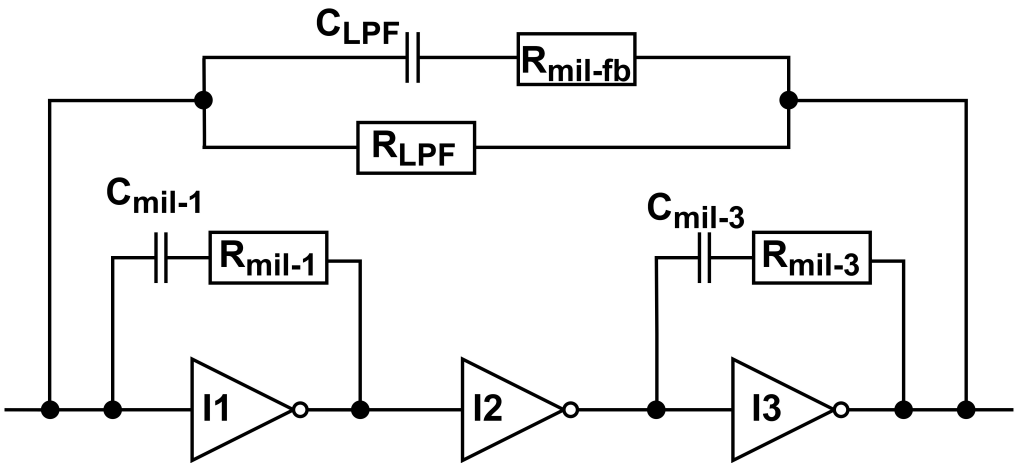

Figure 6.23: A single sided schematic of the closed loop LPF, the implementation of the Miller compensation

The resulting specifications are listed in Table 6.3, the loop gain and phase can be seen in Figure 6.25 and the final LPF transfer function is given in Figure 6.24.

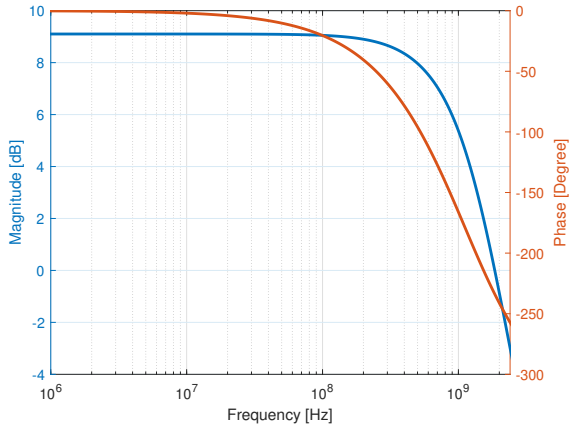

Figure 6.24: Transfer function closed loop amplifier

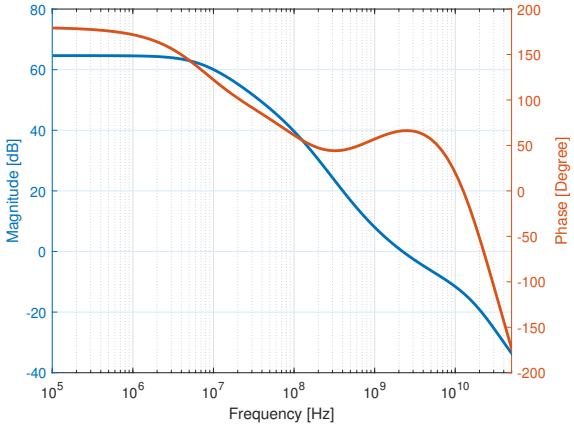

Figure 6.25: Loop gain and phase of the closed loop LPF

Furthermore, the loop gain in Figure 6.25 shows that the bandwidth is around 10MHz. This is acceptable in terms of filtering. With a larger amount of filtering, a larger amount of gain can be applied, but it must not limit the bandwidth of the system. However, the disadvantage is the gain mismatch of the LPF and the virtual ground node at the input of the LPF. The latter can be a problem, because the current summation is less ideal, thus a less accurate latency compensation can be achieved. It is recommended looking into.

Specification	Unit	Obtained
Current	mA	2.0
$P_{n,in}$	nV^2	16.1
Gain	dB	9.1
HDx	dBc	85.8
Phase Margin	°	64.6
Gain Margin	dB	35

Table 6.4: A summary of simulations results of the closed loop filter

Table 6.4, shows that the amplifier achieves the specifications within the current budget. The HDx is limited by the HD_3 and not by the HD_5, which is 87dBc. The CMFB is not taken into account and also not taken into account for the current budget. Nevertheless, the HDx overachieves the requirement. Therefore, an interesting option is to review the impact of the limited loop gain at high frequencies and the response of the APF network on this. It is expected that a larger loop gain is needed at high frequencies to give an accurate summation of the currents. The loop gain can be increased, because the HDx is overachieved. Hence, the magnitude of the loop gain can be traded off for a larger bandwidth. This is recommended looking into. Moreover, the LPF is not properly optimized, which gives room for a smaller power consumption. This will be needed to implement a more sophisticated CMFB, CMRR and PSRR circuitry. However, the LPF is not tested for other variations, such as PVT and component variations. Consequently, this should be investigated and reviewed whether the LPF still achieves the HDx requirement.

6.4. Open loop versus Closed loop implementation

This chapter gives a design of an APF and LPF implementation based on an open loop amplifier implementation and a closed loop implementation. Both implementations exhibit their own

pros and cons, which are reviewed and compared to each other. Their performance is listed in Table 6.5 and shown in Figure 6.26. Note that the total APF resistance is scaled such that it is equal in both implementations, with a total resistance of 450Ω.

For both implementations, it holds that they must improve their CMRR and PSRR, and it is strongly recommended to look into [38], [44]. Nevertheless, the closed loop implementation attenuates its error by the loop gain, hence it is inherently more robust than the open loop implementation. Apart from this, for the closed loop implementation, other amplifier configurations are recommended looking into.

The 2^{nd} order APF is used in both cases and provides a good enough latency compensation for in-band signals. However, with a better latency compensation, the input signal has a smaller magnitude in the residue signal as seen in Chapter 4. This will relax the needed HDx performance of the LPF, which relaxes the LPF design. Therefore, the 4^{th} order APF is recommended to look into. Note that a 4^{th} order APF probably increases the load of the preceding stage, which increases the power consumption of the LPFs. Furthermore, the closed loop implementation has an easier APF design as it has fewer constraints to comply with. On top of this, the closed loop implementation can integrate a Butterworth filter, which improves the out-of-band performance. However, the closed loop implementation does have a limited loop gain, which could lead to a bad the current summation at high frequencies. Resulting in an inaccurate latency compensation and a larger residue magnitude. The exact impact of the limited loop gain is not quantified and must be investigated. The open loop implementation inherently incorporates a low-pass filtering in the DAC path and thereby increasing the out-of-band performance.

In terms of the HDx, the open loop LPF does not reach the specification, but the closed loop implementation overachieves it, see Table 6.5. Consequently, the closed loop implementation performs better in terms of linearity. To improve the linearity of the open loop implementation, either a regeneration resistor can be implemented or calibration techniques must be applied. Both are strongly recommended to look into. Moreover, other open loop amplifier configurations should be investigated, such as a common source stage combined with a regeneration resistor and calibration techniques [45]. Furthermore, the system has a SFDR requirement, which must be explored. It is unknown what the linearity performance must be for the required SFDR. Hence, it could be that the SFDR will dominate the linearity requirement instead of the HDx. Note that the linearity of the LPFs cause a gain error, which must be taken into account designed the digital back end.

The power consumption of the open loop amplifier is far superior to the closed loop amplifier, it is nearly seven times as low, see Table 6.5. However, for a properly optimized closed loop amplifier, the current consumption will decrease. Nevertheless, the CMFB circuitry must be taken into account, which increases the power consumption. The flicker noise is out of the scope of this thesis, because the LPFs are chopped in a later stage of the design. Still, the chopping technique will increase the power consumption of the LPF. In order to save some power in the closed loop implementation, the loop gain can be decreased such that the HDx specification is not overachieved anymore. However, the performance is not checked for PVT and component variations etc. As a result, this must be looked into before lowering the loop gain. The same holds for the open loop implementation, the influence of the PVT variations must be investigated. This is recommended looking into.

The noise performance of the open loop LPF is much better than for the closed loop implementation, see Table 6.5. It has less noise sources and no feedback path that contributes to the noise.

At last, the gain error of both implementations are revised. It is assumed that it can be calibrated and that the digital back end must be able to replicate the LPF transfer function. Nevertheless, this is not quantified and must be thoroughly investigated. Furthermore, the open loop LPF shows a fairly easy transfer function without many poles and zeros. However, the closed loop implementation shows a lot of high frequency poles and zeros, which makes it harder to replicate.

The discrepancies of both implementation, seen in Figure 6.26, are due to slightly too small capacitors values in the design. However, these are easily adjustable.

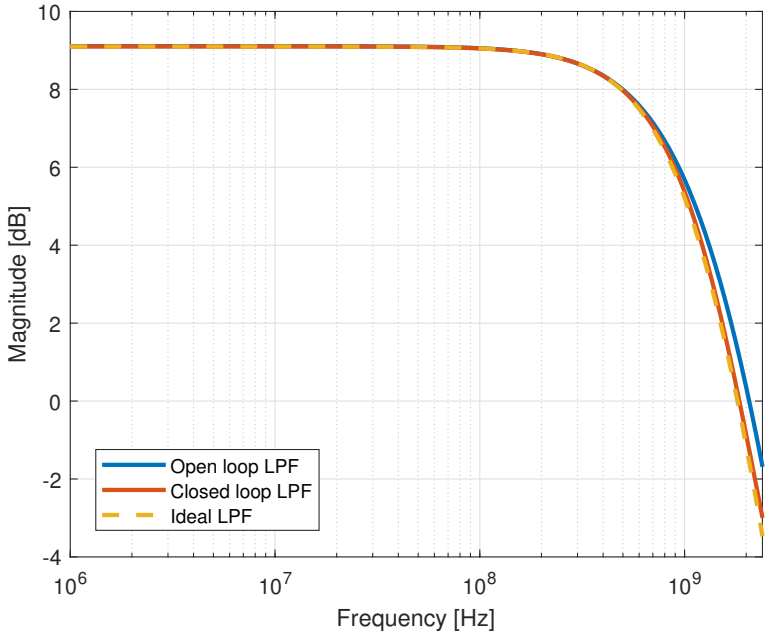

Figure 6.26: The magnitude responses of the different LPF implementations

All in all, the open loop LPF exhibits, very good power efficiency, but lacks in its linearity. Therefore, it is suggested to implement the closed loop filter in the first and second stage, but for the third and fourth stage, the open loop LPF should be implemented. The closed loop implementation will probably consume more power than the budget defines, because it has a bigger load, needs CMFB, must be chopped. However, by designing the back end stages with an open loop LPF, probably power can be saved. Thereby, compensating each other.

Specification	Unit	Open loop	Closed loop
Current	mA	0.3	2.0
$P_{n,in}$	nV^2	15.9	16.1
Gain	dB	14.0	9.1
HDx	dBc	55.1	85.8

Table 6.5: Obtained specifications of the closed loop filter versus the open loop filter

7

Conclusion

7.1. Conclusion

The next generation automotive radar application requires a bandwidth of 400MHz. The literature study shows that the SAR assisted CT $\Delta\Sigma$ ADC exhibits promising properties for this bandwidth. Furthermore, this study suggests that the front end is able to cope with the bandwidth enlargement. The APF is limiting the performance due to its large latency, which reduces the applicable gain by 10dB. This causes the back end ADC to resolve more bits and as a result the power budget for the amplifier is too small. Therefore, the two-stage architecture must be adjusted.

To relax the APF design, more stages that resolve fewer bits must be added. Due to this reduction in bits, the sampling rate increases, consequently the front end is less sensitive to the phase mismatch and increases the out-of-band blocker immunity. Moreover, the increased sampling rate causes a smaller latency. As a result, the applicable gain is closer to the ideal gain, which makes the 2 bit coarse ADC more efficient and enables a larger power budget for the amplifier.
The system study shows that the first stage determines the digital mismatch and jitter requirements. Furthermore, the requirements are more stringent for the 2 bit coarse ADC than the 3 bit coarse ADC. A trade-off between these requirements and the applicable gain (APF complexity) follows. The requirements of the 2 bit coarse ADC appear achievable, thus the best implementation solution is the five-stage (2-2-2-2-6 bit) architecture. The expected power dissipation is 12.7mW, which achieves a FoM of at least 172dB.

The open loop versus the closed loop implementation of the APF and the LPF, shows that the open loop implementation exhibits excellent power efficiency, but lacks in its linearity. The closed loop implementation, achieves the requirements, but consumes more power. To optimize power consumption, the first and second stage must be implemented with the closed loop filters, but the third and fourth stage must be implemented with the open loop filters.

7.2. Thesis contribution

The goal of the thesis is to create a system that can cope with the automotive ADC requirements. Hereafter, the best implementation for the APF and the LPF is compared. This thesis gives the following contributions:

- Creating a good understanding of the front end stage of the hybrid pipeline ADC, in which the contribution of the following system level blocks are evaluated:

  - AAF
  - APF
  - Amplifier
  - Coarse ADC
  - DAC
  - LPF

- Give insight into the feasibility of the APF implementation for a bandwidth of 400MHz.
- Enabling a coarse ADC/DAC implementation that optimizes the achievable SQNR.
- Create a good understanding of the factors that impact the residue signal.
- Investigated architectures with a different amount of stages and their trade-offs.
- Comparing the system level performance of a 2 bit coarse ADC versus a 3 bit coarse ADC.
- Create a lot of new research directions that optimize performance of the architecture.
- Create an overview for the best amplifier implementation for the architecture and the adjustments that have to be made for their implementation.

7.3. Future work

This thesis provides a good starting point for a lot more future research, as an entire system architecture is given as a solution. However, a lot of the system level blocks are not designed yet. These system level blocks are as follows:

- Design of the AAF and the R-DAC.
- Examine the impact of all the error sources combined on the system.
- Dither implementation in the coarse ADC/DAC.
- The coarse ADC resolved 2 bits, therefore, as a Flash ADC is probably a more logical choice instead of a SAR ADC. As it is much faster and the power consumption will probably not change much.
- Back end ADC must be redesigned from a 5 bit to a 6 bit SAR ADC.
- Design and implementation of the digital back end.
- The APF:
  - The circuit implementation of the 4^{th} order APF.
  - A limitation of the analysis is for the higher order transfer function, where the first pole and zero frequency matches, but the second pole and zero frequency is set at a higher frequency. This could be interesting to improve the out-of-band performance of the APF, which could lead to a larger gain at high frequencies.
  - The N-path filters should be investigated, because the accuracy of the latency compensation of the APF is limiting the two-stage architecture. The N-path filters will give a more accurate latency compensation, which is also beneficial, especially if larger bandwidths are targeted with this architecture.
- Digital calibration techniques for the gain error of the LPF.
- Digital calibration techniques for the component variation of the APF and the LPF
- The LPF with a closed loop amplifier:
  - A fully optimized closed loop LPF must be designed.
  - The exact impact of the limited loop gain must be quantified.
  - Improving the CMRR and PSRR, CMFB and PVT variability.

  - Implementing the LPF as a Butterworth filter.
  - Other closed loop amplifier configurations, that could be more efficient.
  - The influence of the LPF on the SFDR specification must be examined.

- The LPF with an open loop amplifier:

  - Calibration techniques to linearize the amplifier.
  - Examine the impact of regeneration resistors.
  - Investigate other amplifier configurations, such as a common sources stage.
  - Improving the CMRR and PSRR and PVT variability.

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