A 10 fJ·K ^{2}Wheatstone Bridge Temperature Sensor with a Tail-Resistor-Linearized OTA

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A 10 fJ·K^2 Wheatstone Bridge Temperature Sensor With a Tail-Resistor-Linearized OTA

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***Abstract*— This article describes a highly energy-efficient Wheatstone bridge temperature sensor. To maximize sensitivity, the bridge is made from resistors with positive (silicided diffusion) and negative (poly) temperature coefficients. The bridge is balanced by a resistive (poly) FIR-DAC, which is part of a 2nd-order continuous-time delta-sigma modulator (CTΔΣM). Each stage of the modulator is based on an energy-efficient current-reuse OTA. To efficiently suppress quantization noise foldback, the 1st stage OTA employs a tail-resistor linearization scheme. Sensor accuracy is enhanced by realizing the poly arms of the bridge and the DAC from identical unit elements. Fabricated in a 180-nm CMOS technology, the sensor draws 55 μW from a 1.8-V supply and achieves a resolution of 150 μK_{rms} in an 8-ms conversion time. This translates into a state-of-the-art resolution figure-of-merit (FoM) of 10 fJ·K^2. Furthermore, the sensor achieves an inaccuracy of ±0.4 °C (3σ) from −55 °C to 125 °C after a ratio-based one-point trim and systematic non-linearity removal, which improves to ±0.1 °C (3σ) after a 1st-order fit.**

***Index Terms*— Continuous-time delta-sigma modulator (CTΔΣM), energy efficiency, linearization, smart sensor, temperature sensor, trimming.**

I. Introduction

IN HIGH-PERFORMANCE integrated frequency references [1]–[6], temperature compensation is critical. To achieve low jitter, the associated temperature sensors must achieve high (sub-mK) resolution [1]–[4]. Due to the fundamental tradeoff between resolution and energy consumption [7], such sensors should be highly energy efficient in order not to dominate the energy consumption of the overall system.

Traditional BJT-based temperature sensors typically employ ΔV_{BE}, the difference in base–emitter voltage of two BJTs, as their main temperature-dependent signal [8]. Depending on the chosen BJT bias currents, the sensitivity of ΔV_{BE} typically varies between 0.1 and 0.2 mV/°C. On the contrary, resistor-based temperature sensors can have much larger sensitivities, especially when resistors with opposite temperature coefficients (TCs) are used in a Wheatstone bridge (WhB) configuration. For example, the WhB in [9] has a net TC of ∼0.44%/°C and can achieve a sensitivity of ∼4 mV/°C when biased at 1.8 V. Compared to BJT-based sensors, this larger sensitivity directly translates into greater energy efficiency.

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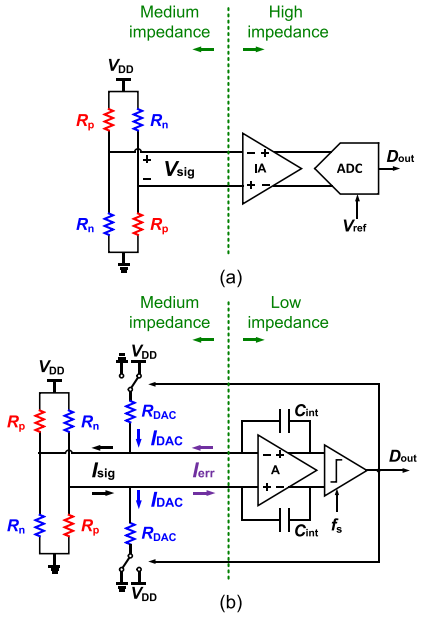

Fig. 1. (a) Conventional WhB readout using IA and ADC and (b) CTΔΣM WhB readout with a resistive DAC.

As shown in [10], the energy efficiency of WhB temperature sensors, as expressed by their resolution figure-of-merit (FoM) [7], is typically one or two orders of magnitude greater than that of their BJT-based counterparts. However, their spread is somewhat larger and typically requires a two-point trim to attain the same level of accuracy as that of one-point trimmed BJT-based sensors.

A WhB temperature sensor is usually read out by digitizing its open-circuit voltage, as shown in Fig. 1(a), where R_p and R_n are resistors with positive and negative TCs, respectively. An instrumentation amplifier (IA) can be used to match the output voltage and impedance of the bridge to the input range and impedance of the ADC, resulting in good energy efficiency. Compared to the classic three-opamp IA [11], a significant improvement in energy efficiency can be achieved by using a current feedback IA (CFIA) [12] or a capacitive-coupled IA (CCIA) [13]. However, the accuracy of the sensors will be limited by the combined gain errors of the IA and the ADC.

A simpler and more accurate way of reading out a WhB is by balancing it with a resistive DAC and, hence, nulling its output current. As shown in Fig. 1(b), the required feedback loop can be conveniently realized as a continuous-time delta-sigma modulator (CTΔΣM) [6]. The modulator's bitstream output D_{out} then drives the resistive DAC so as to null the

difference $I_{\mathrm{err}}(\mathrm{T})$ between the output currents of the DAC and the bridge. The resulting bitstream average will then be proportional to the amount of parallel resistance required to balance the bridge. If R_{DAC} is also an R_n-type resistor, the bitstream average will be solely determined by the temperature-dependent values of R_n and R_p resistors. The system is also robust to supply voltage variations, since the DAC and the bridge share the same supply.

By using a 1-bit CT$\Delta\Sigma$M, the sensor in [6] achieves a resolution FoM of 650 fJ·K^2. In [14], 49 fJ·K^2 was achieved with the help of a low-noise 1st stage and a high-sensitivity bridge consisting of regular poly resistors (R_n) and high-TC silicided poly resistors (R_p). In [15], even greater energy efficiency (20 fJ·K^2) was achieved by using a four-element FIR-DAC to reduce the input current swing and, hence, the supply current, of the modulator's 1st stage.

In this article, a WhB temperature sensor with a resolution FoM of 10 fJ·K^2 is described. This is achieved with the help of two innovations: a sensitivity-preserving return-to-CM (RCM) DAC switching scheme and an energy-efficient OTA with a tail-resistor linearization scheme. Furthermore, the sensor's accuracy is enhanced by merging the poly arms of the bridge with the unit elements of the DAC.

The rest of this article is organized as follows. Section II discusses the design of the bridge, CT$\Delta\Sigma$M, and RCM DAC. Section III focuses on the design of the energy-efficient linear OTA used in the CT$\Delta\Sigma$M, whereas the sensor's circuit implementation is discussed in Section IV. Measurement results are presented in Section V, and the sensor's performance is compared to the state of the art. Finally, conclusions are drawn in Section VI.

II. Architecture and Design Considerations

A. Resistor Choice

Assuming that a WhB temperature sensor is balanced and its thermal noise bandwidth is set by a sinc^1 filter, then its resolution FoM can be expressed as [9]

$$\mathrm{FoM_{WhB}} = \frac{8kT}{(TC_{p1} - TC_{n1})^2} \tag{1}$$

where TC_{p1} and TC_{n1} are the 1st-order TCs of the R_p and R_n resistors, and k is the Boltzmann constant. Hence, to maximize its energy efficiency, the net TC of the bridge should also be maximized. In [9], [14], and [15], silicided poly (R_p) and non-silicided poly (R_n) resistors were used, resulting in a net TC of $\sim$0.44%/°C and a theoretical resolution FoM of 1.7 fJ·K^2. The choice of poly resistors was mainly motivated by their low voltage dependence. In this work, the silicided poly resistors are replaced by silicided diffusion resistors since the latter have $\sim$10% higher TC and almost the same voltage dependence in the chosen technology.

B. CT$\Delta\Sigma$M Readout and FIR-DAC

Apart from the WhB, the readout circuit also consumes power and contributes noise. The power consumption of a CT$\Delta\Sigma$M-based readout is dominated by its 1st stage, which defines its noise level and must also absorb the error current

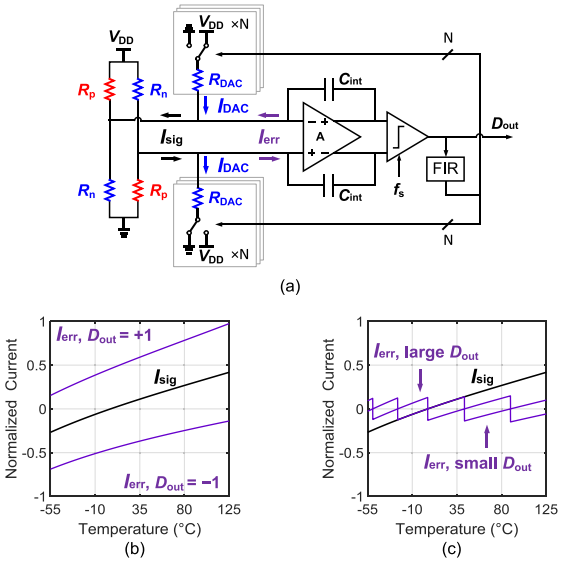

Fig. 2. (a) CT$\Delta\Sigma$M readout of a WhB sensor using FIR-DAC. Error current over temperature with (b) single-bit DAC or $N = 1$ and (c) multi-bit DAC.

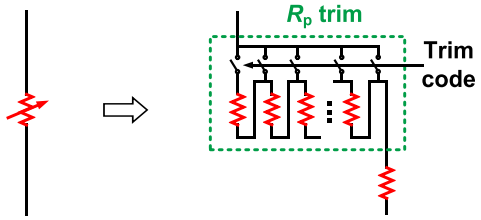

Fig. 3. R_p trim with constant switch ON-resistance.

$I_{\mathrm{err}}(\mathrm{T})$ shown in Fig. 2(a). In the case of a 1-bit DAC, the DAC current I_{DAC} will switch between the two extremes required to cover the desired range of bridge output current I_{sig}, resulting in a relatively large I_{err} over temperature. The 1st stage amplifier then requires a proportionally large supply current, which limits the modulator's energy efficiency. As shown in Fig. 2(c), the magnitude of I_{err} can be significantly reduced by the use of a multi-bit DAC [9], [15].

By using a zoom ADC configuration, the elements of the multi-bit DAC can be driven by a 1-bit quantizer [9]. A better approach, however, is to configure the DAC elements as an FIR filter [18] since this allows the inherent linearity of a 1-bit quantizer to be maintained without the need for dynamic element matching (DEM). Furthermore, since over-ranging is not required, the resulting I_{err} is smaller than that in a zoom ADC [15]. To make the best use of ADC range, R_p ($\sim$105 kΩ) is 3-bit trimmed to compensate for process spread ($\sim$40%) so that the DAC only has to compensate for the temperature dependence of I_{sig} over the targeted temperature range (−55 °C to 125 °C). To minimize the error from trimming switches, a unary trim is applied to ensure that only one switch is in series with the selected segment of R_p [15], as shown in Fig. 3.

C. RCM RDAC

As shown in Fig. 4(a), in [6] and [9], the DAC resistors were switched between the supply rails. Some of the R_n-type DAC

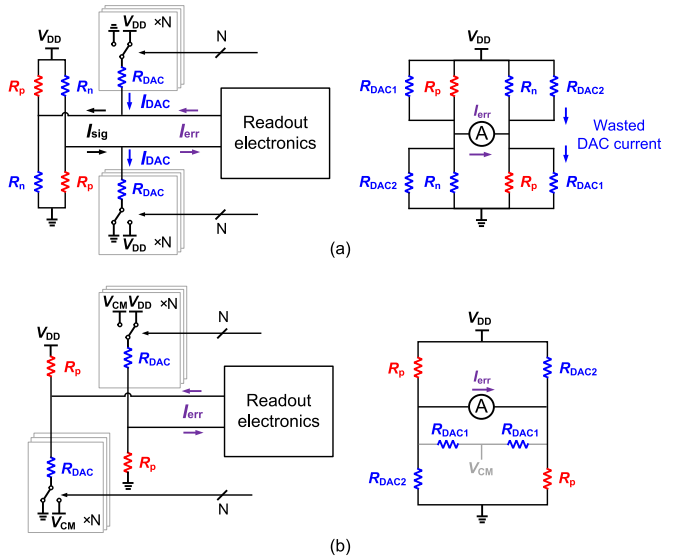

Fig. 4. (a) Rail-to-rail DAC switching scheme of a Wheatstone bridge sensor, showing how the DAC resistors consume extra supply current. (b) Proposed RCM RDAC made from unit elements.

resistors (R_{DAC1}) will then be connected in parallel with the R_p arms, whereas the rest (R_{DAC2}) are connected in parallel with the R_n arms. In a current readout scheme, the addition of balanced DAC resistors ($R_{DAC1} = R_{DAC2}$) will not alter the sensitivity of I_{err} to temperature. However, the added noise and power will degrade the FoM of the resistive front end (WhB and DAC resistors), as shown in Fig. 4(a). For the resistive front end in [15], the FoM will be degraded from 1.7 to 3 fJ·K^2 at room temperature (RT).

To avoid the extra supply current, a 1-bit serial DAC can be realized by using a switch to short a small segment of the R_n branch [16], [17]. However, realizing a linear multi-bit DAC then requires the implementation of non-uniform resistive segments, whose matching cannot be improved by DEM. Alternatively, the unused resistors of a parallel DAC can be switched to the output common-mode voltage of the bridge V_{CM} ($= V_{DD}/2$). As shown in Fig. 4(b), the required V_{CM} can be realized by simply shorting unused DAC pairs together, thus obviating the need for a dedicated voltage reference. Since the voltage drop across the R_{DAC} elements has now been reduced from V_{DD} to $V_{DD}/2$, their values must be halved to achieve the same DAC currents. For the same (minimum) resistor width, this RCM switching scheme also reduces DAC area by half.

With an appropriately scaled DAC, the proposed RCM switching scheme improves the FoM of the resistive front end to about 2.2 fJ·K^2 at RT. Due to the noise of the unused DAC resistors (R_{DAC1}), this is somewhat more than the theoretical FoM of the bridge itself (1.7 fJ·K^2). Although it might be tempting to eliminate their noise contribution by letting the unused resistors float, their parasitic capacitances will then cause slow-settling DAC currents. These, in turn, will cause intersymbol interference (ISI) and significantly increase the modulator's in-band noise (IBN).

D. DAC Array and DAC Range Optimization

As shown in Fig. 4(b), rather than implementing the R_n and R_{DAC} arms as separate resistors [9], [14], [15], they can be implemented as a single array of N unit resistors. To balance the bridge, the modulator must drive the DAC such that, on average, $R_{DAC} = R_p$. If the modulator's bitstream average μ ranges from 0 to N, then μ is given by

$$\mu = \frac{R_{DAC}(T)}{R_p(T)} = \frac{R_{DAC}(T_0)}{R_p(T_0)} \cdot f(T) \tag{2}$$

where T_0 is a reference temperature, $R_p(T_0)$ and $R_{DAC}(T_0)$ are nominal resistances, and $f(T)$ represents the combined temperature dependence of both resistors assuming no TC spread. This means that any spread in the nominal resistances $R_p(T_0)$ and $R_{DAC}(T_0)$ can be corrected by a one-point trim. In practice, TC spread is present and so a two-point trim is required for better accuracy [9], [14], [15].

In this work, the number of parallel DAC resistors ($N = 6$) is a tradeoff between chip area and efficiency: increasing N decreases I_{err} but requires more area-consuming DAC resistors. To cover the targeted temperature range, only four of the six unit elements (each 370 kΩ) are switched, as shown in Fig. 5. Thus, the modulator's bitstream average μ ranges from 2 to 6.

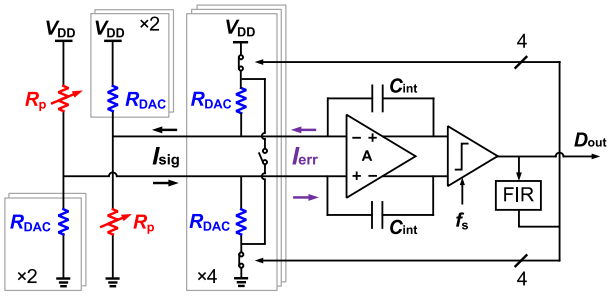

Fig. 5. FIR-DAC CTΔΣM readout of the WhB temperature sensor after DAC range optimization.

E. Integrator Nonlinearity

As for any multi-bit DAC, however, the non-linearity of the input stage will cause quantization noise foldback. In [15], the input stage was built around a two-stage opamp, whose high gain keeps its input swing small (<1 mV) and thus mitigates the non-linearity of its input differential pair, whose supply current could then be dimensioned for noise. However, the power consumed by the output stage then represents a loss of energy efficiency.

Greater energy efficiency can be achieved by building the 1st integrator around a single-stage OTA, since all its supply current is then used to lower its noise. However, for the same level of output current I_{out}, this will result in a significantly larger input swing (tens of mVs) and, hence, non-linearity. In a conventional differential pair, the maximum I_{out} is limited by the tail current, resulting in a compressing V–I nonlinearity [Fig. 6(b)]. On the contrary, an expanding and slightly more linear characteristic can be obtained by employing a pseudo-differential (PD) topology [Fig. 6(a)] [19]. In both cases, the effect of OTA non-linearity can be mitigated by either increasing the tail current or by resistive degeneration, as shown in Fig. 6(c). However, both approaches

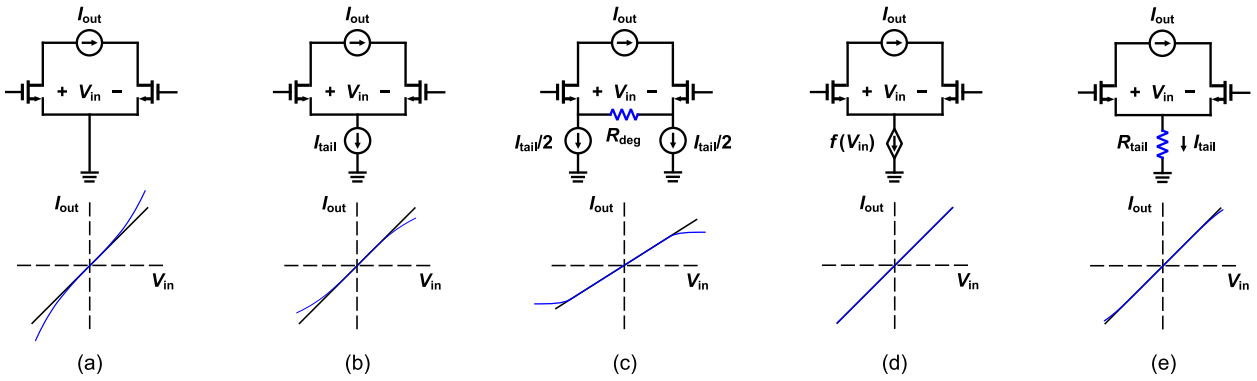

Fig. 6. Output characteristics for OTAs with (a) zero tail impedance, (b) high tail impedance, (c) degeneration, (d) controlled tail impedance, and (e) fixed tail impedance.

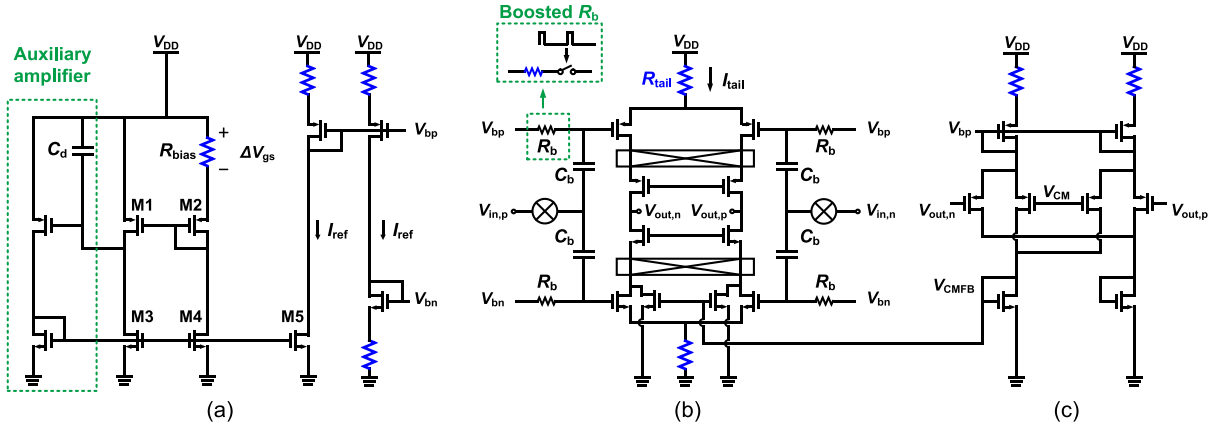

Fig. 7. Simplified schematic diagram of the linearized OTA. (a) Biasing generation. (b) Main circuit. (c) CMFB.

reduce energy efficiency. In Section III, a more energy-efficient way of improving OTA linearity will be discussed.

III. Linearized OTA Design

A. Linearization Principle

In Fig. 6(a) and (b), it can be seen that the impedance of the tail current source has a strong influence on OTA non-linearity. As in [20], it has been shown that the linearity of an OTA can be extended by making its tail current a non-linear function of its input voltage V_{in} [Fig. 6(d)]. Although this approach results in excellent linearity, it requires two trimming knobs to compensate for process spread. As also suggested in concurrent work [21], a simpler solution is to replace the tail current source by a tail resistor and then optimize its value for linearity, as shown in Fig. 6(e).

For input transistors biased in weak inversion, which, therefore, have an exponential I–V characteristic, it can be shown (Appendix) that the value of R_{tail} required to cancel the OTA's dominant 3rd-order non-linearity is given by

$$R_{\text{tail}} = \frac{nV_T}{2I_{\text{tail}}}, \tag{3}$$

where I_{tail} is the tail current for $V_{\text{in}} = 0$, n is a process-dependent slope factor, and $V_T = kT/q$ is the thermal voltage. It should be noted that this technique also works in cases where the input transistors are biased in moderate inversion, e.g., to increase speed. In such cases, however, the required resistor will be somewhat smaller.

B. Biasing Generation

Equation (3) indicates that for a fixed R_{tail}, the optimal I_{tail} should be proportional to absolute temperature (PTAT). This can easily be achieved by a conventional constant-gm biasing circuit [Fig. 7(a)]. Assuming that both $M1$ and $M2$ are biased in weak inversion with a current density ratio of k_1:1 and that the current mirror ratio between $M3$ and $M5$ is 1:k_2, the output reference current can be expressed as

$$I_{\text{ref}} = \frac{nV_T}{R_{\text{bias}}} \cdot \ln(k_1) \cdot k_2. \tag{4}$$

Assuming a ratio of 1:k_3 between I_{ref} and I_{tail}, and combining (3) and (4) then results in

$$R_{\text{bias}} = R_{\text{tail}} \cdot \ln(k_1) \cdot k_2 \cdot k_3. \tag{5}$$

Since R_{bias} is proportional to R_{tail}, a process and temperature robust biasing scheme can thus be achieved by realizing R_{bias} and R_{tail} as a pair of ratio-metrically matched resistors.

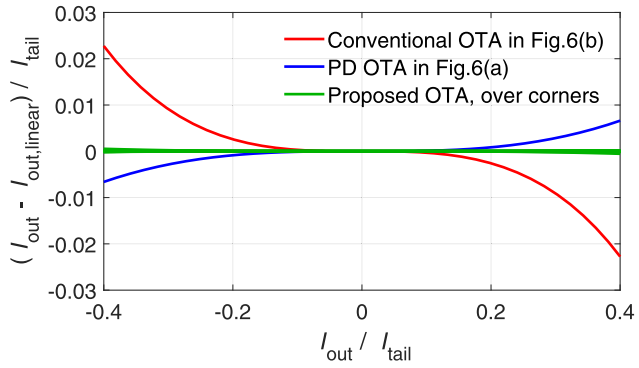

Fig. 8. Relative nonlinearity with different OTA structures.

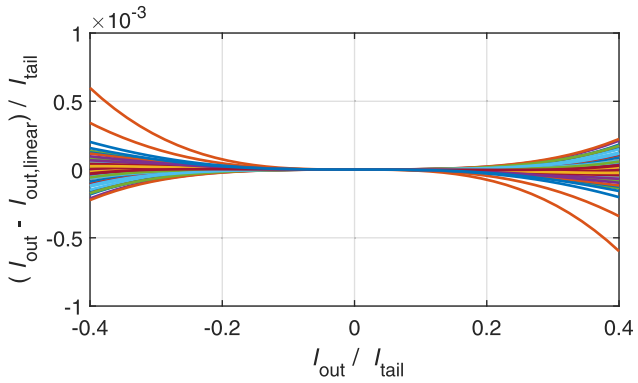

Fig. 9. Relative nonlinearity of the proposed OTA over corners.

C. Circuit Structure

The simplified schematic of the linearized OTA is shown in Fig. 8. To maximize its energy efficiency, its supply current is reused by both PMOS and NMOS input pairs. Both pairs are cascoded to achieve high dc gain. For simplicity, a single PMOS-based constant-Gm biasing circuit was used to set the tail currents of both the NMOS and PMOS input transistors via large biasing resistors R_b. The input voltage is then capacitively coupled to the gate of the input transistors. To minimize its noise contribution at the chopping frequency, R_b should be made quite large. This large resistance ($\sim$1 GΩ) is achieved by duty cycling. As in [19], the entire OTA is chopped, allowing it to amplify dc inputs despite its ac-coupled topology. This also suppresses the offset and $1/f$ noise of the OTA. The use of chopping also improves the OTA's CMRR and PSRR, at least at low frequencies, thus alleviating one drawback of eliminating the conventional tail current source [21]. A conventional continuous-time CMFB circuit is used [Fig. 7(c)]. To facilitate experimental comparison, extra switches (not shown) were included to short all the replicas of R_{tail} shown in Fig. 7, thus converting the linearized OTA into a PD OTA [Fig. 6(a)] with the same bias current.

D. Nonlinearity Simulation Results

To verify its performance, the linearity of the proposed OTA was simulated and compared to that of conventional and PD OTAs biased at the same tail current. As shown in Fig. 8, the use of a tail resistor results in significantly less non-linearity. Even over process and temperature (−55 °C–125 °C), the proposed scheme is quite robust. As shown in Fig. 9, the worst-case nonlinearity is still 12× better than that of the PD OTA and 40× better than a conventional OTA.

E. Power Scaling and System-Level Simulation

To optimize energy efficiency, the tail current of the OTA used in the 1st stage of the CT$\Delta\Sigma$M was set to 7.6 μA at RT. The 1st stage then consumes $\sim$9 μA, including the biasing and CMFB circuit, whereas its input-referred noise is $\sim$20 nV/$\sqrt{\text{Hz}}$. In comparison, the resistive front end consumes $\sim$17 μA, and its noise level is $\sim$36 nV/$\sqrt{\text{Hz}}$. Neglecting the rest of the CT$\Delta\Sigma$M, this results in a theoretical FoM of 4.4 fJ·K^2.

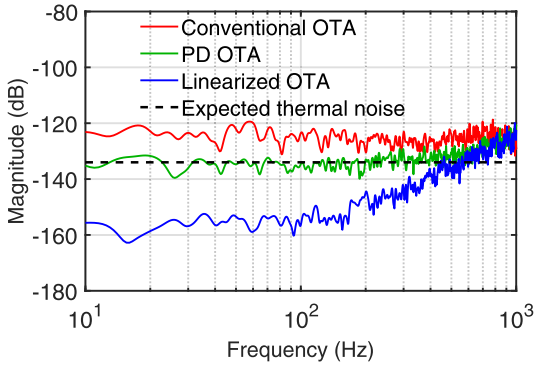

Fig. 10. Simulated $\Delta\Sigma$M bitstream spectrum without noise using the same I_{tail} but different OTA configurations.

Fig. 10 shows the results of system-level simulations to verify the effect of OTA non-linearity on the modulator's IBN. With a four-element FIR-DAC, the maximum swing of I_{err} at RT is about 1/3 I_{tail}. Due to quantization noise folding, the use of a conventional OTA then results in a noise floor that is about 9 dB higher than the expected thermal noise. The improved linearity of a PD OTA reduces quantization noise-folding and brings this to the same level as the thermal noise. After tail-resistor linearization, however, the sensor becomes truly thermal noise limited, as the folded quantization noise drops to about 20 dB below the thermal noise.

In [15], similar suppression of quantization noise folding is achieved by building the 1st stage around a two-stage opamp. However, for similar input noise and output current levels, this almost doubles the required supply current ($\sim$17 μA including the biasing and CMFB circuits).

IV. Sensor Implementation

Fig. 11 shows the block diagram of the proposed temperature sensor. To achieve the required resolution in a reasonable conversion time, a 2nd-order $\Delta\Sigma$M was adopted. A feedforward architecture was chosen to suppress the swing at the output of the 1st stage so that the size of C_{int1} (27 pF) can be minimized. For further area efficiency, C_{int1} is implemented as a high-density metal–insulator–metal (MIM) capacitor, which is located above the WhB. As in [15], the CT$\Delta\Sigma$M's sampling

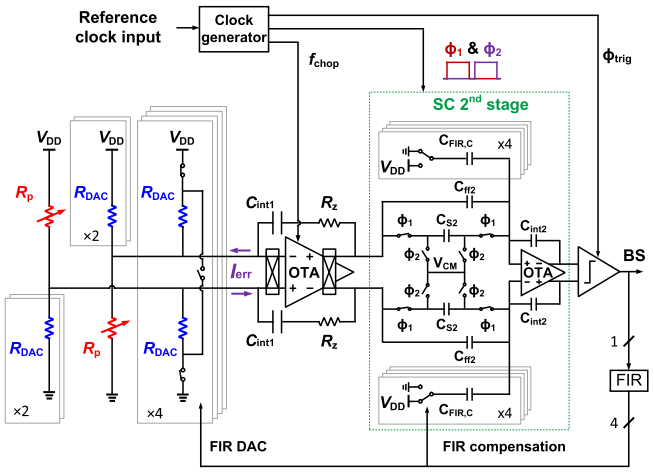

Fig. 11. Simplified system block diagram.

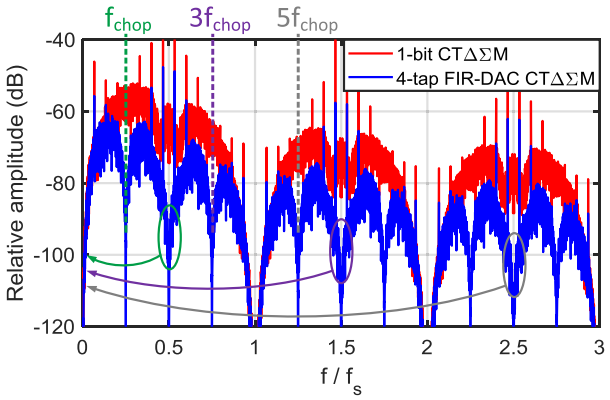

Fig. 12. PSD of the signal at the input of the 1st integrator with a 1-bit DAC and an FIR-DAC, showing the potential noise folding caused by chopping.

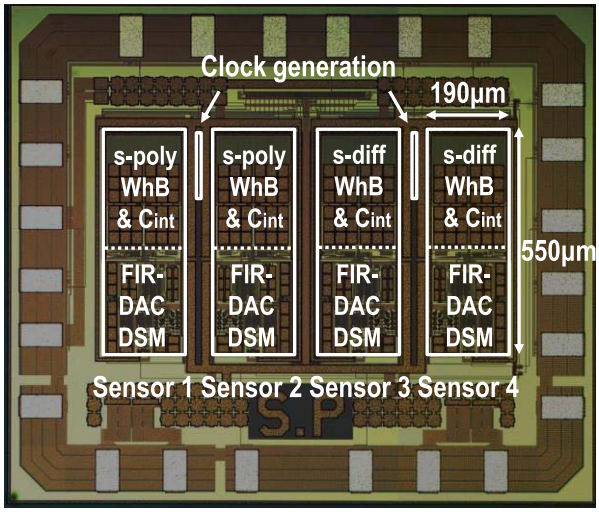

Fig. 13. Die micrograph of the fabricated chip.

frequency (f_s) is set to 500 kHz, which is derived from an off-chip 2-MHz master clock.

The CTΔΣM's 1st stage integrator is based on the tail-resistor linearized OTA introduced in Section III. A delay-line-based pulse generator operating at $2{\cdot}f_{chop}$ is used to duty cycle R_b with pulses of ~4 ns. With $C_b \approx 2$ pF and $R_b \approx 700$ kΩ, the occupied chip area is quite small (<4 × 0.002 mm^2). Meanwhile, the R_b noise is heavily filtered by C_b and is suppressed to ~3 nV/$\sqrt{\text{Hz}}$ at f_{chop} or ~2% of the OTA's total noise. The OTA achieves an 80-dB gain and a unity-gain bandwidth of 18 MHz at the typical corner. To improve its phase response at high frequencies, a zero-cancellation resistor R_z is inserted in series with C_{int}. When chopped at $f_s/4$, frequency components at $f_s/2$, $3{\cdot}f_s/2$, $5{\cdot}f_s/2$, and so on will foldback to DC [22]. Since the FIR-DAC is designed to have notches at exactly these frequencies, no quantization noise folding occurs.

The 2nd stage is implemented as an area-efficient switched-capacitor integrator (C_{S2}, C_{ff2}, and C_{int2}) [15], as shown in Fig. 12. A switched-capacitor FIR-DAC ($C_{FIR,C}$) is inserted to compensate for the delay introduced by the resistive FIR-DAC and stabilize the ΔΣM. Compared to the 1st stage, the noise and linearity requirements of the modulator's 2nd stage are much more relaxed. Hence, the 2nd stage employs a conventional current-reuse OTA, whose tail current is scaled to 1 μA at RT.

V. Measurement Results

As shown in Fig. 13, four WhB temperature sensors were fabricated on the same die in a standard 0.18-μm process. Two employ a silicided-p-poly/n-poly WhB (s-poly WhB), whereas the other two employ a silicided-p-diffusion/n-poly WhB (s-diffusion WhB). Implementing pairs of sensors on the same die allows ambient temperature drift to be effectively rejected by differential measurements. Sinc^2 filters, implemented off-chip for flexibility, are used to decimate the sensors' bitstream output.

Each sensor consumes 27.5 μA/3 μA from a 1.8-V analog/digital power supply and occupies 0.11 mm^2, of which over 50% is occupied by the WhB and the integration capacitors. Four sensors share two clock generation circuits, each occupying 0.003 mm^2. For supply voltages varying from 1.4 to 2 V, both sensors exhibit a supply sensitivity of about 0.04 °C/V at RT, which is mainly limited by the voltage-dependent R_{on} of the trimming/DAC switches.

A. Sensor Characteristic and Inaccuracy After a Linear Fit

After ceramic DIL packaging, 20 samples from one wafer (i.e., 40 sensors of each WhB type) were characterized in a temperature-controlled oven (Vötsch VT7004) from −55 °C to 125 °C. To suppress the effects of oven drift, a calibrated Pt-100 was used as the temperature reference, which, together with the sensors under test, was mounted in good thermal contact with a large metal block [9], [15].

The measured performance of the sensors is shown in Fig. 14. With the same 3-bit coarse trimming code (011), their spread is about ±3% full scale at RT. This means that the trimming code can be simply set by measurements on a single sensor. As expected, the s-diffusion WhB has a higher (~6%) sensitivity than the s-poly WhB.

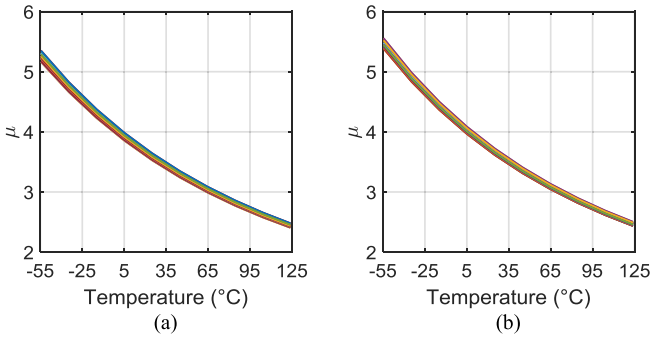

Fig. 14. Bitstream average over the temperature of (a) s-poly WhB sensors and (b) s-diffusion WhB sensors before trimming.

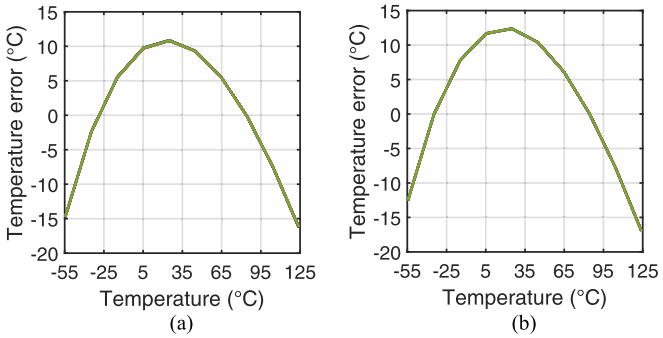

Fig. 15. Temperature error of (a) s-poly WhB sensors and (b) s-diffusion WhB sensors after individual 1st-order fit.

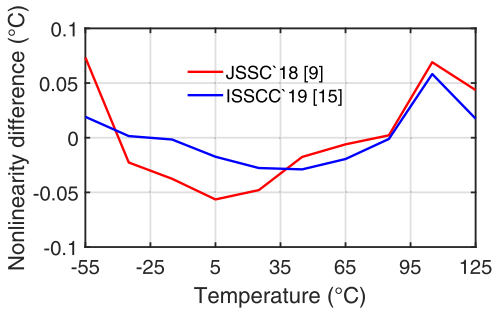

Fig. 16. Differences between the measured systematic nonlinearity over batches.

After an individual linear fit to compensate for process spread, the sensors exhibit a systematic non-linearity (Fig. 15). As in [9] and [15], this can be removed by a fixed 5th-order polynomial, which, in the case of the s-poly bridge, varies by less than 0.1 °C from batch to batch (Fig. 16). This results in a 3σ spread of 0.15 °C for the s-poly bridge and only 0.1 °C for the s-diffusion bridge (Fig. 17). Similar results were achieved when the individual linear fit is replaced by a simpler two-point calibration at −35 °C and 85 °C.

B. One-Point Trim

As discussed in Section II-D, the bitstream average μ is proportional to R_{DAC}/R_p so that a one-point gain trim is enough to correct for the spread in their nominal resistances. As shown in Fig. 18, this results in a residual 3σ spread of 0.65 °C for the s-poly WhB and 0.4 °C for the s-diffusion WhB.

In [23], the sensor's bitstream average was expressed as a number varying between −1 and 1. Denoting this as μ_{ADC}, its

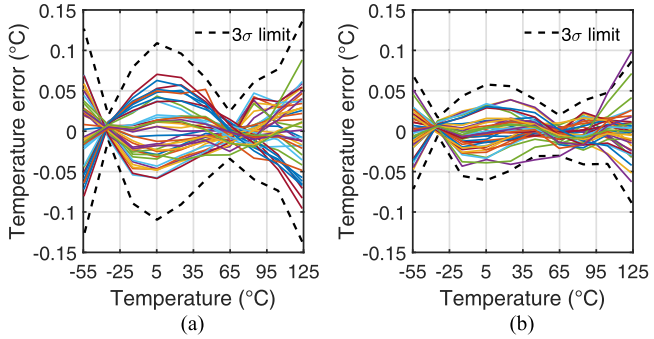

Fig. 17. Residual temperature error of (a) s-poly WhB sensors and (b) s-diffusion WhB sensors after individual 1st-order fit and systematic nonlinearity removal.

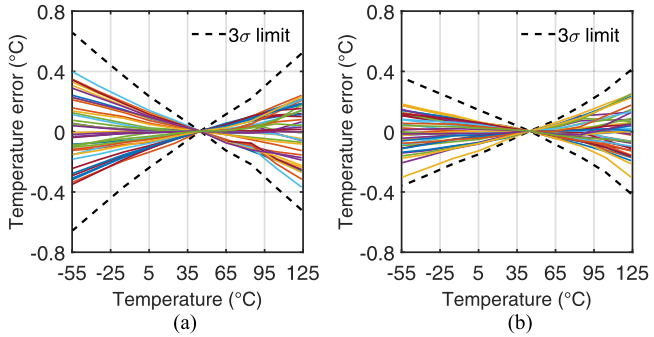

Fig. 18. Temperature error of (a) s-poly WhB sensors and (b) s-diffusion WhB sensors after one-point trim and systematic error removal.

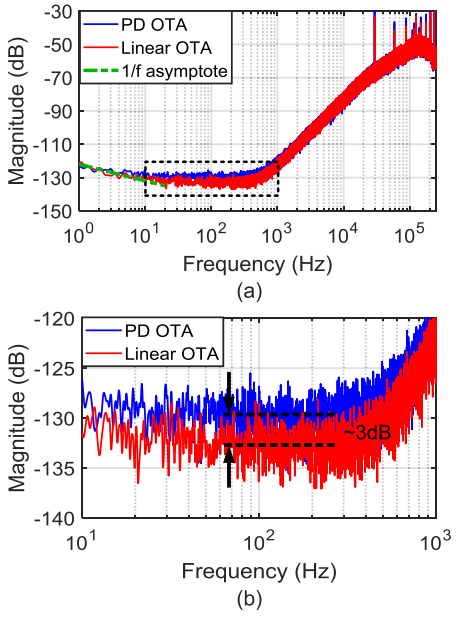

Fig. 19. (a) Bitstream spectrum of the sensor with different OTA configurations (10M samples, Hanning window, 10× averaging) and (b) zoomed-in plot from 10 Hz to 1 kHz.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO PRIOR ART

	Roshan JSSC'17 [1]	Shalmany ISSCC'20 [3]	Jiang JSSC'20 [24]	Pan JSSC'18 [9]	Pan ISSCC'19 [15]	This work	
Sensor type	Dual-MEMS Resonator	BJT	Resistor SC-WhB	Resistor WhB	Resistor WhB	Resistor WhB s-poly	Resistor WhB s-diffusion
CMOS Technology	0.18µm	0.11µm	0.18µm	0.18µm	0.18µm	0.18µm	
Area (mm^2)	0.54	0.2	0.72	0.25	0.12	0.11	
Temperature range	−40°C to 85°C	−35°C to 95°C	−40°C to 85°C	−55°C to 125°C	−55°C to 125°C	−55°C to 125°C	
3σ inaccuracy (°C) (Trimming points)	--	--	0.55 (2)	0.12 (2 *) 1.0 (1)	0.14 (2 *) 0.8 (1)	0.15 (2 *) 0.65 (1)	0.1 (2 *) 0.4 (1)
Supply voltage (V)	1.6	1.125	1.5	1.8	1.8	1.8	
Supply sensitivity (°C/V)	--	--	0.12	0.02	0.03	0.04	
Power consumption (µW)	13000	620	15.6	94	79	55	
Conversion time (ms)	5	0.72	1	5	10	8	
Resolution (mK)	0.02	0.65	2	0.29	0.16	0.16	0.15
Resolution FoM (fJ·K^2) **	40	190	62	40	20	11	10

*1st order fit. ** FoM = Energy / Conversion × (Resolution)^2

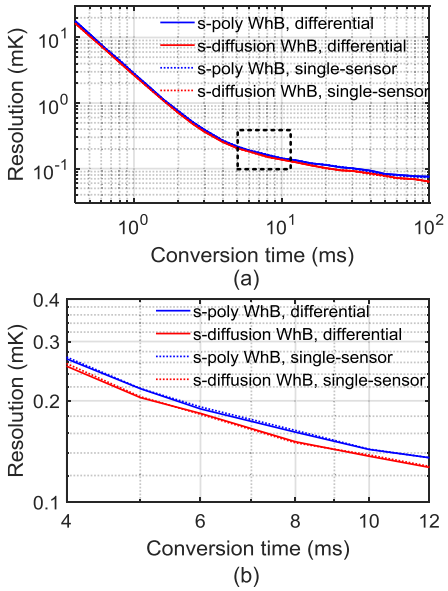

Fig. 20. (a) Sensor resolution based on bitstream data acquired over a 1-s interval and (b) zoomed-in plot from 4 to 12 ms.

relationship with μ is then given by

$$\mu_{\mathrm{ADC}} = 2 - 0.5\ \mu. \tag{6}$$

This formulation does not lead itself to a simple gain trim. Instead, a correlated one-point trim was done based on the observation that after fitting μ_{ADC} to temperature, the resulting 0th- and 1st-order coefficients of multiple samples are strongly correlated [9]. As indicated by (6), however, this correlation is mainly due to the fact that the gain variations in μ affect both the gain and offset of μ_{ADC}. Compared to the simple individual gain trim presented here, correlation-based trimming achieves only slightly (∼10%) better accuracy, at the expense of the batch calibration needed to determine the correlation coefficient.

C. Resolution and FoM

Bitstream spectra (20-s interval, Hanning window, 10× averaging) of the ΔΣM's bitstream output are shown in Fig. 19. Configuring the 1st stage OTA as a PD OTA results in a 3-dB increase in the modulator's noise floor, which agrees with the simulation results shown in Fig. 10. As in [15], the residual $1/f$ noise is mainly due to the non-silicided resistors.

The sensor's resolution is derived via differential measurements, i.e., by calculating the standard deviation of the difference in the output of two identical sensors on the same die [23]. As shown in Fig. 20, with standard deviations computed from bitstream data acquired in a 1-s interval, the s-poly WhB sensor's resolution is estimated to be 160 μK_{rms} in an 8-ms conversion time (T_{conv}). Due to its slightly higher sensitivity, the s-diffusion WhB sensor achieves 150 μK_{rms} in the same T_{conv}. If the drift from single-sensor measurements is removed by assuming it to be a linear function of time [9], the calculated resolution is almost the same, as shown in Fig. 20.

With a 55-μW sensor power, the derived resolution FoMs of s-poly and s-diffusion WhBs are 11 and 10 fJ·K^2, respectively.

D. Comparison to Previous Work

Table I shows the performance of the proposed WhB sensor and compares it with energy-efficient temperature sensors of various types. Its resolution FoM is 2× better than the prior art [15] and is 4 to 20× better than that of MEMS- or BJT-based sensors [1], [3]. Mainly due to the use of an s-diffusion WhB, it is also more accurate than [15] despite occupying less area.

VI. CONCLUSION

An energy-efficient resistor-based temperature sensor has been realized in a 0.18-μm CMOS technology for the temperature compensation of high-performance frequency references. It is built around a Wheatstone bridge that is read out in a self-balanced manner by a continuous-time FIR-DAC ΔΣM. With the help of the improved WhB sensitivity obtained by

using an RCM DAC, and more remarkably, the enhanced linearity of a tail-resistor linearized OTA, the sensor achieves a state-of-the-art resolution FoM of 10 fJ·K^2. In addition, the sensor achieves an inaccuracy of ±0.4 °C (3σ) from −55 °C to 125 °C after a ratio-based one-point trim and systematic non-linearity removal, which improves to ±0.1 °C (3σ) after an individual 1st-order fit.

APPENDIX

In this appendix, the optimum tail resistor value for the 3rd-order OTA nonlinearity suppression is derived, assuming that the transistors are operating in deep weak inversion.

For a single transistor in weak inversion region, its V–I characteristic is exponential, i.e.,

$$I_d = I_s \cdot e^{\frac{V_{gs}-V_{\text{th}}}{nV_T}} \tag{7}$$

where V_{th} is the threshold voltage, I_s is the current at $V_{\text{gs}} = V_{\text{th}}$, n is a process-dependent slope factor, and $V_T = kT/q$ is the thermal voltage.

After applying a differential voltage $\pm\Delta V_g$ on the OTA with a tail resistor, the voltage drop on the tail resistor R_{tail} will increase due to the enlarged total current. Denoting the difference as ΔV_{tail}, the OTA's differential current output ΔI_o can be expressed as

$$\Delta I_o = I_s \cdot e^{\frac{V_{gs0}-V_{\text{th}}+\Delta V_g-\Delta V_s}{nV_T}} - I_s \cdot e^{\frac{V_{gs0}-V_{\text{th}}-\Delta V_g-\Delta V_s}{nV_T}}. \tag{8}$$

Writing its Taylor series up to the 3$^{\text{rd}}$-order term, there is

$$\Delta I_o = I_s \cdot e^{\frac{V_{gs0}-V_{\text{th}}}{nV_T}} \left(\frac{2\Delta V_g}{nV_T} - \frac{4\Delta V_g \Delta V_{\text{tail}}}{2(nV_T)^2} + \frac{2\Delta {V_g}^3 + 6\Delta V_g \Delta {V_{\text{tail}}}^2}{6(nV_T)^3} \right). \tag{9}$$

In order to cancel the 3rd-order nonlinearity, there must be

$$-\frac{4\Delta V_g \Delta V_{\text{tail}}}{2(nV_T)^2} + \frac{2\Delta {V_g}^3}{6(nV_T)^3} = 0. \tag{10}$$

Thus, the relationship between ΔV_g and ΔV_s becomes

$$\Delta V_{\text{tail}} = \frac{\Delta {V_g}^2}{6nV_T}. \tag{11}$$

Alternatively, ΔV_{tail} can be calculated as $\Delta I_{\text{tail}} \cdot R_{\text{tail}}$, i.e.,

$$\Delta V_{\text{tail}} = R_{\text{tail}} \cdot I_s e^{\frac{V_{gs0}-V_{\text{th}}}{nV_T}} \left(e^{\frac{\Delta V_g-\Delta V_s}{nV_T}} + e^{\frac{-\Delta V_g-\Delta V_s}{nV_T}} - 2 \right). \tag{12}$$

Writing its Tylor series up to the 2$^{\text{nd}}$-order term, there is

$$\Delta V_{\text{tail}} = R_{\text{tail}} \cdot I_s e^{\frac{V_{gs0}-V_{\text{th}}}{nV_T}} \left(\frac{-2\Delta V_{\text{tail}}}{nV_T} + \frac{2\Delta {V_g}^2 + 2\Delta {V_{\text{tail}}}^2}{2(nV_T)^2} \right). \tag{13}$$

With $\Delta V_{\text{tail}} = (\Delta {V_g}^2/6nV_T)$, and neglecting the term with $\Delta {V_{\text{tail}}}^2$, (13) can be rewritten as

$$\frac{\Delta {V_g}^2}{6nV_T} = R_{\text{tail}} \cdot I_s \cdot e^{\frac{V_{gs0}-V_{\text{th}}}{nV_T}} \cdot \frac{2\Delta {V_g}^2}{3(nV_T)^2}. \tag{14}$$

Thus, the term $\Delta {V_g}^2$ can be cancelled on both sides, leaving

$$R_{\text{tail}} = \frac{nV_T}{4I_s \cdot e^{\frac{V_{gs0}-V_{\text{th}}}{nV_T}}} = \frac{nV_T}{2I_{\text{tail}}} \tag{15}$$

where I_{tail} is the tail current of the differential pair given a zero differential input.

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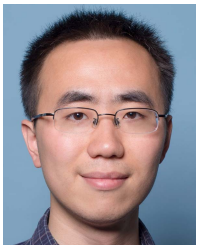

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