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High-efficiency black IBC c-Si solar cells with poly-Si as carrier-selective passivating contacts

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Abstract — In this work, we present the application of poly-Si carrier-selective passivating contacts (CSPCs) as both polarities in interdigitated back-contacted (IBC) solar cell architectures. We compared two approaches to form a gap between the back-surface field (BSF) and emitter fingers. It is proved that the gaps prepared by both approaches are efficient in preventing carriers' recombination. To minimize the reflection losses, we developed a novel modulated surface texturing (MST) structure as anti-reflection coating (ARC). It is obtained by superposing a nano-textured SiO_2 layer on the conventional micro-textured pyramids, which are passivated with a-Si:H / SiN_x:H layers. This approach decouples the light harvesting from the Si surface passivation, which potentially results in the highest possible optical and electrical performances of the solar cells. The reflectance (R) of the MST-ARC is very close to that of the high-aspect ratio nano-structured silicon (*black-Silicon*), achieving R < 1% between 450 and 1000 nm. The J_0 of MST-ARC passivated Si surface (6.3 fA/cm^2) is the same as that of standard a-Si:H/SiN_x:H layers passivated pyramidally-textured Si surface. By applying this novel MST-ARC in our IBC solar cell, the highest J_{SC} observed in a device is 42.2 mA/cm^2 with a V_{OC} as high as 701 mV. A spectral response enhancement in case of the MST-ARC cell is observed over the whole wavelength range with respect to the cell with standard SiN_x:H ARC. The highest efficiency achieved in this work is 23.0%, with the potential to reach 24.0% in short term by using more conductive metal fingers.

Index Terms — poly-silicon, carrier selective passivating contact, light in-coupling, IBC c-Si solar cells.

I. Introduction

The conversion efficiency of c-Si solar cells is continuously increased by means of material innovation with the aim to improve both bulk and surface passivation. Still, minority carriers' recombination velocity at c-Si/contact interface can be further quenched by means of the application of carrier-selective passivating contacts (CSPCs). These technologies are based, for example, on a-Si:H (Silicon Heterojunction, SHJ) [1,2,3,4], doped poly-Si [5,6,7,8], and metal-oxides [9,10]. SHJ technology has recently led to world-record, >26%, interdigitated back-contacted (IBC) solar cells [11]. This is a solar cell architecture with both contacts at the rear side and no optical shading losses are occurring at the front side as is the case for the front/back-contacted (FBC) cell design [12, 13]. A main drawback of the SHJ solar cell is that the temperature stability of the a-Si:H based layers (< 250 ˚C) hinders industrial implementation of this technology for low cost production. Besides that, the limited transparency of the a-Si:H based materials for the short wavelength light induces parasitic absorption losses when they are used on the light facing side of the solar cells. The metal-oxide based passivating contacts, like MoO_x and TiO_x which are transparent, are also rapidly emerging and already enable efficiencies beyond 22% [9,10]. Even though attempts have been made to fire metal contacts on TiO_x [14], such materials still generally exhibit the low thermal stability drawback. Back to 1970s, semi-insulating poly-crystalline silicon (SIPOS)

was developed to passivate and contact Si for PV application [15]. It is a mixture of doped micro-crystalline silicon and silicon oxide (SiO_x). By using such a carrier-selective contact, very good passivation of the c-Si surface was obtained resulting in an V_{OC} of 720 mV for the c-Si solar cell test structure n^+-SIPOS/thin SiO_2/p-type c-Si/thin SiO_2/n^+-SIPOS [15]. Recently, with a similar concept, the poly-crystalline silicon [16, 17, 18,19] and alloys, for example in the form of poly-SiC_x[5,20], have attracted attention in several research groups as a high-temperature stable CSPC structure. They have already been developed and demonstrated solar cells with record-high conversion efficiencies of > 25% (FBC) and > 26% (IBC) [22]. Nevertheless, there is still a restriction that limits the efficiency of solar cells with such materials, which is the high parasitic absorption in the CSPC layers caused mainly by free carrier absorption (FCA), especially for heavily doped poly-Si. Therefore, the best way to use such CSPCs is to apply them on the back side of the IBC solar cells [21,22], even though, the high FCA still induces optical losses, which is potentially solved by the oxygen alloying in the poly-Si films to form poly-SiO_x CSPCs [23,24,25,26], and experimentally demonstrated in the IBC solar cells [27]. Besides the parasitic absorption losses in the solar cells, another main optical loss is the reflection loss from the front side of the cell. In order to minimize such loss, multi-layer anti-reflection coating (ARC) concept is now widely used in the research and industry [28,29,30,31]. Another promising approach to minimize the reflection loss is the application of the so-called black-Silicon (b-Si) technology [32, 33]. However, the passivation for the nanotextured Si surface is more challenging, no matter the b-Si is prepared by dry or wet etching [34,35,36]. In this work, we propose a novel approach to treat the Si surface, for obtaining optical performance like b-Si but with excellent surface passivation.

The goal of this work is to demonstrate - at device level - the application of poly-Si CSPCs in IBC solar cells and the concurrent minimization of reflection losses. We first optimized and simplified the previously developed self-aligned poly-Si CSPCs IBC solar cell process [21] for a more industrially-feasible process. The obtained IBC solar cell results are then presented and discussed. In order to quantify the optical losses, an opto-electrical modelling with TCAD simulation of the IBC solar cells with poly-Si CSPC was performed. With the aim of minimizing the reflectance loss, we report on the development of a modulated surface textured anti-reflection coating (MST-ARC) for application in solar cells. The optical and passivation properties of the MST-ARC are then presented. Finally, the optical enhancement in the IBC solar cell by the application of MST-ARC is presented and discussed.

II. EXPERIMENTAL

A. Poly-Si passivating contacts

Our poly-Si CSPCs consist of an ultra-thin tunnelling SiO_2 layer and a doped poly-Si layer, realized as follows. First, the tunnelling SiO_2 layer is formed on both sides of the wafer by a wet-chemical method. Secondly, the intrinsic amorphous silicon (a-Si, 250 nm) is deposited on both sides of the wafer by means of low-pressure chemical vapour deposition (LPCVD). Ex-situ doping is realized by ion-implantation. Thirdly, a high temperature process is executed to activate and drive-in the implanted dopants, while it is also used to turn the a-Si to poly-Si phase. Finally, a forming gas annealing step is applied for hydrogenating layers and interfaces. The details regarding the process and optimization of the poly-Si CSPCs were previously published [21].

In this work, <100> oriented, 280-µm thick, 1~5 Ωcm, double-side polished FZ wafers were used. The injection-dependent minority carrier lifetime (τ) and the implied open-circuit voltage (iV_{OC}) were measured by a Photoconductance Lifetime Tester using Quasi-Steady State Photoconductance (QSSPC) method [37]. Four-point probe measurements and the transmission line method (TLM) were used, respectively, to obtain the sheet resistance (R_{SH}) of the passivating contacts and the contact resistance (R_C)

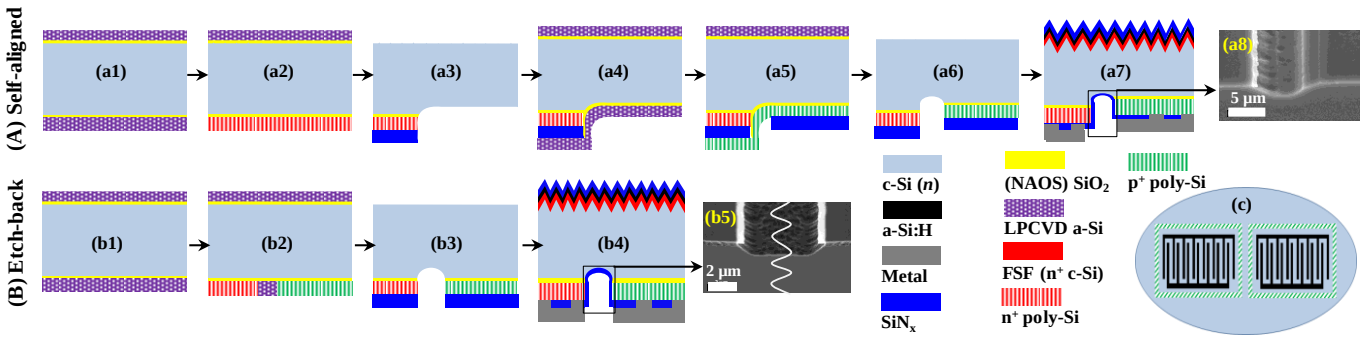

Fig. 1 (A, a1~a7) Schematic representation of the self-aligned process for IBC solar cells; (a8) cross-sectional scanning electron microscope (SEM) picture of the trench between the poly-Si BSF and emitter fingers; (B, b1~b4) schematic representation of the etch back process for IBC solar cells; (b5) cross-sectional SEM picture of the trench between the poly-Si BSF and emitter fingers. (c) Schematic representation of the back side of the wafer, containing two solar cells. For sake of simplicity, the back side SiN_x layer was not drawn.

between such passivating contacts and the evaporated Al. In order to ensure an accurate measurement, the c-Si bulk used for the R_{SH} and R_C measurements exhibited opposite doping type than the one of the passivating contacts under test.

B. IBC solar cells with poly-Si CSPCs

The main steps to fabricate our IBC solar cells with the self-aligned process were presented in our previous work [21]. The schematic description of the process is illustrated in Fig. 1 (A-sequence). A gap between back-surface field (BSF) and emitter is formed during the patterning of BSF and emitter at step-a3 and step-a6 (see SEM image in Fig.1 a8). Due to the BSF patterning etch step at step-a3 (see Fig.1 a3), the BSF and emitter are located at different levels on the back side of the cell surface. And, due to the etch, the c-Si surface shows nano-scale roughness. This surface roughness will influence the passivation properties of the emitter that is deposited on top of it, when compared to that deposited on the polished surface. In this work, we modified the process flow by patterning the BSF and emitter in a different way, ensuring that both BSF and emitter layers are deposited on the polished c-Si surface. Therefore, this modified process flow will enable optimal passivation for both BSF and emitter. By applying this patterning process, shown in Fig. 1 (B-sequence), P and B are locally implanted into the LPCVD intrinsic a-Si layer and an etching step (see Fig.1 b3) is used to separate the BSF and emitter fingers, forming a trench gap between them. After the BSF and emitter patterning steps, both processes (A) and (B) undergo the same front side texturing with mixture solution of TMAH and ALKA-TEX 8 from GP-Solar-GmbH, which results in a pyramid size of less than 3 µm. And then a lightly-doped front surface field (FSF) implantation [38], and a one-step annealing/dopants-activation process are implemented before the metallization. The FSF is then passivated with a-Si:H / SiN_x:H stack. The SiN_x:H layer on the back side is mainly used for optical purpose and to increase the internal reflection. Solar cells on the same wafer are isolated from each other by a 1-mm wide p-type poly-Si area, as in the sketch in Fig. 1(c). The J-V curves of IBC cells are measured with a class AAA Wacom WXS-156S solar simulator. The active area of each cell is precisely illuminated through a laser-cut metallic mask. Series-resistance-free J-V curves and related *pseudo* fill factor (*pFF*) are measured with a Sinton Suns-V_{OC}. The reference cells for both J-V and external quantum efficiency (EQE) measurements were calibrated at the CalLab of Fraunhofer Institute for Solar Energy Systems.

III. RESULTS AND DISCUSSION

A. IBC solar cells performances

The optimization of poly-Si CSPCs and their application into IBC solar cell with the self-aligned process was previously published [21]. The current characteristics of our n^+ poly-Si are: J_0 = 4.5 fA/cm^2, sheet resistance (R_{SH}) = 89 Ω/□, and contact resistance with Al $R_{C,TLM}$ = 0.9 mΩ·cm^2; while the p^+ poly-Si passivating contacts show J_0 = 11 fA/cm^2, R_{SH} = 122 Ω/□, and contact resistance with Al $R_{C,TLM}$ = 0.3 mΩ·cm^2. The passivating a-Si:H / SiN_x:H stack deposited on the FSF yields J_0 = 6.5 fA/cm^2 [39]. The performance of IBC cells prepared by the self-aligned approach (cell #1, #2, and #3), shown in Fig. 1(A), are listed in Table 1. The highest efficiencies so far, prepared with the self-aligned process, reached by us are 22.5% for a 0.72-cm^2 large cell and 21.9% for a 9.0-cm^2 large cell. With this approach, the highest V_{OC} and *FF* obtained (on different devices) are 709 mV and 80.0%, respectively.

Table 1. Performance of IBC solar cells with poly-Si CSPCs, prepared with self-aligned process (Fig. 1 (A-sequence)) and etch-back process (Fig. 1 (B-sequence)).

Cell	Area [cm^2]	V_{OC} [mV]	$J_{SC,\ I\text{-}V}$ [mA/cm^2]	*FF* [%]	η [%]
1[a]	0.72	709	40.7	76.4	22.1
2[a]	0.72	681	41.3	80.0	22.5
3[a]	9.00	696	39.6	79.6	21.9
4[b]	1.00	682	41.6	81.0	23.0
5[b,c]	2.00	701	42.2	77.8	23.0

(a) IBC cells from different runs with the same self-aligned process flow as in Fig. 1 (A-sequence); (b) IBC cells from different runs with the same process flow as in Fig. 1 (B-sequence); (c) IBC cell with MST-ARC, see Section III (c).

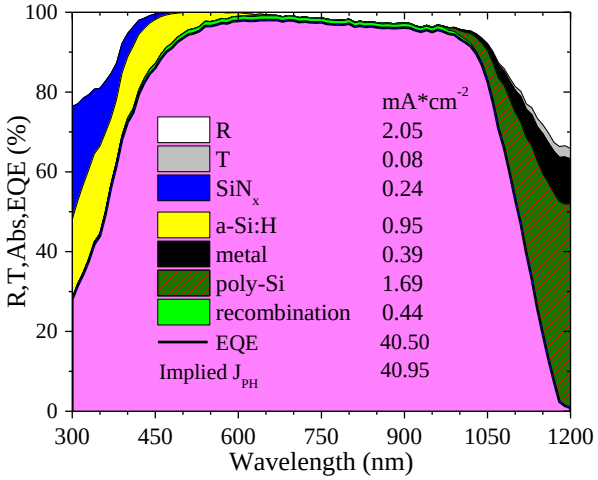

Fig. 2 Measured EQE and estimated losses of Cell #1, reported in terms of mA/cm^2 and integrated between 300 and 1200 nm.

As mentioned in Section II (B), in the self-aligned process, the passivation of the emitter is deteriorated by the nano-roughness of the c-Si surface owning to the wet-etching process in step-a3 (shown in Fig.1 a3). Meanwhile, the two times poly-Si layer deposition increases the complexity of the whole process. We therefore developed an etch-back process (Fig. 1 (B-sequence)). In this process, the LPCVD poly-Si layer for both BSF and emitter is deposited in one single step on polished c-Si surface. The trench between BSF and emitter is obtained by wet-etching with a photolithography-patterned SiN_x protective layer on top of both BSF and emitter. The solar cells prepared with this approach (cells #4 and #5) are also reported in Table 1. For both cells, the efficiencies are 23.0%. *FF* = 81% obtained for the 1-cm^2 wide cell indicates that the well-passivated 20-µm wide gap is large enough to isolate the BSF from the emitter fingers. For both approaches shown in Fig. 1, FF values of 80% or higher have been obtained, proving that both processes allow for very well separated BSF and emitter fingers, thus minimizing shunting losses.

The EQE curve for Cell # 1 and its loss analysis based on TCAD opto-electrical simulation are shown in Fig. 2. The validation of the modelling is presented in our previous work [40]. A perfect match is obtained between the measured and the simulated EQE spectra. Based on Fig. 2, main losses come from two aspects: (1) the high FCA in the n^+/p^+ poly-Si finger regions at the rear of the cell, and (2) the

reflection loss from the front side of the cell. In order to quench the poly-Si FCA optical loss, thinner and more transparent p^+ and n^+ layers based on poly-SiO_x are proposed [23,24,25,26,27] to replace the > 250-nm thick poly-Si films in the role of CSPCs. It was demonstrated that such CSPCs based on poly-SiO_x and their application in solar cells can enhance the infrared light response of the IBC solar cells [27]. Here we report on how we minimized the reflection loss arising the front side of the solar cell. We propose a novel approach that quenches the reflectance spectrum to values as low as those from b-Si [34], while maintaining state-of-the-art passivation for the FSF. This approach is achieved by superposing a nano-textured SiO_2 layer on top of the passivating stack, coating the pyramidally-textured front Si surface. In the following section, the preparation, optical performance and the passivation properties of such ARC will be discussed.

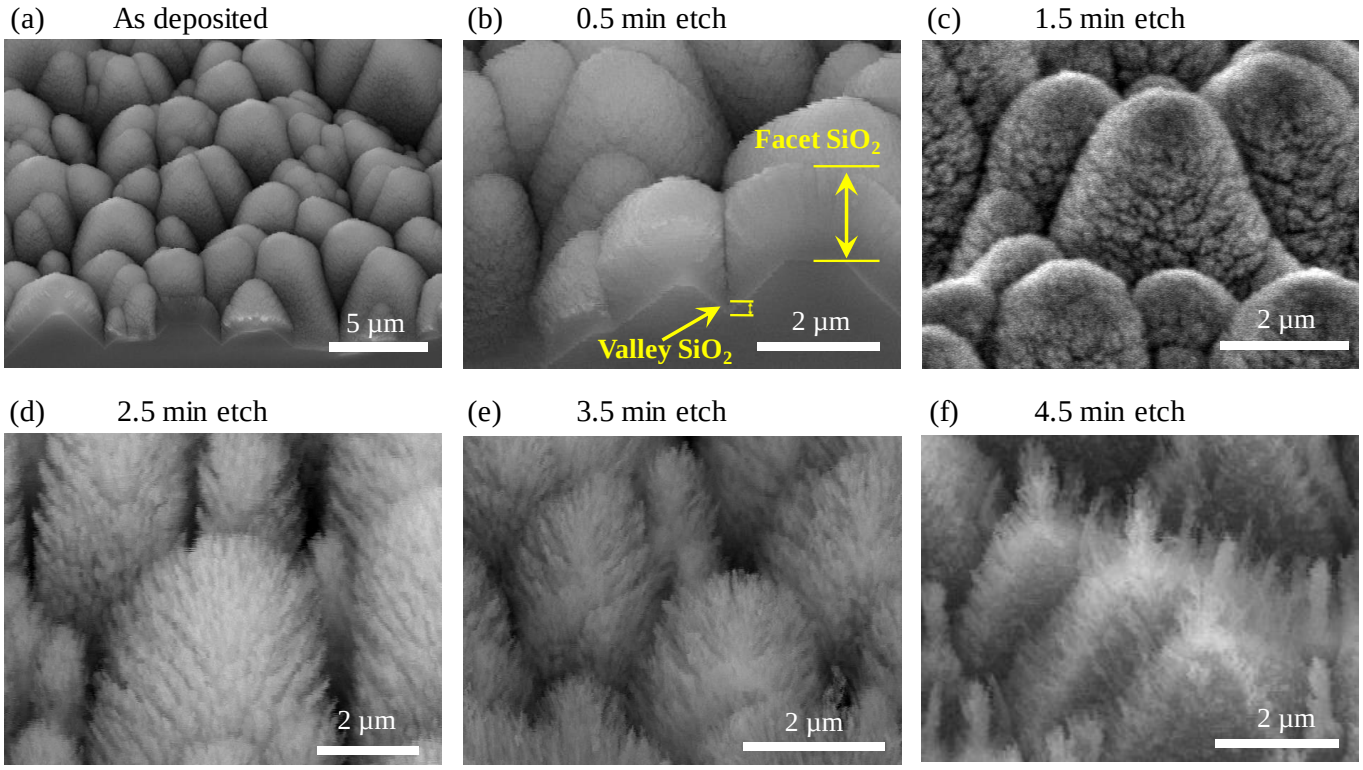

Fig. 3 SEM pictures of the MST-ARC passivated Si surfaces, with (a) the as deposited SiO_2 layer and (b~f) the wet-etched SiO_2 as function of HF etching time.

B. Modulated surface textured passivation stack

On the front side of the IBC solar cell of this work, an a-Si:H (5 nm) / SiN_x:H (75 nm) stack is used as passivating structure for the random pyramidally-textured FSF. Even though the SiN_x:H layer acts as ARC, a high reflection loss can still be observed, as discussed in Section III (A), see Fig. 2. To drastically reduce such a loss, we superpose high-aspect ratio nano-features on the micro-scale pyramids at the front side of the c-Si bulk. This is what we call modulated surface texturing (MST [41,42]), which allows for broad-band anti-reflective effect and efficient light scattering in the cell. In addition, we embed in our MST-ARC high-quality passivation properties. It is fabricated by coating the SiN_x:H ARC layer with a 2-µm thick low-temperature PECVD SiO_2 layer, followed by wet etching in HF to form the nano-textures [43]. The surface morphology of the samples as a function of the HF (0.55%) dip duration is shown in Fig. 3. As etching time increases, nano-meter scale SiO_2 needles appear on the surface. The needles exist until the SiO_2 layer is totally etched away. The samples shown in Fig. 3 are symmetrical passivation test samples endowed with FSF and a-Si:H / SiN_x:H / (nano-textured) SiO_2 as passivation

stack. Compared to the standard a-Si:H / SiN_x:H passivation stack for FSF (J_0 = 6.5 fA/cm^2), the obtained $J_{0,FSF/a\text{-}Si:H/SiNx:H/SiO2}$ is 6.3 fA/cm^2 after the SiO_2 layer deposition, see Fig. 3 (a). This indicates that the deposition of the SiO_2 does not affect the passivation properties at the FSF. Increasing the etching time until 3.5 min, the passivation keeps the same. After etching for 4.5 min, the J_0 increases to 8.3 fA/cm^2, which is attributed to the too thin SiN_x:H layer in the valleys between pyramids. In fact, it can be seen from Fig. 3 (b) that the SiO_2 layer is much thinner in the valleys than on pyramid facets and tips. When the HF dip is operated, the SiO_2 layer in the valley is etched away, leaving exposed the passivating SiN_x:H layer to be unintentionally thinned.

Measurements of reflectance (R) are conducted on these samples to evaluate their light in-coupling and trapping enhancement. The results are shown in Fig. 4 and compared to the reference sample with 75-nm thick SiN_x:H as ARC on randomly pyramid textured Si surface and to a b-Si sample, which is prepared by reactive ion etching, similarly to previously reported [33,42]. All MST-ARC samples with nano-textured SiO_2 layers exhibit a lower reflectance than that for the SiN_x:H ARC reference sample, over nearly the whole wavelength range, except at around 580 ± 70 nm, where the 75-nm SiN_x:H ARC shows its minimal reflectance. In addition, MST-ARC samples etched for 1.5 min and 2.5 min perform very closely to the b-Si reference, achieving R < 1% between 450 and 1000 nm. Compared to b-Si technology, the approach proposed in this work is superior from passivation perspective, owing to the fact that the optical enhancement is decoupled from the excellent FSF passivation ensured by the a-Si:H / SiN_x:H stack. Actually, most of the state-of-the-art passivation technologies used in the academy researches and industries could be used in place of a-Si:H / SiN_x:H stack, such as Al_2O_3 and Silicon-Heterojunction (a-Si:H alloys) passivation layers.

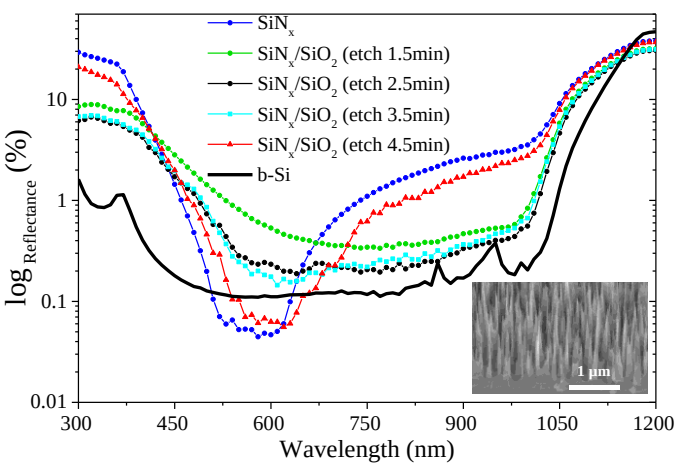

Fig. 4 Log-scale reflectance spectra of symmetrical samples endowed with MST-ARC shown in Fig.3 (c, d, f), or SiN_x:H ARC. A b-Si sample prepared by reactive ion plasma etching is used as reference, whose SEM picture is shown in the inset.

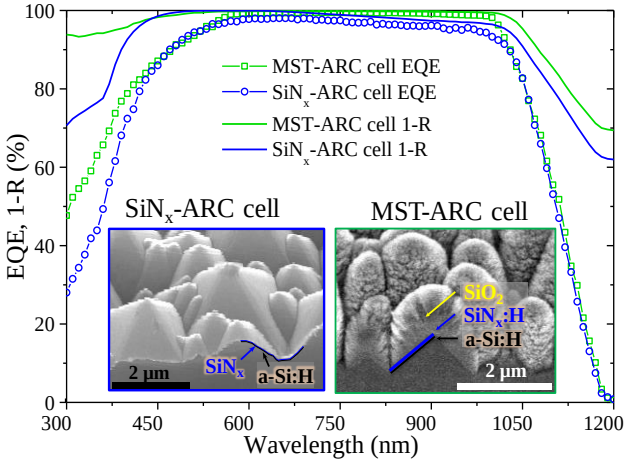

Fig. 5 The EQE and 1-R curves of solar cells with SiN_x:H ARC and MST-ARC (prepared with HF, 0.55%, etching time for 1.5 min). The insets are the cross-sectional SEM images of the front surface of both cells.

C. IBC solar cells with MST-ARC

In order to realize this optical enhancement in solar cells, we applied the MST-ARC process steps in an IBC solar cell fabricated with the etch-back process (see Fig. 1 (B-sequence)). In this solar cell, the morphology of the cell front side is the same as that shown in Fig. 3(c) for ensuring an optimal FSF passivation. The solar cell result is listed in Table 1, as cell #5. A J_{SC} as high as 42.2 mA/cm^2 is obtained from the I-V measurement, which is mainly attributed to the enhanced light management exhibited by the MST-ARC. With this

novel ARC approach, the solar cell surface is as black as those obtained by the b-Si approach [34]. However, as mentioned above, since the optics are decoupled from the passivation of the Si surface, our MST-ARC opens up more opportunities to optimize independently the passivation and the light management. Therefore, a solar cell V_{OC} of 701 mV was achieved, which is higher than the one reported for the 22.1% state-of-the-art black silicon solar cell [34]. Currently, the conversion efficiency of this cell is 23% and is limited by the conductivity of the thin e-Beam evaporated Al fingers. The EQE curve of cell # 5 is shown in Fig. 5 alongside that of cell # 1 (pyramidally-textured c-Si surface covered with SiN_x as ARC) as reference. Compared to cell # 1, cell # 5 shows higher spectral response over nearly the whole wavelength range, which is more obvious for wavelengths below 450 nm and above 800 nm. A further optimization of the nano-textured SiO_2 layer thickness and morphology, and of the underneath SiN_x:H layer thickness can further lower the reflection in the shorter wavelength range. Also, replacing a-Si:H / SiN_x:H passivating stack for the FSF with non-absorbing passivation layers, such as a single SiN_x:H layer, will avoid the parasitic absorption otherwise due to the a-Si:H. Therefore, a further enhancement in the shorter wavelength range response is expected.

IV. CONCLUSION

In this paper we presented the ion-implanted poly-Si with tunnelling SiO_2 as carrier selective passivating contacts (CSPCs) for application in IBC solar cells. Two different patterning approaches are used to pattern the poly-Si layers (BSF and emitter). Both approaches allow for very well separated BSF and emitter fingers with a well-passivated gap between them, thus minimizing shunting losses. We developed a novel MST-ARC approach for solar cell application, which is achieved by superposing the nano-textured SiO_2 layer on the a-Si:H / SiN_x passivation layers coating micro-scale pyramids. This approach decouples light management from surface passivation, since it enables similar level of low reflectance with respect to that of b-Si reference, while maintaining as high-quality passivation properties as in case of the random pyramidally-textured Si surface. A very high J_{SC} value of 42.2 mA/cm^2 was obtained in the IBC solar cell with such MST-ARC. The EQE curve of this cell shows the spectral response enhancement over the whole wavelength range with respect to the standard SiN_x ARC. The best IBC solar cells obtained in this work shows an efficiency as high as 23.0%, with the potential to reach 24% by solving the limits of metal finger conductivity.

V. ACKNOWLEDGEMENT

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