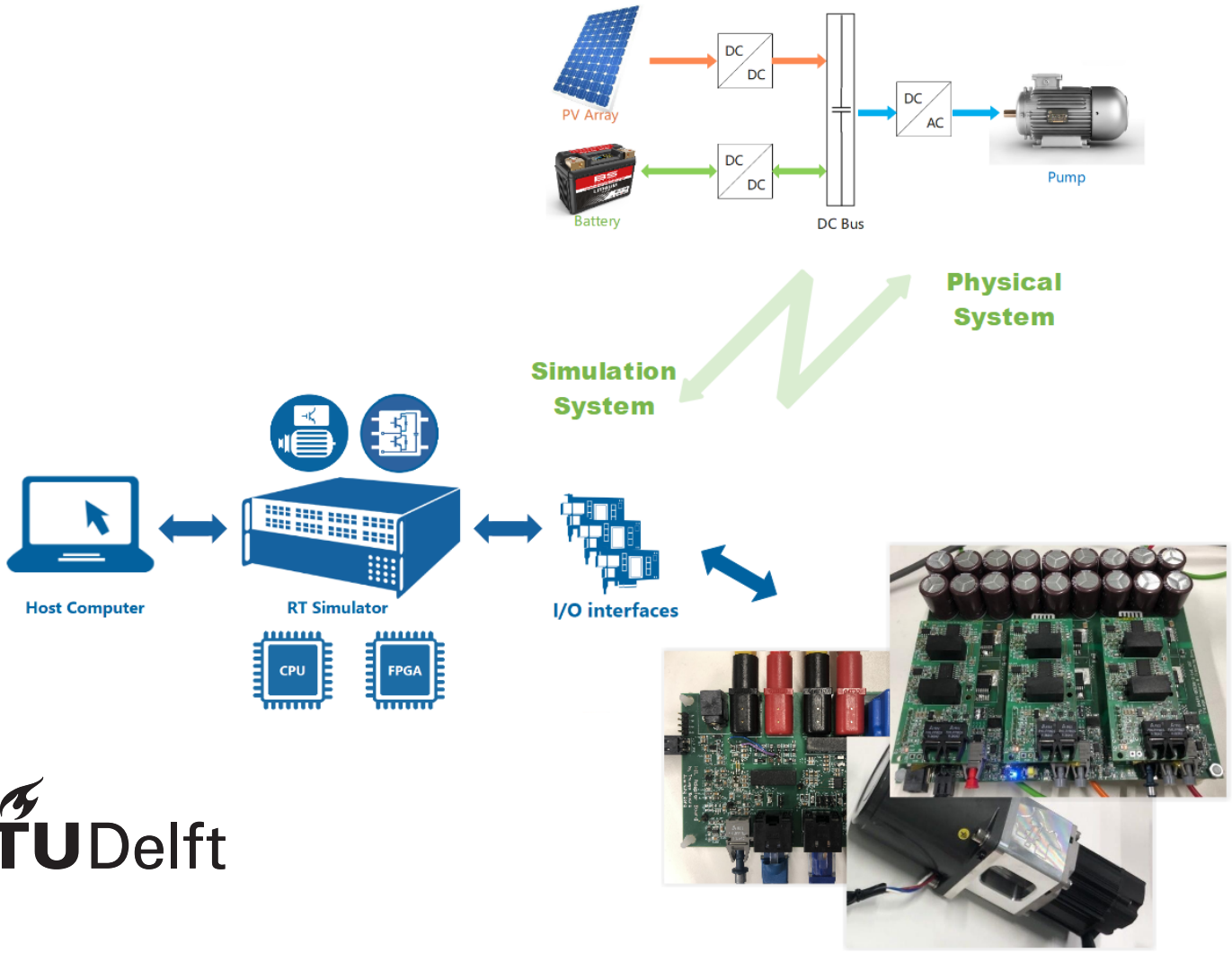
Hardware-in-loop Emulation of a Solar Array Fed Water Pumping System

MSc. Thesis Report

Yujie Liu



TU Delft

Hardware-in-loop Emulation of a Solar Array Fed Water Pumping System

MSc.Thesis Report

by

Yujie Liu

to obtain the degree of Master of Science
at the Delft University of Technology,
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ABSTRACT

Solar array fed water pumping system is a good approach for water management and agriculture purpose. PV panels highly depend on unpredictable environmental conditions, as a result, the development of a PV system is with more technical challenges. System-level simulation on a desktop computer has limitations, such as uncertain accuracy of the models, unable to test the system real-time behaviour and the communication and measurement of sensors that are required on physically implementing the system. On the other hand, implementing tests for a physical system has defects like high cost, unsafety and long development cycle. Therefore, based on the OPAL-RT real-time simulation platform OP4510, this project has implemented the real-time hardware-in-loop (HIL) simulation of the solar array fed water pumping system. In the meanwhile, the proposed HIL emulation system provides a virtual testing environment in the ESP Lab for solar panels, batteries or electrical machines.

To begin with, the different structures and their merit and demerit of common PV-pump systems are discussed. The two-stage PV energy conversion system structure with battery is decided to be used. Delft, the Netherlands, is selected as the design target. Then, based on the local environment and the system load demand, the PV array, the battery capacity and other system parameters are decided. The perturbation and observation (P&O) MPPT method is used to extract the maximum power from the PV array. The double closed-loop control is implemented to control the battery, regulating the DC bus voltage and limiting the battery current. The open-loop scalar control is implemented to control the motor speed. To make the system be able to operate stably and safely under extreme conditions, a central management control algorithm has been proposed.

Next, the system software-in-loop (SIL) simulation has been implemented as the preparation of the HIL simulation. In SIL simulation, the system plant models, power converter models and controller are all executed in the real-time simulator. The battery and PV model is programmed in the CPU. The motor model and the simulated controller are programmed in FPGA and be executed at a higher frequency. The system model and control algorithm has been validated.

Subsequently, the battery subsystem and the motor subsystem are replaced by real hardware. The communication between the real-time simulator and the external hardware is done through the I/Os of the OP4510 simulator. The measurement board is used to measure the target signals and then the signals are transferred to the simulated controller. The generated PWM signals are transferred to the real power converters to achieve the closed-loop control. Finally, the HIL testing of the system is completed.

The simulation results show the expected behaviour of the motor speed, PV output power and the charging and discharging of the battery. In the HIL simulation, the simulated models can interact with external hardware completing the system-level real-time simulation. The built PV-pump system can adjust the system operation mode according to the current system performance and environmental condition, eventually to make sure the effective and stable operation of the system. Finally, the system loss has been analyzed.

ACKNOWLEDGEMENTS

I would like to express my sincere appreciation to my supervisor Dr.Jianning Dong and Dr.ir.Thiago Batista Soeiro for their valuable advice and generous guidance. They gave me many valuable suggestions and valuable feedback when I faced difficulties, and their help has kept me continuously motivated to work on this project for seven months.

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Yujie Liu
Delft, August 2021

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1 INTRODUCTION

With the depletion of fossil energy and the growth of environmental problems such as global warming that follows the use of fossil fuel, more and more people pay attention to renewable energy. Renewable energy sources, such as wind, solar, tidal, are becoming more popular. Within all these renewable energy technologies, because of no toxic emissions, low maintenance cost and no greenhouse gases emissions, solar photovoltaic (PV) is becoming one of the most used renewable energy sources [7]. The PV technology is introduced in the late 80s and get popular in the 90s [8]. Until today, PV technology is still developing. After all these developments, the general efficiency of PV panels is improved to around 15-20%. For the laboratory conditions, the efficiency can even reach 42%.

PV is generally used in remote areas as a stand-alone power, providing electricity for lighting, remote buildings and water irrigation pumps, etc. For the field of rural areas, a standalone solar array fed water pumping system is a good approach for water management and agriculture purpose. Renewable energy source highly depends on environmental conditions, like the variation of the solar energy and the variation of the environment temperature, which are un-predictable and bring the system with more technical challenges [9]. The system is required to operate under restrict and variable power conditions as the temperature and solar radian are not stable [10].

These challenges can be surmounted by the effective design of the control system and architectural design. With the help of simulation software, like MATLAB, the simulation of a PV water pumping system can be designed and tested [11]. However, the system-level simulation on a desktop computer has limitations. Parameters for the models are all be estimated, so the accuracy of the simulated models is uncertain. For instance, a more realistic power converter includes diode loss, switching loss and resistive losses on inductors and capacitors [12]. On the other hand, implementing the system physically involves more research points, for example, implementing a microcontroller, measurements of target signals by sensors and the communication between different portions of the system. A PV pumping system was designed and operated in Sohar, Oman in [13]. The system investment capital cost was 2400 USD and the system performance was tested under the local environment at that time. Implementing tests for a physical system involve many factors, such as safety issues, costs and required equipment, etc. Validating the real-time behaviour of the controller when the software-hardware integration is completed makes the defects of the controller found at this stage be more expensive and difficult to remedy. Due to the uncertainty of the environment, to ensure the robustness and stability of the designed system, system operation tests under extreme conditions should be implemented. However, this kind of testing may be impossible or difficult to carry out. The test environment is not safe and it will greatly increase development costs when any failure occurs.

At early testing of such a control system, one of the most cost-effective development methods is to implement real-time hardware-in-loop (HIL) simulations. In HIL simulation the plant model will run on a real-time computer and be executed fast enough to simulate the real-time behaviour of the actual plant hardware. Virtual plants are more costs friendly, safer when operating under extreme conditions and with higher flexibility. So, by implementing the real-time HIL simulation, the

potential risks can be prevented and the develop-cycle of a control system can be reduced since the system performance can be tested before the final hardware design is complete.

A real-time simulation platform from OPAL-RT, the OP4510 simulator, is available in the Electrical Sustainable Power (ESP) Lab. This real-time simulator operates with a FPGA and four CUP cores. It is also equipped with digital and analog I/O blocks that necessary for HIL simulation.

Therefore, this project is aiming to implement the HIL emulation of a solar array fed water pumping system. In the meanwhile, the proposed HIL emulation system can provide virtual testing, such as for testing of real solar panels or batteries without implementing a real pumping system in the lab.

1.1 RESEARCH OBJECTIVES

Generally, this project is aiming to build a standalone PV system from the ground up. In the meantime, developing and providing a testing platform for PV panels, batteries, electric machines or control algorithms for these targets. Therefore, this system was not designed for operating under certain conditions and environments. The design of the system focused on the flexibility of its application, but not focused on finding the optimal solution of system sizing either on improving the system operation efficiency.

For the simplest solution of a PV fed water pumping system, a PV panel and a motor would be enough. However, in order to provide testing for more objectives the energy storage system (battery) is included as well. Any part of the system, the PV array, the battery or the motor, is able to be the external hardware implementing the HIL simulation and be tested in a virtual system. In summary, the research objectives of this thesis project are:

1. Implementing the real-time HIL simulation of a PV pumping system. The system is able to extract maximum power of the PV array, control the speed of an induction motor and keep the bus voltage stable by controlling the battery.

2. Providing a virtual testing environment for PV panel, electrical machine and battery. Each part of the system, any plant or power converter, is able to be selected either as a simulated part in the real-time simulator or as a hardware part running external the simulator.

There are also some conditions and limits set:

1. The used plant models, the PV array model and the battery model, are built based on the pre-existing models from Simulink/Simscape library. Designing and building the PV array model and the battery model is not one of the objects of this project.

2. The implemented space vector modulation (SVPWM) for the three-phase inverter is not one of the objects of this project. Implementing the SVPWM is with the help of the pre-existing models from the Simulink/RT-EVENTS library.

1.2 RESEARCH QUESTIONS

For the thesis objectives mentioned previously, the research questions are listed in the following:

1. To let the system effectively and stably operate at the assumed location, how to design the system parameters? And how to design the control strategy for the system?

2. For the system model simulation, the controller and the power converters run at different frequencies, how to let the whole system synchronized? How to model and simulate the system in real-time?

3. How to let the simulated models and the external hardware interact with each other and implement the HIL testing in the ESP Lab environment?

1.3 RESEARCH METHODOLOGIES

A target location has been chosen to place the proposed system. Based on the research objective to design the system structure and control algorithm. Based on the annual average hourly solar irradiance data and load demand to design the system parameters.

Use Simulink-based modeling and the OP4510 real-time simulator from OPAL-RT to build the real-time simulation.

To integrate the power converters and the real-time simulator, use a developed measurement board, digital I/Os of OP4510, and optical link.

1.4 THESIS OUTLINE

The thesis report consists of 6 chapters.

The first chapter introduces the project background and defines the project research objectives.

Chapter 2 presents the different structures of general PV-pump systems discusses their merit and demerit. The mathematic models of the PV array, the battery, and the pump are described. System parameters include PV array, battery capacity are decided. Then, the control algorithms for the PV array, the battery, the motor, and the central management are determined.

In chapter 3, the system software-in-loop (SIL) simulation is implemented. The real-time simulation concept and the OP4510 simulation platform are introduced. The real-time models of the plants, the power converters, and the induction machine are built. Then, the simulated controller is built, and the PI controller parameters are designed.

In chapter 4, the system HIL simulation is implemented. The description of the system's external hardware is presented. The communication between the simulated model and the external hardware is realized.

Chapter 5 presents the system SIL and HIL simulation results. The effectiveness of the system has been proved. The system mode switching performance under extreme conditions is validated.

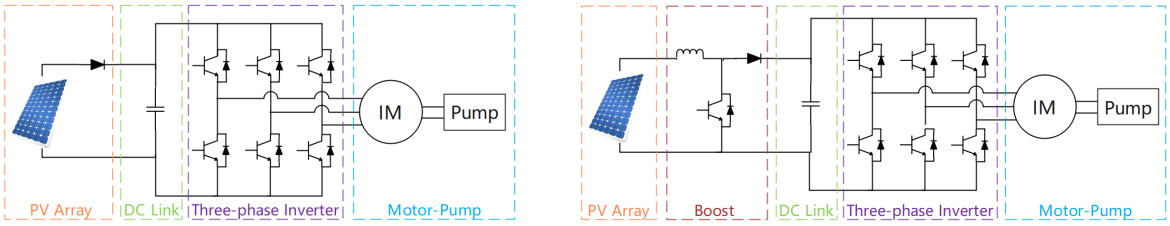
Chapter 6 summarized this thesis and gave the conclusions and the recommendations of the project.

2 OVERVIEW AND SIZING OF A SOLAR ARRAY FED WATER PUMPING SYSTEM

2.1 OVERVIEW OF THE SOLAR ARRAY FED WATER PUMPING SYSTEM

In the solar array fed water pumping system, the PV array converts solar energy into DC power and provides a power source for the entire system. The motor is powered to drive the water pump to fetch water from any water source. Many ways can be used to classify solar array feedwater pump systems.

According to the system power conversion stage, the system can be divided into the two-stage PV energy conversion system that includes a front-stage boost converter and the single-stage PV energy conversion system that PV array directly connected to an inverter. Figure 2.1 shows the schematics of the two-stage and single-stage PV energy conversion system.



(a) Single-stage **(b)** Two-stage

Figure 2.1: Schematics of the two-stage and signal-stage PV energy conversion system [1].

For the two-stage PV pumping system, the DC power from the PV array firstly go through a boost converter, then output AC power through a DC-AC inverter. For the single-stage PV pumping system, the DC power generated by the PV array is directly inverted by a DC-AC inverter. In this kind of structure, both the maximum power extraction of the PV array and the motor control is achieved through the inverter. In [1], a single-stage PV pumping system without a battery is proposed. The system is easy to implement and compact and able to pump the water approximately 104,504 litres in 9 hours [1].

Based on whether the system includes an energy storage subsystem, the system can be divided into a PV pumping system with a battery and a PV pumping system without a battery. Figure 2.2 and Figure 2.3 present the schematics for these two kinds of structures. A system with an energy storage subsystem is stable, reliable and flexible for different operation conditions. However, it also brings the defects of a more complex system configuration, higher costs for installation and maintenance. In [14], a PV pumping system without a boost converter and with a battery is proposed. In this system, the maximum power extraction of the PV array is achieved by either the three-phase inverter or the bidirectional dc-dc converter. Only two of the three subsystems are able two operate at a time, the

PV/battery powers the motor or the PV array charges the battery, which makes the system has low flexibility.

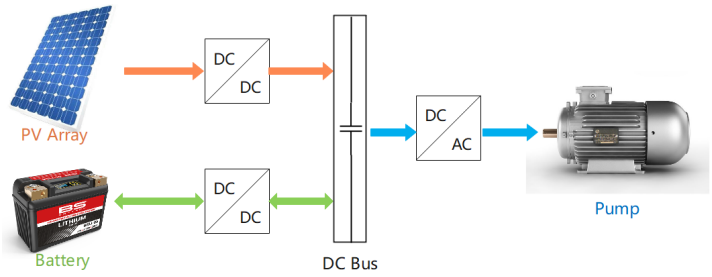


Figure 2.2: PV pumping system with a battery.

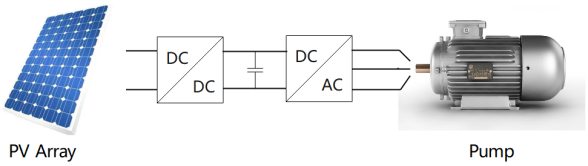


Figure 2.3: PV pumping system without a battery.

Considering this project is aiming to provide a hardware-in-loop test platform as well, in order to have higher flexibility for people to test their PV panel, battery or machines, the proposed standalone solar array fed water pumping system in this project uses the two-stage structure including a battery.

2.1.1 PV Array Subsystem

In a solar power plant, photovoltaic cells' performance is affected not only by the internal characteristics of the photovoltaic cell itself but also by the environment to be operated, such as solar irradiance, temperature, and load etc. Under different conditions, the PV panel exhibits a unique maximum power point. From the P-V curve of a PV array, as shown in Figure 2.4, the slope of the curve is positive on the left of the maximum power point, negative on the right of the maximum power point and zero at the maximum power point. It is essential for a solar power plant to find the optimal working condition and extract the maximum energy during its operation. The control strategy that achieves the maximum power point operation of a PV array is called maximum power point tracking (MPPT). Many MPPT technologies have been well established. Ten different MPPT techniques have been compared in [15], regarding the MPPT implementation costs. Based on PSIM and Simulink, a comparison of hill climbing (HC), incremental conductance (INC), perturb-and-observe (P&O), and fuzzy logic controller (FLC) MPPT methods has been done to evaluate the control responses under rapid weather changing conditions in [16]. In this project, the P&O technology is implemented to achieve the maximum power extraction of the PV array.

2.1.2 IM Subsystem

In a solar array fed water pumping system, the motor plays an important role. Because of its reliability, low maintenance requirement, reliable and more flexibility of control, the induction machine

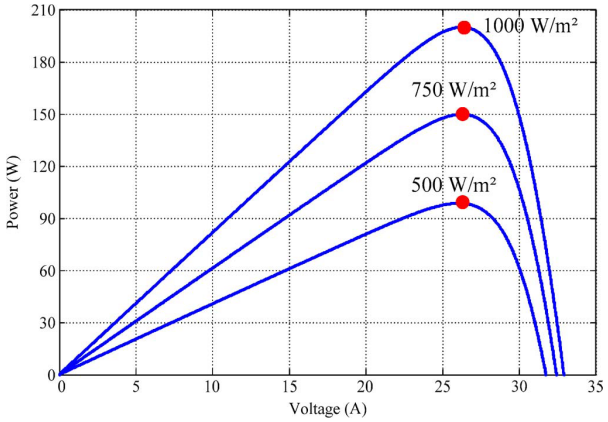


Figure 2.4: PV power characteristic at different irradiance [2].

is generally used in home and industrial applications [8]. Field-oriented control (FOC), also called vector control, achieves the control of IM by controlling the excitation current and torque current of the motor based on the principle of magnetic field orientation, eventually converting the control of an AC machine to the control of a DC machine. This method requires high computational work and good knowledge of flux orientation. Another advanced control method is the direct torque control (DTC) method. In this method, the stator flux and electromagnetic torque are directly controlled by the stator field orientation and the analyzing of the space vector, do not require complex coordinate transformation. However, in the pumping system, high precision control and soft transient performance are not required [17]. As a result, due to the simple implementation and low cost, the scalar control (V/f control) is selected in this project to control the speed of IM.

2.1.3 Battery Subsystem

Battery plays an essential role for a standalone PV system. The main objective of the battery is to help provide sufficient power to the load regardless of the solar irradiance. According to the current irradiance, the battery operates in either the charging mode or the discharging mode. When the power generated by the PV array is insufficient for the load demand, the battery will operate in discharging mode to supply the load. When the PV array generates excess energy, the battery will operate in the charging mode to store the excess energy. By charging and discharging the battery, the bus voltage is kept constant and regulated to be the reference value.

2.2 SYSTEM MODELLING

2.2.1 Modelling of PV Array

For a PV pumping system, the PV array is the power source. There are different sizes of PV panels available for users to select in the market. And a number of PV cells combined in parallel or series can provide a PV array with demanded power. The PN junction is the core of the semiconductor and generates electricity through the photoelectric effect. Under ideal conditions, a PV cell can be seen as

a circuit with a constant current source and a diode in parallel. The equivalent circuit diagram of a PV cell is shown in Figure 2.5.

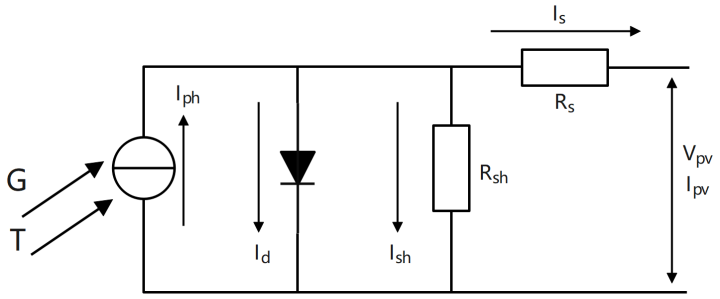


Figure 2.5: Equivalent circuit diagram of a PV cell.

From the equivalent circuit of the PV cell, the mathematical description is,

$$I_{pv} = I_{ph} - I_d - I_{sh} \tag{2.1}$$

$$I_{pv} = I_{ph} - I_0\{exp[\frac{q}{nKT}(V_{pv} + I_{pv}R_s)] - 1\} - \frac{V_{pv} + I_{pv}R_s}{R_{sh}} \tag{2.2}$$

Where, I_{pv} is the output current of a PV cell (A), V_{pv} is the output voltage of a PV cell (V), I_{ph} is the photo current (A), I_0 is the saturation current (A), $q = 1.6 \times 10^{-}19$C is the electron charge, R_s is the series resistance inside the PV cell (Ω), R_{sh} is the shunt resistance inside the PV cell (Ω), n is the ideality factor of the diode, $K = 1.38 \times 10^{-}23$ J/K is the Boltzmann's constant and T is the operating temperature of the PV cell (K).

Under the ideal condition, R_s approximates to zero, R_{sh} approximates to infinite. As a result, Equation 2.2 can be reduced to,

$$I_{pv} = I_{ph} - I_0[exp(\frac{q}{nKT}) - 1] \tag{2.3}$$

When a PV array is composed of N_p PV cells in parallel and N_s PV cells in series, then,

$$I_{pv} = N_p I_{ph} - N_p I_0[exp(\frac{q}{nKTN_s}) - 1] \tag{2.4}$$

Analyzing the characteristic of PV cells, the mathematical models of the open-circuit voltage V_{oc} and short-circuit current I_{sc} are important. When the PV cell is short-circuited the output voltage $V_{oc} = 0$, the mathematical equation of I_{sc} is,

$$I_{sc} = I_{ph} - I_0[exp(\frac{qI_{pv}R_s}{nKT}) - 1] - \frac{R_s I_{sc}}{R_{sh}} \tag{2.5}$$

Similarly, R_s approximates to zero, R_{sh} approximates to infinite and the saturation current I_0 is very small [18], then,

$$I_{sc} \approx I_{ph} = [I_{scr} + K_i(T - T_n)]\frac{G}{G_r} \tag{2.6}$$

Where, I_{scr} is the reference short-circuit current of the PV cell, K_i is the short-circuit current of the cell at $25^{\circ}C$ and $1000W/m^2$, T_n is the nominal temperature (K), G is the solar irradiance (W/m^2) and $G_r = 1000W/m^2$ is the nominal solar irradiance.

From Equation 2.6, the short-circuit current I_{sc} is related to the solar irradiance G and the temperature T of the PV cell. Since there is an initial nominal temperature T_n and $T - T_n$ relatively small compared to T_n, the temperature of the PV cell has little effect on the short-circuit current. The short-circuit current is proportional to solar irradiance, therefore the solar irradiance has more effect on the short circuit current.

When the PV cell is open-circuited, the PV output current $I_{pv} = 0$, then,

$$I_{ph} = I_0[exp(\frac{qV_{oc}}{nKT}) - 1] + \frac{V_{oc}}{R_{sh}} \tag{2.7}$$

After reducing Equation 2.7, the mathematical description of the open-circuit voltage V_{oc} is,

$$V_{oc} \approx \frac{nKT}{q} ln(\frac{I_{ph}}{I_0}) \tag{2.8}$$

From Equation 2.8, the temperature on the surface of the PV cell has more effect on V_{oc} and the solar irradiance has less effect.

According to the model of the PV cell,

$$I_0 = I_{scr}(\frac{T}{T_n})^3 exp[\frac{qE_g}{nK}(\frac{1}{T_n} - \frac{1}{T})] \tag{2.9}$$

Where, E_g is the band gap energy of the semiconductor (eV).

2.2.2 Modelling of battery

Among all the commercial batteries in the market, lead-acid batteries are the most popular and wildly used in renewable energy systems [19]. The equivalent circuit can characterize the dynamic model of the lead-acid battery. The circuit consists of a controlled voltage source and a constant resistance, as shown in Figure 2.6.

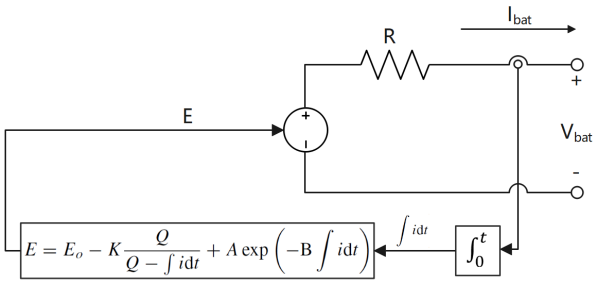


Figure 2.6: Battery model.

The equivalent circuit is described by mathematical equations,

$$E = E_0 - K\frac{Q}{Q - \int idt} + Aexp(-B\int idt) \tag{2.10}$$

$$V_{bat} = E - i \times R \tag{2.11}$$

Where, E is the nonlinear voltage (V), E_0 is the battery constant voltage (V), K is the polarization constant (V/Ah), or polarization resistance (Ohms), Q is the maximum battery capacity (Ah), $\int idt$ is the extracted capacity (Ah), A is the exponential voltage (V), B is the exponential capacity (Ah^{-1}), Vbat is the battery voltage (V), R is the internal resistance (ohm), i is the battery current (A).

The amount of power left in a battery is also called the battery state of charge (SOC), Indicating the ratio of the remaining capacity to the total available capacity after the battery is used or left for a long period of time. A conventional SOC estimation method is the current integration method, also known as the coulomb counting method. In this method, during charging and discharging the battery current is measured and be integrated in time, as described in Equation 2.12.

$$SOC_{now} = SOC_{past} - \frac{I_{bat,now} \times t}{Q} \tag{2.12}$$

2.2.3 Modelling of the pump

For the pump application, the load torque is proportional to square of speed. The motor torque equation can be expressed by:

$$T_e - K_{pump}\omega^2 = J(\frac{dw}{dt}) \tag{2.13}$$

Where, T_e is the torque generated by the motor ($N \cdot m$). K_{pump} is the pump proportionality constant ($N \cdot m/(rad/s)^2$). J is the inertia of the induction machine ($kg \cdot m^2$). $\frac{dw}{dt}$ is the rate of change of angular velocity with time.

The pump proportionality constant can be calculated by,

$$K_{pump} = \frac{T_{rated}}{\omega^2{}_r} \tag{2.14}$$

Where T_{rated} is the torque offered by the motor under steady-state and $\omega^2{}_r$ is the angular velocity of the rotor.

2.3 SYSTEM SIZING

The system configuration of the solar array fed water pumping system is described in Figure 2.7. The system in this project consists of a PV array connected to a boost converter. A three-phase inverter that used to provide AC voltage to the IM. A battery that regulates the dc bus voltage through a bidirectional dc-dc converter and supplies sufficient power to the motor. The P&O MPPT method is used to control the maximum power extraction of the PV array. The V/f control is implemented to regulate the speed of the IM motor. A double-loop control is used to control the charging and discharging of the battery.

The system parameters are designed in this section, including the PV array design, the battery capacity design and the converter parameters design.

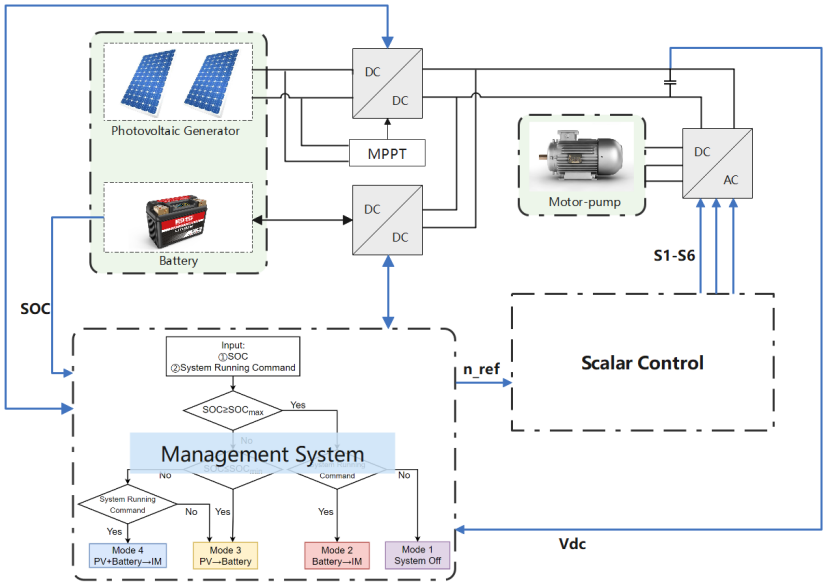


Figure 2.7: The system configuration of the solar array fed water pumping system.

2.3.1 DC Link Voltage

An induction motor of 1.5kW is assumed to be selected in the system. Table 2.1. shows the relative parameters of the selected motor. According to the rated voltage of the selected motor, the demanded DC link voltage can be calculated using,

$$V_{dc} = \sqrt{2} \times 400 = 565.7V. \tag{2.15}$$

Therefore, the DC link voltage is chosen to be 580V.

Type code	AAP90S2A	Rated output	1.5kW
Rated voltage	Δ400V±5%	Number of poles	2
Frequency	50Hz±2%	Rated speed	2920rpm
Rated current	4.1A	Rated torque	4.9Nm

Table 2.1: Motor parameters

2.3.2 Design of the PV Array

For PV array sizing, to let the pumping system be able to operate within the whole year, the month with the lowest radiation on the array plane is chosen as the design month. Assuming the PV array will be placed in Delft, the Netherlands, the average hourly profile of the solar irradiance for each month in Delft is shown in Figure 2.8. The weather condition varies greatly in different seasons. The month with the lowest radiation, in delft is December and the average daily irradiance is $G_{low} = 888Wh/m^2$.

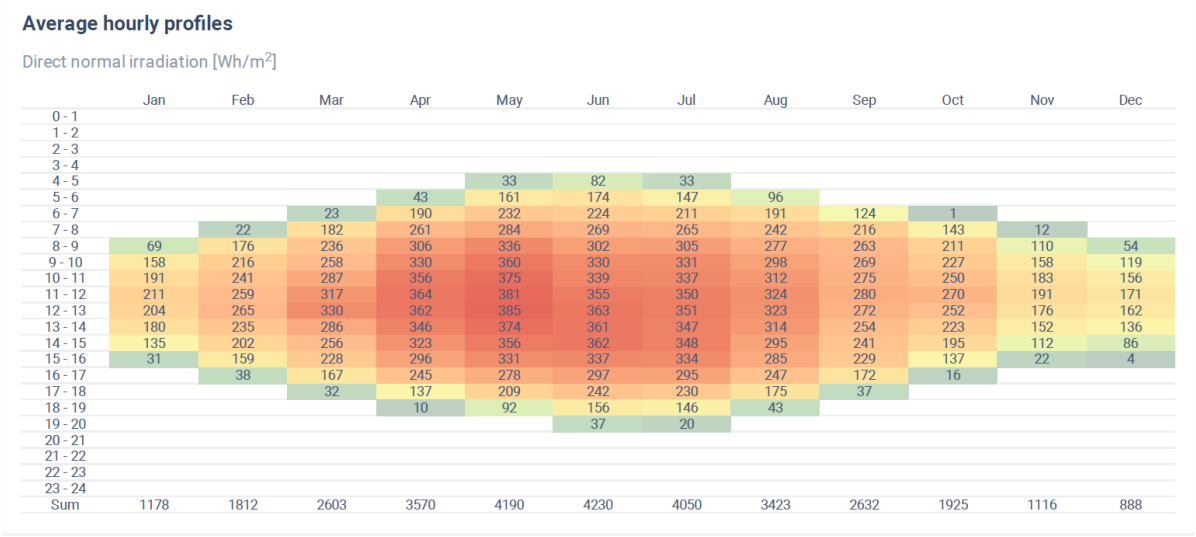


Figure 2.8: Average hourly profile of the solar irradiance for each month in Delft [3].

Canadian Solar 200 Watt Solar Panel CS6P-200P is selected in the designed system. Table 2.2 shows the relative parameters of the PV panel.

Nominal Maximum Power at STC P_{max}	200W
Optimum Operating Voltage V_{mp}	28.9V
Optimum Operating Current I_{mp}	6.93A
Open Circuit Voltage V_{oc}	36.2V
Short Circuit Current I_{sc}	7.68A
Operating Temperature	-40°C +85°C
PV efficiency	14%
Dimensions	1638×982×40mm

Table 2.2: Canadian Solar 200 Watt Solar Panel CS6P-200P

Assuming the water pump will work 2 hours a day and 7 days a week, the power demand can be calculated.

$$P_{load} = \frac{1500 \times 2 \times 7}{7} = 3000Wh/day. \tag{2.16}$$

$$I_{load} = \frac{3000Wh}{580V} = 5.2Ah/day. \tag{2.17}$$

$$P_{PV,demand} = \frac{P_{load}}{\eta_1 \eta_2 \eta_3} \tag{2.18}$$

Where, $P_{pv,demand}$ is the designed PV array power. η_1 is the wiring loss factor (typically 0.9). η_2 is the charge regulator efficiency (typically 0.85). η_3 is the battery efficiency (typically 0.9).

So,

$$P_{PV,demand} = \frac{3000}{0.9 \times 0.85 \times 0.9} = 4.3573kW$$

The demanded PV area can be calculated as,

$$APV = \frac{P_{pv,demand} \times \eta_{safety}}{G_{low} \times \eta_{pv}} \tag{2.19}$$

Where, $\eta_{safety} = 1.3$ is the PV array sizing safety factor, η_{pv} is the PV efficiency.

Then,

$$APV = \frac{4375.3 \times 1.3}{888 \times 0.14} = 45.6m^2$$

From Table 2.2, the PV module area of the selected panel is $A = 1.638 \times 0.982 = 1.609m^2$. The number of PV modules can be calculated as,

$$N = \frac{APV}{A} = \frac{45.6}{1.609} = 28.3 \tag{2.20}$$

The number of PV modules connected in parallel is:

$$N_p = \frac{I_{load}}{I_{mp} \times Numberofpeaksunhours \times Systemconversionefficiency}$$

$$= \frac{5.2}{6.93 \times 0.888 \times 0.7} = 1.21 \approx 2 \tag{2.21}$$

Then, the total number of PV modules is selected as 30 and the number of series connected PV modules is $N_s = 15$. Table 2.3 shows the complete PV array parameters. Figure 2.9 shows the P-V and I-V characteristic of the designed PV array.

Maximum Power	2444W
Open Circuit Voltage V_{oc}	522.3V
Short Circuit Current I_{sc}	6.164A
Voltage at maximum power V_{mp}	438.4V
current at maximum power I_{mp}	5.573A

Table 2.3: Complete PV array

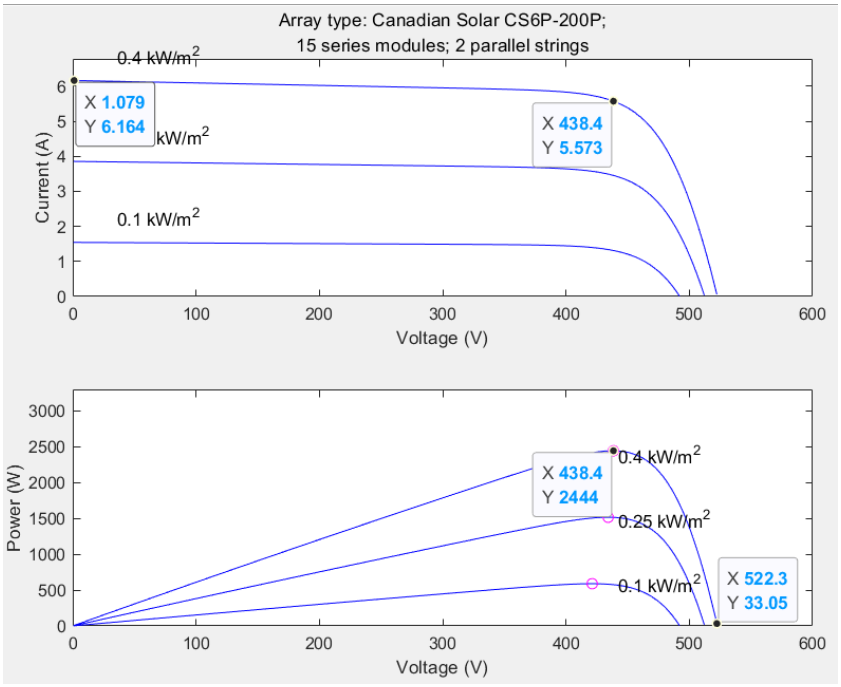


Figure 2.9: Average hourly profile of the solar irradiance for each month in Delft.

2.3.3 Sizing of the Battery

The capacity of the battery is determined by the power output of the PV array, the load capacity and the inverter efficiency.

$$C = \frac{P_m \times D}{K_1 \times K_2 \times K_3 \times V_{DC}} \tag{2.22}$$

Where, C is the battery capacity (Ah). D is the maximum number of hours without sunlight (h). P_m is the load power (W). K_1 is the discharge depth of the battery (typically 0.5-0.7). K_2 is the inverter efficiency (typically 0.8-0.9). K_3 is the wiring losses (typically 0.95-0.98). V_{DC} is the DC bus voltage of the system.

So,

$$C = \frac{1500 \times 2.5 \times 24}{0.6 \times 0.85 \times 0.965 \times 580} = 315Ah$$

2.3.4 Design of the DC link capacitor

In order to provide sufficient energy during system transients such as the decrease and increase of the radiation, the DC link capacitor is calculated as [20],

$$\frac{1}{2}C_{DC}(V_{DC,ref}^2 - V_{DC,min}^2) = 3\alpha VIt \tag{2.23}$$

Where, α is the overloading factor, $V_{DC,min}$ is the acceptable lowest DC link voltage, I is the per phase current of motor and t is the time duration of transients. Generally α=1.2, $t = 0.005s$ [20].

Then,

$$\frac{1}{2}C_{DC}(580^2 - 570^2) = 3 \times 1.2 \times 400 \times 4.1 \times 0.005$$

So, DC link capacitor is selected to be $C_{DC} = 6mF$.

2.3.5 Design of DC-DC Boost Converter

The inductance of the boost converter is [21],

$$D = \frac{V_{DC} - V_{mp}}{V_{DC}} = \frac{580 - 438.4}{580} = 0.2441 \tag{2.24}$$

$$L_{m,boost} = \frac{V_{mp}D}{\triangle I f_s} = \frac{438.4 \times 0.2441}{5 \times 10000} = 2.14mH \tag{2.25}$$

Where, f_s is the switching frequency, $\triangle I$ is the current ripple. The inductance value is selected to be 2mH.

2.3.6 Design of the Bidirectional DC-DC Converter

Same as in Section 2.3.5, the inductance can be calculated as,

$$D = \frac{V_{DC} - V_{bat}}{V_{DC}} = \frac{580 - 480}{580} = 0.1724 \tag{2.26}$$

$$L_{m,bi} = \frac{V_{bat} D}{\triangle I f_s} = \frac{480 \times 0.1724}{3 \times 10000} = 2.14mH \tag{2.27}$$

The inductance value is selected to be 2.8mH.

2.4 CONTROL STRATEGY FOR THE PROPOSED SYSTEM

2.4.1 P&O Method for MPPT

In this PV fed water pumping system, the perturbation and observation method (P&O) is used to achieve MPPT. The objective of this method is to periodically change the output voltage (or current) of the PV cell and observe the variation of the output power from the PV cell. Based on the increasing or decreasing of the output power, keep changing the output voltage (or current) and finally let the PV cell operate at the maximum power point. As shown in Figure 2.4, when the operating point of the PV cell is at the left side of the maximum power point, the MPPT control will make the voltage output increase. When the operating point is at the right side of the maximum power point, the MPPT control will make the voltage output decrease. By keeping the search process, the PV cell will eventually operate at the maximum power point. In this method, dP/dU is replaced by $\triangle P/\triangle U$. The final operation point will satisfy $\triangle P/\triangle U = 0$, in other words, the maximum power point. The flow chart of the implemented P&O method in this project is shown in Figure 2.10.

2.4.2 Battery Control Strategy

The charging and discharging of the battery are controlled through a bidirectional dc-dc converter. The battery control includes two loops. The outer loop is the bus voltage control loop which will control the bus voltage to be the reference value. The inner loop is the battery current control loop which will control the charging and discharging current of the battery and in the meanwhile keep the battery current in the safety range. When the bus voltage V_{DC} is lower than the reference voltage$V_{DC,ref}$, the bidirectional operates as a boost converter. When the bus voltage is higher than the reference voltage, the bidirectional dc-dc operates as a buck converter. The switching signals for the two switches are complimentary.

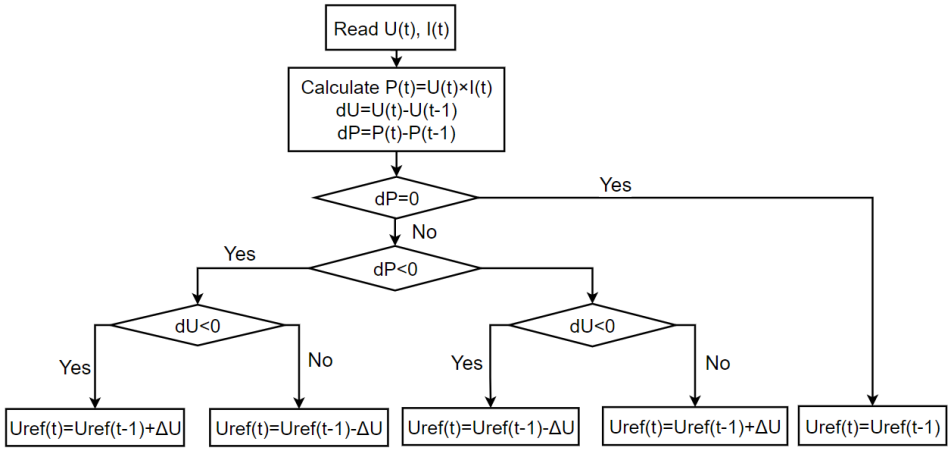


Figure 2.10: Flowchart for perturbation and observation method (P&O).

The battery control diagram is shown in Figure 2.11. The measured dc bus voltage is compared with the reference bus voltage. The error signal will pass through a PI controller and give the battery reference current. Based on the battery requirement, the battery reference current value from the PI controlled will be limited in the safety range. The measured battery current is compared with the current reference value. The error signal will pass through a PI controller and give the duty cycle for the bidirectional dc-dc converter.

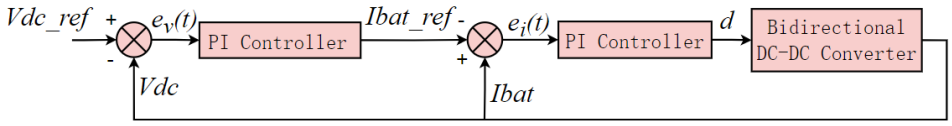


Figure 2.11: Battery control diagram.

2.4.3 Scalar Control of Induction Machine

Scalar control, also called the V/f control, is the most common, simple and cost-effective control method for induction machines [8]. In order to take full advantage of the machine torque and avoid flux saturation, for the speed control of an IM it is desired to keep a constant air-gap flux. The flux magnitude $\varphi_s = \frac{V}{\omega}$. Therefore, the voltage magnitude should be controlled to be proportional to the frequency. When neglecting the slip speed, the rotor speed is proportional to the frequency of the machine input voltage. In other words, the speed of an induction machine can be controlled by controlling the frequency of the three-phase voltage. For the V/f control, the magnitude of the three-phase voltage is decided by the frequency as well. The induction machine is usually fed by a voltage source inverter (VSI). By controlling the switching on the VSI, it is able to output three-phase voltage with desired frequency and magnitude. Open loop V/f control is implemented in the proposed system. The control block diagram is shown in Figure 2.12.

In this system, the space vector pulse width modulation (SVPWM) is implemented on a three-phase inverter to control the machine's input voltage.

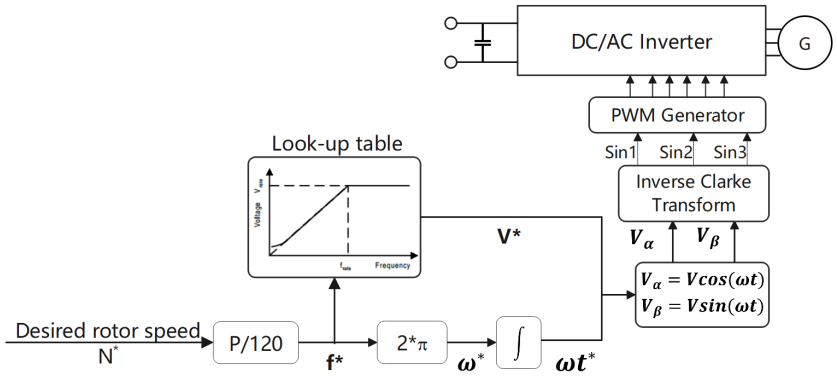


Figure 2.12: Open loop V/f control diagram.

2.4.4 Central Management Control

In order to maintain the safe and stable operation of the system, it is essential to have a central management subsystem. In that case, when the system is operating under different conditions, for instance, when the battery SOC is lower than the battery safety range or when the pumping system is not required, the central management subsystem will decide the system operation mode based on certain control parameters. Depending on the system's on&off command and the battery SOC, the system is able to operate under 4 modes:

1. Standby Mode.

When the battery SOC is higher than the battery SOC_{max} and the system don't receive the running command, the motor speed is set to be 0, no power will be delivered by the PV array.

2. Battery + IM Mode.

When the battery SOC is higher than the battery SOC_{max} and the system receives the running command, no power will be delivered by the PV array and the battery will power the motor to run at the rated speed.

3. PV +Battery Mode.

When the battery SOC is lower than the battery SOC_{min}, the motor speed is set to be 0 and the PV array will charge the battery.

4. PV + Battery + IM Mode.

When receiving the running command and $SOC_{min} < SOC < SOC_{max}$, PV array and the battery will work together to power the motor to operate at the rated speed. The control diagram of this central management system is shown in Figure 2.13.

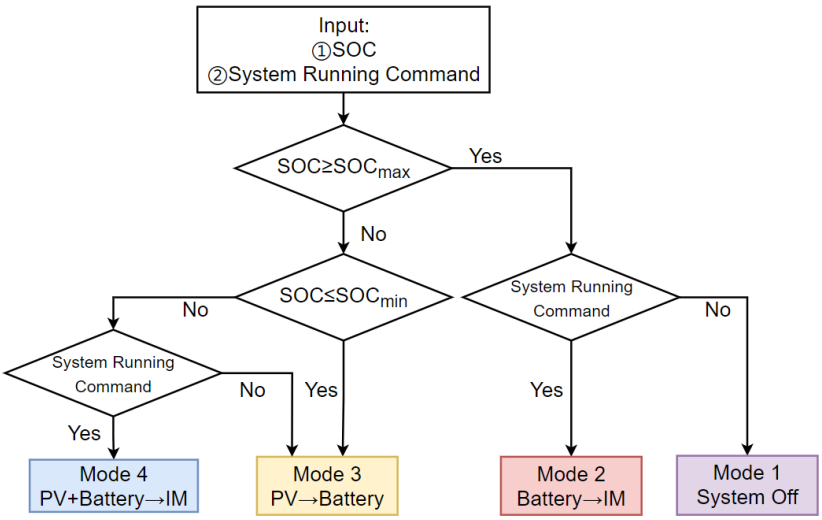


Figure 2.13: Central management control diagram.

3 IMPLEMENTATION OF SYSTEM SIL SIMULATION

After completing the system design and before moving on to the hardware implementation, a software-in-loop (SIL) simulation of the solar array fed water pumping system is implemented. In the SIL simulation testing, both the plant models and the controller model are simulated and executed in the real-time simulator.

In this chapter, the concept of real-time simulation and the OPAL-RT real-time simulation platform is introduced. The workflow of simulating the plant model and the power converter model using the OPAL-RT real-time simulator is described.

3.1 OPAL-RT AND REAL-TIME SIMULATION

In the engineering workflow that before moving on to the real hardware design, the implementation of system-level simulation is essential. In the system-level simulation the system control strategy can be tested and the interaction between electronic devices in the system can be verified. However, the desktop software, such as Simulink, is not able to validate the real-time behavior of the embedded software running on an actual target. Implementing real-time simulation allows engineers to find problems at an early stage, proceed to device design before the actual system is ready, reduces the potential risks and costs on testing physical devices under different conditions, as well as to test all possible scenarios in a secure environment.

In the real-time simulation, time step is fixed from the beginning to the end of simulation. Within one time step, the processor has to read input signals, complete all necessary calculations and send all outputs.

3.1.1 Real-time Simulation and OPAL-RT

The OPAL-RT system consists of a software tool RT-LAB that runs on the host computer and a real-time simulator as the hardware part. Simulink models can be imported into RT-LAB and be edited in RT-LAB, then RT-LAB will generate C code to transform the designed model into a real-time application. The host computer can be also seen as the user interface. The real-time simulator (also the called target computer) is responsible for the I/O and real-time model execution. The simulator and RT-LAB communicate with each other through the TCP/IP protocols. Figure 3.1 shows the system configuration of the OPAL-RT system.

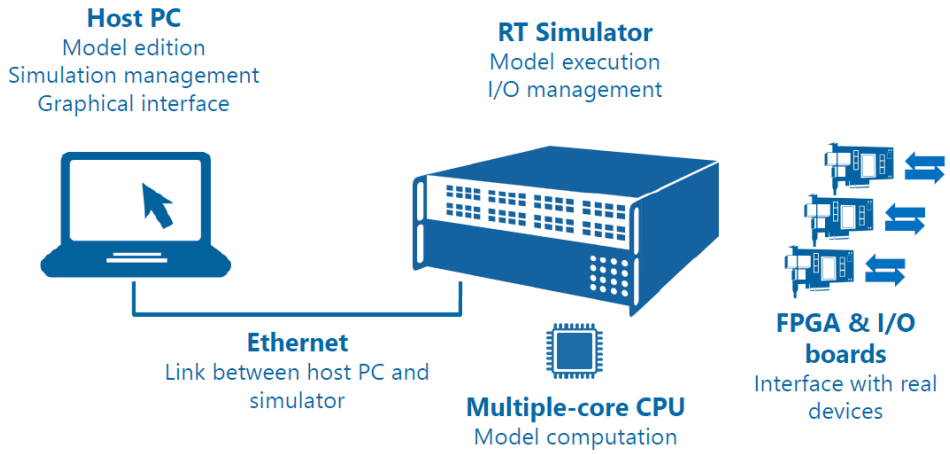


Figure 3.1: The OPAL-RT system [4].

3.1.2 Conversion from Simulink Model to Real-time Model

In order to import Simulink models into RT-LAB, the built models must be regrouped into subsystems. Each top-level subsystem will be computed on one core. There are three types of subsystems, Master Subsystem (MS), Console Subsystem (CS) and Slave Subsystem (SS). Every subsystem is computed on a different computation node in the OPAL-RT simulator. Only one master subsystem and one console subsystem are allowed in an RT-LAB project. The slave subsystem is optional. The typical configuration of the top-level of the model is shown in Figure 3.2.

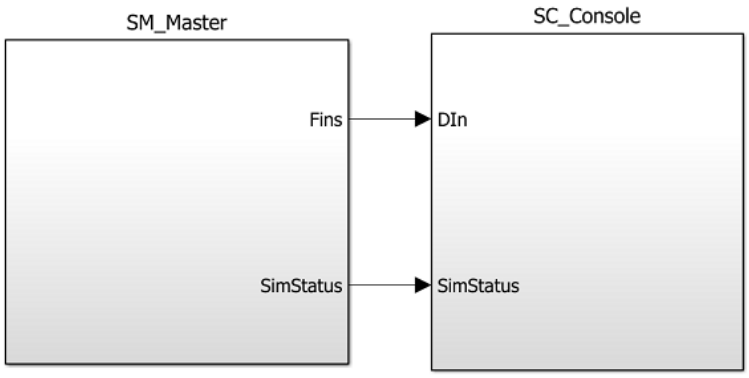


Figure 3.2: Typical configuration of the top-level of the model.

The master subsystem is the main and necessary subsystem. It contains all the computational elements, I/O blocks and signal generators, etc. The slave subsystem has a similar function as the master subsystem, but it is only needed when computational elements must be distributed across multiple nodes.

The console subsystem contains all the user interface blocks, such as scope, displays, switches, etc. When the system is running, the console subsystem enables the user to interact with it. No computational node is linked to this subsystem, so no signal generation should in this subsystem.

3.1.3 OP4510

The OP4510 from OPAL-RT, as shown in Figure 3.3, is the used real-time simulator for this project and it operates with a Kintex7 FPGA. The specifications of the OP4510 are shown in Table 3.1.

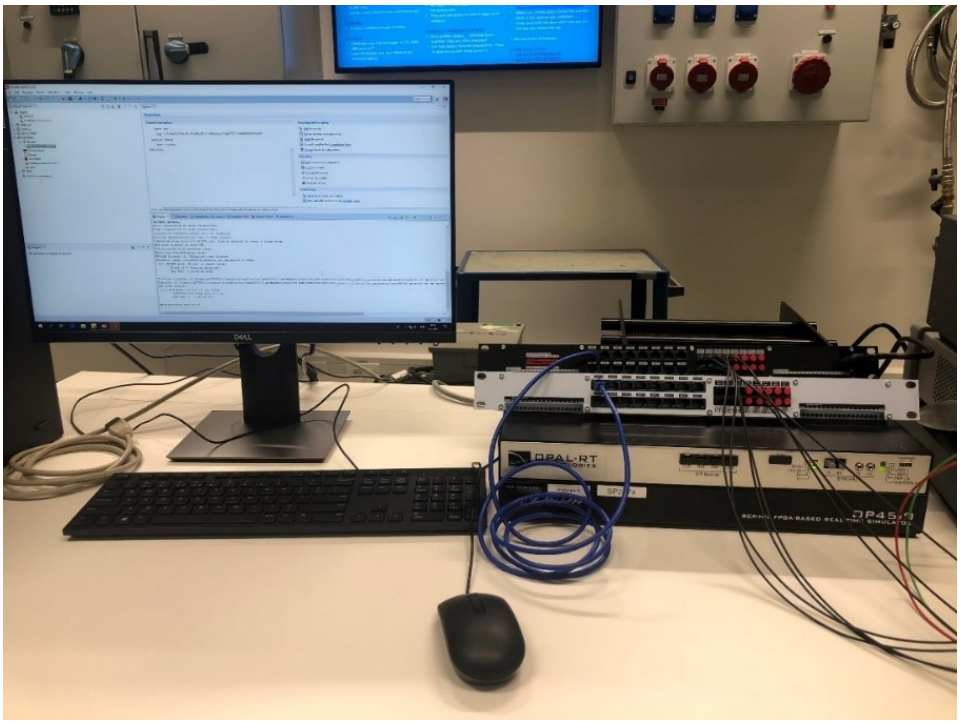


Figure 3.3: OP4510 real-time simulator and host machine station in the laboratory.

Items	Quantity	Description
Chassis Type	1	OP4510
CPU	1	Intel Xeon 3.5GHz
Total Core	4	-
Memory	2	8G
OP5353-1	1	Digital In
OP5360-2	1	32 Digital Out
OP5342	1	16 Analog In
OP5330-1	1	16 Analog Out

Table 3.1: Specification of OP4510.

3.1.4 CPU Model and FPGA Model

When running the real-time simulation in the CPU core, depending on the complexity of the plant model and the simulated controller, the minimum time-step of the simulation is limited to 10μs. This limitation brings a serious drawback to the CPU based real-time simulation. When implementing the system with power electronic converters with high-frequency signals, the time-step of the simulation should go below 1μs. Therefore, achieving low latency between the controller and the control target

as well as achieving the high sampling resolution of the PWM signals. The effective solution for meeting the timing requirement is the FPGA based real-time simulation which is able to execute the model in nanoseconds.

Implementing a circuit on FPGA requires solving differential equations on FPGA, which is not easy and requires advanced FPGA programming skills. The eHS solver can help to work on the FPGA programming of circuits. The circuit will be designed and built on the circuit editor, such as Simulink, then loaded on the eHS solver. The eHS solver will automatically generate the FPGA solution of the circuit. The eHS can be seen as a black box in the CPU model where only sources, measurements and switch gates can be accessed, as shown in Figure 3.4.

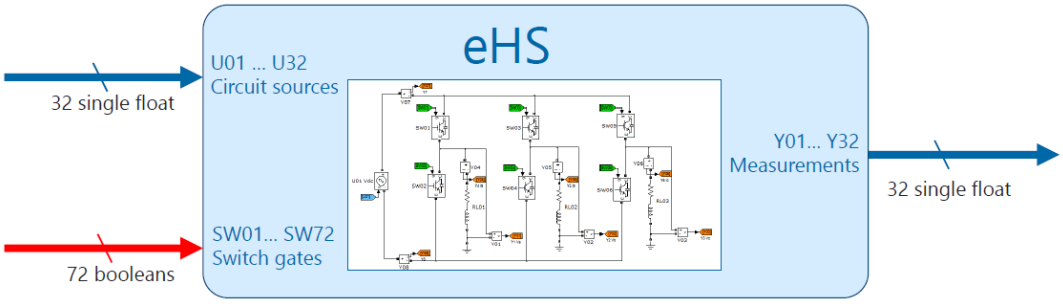


Figure 3.4: The configuration of eHS [5].

As mentioned previous, the OPAL-RT system consists of a real-time simulator and a host computer. Figure 3.5 shows the structure of OPAL-RT system. Inside the simulator, there are CPU cores and FPGA. The CPU will configure the circuit model in FPGA and run the computation in FPGA. The results can be either transfer to the external controller or to the host computer to monitor and see the results.

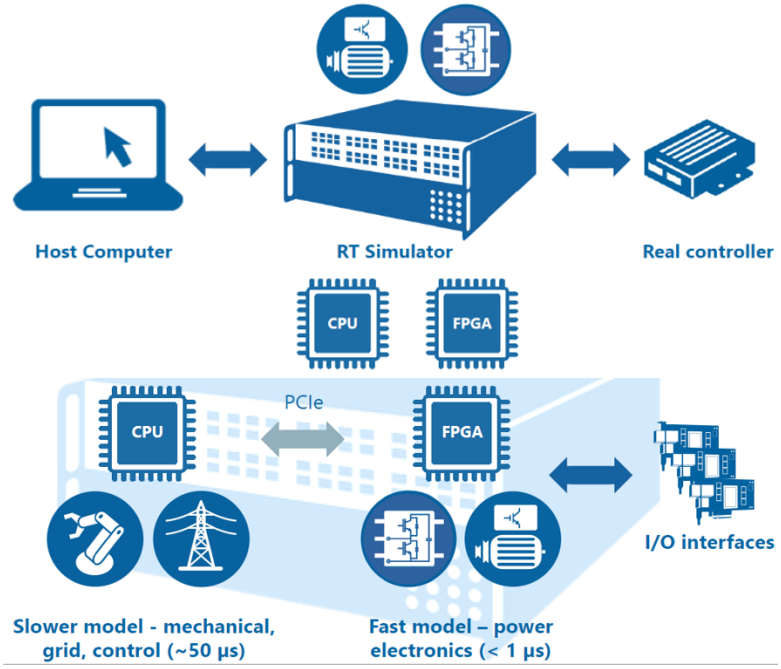


Figure 3.5: The structure of OPAL-RT system [5].

3.2 CONVERTERS, PV AND BATTERY REAL-TIME SIMULATION IN RT-LAB

In the OPAL-RT real-time simulation, depends on the complexity of the model and the required simulation time-step, the real-time simulation can either be implemented based on CPU or FPGA.

The plant model, the PV array model and the battery model, which do not require simulation time-step as low as 10us has been built in the CPU model. In this section, a brief description of the PV array model and the battery model is given.

As mentioned in Section 3.2.1 , eHS solver from the eFPGASIM library provides a solution to program the electric circuit models in FPGA. Therefore, in this section, the boost converter for MPPT control and the bidirectional dc-dc converter has been built in Simulink as the FPGA model. The communication established between the FPGA model and the CPU model is described.

3.2.1 PV and Battery Model

The PV and battery models from the Simscape library in Simulink are used as the reference to build the PV and battery models in this system.

As described in Section 2.2.1, the PV array is a five-parameter model which consists of a light-generated current source IL, diode, series resistance RS and shunt resistance Rsh, as shown in Figure 3.6. The light-generated current IL and diode current Id+Ish are calculated by the PV mathematical models.

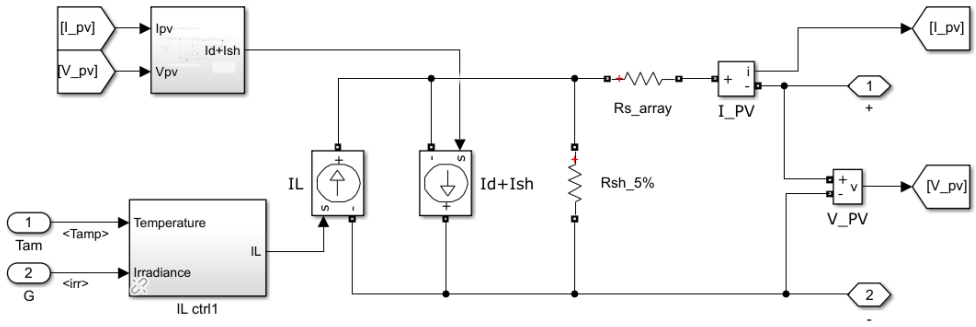


Figure 3.6: Five-parameter model of PV.

For the battery model, the input of the model is battery current and the model outputs are battery voltage and SOC. As described in Section 2.2.2, the battery model consists of both the electrical circuit part and the mathematical model part as shown in Figure 3.7.

3.2.2 Boost and Bidirectional DC-DC Converter Model

The boost and bidirectional dc-dc converter circuits are built in a separate Simulink file which can be called as the FPGA model. After combining the electrical circuit part of the PV and battery model and

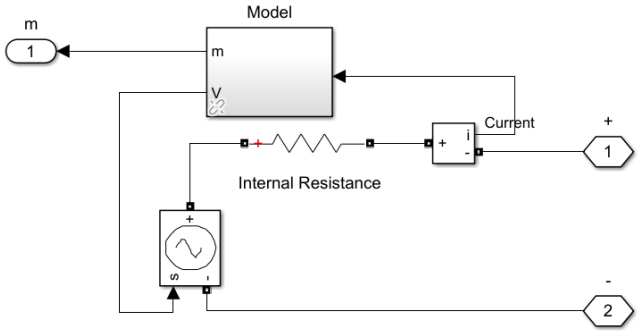


Figure 3.7: Battery model.

the converter circuit, the FPGA model is complete, as shown in Figure 3.8. The eHS solver is placed in the CPU model. After loading the designed circuit on the eHS solver, the CPU model is able to configure the FPGA model and let the electrical circuit run on the FPGA board. Control blocks for PV and battery can also be implemented in the CPU model. The eHS solver automatically computes the minimum time-step that allowed the FPGA to execute the designed electrical circuit. For the boost and bidirectional converter, the minimum time-step is Ts=230ns, as shown in Figure 3.9.

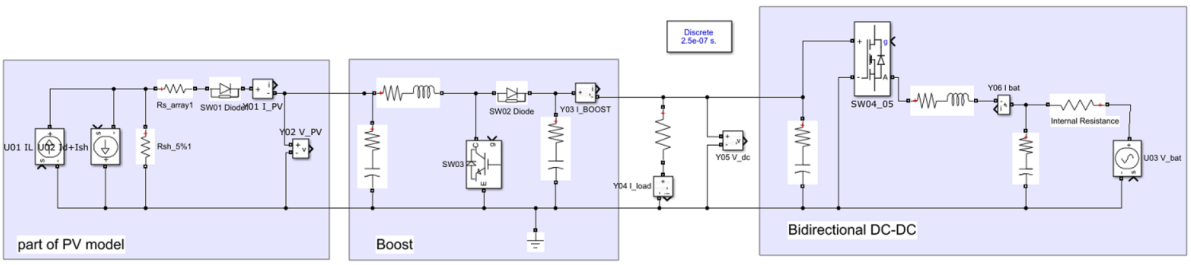


Figure 3.8: Converter FPGA model.

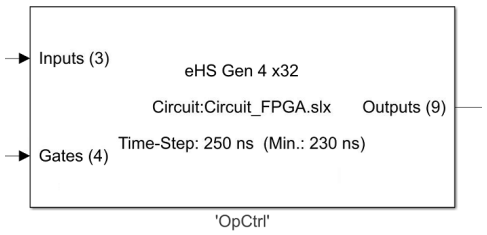


Figure 3.9: eHS solver with loaded circuit.

The converter circuit in Figure 3.8 communicates with the control blocks in the CPU model by exchanging voltage, current and gate signals. The list of all the signals is shown in Table 3.2. signals U01 and U02 contains in the PV model, they emulate the light-generated current and diode current in the model. Signal U03 is the controlled voltage source and represents the battery voltage in the battery model. They establish the link between the other mathematical models of the PV and battery in the CPU model.

There are 6 measurements shown in Figure 3.8, includes the current and voltage measurement of the PV array, the battery current measurement, the DC bus voltage measurement, the boost output

current and load current measurements. The measured signals will be linked to the CPU model for monitoring the results or further computation.

There are 5 gates, 2 for diodes and 3 for IGBTs. The gate signals can be either generated by the CPU board or by the FPGA board.

Type	Signal name	Function
Input	U01	PV model, light-generated current I_L
	U02	PV model, diode current
	U03	Battery voltage
Gates	SW01	Diode for the PV output
	SW02	Diode for the boost converter
	SW03	Switch of the boost converter
	SW04	Upper switch of the bidirectional dc-dc converter
	SW05	Lower switch of the bidirectional dc-dc converter
Output	Y01	PV current
	Y02	PV voltage
	Y03	Boost output current
	Y04	Load current
	Y05	DC bus voltage
	Y06	Battery current

Table 3.2: Exchanged signals between CPU and FPGA model (PV and battery subsystem).

3.3 INVERTER AND INDUCTION MACHINE REAL-TIME SIMULATION IN RT-LAB

OPAL-RT has a unique solution for testing electric machine controllers. The machine and the mechanical load connected on the shaft of the motor, a pump, in this case, are simulated by the real-time simulator. The eFPGASIM library provides several electrical machine models, the power converter portion of the model is simulated by the eHS solver. Eventually, both the converter and machine model are programmed into the FPGA board. The coupling between the eHS solver and the machine model is done by following a certain workflow.

1. Creating and configuring the RT-LAB project model.

2. Adding the eHS block and configure the communication port.

3. Adding the machine blocks and configure the communication settings and the model parameters.

4. Building the power converter circuit on eHS solver.

5. Establishing the coupling and configuring the interface between the eHS and machine.

For the machine subsystem, the model consists of an induction motor and a three-phase inverter that connected to each other.

3.3.1 Three-phase Inverter Model

eHS is typically used to simulate the power electronic circuit part of the system. As for the boost converter and the bidirectional dc-dc converter, the three-phase inverter is simulated by the eHS solver as well. For the eFPGASIM solution of building the machine and drive system, the coupling of eHS solver and machine model is shown in Figure 3.10. The three-phase induction machine connects at the terminal of the three-phase inverter. After being measured by the voltage measurements, the three-phase voltages is sent out to the machine model. The machine model outputs phase currents and feedback to the controlled current source blocks in the eHS circuit.

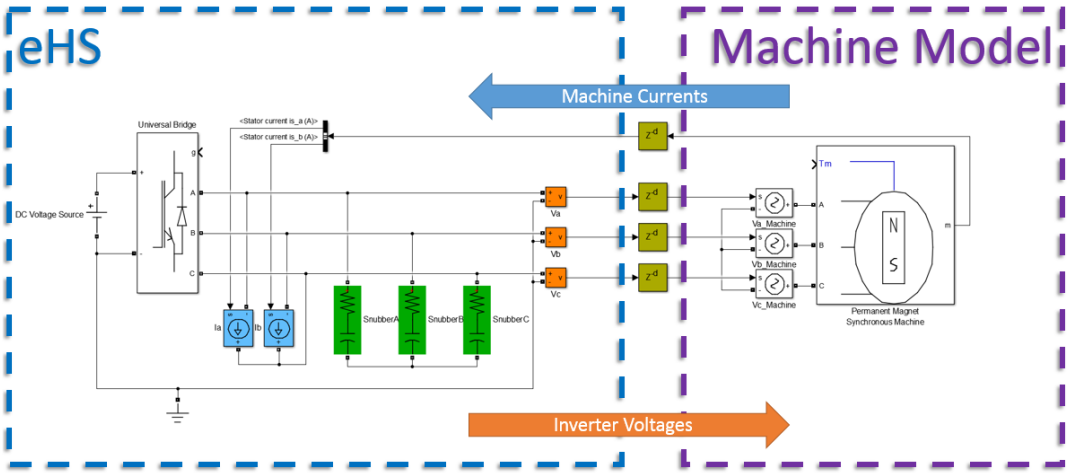


Figure 3.10: Circuit and coupling between the eHS and the machine model [6].

Since there are both stator and rotor sides in the induction machine, the rotor side circuit needs to be built as well. The complete eHS circuit model that includes three-phase inverter coupling with induction machine, the boost and bidirectional dc-dc converter is shown in Figure 3.11. For the machine subsystem, there are six voltage measurements as outputs and 4 controlled current sources as input.

There are six gates for the three-phase inverter. The gate signals are sampled by the CPU. As a supplement to Table 3.2, the exchanged signals between the CPU and FPGA model for the machine subsystem is shown in Table 3.3.

3.3.2 Induction Machine Model

There are several types of machine models in the eFPGASIM library. In this project, a squirrel-cage induction machine is selected. The induction machine model from eFPGASIM is shown in Figure 3.12, and for each machine, one block is needed to be placed in the CPU model. The motor parameters shown in Table 2.1 are set into the machine block.

For this machine model, there are six voltage signals (three stator phase voltages and three rotor phase voltages) and 4 current signals (two phase currents on the stator side and two phase currents on the rotor side) that are required to communicate with eHS. Other than these, the input of the motor model is the rotor speed in rpm and the outputs are the machine operating data, such as stator currents, rotor mechanical speed in rpm and the machine torque.

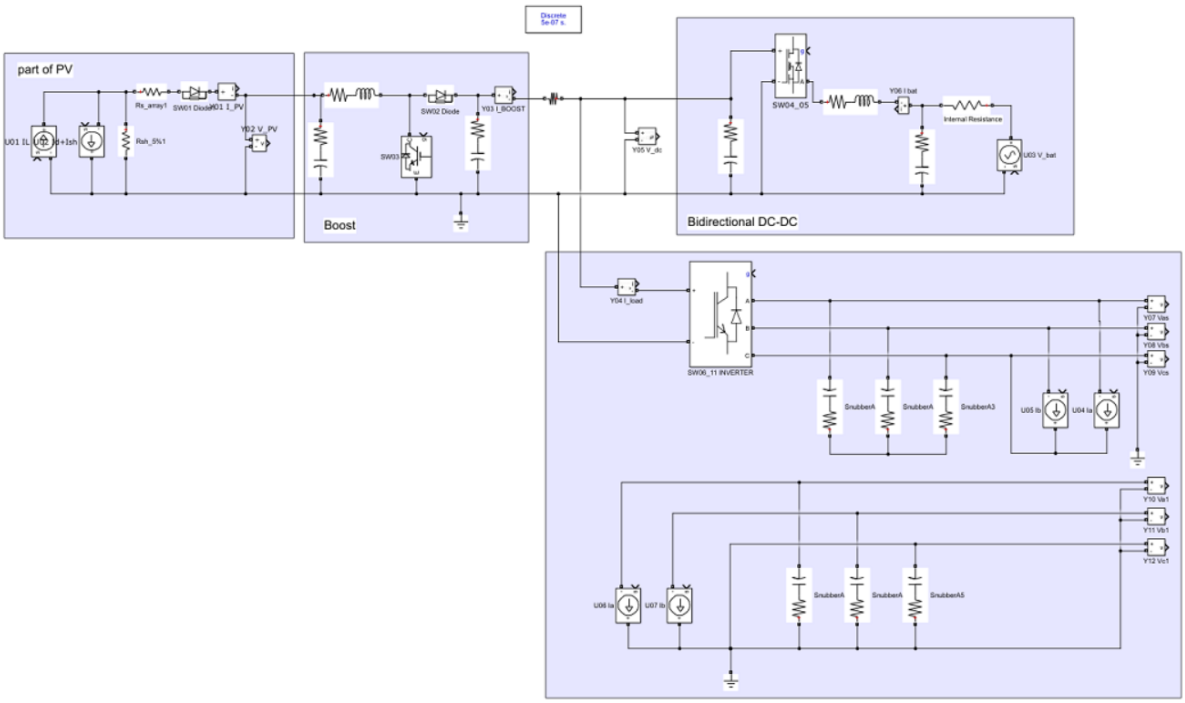


Figure 3.11: eHS circuit model.

Type	Signal name	Function
Input	U04	Stator phase current I_{SA}
	U05	Stator phase current I_{SB}
	U06	Rotor phase current I_{RA}
	U07	Rotor phase current I_{RB}
Gates	SW06-11 INVERTER-01	Phase leg 1 switching signal upper switch
	SW06-11 INVERTER-02	Phase leg 1 switching signal lower switch
	SW06-11 INVERTER-03	Phase leg 2 switching signal upper switch
	SW06-11 INVERTER-04	Phase leg 2 switching signal lower switch
	SW06-11 INVERTER-05	Phase leg 3 switching signal upper switch
	SW06-11 INVERTER-06	Phase leg 3 switching signal lower switch
Output	Y07	Stator phase-to-ground voltage V_{SA}
	Y08	Stator phase-to-ground voltage V_{SB}
	Y09	Stator phase-to-ground voltage V_{SC}
	Y10	Stator phase-to-ground voltage V_{RA}
	Y11	Stator phase-to-ground voltage V_{RB}
	Y12	Stator phase-to-ground voltage V_{RC}

Table 3.3: Exchanged signals between CPU and FPGA model (IM subsystem).

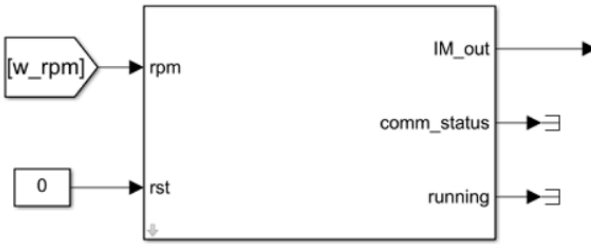


Figure 3.12: Induction machine model.

The first step is to couple the eHS with the machine model. The machine interface model as shown in Figure 3.13 is added to the master subsystem. In the three-phase inverter model, the phase voltage Va/Vb/Vc is measured by Y01/Y02/Y03. Therefore, IM1 uses the eHS Y01/Y02/Y03 as inputs for the stator three-phase voltage. Since the squirrel-cage induction machine model is selected, the rotor voltages should be forced to be 0V. This can be done by either connecting the 3 rotor voltages to unused outputs or connect to the same output of the eHS as shown in Figure 3.14.

Figure 3.13: Machine interface block.

To coupling the machine model to eHS, the eHS solver inputs should be configured as shown in Figure 3.15. The controlled current sources are mapped to the IM.

3.3.3 Simulation of the Pump Model

The motor torque equation has been described in Section 2.2.3. From the motor nameplate, the rated torque of the induction motor is 4.9N·m and the rated speed of the rotor is 2920rpm. Then,

$$K_{pump} = \frac{4.9}{(\frac{2\times\pi\times2920}{60})^2} = 5.24\times10^{-5} N\cdot m/(rad/s)^2$$

To emulate the water pump operation, the pumping transmission model is built based on Equation 2.13, as shown in Figure 3.16. Te is the machine electrical torque from the output of the induction machine model block. The moment of inertia of a pump changes as the shaft rotating. To simplify the simulation, the rotational inertia of the system is set to a constant value. By integrating the rate of change of angular velocity with time, the rotor angular speed is calculated. After converting the rotor speed in rpm, the rotor speed is sent as input of the induction machine block.

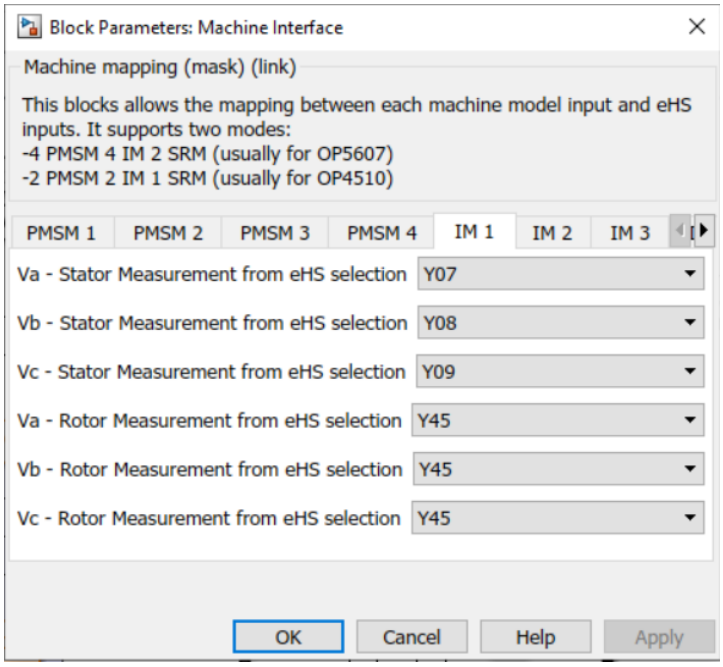


Figure 3.14: Machine interface settings.

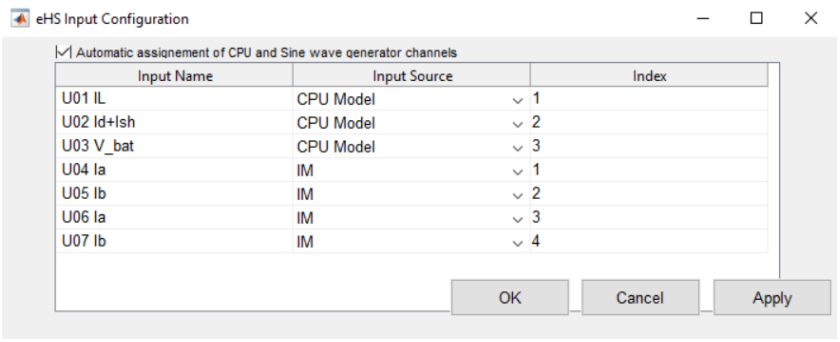


Figure 3.15: eHS inputs configuration.

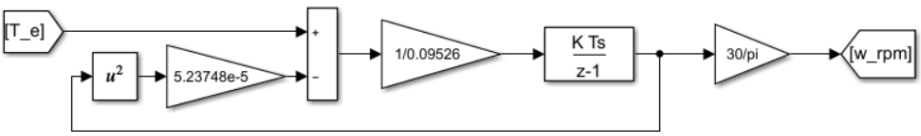


Figure 3.16: The pumping transmission model.

3.4 IMPLEMENTATION OF THE SIMULATED CONTROLLER

Before implementing the HIL test of the PV fed water pumping system, the SIL simulation is implemented to test the system performance, control algorithm and its interaction with the plant model. For the SIL simulation, the plant model and controller are all simulated in the OP4510 real-time simulator. The induction motor model and power converter model are executed in the FPGA. The battery and PV array models are built and executed in the CPU. The controller of this system is simulated and executed in the CPU as well. The SIL simulation system diagram and the signal communications are shown in Figure 3.17.

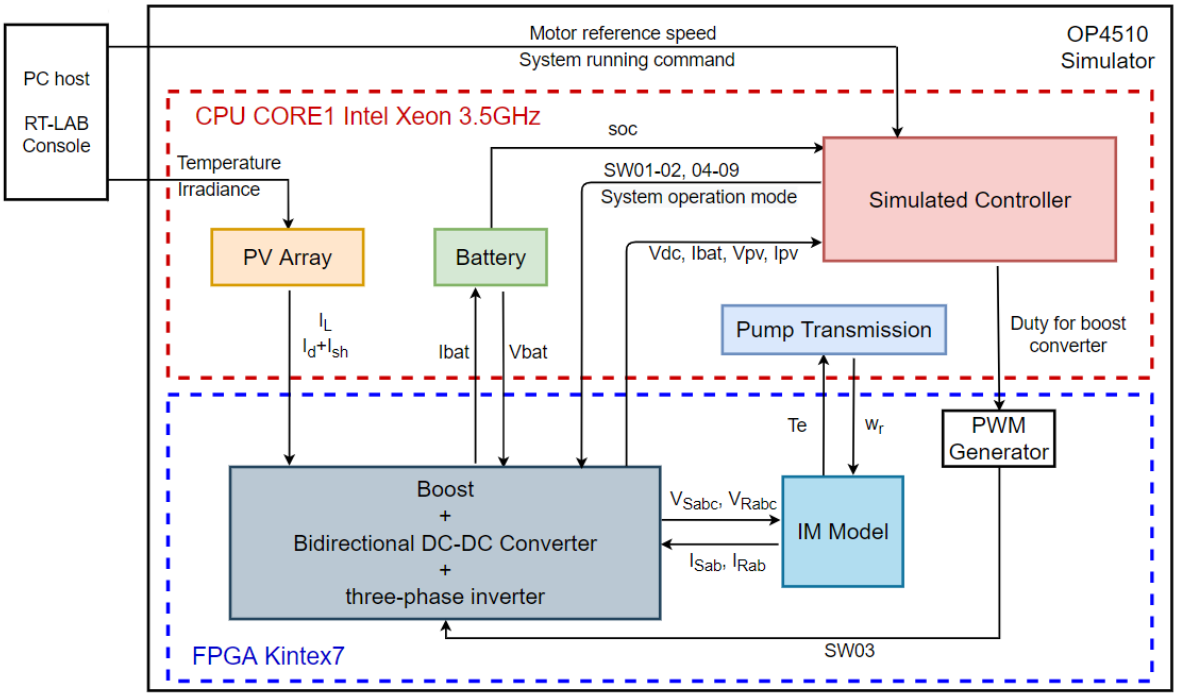


Figure 3.17: SIL simulation system diagram.

There are three controls in the system. The MPPT control for the PV array through the boost converter will extract maximum power from the PV array. The battery charging/discharging control based on the bidirectional dc-dc converter, which helps to supply sufficient power to the load and regulates the dc bus voltage. The motor speed control regulates the motor running at the rated speed. The control strategies have been discussed in Chapter 2. In this section, the controller model in real-time simulation is built and presented.

The control subsystem is shown in Figure 3.18. The central management subsystem decides the system operation mode based on certain system parameters. The motor control subsystem generates SVPWM signals for controlling the induction motor speed. Since the switching frequency of the boost and bidirectional dc-dc converters is selected to be 10kHz, the control subsystem of PV and battery is triggered at 10kHz frequency. Every 100us, the duty cycles of the boost and bidirectional dc-dc converter will be sent to the two converter models. The simulation time-step for the CPU model is 20us. The simulation time-step for the FPGA model is 500ns.

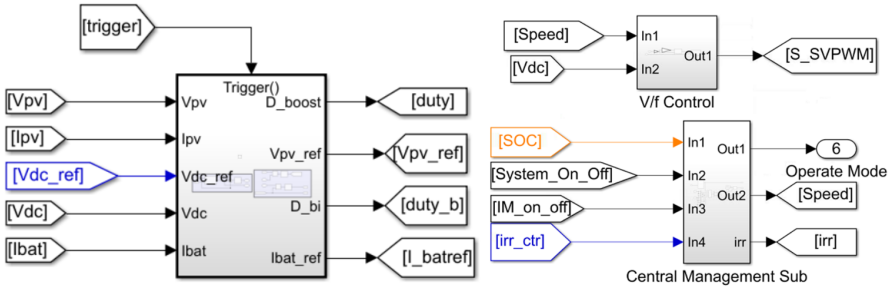


Figure 3.18: Simulated control blocks.

3.4.1 MPPT for PV control

For the PV subsystem, to obtain the maximum power from the PV array, a maximum power point tracking (MPPT) algorithm is implemented through the boost converter. Following Section 2.4.1, the P&O MPPT method is used. The control blocks for PV are built in the CPU model, as shown in Figure 3.19. The P&O MPPT control algorithm is written in a MATLAB Function block. As the outer loop, the inputs of the algorithm are the PV voltage and current, the output is the PV reference voltage. As the inner loop, a PI controller is used to control the PV voltage and a give duty cycle to the boost converter. As shown in Figure 3.20, for the boost converter, the gate signal is directly generated by the FPGA. The switching frequency is 10kHz.

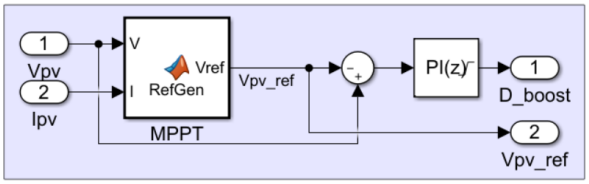


Figure 3.19: Implemented MPPT in CPU model.

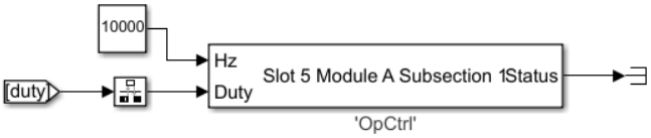


Figure 3.20: Gate signal for the boost converter that directly generated by FPGA.

3.4.2 Battery Control Strategy

Following Section 2.4.2, the battery is controlled through a bidirectional dc-dc converter. Double closed-loop control is implemented. The outer loop is the dc bus voltage control loop and the inner loop is the battery current control loop.

Figure 3.21 shows the control blocks of the bidirectional dc-dc converter. The RTE PWM block from the RT-EVENTS library is used to generate the PWM signals for the two switches of the bidirectional dc-dc converter, as shown in Figure 3.22. The switching frequency is 10kHz. The generated PWM signals are sent as gate inputs of the eHS block.

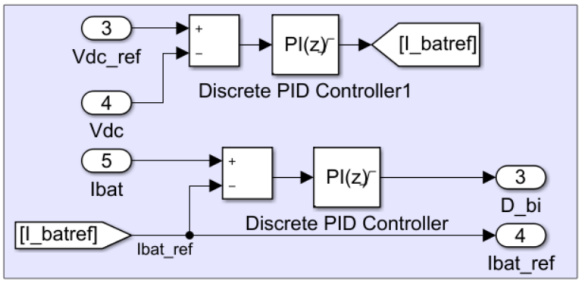


Figure 3.21: Control of the bidirectional dc-dc converter.

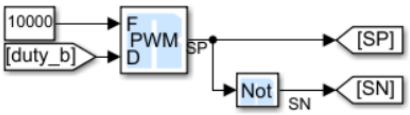


Figure 3.22: RTE PWM blocks.

3.4.3 PI Controller Design

1.Boost converter PI controller parameters

For the Boost converter, the input of the PI controller is the error between the reference DC bus voltage from the MPPT algorithm and the actual bus voltage, the output of the PI controller is the duty ratio of the switch. The relation between the input and the output is,

$$V_{pv} = V_{dc} - DV_{dc} \tag{3.1}$$

According to the automatic control theory, when V_{dc} is stable the disturbance from it to the system can be ignored. Then the open-loop transfer function $G_o(s)$ between the pv voltage and duty ratio $\frac{V_{pv}(s)}{D(s)}$ is obtained as given in Equation 3.2. The closed-loop control block diagram is shown in Figure 3.23.

$$G_o = \frac{V_{pv}(s)}{D(s)} = G(s)G_i(s) = (K_p + \frac{K_i}{s})(-V_{dc}) \tag{3.2}$$

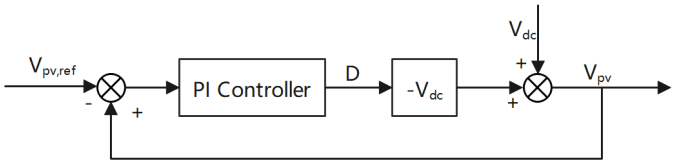


Figure 3.23: Boost converter PI control diagram.

The closed-loop transfer function is,

$$G_c(s) = \frac{G_o(s)}{1 + G_o(s)} = \frac{-K_p V_{dc} s - K_i V_{dc}}{(1 - K_p V_{dc})s - K_i V_{dc}} \tag{3.3}$$

The control objective is to let $V_{pv} = V_{pv,ref}$, in other words, $G_c = 1$. Then, $1 - K_p V_{dc} \approx -K_p V_{dc}$ is needed. In conclusion, for the boost converter, the PI controller $K_p V_{dc} >> 1$, K_i can be any value.

2.Bidirectional DC-DC converter current loop PI controller parameters

The circuit diagram of the bidirectional dc-dc converter is shown in Figure 3.24

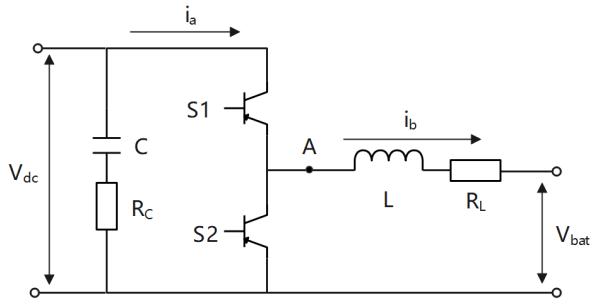


Figure 3.24: Circuit diagram of the bidirectional dc-dc converter.

In this system, the current loop PI controller outputs the duty ratio D of the upper switch $S1$. Complementary PWM signal is given to the upper and lower switch. According to Figure 3.24, when $S1$ is on, $S2$ is off, $V_a = V_{dc}$. When $S1$ is off, $S2$ is on, $V_a = 0$. Then, it can be seen that $V_a = D \times V_{dc}$.

The equation of the inductor current i_b is established,

$$V_a - V_{bat} = DV_{dc} - V_{bat} = L\frac{di_b}{dt} + R_L i_b \tag{3.4}$$

According to the automatic control theory, when V_{bat} is stable the disturbance from it to the system can be ignored. Then the transfer function $G_{current}(s)$ between inductor current and duty ratio $\frac{i_b(s)}{D(s)}$ is obtained as given in Equation 3.5. The current closed-loop control block diagram is shown in Figure 3.25.

$$G_{current}(s) = \frac{i_b(s)}{D(s)} = \frac{V_{dc}}{Ls + R_L} \tag{3.5}$$

The current open-loop transfer function is,

$$G_{o,c}(s) = G_{PI,c}(s)G_{current}(s) = (K_{P,c} + \frac{K_{i,c}}{s})\frac{V_{dc}}{Ls + R_L} \tag{3.6}$$

To reduce the system order and make the system easy to control, pole-zero cancellation method is used. Then,

$$\frac{K_{p,c}}{L} = \frac{K_{i,c}}{R_L} = K_c \tag{3.7}$$

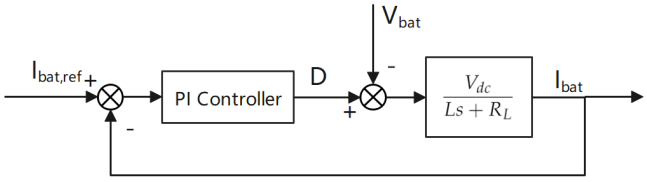


Figure 3.25: Current closed-loop control block diagram.

Where, K_c is the gain parameter and it is a constant number.

If Equation 3.7 is substituted in Equation 3.6, then,

$$G_{o,c}(s) = \frac{V_{dc}K_c}{s} \tag{3.8}$$

The current close-loop transfer function is,

$$G_{c,c}(s) = \frac{G_{o,c}(s)}{1 + G_{o,c}(s)} = \frac{V_{dc}K_c}{s + V_{dc}K_c} = \frac{V_{dc}K_c}{j\omega + V_{dc}K_c} \tag{3.9}$$

$$|G_{c,c}(s)| = \frac{V_{dc}K_c}{\sqrt{\omega^2 + V_{dc}^2{K_c}^2}} \tag{3.10}$$

Take the logarithm of Equation 3.10, then,

$$log|G_{c,c}(s)| = 20lg(\frac{V_{dc}K_c}{\sqrt{\omega^2 + V_{dc}^2{K_c}^2}}) \tag{3.11}$$

When the gain is -3dB, the signal is cut off. The cut off frequency ω_c can be obtained,

$$20lg(\frac{V_{dc}K_c}{\sqrt{{\omega_{c,c}}^2 + V_{dc}^2K_c^2}}) = -3 \tag{3.12}$$

$$\omega_{c,c} = V_{dc}K_c \tag{3.13}$$

The system switching frequency $f_s = 5kHz$, then,

$$\begin{cases} \omega_{c,c} = V_{dc}K_c = 2\pi f_{c,c} \\ f_{c,c} = 500 \end{cases} \tag{3.14}$$

So, the gain parameter $K_c = \frac{50}{29}\pi$.

The current close-loop transfer function,

$$G_{c,c}(s) = \frac{1000\pi}{s + 1000\pi} \tag{3.15}$$

3.Bidirectional DC-DC converter voltage loop PI controller parameter

According to Figure 3.24, when $S1$ is on, $S2$ is off, $i_a = i_b$. When $S1$ is off, $S2$ is on, $i_a = 0$. Then, it can be seen that $i_a = D \times i_b$.

The equation of the capacitor current i_c is established,

$$i_c = i_a = C\frac{dV_c}{dt} \tag{3.16}$$

$$Di_b = C\frac{d(V_c - R_c D i_b)}{dt} \tag{3.17}$$

The transfer function $G_{voltage}$ between DC bus voltage and battery current $\frac{V_{dc}(s)}{i_b(s)}$ is obtained as given in Equation 3.18. The double closed-loop control block diagram of the bidirectional DC-DC converter is shown in Figure 3.26.

$$G_{voltage}(s) = \frac{V_{dc}(s)}{i_b(s)} = D\frac{1 + R_c Cs}{Cs} \tag{3.18}$$

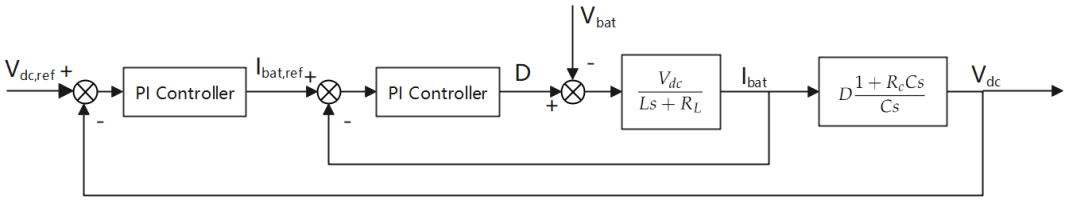


Figure 3.26: Double closed-loop control block diagram of the bidirectional DC-DC converter.

The voltage open-loop transfer function is,

$$G_{o,v}(s) = G_{PI,v}(s)G_{voltage}(s) = D(K_{P,v} + \frac{K_{i,v}}{s})\frac{1 + R_c Cs}{Cs} \tag{3.19}$$

Since the value of $R_c C$ is too small Equation 3.19 is reduced to,

$$G_{o,v}(s) = D(K_{P,v} + \frac{K_{i,v}}{s})\frac{1}{Cs} \tag{3.20}$$

To reduce the system order and make the system easy to control, same as the current loop controller, pole-zero cancellation method is used. The voltage open-loop transfer function is further reduced to,

$$G_{o,v}(s) = \frac{DK_{p,v}}{Cs} \tag{3.21}$$

When the gain is -3dB, the signal is cut off. The cut off frequency $\omega_{c,v}$ can be obtained,

$$\omega_{c,v} = \frac{DK_{p,v}}{c} \tag{3.22}$$

The system switching frequency $f_s = 5kHz$. For the outer voltage control loop,

$$\begin{cases} \omega_{c,v} = \frac{DK_{p,v}}{C} = 2\pi f_{c,v} \\ f_{c,v} = 50 \end{cases} \tag{3.23}$$

The voltage close-loop transfer function,

$$G_{c,v}(s) = \frac{100\pi}{s + 100\pi} \tag{3.24}$$

Based on the double closed-loop control block diagram as shown in Figure 3.26, the controller closed-loop transfer function is decided,

$$G_{closed} = (K_{P,v} + \frac{K_{i,v}}{s}) \times G_{c,c} \times \frac{D}{Cs} = \frac{5922}{0.006s^2 + 18.85s + 5922} \tag{3.25}$$

Using MATLAB the bode diagram of the double closed-loop transfer function has been plotted, as shown in Figure 3.27. From the bode plot, the system bandwidth meets the requirements, and the system has a good dynamic response.

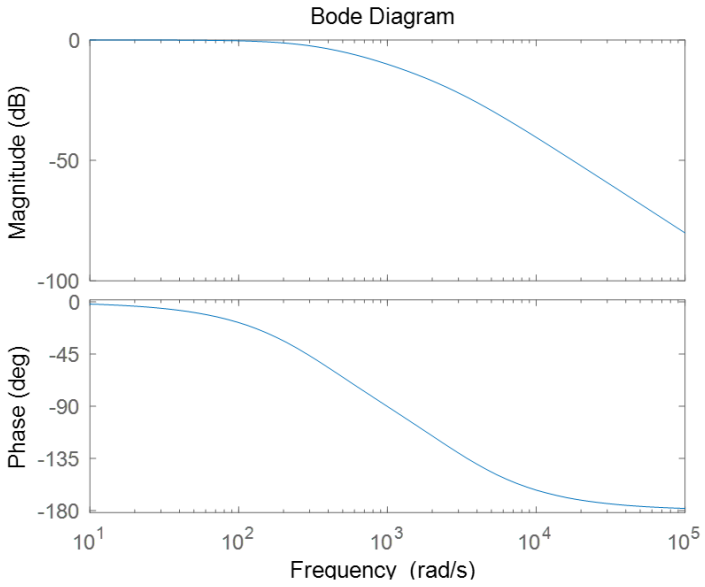


Figure 3.27: Bode diagram of the closed-loop transfer function.

3.4.4 V/f control

A simple open-loop V/f control is implemented in this system to control the motor speed. The induction machine control block is shown in Figure 3.28. In order to let the induction machine

operate under constant flux, the ratio of V/f should be kept constant. Therefore, for the IM control, the frequency of the three-phase voltage is determined by the motor's reference speed, the voltage amplitude is determined by the frequency and the constant V/f ratio. The three-phase reference voltage is generated and inputs to the SVPWM generation block to generate the six gate signals for the three-phase inverter.

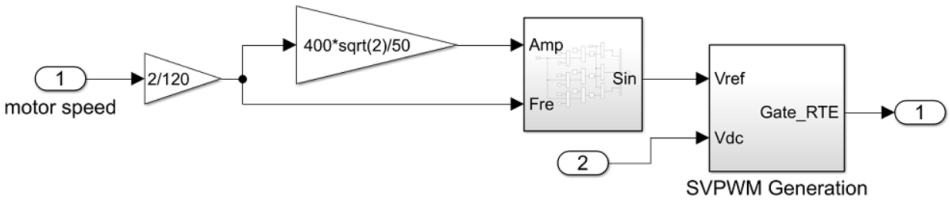


Figure 3.28: IM control blocks.

3.4.5 Central Management System

To maintain the safe and stable operation of the system, central management control is implemented. As described in Section 2.4.4, the PV fed water pumping system designed in this project is able to operate under 4 modes.

The central management subsystem is built based on the control diagram shown in Figure 2.13. In the real-time simulation, the central management subsystem model is shown in Figure 3.29. According to the battery SOC and the system on&off command, the system operation mode is decided. Based on the system operation mode, the motor reference speed and the solar irradiance that on the PV array are sent to the motor controller and the PV model.

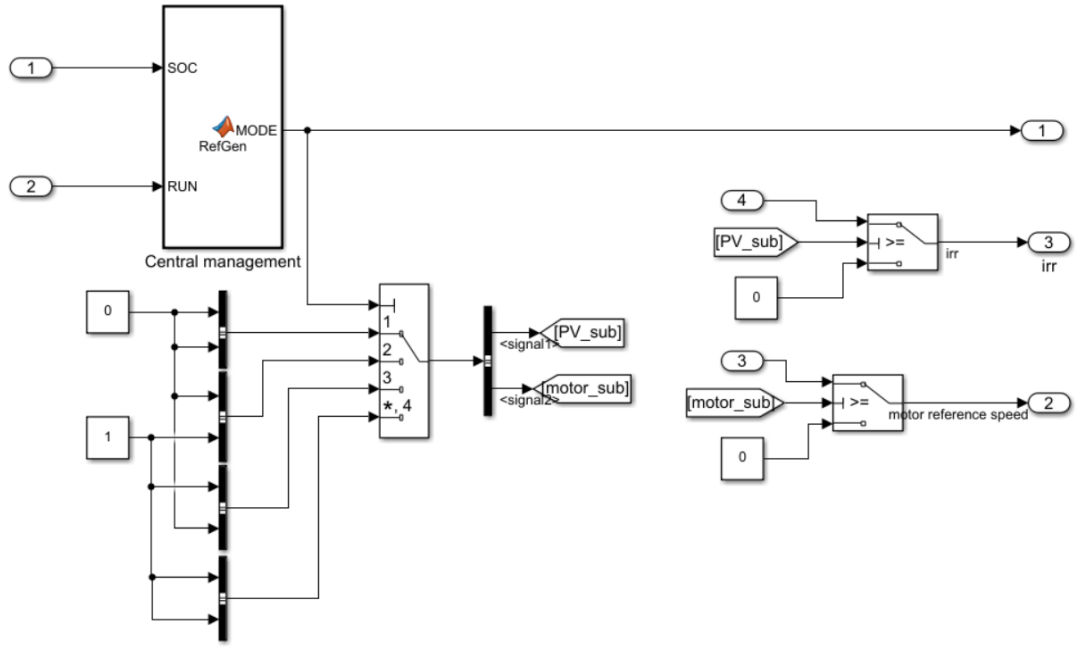


Figure 3.29: Central management subsystem.

4 IMPLEMENTATION OF SYSTEM HIL SIMULATION

After implementing the SIL simulation of the solar array fed water pumping system, some part of the system has been replaced and implemented by real hardware. In this project, the hardware part includes two three-phase inverters and their gate drivers, a current/voltage measurement board. The controller was still simulated in the real-time simulator, as described in Section 3.4. In this chapter, the used boards are introduced and described. The communication between the external hardware and the OP4510 real-time simulator through I/Os is achieved and explained, eventually, achieving the HIL simulation.

Two HIL testings have been done. The first one is the battery-in-loop simulation, in which the battery subsystem is implemented as the external hardware part and the rest of the system is simulated in the real-time simulator. The second one is the battery-motor-in-loop simulation, in which the system is controlled to operate under mode 2. The external hardware includes the bidirectional dc-dc converter, the three-phase inverter, the DC power source and an induction motor.

In the battery HIL testing, the battery subsystem is implemented by real hardware. After connecting an inductor, one phase leg of a three-phase inverter is used to construct the bidirectional dc-dc converter. The bidirectional dc-dc converter works under boost mode. The input current (can be seen as the battery current I_{bat}) and the output voltage (can be seen as the DC bus voltage V_{dc}) is measured by the measurement board. The results are transferred to the controller in the OP4510 simulator through I/Os. The CPU generates the PWM signals and output to the bidirectional dc-dc converter according to the generated control signals. Eventually achieving the closed-loop control of the battery subsystem. Since other parts of the system are simulated in the real-time simulator, the measured Vdc value is input to the controlled voltage source in the circuit model as the DC-bus voltage. As a result, from the simulated PV array and motor side, the DC bus voltage is kept constant. The system diagram of the battery-in-loop simulation and the signal communications are shown in Figure 4.1. This figure describes every part of the system, introduces what models are simulated in CPU and what models are simulated in FPGA, as well as shows how the simulated models are interfaced with the external hardware.

In the battery-motor HIL testing, since the system is controlled to operate under mode 2, only the battery and motor subsystems operates. Based on the battery-in-loop simulation, a real three-phase inverter is connected on the bus side of the bidirectional dc-dc converter. The CPU generates the SVPWM signals for the three-phase inverter and achieving the motor speed control. The system diagram of the battery-motor-in-loop simulation and the signal communications are shown in Figure 4.2.

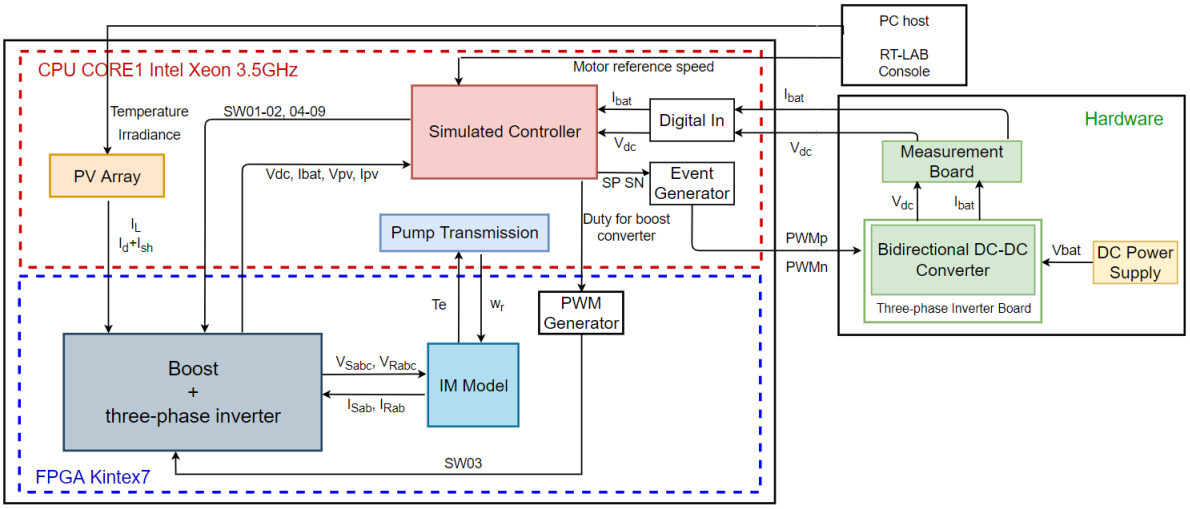


Figure 4.1: The battery HIL simulation system diagram and the signal communications.

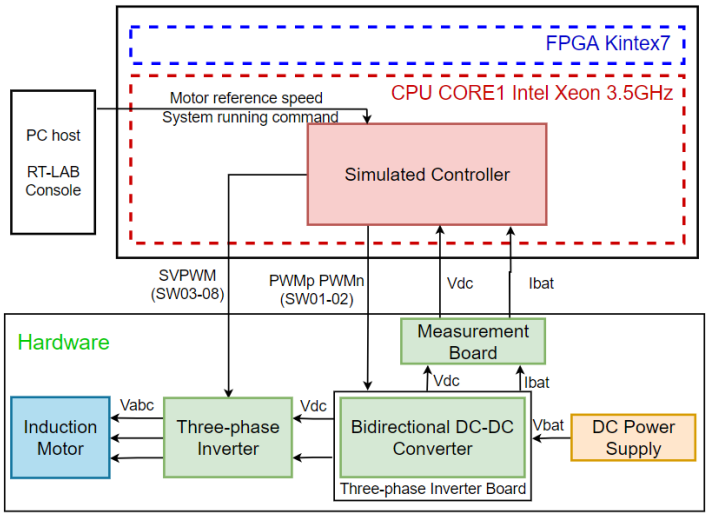


Figure 4.2: The battery-motor HIL simulation system diagram and the signal communications.

4.1 DESCRIPTION OF THE EXTERNAL HARDWARE

4.1.1 Three-phase Inverter Board

The used three-phase inverter and its three gate drivers are shown in Figure 4.3. One gate driver is responsible for one phase leg of the mentioned inverter. In order to avoid the unwanted triggering of MOSFETs, complementary PWM signals should be given to the two switches on each phase leg of the inverter.

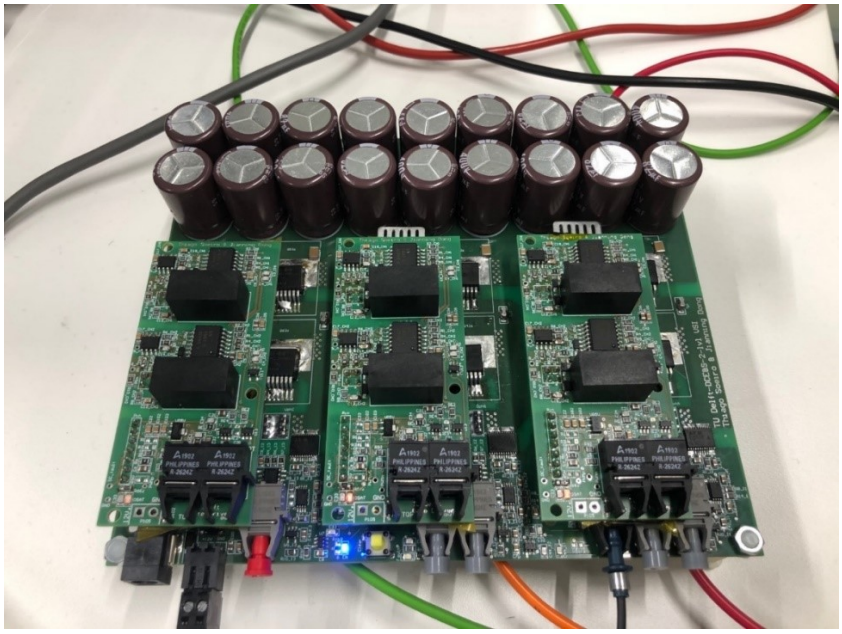


Figure 4.3: The used three-phase inverter and its gate drivers.

The PWM signal is mapped to the simulator's module and then transferred to the gate driver board. This board is able to convert the DC voltage to the three-phase AC supply and is also able to implement overcurrent detection. When failures occur fault signal will be generated and resulting in a shut-down of the entire board. Figure 4.4 shows the system description. More details about the mentioned modules in Figure 4.4 are described in Appendix A.

4.1.2 Measurement Board

The used measurement board is shown in Figure 4.5. This measurement board is able to measure one current and one voltage at a time. The value of the measured current/voltage can be either output by analog signal or digital signal.

There are three signal channels to be selected, the analog measurement channel, the frequency channel and the delta-sigma measurement channel. For the analog measurement channel, the differential signal is output by the internet cable. For the frequency channel, the measured signal is processed by the inverting amplifier circuit and then output to the voltage-controlled silicon oscillator LTC6990. LTC6990 generates a frequency that is proportional to the input voltage and the frequency

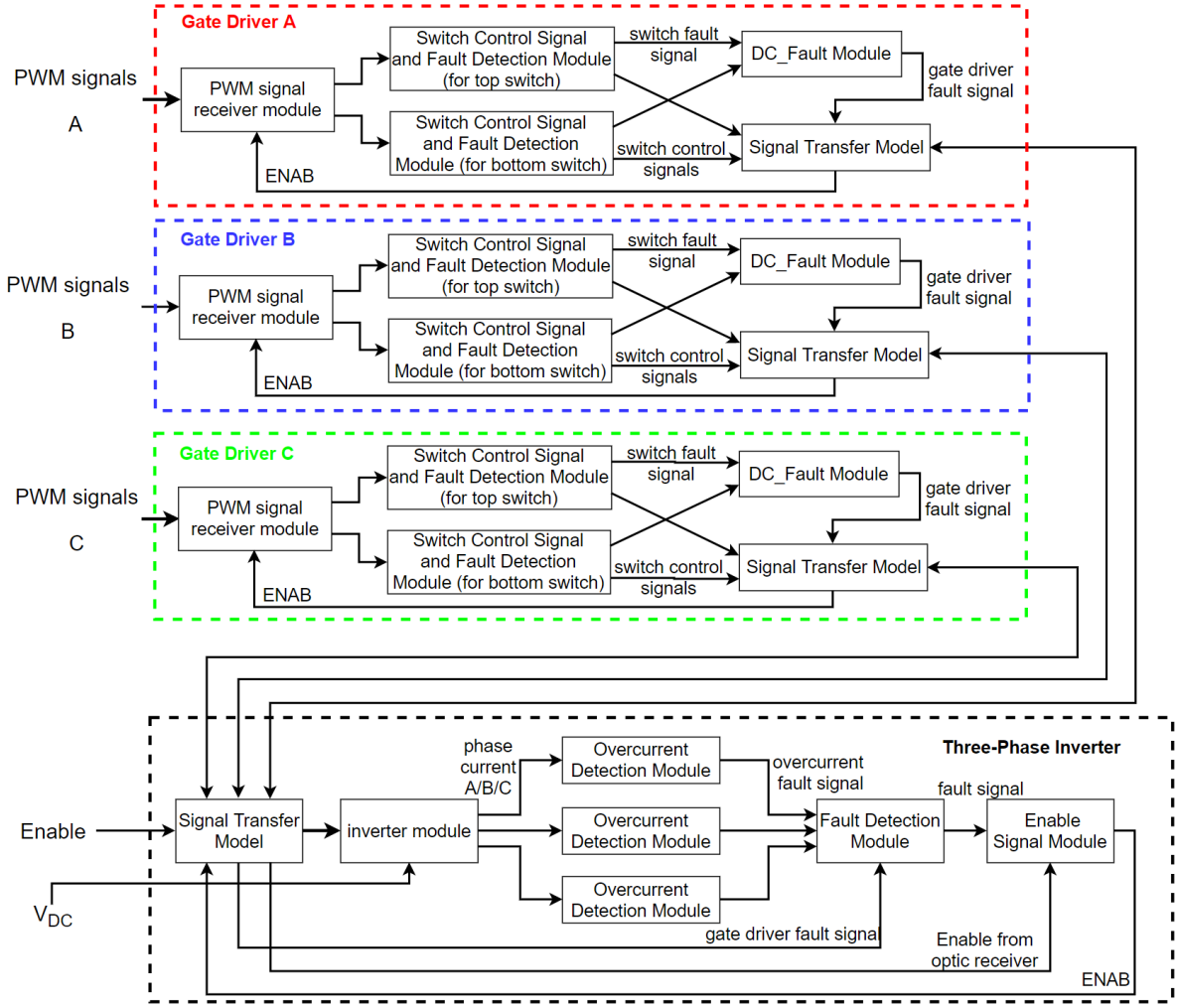


Figure 4.4: System description of the three-phase inverter and its gate drivers.

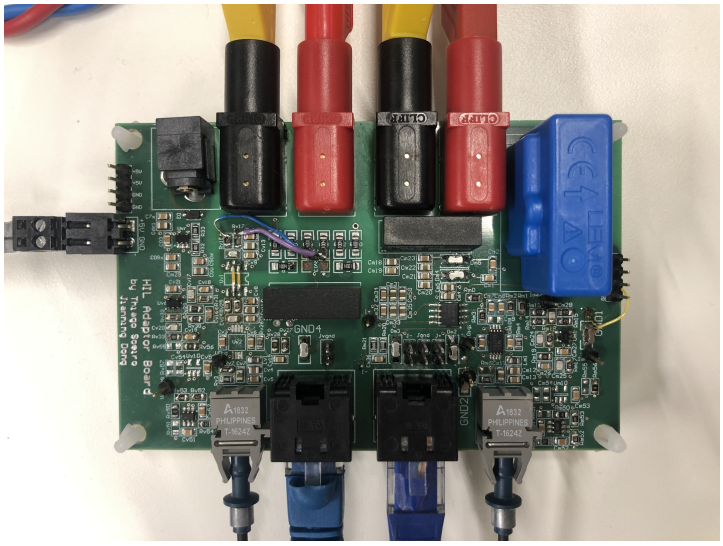


Figure 4.5: The used measurement board.

is output by the fiber optic transmitter. For the delta-sigma measurement channel, the input signal is sampled by the delta-sigma modulator ADS1203 and then outputs the Manchester-encoded data that carrying the data information of the measured signal. (Because the Manchester decoder is not ready so far, the delta-sigma measurement channel is not used in the project). In this project, the value of the measured current/voltage can be either output by analog signal or digital signal. Figure 4.6 shows the system description of the measurement board.

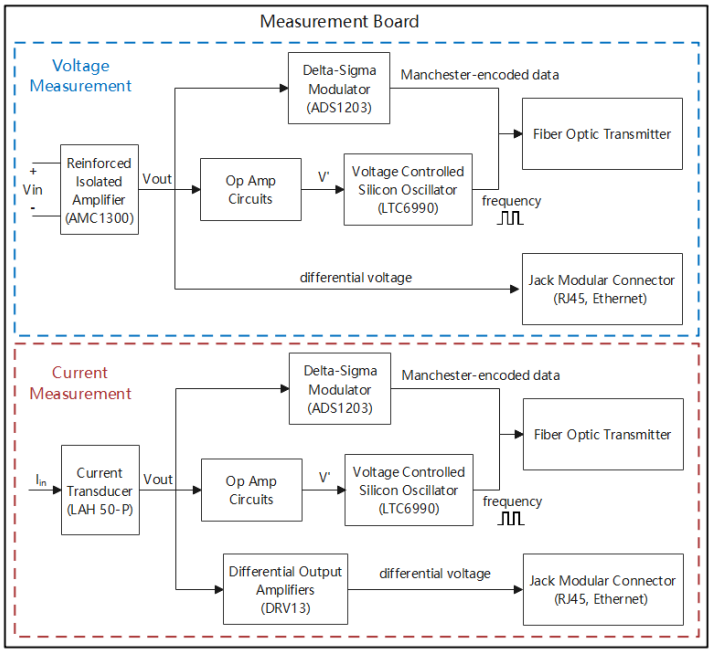


Figure 4.6: System description of the measurement board.

4.1.3 Induction Motor

For master students who work in the ESP Lab alone, voltages exceeding 50V are not allowed to use. In the HIL testing, the maximum output power of the used DC voltage source that replacing the battery is only 300W. Due to these restrictions, the motor HIL simulation has been done neither with the selected IM described in section Section 2.3.1 nor with the big induction machine placed in the lab. The real motor used in the hardware-in-loop experiment is a small induction motor, the M800006 from EMsynergy provided by the DCE&S group. The motor parameters are shown in Table 4.1.

Model number	M800006	Rated output	13.6W
Rated voltage(line to line)	14.7V RMS	Number of poles	4
Frequency	50Hz	Speed at full load	1121rpm

Table 4.1: M800006 parameters.

4.2 COMMUNICATION BETWEEN THE SIMULATOR AND THE EXTERNAL BOARD

4.2.1 Data Conversion Module

From Section 4.1.2, the measurement board transfers data through fiber optic receivers/transmitter. Since the simulator output data through series communication ports, a signal conversion module is needed. Figure 4.7 shows the signal conversion module (the white and black boards) for the used simulator, which is able to convert the signal and output/input data through internet cable or optic fiber.

4.2.2 Communication Through I/Os of OP4510 Simulator

In order to achieve the control of the battery subsystem, as described in Section 3.4.2, the voltage on the bus side of the bidirectional dc-dc should be feedback to the voltage PI controller and generate battery reference current, the battery current should be feedback to the current PI controller and generate duty cycle for the bidirectional dc-dc converter. Finally, the duty cycle and the desired switching frequency are input to the RTE PWM generator from the RT-EVENT library. At this stage, the PWM signals are in the datatype of RTE. Same for the motor subsystem, the measured Vdc has been given to the SVPWM generation block and the generated SVPWM signals are in RTE datatype. Different from what in the Section 3.4, in the HIL simulation, the bidirectional dc-dc converter and inverter run as real hardware outside the simulator. Therefore, the PWM signals should output the simulator through I/Os. The PWM signals generated by the blocks in Figure 3.22 are mapped to the DO models of OP4510 through the event generator as shown in Figure 4.8.

The digital channels are used to transfer the measured values of current and voltage. These values are sent to the simulator through the data transfer module in Figure 4.7. These data are mapped to the digital in block, as shown in Figure 4.9, and input to the simulated controller in the CPU model.

Figure 4.7: Data Conversion Module.

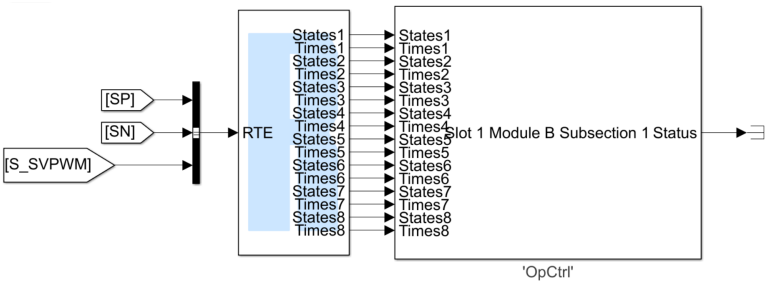


Figure 4.8: PWM signals in RTE data type are sent out through Event Generate Block.

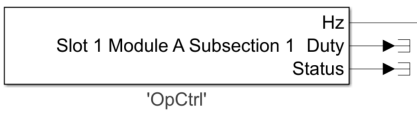


Figure 4.9: Digital In block.

4.2.3 Calibration of the Measurement Board

Because the current and voltage value implemented on the converter is relatively low compared to what the measurement board was designed for, frequency (digital) channels are selected to maintain the sampling accuracy. Before implementing the closed-loop control, different current/voltage values are input to the measurement board, the corresponding output frequency is recorded. Using Matlab to process these two groups of data, the relation between the input voltage/current and the output frequency for the voltage/current digital measurement channel has been found. The original data sampled from the measurement board is processed in the CPU model, eventually, the real measured current/voltage values are shown. This step is achieved by the blocks in Figure 4.10.

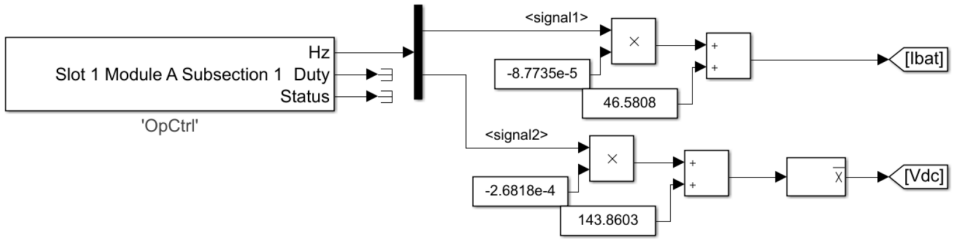


Figure 4.10: Signal calibration.

5 RESULTS AND DISCUSSION

5.1 MAXIMUM POWER EXTRACTION OF PV ARRAY

When testing the PV array subsystem and its control separately, a DC voltage source has been used in the model to emulate the DC bus voltage.

5.1.1 Boost Open-loop Control

Analog-out module has been used to mapping PWM signals from the model in CPU to the analog output channels of the real-time simulator OP4510. An oscilloscope was used to measure and test the PWM signals with different duty cycles. The switching frequency for the boost converter is 10kHz. Figure 5.1 shows the measured PWM signals, the switching period is 100us. The turn-on time duration for the PWM signal matches the duty cycle.

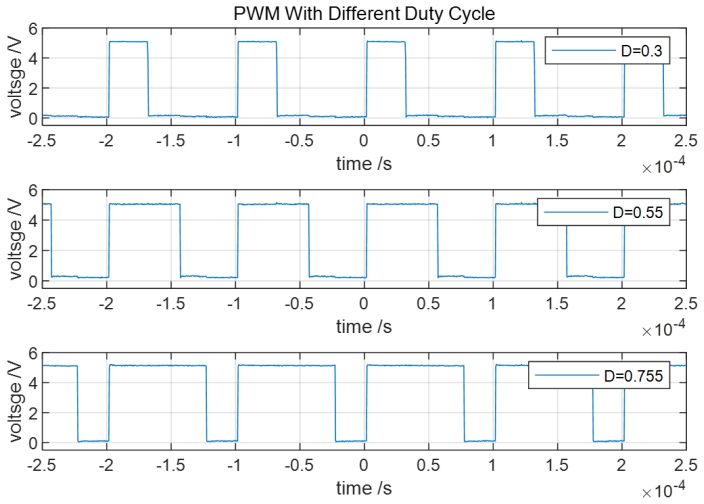


Figure 5.1: Output PWM signals with different duty cycles.

5.1.2 Closed-loop Control

When the MPPT control is implemented, according to the solar irradiance the P&O method would give the relevant reference value for the PV voltage V_{mp_ref} at the maximum power. The difference between the PV voltage measured from the PV array model and the V_{mp_ref} is input to the PI controller.

Then the desired duty cycle for the boost converter is generated. As a result, the PV array are able to generate the maximum power during operation.

In Figure 5.2, the given solar irradiance varies between $50W/m^2$ and $400W/m^2$, output PV voltage follows the reference value. Ignoring the slight deviation between the built model and the actual PV array, the maximum power points for different solar irradiances in the real-time simulation matches the I-V curve from Figure 2.9. When the solar irradiance is $250W/m^2$, the PV voltage and current at the maximum power point are 436V and 3A. This PV array subsystem is able to achieve maximum power tracking.

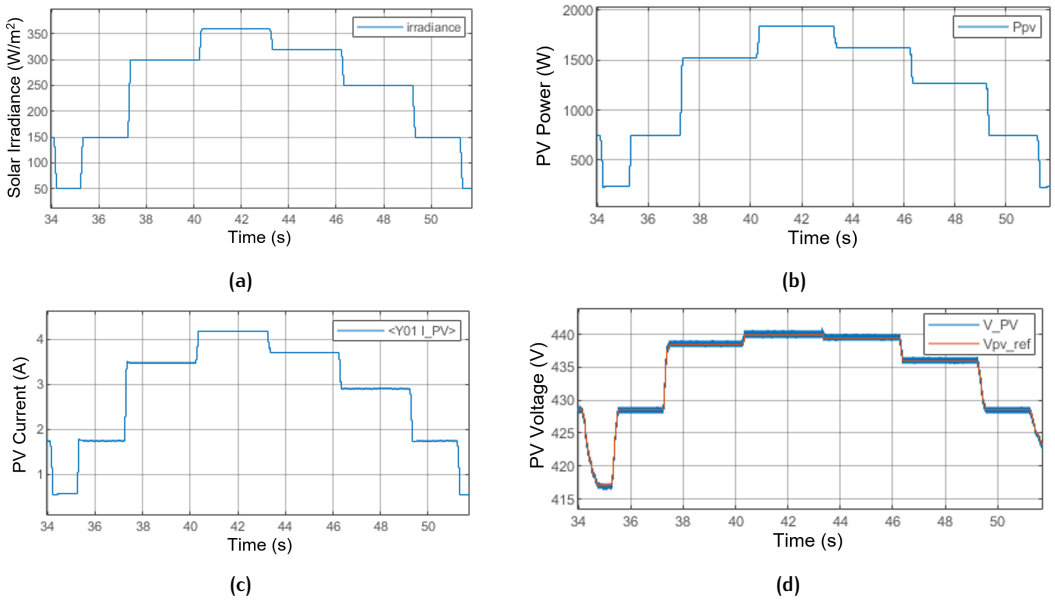


Figure 5.2: Maximum power tracking of the simulated PV array subsystem.

5.2 DC BUS VOLTAGE CONTROL OF THE BATTERY

5.2.1 Open-loop Control of the Bidirectional DC-DC Converter

Complementary PWM signals are used for the top and bottom switches of the bidirectional dc-dc converter. Using the analog-out block and an oscilloscope, the PWM signals for the converter from the real-time simulator were measured. The PWM signals were given to the gate driver board described in Section 4.1.1. Then, the gate signal from the gate driver to the converter board was measured.

When the duty cycle for the top switch is 0.1, the measured signals are shown in Figure 5.3. The switching frequency for the bidirectional dc-dc converter is 10kHz. -5V voltage is given to the switch gate to ensure the turn-off of the switch. 13.3V voltage is given to the switch to turn on the switch.

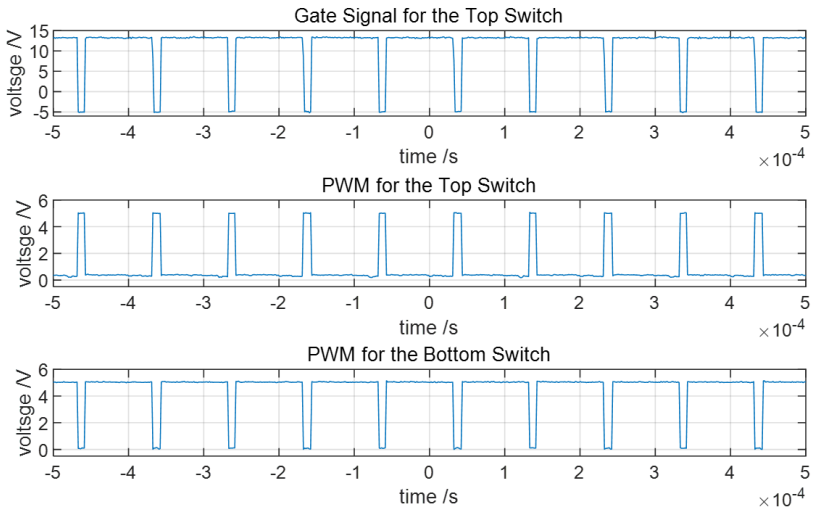


Figure 5.3: PWM and gate signal for the bidirectional dc-dc converter.

5.2.2 DC Bus Voltage Control

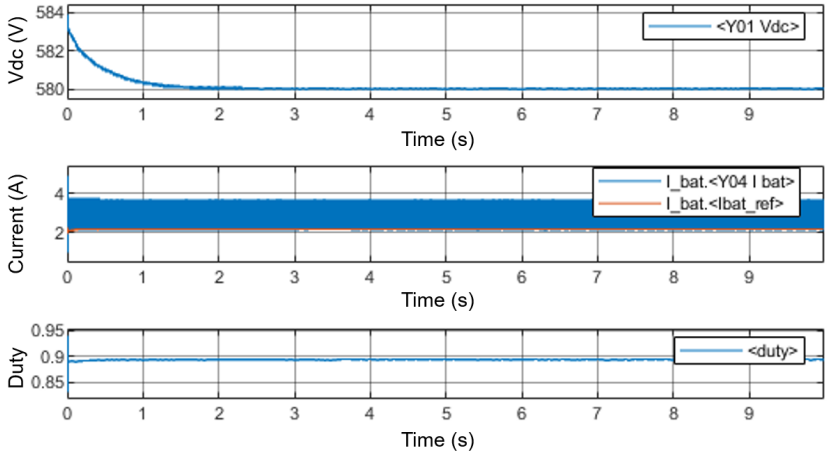
Both SIL test and HIL test have been implemented on the battery subsystem.

When implementing the SIL simulation, the bus voltage V_{dc} and the battery current I_{bat} were measured from the converter model in FPGA. The load was a resistor. The voltage and current that measured from the boost model executed in the FPGA were sampled by the CPU. Then the simulation results were seen in the scope from the console subsystem. Testing results are shown in Figure 5.4. The CPU time-step is 20us, therefore the waveform is in steps and the time duration for each step is 20us. The desired DC bus voltage is 580V. When the battery provides the load with 1500W power, the desired duty cycle is around 0.89, as shown in Figure 5.4a. Figure 5.4b shows the inductor current (battery current), the current ripple is 1.75A and in 10kHz.

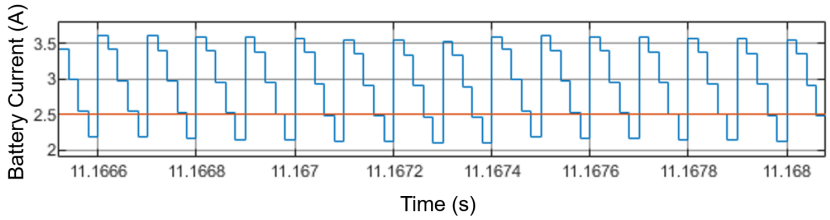
When implementing the HIL real-time testing, the bidirectional dc-dc converter operated at the boost mode. In the HIL testing, the actual voltage on the bus side of the converter and the current on the battery side of the converter were sampled by the measurement board. The measured values were input to the simulator through I/Os. Because of the voltage limitation when working in the lab, the HIL testing of the battery subsystem was implemented under lower voltage. The bus voltage and the battery voltage that selected in this system have been reduced by 60 times at the same time. In other words, in the HIL testing, the actual used battery side voltage was 8V and the bus side voltage was 9.6V. A resistor was used as load on the bus side.

The HIL real-time simulation results are shown in Figure 5.5. After turning on the system, the bus side voltage follows the reference value. The duty cycle at steady-state is around 0.8. In Figure 5.5c, the battery side current is shown. Same as in the SIL simulation, the HIL simulation results are sampled by the CPU. Therefore, the waveforms are in steps. The current fluctuation is caused by the switching and the current ripple is 1.75A for the used voltage and inductance.

Under the boost model, the duty cycle for the bottom switch of the bidirectional dc-dc is 0.1724, as calculated in Section 2.3.6. In this subsystem, the output duty cycle from the controller is for the top switch. Since complementary PWM signals are given to the top and bottom switches, the theoretical duty cycle for the bottom switch is 0.8276.



(a) bidirectional dc-dc converter performance.



(b) Inductor current ripple

Figure 5.4: SIL simulation results.

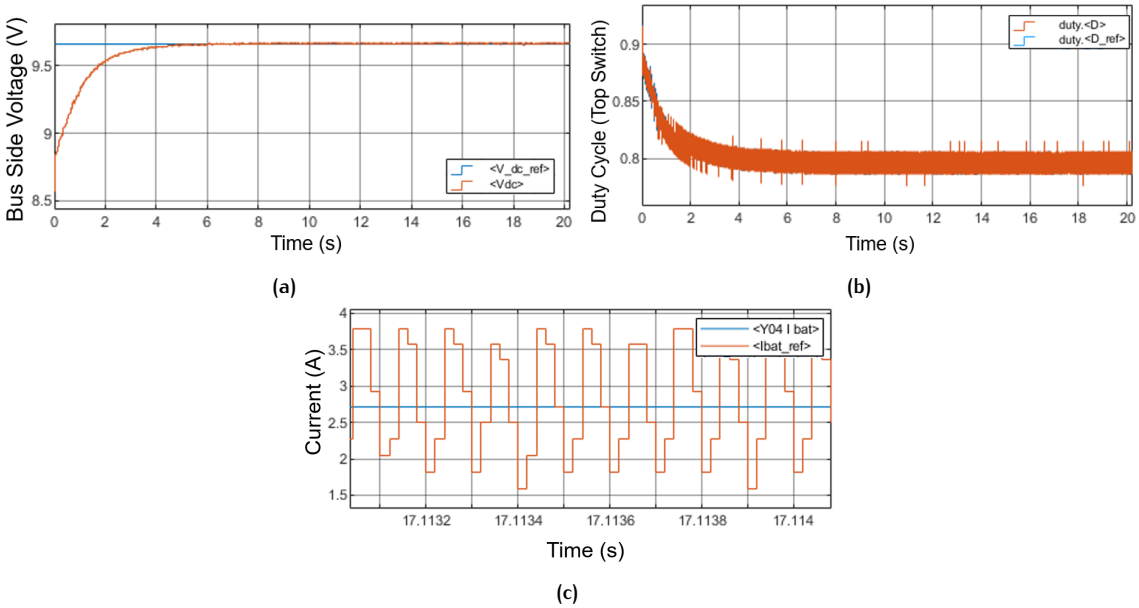


Figure 5.5: HIL bidirectional dc-dc converter performance.

As shown in Figure 5.4, in the SIL testing D=0.89. A battery model has been implemented in the SIL simulation to charge the DC bus. The used battery voltage is 480V. However, according to the battery characteristics, the operation voltage of a battery is not a fixed value but varies over a voltage range. When the battery SOC is high, the operation voltage could be higher than 480V. When the battery SOC is low then the operating voltage could be lower than 480V. The SIL simulation result shown in Figure 5.4 is when the SOC equal to 70, so the actual bidirectional dc-dc converter battery side voltage is higher than 480V. As a result, the duty cycle shown in the figure is higher than 0.8276.

As shown in Figure 5.5, in the HIL testing D=0.8. The duty cycle is lower than the calculated value. The reason is, in the HIL testing, a dc power supply has been used to replace the actual battery. Therefore the battery side voltage is fixed. Also, different from the SIL simulation where more ideal switches are used, in the HIL testing the actual efficiency of the real bidirectional dc-dc converter is lower. To complement the power loss, more power is needed to be generated. As a result, the duty cycle shown in the HIL simulation is lower than 0.8276.

5.3 MOTOR SPEED CONTROL

5.3.1 Inverter Model

In order to validate the real-time model of the three-phase inverter, the output line-to-line voltages Vab, Vbc and Vca were measured from the model and are output through the analog output I/O channels. An oscilloscope was used to measure these analog signals. Figure 5.6 shows the measured output three-phase voltage required from the motor for operating at the rated working state. The frequency of the voltage is 50Hz. The voltage range is ± 580V, where 580V is the bus voltage Vdc of this standalone system.

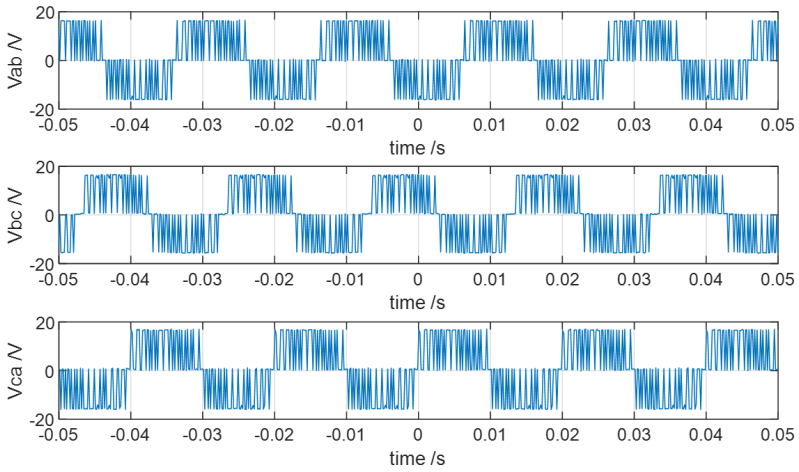
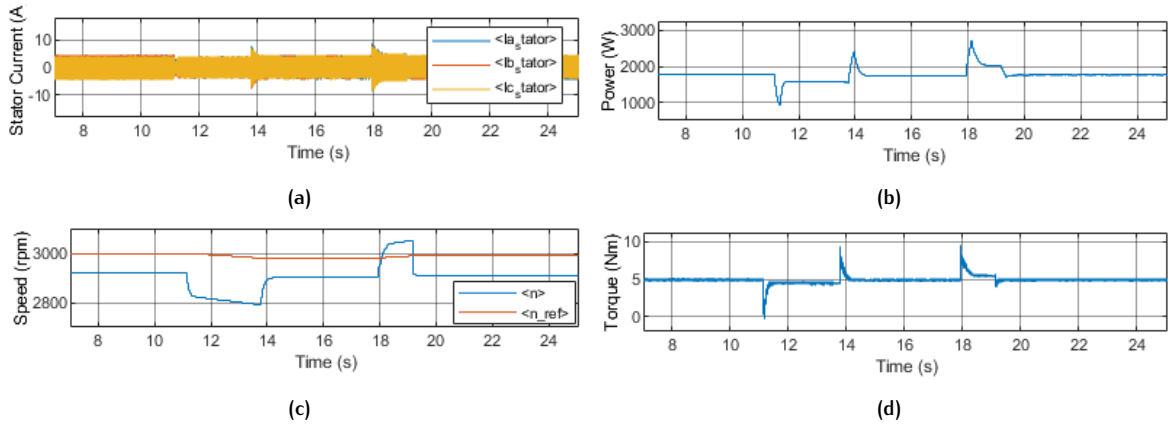


Figure 5.6: Three-phase line-to-line voltage measured from the inverter model.

5.3.2 Pump Model and Motor Speed

As described in Section 3.3.3, the load torque for a pump is proportional to the square of the rotor rotational speed. In this specific case, during the motor operation, the motor satisfies the mathematical relationship $T_e - K_{pump}\omega^2 = J(\frac{dw}{dt})$. As a result, as the rotor accelerates the load torque increased as well. At steady-state, the motor generates torque $T_e = K_{pump}\omega^2$. In this system, the motor is required to operate at the rated speed which is 2920rpm, as shown in Table 2.1, therefore Te=4.9Nm at steady-state.

The real-time test for the induction machine model and the three-phase inverter model is implemented. Figure 5.7 shows the system performance of the machine. The machine reference speed is 3000rpm at the beginning and is switched to 2980rpm at t=11s, switched to 2990 at t=18s. Since the open-loop scalar control is implemented, a rate limiter is used to limit the changing rate of the motor reference speed. It takes some time to change the speed reference value. Figure 5.7c shows that as long as the reference value is stabilized, the motor speed follows the reference speed immediately, and the slip is 0.027.



(a) (b) (c) (d)

Figure 5.7: Induction machine performance during speed changing.

5.3.3 Battery-motor HIL testing

As described in Chapter 4, battery-motor HIL testing has been done. The used motor in the lab testing has been introduced in Section 4.1.3. The battery-motor HIL testing was implemented based on the battery HIL testing in Section 5.2. In this testing, the bidirectional dc-dc converter works in the boost mode. To fulfil the motor desire, the bus side voltage of the bidirectional dc-dc converter has been controlled to be 21V. The battery side voltage was 8V. Then the duty cycle for the upper switch should be $d = \frac{8}{21} = 0.381$.

The system performance of the battery-motor HIL testing is shown in Figure 5.8. Figure 5.8a is the waveform of the duty cycle for the bidirectional dc-dc. At steady-state, the duty cycle is around 0.38-0.4, which matches the calculated value. Figure 5.8b is the bus voltage, the measured bus voltage follows the reference value. Figure 5.8c shows the inductor current (battery current), the current ripple is 5A and in 10kHz.

Using current probes and oscilloscope, the motor three-phase stator currents are measured. As shown in Figure 5.9 the current amplitude is 1.05A and the frequency is 50Hz.

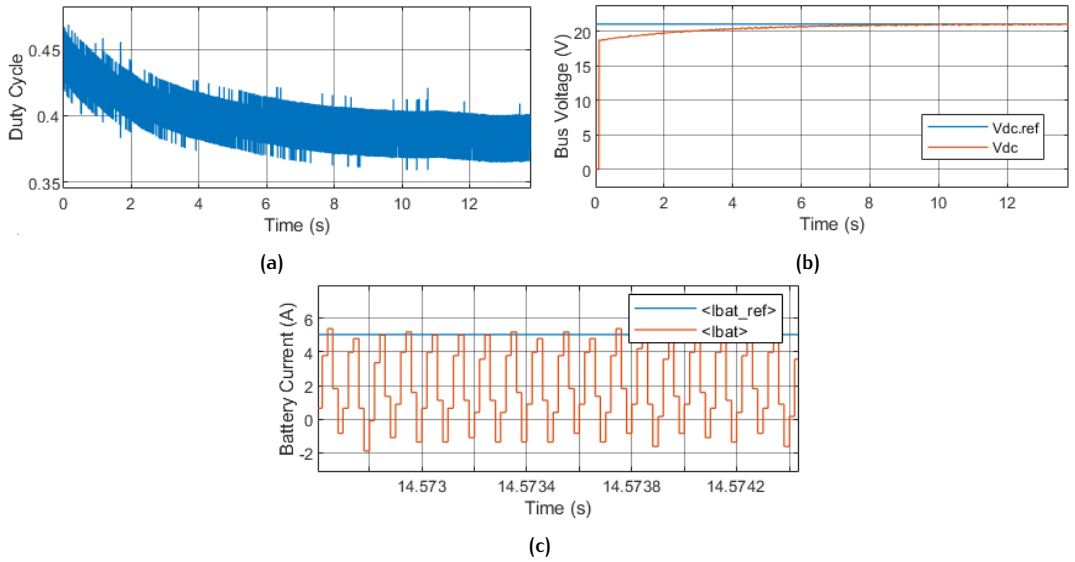


Figure 5.8: Battery-motor HIL testing.

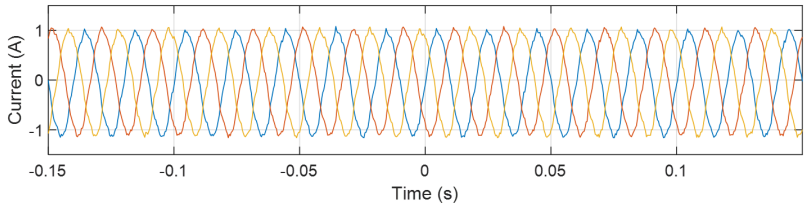


Figure 5.9: Battery-motor HIL testing-motor stator three-phase current.

5.4 SYSTEM PERFORMANCE

According to the operator requirements and the current system working condition, the operating mode of the designed PV pumping system is decided by the central management subsystem. As the control diagram described in Section 2.4.4, based on the current SOC, there are three kinds of switching processes.

1. When $SOC_{min} \leq SOC \leq SOC_{max}$ and the pump does not need to operate, the PV array will charge the battery until $SOC > SOC_{max}$ and then enters the standby mode. The system will switch from mode 3 to mode 1. If pumping is desired, the motor will start to operate and the system works under mode 4.

2. When the battery SOC is about to be charged to the maximum safety value ($SOC > SOC_{max}$) and the pump does not need to operate, then the system will enter the standby mode (Mode 1). If the pump is desired to operate, then the PV subsystem will be cut off and only the battery itself will

power the motor. The system switches from mode 4 to mode 2 and will be locked in mode 2 until the battery is discharged to SOC≤50.

3. When the battery SOC is about to be discharged below the minimum safety value ($SOC > SOC_{max}$), the system will directly enter mode 3. The PV array will charge the battery and the system is locked in this mode until the battery SOC reaches 50%.

In this section, three switching conditions have been selected and the system performance has been presented.

5.4.1 Given System Running Command

If the battery SOC is within the safety range, the system would operate either under mode 3 or under mode 4 depends on whether the system running command is given. After given the system running command the system would switch from mode 3 to mode 4. The motor will start rotating and the battery will switch from the charging mode to the discharging mode according to how much power is generated by the PV array. In this simulation, the solar irradiance varied between $50W/m^2$ and $400W/m^2$ and the system running command was given at 6.7s.

Figure 5.10 shows the motor performance. When the system running command is given at t=6.7s, the motor starts to operate. The motor speed is shown in Figure 5.10a. The total power consumed by the motor is shown in Figure 5.10b.

Figure 5.11 shows the battery performance. Before the system running command is given, the system operates under mode 4. In the meantime, the battery is charged. The SOC increases and the battery current is negative.

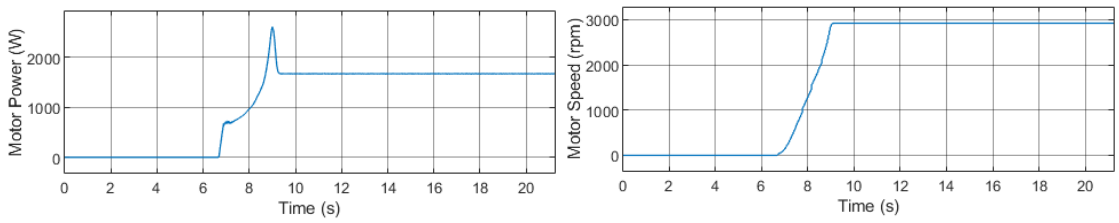
Figure 5.12 shows the PV array performance. From Figure 5.12b, the PV output power always follows the solar irradiance that is shown in Figure 5.12a.

The system overall performance is shown in Figure 5.13. From Figure 5.13a, the bus voltage is able to be controlled at 580V. A voltage spike occurs when mode switching but within the acceptable range. From Figure 5.13b, the system efficiency during the motor operation is between 70%-90%.

At steady-state, there is a 10W loss on the bidirectional DC-DC converter, 175W loss on the three-phase inverter and motor, and 120-550W loss on the boost converter according to the solar irradiance. When the solar irradiance is $150W/m^2$, the power loss on the boost converter is 275W wihch is almost 60% of the total loss. The system efficiency can be calculated as $\eta = \frac{P_{motor}}{P_{pv}+P_{bat}} = \frac{1495W}{745.2W+1200W} = 0.769$ which is the same as the value shown in Figure 5.13b. Therefore it can be seen that most of the power loss is on the boost converter.

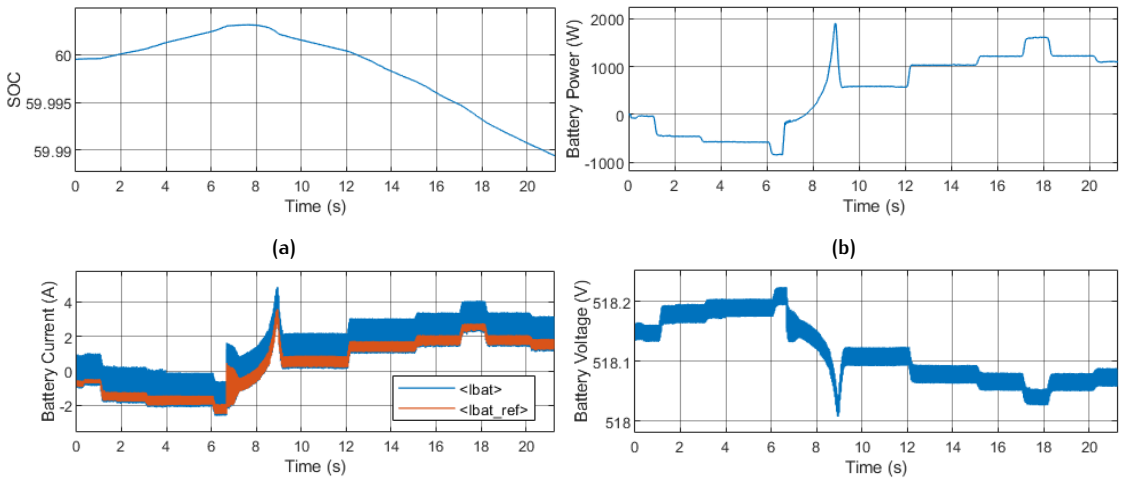
5.4.2 SOC Reaches the Maximum Limitation

When the battery SOC is about to reach the maximum limitation, there will be two situations. The first one is when the system running command is given. At the time, the PV array will be cut out of the system, the battery will completely into the discharging mode and provide sufficient power to the motor. The other situation is when pumping is not required. At the time, the system will switch



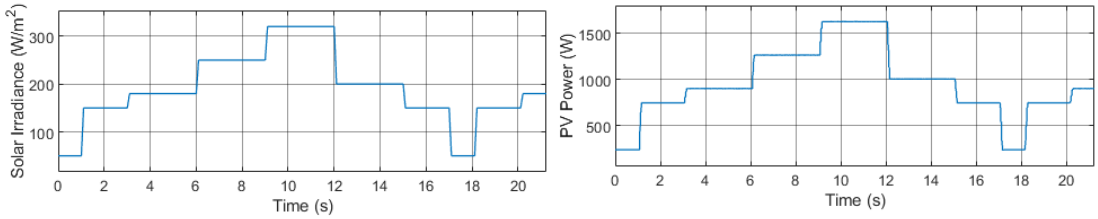
(a) (b)

Figure 5.10: Motor performance when switching from mode 3 to mode 4.



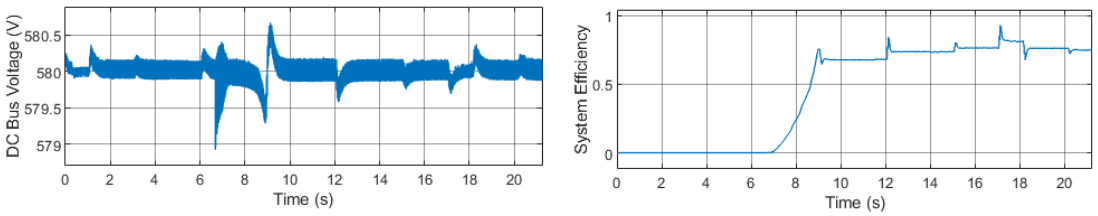
(a) (b) (c) (d)

Figure 5.11: Battery performance when switching from mode 3 to mode 4.



(a) (b)

Figure 5.12: PV array performance when switching from mode 3 to mode 4.



(a) (b)

Figure 5.13: System performance when switching from mode 3 to mode 4.

from mode 3 to the standby mode, mode 1. During this switching, the PV array will be cut out of the system and no power will be generated.

Figure 5.14 to Figure 5.17 show the system performance. During the operation, the solar irradiance is kept at $600W/m^2$. In the beginning, the system operates under mode 4. Because of the sufficient solar irradiance, the PV array is able to not only supply enough power to the motor but also charge the battery. The battery SOC keeps increasing until, at t=5s, the SOC reached the maximum limit. The system reacts immediately and switches to mode 2. Under mode 2 the battery powers the motor alone. At t=10s, the motor stop command is given and the system switches to mode 3. At the time, the PV array starts to charge the battery. As a result, battery SOC starts to increase again. When t=14s, SOC reaches SOC_{max} again and the system switches to standby mode. The whole system stops operation.

Figure 5.14 shows the battery performance. The battery current and power are positive or negative depends on the battery operating mode.

Figure 5.15 shows the PV array performance. From Figure 5.15a the solar irradiance is kept constant at $600W/m^2$. From Figure 5.15b the PV voltage and the output power, it can be seen that when the system operating under mode 1 or 2 no power is generated by the PV array.

Figure 5.16 shows the motor performance. During t=0-10s, the motor is able to keep running smoothly without being affected by the mode switching. After t=10s, the motor is controlled to stop rotating.

Figure 5.17 shows the system DC bus voltage. During mode switching, at t=5s, t=10s and t=14s, voltage spikes occurs on the bus and they are all within the acceptable range.

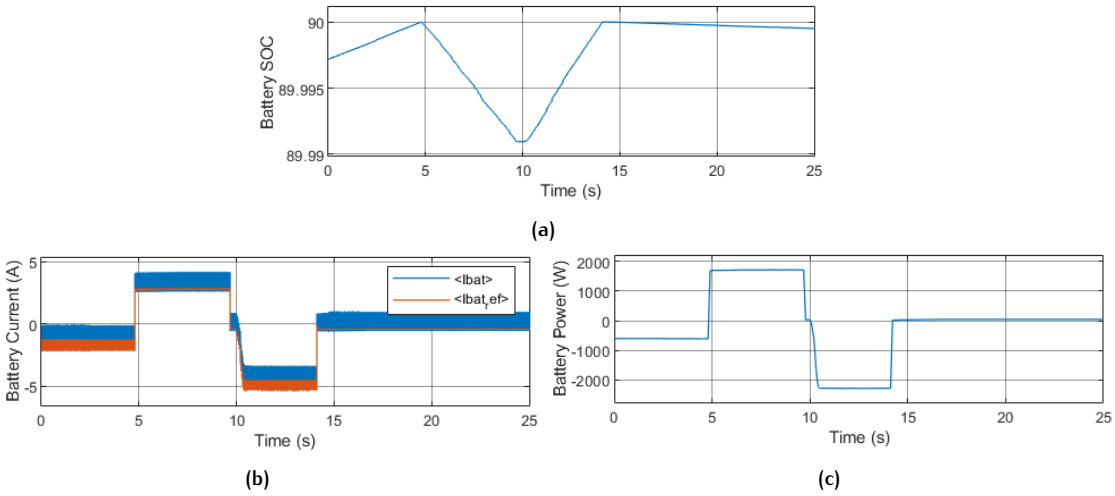


Figure 5.14: Battery performance when SOC reaches the maximum limitation.

5.4.3 SOC Reaches the Minimum Limitation

When the battery SOC is about to go below the battery minimum safety value SOC_{min}, the central management subsystem will react immediately and control the system to operate under mode 3. During this time, the motor stops operate and the battery is charged by the PV array.

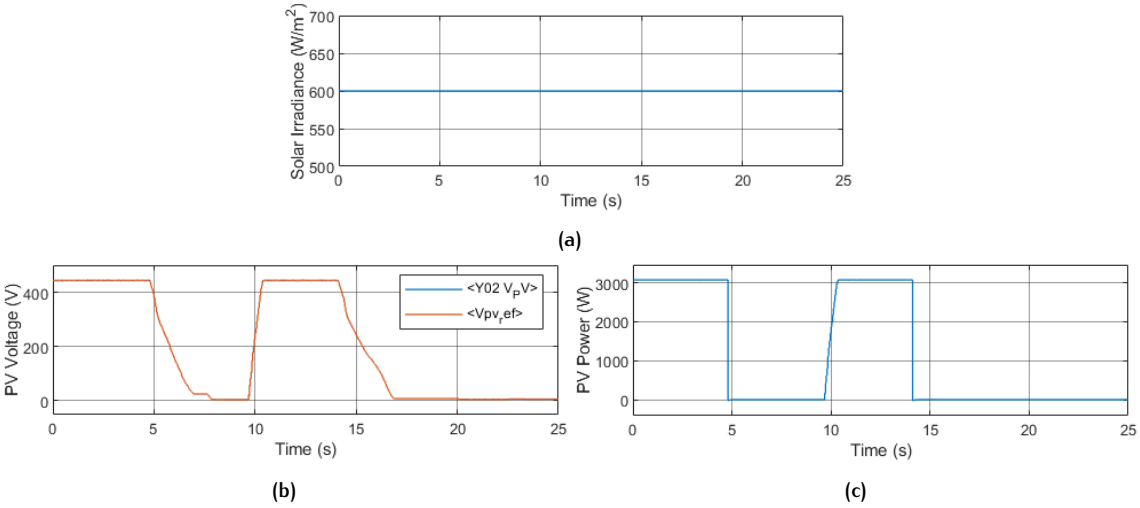


Figure 5.15: PV array performance when SOC reaches the maximum limitation.

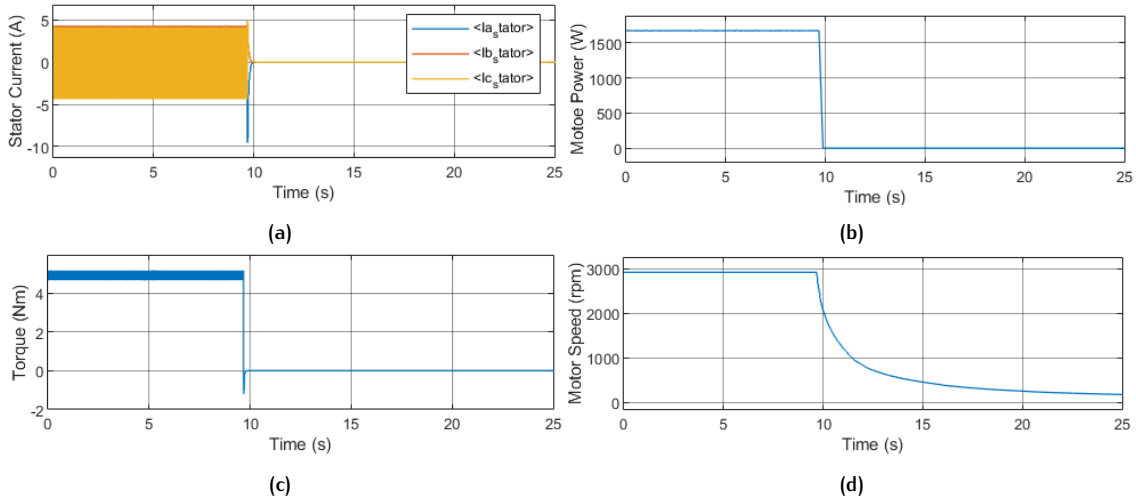


Figure 5.16: Motor performance when SOC reaches the maximum limitation.

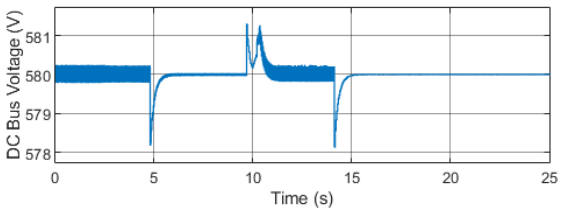


Figure 5.17: DC bus voltage when SOC reaches the maximum limitation.

Figure 5.18 to Figure 5.21 show the system performance when the system switches from mode 4 to mode 3.

As shown in Figure 5.18, before the battery SOC reaches 10 at 4.25s the battery keeps discharging. The battery current is positive and the battery supplies power to the load. The system efficiency is around 75%, as shown in Figure 5.21b. After 4.25s, the system switches to mode 3 and the battery starts storing power. During the mode switching, there is a voltage spike in the DC bus, as shown in Figure 5.21a.

When the system operates under mode 3, the motor is forced to shut down. As shown in Figure 5.19a, after 4.25s the motor speed keeps decreasing.

The PV array performance is shown in Figure 5.20. The PV generated power follows the solar irradiance and the PV array keeps operating under the maximum power point.

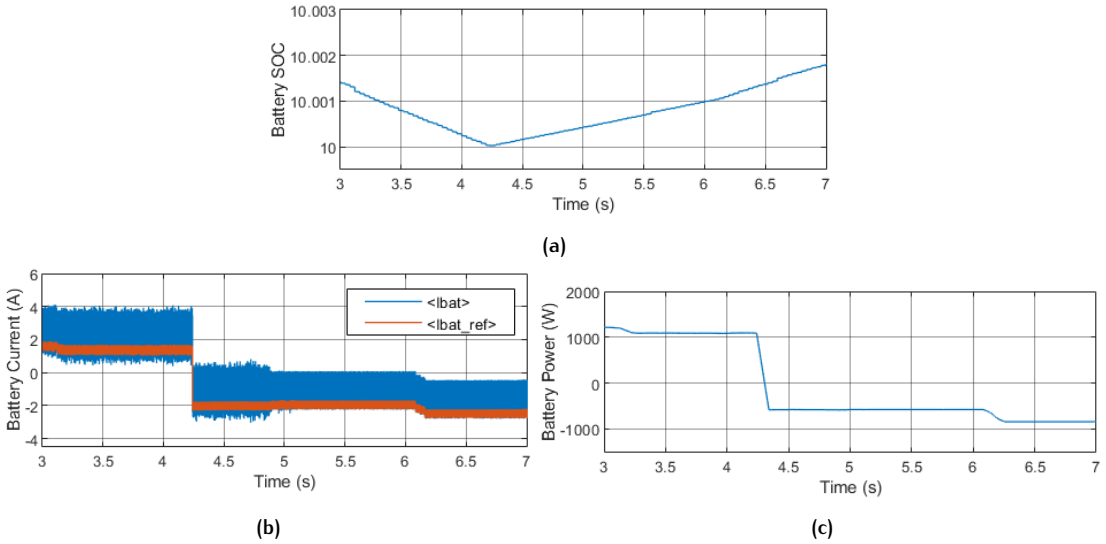


Figure 5.18: Battery performance when switching from mode 4 to mode 3.

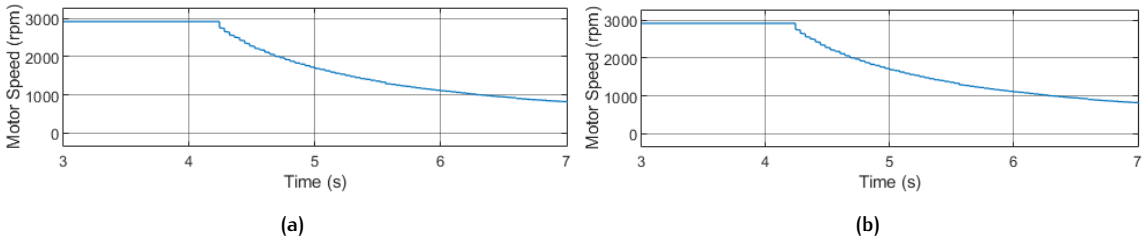
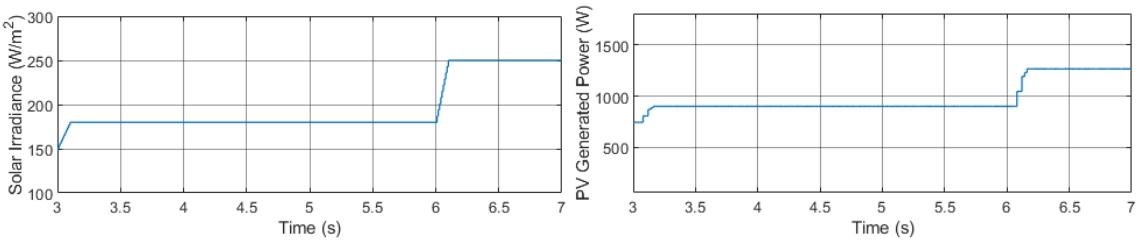
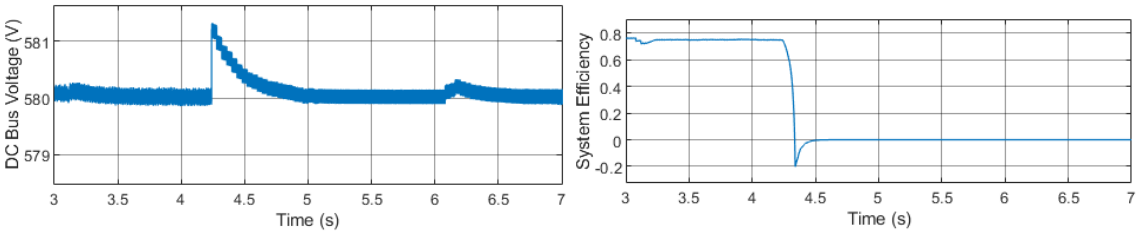


Figure 5.19: Motor performance when switching from mode 4 to mode 3.



(a) (b)

Figure 5.20: PV array performance when switching from mode 4 to mode 3.



(a) (b)

Figure 5.21: System performance when switching from mode 4 to mode 3.

6 CONCLUSIONS AND RECOMMENDATIONS

6.1 CONCLUSION

This project takes Delft, the Netherlands, as a reference and system location to design a solar array fed water pumping system. Based on the OPAL-RT real-time simulation platform, a real-time hardware-in-loop emulation of the PV system has been built. The built system can stably provide sufficient energy for the water pump in different seasons according to the sunlight condition in the delft area. At sunny days and the PV array generates more power than the pump required, the battery will store the surplus energy. When the PV array is not enough to generate the energy required by the pump, the battery will discharge the bus to stabilize the grid voltage. From the test results shown in Section 5.4, under different sunlight conditions and user requirements, the system can switch to a proper operation mode immediately. As a result, ensure the system overall lifespan and safety in operation. When the battery SOC is too low, the central management system would stop the motor and prevent the battery from over-discharge. The PV array would put a higher priority on charging the battery. If the sunlight condition is too well and the battery is going to overcharge, the central management system will stop the PV array to generate more power and put a higher priority on using the power inside the battery.

To help to implement the HIL simulation of the system, the system SIL simulation is implemented first. Through the SIL testing, the real-time system responses can be analyzed and in the meanwhile avoiding damage to the hardware during testing. Also, the system control algorithm can be tested before the hardware part is ready and accelerating the system development process. The testing results in Section 5.2 and Section 5.3 show that the system responses of the SIL and HIL simulation are very close to each other.

The synchronisation between different parts of the system is a vital point of achieving the system real-time simulation. Section 3.2 to Section 3.4 have described how to achieve the real-time simulation. With the help of the eHS solver and eFPGASIM library, the model of power converters and electrical machines are programmed in FPGA. To fulfil the high-frequency sampling and also to coordinate with other control components of the system, the simulation time-step of the FPGA model is set to 500ns. On the other hand, the plant model and controller are simulated by the CPU with the time-step Ts=20us. According to the control results, the CPU model and FPGA model can coordinate with each other, not only achieving the real-time simulation but also fulfilling the frequency requirements of all the elements. Furthermore, in Section 4.2, this project successfully makes the real-time simulated models interact with external hardware and eventually make it possible to independently test any hardware performance of the system.

System integrity and effectiveness have been validated. The HIL simulation of the solar array fed water pumping system can be seen as the foundation of developing a real PV system, implementing

testing of a control algorithm for any part of the system or implementing testing for these plant models.

6.2 RECOMMENDATION

This project can be seen as the preliminary work of building a physical PV-pump system. There are two directions of work that can be carried out in the future.

One direction is to optimize the system. Currently, the motor control is open loop. From the simulation results, when the motor starts and changes speed, it will greatly impact the system. Therefore, in the future, a more advanced machine control method can be implemented to have a smoother operation of the motor. As discussed in Section 5.4.1, the system overall efficiency is around 0.7-0.8, and most of the losses are on the boost converter. In the next step, the power converter's parameters can be improved to increase the system efficiency. Due to hardware limitations, as mentioned in Chapter 4, a smaller induction machine and a DC voltage source were used in the HIL simulation instead of the bigger motor and actual battery that was implemented in the SIL simulation. When the real battery and induction machine selected in Chapter 2 are used in the system, a more detailed comparison of the SIL simulation and HIL simulation can be made.

The other direction is to use this platform to test the hardware. The proposed system in the project can provide a virtual testing environment, such as for testing real batteries and PV panels without implementing a real pumping system in the lab. As a real-time testing platform, the communication between the real-time simulated model and the external hardware can be done through the I/Os of the real-time simulator OP4510. Using power amplifiers to provide the necessary DC and AC power levels, this system can achieve power HIL testing, including battery management system testing, gride connected testing, etc.

A THREE-PHASE INVERTER BOARD

In this project, the controller consists of a three-phase inverter and three gate drivers. One gate driver is responsible for one phase leg of the mentioned inverter. The used topology of the three-phase inverter is shown in Figure A.1. In order to avoid the unwanted triggering of MOSFETs, complementary PWM signals are given to two switches on each phase leg of the inverter.

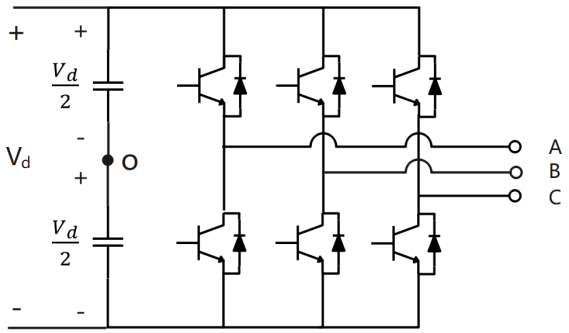


Figure A.1: The used topology

The PWM signal will be mapped to the simulator's module and then transferred to the external control board. This external controller is able to convert the DC voltage to the three-phase AC supply and is also able to implement overcurrent detection. When failures occur fault signal will be generated and resulting in a shut-down of the entire board.

A.1 GATE DRIVER

The three gate drivers are the same. For each driver, there are two PWM inputs, one fault signal transfer jack, and two gate signal output jacks (for the top and bottom switches of one phase leg). There are mainly 4 modules in the gate driver, PWM receiver module, Switch Control Signal and Fault Detection Module, DC_Fault Module, and Signal Transfer Model.

A.1.1 PWM receiver module

Figure A.2 shows the PWM signal receiver. U5 receives the PWM signal for the top switch, and U4 receives the PWM signal for the bottom switch. Enable signal, as shown in Figure A.3, is from the three-phase inverter and transferred by the Pin jack which will be explained later. After comparing

Enable and PWM signals, the control signals, A1 and A2, will be transmitted to the respective gate-drive optocoupler.

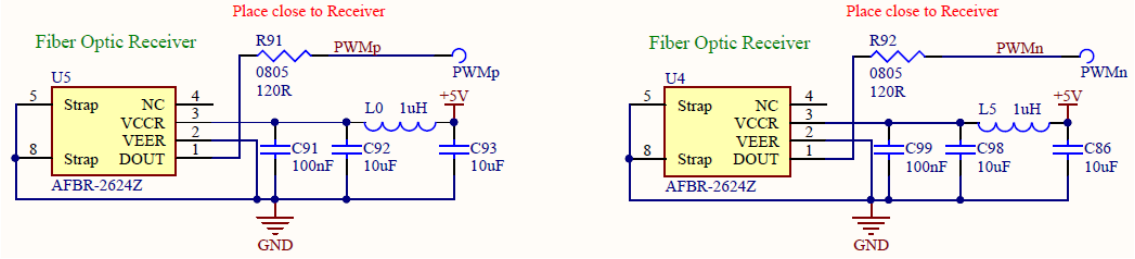


Figure A.2: PWM signal receivers

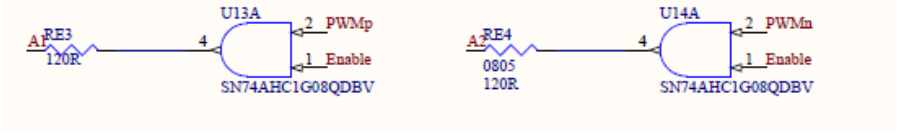


Figure A.3: Generating control signals to the top and bottom switches

A.1.2 Switch Control Signal and Fault Detection Module

Figure A.4 shows the module responsible for generating the switch control signal and monitoring the MOSFET's condition. There are two such modules in one gate driver, one for the top and the bottom. Port A inputs PWM signal (A1/A2 in Figure A.3), and port B is connected to the ground. Vout is the gate signal of the gate driver. When the device is on, it will be approximately 15V. When the device is off, it will be approximately -4V. Port G. DESAT outputs the generated gate signal is linked to either port C (linked to phase voltage of inverter) or the reference voltage. When DESAT exceeds 7V, FAULT output (TRIP) goes low and gives a fault signal to the inverter through port FB.

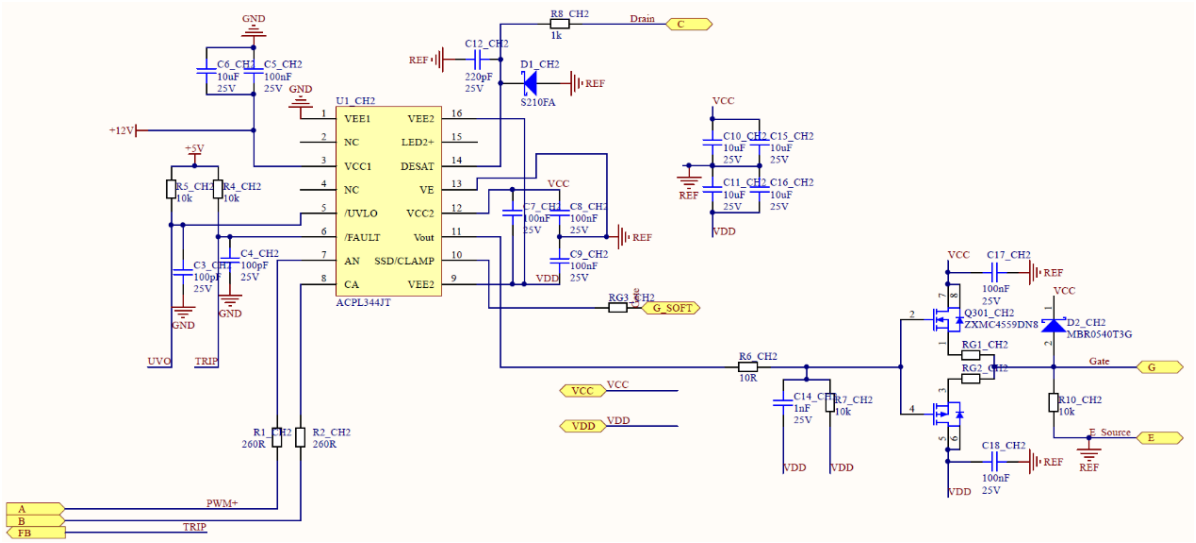


Figure A.4: Switch control signal and fault detection module for top/bottom switch

A.1.3 DC_Fault Module

The fault signals that from the two switches are processed by the module shown in Figure A.5. U12A is a 2-input positive-AND gate. FB1 and FB2 are the fault signals for the top and bottom switches of one phase leg. As mentioned in the Switch Control Signal and Fault Detection Module, when the switch gives the fault signal FB goes low. As a result, through the AND gate, DC_Fault will go low, and LED DSAT will be turned off. On the contrary, when both switches work properly, *DC_Fault* will stay high, and LED DSAT will stay on.

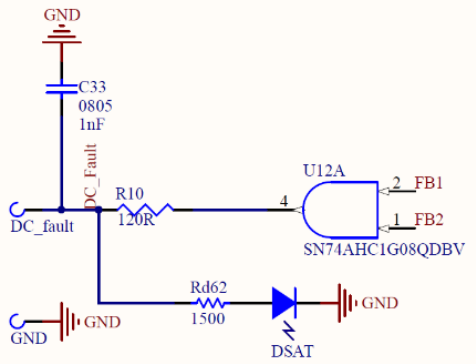


Figure A.5: *DC_Fault* Module

A.1.4 Signal Transfer Model

The signal transfer between gate driver and inverter is done by three headers, Pin, P1p, and P1n.

As shown in Figure A.6, Pin transfers the enable signal from the inverter to the gate driver, when Enable is high PWM signal will be given to the gate-drive optocoupler (shown in Figure A.4). *DC_Fault* signal is transferred from gate driver to inverter. (PWMp and PWMn shown in Figure A.6 are not used in this project.)

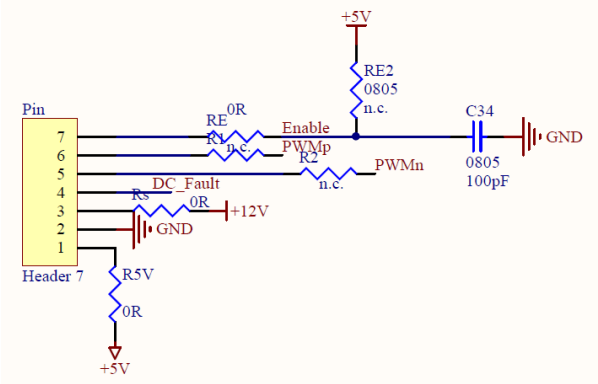


Figure A.6: Schematic of Pin

P1p and P1n, as shown in Figure A.7, are the headers that transfer top and bottom switch signals (from the switch control signal and fault detection module) between the gate driver and inverter.

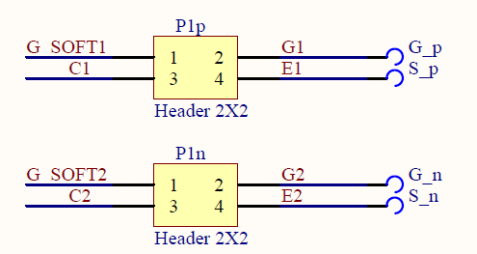


Figure A.7: Schematic of P1p and P1n

A.2 THREE-PHASE INVERTER

There are mainly 5 modules in this three-phase inverter, the inverter module, the overcurrent detection module, the fault detection module, the signal transfer module, and the enable signal module. Only the modules that are used in this project are mentioned in this section.

A.2.1 Inverter Module

Figure A.8 shows the used inverter topology. DC power is inputted from ports Up and Un on the left side. Three-phase AC power is outputted from port PhOutA/B/C. As mentioned in Figure A.7, the headers from Figure A.9 transfer switch control signals from the gate driver to the relative phase leg.

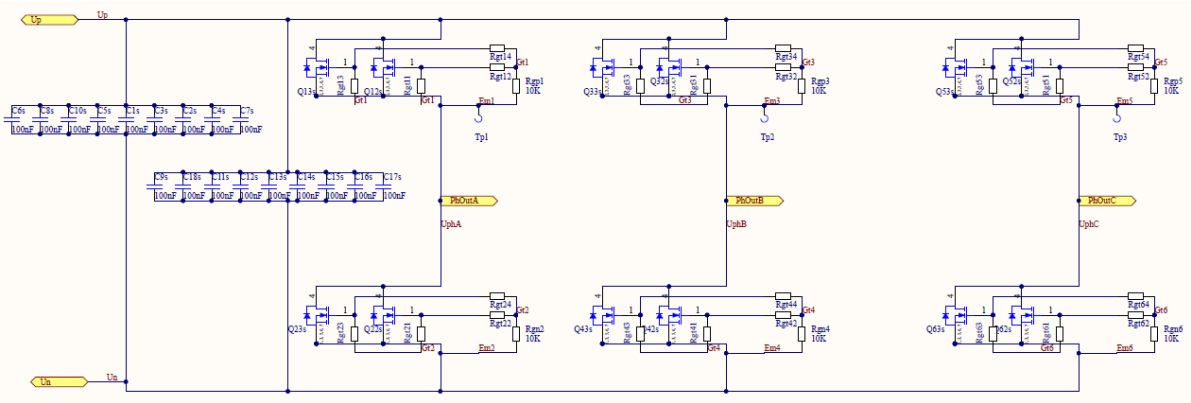


Figure A.8: Schematic of three-phase inverter

A.2.2 Overcurrent Detection Module

Each phase of this inverter has one overcurrent detection module. Figure A.10 shows the schematic of the overcurrent detection module. Phase current at the AC side of the three-phase inverter is imported through port P and N. Cq-330G (U1_I1) is a coreless current sensor that outputs analog voltage that is proportional to the input AC/DC current, the output pin can only vary from 0V to 5V (the equivalent current is -20A to 20A). Two comparators are within U4-I1. When IsenseA is over 4.15V or below 0.85V, through the AND-gate U5_I1A, fault signal 0 will be sent to port OC_sig.

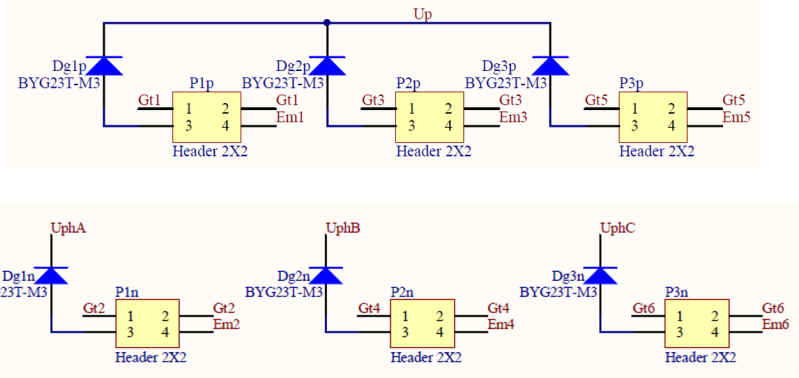


Figure A.9: Switch-control-signal transfer headers

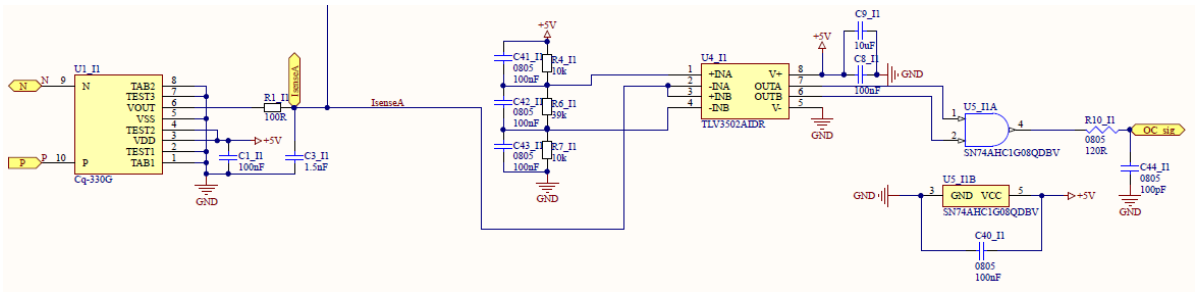


Figure A.10: Schematic of overcurrent detection module

A.2.3 Fault Detection Module

The schematics showed in Figure A.11 process all fault signals. U5A and U6A are AND gates. FBA/B/C is the switch DC_Fault signal from each gate driver as shown in Figure A.5. When any switch gives a fault signal, TRIP goes low. OC1/2/3 is the fault signal from each phase's overcurrent detection module. When any phase current is not within the safety range, OverI goes low. U7A is a NAND gate. As a result, when any fault occurs on the control board Fault will go high.

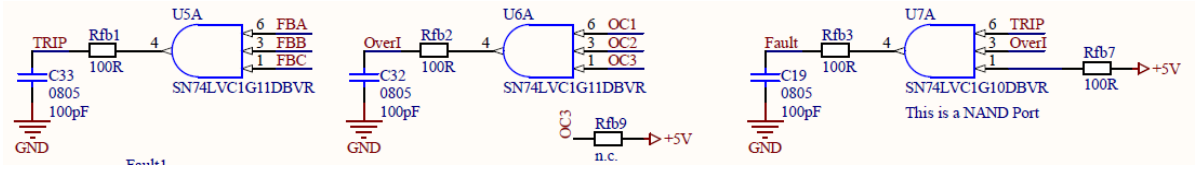


Figure A.11: Fault signals on the control board

A.2.4 Signal Transfer Model

As shown in Figure A.12, it's the Enable signal receiver. Figure A.13 shows the three headers connected to phase A/B/C's gate driver (connect to the header shown in Figure A.6).

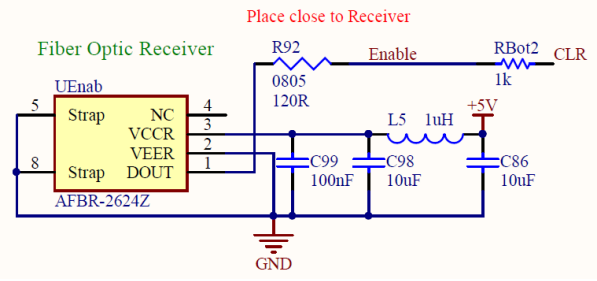


Figure A.12: Enable signal receiver

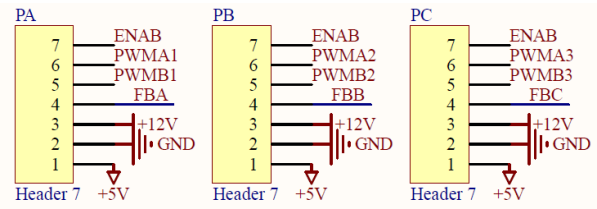


Figure A.13: Connectors to/from gate drivers

A.2.5 Enable Signal Module

Fault logic is shown in Figure A.14. ULatch is a single positive-edge-triggered D-type flip-flop. The function table of it is shown in Figure A.15. When Enable is given through the Enable signal receiver, CLR will stay high. And as mentioned, the Fault will go high as any fault occurs on the control board, LED Fault1 will light up. Therefore, due to the positive edge from CLK, see from the function table in Figure A.15, TRZN will go low.

From the schematic in Figure A.16, when TRZN goes low, through the AND gate U13A, the enable signal ENAB that is sent to every gate driver will be turned off. Then the entire system will be shut down. (TRZ is not used.)

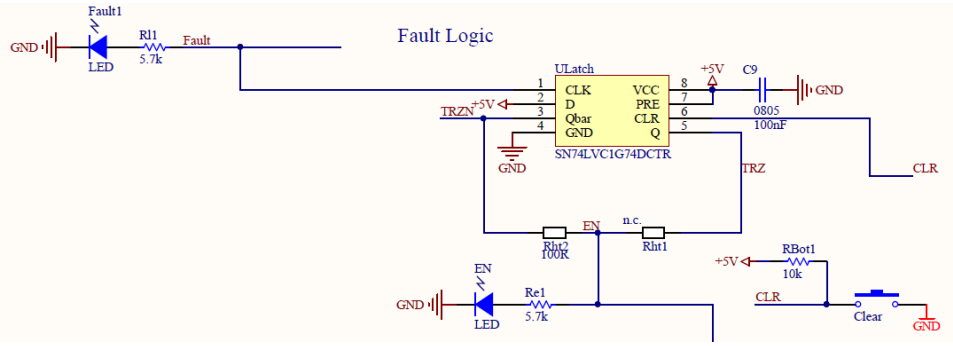


Figure A.14: Fault logic

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H(1)	H(1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

(1) This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

Figure A.15: Function table of ULatch

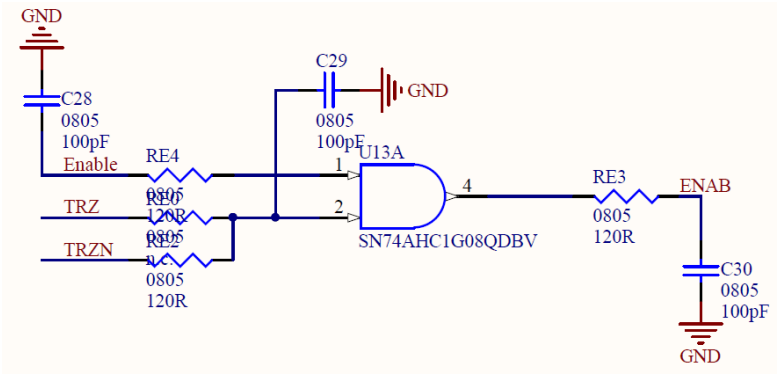


Figure A.16: Enable signal to gate driver

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