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Three-Phase AC/DC Quasi-Single-Stage Isolated Resonant PFC Converter With Integrated Transformer

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ABSTRACT Converters that produce an isolated dc output from a three-phase mains supply are often required. Moreover, input power factor correction (PFC) functionality is essential. A standard two-stage conception with ac/dc and dc/dc converters may be used. However, a single-stage or quasi-single-stage solution can simplify the circuitry and increase efficiency; therefore, many variants of single-stage converters have been researched and published. This paper introduces a novel quasi-single-stage resonant topology with an integrated transformer. Additionally, an original control structure is proposed. This converter enables full control over the output dc voltage and current. Another benefit of the proposed converter is a relatively low complexity of its power circuit and control compared to other single-stage converters. The operation principle of the power circuit is explained and the control strategy is also analyzed in detail. A description of the integrated transformer together with aspects of the resonant circuit design are presented. A simulation of the entire converter was performed and evaluated. Furthermore, a test-bench prototype was designed and constructed and is outlined in this paper. The test-bench measurement results are provided and compared to the simulation results. Power factor and efficiency measurements in terms of their dependence on the output voltage and current are included.

INDEX TERMS Isolated power factor correction (PFC) source, magnetic-combination transformer, phase-shift control, resonant converter, quasi-single-stage converter, three-phase ac/dc converter, wide output voltage range.

I. INTRODUCTION

In recent years, the demand for high-power dc supplies has increased. Traditional applications include server rooms, data centers, telecom equipment [1] and electroplating supplies. In addition, on-board and off-board battery chargers of various power and voltage ratings will be required in large quantities for electric vehicles in the near future. Three-phase mains electricity must be used to supply power to dc sources that require more than a few kilowatts. Moreover, power factor correction (PFC) is necessary, otherwise, the distorted line current could have a detrimental effect on the mains supply, leading to higher conduction losses due to increased rms currents, electromagnetic compatibility (EMC) issues, and line voltage waveform distortion—more so with the widespread application of high-power loads. Furthermore, the efficiency of such supplies and converters becomes exceedingly important, especially in the context of the ongoing energy and climate crises.

In contrast to the classic two-stage approach (PFC rectifier and dc/dc converter), e.g., [2], [3], or [4], researchers often focus on a single-stage or quasi-single-stage approach for ac/dc converters [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [23], [24]. A true single-stage topology does not contain an input passive diode rectifier but only one AC/DC converter with semiconductors providing mains rectification and at the same time producing

the HF voltage for the pulse transformer. The quasi-single-stage topology includes an input passive diode rectifier but it does not use a filtered DC link. The semiconductors of the converter behind the input diode rectifier provide the HF voltage for the pulse transformer and at the same time ensure the PFC functionality (input phase current shaping). The advantage of the quasi-single-stage topology over the traditional two-stage consists in the fact that only one active stage with controlled semiconductors is used. Such a configuration permits a decrease in complexity and/or an increase in efficiency. Both single-stage and quasi-single-stage converters tend to require a more complex control structures because of the mutual influences of both functions, which are based on common control signals. Often, compromises must be made, and more sophisticated circuits must be used.

For a single-phase supply, the instantaneous input power must drop to zero during voltage zero crossing transitions, which means it is not possible to realize a constant output power converter without additional energy storage, usually in the form of electrolytic capacitors [5], [6], [7], [9]. In a symmetrical three-phase system with unity power factor, i.e., sinusoidal line current waveforms, the sum of the instantaneous powers of all three phases is constant, see (1)–(5) below. Owing to these facts, it is possible to realize a three-phase ac/dc converter without electrolytic capacitors for additional energy storage, resulting in a longer service life.

Various single-stage ac/dc converter topologies with PFC were researched and presented. A number of these topologies are exclusive to the three-phase solution; however, all the single-phase topologies, e.g., [5], [6], [7], [8], [9], can also be modified for a three-phase usage.

An overview of some single-phase quasi-single-stage PFC topologies with hard switching is given in [8]. A solution that uses a two-switch flyback converter, where one switch also serves as part of a PFC boost converter, is presented in [6], and a special solution that uses a non-standard single-switch flyback PFC converter (without any boost converter) is given in [9]. Only one switch is used in the latter, which is a distinct advantage. The flyback converter generally carries some disadvantages for high power, e.g., a high rms current in the output capacitor or additional transformer-winding eddy current losses arising from the air-gap fringing flux. In [7], the two-switch flyback converter is replaced with a half-bridge resonant LLC dc/dc converter. There is an issue with the control complexity due to the mutual effects of both converter functions that are included. Moreover, the discontinuous current in the input inductor proposed in [7] results in an elevated input voltage ripple and increased inductor losses. Numerous other publications adopt this principle to combine boost and LLC converters. An example may be [5], where a transductor as a non-typical control element is proposed. At a specific voltage–time integral, the corresponding ac component of the core flux density in the transductor must be low to avoid strong non-linearity. This necessitates a large transductor, which is disadvantageous.

A suitable solution for a three-phase single-stage ac/dc PFC converter is discussed in [10] and [11]. It is based on a dual active bridge (DAB) circuit in which the input six-pulse diode rectifier and transistor full bridge are replaced with a six-switch matrix converter. There is one common high-frequency (HF) transformer and a secondary transistor bridge. Because no diode rectifiers are used, this topology even enables a bidirectional power flow. In practice, there is a potential risk of failure in the event that an error occurs in the switching pattern of the matrix converter.

A design similar to [6] and [7] mentioned above, i.e., a combination of a boost PFC and dc/dc converter in a single switch or leg and modified for a specific three-phase solution, is presented in [12]. Instead of a flyback or LLC resonant converter, a full-bridge forward converter is implemented, but no output choke is present. A single common HF transformer is used. Again, the minor disadvantages of the discontinuous input inductor currents mentioned above arise here. Further, the absence of an output inductor results in a necessary discontinuous output dc current, where the slope of the triangular current is limited by the transformer leakage. This unfortunately causes high rms currents in the transformer and transistor, along with other problems. The particular topologies analyzed in [13] and [21] are not dissimilar to [12], although a "Taipei" input rectifier is used there. This rectifier is a boost PFC type containing a six-pulse diode bridge with inductors in the ac inputs and one transistor leg. In [13] and [21], this transistor leg is also a component of the following dc/dc converter. In the "Taipei" rectifier, an HF rectangular voltage (high dv/dt slope) between the dc link and ground is present. This could potentially result in common-mode EMC problems.

All the aforementioned topologies contain one common HF transformer. There is an approach using two transformers, [24], [25], [26]. This configuration is based on an unfolding three-phase rectifier. The relatively high number of switches could present a disadvantage, although the switches in the unfolder do not operate at a high frequency.

The following topologies use three separate HF transformers. In [14] and [18], a nine-switch transistor bridge with three input inductors operates as a boost PFC converter, and the primary windings of the transformers in the resonant LLC dc/dc converter are driven by other nodes of the same bridge. A reasonably sophisticated control structure is required. Another possibility is in [16], where a special three-phase supplied three-switch flyback converter is used, and the primary as well as the secondary windings of three separate transformers are delta-connected. A typical output rectifier with an output capacitor and without a choke inductor follows. As this topology excludes the use of two-switch flyback converters (only one switch is used in one flyback), there is an issue with energy stored in the transformer leakage inductance, commonly resulting in turn-off voltage spikes. The authors of [16] countered this problem using an additional clamping circuit with a dc/dc converter, which transferred the energy to the dc output. However, this creates increased complexity.

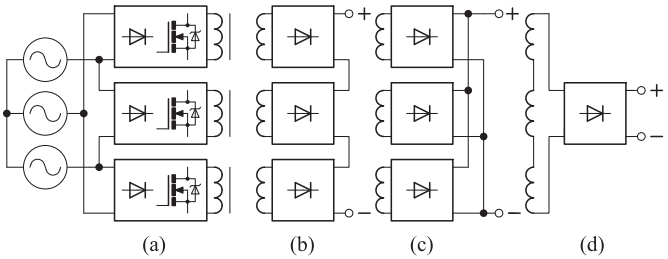

FIGURE 1. Modular converter configurations: (a) primary circuits; (b), (c), and (d) variants of the secondary connection type.

So-called "modular" converters are a specific category of the three-transformer topologies. They are based on three discrete but identical modules belonging to corresponding phases. Either the secondary windings of three transformers are connected in series with one common rectifier, or there are three separate output rectifiers whose outputs are connected in series or parallel (see Fig. 1).

One possible modular solution based on a single-ended primary-inductance converter (SEPIC) topology is described in [19]. All three dc outputs are connected in parallel. A second, very similar solution is presented in [23], the only difference being the usage of a Ćuk converter instead of a SEPIC. Both of these solutions present issues with transformer leakage inductance energy recovery, as mentioned above. These problems are solved in [19] and [23] using a resistor-capacitor-diode (RCD) passive snubber circuit. Moreover, the SEPIC variant [19] has a problem with transformer fringing flux, leading to increased winding losses (the transformer in a SEPIC operates in flyback mode—an inductor with two windings).

There is a solution proposed in [17], which uses an input diode bridge and a classical hard-switching full-bridge converter with an HF transformer in each phase module. There are three secondary rectifiers with *LC* filters, and their dc outputs are connected in parallel. Unfortunately, the combination of forward converters and the paralleling of their outputs prevents a sinusoidal input from being achieved in the ac line currents in the overall PFC converter. In a forward converter, a condition must be fulfilled whereby the input dc voltage is higher than the output voltage divided by the transformer ratio N_2/N_1 and by the maximum duty cycle. For a lower instantaneous input voltage, the converter must operate with a discontinuous output inductor current, which causes a dramatic decrease in the output current.

A useful modification of the last-mentioned topology [17] can be found in [15] and [20]. The difference consists in a series connection between all three secondary windings followed by one common secondary rectifier with an *LC* filter. The critical problem highlighted in [17] is entirely eliminated this way.

The topology from [15] and [20] is depicted in Fig. 2. A standard hard-switching forward converter with an output *LC* filter is utilized. This circuit formed the basis for our further topology development. However, in our case a resonant

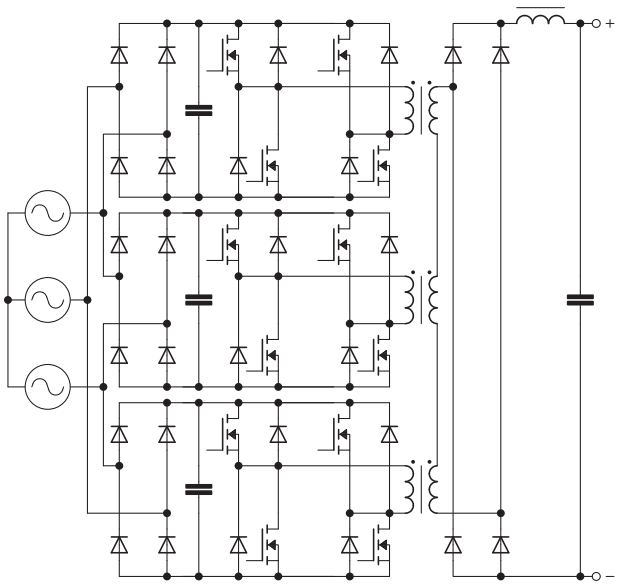

FIGURE 2. Basic topology proposed in [15] and [20] chosen for further presented research.

mode is used, wherein resonance between the transformer leakage inductance and a resonant capacitor is utilized; in this scenario, the output inductance in Fig. 2 would disturb the resonance and must not be present. With a proper control, the resonant mode allows for zero-voltage turn-on of the transistors, thus suppressing noise and electromagnetic interference (EMI) and increasing the efficiency across a wide range of load currents. These are the main advantages of the proposed solution in comparison to [15] and [20]. Another substantial difference in the proposed topology is the application of an integrated transformer (that replaces three individual transformers with series-connected secondary windings) and the addition of magnetic shunts to set an appropriate level of leakage inductance.

The modular conception of the quasi-single-stage three-phase PFC converter with a resonant topology is familiar to researchers, e.g., [27] and [28]. Moreover, some types of integrated transformers were researched. However, the proposed novel topology combines these features in a specific way and includes an original control structure. The viability of the proposed solution is documented and validated, with practical measurements included in this paper.

In this paper, the proposed converter topology is described and explained in Section II, the control strategy is introduced and mathematically analyzed in Section III, the results of the simulations are presented in Section IV, ideas and construction details relating to the integrated transformer are included in Section V, and a physical prototype for a 20 kW converter is presented in Section VI, where the practical measurement results are reported and compared to those of the simulations, documenting the practical feasibility of the converter. Finally, the conclusions are set out in Section VII.

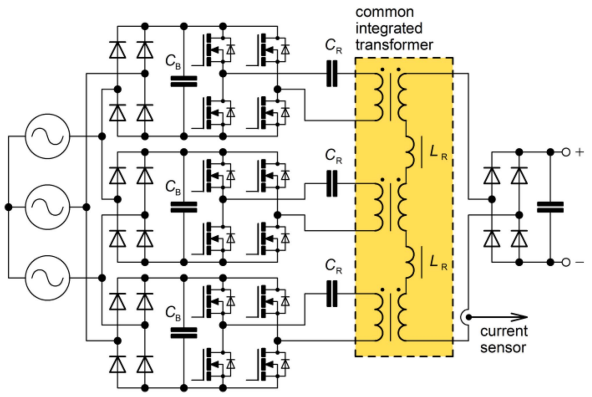

FIGURE 3. Proposed modular three-phase isolated PFC converter.

II. PROPOSED CONVERTER TOPOLOGY

The power circuit of the proposed modular PFC converter is depicted in Fig. 3. Each phase module is supplied with a corresponding phase-to-phase ac voltage. A low-capacitance bypass film capacitor C_B on the dc side of the input diode bridge generates a soft dc link with a two-pulse rectified mains voltage waveform. A full transistor bridge is supplied by this dc link. These transistors form the primary side of a resonant converter. Although its topology is related to the widely used LLC converter, a different mode of operation and an alternate control structure are used. The resonant tank is made up of the resonant capacitor C_R and the primary leakage inductance; for a detailed description, see Section V. A single special integrated HF transformer with a defined, intentionally increased leakage is adopted in lieu of three individual transformers with a series connection of their secondary windings. One common secondary HF bridge rectifier with an output capacitor (but no output inductor) is used.

The output current sensor is positioned in front of the output rectifier (see Fig. 3), so an HF ac current is sensed. A dc output current could be detected directly (e.g., with a shunt or Hall effect sensor). However, if the current sensor is placed on the ac side, a simple HF current transformer with inherent galvanic isolation may be used. In the proposed converter, all the ac current is rectified to the output; thus, an image of the output dc current can be obtained by first sensing the ac current, rectifying it, and then filtering it (average absolute value).

Sinusoidal input phase currents and a controllable constant output voltage from the converter are desired. Furthermore, at a given load, the instantaneous output power must also be constant. This is attainable even without additional energy storage capacitors, owing to the fact that the sum of all three instantaneous phase powers in a symmetrical mains supply is constant (provided the currents are sinusoidal); thus, theoretically, considering unity efficiency, this sum of all three instantaneous phase powers should equal the constant instantaneous output power. This is one of the basic ideas utilized in the proposed converter. It can be proven as follows. Let us consider a sinusoidal input module voltage with amplitude V and a sinusoidal input module current with amplitude I in phase with the module input voltage ($\cos\varphi = 1$). Thus, the instantaneous power of one module is

$$p_1(t) = v_1(t) \cdot i_1(t) = VI\sin^2(\omega t), \tag{1}$$

where $v_1(t)$ and $i_1(t)$ are the instantaneous input module voltage and current, respectively, and ω is the mains supply angular frequency. In the second and third module, the situation is analogous:

$$p_2(t) = v_2(t) \cdot i_2(t) = VI\sin^2\left(\omega t + 120^\circ\right), \tag{2}$$

$$p_3(t) = v_3(t) \cdot i_3(t) = VI\sin^2\left(\omega t + 240^\circ\right). \tag{3}$$

Using (1), (2), and (3), the sum of the three instantaneous module powers can be expressed as

$$p(t) = VI\left[\sin^2(\omega t) + \sin^2\left(\omega t + 120^\circ\right) + \sin^2\left(\omega t + 240^\circ\right)\right]. \tag{4}$$

The solution of the expression in square brackets in (4) results in a constant value equal to 1.5. Therefore, the sum of the instantaneous module powers is constant:

$$p(t) = 1.5VI = 3V_{rms}I_{rms} = const. \tag{5}$$

As all three secondary windings are connected in series (see Fig. 3), all three secondary current waveforms are identical; therefore, the primary currents are also identical (neglecting magnetizing currents). The average absolute value of the HF secondary winding current equals the constant dc output current.

The sum of the peak voltage values provided by all three primary transistor bridges takes the form of a six-pulse rectified three-phase ac voltage (without filtering). This time-variable peak value, transformed via the transformer turns ratio, must remain higher than the output dc voltage. This is a necessary condition for proper converter operation, which enables an uninterrupted and time-constant actual power transfer from the three-phase ac input to the dc output. Only then is it possible to introduce the secondary HF current with the above-mentioned constant (time-invariable) average absolute value.

As demonstrated in Fig. 3, there is no output inductor, and a filtering capacitor is connected directly to the output of the secondary rectifier. Thus, theoretically, zero impedance is observed in the series connection of secondary windings when the rectifier diodes are open. Furthermore, the transistor bridges behave, in theory, as pulse voltage sources with zero internal impedances. This permits resonance to emerge between the transformer leakage inductance seen on the primary side and the resonant capacitors C_R.

The presence of the resonant circuit with a relatively high quality factor enables the production of an approximately sinusoidal waveform of the previously mentioned HF secondary and primary currents (see Fig. 7 for a more detailed description). Thus, the secondary and primary currents can be considered as an HF sine, with a constant (unmodulated) amplitude arising from the fact that their average absolute value is also constant due to the constant output dc current.

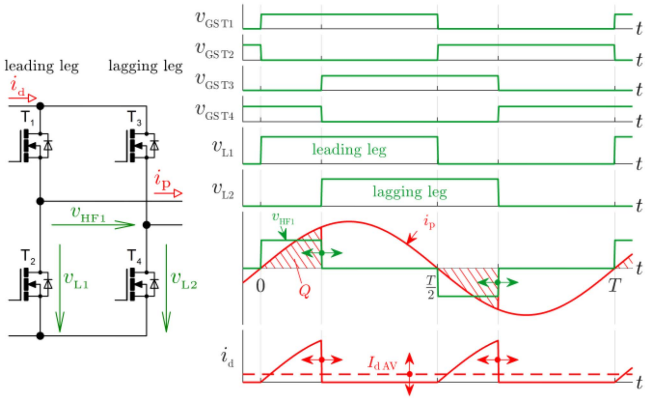

FIGURE 4. HF primary current, transistor bridge output voltage, and transistor bridge input current consumed from the soft dc link.

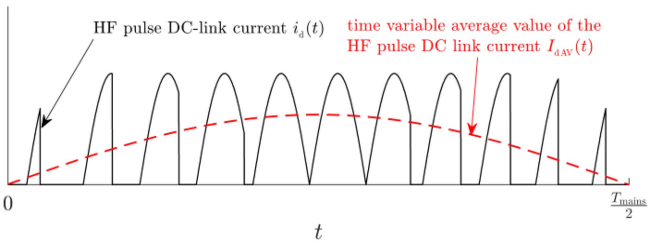

FIGURE 5. Duty cycle control to achieve the LF sinusoidal shape of the soft dc link average current (i.e., the phase current).

Fig. 4 shows the phase shift control of the transistor bridge, where $v_{L1}(t)$ and $v_{L2}(t)$ are the leg output voltages of one bridge, $v_{HF1}(t)$ is the bridge output voltage, $i_p(t)$ is the bridge output current (primary transformer current), and $i_d(t)$ is the current drawn from the soft dc link by the transistor bridge.

If the duty cycles of the primary transistor bridges were constant, the average value of the HF pulse currents consumed from the soft dc links by the transistor bridges would also be constant. Consequently, the low-frequency (LF) input ac module currents would be rectangular, which is not acceptable. This is why the duty cycle (phase shift) of each primary bridge must be controlled relative to the instantaneous soft dc link voltage value so as to achieve sinusoidal phase currents (see Figs. 4 and 5).

III. CONTROL STRATEGY

The waveform of the dc link HF current according to Fig. 4 can be expressed in the time interval t_{on} as

$$i_d(t) = I_{d\max} \sin(\Omega t), \tag{6}$$

where Ω is the angular frequency of the HF current and $I_{d\max}$ is its amplitude. The charge, denoted by Q in Fig. 4 is calculated using

$$Q = \int_0^{t_{on}} I_{d\max} \sin(\Omega t)\, dt = \frac{I_{d\max}}{\Omega} [1 - \cos(\Omega t_{on})]. \tag{7}$$

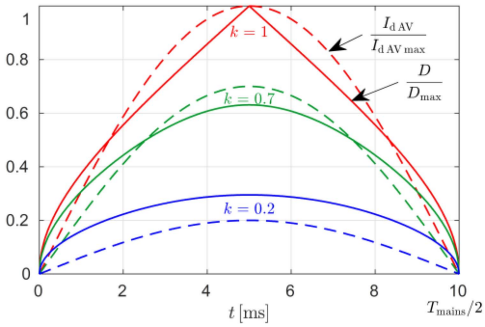

FIGURE 6. Required theoretical dependence of duty cycle on time and the corresponding sinusoidal shape of the module input current for different values of k (mains frequency of 50 Hz considered).

The average value of the HF current pulses is

$$I_{dAV} = \frac{Q}{T/2} = \frac{I_{d\max}}{\pi} [1 - \cos(\Omega t_{on})], \tag{8}$$

where T is the period of the HF sine bridge output current. Consideration is now needed for the fact that this average current must be an LF sinusoidal function of time from a macroscopic perspective to achieve the LF sinusoidal shape of the input module current:

$$I_{dAV}(t) = k \cdot I_{dAV\max} \sin(\omega t) = k \frac{2 I_{d\max}}{\pi} \sin(\omega t), \tag{9}$$

where ω is the angular frequency of the input module sinusoidal current (LF), I_{dAVmax} is the maximum average value of the HF dc link current obtained from (8) by substituting $T/2$ for t_{on}, and k is a modulation coefficient enabling control of the phase current amplitude.

By comparing (8) and (9), an equation is obtained from which the necessary dependence of t_{on} on time can be expressed as

$$t_{on}(t) = \frac{1}{\Omega} \arccos[1 - 2k \sin(\omega t)], \tag{10}$$

where t is variable between 0 and $T/2$. Knowing (10), we can express the required duty cycle time dependence as

$$D(t) = \frac{t_{on}}{T} = \frac{1}{2\pi} \arccos[1 - 2k \sin(\omega t)]. \tag{11}$$

The function in (11) normalized to 1 is plotted in Fig. 6 for three different values of k.

The resulting formula (11) was derived assuming switching of the leading leg exactly at current zero crossing (see Fig. 4). However, in practice, it is advantageous to move the switching transitions slightly before the zero crossing to allow also zero voltage switching (ZVS), see below. This causes an inaccuracy of (11). In a real control structure a dc link average current controller is employed for its shaping. This controller sets the appropriate instantaneous duty cycle automatically (to achieve harmonic input phase current). Equation (11) serves only as a theoretical principal insight.

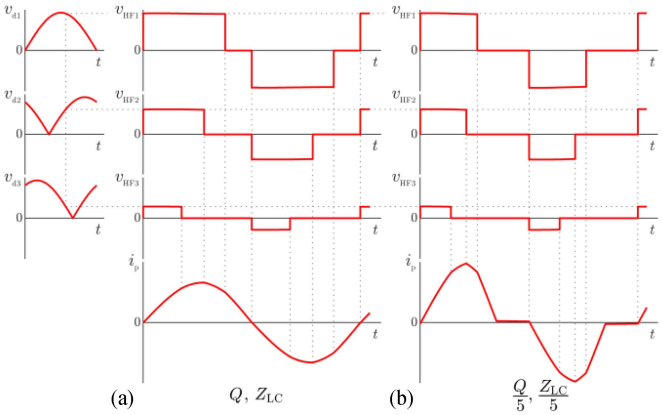

FIGURE 7. Soft dc link voltages (v_{d1}, v_{d2}, and v_{d3}), transistor bridge output voltages (v_{HF1}, v_{HF2}, and v_{HF3}), and primary current i_p (identical for all three modules).

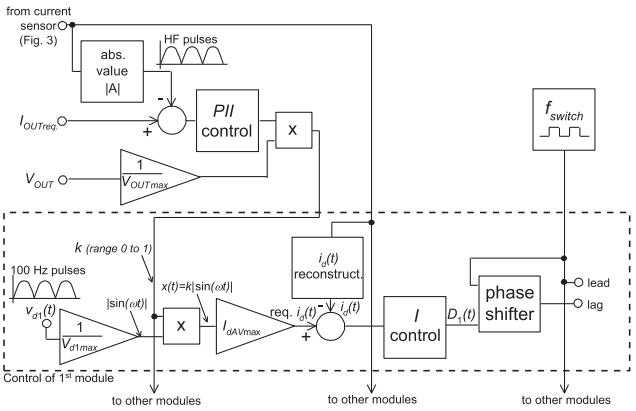

FIGURE 8. Basic converter control structure.

Important waveforms of the converter are depicted in Fig. 7. There is a time instant marked in the soft dc link voltage waveforms. The HF bridge output voltage waveforms correspond to this time instant. The marked time instant results in different duty cycle values being used in each module, according to each module instantaneous dc link voltage.

The transformer primary current i_p, neglecting the magnetizing current, is identical in all three modules due to the series connections of the secondary windings. The i_p waveform is comprised of sine wave segments corresponding to the individual switching intervals of the three modules.

All three HF bridge output voltages influence the i_p waveform shape. The switch-on time instant of the bridge output voltage (rising edge) is synchronous in all three modules, this time instant is further synchronous with the i_p zero crossing, resulting in zero current switching (ZCS) (see Fig. 7). At the rising edge of the bridge output voltage, the leading leg switches over, while the lagging leg does not change its state (see Fig. 4). It is possible to achieve ZVS while preserving near-ZCS in the leading leg if the synchronous switching transition is repositioned a short time instant before the i_p current zero crossing. In this scenario, the current remains large enough to commutate the leg voltage, i.e., recharge parasitic capacitances during the dead time. The switch-off time instant of the bridge output voltage (falling edge) relies on the duty cycle. These switch-off instants in both half-waves of the current i_p correspond to the lagging leg being switched over (see Fig. 4), while the leading leg maintains its state. There is no ZCS in the turning-off transistor of the lagging leg; the current in this transistor flows in a positive direction (from drain to source). However, ZVS is possible in the opposite transistor of the lagging leg—the current recharges the parasitic capacitances during the dead time. All the discussed assumptions require the switching frequency to be fractionally higher than the resonant frequency. If the load current is reduced, then the switching frequency should increase to preserve the abovementioned ZVS/ZCS conditions.

From the description above, it is evident that the switching losses of the lagging leg will be slightly greater than those of the leading leg because the transistor in the lagging leg turns off with current flowing through it. However, the switching loss and interference are still far lower in this case than for a hypothetical turning on with a current flowing through the opposite diode.

Let us define the quality factor Q_{factor} as the ratio of the reactive power P_Q on the L or C element of the series-resonant LC circuit to the output active power P of the corresponding transformer:

$$Q_{factor} = \frac{P_Q}{P}. \tag{12}$$

Two situations, for a higher and lower quality factor, are proposed in Fig. 7. It is apparent that the higher quality factor results in an i_p waveform close to a pure sine wave. To achieve the same amplitude of the LF module input current and the same dc output voltage and current, lower duty cycle values can be observed in the case of a lower quality factor. The reason is following: If the given dc output voltage and duty cycles remained constant, the LC series branch voltage would remain unaltered too. But the impedance of the LC circuit decreases as the quality factor decreases because L must be reduced and C increased to achieve the same resonant frequency and the lower quality factor. Then, the amplitude of the current through the LC circuit would increase. Consequently, the duty cycle must be decreased to achieve the same required average absolute value of the current $i_p(t)$.

A block diagram of the converter's control structure is provided in Fig. 8. A current control loop for the dc output current is implemented. There is a single universal current controller which is common for all three modules. The requested dc output current value I_{OUTreq} is a constant adjusted by the user. The actual dc output current value is considered to be the average absolute value of the measured transformer's secondary current waveform (see Fig. 8). A low-pass filter is not used to obtain the dc average absolute value of the secondary current, but the controller itself eliminates the ac component of the waveform. Therefore, not a PI but a PII controller is used in the proposed solution. The PII controller is based on a

standard PI controller, although it contains an additional low-pass filter for high frequencies. Such configuration is often used in switching converters, where the second low-pass filter acts to suppress unwanted signals at the switching frequency (e.g., current ripple), high-frequency noise, interference, etc. In our case, the current ripple is 100%—the sensed current waveform falls to zero every half-cycle. In this situation, sufficient filtering properties in the controller at the switching frequency are essential. This second cutoff frequency is defined by brackets in the denominator in (14).

The output of the PII controller is multiplied with the normalized output voltage to obtain the modulation coefficient k (common for all three modules) with a range from 0 to 1. The multiplication with the normalized output voltage allows a possibility to decrease the current controller preamplification (see the number 25 in (14) designed for full output voltage). The principal reason consists in the fact that the outer output current PII controller sets the required amplitude for a inner controller for the dc link current. The inner-controlled dc link current is proportional to the power but the outer-controlled output current equals to the ratio of power and output voltage. Therefore, the appropriate transfer function of the outer PII controller should be parametrically influenced with the output voltage to achieve optimum controller setting and stability behavior in a wide range of output voltage.

The framed control structure in Fig. 8 belongs to one converter module. There are two more analogous parts corresponding to the other modules. Only the part belonging to one module is shown in Fig. 8. The voltage values of soft dc links are detected and normalized to 1. If the module input voltage is sinusoidal, then, in the first module, the following signal is obtained after normalization:

$$\frac{v_{d1}(t)}{V_{d1\,\max}} = |\sin(\omega t)|\,. \tag{13}$$

In other modules, identical results are obtained, albeit phase-shifted by 120 and 240 degrees. These signals could alternatively be generated from the module input voltage using a phase-locked loop. In this scenario, a sinusoidal signal shape would be obtained, even if the mains voltage was distorted. In the proposed solution with sensing of instantaneous soft dc link voltage (100 Hz pulses), the resulting signal copies the shape of the distorted input mains voltage. As such, the resulting module input current will theoretically contain the same distortion as the input voltage. This can be beneficial, as it imitates a resistive load.

Further, the mentioned normalized signals, as in (13), are multiplied with the modulation coefficient k and further multiplied with the maximum average value $I_{dAV\max}$ of the HF dc link current. Resulting signal represents the required instantaneous value of the dc link average current with a shape of LF sine halfwaves (100 Hz).

The actual value of the dc link average current could be sensed directly from the primary power circuit. However, to avoid using additional three current sensors (for all three modules) with DC measuring capability, the actual value is reconstructed from a single secondary sensor (see Fig. 3). At first, the i_p current (see Fig. 4) and its negative value $-i_p$ are calculated based on the transformer turns ratio. A tri-state analog switch follows, the output of which is $+i_p$, $-i_p$ or zero, depending on the state of the bridge legs. This signal switch mimics the switching of the bridge legs in the power part. This way an image of actual current i_d is obtained.

Above described required and actual values of i_d current are routed to the integrating (I) controller of the dc link average current providing the duty cycle control signal for a phase shifter. Finally, the phase shifter produces the switching signals for the lagging leg transistors. In each module, the leading leg is controlled directly by a rectangular clock signal common to all three modules with a duty cycle of 0.5 (clock generator). The lagging leg is controlled with a rectangular signal, which is achieved by phase shifting (delaying) this clock signal. The mutual phase shift of the two control signals is in the range of 0 to 180 degrees.

TABLE 1. Parameters of the Simulated Converter and Realized Prototype

ac supply voltage	3x 400 V rms, 50 Hz
dc output voltage	0–100 V
dc output current	0–200 A
maximum output power	20 kW
switching frequency (variable)	41 to 58 kHz

IV. SIMULATIONS

The simulation schematic corresponds to the basic converter control structure in Fig. 8. MATLAB-SIMULINK was used to perform the simulations. Table 1 lists the basic parameters of the simulated converter along with the realized prototype.

First, the power circuit of the converter (see Fig. 3) was designed to fit the required parameters. The most important component values that resulted, which were used for further simulations, were the resonant capacitances C_R of 330 nF, total secondary side leakage inductance (i.e., $2 \times L_R$ in Fig. 3) of 3.7 μH, and the transformer turns ratio (secondary to primary) of 0.14. The other designed values were C_B of 4.7 μF and the primary magnetizing inductance of 5.5 mH for each transformer.

Parasitic resistance and inductance of the mains supply are considered in the simulation (R–L circuit in series with each supply's ideal voltage source in Fig. 3, R of 0.1 Ω, L of 100 μH). Static parameters, such as diode forward voltage and MOS-FET R_{DSon}, were also considered.

The PII controller (see Fig. 8) was tuned experimentally during the simulations. The resulting transfer function is

$$F(p) = 25 \cdot \frac{1 + 5 \cdot 10^{-5} s}{s \cdot \left(1 + 7 \cdot 10^{-6} s\right)}, \tag{14}$$

when considering unity gain of the current sensor. The upper cutoff frequency is 23 kHz, which is more than three times lower than the lowest current ripple frequency (at double the minimum switching frequency, i.e., 82 kHz).

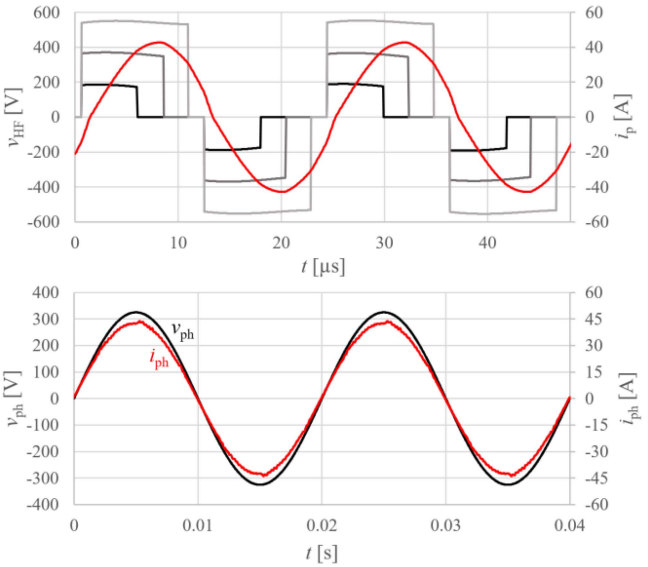

FIGURE 9. Full load (100 V, 200 A) simulated waveforms. Top graph: bridge output voltages v_{HF} and transformer primary current i_p. Bottom graph: input phase voltage v_{ph} and current i_{ph}.

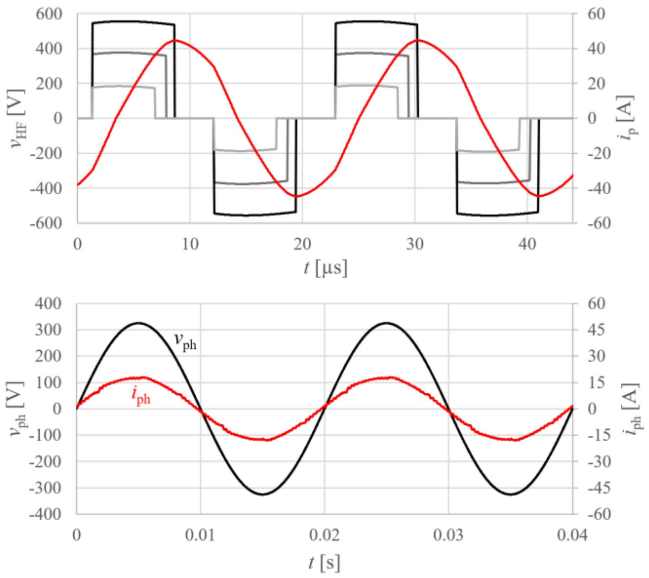

FIGURE 10. Reduced load (40 V, 200 A) simulated waveforms. Top graph: bridge output voltages v_{HF} and transformer primary current i_p. Bottom graph: input phase voltage v_{L1} and current i_{L1}.

The simulation results for a steady-state operation at the full output parameters of 100 V and 200 A are provided in Fig. 9. The expected behavior of the converter can be observed. The switching frequency is slightly over the resonant frequency to achieve leading leg switching slightly before current zero crossing (refer to Section III). The phase current waveform is almost sinusoidal; only a slight distortion can be seen. The calculated total harmonic distortion (THD) is 1.1 %.

The simulation results for a steady-state operation at reduced output voltage but full current (40 V, 200 A) are provided in Fig. 10. Lower duty cycles than those in the previous scenario can be seen. The switching frequency increased slightly to keep switching of the leading leg before current zero crossing. As explained in Section III, this is advantageous. Again, a very low distortion can be noted in the phase current waveform; the calculated THD value is 2.7 %.

The simulation results for a steady-state operation at full voltage but reduced output current (100 V, 50 A) are provided in Fig. 11. Unfortunately, the switching of the leading leg before the current zero crossing is not achieved anymore as the switching frequency reached its set upper limit, while the situation would demand its further slight increase. The upper limit of the switching frequency was set to avoid unacceptable losses of the MOSFET driver circuits. A higher but still relatively low distortion can be noted in the phase current waveform; the calculated THD value is 4.3%. This distortion is caused mostly by the bypass capacitors placed in the soft dc-links in conjunction with the input bridge rectifier commutation. The small barely observable damped oscillations appearing at these commutation instants are caused by parasitic inductance of the mains network and dc-link capacitors.

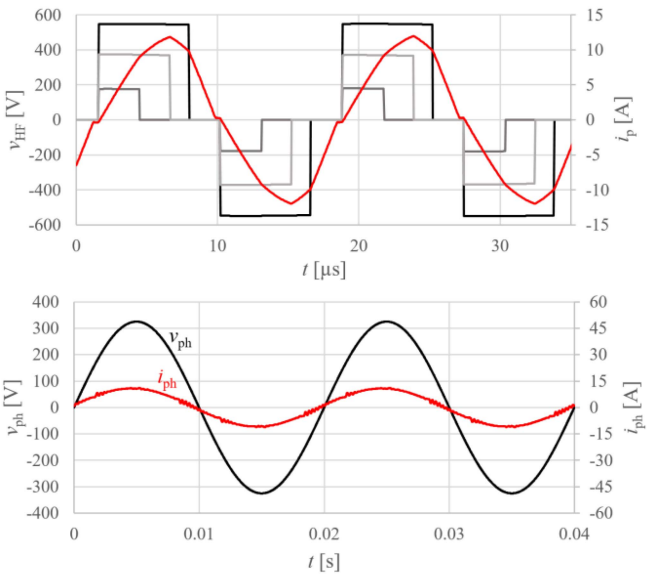

FIGURE 11. Reduced load (100 V, 50 A) simulated waveforms. Top graph: bridge output voltages v_{HF} and transformer primary current i_p. Bottom graph: input phase voltage v_{ph} and current i_{ph}.

The simulation results for a steady-state operation at reduced both output voltage and current (40 V, 50 A) are depicted in Fig. 12. The switching of the leading leg again occurs at zero current (not before). Again the upper limit of the switching frequency has been reached as in the situation in Fig. 11. A relatively low distortion (considering the low power of 10 %) can be observed in the phase current waveform, with a calculated THD value of 10.1 %.

The system's response to a step of the requested dc output current from 200 A to 100 A can be seen in Fig. 13. The

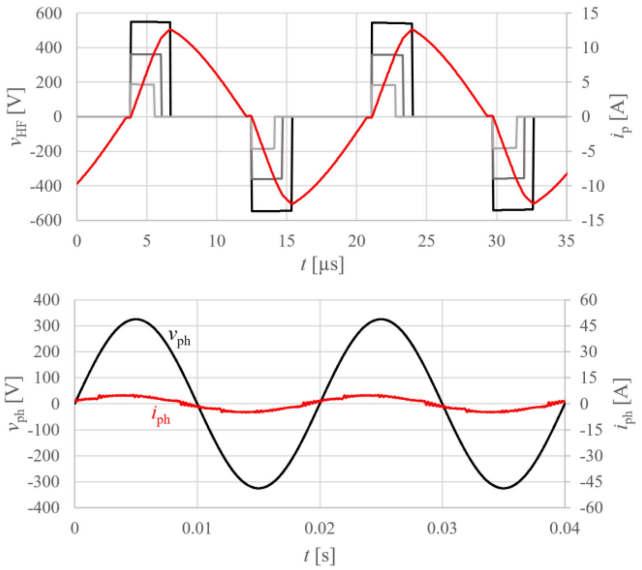

FIGURE 12. Reduced load (40 V, 50 A) simulated waveforms. Top graph: bridge output voltages v_{HF} and transformer primary current i_p. Bottom graph: input phase voltage v_{L1} and current i_{L1}.

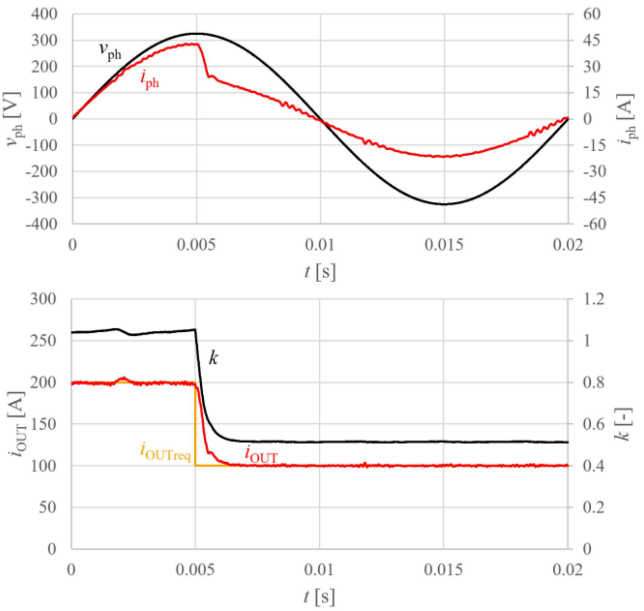

FIGURE 13. System response to a requested output dc current step. Top graph: phase voltage v_{ph} (black), phase current i_{ph} (red). Bottom graph: requested dc output current i_{OUTreq} (brown), actual dc output current i_{OUT} (red), and controller output k (black).

response is sufficiently fast and without overshoot or oscillations. Good dynamic behavior and stability in the control structure and overall system were verified.

Only a very small ripple (300 Hz) in the dc output voltage at full power operation can be seen in Fig. 14. Thus, the principal ability of the converter to provide a constant instantaneous output power (see Section II) was verified.

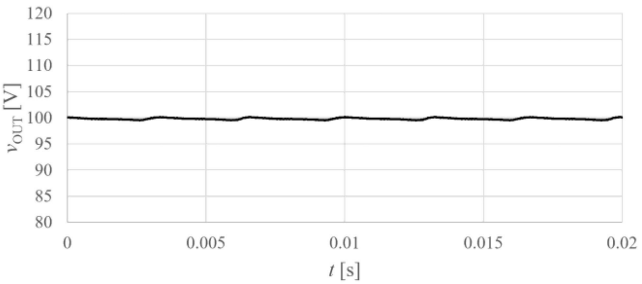

FIGURE 14. Simulated output voltage ripple at the full load of 100 V and 200 A (resistive load).

V. INTEGRATED TRANSFORMER

A single integrated transformer, common to all three modules of the converter, was designed (see Fig. 3 for its connection diagram).

Each primary winding is wound around its own ferrite toroidal core. As the secondary windings must be connected in series, it is possible to use one common secondary winding threaded through all three toroidal rings, as shown in the top part of Fig. 15. In this manner, the length of the secondary winding litz wire and its resistance are minimized. This is the initial idea for the integrated transformer. A similar idea was presented in [22], but E-cores were used there. A practical layout of the transformer can be observed clearly in the middle part of Fig. 14, showing an early version with a lower power of only 5 kW. The final 20 kW transformer can be seen in the bottom part of Fig. 15.

As the primary windings and the common secondary winding are spread around the circumference of the toroids, there is a very low stray field. Subsequently, the natural leakage inductance of the transformer is low. However, a relatively high leakage inductance is necessary for the converter to operate properly. It is useful to achieve this using additional inductors, not by altering the transformer's winding geometry and increasing the stray leakage flux. The stray leakage flux in the case of intentionally altering the winding geometry (weaker winding coupling) would result in high eddy current losses in the windings and EMI issues.

A novel means of increasing the leakage inductance without increasing the stray field is proposed: the additional inductors (see L_R inductances in Fig. 3) are integrated into the transformer using magnetic shunts. Ferrite frames with air gaps are placed between the toroidal cores with primary windings (see Fig. 15). The secondary winding is wound through them. An additional inductance in series with the secondary winding is formed with the secondary turns on these frame cores. The air gaps define the frames' reluctance to ensure the necessary leakage inductance and to avoid saturation of the ferrite frames. This way, the flux corresponding to the leakage is confined to the magnetic shunts (ferrite frames) and almost no stray field is produced.

Powdered toroids were considered for use as the magnetic shunts. Their distributed air gap is more advantageous than a

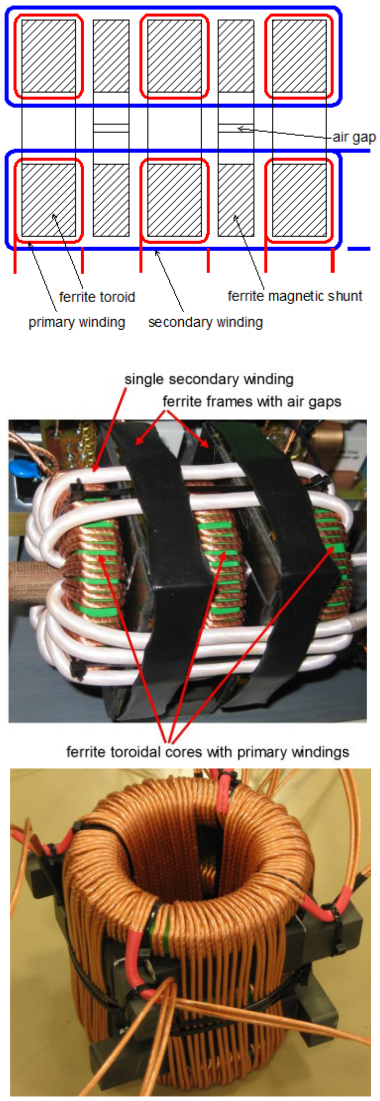

FIGURE 15. **Integrated transformer. Top: layout of the integrated transformer. Middle: manufactured transformer of a first 5 kW version. Bottom: finished transformer of the final 20 kW version.**

discrete air gap as they do not produce magnetic flux that radiates into the closely placed windings, which would result in eddy current losses. However, a problem with high core losses emerged. With the powdered toroids, the chosen maximum flux density had to be extremely low to avoid core overheating, which would result in unacceptable core size. Therefore, the ferrite frames were used—ferrite has very low power losses compared to the powdered material.

The frame is made up of four I-cores and four inserted air gaps. This way, the total air gap is also partially distributed around the core, although not as perfectly as in the powdered cores. Moreover, as is evident in Fig. 15, these air gaps are relatively far from the primary and secondary turns, so the foregoing problem of discrete air gaps is suppressed.

If the maximum flux density in the ferrite frame is $B_{\max}$ and the cross-section of one ferrite frame is S_{Fe}, then the necessary number of secondary turns is

$$N_2 = \frac{L_{R2} \cdot I_{2\max}}{B_{\max} \cdot 2S_{Fe}} \tag{15}$$

and, theoretically, the required total air gap is

$$l_v = \frac{N_2 \cdot I_{2\max} \cdot \mu_0}{B_{\max}}. \tag{16}$$

The simulation showed that the optimum transfer ratio N_2/N_1 corresponds to the amplitude of the secondary voltage of one transformer equal to circa 80% of the dc output voltage (if three individual transformers were used). This is equal to the transfer ratio from one converter module to the combined secondary winding. This amplitude of the secondary voltage appears at the maximum soft dc link voltage V_{Dmax}. Therefore, the necessary transfer ratio is

$$p = {}^{N_2}\!/_{N_1} = \frac{0.8 \cdot V_{OUT}}{V_{D\max}}. \tag{17}$$

Knowing the secondary number of turns, we can calculate the necessary number of primary turns using

$$N_1 = \frac{N_2}{p}. \tag{18}$$

For the cross-section S_{Fe1} of the toroidal core with the primary winding, the maximum flux density in the core can be verified with

$$B_m = \frac{V_d \frac{T}{2}}{2S_{Fe1}N_1} = \frac{V_d}{4 \cdot f \cdot S_{Fe1}N_1}. \tag{19}$$

This calculation of B_m would only be exact if the resonant capacitor was on the secondary side. In our application, primary-side resonant capacitors are used to guarantee zero dc bias on the primary windings, and also the resonant current is low. In this instance, the primary voltage is not a square wave as considered in the calculation above. Nonetheless, the real shape is expected to possess similar volt-seconds based on the results of the simulation.

The transformer leakage inductance is a part of the resonant tank. If a single resonant capacitor was placed on the secondary side, then its capacitance would be represented by

$$C_{\mathrm{sec}} = \frac{1}{4\pi^2 f_R^2 L_{R2}}, \tag{20}$$

where f_{R} is the resonant frequency and L_{R2} is the leakage inductance recalculated to the secondary side, which is $2L_{\mathrm{R}}$—series connection of two inductances L_{R} in Fig. 3 corresponding to the two ferrite frames. However, there are three resonant capacitors connected in series with primary windings in our design. If only a single transformer was present, then the secondary capacitance would be recalculated to the primary side with the square of the turns ratio. In our scenario, the integrated transformer can be imagined as three identical transformers with secondary windings connected in series. The secondary leakage inductance L_{R2} in series with all three secondary windings can be divided into three individual inductors with an inductance of one-third of L_{R2}, each

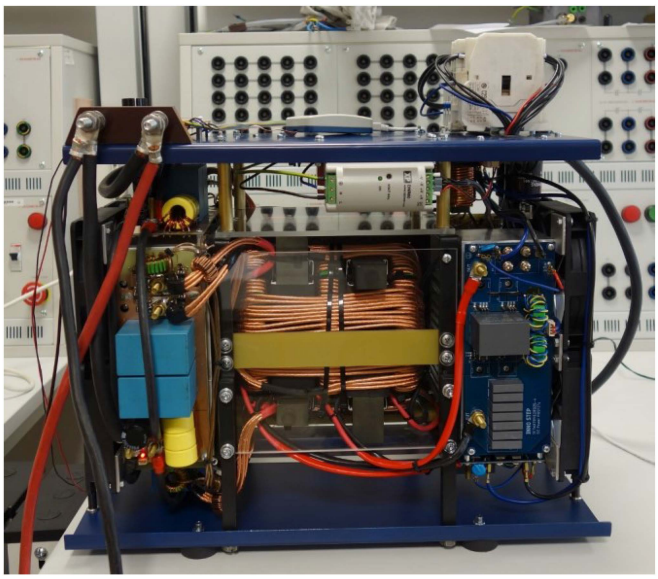

FIGURE 16. View of the constructed converter.

corresponding to one transformer. These inductances can be recalculated to the individual primary sides using the square of the turns ratio

$$L_{R1} = \frac{L_{R2}}{3}\left(\frac{N_1}{N_2}\right)^2, \tag{21}$$

where N_1 and N_2 are the primary and secondary number of turns, respectively. These inductances must be tuned to resonance with the primary capacitors C_R. As such, their capacitances must be given by

$$C_R = \frac{1}{4\pi^2 f_R^2 L_{R1}} = 3 \cdot \left(\frac{N_2}{N_1}\right)^2 C_{\text{sec}}. \tag{22}$$

Note: Theoretically, different resonant capacitances could be used in each module. However, their series connection value must be equal to one-third of the calculated C_R. Thus, even a single capacitor $C_R/3$ could be used in just one module and no capacitors in other modules. Nevertheless, practically, it would not be beneficial because different primary voltages would appear, resulting in the risk of saturation of some primary cores.

VI. PRACTICAL TESTS AND MEASUREMENTS

The constructed test-bench prototype of the converter is depicted in Fig. 16. The selected parameters correspond to those used in the simulation—see Table 1, Section IV.

The internal resistance and inductance of the supply may differ from the values considered in the simulation, but their influence is not substantial.

Silicon carbide (SiC) MOS-FETs are used in the primary transistor bridges, which are located on the right side of Fig. 16. Each bridge leg is driven with one toroidal gate drive transformer, visible in Fig. 16. The secondary synchronous

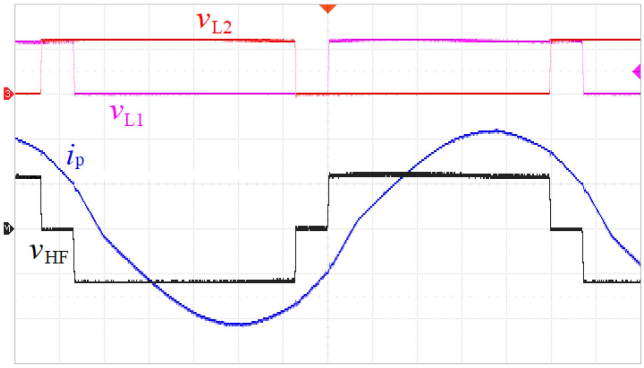

FIGURE 17. Bridge leg voltages v_{L1} and v_{L2}, bridge output voltage v_{HF} and transformer primary current i_p at full load 100 V and 200 A. Vertical 500 V/div, 20 A/div, horizontal 2 μs/div.

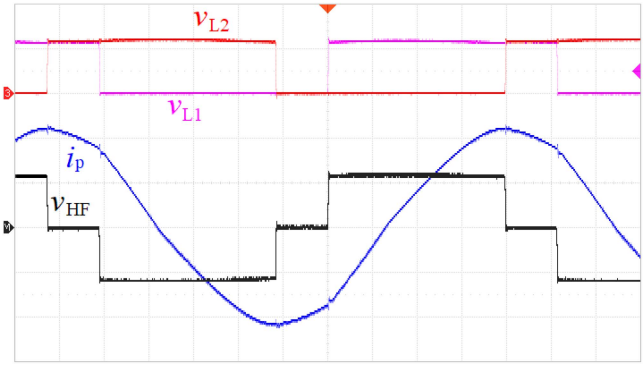

FIGURE 18. Bridge leg voltages v_{L1} and $v_{L,2}$, bridge output voltage v_{HF}, and transformer primary current i_p at reduced load 40 V and 200 A. Vertical 500 V/div, 20 A/div, horizontal 2 μs/div.

HF rectifier contains MOS-FETs IRF150P220. As the secondary transistors are stressed only by the output voltage without any voltage overshoot, low-voltage MOS-FETs with low R_{DSon} can be used. This is an advantage over other topologies that require a higher ratio of the diode (transistor) reverse voltage to the dc output voltage (such as a forward converter with an *LC* filter).

After the final adjustments to the control circuit parameters and testing of the power part, all important measurements were carried out. The oscillograms documenting the behavior of one of the transistor bridges at full power operation are shown in Fig. 17. These oscillograms were captured at the peak of the soft dc link voltage. It is clear that the phase shift is near its maximum 180 degrees (full duty), although adequate control headroom is available. The measured oscillograms align very well with the simulated waveforms in Fig. 9. Switching transitions before current zero crossing are apparent.

At a reduced output voltage and full current, a decrease of the phase shift and increase of switching frequency can be observed in Fig. 18. Switching transitions before current zero crossing are apparent. Again, there is a very good correspondence between the measured and simulated waveforms (see Fig. 10).

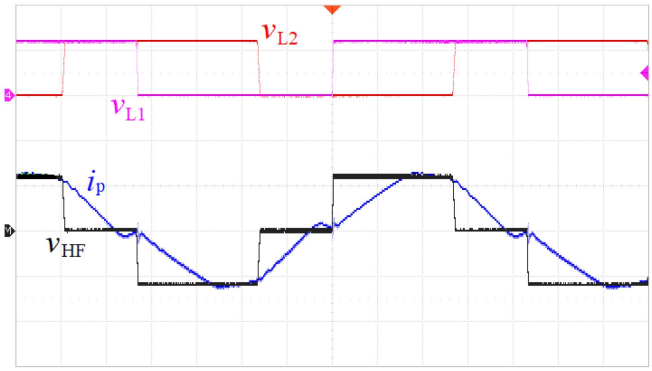

FIGURE 19. Bridge leg voltages v_{L1} and v_{L2}, bridge output voltage v_{HF}, and transformer primary current i_p at a reduced load of 100 V and 50 A. Vertical 500 V/div, 10 A/div, horizontal 2 μs/div.

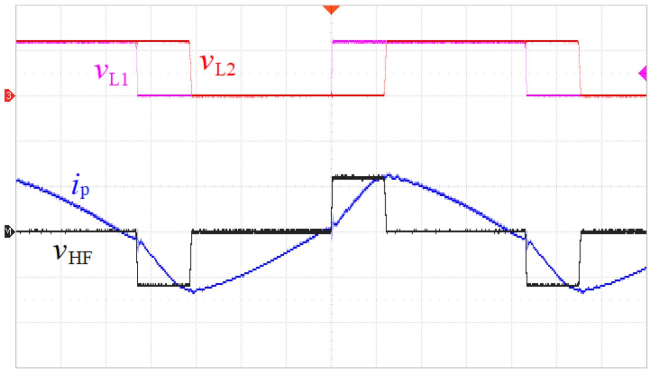

FIGURE 20. Bridge leg voltages v_{L1} and v_{L2}, bridge output voltage v_{HF}, and transformer primary current i_p at a reduced load of 40 V and 50 A. Vertical 500 V/div, 10 A/div, horizontal 2 μs/div.

At a reduced output current but full voltage, a lower phase shift (lower duty) and further frequency increase can be observed in Fig. 19. The primary transformer current drops to zero for a small part of the switching half-cycle; for a detailed description of drawbacks of this behavior, see Section III. Greater frequency increase could eliminate this problem, however, there is an upper frequency limit set in the experimental converter to avoid gate driver overheating. A good correspondence to the simulated waveforms in Fig. 11 can be seen.

At a both reduced output voltage and current, a still lower phase shift (lower duty) can be observed in Fig. 20. Switching slightly after current zero crossing is apparent; for a detailed description of drawbacks of this behavior, see Section III. Again, greater frequency increase could eliminate this problem, however, there is an upper frequency limit set in the experimental converter to avoid gate driver overheating. Again, a very good correspondence to the simulated waveforms in Fig. 12 can be seen.

The phase input voltage and current at full power operation (100 V, 200 A) are shown in Fig. 21. A typical distortion in the phase voltage, i.e., a slight flattening of peaks in the sine wave caused by many consumers using simple diode rectifiers with output capacitors, can be observed. The measured waveform of the phase current is similar to the simulated waveform

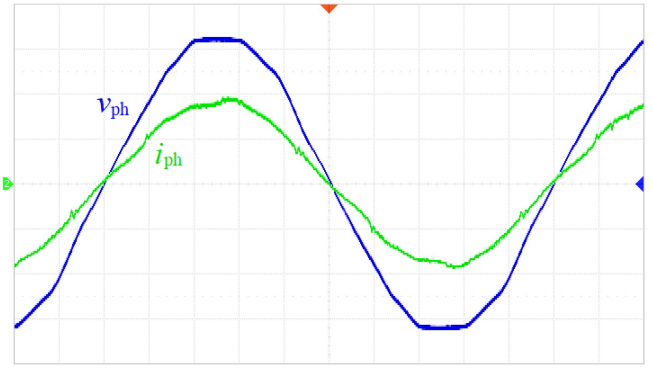

FIGURE 21. Phase voltage and current at the full load of 100 V and 200 A. Vertical 100 V/div, 20 A/div, horizontal 2 ms/div.

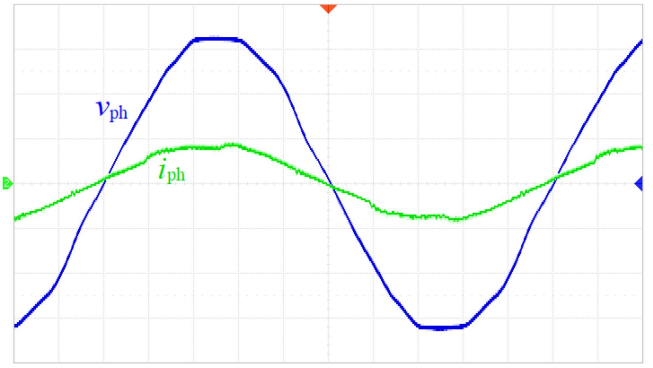

FIGURE 22. Phase voltage and current at a reduced load of 40 V and 200 A. Vertical 100 V/div, 20 A/div, horizontal 2 ms/div.

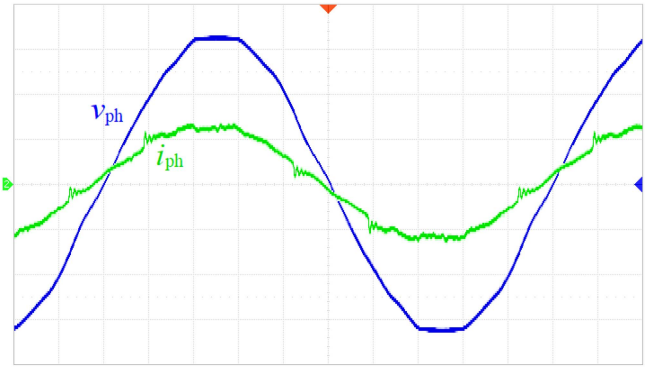

FIGURE 23. Phase voltage and current at a reduced load of 100 V and 50 A. Vertical 100 V/div, 8 A/div, horizontal 2 ms/div.

in Fig. 9; however, there are minor differences most likely caused by component tolerances.

The phase input voltage and current at a reduced output voltage operation (40 V, 200 A) can be observed in Fig. 22. A comparable result to that of the simulation in Fig. 10 can be seen. The distortion of the current waveform is still relatively low.

The phase input voltage and current at a reduced output current operation (100 V, 50 A) are shown in Fig. 23. Some small steps and ringing, comparable to the simulated waveform in Fig. 11, caused by the switching of diodes in input

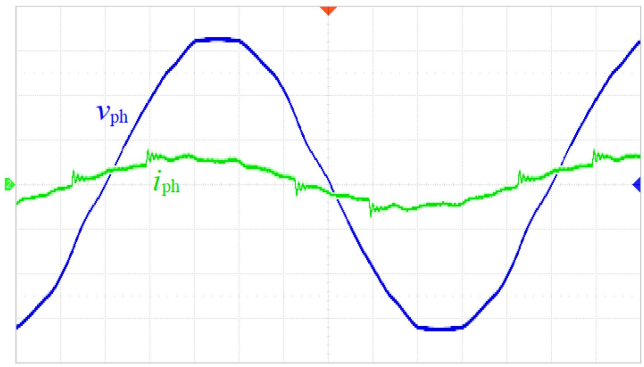

FIGURE 24. Phase voltage and current at a reduced load of 40 V and 50 A. Vertical 100 V/div, 8 A/div, horizontal 2 ms/div.

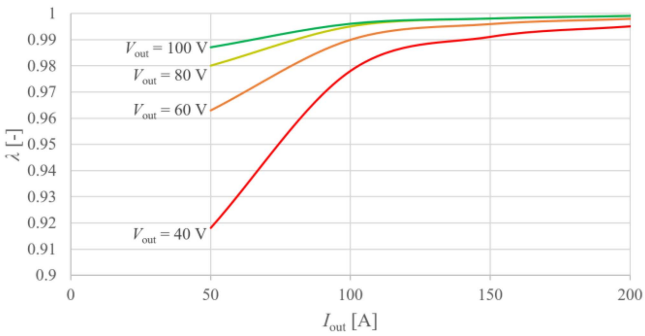

FIGURE 25. Power factor λ in dependence on output voltage and current.

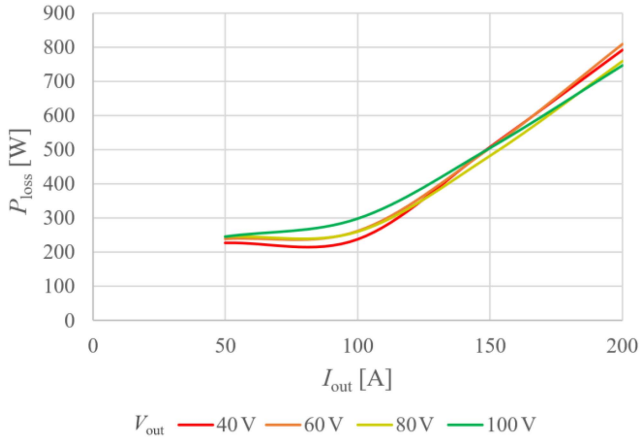

FIGURE 26. Converter power loss in dependence on output voltage and current.

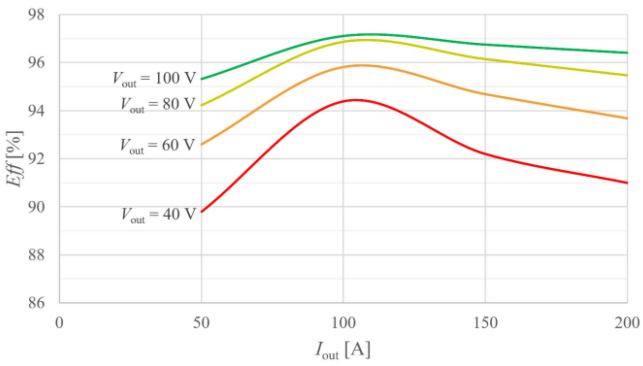

FIGURE 27. Converter efficiency dependence on output voltage and current.

bridge rectifiers with non-zero capacitances C_B connected to their outputs (see Fig. 3) can be seen in the current waveform.

The phase input voltage and current at both reduced output voltage and current operation (100 V, 50 A) are shown in Fig. 24. The situation is similar to Fig. 23 but the steps and ringing are more apparent as the current amplitude is lower. This is acceptable considering the low power of only 10 % in this case.

The power factor λ depends on the output voltage and current, as shown in Fig. 25. At full power an excellent power factor of 0.999 was reached. Lower power factor values at reduced power are mostly caused by the non-zero capacitances at the output of the diode bridges (see Fig. 3), which cause a phase shift in the current waveform as well as small steps and ringing (see above). However, at 10 % of full power the power factor is still good at 0.92.

The total losses of the converter power part in their dependence on output voltage and current are provided in Fig. 26 (the consumption of control circuits and fans is not included). It is clear that the losses depend mainly on the output current because the amplitude and rms value of the HF transformer currents and primary transistor current are independent of the phase shift, i.e., the output voltage. Theoretically, a further decrease of losses would be expected for currents below 100 A. However, the reached upper limit of the switching frequency does not allow ZVS for these low currents (see e.g., the description of Fig. 19).

The dependence of the converter's efficiency on the output voltage and current is revealed in Fig. 27. At a full power of 20 kW (100 V, 200 A) an efficiency of 96.4 % was achieved. Maximum efficiency of 97.1 % was achieved at a load of 100 V and 100 A, i.e., maximum voltage and half current. Even at a low output current of 50 A and full voltage of 100 V, the efficiency is still very good at 95.3 %.

VII. CONCLUSION

A three-phase ac/dc soft-switching PFC converter with galvanic separation and good controllability of the output dc voltage was proposed. A quasi-single-stage modular conception with a common integrated transformer was designed. The topology was verified through both theoretical simulations and the practical construction of a 20 kW prototype. The results obtained from simulations and practical measurements confirmed good behavior of the converter and acceptable waveforms, not only at full power but also at reduced output voltage and output current. The practically measured waveforms correspond well to the theoretical simulation results.

A control structure that operated with a variable switching frequency was applied to achieve the switching of the leading leg slightly before the HF current zero crossing at full power. At a reduced dc output current (below ca. 70 A), the HF

current drops to zero before the switching time instant of leading leg, which is not optimal, as explained in Section III. The maximum switching frequency was limited to a relatively low value to avoid unacceptable losses in the driver circuits.

One of the mechanisms responsible for the distortion in the input phase current (steps and ringing) was the commutation of input diode bridges together with the presence of dc link capacitors. This could be suppressed by moving a part of this capacitance in front of the rectifier.

An efficiency map (dependence of efficiency on the dc output voltage and the current) was measured. A maximum efficiency of 97.1 % was achieved.

The efficiency dependence on the output dc current is relatively flat, which is very advantageous when using the converter as a battery charger. The efficiency is more heavily dependent on the output dc voltage; however, this is not relevant when charging a battery, where the voltage changes only within a narrow range and is dependent on the battery state of charge.

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