# A Dual Active Bridge DC-DC Converter for Automotive Applications

## Design of a High Efficiency Bidirectional DAB Converter for the Lightyear One

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TU Delft

Lightyear

# A Dual Active Bridge DC-DC Converter for Automotive Applications

## Design of a High Efficiency Bidirectional DAB Converter for the Lightyear One

by

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# Abstract

In the past years electric cars have been rapidly taking market share in the automotive industry. Stimulated by their sustainable image and due to large investments in the charging infrastructure, the electric automobile has gained popularity in the field of research. Many papers are written on a variety of power converters inside the cars to interface between batteries, chargers and motors. Usually, these converters are made as universal as possible, in order to suit the needs of many different vehicles. As a result, they are capable of operating at wide voltage and power ranges, often at the cost of weight or efficiency.
The Dutch electric car startup Lightyear aims at a completely different strategy. Their car with integrated solar panels is designed with one goal: increasing efficiency. For that reason, all components have been reconsidered and, if sufficient gains in efficiency can be achieved, completely redesigned. One of these components is an isolated bidirectional DC-DC converter that ensures power transfer from the solar panels to the main battery.
In this thesis that DC-DC converter is developed. Special focus is put on maximizing the efficiency to ensure as much energy from the solar panels can be used to power the car. First, all possible topologies that meet the requirements are investigated and the best option is selected. Then, a script is developed that configures the power stage of the converter using a provided list of components. The implementation with the highest average efficiency over the operating range is automatically selected. After that, alternative modulation strategies are investigated, aimed at reducing the conduction losses of the converter. Finally, a controller is created and validated for the designed converter.
The result of the presented work is an isolated bidirectional DC-DC converter, achieving an average power stage efficiency of 98.1 % over a wide range of input voltages and output voltages at a constant power output.

# Acknowledgements

As crazy as it might seem, writing this part of my thesis might have been the hardest for me. During the course of my thesis work I have had the privilege to meet so many great people who helped me, that I do not know where to start, afraid that I might forget to mention someone.
The one that has helped me the most during the development of my project, on both a technical and personal level, and who was never shy of reserving many hours in his agenda to review my work, is Tom, my supervisor within Lightyear. I would like to thank him for guiding me through the project, giving critical feedback and helping me out with whatever question I had.
The next person that logically follows is my supervisor from TU Delft, Thiago. Despite the long distance between Delft and Eindhoven and consequently the one single face-to-face meeting we had, I have experienced his supervising and guidance as extremely helpful. Many Skype calls and even more emails have been sent to which he has always taken the time to help me out. Thank you!
Within Lightyear I have had the pleasure to work with awesome colleagues, but I want to thank a few in particular. A special thank you to Oguzhan, who has supported me throughout the design phase with insightful feedback and many fruitful discussions. Next is the team that reviewed my work and contributed to my thesis in other areas, consisting of among others, Marald, Jeroen, Jose, Michael and Nazar.
On a more personal level I would like to thank my dear parents and family. Whatever step I took in my life, they supported me to the fullest. Without any hesitation they have been there for me, unconditionally believing in me, getting the best out of me and enabling me to pursue my dreams.
Last, but not least, I would like to express my gratitude to my girlfriend, who has always stood by my side. Her warmth, kindness and unconditional support during the course of my studies have been extremely important to me.

*T.B. Huisman*
*Barendrecht, September 2020*

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# 1 Introduction

This chapter introduces the work of this thesis by providing background information and the motivation of the project. First, the company at which this thesis has been carried out will be introduced in section 1.1. It is of importance for the understanding of the background of this thesis that the reader has a good overview of the company and the product it aims to create. Then, the project context will be described in section 1.2, followed by the goals and scope of the project in section 1.3. Lastly, the structure and content of this report will be briefly outlined in section 1.4.

## 1.1. Introduction to Lightyear

For decades in a row, the automotive industry has largely been the same. Large, established car manufacturers ruled the industry with ever so slightly updated models of the same, polluting cars. However, a recent change has been noticed, motivated by, amongst others, the tightening regulations from governments around the globe [1]. Emission of $CO_2$, $NO_x$ and other polluting gasses, which are collectively called greenhouse gasses, emitted by cars need to be lowered, which has motivated car manufacturers to invest in alternative ways of powering cars. This all has led to the emerge of electric vehicles.

One of the major downsides of a battery electric vehicle (BEV) is that the production of the battery pack itself contributes significantly to the emission of greenhouse gasses. Together with the inconvenience of continuously needing to charge the car when not using it make the transition towards BEVs less inviting to people. For that reason, five students from the TU Eindhoven came with the idea to develop a solar-powered electric car back in October 2016.

A BEV with integrated solar panels tackles the aforementioned disadvantages of BEVs. First of all, because of the integration of photovoltaic (PV) panels that deliver energy to the main battery, a smaller battery can be equipped in the car. This smaller battery means less rare-earth materials and less emission of greenhouse gasses in the production of each car, while the range of the car is similar compared to a BEV. Second, since the PV panels can charge the battery continuously, an extension of range as well as fewer charging moments can be realized.

The idea of such a car is revolutionary and got a lot of media attention. Since its founding in 2016, Lightyear has grown to a company of over 100 employees. The focus of the whole company is to develop and build the Lightyear One, the first car of Lightyear. This car, which has 5 $m^2$ of solar panels integrated in its body, is able to drive 725 km on a fully loaded battery according to the WLTP-cycle [2]. This globally standardized drive cycle test is used as a measure to compare the range of different BEVs. In comparison, a Tesla Model 3 Long Range version achieves a range of 518 km on a full charge, according to the same WLTP cycle [3].

In order to achieve such a WLTP range, a highly efficient powertrain needs to be developed. Every component of the car is reconsidered and redesigned if efficiency can be improved. On top of this, highly efficient solar panels charge the battery both while driving and while being parked. The PV panels ensure that up to 40% of the total energy used to drive the car comes from solar energy [1]. This significant number is drastically influenced by all conversion steps from sunlight to electricity, which is then fed to the battery, and eventually

[1] This number is based on the assumption of someone living in the Netherlands and driving 13.000 km per year, which is the yearly average for the Netherlands. Based on different climates and driving frequencies this number will change.

to the motors of the car. One of these steps is the conversion of the voltage from the solar cells into the high voltage battery, which is being addressed in this thesis.

## 1.2. Thesis context

As mentioned before, the converter that is of interest for this thesis will convert the voltage of the solar cells to the voltage of the HV battery pack. In fact, this is a major simplification of the actual system, of which a more detailed sketch is shown in fig. 1.1.

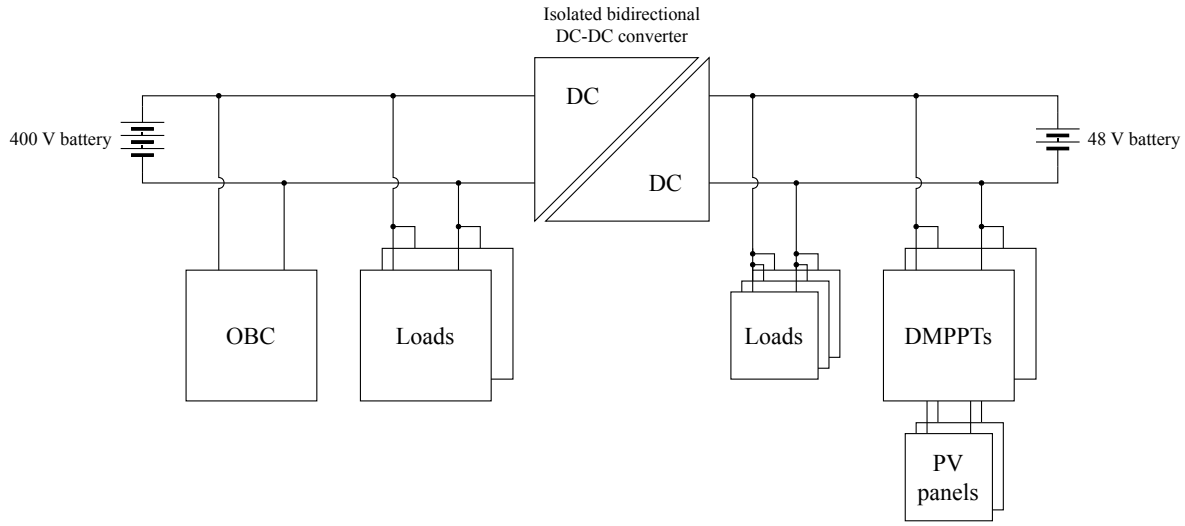



Figure 1.1: A simplified general system overview of the powertrain topology of the Lightyear One.

In the car there are two main DC buses, a 400 V bus and a 48 V bus. Attached to the 400 V bus are among others the main HV battery, an onboard charger (OBC) and several loads, including the inverters to drive the motors of the car. On the 48 V bus the output of distributed maximum power point tracking (DMPPT) converters is connected, as well as a 48 V battery, together with several loads, which are not of interest for this thesis. To harvest the energy of the PV panels as efficiently as possible a special type of converter is needed, which is the DMPPT converter. This converter runs on an algorithm that always operates at the maximum power point that the solar panels can deliver. When one of the solar cells in the string has a lower irradiance, it would limit the total power output of that complete array. With the DMPPTs, the maximum power point is tracked and ensures maximum power under all conditions, as designed in [4].
In between the two main buses an isolated bidirectional DC-DC converter (IBDC) is placed. This converter transports energy from the low voltage (LV) side to the high voltage (HV) side when the solar panels produce a lot of energy and the 48 V battery is full. On the other hand, when the 48 V battery is empty and solar power is not enough to drive the loads on the 48 V bus, power from the main battery will be delivered through the IBDC. So, based on the control strategy employed on the powertrain of the Lightyear One, the IBDC may have to transfer energy from its LV side to its HV side, or vice versa. Therefore, bidirectionality is demanded. Additionally, the two buses should be electrically isolated from each other, meaning that the converter should have galvanic isolation.
From this top level description, the operating conditions of the IBDC can be specified. An overview of the specifications of the to be designed converter is given in table 1.1.

Table 1.1: The specifications of the DC-DC converter.

| Parameter | Minimum | Typical | Maximum |
|---|---|---|---|
| HV side voltage | 260 V | 378 V | 437 V |
| LV side voltage | 42 V | 50.4 V | 57.4 V |
| Operating power | 2.5 kW | | |

The voltages are determined based on the minimum and maximum voltages of both batteries. The operating power of the converter is determined to be a constant 2.5 kW and is not variable. This requirement comes

from the control of the powertrain within the Lightyear One, to which this converter must comply. In all other situations the converter will be turned off to save energy. When operational, it will operate at its peak efficiency point, which will be designed to be at 2.5 kW.
However, the absolute limits of the HV battery will not be reached frequently. Instead, the control of the powertrain is designed in such a way that the main battery never reaches its limits under normal operation. Therefore, a 90 % operating window can be defined, in which the converter will operate 90 % of the time. This is the region for which the converter will be optimized, which is displayed in fig. 1.2.

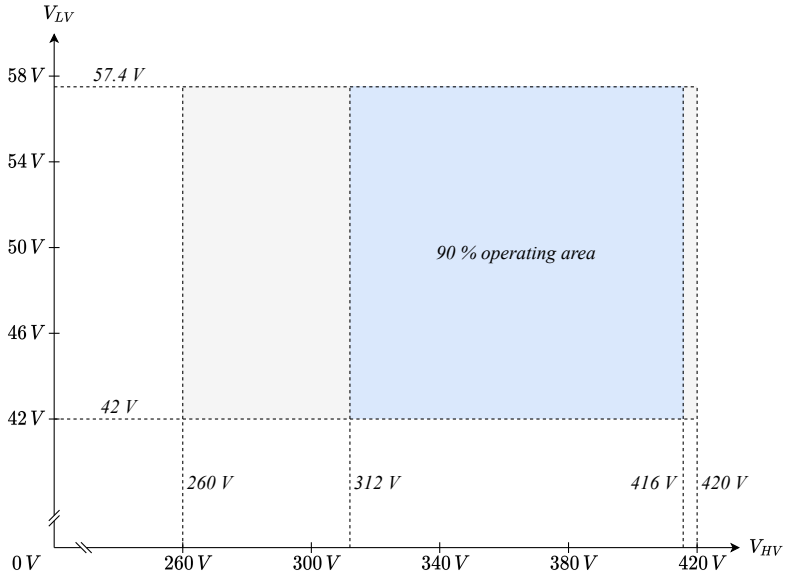



Figure 1.2: The 90 % use case operating window (blue) given within the full operating range (grey) for the bus voltages of the converter.

From the description above together with the project goals as stated by Lightyear, the following requirements for the converter can be listed:

1. The converter needs to ensure a highly efficient power conversion (target > 94 % average power stage efficiency over the 90 % operating range) at a constant power of 2.5 kW (in both directions).

2. The converter needs to have basic isolation with a minimum working isolation voltage of 437 V.

3. The maximum weight of the completed prototype should be no more than 5 kg, including a casing.

4. The components of the prototype should have an automotive rating (AEC-rating).

5. The converter needs to be cooled by either natural or forced convection.

6. The total cost of a single prototype cannot exceed €1000.

The requirements are listed based on priority, with the first one leading the design of the converter. The latter requirements are there to provide a basis for trade-offs. An example can be to go for non-automotive rated MOSFETs if that yields an additional 1 % gain in efficiency.

## 1.3. Thesis goals and scope

The goal of this thesis is to investigate, design, simulate and build a prototype of an isolated bidirectional DC-DC converter. There are no further restrictions than the ones as listed in section 1.2, so the goal of this thesis is to develop the most optimal converter design, given the requirements. The design and simulation of magnetic components will not be a part of this thesis, since Lightyear has a partner for this. The reason is that the design, simulation and manufacturing of automotive rated magnetics is too in-depth to add to the stated scope of this thesis.

### 1.3.1. COVID-19

During the development of the prototype of the designed converter, limitations were encountered due to the consequences of COVID-19. The original goal of the thesis was to validate the design using a fully functional prototype PCB. However, due to the corresponding delays at manufacturing partners of Lightyear (PCB builders, component deliverers etc.) the PCB was not finished before the end of this thesis. Therefore, to compensate the lack of detailed measurements and analysis of the performance of the prototype, the theoretical part of this thesis has been extended with the design of a controller for the converter. The testing and (physical) validation are consequently considered to be future work. However, the design of the prototype PCB, including its thermal design, will be shown in Appendix C to fully cover the work done for this thesis.

## 1.4. Report structure

The content of this thesis is structured as follows. Chapter 2 investigates the most suited converter topology for this project. Relevant literature is reviewed and analyzed to reduce the optional topologies to three promising candidates. Then, the candidates are investigated in terms of performance for the given operating conditions of the eventual converter, after which the best solution is picked. In chapter 3 a detailed loss model for the chosen converter is made, together with a script that constructs the most efficient combination of components for the given topology across the operating region. After that, chapter 4 describes the different modulation methods for the selected topology to further increase the efficiency and decrease component stress. Based on the findings of chapter 3 and 4, a control algorithm is designed and validated in chapter 5. Finally, the conclusions and future recommendations for this thesis work are given in chapter 6.

# 2

# Topology

Many topologies exist that can be used for the design of an isolated bidirectional DC-DC converter. First, a selection of suitable topologies is made, which is discussed in section 2.1. Then, based on the converter requirements a selection of the three most promising topologies will be made. From there on, these three topologies are investigated. The operation principle and characteristics of these converters are described individually per topology in sections 2.2–4. Finally, in section 2.5 the three topologies will be compared after which one ise chosen as the best option for this particular converter design.

## 2.1. Isolated bidirectional converters

From the requirements given in section 1.2, a few apply to the choice of topology and are summarized below for convenience.

1. The topology needs to ensure a highly efficient conversion at a constant power level.
2. The topology needs to contain as little components as possible in order to reduce weight, size and cost.
3. The topology needs to offer galvanic isolation.

Since the requirements specify the need of an isolated converter, this narrows down the options regarding topologies. Within the selection of isolated converters a distinction will be made between several topologies based on the number of switches. This results in one group of isolated bidirectional converters which are non-(half)bridge switch topologies, one group of converters built-up of bridges (either half or full bridges) and the last group built-up of bridges with a resonant tank present. An overview of the different topologies can be seen in fig. 2.1.

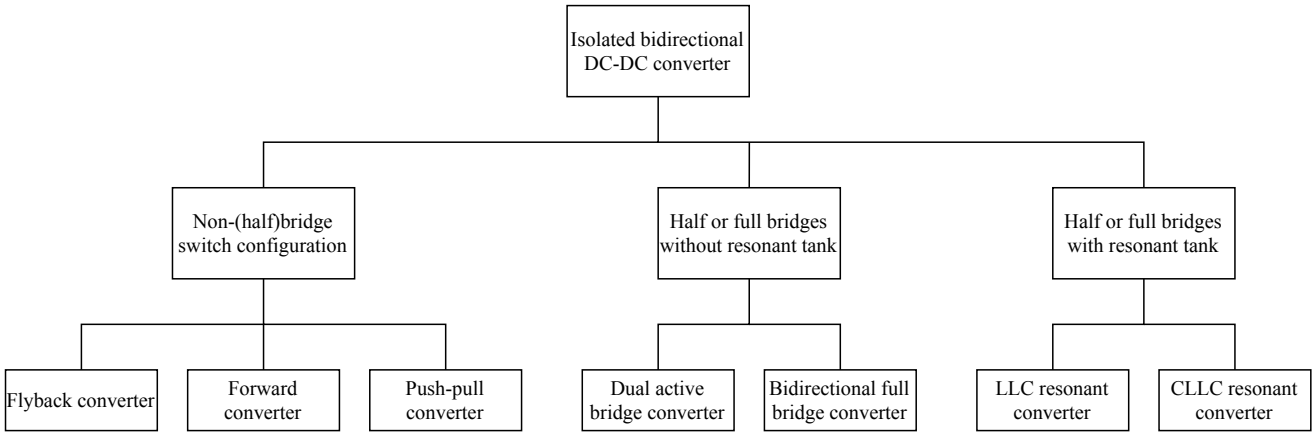



Figure 2.1: An overview of the different isolated bidirectional DC-DC converter topologies.

### 2.1.1. Non-(half)bridge switch configuration converters

Within this first group, many of the converters derived from non-isolated converters can be placed [5, 6]. Examples of these converters are the flyback (derived from buck-boost converter) and the forward converter (derived from the buck converter). These converters are not bidirectional in their standard form, so to make them bidirectional one can either replace the diodes by switches or place two converters anti-parallel to each other. With the latter option, one of the converters is active depending on the direction of power flow.

**Flyback converter**

The flyback converter is one of the simplest isolated converters, consisting of a minimum amount of components. Its topology can be seen in fig. 2.2 and consists of one switch, a transformer, a diode and a capacitor.

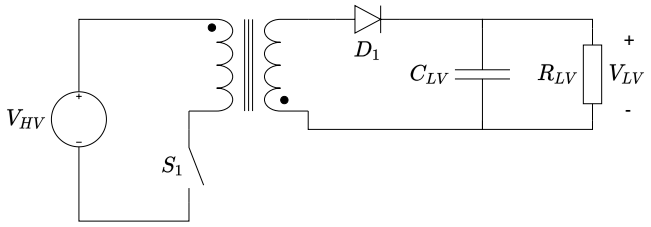



Figure 2.2: Schematic of a flyback converter.

The main advantage of a flyback converter is its limited number of components. Due to this simplicity the operation principle is straightforward and the cost, volume and weight of the converter can be kept low. However, flyback converters are known to be less efficient than alternative topologies. Since efficiency is one of the key design goals of the final converter, the flyback is considered to not be a good candidate.

**Forward converter**

Another isolated converter is the forward converter. Its topology is based on a buck converter and can be seen in fig. 2.3.

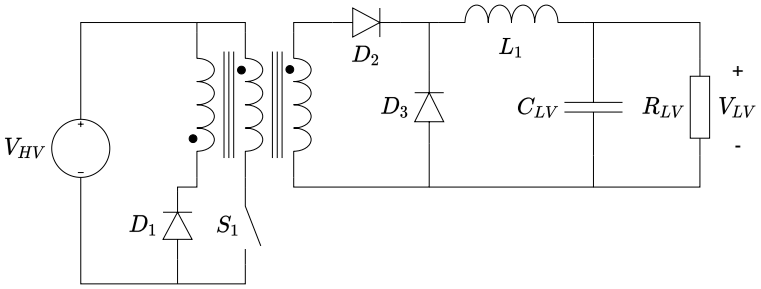



Figure 2.3: Schematic of a forward converter.

The forward converter is more suited for higher power applications, in contrast to the flyback converter [7]. One of the reasons is that the flyback has to store energy in the transformer, while for the forward converter the stored energy can be retrieved and fed back to the input via diode $D_1$. A disadvantage of the forward converter is that it has a complicated transformer design, together with an additional filter inductor at the LV side. Combined with the fact that the forward converter is most suited for medium power levels (up to 500 W) [7], makes that the forward converter is not considered as a good option for this converter design.

**Push-pull converter**

The last non-(half)bridge converter that was selected is the push-pull converter. It consists of a center tapped transformer, two switches, two diodes and an LC filter at the output as can be seen in fig. 2.4.
Push-pull converters are widely used in higher power circuits, up to 1000 W typically [7]. When comparing the push-pull converter to the flyback and forward converter it can be seen that the transformer utilization is improved. The push-pull topology allows the core to be magnetized in both directions. Additionally, the typical power range of this topology is in the range of power of the converter that has to be designed for this thesis. A parallel connection of two push-pull converters per direction can be sufficient. However, the typical

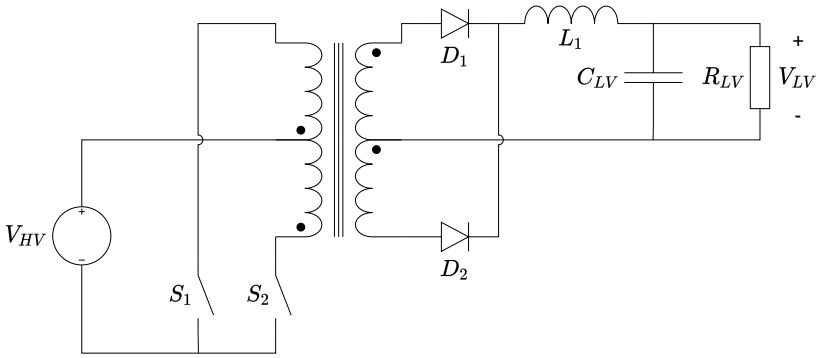



Figure 2.4: Schematic of a center tapped push-pull converter.

efficiency for the push-pull converter in fig. 2.4 is still not as high as the efficiencies that can be obtained with the bridge-based converters. Therefore, the push-pull converter is disregarded as a potential topology.

### 2.1.2. Bridge-based converters without resonant tank

Within the group of bridge-based converters, the most promising efficiencies, modularity and simplicity can be found for the dual active bridge (DAB) converter and the bidirectional full bridge converter. Because of the full bridges, the converters are automatically bidirectional. For that reason a single converter can be used instead of two (or more) anti-parallel unidirectional converters.

**DAB converter**

The first selected bridge based converter is the DAB converter. It was first introduced by [8] and consists of two full bridges connected by a high frequency (HF) transformer. The topology of a DAB converter can be seen in fig. 2.5.

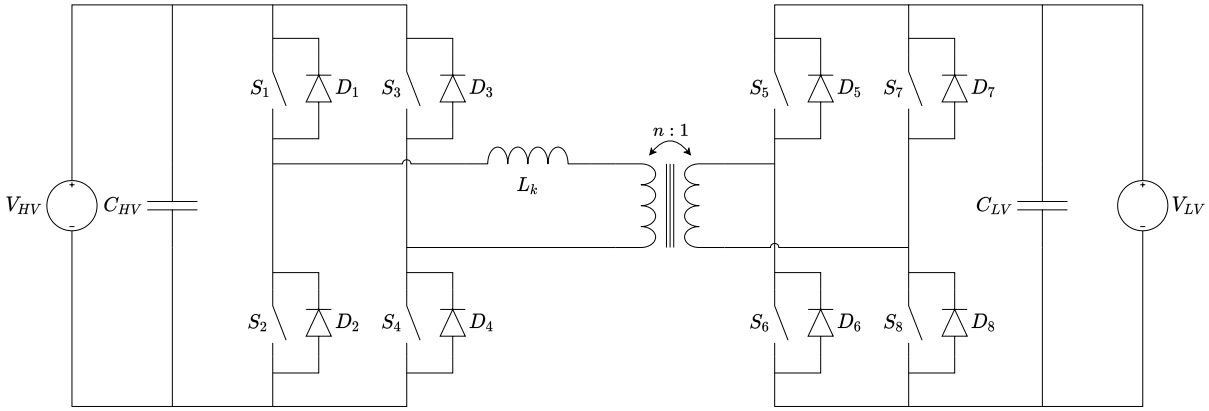



Figure 2.5: Schematic of a dual active bridge converter.

As can be seen from the figure, the DAB converter has its leakage inductance of the HF transformer depicted as well. The reason is that this topology makes use of the otherwise parasitic inductance for its power transfer. Due to the symmetrical topology, bidirectionality is inherently present and modelled in fig. 2.5 as a voltage source on both ends of the converter. This symmetry allows for an easy operation and flexibility with respect to control schemes [5].
Disadvantages of the dual active bridge topology are the large amount of switches and the high ripple currents in the bus capacitors of the lagging bridge [9]. Despite these disadvantages, the DAB converter will be further investigated in section 2.2 as a potential candidate.

**Bidirectional full bridge converter**

An alternative to the DAB converter is the bidirectional full bridge converter. This topology consists of two full bridges coupled by an HF transformer, similar to the DAB. The LV bridge has an inductor in series with the output, creating a current-fed bridge as shown in fig. 2.6.

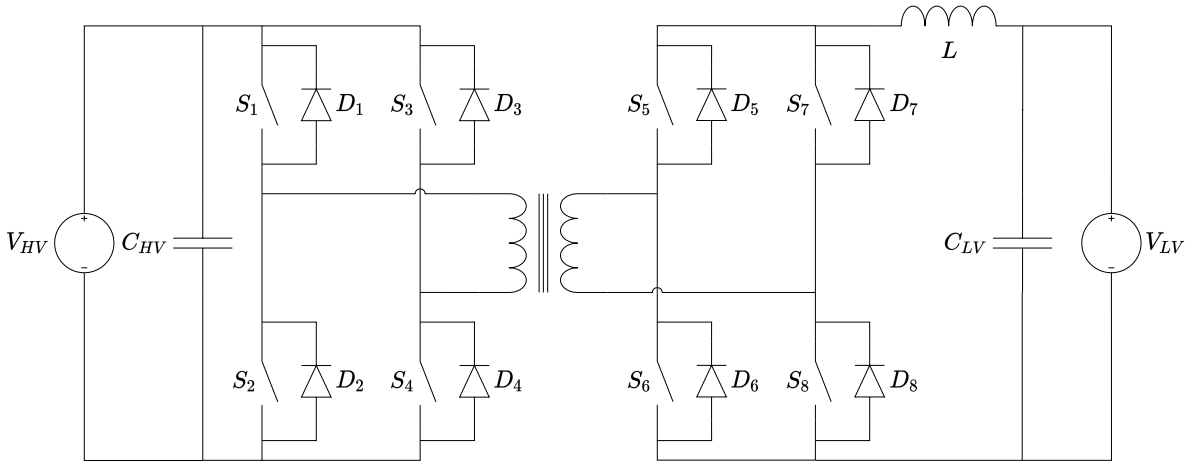



Figure 2.6: Schematic of a bidirectional current-fed full bridge converter.

An advantage of this current-fed topology is that the LV side capacitor ripple is lower compared to the DAB converter [9] when power is transferred from the HV to LV bus. However, the switches experience higher current stresses than in the DAB. This, together with the fact that an additional large DC inductor is needed that is difficult to manufacture [10], makes the bidirectional current-fed full bridge converter less suitable for this converter design.

### 2.1.3. Bridge-based converters with resonant tank

The last group of converters consists of bridge based converters with a resonant tank. The resonant tank ensures soft switching over a wide range of powers. In literature many resonant topologies can be found [11–15], of which the resonant tank can be built-up out of different configurations of inductors and capacitors [16]. The potential candidates have been limited to full bridge topologies, since these allow for more degrees of freedom with respect to optimal control and optimization of the converters [17].

**LLC resonant converter**

The main bridge based resonant converter that is selected is the LLC resonant converter. As the name suggests, its resonant tank consists of two inductors and one capacitor, as is depicted in fig. 2.7.

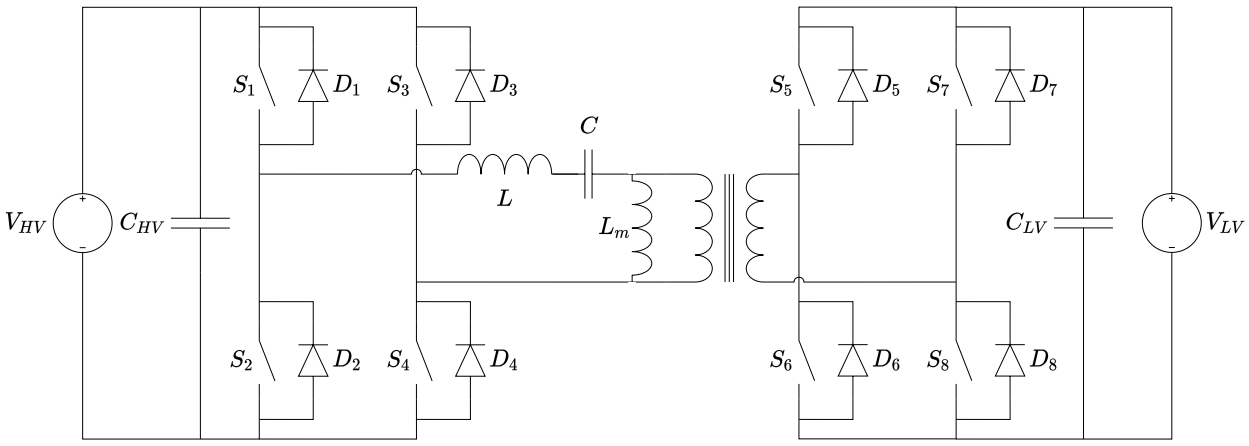



Figure 2.7: Schematic of a bidirectional LLC resonant converter.

The resonant tank can be recognized to be of a series resonant type, meaning that it can be modelled as a series loaded resonant (SLR) circuit. The exact operation of this tank will be discussed in more detail in section 2.3. Because of this resonating tank the transformer currents are nearly sinusoidal, which means that this topology has reduced transformer RMS currents compared to the DAB converter. A potential downside of the LLC converter is that it operates optimally when the ratio between the HV bus and LV bus voltage lies

close to the transformer winding ratio. Still, the LLC converter will be further analyzed in section 2.3 as it is expected to be a good contender for the final converter design.

**CLLC resonant converter**
Another type of resonant converter that has been picked for a brief investigation is the CLLC resonant converter. Similarly to the LLC converter, the name of this topology indicates how the resonant tank is built-up, namely out of two inductors and two capacitors. The schematic of this converter can be seen in fig. 2.8.

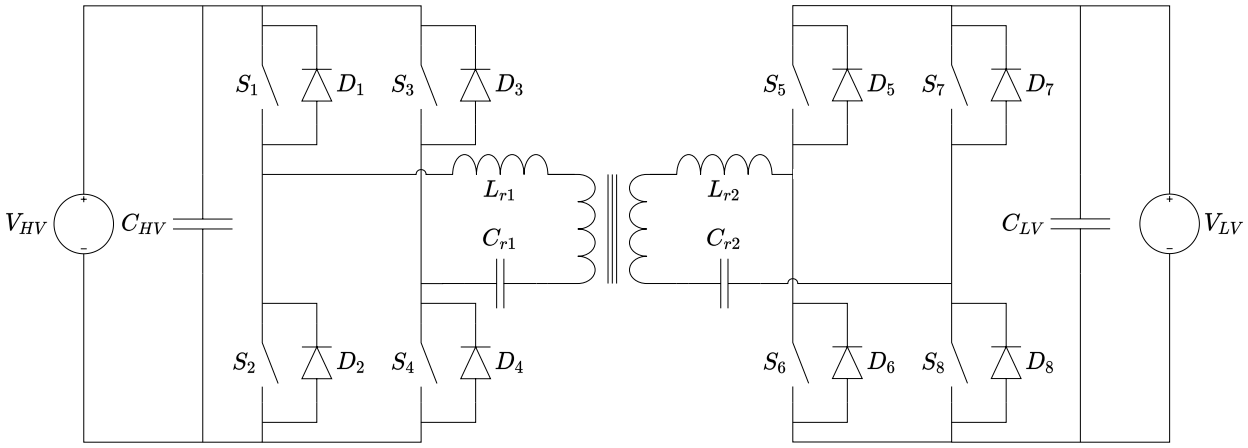
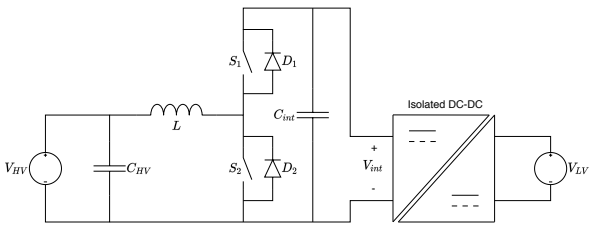



Figure 2.8: Schematic of a bidirectional CLLC resonant converter.

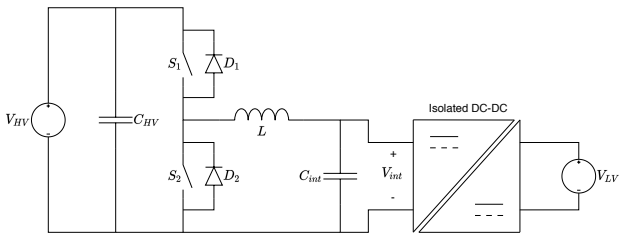
A major advantage of the CLLC converter over the LLC converter is that it is symmetrical. This allows for a better and more straightforward bidirectional control [18, 19]. However, the additional resonant capacitor increases the total number of energy storage components to four, thereby greatly raising the complexity of analyzing the behaviour of the circuit [20]. For that reason the CLLC converter is not considered to be a suitable option for this converter design.

## 2.1.4. Multi-stage converters

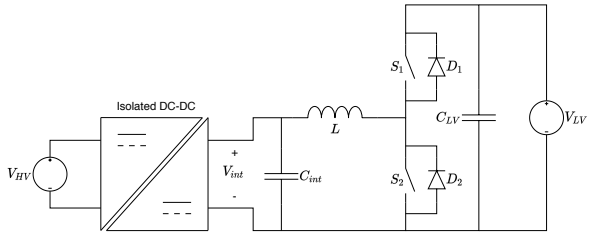
So far, the only considered converters have been single stage topologies. A multi-stage topology can be an interesting choice for the design of this converter as the operating conditions dictate a wide voltage range on both the HV bus and LV bus. Since one of the objectives of the design of the converter is to keep its size and weight low, only options will be considered where the additional stage is built-up out of a simple bidirectional buck or boost converter. With this decision there are four optional topologies, which can be seen in fig. 2.9.



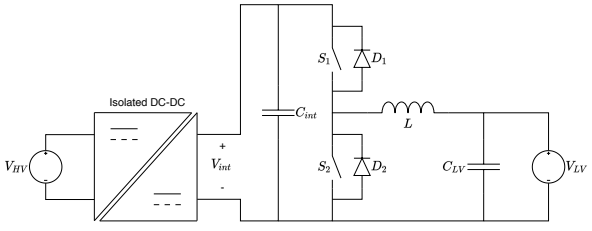

(a) A bidirectional boost stage at the HV bus.




(b) A bidirectional buck stage at the HV bus.




(c) A bidirectional boost stage at the LV bus.




(d) A bidirectional buck stage at the LV bus.

Figure 2.9: The four options for placement of bidirectional buck or boost converters.

Each option will create an intermediate voltage level, which is called $V_{int}$. This intermediate voltage has a different level depending on the additional stage, which will be discussed individually.

**Boost stage at the HV bus**
By placing a boost stage at the HV side (fig. 2.9a), a new voltage level is created that is higher than the HV bus voltage level itself: $V_{int} > V_{HV}$. A positive consequence of this is that at a similar power level the intermediate bus current will be reduced, thereby greatly reducing the conduction losses of the bidirectional isolated converter. However, this increased voltage means that the switches need to have a higher blocking voltage. Since switching losses can be expected to be limited due to the aim of achieving zero voltage switching (ZVS) at the HV side of the isolated stage, this option appears to be promising. However, when looking into optional switches, it can be seen that semiconductors with a breakdown rating above 600 V are very limited. Within the range of interest, which will be a $V_{ds}$ of 800 V for the boost stage at the HV side, only 400 optional switches exist, in contrast to 1700 switches for a $V_{ds}$ of 600 V. The price for switches with a higher blocking voltage is almost quadruple of that of comparably performing [1] switches at 600 V. Based on this significant increase in costs and the limited amount of semiconductors, this topology is considered not suitable.

**Buck stage at the HV bus**
Replacing the HV stage with a bidirectional buck converter (fig. 2.9b) has the opposite effect when compared to the boost stage at the HV bus. Since the intermediate voltage level will be lower than the HV bus voltage, $V_{int} < V_{HV}$, conduction losses will increase due to the flow of higher currents. The blocking voltage rating of the switches will drop, typically leading to a decrease of the on-state resistance, $R_{ds,on}$. Additionally, the buck stage will reduce the voltage swing of the HV side of the isolated stage, thereby contributing to an increased performance there.

**Boost stage at the LV bus**
The first option for an additional stage at the LV side of the isolated converter is to place a boost topology (fig. 2.9c). The effect of this boost stage is that the intermediate voltage level is lower than the LV bus voltage, $V_{int} < V_{LV}$. This means that the intermediate voltage level will be even lower than 48 V. When the converter would operate at full power, this lower voltage would lead to excessive current levels. For that reason, this option is not considered any further.

**Buck stage at the LV bus**
The second option for an additional stage at the LV side would be to implement a buck topology. This means that the intermediate voltage level is raised above the LV bus voltage: $V_{int} > V_{LV}$. When a buck stage is added at the LV side it will be difficult to realize an efficient high current buck converter. The design of high current, low voltage converters is generally difficult when the aim is to have high efficiencies (e.g. higher than 90%) without complex control or (liquid) cooling [9]. This leads to this option being less suitable for the converter design.

### 2.1.5. Conclusion

The remaining converter topologies that have not been eliminated yet are the following:

- Dual Active Bridge converter
- LLC resonant converter
- Two-stage converter with buck stage at the HV side

All of these topologies appear to be attractive for this converter design. So far, only a descriptive analysis has been done for each topology. In order to narrow down the choice to one single topology, the remaining converters will be analyzed individually. Per converter the operation principle and its limitations will be discussed to get a more profound understanding of the three topologies.

[1] To compare the switches the following figure of merit (FOM) has been used: $Q_G \cdot R_{ds,ON}$. This FOM incorporates no switching losses, as these are expected to be non-existing due to ZVS in the isolated stage.

## 2.2. Dual active bridge converter

This section will go over the operation principle of the DAB converter. The DAB can be controlled using a variety of control schemes, given the fact that it is symmetrical and therefore highly controllable. To get a basic understanding of the operation of the DAB only the single phase shift (SPS) control will be considered. It is assumed that this mode of operation will give enough insight in the advantages and limitations of the DAB converter.

### 2.2.1. Simplified circuit

The analysis starts with deriving a simplified schematic of the DAB converter in order to reduce the complexity of the analysis. The DAB will be controlled using SPS control, which makes the diagonal switches of the full bridges being operated with a 50 % duty cycle. The resulting output of the bridges is a square wave. Consequently, the voltage-fed full bridges can be modelled as two ideal voltage sources. Additionally, the converter is assumed lossless, the transformer is assumed ideal and the converter is operating in steady state, meaning that the DC HV bus and LV bus voltages do not change. Finally, all secondary (LV) side quantities are referred to the primary (HV) side via the turn ratio of the ideal transformer, resulting in the simplified circuit of fig. 2.10b.

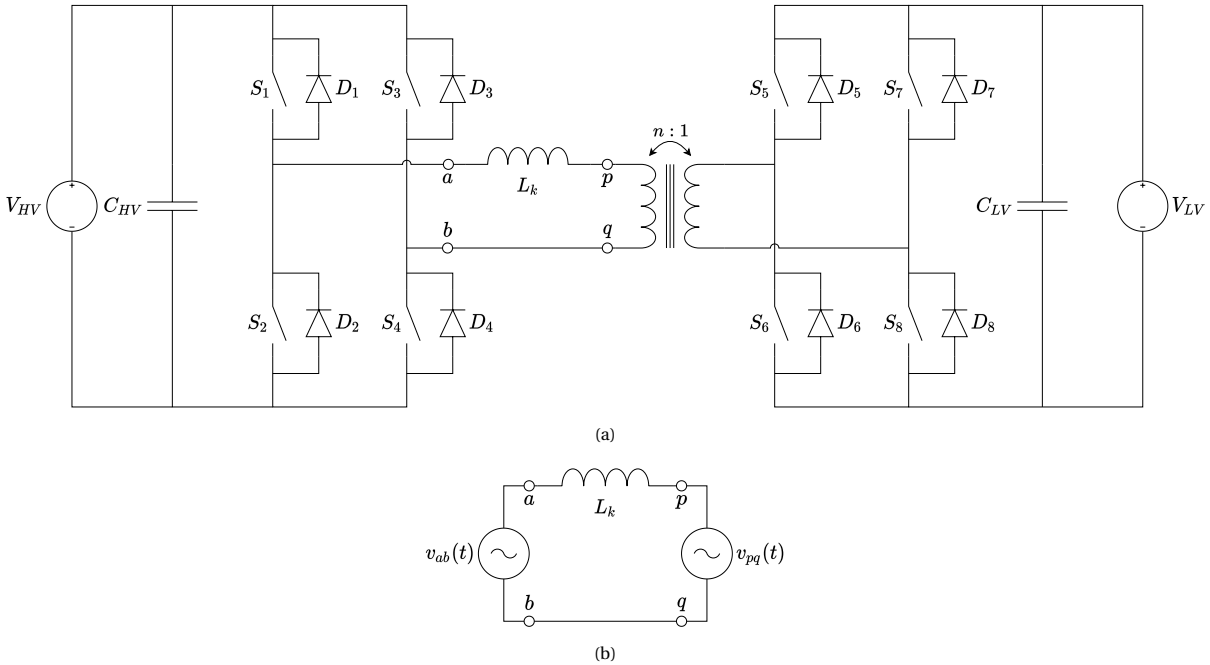



Figure 2.10: (a) The DAB converter with the ports of the HF transformer labelled. (b) Simplified schematic of the DAB converter.

Here, $v_{ab}(t)$ and $v_{pq}(t)$ are square wave voltages that are created by the full bridges in the real converter. $v_{ab}(t)$ has an amplitude of $V_{HV}$ and $v_{pq}(t)$ has an amplitude of $nV_{LV}$. In this ideal circuit the ratio between the HV bus and LV bus voltage is assumed to be close to the transformer turn ratio, meaning that both sides of the inductor $L_k$ in fig. 2.10b experience a square wave with comparable amplitude. In the case of larger voltage differences the peak currents can drastically increase, as can be concluded from the voltage-current relation of an inductor:

$$V_{L_k} = L_k \frac{di_{L_k}}{dt}. \tag{2.1}$$

### 2.2.2. Operation principle

In order to control the power flow through the converter the phase shift between the two waveforms can be controlled. The power transfer through an inductive element excited by two square waves can be expressed as [5]:

$$P = \frac{nV_{HV}V_{LV}}{2\pi^2 f_s L_k}\varphi(\pi - \varphi), \tag{2.2}$$

where $f_s$ is the switching frequency and $\varphi$ is the phase shift in radians. If the switching frequency is assumed to be constant, from eq. (2.2) it can be seen that the power transfer of the DAB converter with SPS control can be regulated by the phase shift $\varphi$ between the two square waves produced by the full bridges. The waveforms and corresponding current through the inductor $L_k$ can be seen in fig. 2.11.

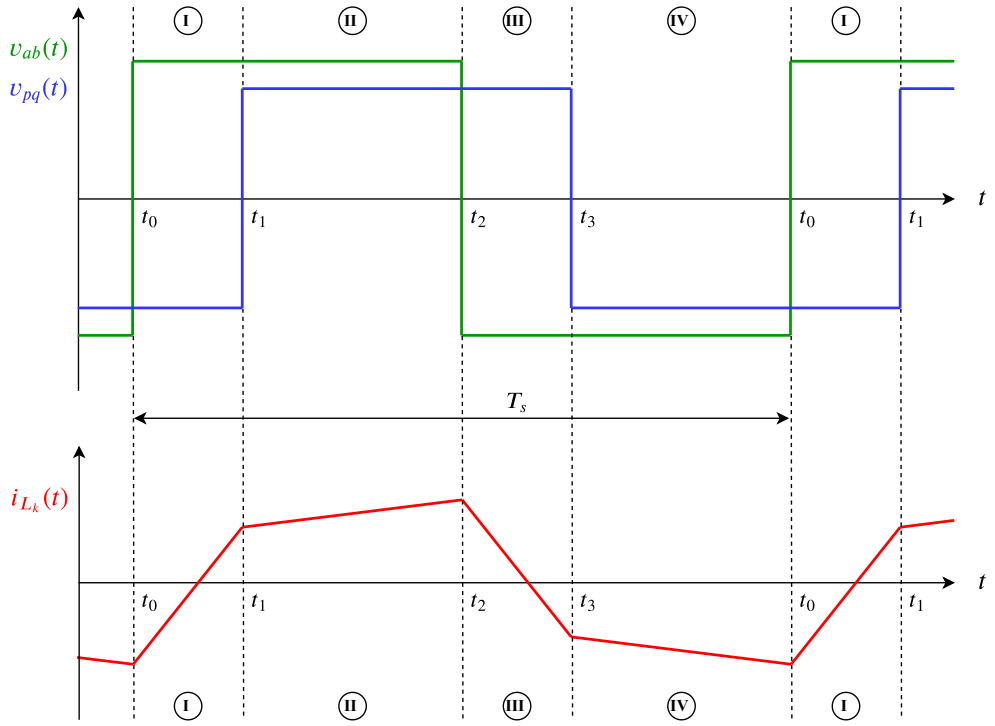



Figure 2.11: Ideal waveforms of the simplified DAB converter for SPS control in steady state.

As can be seen from fig. 2.11 it is possible to divide one period into four individual parts. Further, for SPS control it holds that the voltage waveforms and current waveform repeat every half of the switching period with a reversed sign. The inductor current is shaped according to the voltage across it at a given time instant, where the slope can be calculated by rewriting eq. (2.1):

$$\frac{di_{L_k}}{dt} = \frac{V_{L_k}}{L_k}, \tag{2.3}$$

where $V_{L_k} = v_{ab}(t) - v_{pq}(t)$. The possible voltage levels of $v_{ab}(t)$ and $v_{pq}(t)$ for SPS control can be expressed as:

$$v_{ab}(t) = \begin{cases} +V_{HV} & \text{for } t_0 \le t < t_2 \\ -V_{HV} & \text{for } t_2 \le t < t_0 \end{cases} \tag{2.4}$$

$$v_{pq}(t) = \begin{cases} +nV_{LV} & \text{for } t_1 \le t < t_3 \\ -nV_{LV} & \text{for } t_3 \le t < t_1. \end{cases} \tag{2.5}$$

### 2.2.3. ZVS region

As described before, one of the advantages of the DAB converter is its soft switching capability. However, the power range for which soft switching is achieved is limited. In order to make a trade-off between the three

converters it is important to analyze this region of soft switching. Hard switching will significantly increase the total losses of the converter and needs to be prevented. An analytical expression for the zero voltage switching (ZVS) region will be derived in this subsection.

In general, ZVS turn-on is achieved by having a switch close when the voltage across it is approximately zero. In the case of MOSFETs, the body diode allows for a built-in ZVS possibility. When a current flows through this body diode, it inherently means that the voltage across the drain and source will be near zero (just the forward voltage drop of the diode), resulting in ZVS when the MOSFET is turned on. In a similar way, a diode can be placed in parallel to the switching device to provide this ZVS option. For the DAB converter ZVS can be achieved because of a resonant transition during a switching moment. This resonance takes place between the parasitic output capacitance of the switches and the inductor $L_k$. The energy stored in the inductor allows for a displacement of the energy that is stored in the output capacitance of the switches of the full bridge [21]. This process can be described in a more analytical way. First, some important points in the inductor current waveform of fig. 2.11 need to be defined. This is done in fig. 2.12, where the phase shift is expressed as $\delta \cdot T_s$, with $\delta$ being a fraction of the total switching time $T_s$.

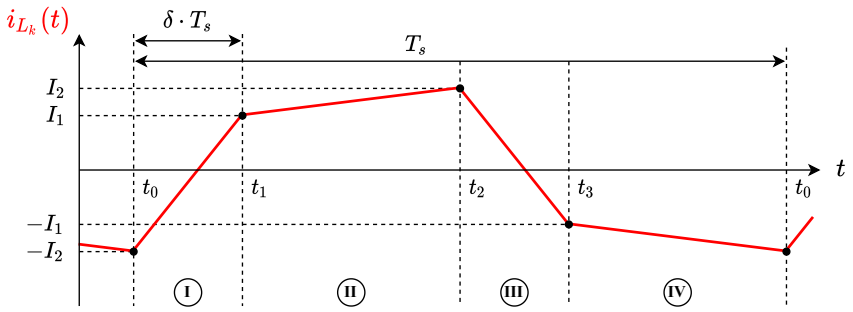



Figure 2.12: Zoomed ideal inductor current waveform of the simplified DAB converter for SPS control in steady state.

The instantaneous values of the inductor current during the switching instances have been labeled $I_1$ and $I_2$ for time instance $t_1$ and $t_2$, respectively. Because of the earlier mentioned symmetry of the current waveform, the values of the current waveform at switching instance $t_3$ and $t_0$ are similar to $t_1$ and $t_2$, respectively, with a change of sign:

$$\begin{aligned} I_1 &= i_{L_k}(t_1) = -i_{L_k}(t_3), \text{ and} \\ I_2 &= i_{L_k}(t_2) = -i_{L_k}(t_0). \end{aligned} \tag{2.6}$$

An expression for the currents $I_1$ and $I_2$ can be derived. The reason these current points are of interest, is because for ZVS the values of these currents should be larger than zero for the transition between switching period I and II, and between period II and III, as defined by fig. 2.12. When $I_1$ is larger than zero, ZVS is obtained for the lagging bridge, which is the LV bridge in this case. In a similar way, an inductor current $I_2$ that is larger than zero will ensure ZVS for the leading bridge, which is the HV bridge in this example. Because of the symmetry, for the transition between period III and IV, and IV and I, the inductor current should be negative. The reason for this is that the remaining energy in the inductor $L_k$ should be sufficient to transfer the energy stored in the output capacitance of the switches. Since the energy stored in an inductor is proportional to the current flowing through it, the currents $I_1$ and $I_2$ should be larger than zero to obtain a positive energy.

The inductor current can be easily derived by rewriting eq. (2.3) into

$$\frac{\Delta i_{L_k}}{\Delta t} = \frac{V_{L_k}}{L_k}. \tag{2.7}$$

By using eq. (2.4), eq. (2.5), eq. (2.7), the definitions shown in fig. 2.12 and assuming that the HV bus voltage $V_{HV}$, LV bus voltage $V_{LV}$, switching frequency $f_s$ and the inductance $L_k$ are known, an expression for the inductor current during switching period I can be derived as:

$$\frac{I_1 + I_2}{\delta \cdot T_s} = \frac{V_{HV} + n \cdot V_{LV}}{L_k}. \tag{2.8}$$

In a similar way an expression for period II can be found as:

$$\frac{I_2 - I_1}{\left(\frac{1}{2} - \delta\right) T_s} = \frac{V_{HV} - n \cdot V_{LV}}{L_k}. \tag{2.9}$$

A system of equations is formed by eq. (2.8) and eq. (2.9), which has two unknowns, $I_1$ and $I_2$. This means the system can be solved for both currents, resulting in:

$$I_1 = \frac{T_s}{4L_k}\left(n \cdot V_{LV} - V_{HV} + 4\delta \cdot V_{HV}\right) \tag{2.10}$$

$$I_2 = \frac{T_s}{4L_k}\left(V_{HV} - n \cdot V_{LV} + 4\delta \cdot n \cdot V_{LV}\right). \tag{2.11}$$

With these expressions, the boundary conditions for ZVS can be obtained. For this converter design it is valuable to know the ZVS limits for different voltage transfer ratios. As the HV bus and LV bus voltage swing are large, it is important to evaluate whether ZVS can be achieved for all operating points. When the voltage transfer ratio is defined as

$$M = \frac{n \cdot V_{LV}}{V_{HV}}, \tag{2.12}$$

then eq. (2.10) and eq. (2.11) can be rewritten as

$$I_1 = \frac{T_s \cdot V_{HV}}{4L_k}\left(1 - M + 4\delta \cdot M\right) \tag{2.13}$$

$$I_2 = \frac{T_s \cdot V_{HV}}{4L_k}\left(M - 1 + 4\delta\right). \tag{2.14}$$

For ZVS it was explained that both these inductor currents should be larger than zero. Imposing this condition and solving eq. (2.13) and eq. (2.14) for the phase shift ratio $\delta$ results in:

$$I_1 > 0: \qquad \delta > \frac{M-1}{4M} \tag{2.15}$$

$$I_2 > 0: \qquad \delta > \frac{1-M}{4}. \tag{2.16}$$

With the conditions imposed by eq. (2.15) and eq. (2.16) for the phase shift ratio $\delta$ an overview can be made for the ZVS region, depending on the voltage transfer ratio $M$. In fig. 2.13 a plot of the voltage gain $M$ against the positive phase shift ratio $\delta$ is shown. It should be mentioned that fig. 2.13 is symmetrical around the y-axis for $\delta < 0$.

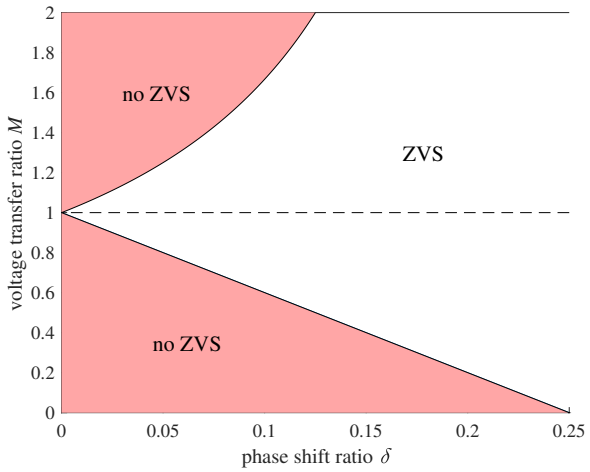



Figure 2.13: ZVS region for the ideal DAB converter.

The analysis so far has only considered the fact that the inductor current at time instances $t_1$ and $t_2$ should be larger than zero. It can be seen from fig. 2.13 that ZVS will only be possible for certain combinations of voltage transfer ratio $M$ and phase shift ratio $\delta$. An increased $\delta$ allows for a wider range of HV bus and LV bus voltages, however, a higher transferred power is an implicit consequence, as follows from eq. (2.2).
The conditions dictated by eq. (2.15) and eq. (2.16) are on its own not sufficient to guarantee that the voltage across the switch will be zero when switched on. As briefly mentioned before, the output capacitance of the switches that are turning on need to be fully discharged. This might not be the case when the inductor current at time instance $t_1$ or $t_2$ is slightly larger than zero. When the inductor current drops to zero, the energy in the capacitances of the switches could not yet have been transferred. So, eq. (2.15) and eq. (2.16) are incomplete; the energy in the output capacitance of the switches needs to be considered.
Described in a more analytical manner, the energy stored in the inductor at the end of region I and region II needs to be larger than the energy stored in the capacitances across the switches:

$$E_{L_k} > E_{C_{tot}} \quad \Rightarrow \quad \frac{1}{2} L_k i_{L_k}^2 > 4 \cdot \frac{1}{2} C_{tot} V_C^2, \tag{2.17}$$

where $C_{tot}$ is the total equivalent capacitance across a switch of the full bridge ($S_x$ in the figures, where $S_x$ can consist of multiple parallel switching devices) and $V_C$ is the voltage across the switches when the energy exchange takes place. For the HV side bridge $V_C$ is equal to $V_{HV}$ and for the LV side bridge equal to $V_{LV}$. Rewriting eq. (2.17) into a requirement for the inductor current leads to:

$$i_{L_k} > 2 \cdot V_C \sqrt{\frac{C_{tot}}{L_k}}. \tag{2.18}$$

Finally, by combining eq. (2.18) with eq. (2.15) and eq. (2.16) leads to

$$\delta > \frac{M-1}{4M} + \frac{4\sqrt{L_k \cdot C_{tot,in}}}{T_s \cdot M} \tag{2.19}$$

$$\delta > \frac{1-M}{4} + \frac{4M \cdot n \cdot \sqrt{L_k \cdot C_{tot,out}}}{T_s}. \tag{2.20}$$

To conclude, the inductor current values at time instances $t_1$ and $t_2$ should be larger than 0 and large enough to ensure that sufficient energy is left in the inductor to transfer the energy between the capacitors. It should be mentioned that the no-ZVS region as shown in fig. 2.13 will expand due to the additional conditions imposed by eq. (2.19) and eq. (2.20). With this ZVS region and the analysis of the power transfer of the DAB converter using SPS control, enough information is gathered on this topology for a more thorough comparison with the LLC topology and two-stage converter.

## 2.3. LLC converter

For the LLC converter a similar approach will be used as for the DAB converter in section 2.2. First, the converter schematic shown in fig. 2.7 will be simplified to do a basic analysis of the operation of the LLC converter. Then, specific operating conditions and limitations will be discussed, such that they can be compared with the limitations of the DAB converter and the two-stage converter.

### 2.3.1. Simplified circuit

The schematic of the LLC converter can be simplified in a similar way as the DAB converter. By recognising that the full bridges output a square wave to the resonant tank, the simplified circuit as shown in fig. 2.14b can be derived. In this simplified circuit, the transformer is considered ideal and only the magnetizing inductance is represented in the equivalent model of fig. 2.14b. The LV side voltages and currents are referred to the HV side, thereby eliminating the transformer completely. The resulting simplified LLC circuit can be recognized and treated as a series loaded resonant (SLR) circuit, in which the following formulae apply [6]:

$$i_L(t) = I_{L0} \cdot \cos\big(\omega_0(t-t_0)\big) + \frac{V_{ap} - V_{C0}}{Z_0} \sin\big(\omega_0(t-t_0)\big) \tag{2.21}$$

$$v_C(t) = V_{ap} - \big(V_{ap} - V_{C0}\big) \cdot \cos\big(\omega_0(t-t_0)\big) + I_{L0} Z_0 \sin\big(\omega_0(t-t_0)\big), \tag{2.22}$$

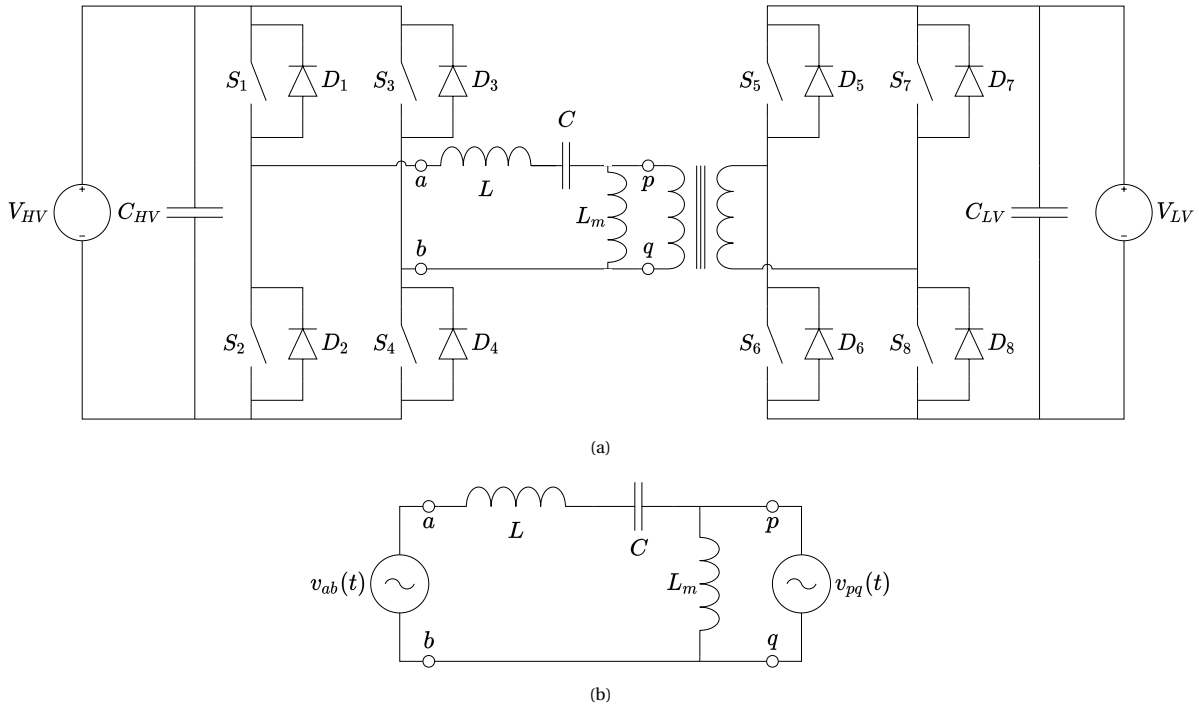



Figure 2.14: (a) The LLC converter with the ports of the HF transformer labelled. (b) Simplified schematic of the LLC converter.

where $V_{ap}$ is the voltage over the combination of $L$ and $C$, $\omega_0$ is the natural frequency and $Z_0$ is the characteristic impedance of the resonating circuit consisting of $L$ and $C$. In the time interval where a resonance cycle occurs, it is assumed that the HV and LV bus voltages applied to the resonant tank can be modelled as DC. When eq. (2.21) and eq. (2.22) are applied and analyzed it can be shown that at regular time instances ZVS and ZCS can occur. Since the current through $L_m$ is controlled by the voltage source $v_{pq}(t)$, this current can be analyzed by the first order differential equation according to eq. (2.1) [9].

### 2.3.2. Operation principle

The operation of the full bridges of the LLC converter is largely similar to that of the DAB. The output of the HV side bridge is a square wave voltage, which is applied to the resonant LLC tank. The result is a nearly sinusoidal current flow through the transformer, to which the LV side provides synchronous rectification. A difference with the DAB topology is that the LLC topology is not symmetrical. As a consequence, the operation in forward mode, from HV input to LV output, differs from the operation in backward mode. For that reason, the operation will be separately discussed for the two modes.

**Operation in forward mode**

To simplify the analysis of the operation principle, the first harmonic approximation (FHA) is used [11]. FHA assumes that only the first harmonic of the waveforms is responsible for power transfer between the bridges. The advantage of this simplification is that the circuit can be characterized in a much simpler, yet accurate way. This means that instead of characterizing $v_{ab}(t)$ as a square wave voltage, this input voltage of the resonant tank can be represented as:

$$v_{ab}(t) = V_{HV} \cdot \frac{4}{\pi} \cdot \sin(\omega t). \tag{2.23}$$

To further simplify the analysis, the equivalent AC resistance of the LV full bridge can be written as [22]:

$$R_{LV,AC} = n^2 \cdot \frac{8}{\pi^2} \frac{V_{LV}^2}{P_{LV}}. \tag{2.24}$$

Lastly, before any further calculations will be done, the following substitutions are introduced, as defined in [22]:

$$V'_{LV} = n \cdot V_{LV}, \qquad f_{r1} = \frac{1}{2\pi\sqrt{LC}}, \qquad k = \frac{f_s}{f_{r1}},$$
$$h = \frac{L_m}{L}, \qquad Z_0 = \sqrt{\frac{L}{C}}, \qquad Q = \frac{Z_0}{R_{LV,AC}}. \tag{2.25}$$

Here, $k$ is the ratio between the switching frequency and the first resonant frequency of the LLC tank, $Z_0$ is the characteristic impedance of the resonant tank and $h$ is introduced together with $Q$ to remove the values of the inductors and to keep the formulae more intuitive.
It can be seen from eq. (2.25) that the value of $Q$ is affected by the load. For high output powers, when $R_{LV,AC}$ is low, a high value of $Q$ will be realized, for low loads, $Q$ will be low too. The last variable that will be introduced is $f_{r2}$, which is the switching frequency at which the voltage transfer ratio $M$ (which is defined below) is maximal. From here, the voltage transfer ratio can be determined, which can be worked out to

$$M = \frac{V'_{LV}}{V_{HV}} = \frac{1}{\sqrt{\left(Q\left(k - \frac{1}{k}\right)\right)^2 + \left(1 + \frac{1}{h} - \frac{1}{hk^2}\right)^2}}. \tag{2.26}$$

An important aspect of the LLC resonant converter can be shown now, when the voltage gain is plotted for different switching frequencies, and different load powers (different values of Q), as shown in fig. 2.15a.

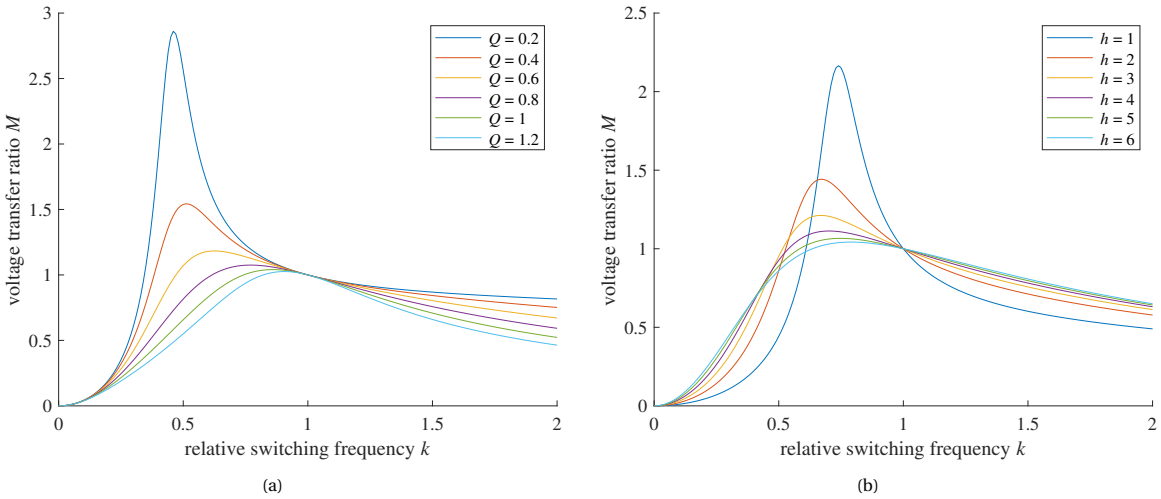



Figure 2.15: The voltage transfer ratio of the LLC converter plotted against the relative switching frequency $k$ for (a) different power levels $Q$ with $h = 4$ and (b) different inductor ratios $h$ with $Q = 0.7$.

From fig. 2.15a it can be seen that for high load powers (a high value of $Q$) the LLC resonant converter is limited in its ability to support a wide LV bus voltage range. In this example, the transformer turn ratio $n$ is put to 7. Now, looking at the requirements for the converter that has to be designed, the maximum voltage transfer ratio that should be achieved is

$$M_{max} = \frac{n \cdot V_{LV,max}}{V_{HV,min}} = \frac{7 \cdot 57.4}{260} \approx 1.55, \tag{2.27}$$

which will only be achievable when having a $Q$ of $0.2 - 0.4$ (for an $h$ of 4). This imposed restriction on Q means that full power will not be achievable for the LLC. This is a major downside, as the resonance works best around the region where the voltage ratio $M$ is close to the transformer winding ratio $n$. Additionally, it can be seen from fig. 2.15 that around $M = 1$ there are many options for switching frequencies and inductor ratios $h$. This would give a good ability to optimize the converter around that area. When the LLC converter is operated as the second conversion stage, in the two stage scenario, the performance and flexibility of the

converter can be improved. As an example, if the HV bus voltage would be kept at 345 V by a first stage, $M_{max}$ will be reduced to $(7 \cdot 57.4)/345 \approx 1.16$, which is close to 1, even for the worst case scenario of the converter.
Another conclusion that can be drawn from fig. 2.15 are the limited options for voltage transfer ratios $M$ when the switching frequency is higher than the resonant tank frequency $k > 1$. Moreover, large variations in switching frequencies are needed to obtain a slight change in the voltage gain in this region, as the gain curve shows for $k > 1$. This region does allow for ZVS on the HV side though, whereas on the LV side ZCS can be achieved [22].
The opposite is true for switching frequencies below the resonant tank frequency. Here, a wide variety of voltage gains can be realized with minimum changes in the switching frequency. Additionally, when $M$ is close to 1, a wide power range can be supported. However, since the behavior of the resonant tank is capacitive for switching frequencies below $f_{r2}$, ZVS is lost for this region of operation [11]. For that reason, this region of switching frequencies has to be avoided to ensure a highly efficient operation of the converter.
The last conclusion that can be drawn from this analysis is that the voltage transfer ratio $M$ can be boosted by changing the ratio between the two inductors of the LLC design, $L$ and $L_m$. The effect can be seen in fig. 2.15b, where a similar value of $L$ and $L_m$ results in a high voltage gain just before $k = 1$. This means that the resonant tank of the LLC converter can be highly tuned depending on the application and requirements.

**Operation in backward mode**

Even though the LLC topology is not symmetrical, the backward operation does not differ much from the forward operation, as will be shown in this section. For starters, the voltage gain formula as defined by eq. (2.26) should be adjusted [22]:

$$M = \frac{V_{HV}}{V'_{LV}} = \frac{1}{\sqrt{\left(Qk - \frac{Q}{k}\right)^2 + 1}}. \tag{2.28}$$

Similarly, a new expression for the $Q$ can be derived from eq. (2.28), resulting in [22]:

$$Q = \frac{R_{HV,AC}}{Z_0} = \frac{Z_0 \pi^2}{8} \frac{P_{HV}}{V_{HV}^2}. \tag{2.29}$$

Similar to the forward mode the voltage transfer ratio $M$ can be plotted against the relative switching frequency $k$ for different output powers. This plot is shown in fig. 2.16.

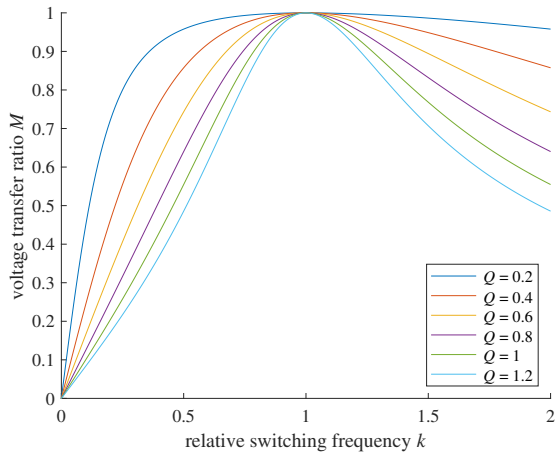



Figure 2.16: The voltage transfer ratio of the LLC converter in backward mode plotted against the relative switching frequency $k$ for different power levels $Q$.

Now that all equations for the LLC in both modes are known, the similarities to the SRC can be displayed. As mentioned before, the current of inductor $L_m$ is solely determined by the voltage over it, which is $V'_{LV}$. This means that the magnetizing inductance is not actively contributing to the power transfer of the converter and does not participate in the resonance effect of the tank. For this resonance, only $L$ and $C$ are contributing.
This means that the tank can be approached as an SRC topology, which means that eq. (2.21) and eq. (2.22) hold. From the SRC it is known that its output voltage cannot be controlled for no-load cases [11]. This

drawback will not be of high importance for this application of the converter, since the DC-DC converter to be designed, will only operate at a constant power. Another drawback of the SRC and thus the LLC converter, is the fact that high ripple currents will be experienced by its output capacitor [11], which in the case of the LLC depends on the transferred power direction. Because of the mentioned drawbacks the suitability of the LLC converter needs to be reconsidered.

Many downsides that are mentioned in this section can be overcome by applying certain switching schemes. For now, the basic operation principle and limitations of the LLC converter have been discussed. Possible solutions are present, but will not be discussed until the LLC will be opted as the most promising topology. At a later stage, if the LLC will be chosen as the best candidate, the switching schemes and patterns will be considered.

## 2.4. Two stage converter

In this section, a more detailed description is given for the buck operation and the boost operation of the added converter. As was concluded before, the decision is made to create an intermediate voltage level between the HV bus and the input of the isolated converter stage by means of a buck stage. For convenience, a zoomed version of the schematic of the buck stage depicted in fig. 2.9b is given in fig. 2.17.

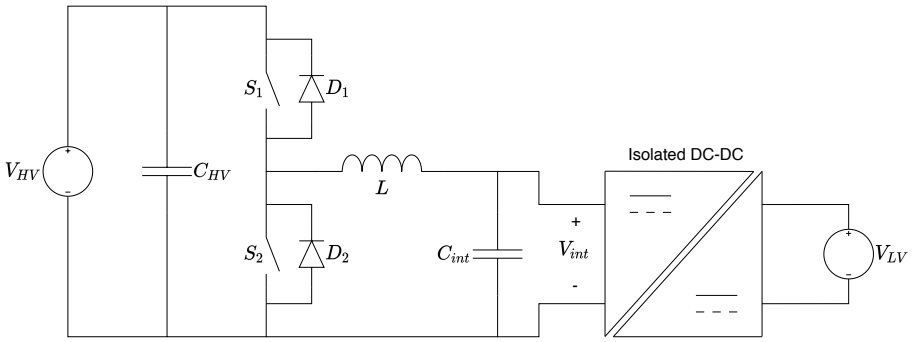



Figure 2.17: The schematic of the two stage converter with a buck stage at the HV side.

### 2.4.1. Buck operation

For the buck operation of the converter, the well-known formulae for a buck converter apply. The waveforms for the buck operation can be seen in fig. 2.18.

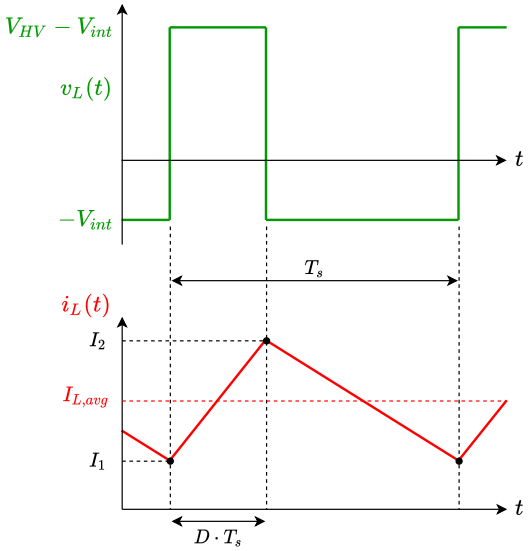



Figure 2.18: Ideal waveforms for buck operation of the bidirectional buck converter.

The relation between the output voltage of the buck converter, $V_{int}$, to the input voltage, $V_{HV}$, can be expressed by the duty cycle as:

$$D_{buck} = \frac{V_{int}}{V_{HV}}. \tag{2.30}$$

In order to get an indication of the losses in the converter, some average and RMS values of currents are needed. First, the average current through the inductor can be obtained by assuming steady state operation, which leads to:

$$I_{L,avg} = \frac{P_{int}}{V_{int}}, \tag{2.31}$$

where $P_{int}$ is the power of the buck stage which is fed to the second stage. Additionally, the inductor RMS current needs to be calculated. To do so, the current ripple is needed. By considering the voltage over the inductor during the OFF period of the switch, the following formula can be obtained:

$$\Delta I_L = \frac{V_{int}(1-D)}{f_s \cdot L}. \tag{2.32}$$

Now that the inductor currents are known, the RMS current through the inductor can be obtained.
The derivation of the RMS currents can be found in Appendix A.1. From the derivations it can be seen that the RMS current of the inductor can be decomposed into a constant value, $I_{L,min}$ and the triangular waveform $i_{L,ripple}(t)$. Using the definition of RMS current, it can be found that the RMS current through the inductor can be expressed as:

$$I_{L,RMS} = \sqrt{\frac{1}{12} I_{pp}^2 + I_{L,avg}^2}, \tag{2.33}$$

as given by eq. (A.9), where $I_{pp}$ is the peak-to-peak current ripple.
In a similar way, the switch and diode currents can be expressed, based on the inductor currents. The average switch current and RMS current can be expressed as:

$$I_{sw,avg,buck} = D_{buck} \cdot I_{L,avg} \tag{2.34}$$

$$I_{sw,RMS,buck} = \sqrt{D_{buck}} \cdot I_{L,RMS}. \tag{2.35}$$

Finally, the diode currents can be expressed as:

$$I_{D,avg,buck} = \left(1 - D_{buck}\right) \cdot I_{L,avg} \tag{2.36}$$

$$I_{D,RMS,buck} = \sqrt{1 - D_{buck}} \cdot I_{L,RMS}. \tag{2.37}$$

### 2.4.2. Boost operation

Similar to the buck operation, for the boost operation of the converter, the well-known boost converter formulae apply. The ideal waveforms for the boost mode can be seen in fig. 2.19.
The relation between the output voltage of the boost mode to its input voltage can be expressed as

$$\frac{V_{int}}{V_{HV}} = \frac{1}{1-D}. \tag{2.38}$$

To get an estimate of the losses in the converter, average and RMS values of currents through the components are needed. It can be derived that for similar operating conditions as the buck mode (CCM, constant HV and LV bus voltages, no losses, similar output powers) the duty cycle of the buck mode and boost mode relate as

$$D_{boost} = 1 - D_{buck}. \tag{2.39}$$

From here, it follows that the calculated inductor average and RMS currents from the buck mode can also be applied for the boost mode. The only difference is that the input and output voltage in the formulae swap

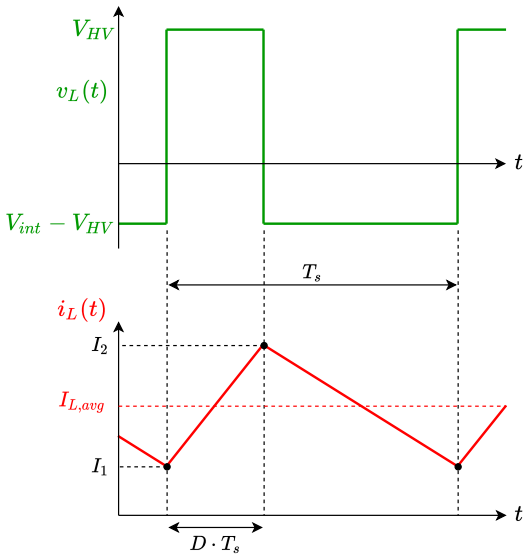



Figure 2.19: Ideal waveforms for boost operation of the bidirectional buck converter.

and that the duty cycle of the boost converter should be applied. Considering the other currents in the circuit results in:

$$I_{sw,avg,boost} = D_{boost} \cdot I_{L,avg} \tag{2.40}$$

$$I_{sw,RMS,boost} = \sqrt{D_{boost}} \cdot I_{L,RMS} \tag{2.41}$$

$$I_{D,avg,boost} = \left(1 - D_{boost}\right) \cdot I_{L,avg} \tag{2.42}$$

$$I_{D,RMS,boost} = \sqrt{1 - D_{boost}} \cdot I_{L,RMS}. \tag{2.43}$$

It can be seen from both the buck and boost mode that the conduction losses will be significant as the full inductor current has influence on the losses in the switch and the diode. On top of the conduction losses, the switching losses will be added. It is expected that these additional losses will be higher than the losses that will be saved in the isolated stage by adding an additional converter. This expectation is confirmed by the research done in [9], where a single stage DAB converter is compared to a two stage converter. The latter consists of a similar bidirectional buck converter (called a buck-or-boost converter) and a DAB converter as isolated stage. The average efficiency of the two stage converter is lower than the average efficiency of the single stage DAB. The operating conditions of the converters in [9] are similar to the converter that has to be designed in this thesis, meaning that the results from the PhD dissertation can be applied to this converter design as well.

## 2.5. Selected topology

Based on the analysis of the three optional circuits a final decision regarding the topology of choice has to be made. The final decision is to go with the DAB converter, based on the literature research and calculations as presented in this chapter. The main reasons to not go for certain topologies will be repeated once again in this section, to provide a concise overview of the decision.

**DAB converter**

The main advantage of the DAB converter is its ease of operation. Due to its symmetry the direction of power flow does not influence the efficiency[2]. Besides, the number of components is lowest for the DAB converter when compared with the other options. Moreover, overall component stresses are low for the DAB topology, despite the fact that the lagging bridge capacitor experiences large ripple currents. Additionally, the large ZVS range for wide voltage swings and soft switch options of the DAB converter make it very attractive when efficiency over the whole operating range is an important criterion. Finally, a lot of optimization techniques, modulation schemes and highly efficient prototypes have been presented in literature as the DAB converter

[2]The symmetry of the converter is only achieved when no external series inductor is used to obtain the desired leakage inductance.

has gained popularity in recent years due to its advantages.
Remaining downsides of the DAB converter are the high conduction losses when compared with other topologies. Additionally, the decreased efficiency for wide input and output voltage ranges is a drawback with respect to this design. Still, this drop in efficiency is lower for the DAB than for the LLC resonant converter.

**LLC converter**
One of the attractive features of the (full bridge) LLC converter is the fact that the ZVS range is increased for multiple power levels with respect to the DAB converter. The LLC converter outperforms the DAB converter at low power points, simply because in this region the DAB loses ZVS where the LLC still ensures soft switching. Together with the nearly sinusoidal transformer waveforms this ensures low losses. Moreover, the efficiency of an LLC converter on a specific operating point can be made higher than with a DAB converter. The tuning of the resonant tank can be tailored to perform best at a desired operating point.
Drawbacks of the LLC are the additional components, the more complex control and its vulnerability to wide input and output voltage ranges. The latter is not a strong point for the DAB either, however, it influences the efficiency of the LLC converter even more. Literature has proposed some solutions, but usually those imply additional components or a more complex control scheme.

**Two stage converter**
The idea of a two stage converter is very attractive in combination with one of the earlier mentioned converters. The advantage of an additional stage is that it can tackle one of the major disadvantages of both converters. Since both the LLC and DAB are isolated, this means that a simple buck-or-boost converter can be implemented, adding a minimal amount of components. Together with the possibility of reducing component stress of the isolated stage by providing an extra degree of design freedom (the intermediate voltage level can be freely chosen) makes the two stage an interesting trade-off.
Obviously, the main disadvantage of this solution is that the additional stage should be highly efficient. The losses that are saved by limiting the voltage swing of one side of the isolated stage should be larger than the introduced losses of this additional stage. In other words, the efficiencies of both individual stages needs to be around 97-98 % (total two stage efficiency will then be 94 %) in order to outperform the single stage DAB converter (DAB converters with efficiencies higher than 94 % have been presented in literature [21, 23–25]). This in itself is a considerable challenge, especially since buck converters suffer from high switching losses. For that reason, together with the additional hardware, costs and volume of the extra stage, the two-stage converter is found not to be suitable. Additionally, [9] designed a two-stage converter with comparable operating conditions and showed that the overall efficiency is lower than for a single stage DAB.

## 2.6. Adjustment to the dual active bridge converter

Now that the DAB converter has been selected as the best candidate, there is one more topic to investigate, which is the saturation of the magnetics. There is a remark to the use of a transformer in the DAB topology. The average voltage over the transformer should be zero such that no DC current bias can build-up in the transformer core, which would lead to saturation. Since there is very little energy stored in the (series) leakage inductance, a small variation in voltage waveforms or duty cycles would lead to unbalance and saturation of the transformer core. Additionally, a DC bias will lead to the reduction of the ZVS region for one switching leg, and increase the ZVS region for the other leg. This leads to uneven losses, which, if not properly monitored, could lead to device failure.

There are several solutions to overcome this issue, of which one is to add an air gap to the transformer core. This will not solve the above mentioned problem of DC bias, but will drastically reduce its effects and gives some headroom to counter the unbalance in voltage with control. The air gap will increase the total reluctance of the path the flux will take. This decreases the inductance, meaning that less flux is created with the same current. In the end, this would mean that the transformer core will saturate less quickly, thereby introducing more margin and time for control to counter the DC bias current. An alternative solution is to add a DC blocking capacitor in series with the leakage inductance, which will be introduced in this section. Lastly, a current sensor should be placed to monitor the DC bias of the inductor current, so that a current control loop can be added to the control.

In series with the leakage inductance (in practice in series with the external inductor and transformer), the capacitor(s) can be placed. The best location for the cap is before the inductor on the HV side, to limit the magnitude of current it will experience. Also, care should be taken with the value of this capacitor, since it

introduces an LC network, together with the external inductor and leakage inductance of the transformer (not the magnetizing inductance, this is way too large compared to the leakage). A good practice is to limit the resonance frequency of this LC network to maximum 20 % of the switching frequency. Anything lower is good, therefore 10 % is used such that the capacitor will actually operate as a DC blocking device rather than create oscillations. The schematic overview of the DAB topology has been updated with the additional DC blocking capacitor and can be seen in fig. 2.20.

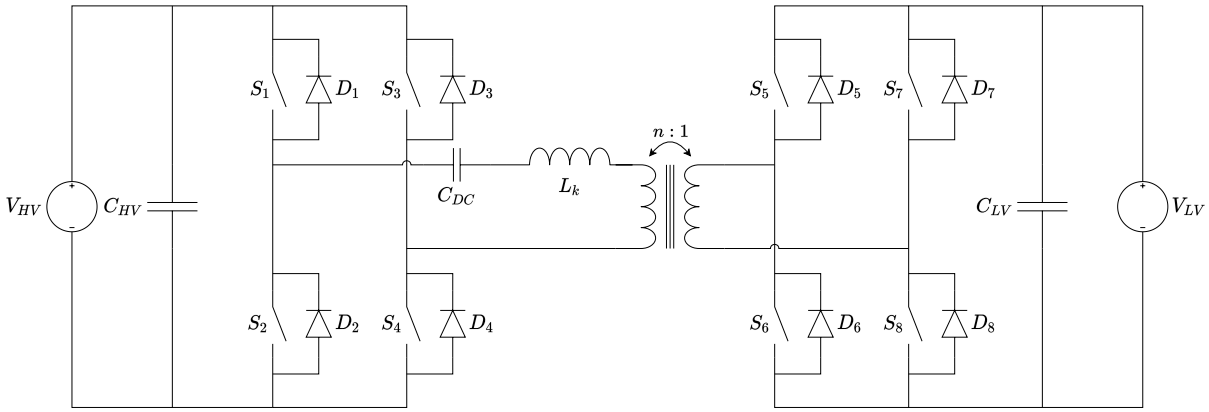



Figure 2.20: Schematic of a dual active bridge converter with added DC blocking capacitor.

When this series capacitor $C_{DC}$ is added, ideally no DC current can build-up in the transformer and inductor. However, still care should be taken with this assumption, as the voltage waveforms are continuously changing and can therefore provide unbalance.

In this thesis, the DC bias capacitor is implemented and will be discussed in the component selection process. However, for calculations on the operation of the DAB converter in steady state, the effect of the DC blocking capacitor will be ignored. When its capacitance is chosen to be as such that the natural frequency of the leakage inductor and series capacitor is 10 % of the switching frequency, its effect on the steady state behavior can be neglected. It does still contribute to the losses due to the presence of a series resistance (ESR), which will be taken into account. For the rest it is assumed for all analyses that the converter operates in steady state with symmetrical, balanced voltage waveforms over the leakage inductor.

# 3

# DAB Converter Loss Model

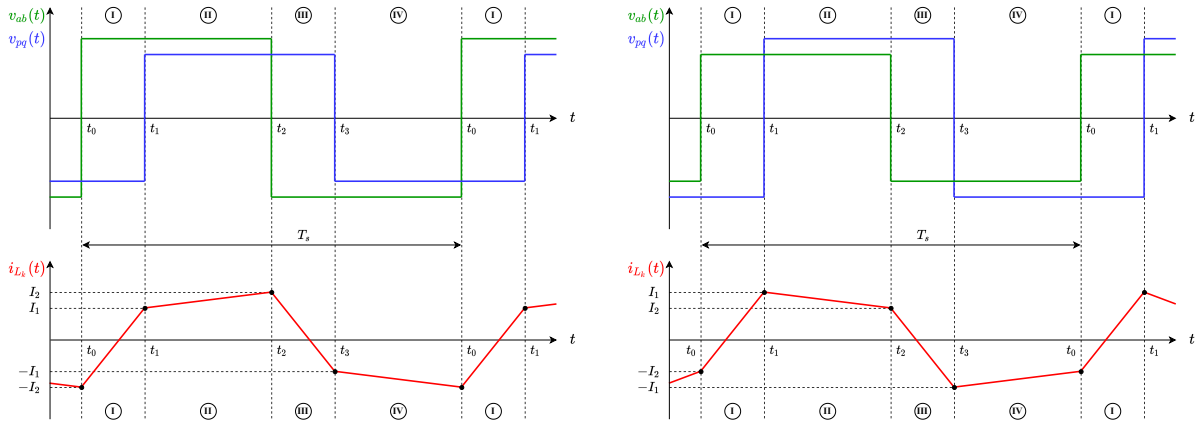
The DAB converter has been chosen due to its variety of advantages, such as a high possible efficiency, low number of components and its simplicity. In section 2.2.3 it appeared that the efficiency of the DAB was influenced by the voltage transfer ratio $M$ and the phase shift $\varphi$. One of the contributing factors is that soft switching might be lost for certain operating points, which leads to additional switching losses. Especially at the HV bridge these switching losses can be significant. During hard switching the parasitic capacitances of the switches have to be discharged when turning on, which is all dissipated in the switch itself. In order to quantify the losses that are present in the switches as well as the other components, section 3.1 will describe the loss models that are created for the components of the DAB. Then, these loss models will be implemented in a numerical minimum search script, which runs multiple converter designs in order to find the one with the highest efficiency. The design and implementation of this minimum search script, that makes use of SPS modulation, will be discussed in section 3.2. Finally, the chapter ends with a discussion of the results of the optimizer and the optimal component choice for the DAB converter in section 3.3. In this chapter for now only positive power is considered, which is defined as a net power transfer from the HV side to the LV side. For negative power the principles remain the same. In the actual models and minimum search script, both power directions have been considered.
Throughout this chapter, the switching frequency is assumed to be given. Determining the optimal switching frequency is an iterative process which influences many parameters. Therefore, an initial switching frequency of 100 kHz was selected based on a qualitative trade-off between converter sizing (especially the magnetic components) and expected switching losses, in a similar way as in [9]. After that, a sensitivity analysis was done using the designed minimum loss script around 100 kHz, from which it turned out that the lowest losses were obtained for 100 kHz. Therefore, the DAB converter will be operated at 100 kHz, which is the frequency that is used for all loss models in this chapter.

## 3.1. Loss models

The first step in finding the minimum loss converter design is by reproducing the voltage and current waveforms for SPS modulation. The reason is that the loss models of the components require the current values or the voltage waveforms to compute the losses. To this end, first the average and RMS values of the leakage inductor current will be computed, followed by the loss models of the different components in the DAB converter. The calculated average and RMS currents will be used in these loss models.

### 3.1.1. Calculation of the inductor current

For SPS modulation there are two typical waveforms. The first is for the case that $V_{HV} > nV_{LV}$, which will be called SPS-1, and the second for $V_{HV} < nV_{LV}$, which is labelled as SPS-2. These two waveforms are shown in fig. 3.1a and fig. 3.1b, respectively.
As can be seen from the figures, in the case of SPS-1 the inductor peak current is determined by $I_2$, whereas for SPS-2 the peak current is dictated by $I_1$. In this chapter, only SPS-1 will be used to derive the average and RMS values of the current. The current values for SPS-2 can be obtained in a similar way.
In order to calculate the average and RMS values of the currents, eq. (2.10) and eq. (2.11) can be used. It is assumed that the average value of the inductor current $i_{L_k}(t)$ is zero, since the average values of the applied




(a) SPS-1

(b) SPS-2

Figure 3.1: The two possible waveforms for SPS modulation. (a) with $V_{HV} > V_{LV}$ and (b) with $V_{HV} < V_{LV}$.

voltages $v_{ab}(t)$ and $v_{pq}(t)$ must be zero to prevent saturation of the transformer core. Using this property, the peak-to-peak inductor current, $I_{pp}$, which is needed in one of the loss models, can be easily found as twice the value of $I_1$.
Now, the RMS value of the inductor current waveform has to be computed. The RMS value is relevant as it will be used to compute the conduction losses in the DAB. To calculate the RMS value, the inductor current waveforms as shown in fig. 3.1 can be recognized as periodic piecewise linear functions. Each function can be split into segments, in which the current is linear. The RMS value of such a function can be expressed as [26]:

$$I_{L_k,RMS} = \sqrt{\sum_{k=1}^{K} D_k u_k}, \tag{3.1}$$

where $K$ is the total number of segments in one period, $k$ is the current segment number that is being computed, $D_k$ is the duty cycle of segment $k$ and $u_k$ is the contribution of that segment. The duty cycle is the segment duration time with respect to the total switching cycle time. The contribution $u_k$ corresponding to a trapezoidal segment, like period II of $i_{L_k}(t)$, having a nonzero beginning $I_1$ and nonzero ending $I_2$, is expressed as

$$u_k = \frac{1}{3}\left(I_1^2 + I_1 I_2 + I_2^2\right). \tag{3.2}$$

From here, both the RMS value of the inductor current as well as the average current over the whole switching cycle of the inductor can be calculated, with the latter one being zero. In a similar fashion, the switch RMS current can be calculated. The difference between the HV and LV switch currents differs by the transformer turn ratio $n$. Every switch conducts the inductor current for 50 % of the time, resulting in:

$$I_{sw,RMS} = \begin{cases} \sqrt{0.5} \cdot I_{L_k,RMS} & \text{for HV switches} \\ \sqrt{0.5} \cdot n \cdot I_{L_k,RMS} & \text{for LV switches} \end{cases} \tag{3.3}$$

### 3.1.2. Loss model of the switches

Now that the switch currents are known, the losses of the switching devices can be determined. These losses can be divided into conduction losses and switching losses. Conduction losses exist only when the switch is actively conducting current, whereas switching losses only occur when the switching device changes state; from ON to OFF or vice versa. These losses can be divided and treated separately. The switching devices that will be used are MOSFETs and the subsequent models will be made considering those type of switches. Furthermore, $S_{1-4}$, as seen in fig. 2.10a, will all be similarly implemented, meaning that the H-bridge is symmetric. The same holds for the LV bridge; when $S_5$ has multiple MOSFETs in parallel, $S_{6-8}$ have the exact same number of parallel MOSFETs of the same type.

**Conduction losses**
For the conduction losses, the RMS value of the switch current has to be used, that is obtained from eq. (3.3). Considering that a number of MOSFETs can be used in parallel to enable current sharing, the conduction loss can be calculated using:

$$P_{con} = I_{sw,RMS}^2 \frac{R_{ds,ON}}{N_{par}}, \tag{3.4}$$

where $R_{ds,ON}$ is the on-state resistance of the MOSFET and $N_{par}$ is the total number of parallel MOSFETs. The consequence of placing multiple switching devices in parallel is that the total equivalent drain-to-source resistance reduces. However, this comes at the cost of additional components, gate drivers and gate losses, as will be shown in the next section.

**Switching losses**
The switching losses are losses that occur during every state transition of the switching devices. The switching losses have to be calculated for both the HV bridge and the LV bridge switches, because of the different origin of the losses. For the HV bridge, low currents with high voltages will be switched, whereas for the LV bridge high currents with a low voltage will be switched. The switching losses that will be derived in this section are the losses that occur in one switch, for example $S_2$ in fig. 2.10a, which can be implemented by multiple parallel connected MOSFETs. To get the total switching losses for the full bridge, the calculated losses have to be multiplied by 4.
For the HV bridge switching losses, there are several contributing factors. First of all, there is the loss due to the charge that is present in the parasitic output capacitance of the MOSFETs when hard switching. When the MOSFET is in the off state, this capacitance is charged, whereas when the MOSFET switches on, this capacitance has to be discharged. During the on transition, this charge gets dissipated in the MOSFET, thereby contributing to the total switching losses.
Then, there are the losses due to the overlap of the voltage and current waveforms when hard switching. An approximation of the energy that is lost can be made by means of [6]:

$$E_{overlap} = \frac{1}{2} V_{ds} I_d \left(t_{on} + t_{off}\right), \tag{3.5}$$

where $V_{ds}$ is the voltage over the MOSFET when switching on, $I_d$ is the current that the MOSFET conducts when switched on, $t_{on}$ is the time it takes to switch to the on state and $t_{off}$ is the time it takes to switch to the off state. The MOSFET turn on and turn off times can either be taken from the datasheet or can be calculated by making use of the method presented in [27]. For this thesis, the latter option has been taken, since the datasheet variables are subject to the operating conditions that the manufacturer used to determine those times. In order to make a fair comparison between different MOSFETs of different manufacturers, the times have been calculated.
Both these losses contribute largely to the total switching losses, but are only present when hard switching occurs. Fortunately, the DAB converter has a ZVS mechanism that is further analyzed and explained in section 4.1. For the loss model, the switching losses will be assumed zero when ZVS is achieved. However, when the operating conditions of the DAB converter prevent ZVS, the hard switching losses consist of the overlap losses and the output capacitance losses. The switching losses can be notated as:

$$P_{sw,HV} = \begin{cases} 0, & \text{if ZVS is obtained} \\ \left(\frac{1}{2} C_{oss,EE} V_{in}^2 \cdot N_{par} + E_{overlap}\right) f_s, & \text{for hard switching,} \end{cases} \tag{3.6}$$

where $C_{oss,EE}$ is the energy equivalent output capacitance of the MOSFET. This output capacitance is used as it represents the equivalent energy stored in the parasitic capacitance [28].
For the LV bridge switching losses, similar hard switching losses occur. However, due to the high current switching of the LV bridge, parasitic inductances start to play a role, even when ZVS is achieved. The reason is that ZVS does not necessarily mean zero current switching (ZCS). The additional energy that is dissipated due to the interruption of the high inductor current in the LV bridge can be approximated by [29]:

$$E_{off,LV} = \frac{1}{2} \frac{L_d + L_s}{N_{par}} I_{sw,LV}^2 \frac{V_{br}}{V_{br} - V_{sw}}, \tag{3.7}$$

where $L_d$ and $L_s$ are the parasitic drain and source inductance of the package of the MOSFET, $V_{br}$ is the drain-source breakdown voltage and $V_{sw}$ is the voltage over the switch, in this case the output voltage of the

converter. With increasing number of parallel switches, the total parasitic inductance decreases. Equation 3.7 does not account for the inductance of the eventual PCB traces, which will also contribute to these losses. For now, it is assumed that the design of the PCB traces is made to reduce parasitic inductances, so that they can be ignored with respect to the lead inductances of the packages of the MOSFETs.
Now, the total switching losses of the LV bridge switch can be summarized as

$$P_{sw,LV} = \begin{cases} E_{off,LV} \cdot f_s, & \text{if ZVS is obtained} \\ \left(\frac{1}{2} C_{oss,EE} V_{out}^2 \cdot N_{par} + E_{off,LV} + E_{overlap}\right) f_s, & \text{for hard switching} \end{cases} \tag{3.8}$$

**Reverse recovery losses**
Since MOSFETs are used to implement the switches, another phenomenon plays a significant role: the reverse recovery losses. Every MOSFET has an intrinsic body diode, which originates from the structure of a MOSFET, being built-up out of p-n junctions. The parasitic diodes are depicted in a schematic representation of the structure of a power MOSFET in fig. 3.2.

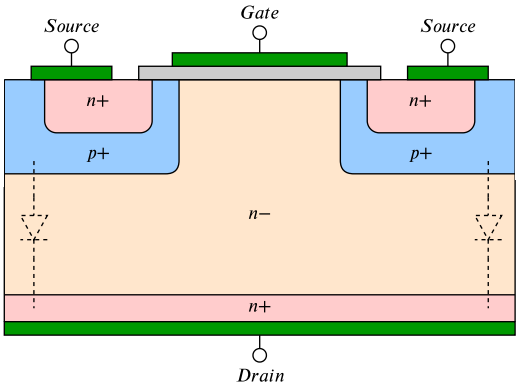



Figure 3.2: Schematic representation of the structure of a power MOSFET. The green areas are the metallizations, used for a low ohmic connection to the silicon structure. The blue area is the highly doped $p+$ region, whereas the highly doped $n+$ region is depicted as the red area. The gray bar underneath the gate metallization is the oxide layer. The light-yellow area is the $n-$ region, which is present in a power MOSFET to withstand a higher breakdown voltage. The parasitic diodes are depicted as dotted lines in the figure, connecting the source to the drain.

Because of these parasitic diodes, the MOSFET is able to conduct current from source to drain, even when the MOSFET is not switched on. This characteristic of the MOSFETs is beneficial for the DAB converter, since a current flow through the body diode prior to turning on allows for ZVS turn-on. However, the downside of this diode is that it introduces reverse recovery losses. Reverse recovery is the inability of a diode to immediately block a reverse current after conduction. When the diode is conducting current and the direction of current changes, the diode needs a finite amount of time before this reverse current flow can be blocked.
When the DAB converter HV bridge loses ZVS, the reverse recovery losses will be added to the HV bridge losses. The reason is that the parasitic diode starts to conduct right before commutation during hard switching. Because of this forced commutation of the diode, reverse recovery losses are introduced. Since these losses can be substantial for silicon (Si) MOSFETs due to their high reverse recovery charge $Q_{rr}$ and large reverse recovery time $t_{rr}$ [7], hard switching should be prevented at all times. The reverse recovery losses can be approximated by

$$P_{rr} = \begin{cases} 0, & \text{if ZVS is obtained} \\ Q_{rr} V_d f_s, & \text{for hard switching,} \end{cases} \tag{3.9}$$

where $Q_{rr}$ is the total reverse recovery charge given by the datasheet of the MOSFET and $V_d$ is the voltage applied to the diode when in blocking state. Usually, the datasheet value of $Q_{rr}$ is given for a certain di/dt that the body diode of the MOSFET is subjected to. However, when the di/dt of the test that the manufacturer did to determine $Q_{rr}$ is low, the peak reverse recovery current $I_{rr}$ will be low too, since a fast changing current leads to an increased $I_{rr}$ [30]. Additionally, a higher di/dt leads to an increased $Q_{rr}$. Therefore, care should be taken when comparing reverse recovery losses among different MOSFETs.

The final part that is added to the total switch losses are the gate driver losses. Every switching instance the gate driver either has to charge or discharge the gate(s) of the MOSFETs that need to change state. The charge that is transported into the gate of the MOSFET to enable conduction is assumed to be fully dissipated by the gate driver when the gate gets discharged again. Furthermore, that charge went through the gate driver itself, which has losses too. The total power that is dissipated by charging and discharging the gates of the MOSFETs can be approximated as

$$P_{gate} = \frac{1}{0.9} \cdot N_{par} \cdot Q_{gate} V_{gs} f_s, \tag{3.10}$$

where the fraction represents an efficiency of 90 % of the gate driver(s), $Q_{gate}$ is the total gate charge of the MOSFET and $V_{gs}$ the drive voltage of the gate. The efficiency of the gate driver losses is an approximation based on available gate drivers. The reason it is incorporated is to provide a reasonable estimation of the losses, such that the minimum search script can make a trade-off between total the number of MOSFETs in parallel (and thus a reduction of conduction losses) and the accompanied additional losses (such as increased gate driver losses).
The total MOSFET losses for the HV full bridge can be summarized as:

$$P_{MOS,HV} = 4 \cdot \left(P_{con} + P_{sw,HV} + P_{rr} + P_{gate}\right) \tag{3.11}$$

and for the LV full bridge as

$$P_{MOS,LV} = 4 \cdot \left(P_{con} + P_{sw,LV} + P_{rr} + P_{gate}\right). \tag{3.12}$$

Obviously, $P_{con}$, $P_{rr}$ and $P_{gate}$ have been calculated with the datasheet variables of the MOSFETs that are used in that bridge. $P_{con}$, $P_{rr}$ and $P_{gate}$ are different for the HV and LV bridge.

### 3.1.3. Loss model of the magnetics

For the realization of the magnetic components, Lightyear has been in contact with a partner to develop a transformer according to the specs of this converter. The reason for that is that the design, simulation and packaging of a high efficiency, production-ready transformer with a tailored leakage inductance is complicated and requires knowledge of finite element method to simulate the behaviour, as has been done in [9]. For the scope of this thesis, the design and simulation of such a transformer is therefore considered to be too much work and is disregarded in this document. Instead, the design has been made by an external company, who concluded that a combination of an external inductor and a transformer would be the best option for the implementation of the magnetics. The reason is that it is generally difficult to tune the leakage inductance of a transformer to a desired accurate value. Therefore, an external inductor with well-defined inductance is connected on the HV side of the transformer, which complements the inaccurate low leakage inductance of the transformer itself.
In order to model the losses of both components, a detailed loss model should be made. However, the external company was only able to provide the maximum losses for the maximum operating conditions. Therefore, standard loss models will be used and curve fitted based on the indication of maximum losses as provided by the production partner. The description of the losses for both the inductor and transformer follow the same structure and largely the same formulae.
Similar to the switch losses, the losses in the magnetics can be split into two parts: the conduction and core losses. The conduction losses, also known as copper losses, originate from the current flowing through the windings. Core losses are the losses that are present due to the changing magnetic flux in the core. Both types of losses will be discussed individually.

#### Conduction losses

The conduction losses consist of the losses inside the windings of the inductor and transformer. As the current changes rapidly over time with the switching frequency, the DC resistance of the copper windings is not the only contributing factor to the total losses. Next to the copper DC resistance, its AC resistance takes up part of the losses too. Depending on the type of wire, such as a solid wire or Litz wire, and the operating frequency, the AC losses can take up a significant part of the conduction losses.
One of the mechanisms that contributes to the AC losses is the skin effect. Skin effect causes the majority of the current to flow at the outer edges of the conductor, thereby increasing the total AC resistance. The inner part of the conductor experiences a much lower current density, which reduces the effective use of the

conductor. Skin effect can be limited by using a collection of small diameter wires. The reason is that for a given frequency a certain skin depth can be calculated, which is the depth below the surface at which the current density has been reduced to only $1/e$, with $e$ being Euler's number. A collection of smaller wires thus reduces the effect of skin effect. The diameter is chosen to be smaller than the skin depth, resulting in a good conductor utilization. Skin effect plays a role for higher frequencies, such as the 100 kHz of this converter.

To evaluate the AC losses, the method described by [31] has been used. First, the AC-to-DC resistance of the selected Litz wire has to be calculated, using the approximation

$$\frac{R_{AC}}{R_{DC}} = H + K\left(\frac{N d_i}{d_o}\right)^2 G, \tag{3.13}$$

where $R_{AC}$ is the AC resistance of the equipped Litz wire, $R_{DC}$ is the DC resistance of the Litz wire, $H$ is the resistance ratio of one strand of the Litz bundle, $K$ is a constant that depends on the number of strands in the bundle, $N$ is the number of strands, $d_i$ is the diameter of the individual strands in inches, $d_o$ is the outer diameter of the total cable in inches (including isolation etc.) and finally, $G$ is the eddy current basis factor, which is expressed as

$$G = \left(\frac{d_i\sqrt{f_s}}{10.44}\right)^4. \tag{3.14}$$

From eq. (3.13) it can be concluded that the AC resistance of the windings of the inductor, which are Litz wires, depends on many factors. Especially the diameter of the individual strands has a large influence on the resistance, as well as on the fill factor of the inductor windings.
With the use of tables provided by the manufacturer of Litz wires, the total AC resistance can be computed. The parameters of the chosen Litz wire are inserted in eq. (3.13) and eq. (3.14), from which the AC-to-DC resistance ratio is calculated. Since the DC resistance of the Litz wire is given for a specific cable, the AC resistance can be computed using the AC-to-DC resistance ratio. Now, the total conduction losses can be computed in a similar way as the conduction losses of the MOSFETs. Using the formula for RMS current given by eq. (A.9), the inductor conduction losses can be expressed as

$$P_{L,con} = I_{L,RMS}^2 R_{DC} + \frac{I_{pp}^2}{12} R_{AC}. \tag{3.15}$$

For the transformer primary and secondary winding losses eq. (3.15) can be adjusted using the transformer currents and their respective winding resistances.

**Core losses**
For an approximation of the core losses, the Steinmetz equation as introduced by [32] has been used. The Steinmetz equation is used as a first estimate of the losses of the core of the magnetic components. However, the Steinmetz equation is derived for the use of sinusoidal waveforms in a core, whereas the waveforms of the DAB converter are primarily non-sinusoidal. Non-sinusoidal waveforms as well as DC biases can result in significantly higher core losses [33]. Even though the Steinmetz equation is based on sinusoidal waveforms, it is considered to be a good first estimation. Considering the fact that the current waveforms through the inductor and transformer approach sinusoidal shapes (as can be seen in fig. 3.1a and fig. 3.1b) and that the DC blocking capacitor that is implemented will prevent a DC bias of the transformer, the mismatch in losses is expected to be minimal.
The core losses are approximated by the Steinmetz equation for ferrite core losses, which is given by [32] as:

$$\overline{P}_{core} \approx V_{core} k f_s^{\alpha} B_{peak}^{\beta}, \tag{3.16}$$

where $\overline{P}_{core}$ is the average core loss, $V_{core}$ the total volume of the core, $B_{peak}$ the peak flux density and $k$, $\alpha$ and $\beta$ are the Steinmetz coefficients that are dependent on the core material, as given in their corresponding data sheets.

Now that the conduction losses and the core losses can be computed, the total inductor losses are estimated by

$$P_{ind} = P_{L,con} + \overline{P}_{core}. \tag{3.17}$$

In a similar way, the transformer losses can be summed up, consisting of the core losses and the conduction losses in both windings.

### 3.1.4. Loss model of the DC blocking capacitor

For the DC-blocking capacitor, a simple loss model applies that will take the equivalent series resistance (ESR) of the capacitor and use that to calculate the conduction losses. This has been implemented in the script as:

$$P_{DCcap} = I_{L,RMS}^2 R_{C_{ESR}}. \tag{3.18}$$

## 3.2. Minimum search script

The most essential part of the converter to ensure high efficiency is to make a good selection of components. Therefore, first the component selection is discussed in section 3.2.1, whereafter the implementation of the minimum search script is discussed in section 3.2.2.

### 3.2.1. Component selection

From the loss models discussed in section 3.1 and operation principle of the DAB converter explained in section 2.2.2 a selection of possible components can be made. Per component the selection criteria and resulting overview of components will be discussed individually.

**MOSFET selection**

For the MOSFET selection, the selection criteria are summarized in table 3.1. A criterion that is not listed is that the MOSFETs should preferably be rated according to AEC-Q101, which is the stress test qualification made by the Automotive Electronics Council for discrete semiconductors for automotive applications [34]. Second, the minimum breakdown voltage of the HV MOSFET has to be at least 140 % of the maximum operating voltage in the circuit, as a safety margin. The additional 40 % is incorporated to prevent the MOSFETs from failures when sudden voltage spikes or transient situations induce higher voltages. Due to the high current inductive switching on the LV side, the 40 % margin is not sufficient. Calculations indicate a maximum LV peak current of 150 A. A typical drain-source fall time of a 100 V MOSFET is 40 ns, which results in a frequency of 12.5 MHz (two times 40 ns). Then, the package with largest parasitic inductance of [35] is taken, which is the D2PAK with a parasitic inductance of 4.8 nH above 5 MHz. Adding an estimated 5 nH of PCB trace inductance results in a total inductance of 9.8 nH. Using eq. (2.1) with a dt of 40 ns, results in a total inductive voltage of 36.8 V. This leads to a total voltage of 36.8 + 57.4 = 94.2 V, which means that MOSFETs with a minimal $V_{ds}$ of 100 V are required. Last, the switches should be able to continuously withstand the worst case RMS current, which is calculated by using the methodology of section 3.1.1.

Table 3.1: The selection criteria for the HV and LV bridge MOSFETs.

| | **HV bridge** | **LV bridge** |
|---|---|---|
| Technology | SiC/Si | Si |
| Max. operating voltage [$V$] | 437 | 57.4 |
| Min. breakdown voltage [$V$] | 610 | 100 |
| Max. RMS current [$A_{RMS}$] | 9.6 | 58 |
| Max. peak current [$A$] | 25 | 150 |

Based on these criteria a selection of MOSFETs has been made. A variety of MOSFETs were selected, one with the lowest $R_{ds,ON}$, one with the lowest gate charge $Q_g$ and one with the lowest output capacitance $C_{oss}$. Additionally, alternative MOSFETs were selected that have characteristics in between the previously mentioned ones. A correction is applied to the reverse recovery losses if the testing conditions are significantly different for one of the MOSFETs, to provide a fair comparison. The numbers are scaled to represent the reverse recovery losses at a di/dt of 1000 A/µs. An overview of the selected HV MOSFETs is given in table 3.2 and the selected LV MOSFETs are listed in table 3.3.

The list of candidates also contains automotive rated (AEC-Q101) MOSFETs, indicated with an asterisk. Based on the results of the minimum search script, a comparison between a fully automotive rated system and non-automotive rated system is made, in order to understand what the cost in efficiency is. Automotive rated components have higher failure and safety standards than normal components, which often results in slightly

Table 3.2: The selected MOSFETs for the HV bridge.

| MPN | $R_{ds,ON,max}$ | $Q_g$ | $V_{gs,max}$ | $V_{dss}$ | $C_{oss}$ | $Q_{rr,corrected}$ |
|---|---|---|---|---|---|---|
| SCTH90N65G2V-7 | **24 mΩ** | 157 nC | 22 V | 650 V | 294 pF | 154 nC |
| SCT3060ALHR* | 86 mΩ | 58 nC | 22 V | 650 V | **55 pF** | 186 nC |
| NVBG020N090SC1* | 28 mΩ | 200 nC | 19 V | 900 V | 295 pF | 186 nC |
| UJ3C065030B3 | 43 mΩ | 51 nC | 25 V | 650 V | 320 pF | 400 nC |
| SCTH35N65G2V-7AG* | 67 mΩ | 73 nC | 22 V | 650 V | 125 pF | **85 nC** |
| UF3SC065030D8S | 55 mΩ | **43 nC** | 25 V | 650 V | 320 pF | 242 nC |
| SCTH100N65G2-7AG* | 32 mΩ | 162 nC | 22 V | 650 V | 267 pF | 296 nC |

Table 3.3: The selected MOSFETs for the LV bridge.

| MPN | $R_{ds,ON,max}$ | $Q_g$ | $L_{leads}$ | $V_{dss}$ | $C_{oss}$ | $Q_{rr,corrected}$ |
|---|---|---|---|---|---|---|
| IPB017N10N5LFATMA1 | **1.7 mΩ** | 195 nC | 5.2 nH | 100 V | 2500 pF | 452 nC |
| IAUT300N10S5N015ATMA1* | 2 mΩ | 216 nC | 2 nH | 100 V | 2496 pF | 880 nC |
| IPT015N10N5 | 2 mΩ | 211 nC | 2 nH | 100 V | 2300 pF | 2528 nC |
| IPB017N10N5ATMA1 | 2 mΩ | 210 nC | 5.2 nH | 100 V | 2353 pF | 1880 nC |
| IAUT260N10S5N019* | 2.5 mΩ | 166 nC | 2 nH | 100 V | 1900 pF | 720 nC |
| IPB025N10N3G | 2.5 mΩ | 206 nC | 5.2 nH | 100 V | 2580 pF | 928 nC |
| IPT020N10N3ATMA1 | 2 mΩ | 207 nC | 2 nH | 100 V | 2673 pF | 928 nC |
| IPB027N10N3G | 2.7 mΩ | 206 nC | 2.8 nH | 100 V | 2580 pF | 928 nC |
| STH310N10F7-6 | 2.3 mΩ | 180 nC | 5.2 nH | 100 V | 3500 pF | 800 nC |
| FDMS86180 | 5.4 mΩ | **84 nC** | 2 nH | 100 V | 3730 pF | 269 nC |
| CSD19536KTT | 2.4 mΩ | 153 nC | 5.2 nH | 100 V | 2370 pF | 712 nC |
| STH310N10F7-2 | 2.3 mΩ | 180 nC | 5.2 nH | 100 V | 3500 pF | 800 nC |
| STH240N10F7-2 | 2.5 mΩ | 160 nC | 5.2 nH | 100 V | 2950 pF | 1260 nC |
| SUM70030E-GE3 | 2.88 mΩ | 214 nC | 2.8 nH | 100 V | **820 pF** | 960 nC |
| AUIRF7669L2TR* | 4.4 mΩ | 120 nC | **0.7 nH** | 100 V | 1140 pF | 840 nC |
| IPB180N10S402ATMA1* | 2.5 mΩ | 200 nC | 2.5 nH | 100 V | 4760 pF | **230 nC** |

decreased performance, as can be seen from table 3.2. The SCTH90N65G2V-7 and the SCTH100N65G2-7AG are the same model MOSFETs, however the SCTH100 is adjusted to comply with the AEC-Q101 rating, leading to higher drain-source resistance and reverse recovery losses.

**Inductor designs**

For the series inductor, three designs have been made according to the design strategy that is explained in Appendix B. In this way the design of the partner of Lightyear was compared to alternative designs, equipped with different core sizes and number of turns. The designs and their specifications are summarized in table 3.4.

Table 3.4: The specifications for the three designed series inductors.

| Core size | Number of turns n | Air gap length $l_g$ | Core volume $V_e$ | Average turn length $l_{turn}$ | Operating point $B_{max}$ |
|---|---|---|---|---|---|
| ETD39-3F3 | 24 | 3.6 mm | 11500 $mm^3$ | 69 mm | 250 mT |
| ETD44-3F3 | 18 | 2.8 mm | 17800 $mm^3$ | 77 mm | |
| ETD49-3F3 | 15 | 2.4 mm | 24000 $mm^3$ | 85 mm | |

As a first observation it can be seen that for larger core sizes the required number of turns decreases. It can be expected that for a lower number of turns the copper losses will decrease, even though the total average turn length increases with volume. However, a larger core size almost always leads to more core losses, as is shown by eq. (3.16). Thus, a trade-off between a low number of turns and a small core will most likely result in the optimal inductor design with respect to efficiency, if the core and copper losses are comparable.

**Parallel diode selection**
As can be seen from the reverse recovery charges of table 3.2 and table 3.3 when evaluated using eq. (3.9), the reverse recovery losses can play a significant role in the total converter losses. Next to the reverse recovery losses, the internal body diodes of the MOSFETs have a significant forward voltage drop, which can be as high as 4.5 V (SCTH35N65G2V-7AG) for the HV switches and 1.5 V (STH310N10F7-2) for the LV switches. Especially on the LV side, the high currents flowing through the body diodes in combination with the forward voltage drop, will again lead to an increase of losses. To reduce these losses, the minimum search script is extended with an option to add parallel diodes. Especially Schottky barrier diodes and SiC diodes are of interest, due to their low or non-existing reverse recovery losses. The selection of HV diodes are listed in table 3.5 and for the LV bridge in table 3.6.

Table 3.5: The selected diodes for the HV bridge.

| MPN | Forward voltage | $V_{reverse}$ | $Q_{rr}$ | $C_{junction}$ |
|---|---|---|---|---|
| LSIC2SD065D06A | 1.85 V | 650 V | 0 C | 30 pF |
| FFSB1065B-F085 | 2.4 V | 650 V | 0 C | 35 pF |
| STPSC20065-Y | 1.65 V | 650 V | 0 C | 100 pF |

Table 3.6: The selected diodes for the LV bridge.

| MPN | Forward voltage | $V_{reverse}$ | $Q_{rr}$ | $C_{junction}$ |
|---|---|---|---|---|
| 123SPC100A | 0.87 V | 100 V | 0 C | 950 pF |
| APT30SCD120S | 2.1 V | 100 V | 135 nC | 130 pF |
| FFSB3065B-F085 | 2.4 V | 100 V | 0 C | 300 pF |

**DC blocking capacitor selection**
The choice for the best DC blocking capacitors has been made a posteriori, since it depends on the optimal value of the leakage inductance. Once this was known to be 25 $\mu$H, as will be shown in table 3.7, the total capacitance could be selected.
The goal is to have the resonance frequency of the LC circuit, consisting of the DC-blocking capacitor and leakage inductance, to be at maximum 20 % of the switching frequency. In practice, 10 % of the switching frequency is a good design goal. If the resonance frequency would be higher, it would have an impact on the steady state operation of the converter, since it can influence the voltages and currents within one switching cycle.
So, the minimum capacitance that is needed can be found by using:

$$C_{DC,min} = \frac{1}{L_k \left(2\pi f_0\right)^2}, \tag{3.19}$$

where $f_0$ is the target resonance frequency of the LC network. A leakage inductance of 25 $\mu$H and a resonance frequency of 10 kHz results in a capacitance of 10 $\mu$F. To determine what capacitors are suited, the voltage rating should be known. As an estimation of the maximum voltage that can be expected, the following formula can be used:

$$V_{C,max} = k \cdot \sqrt{2} \frac{I_{L,RMS}}{2\pi f_s C_{DC}}, \tag{3.20}$$

where $k$ is a safety factor, which is chosen to be 2 here. For the inductor RMS current a worst case simulation is done in LTSpice, which is for $V_{HV}$ = 437 V and $V_{LV}$ = 42 V. The simulated maximum $I_{L,RMS}$ of 12.5 $A_{RMS}$, with an additional 40 % of margin, leads to a current capability requirement of 17.5 $A_{RMS}$. Filling in eq. (3.20) gives a voltage amplitude of 7.9 V.
The final selection for the DC capacitors is a process of finding available capacitors and checking the current ratings for them. This is not of interest for this thesis, and thus the final design is given, which is an implementation of 3x R60DF4330506AK added in parallel. These 3.3 $\mu$F film capacitors have a voltage rating of 40 Vac and 63 Vdc, which is more than sufficient. The reason to use 3 parallel capacitors is to stay within the current capabilities of the capacitors, which are fairly low at 100 kHz.
Finally, the same worst case simulation has been run with the designed capacitors in place. The results are shown in fig. 3.3.

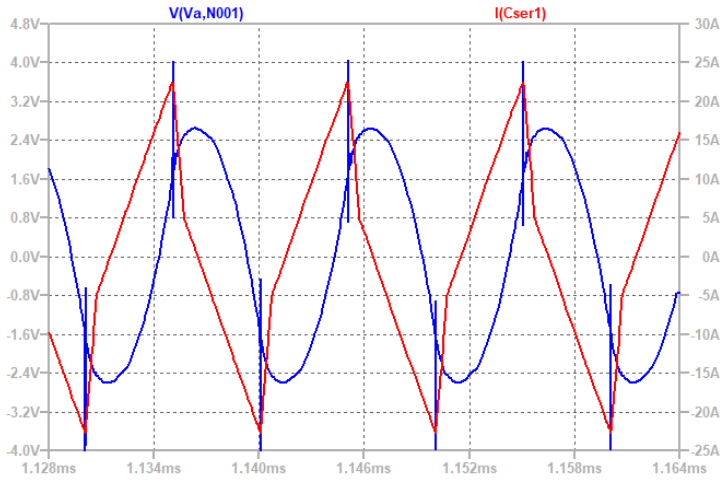



Figure 3.3: LTspice simulation waveforms of the series DC blocking capacitor in steady state for $V_{HV}$ = 437 V and $V_{LV}$ = 42 V with $P_{LV}$ = 2500 W. The blue trace is the capacitor voltage and the red trace is the (total) capacitor current.

It can be seen that from this worst case scenario the capacitor voltage reaches peaks of 4 V, with an amplitude of 2.6 V. The peaks are induced from switching of the HV bridge. With the capacitor in place, any DC bias current is removed from the transformer. From the simulation the capacitor RMS current is 12.5 $A_{RMS}$. Re-calculating the expected voltage amplitude using eq. (3.20) with safety factor $k$ = 1, $I_{L,RMS}$ = 12.5 $A_{RMS}$ gives an amplitude of 2.8 V, verifying the equation with the simulations.

### 3.2.2. Implementation of the minimum search script

The minimum search script will run through all possible combinations of the converter design, given its inputs. Then, the average efficiency over all operating points of each design is compared to the maximum obtained average efficiency so far. By doing so, the outcome of the script is the optimal DAB converter design for SPS modulation with respect to efficiency. The operating conditions are defined by the HV and LV bus voltage range, at a constant power level. The HV bus swing for the 90 % operating region is from 312 V to 416 V, and the LV bus swing is from 42 V to 57.4 V. The transferred power level is kept constant at ± 2.5 kW.
The input parameters from which the script runs all combinations will be discussed individually. The minimum and maximum values will be given over which a sweep will be executed. The step size between the two limits is made variable and is adjusted, if necessary, based on the outcome of the script. When the script gives a certain optimal converter design, the limits of all parameters will be narrowed down and the step size is decreased, until the script converges to a single optimal design.

**Transformer turn ratio $n$**

The transformer turn ratio has a large impact on the total converter operation, because it changes the voltage transfer ratio $M$, which has a direct influence on the ZVS region. The range for the transformer turn ratio is from $n = 5$ to $n = 7$. These limits are determined by calculating the minimum and maximum voltage transfer ratio for each $n$. When the range of $n$ would be increased further, $M$ will not reach unity for any operating point, which means that the converter design is not able to achieve ZVS over a large range of operating points.

**Leakage inductance $L_k$**

The leakage inductance has a range from $L_k$ = 5 $\mu$H up to $L_k$ = 27.3 $\mu$H. The upper boundary is determined by calculating the maximum possible leakage inductance while still being able to transfer 2.5 kW. It is derived in Appendix A.2 and given as:

$$L_k \leq \frac{\min(V_{HV})\min(nV_{LV})}{8 f_s P_{max}}. \tag{3.21}$$

Filling in the converter specifications with $V_{HV}$ = 260 V, $V_{LV}$ = 42 V and $n$ = 5 leads to a maximum allowable $L_k$ of 27.3 $\mu$H. The lower boundary of $L_k$ is set at 5 $\mu$H and not lower, since a very low $L_k$ reduces the ZVS region of the DAB considerably [21].

**MOSFETs, inductor designs and diodes**
From the list of selected MOSFETs, inductors and diodes, the script takes one and runs all the iterations needed to make all possible combinations. When a design is found that is more efficient than the previous most efficient design, the used MOSFET, inductor and diode are stored. At the end, the optimal MOSFET, inductor and diode can be given as an output of the minimum search script. For the diodes, there is an additional option to not include a diode at all and use the body diodes of the MOSFETs instead.

**Number of parallel switches**
For both full bridges, it is possible to implement the switches with multiple parallel MOSFETs. In the minimum search script a distinction is made for the number of parallel switches per bridge, meaning that the LV bridge can have a different number of parallel MOSFETs than the HV bridge.

## 3.3. Minimum loss design

Using the described set-up and the designed and selected components from section 3.2, the minimum search script has been implemented. The script runs in MATLAB, making it convenient to display loss maps and do performance analyses. The most important output of the script is the optimal efficiency design of the converter power stage. The results for the 90 % operating region are summarized in table 3.7.

Table 3.7: Outcome of the minimum search script for SPS modulation over the 90 % operating region.

| Item | Value |
|---|---|
| Average efficiency $\eta_{avg}$ | 98.67 % |
| Peak efficiency $\eta_{pk}$ | 99.14 % |
| Transformer turn ratio $n$ | 6 |
| Leakage inductance $L_k$ | 25 $\mu$H |
| HV MOSFET | UJ3C065030B3 |
| Number of parallel HV MOSFETs $N_{par,HV}$ | 2 |
| LV MOSFET | CSD19536KTT |
| Number of parallel LV MOSFETs $N_{par,LV}$ | 3 |
| Most efficient inductor design | ETD39-3F3 |
| Parallel diode on HV side | LSIC2SD065D06A |
| Parallel diode on LV side | 123SPC100A |

As can be seen from the results, the average power stage efficiency is 98.67 %, with a maximum efficiency of 99.14 %. All the efficiencies at the operating points have been saved and are visually presented by means of a contour plot. The maximum efficiency is obtained for an input voltage of 378.8 V and an output voltage of 57.4 V, as can be seen from fig. 3.4.

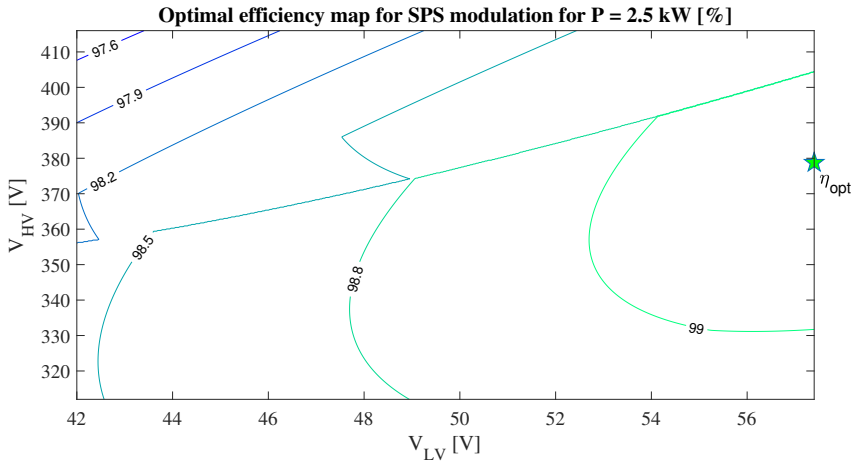



Figure 3.4: Contour plot showing the DAB power stage efficiency for the 90 % operating region with SPS modulation at a power of $P$ = 2.5 kW. The peak efficiency is depicted with a green star, which reaches 99.14 % for $V_{HV}$ = 378.8 V and $V_{LV}$ = 57.4 V.

The script is run again for a power of $P = -2.5$ kW, which results in the graph as seen in fig. 3.5

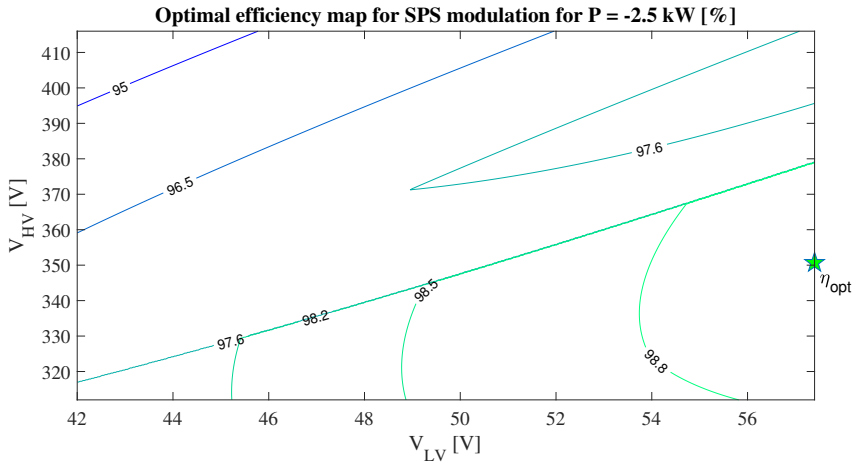



Figure 3.5: Contour plot showing the DAB power stage efficiency for the 90 % operating region with SPS modulation at a power of $P = -2.5$ kW. The peak efficiency is depicted with a green star, which reaches 98.96 % for $V_{HV} = 350.7$ V and $V_{LV} = 57.4$ V.

As expected, the total converter efficiency is generally highest for high voltages, since that results in lower currents and thus lower conduction losses. Additionally, the expectation that conduction losses will dominate is confirmed by the high number of parallel MOSFETs for the LV bridge. Per switch, 3 MOSFETs are equipped in order to reduce the conduction losses. However, for high LV bus voltages and low HV bus voltages there is a large dip in efficiency. Similarly, there is a visible line that divides the efficiency map in two. This has to do with one of the bridges losing ZVS, which will be elaborated on in section 3.3.2.

### 3.3.1. Sensitivity analysis

With the optimal efficiency in place, now a trade-off between efficiency, component count and reliability (AEC-Q101 rating or not) can be made which is shown in table 3.8. For this analysis, the number of parallel MOSFETs was fixed for each run leading to the average efficiencies for those specific MOSFETs and number of parallel MOSFETs. The results are only shown for the positive power transfer ($P = 2.5$ kW).

Table 3.8: Effect of the number of parallel MOSFETs on the total converter efficiency.

| NparHV | NparLV | HV MOSFET | LV MOSFET | $\eta_{avg,90\%region}$ | $\eta_{avg,100\%region}$ |
|---|---|---|---|---|---|
| **1** | 1 | **SCTH90N65G2V-7** | **IPT020N10N3ATMA1** | 98.29 % | 98.09 % |
| | **2** | | | **98.51 %** | **98.37 %** |
| | 3 | | CSD19536KTT | 98.56 % | 98.41 % |
| 2 | 1 | UJ3C065030B3 | IPT020N10N3ATMA1 | 98.36 % | 98.16 % |
| | 2 | | | 98.58 % | 98.44 % |
| | 3 | | CSD19536KTT | 98.67 % | 98.49 % |

It can be seen that the difference between 1 or 2 parallel HV MOSFETs is limited, on average only 0.07 % (for the 90 % operation region). The difference for LV MOSFETs is larger though, with the difference between 1 or 2 parallel MOSFETs being 0.22 % on average. Between 2 and 3 parallel LV MOSFETs the difference is 0.05 % on average, which also includes a change in MOSFET. From this sensitivity analysis the decision is made to go on with 1 parallel HV MOSFET and 2 parallel LV MOSFETs, resulting in an average total efficiency of 98.51 % for the 90 % operation region. The selection is made bold as can be seen in table 3.8.
The selected switches are non-automotive MOSFETs. The SCTH90N65G2V-7 actually has an automotive rated version, which is the SCTH100N65G2-7AG. The higher reliability because of the AEC rating, makes it attractive to implement in the DAB converter. The same holds for the LV bridge, where the best automotive rated alternative would be the IAUT300N10S5N015ATMA1. The best candidate is the non-automotive rated IPT020N10N3ATMA1, but the additional reliability of an AEC rated MOSFET might make the small decrease in efficiency worth it. A comparison of the above is shown in table 3.9, where the best performing automotive rated MOSFETs are used in different combinations. The same has been done for a negative power flow, however, only the positive power flow results are shown here.

Table 3.9: Effect of an automotive rated MOSFET on the total converter efficiency.

| HV MOSFET | NparHV | LV MOSFET | NparLV | $\eta_{avg,90\%region}$ | $\eta_{avg,100\%region}$ |
|---|---|---|---|---|---|
| SCTH90N65G2V-7 | 1 | IPT020N10N3 | 2 | 98.50 % | 98.37 % |
| SCTH100N65G2-7AG | 1 | | 2 | 98.42 % | 98.30 % |
| SCTH90N65G2V-7 | 1 | **IAUT300N10S5N015** | 2 | 98.49 % | 98.36 % |
| **SCTH100N65G2-7AG** | **1** | | **2** | **98.41 %** | **98.30 %** |

As can be seen from table 3.9, the effect of selecting automotive rated MOSFETs is very limited on the total converter efficiency. The biggest difference can be seen when the HV MOSFET is swapped to the SCTH100N65G2-7AG, which still is only 0.08 % on the 90 % operating region. The final conclusion is to go for both the automotive rated switches on the HV and the LV side, which has been made bold in table 3.9. The gain in reliability outweighs the loss in efficiency in this case. The resulting efficiency plot over the 90 % operating range after these sensitivity analyses can be seen in fig. 3.6 for a positive power transfer and in fig. 3.7 for a negative power transfer.

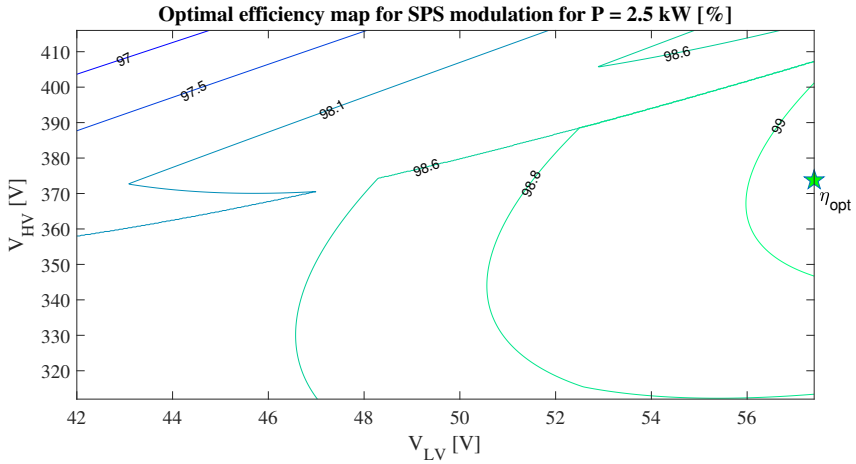



Figure 3.6: Contour plot showing the DAB power stage efficiency for the 90 % operating region for the design after trade-offs at a power of $P = 2.5$ kW. The peak efficiency is depicted with a green star, which reaches 99.14 % for $V_{HV} = 371.7$ V and $V_{LV} = 57.4$ V.

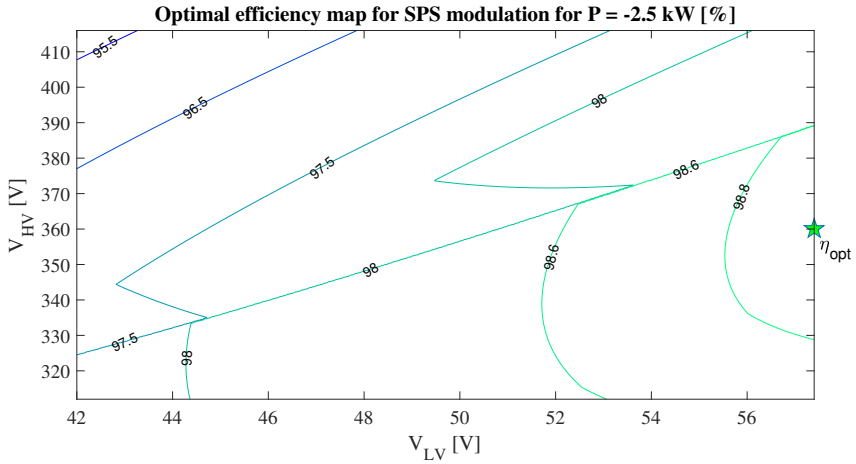



Figure 3.7: Contour plot showing the DAB power stage efficiency for the 90 % operating region for the design after trade-offs at a power of $P = -2.5$ kW. The peak efficiency is depicted with a green star, which reaches 99.14 % for $V_{HV} = 360$ V and $V_{LV} = 57.4$ V.

### 3.3.2. MOSFET losses

For the switch losses, a contour plot has been made as well, similar to the graph that was shown in fig. 3.4, but now for losses instead of efficiency. This has been done separately for both the HV bridge and the LV bridge, as can be seen in fig. 3.8a and fig. 3.8b, respectively.

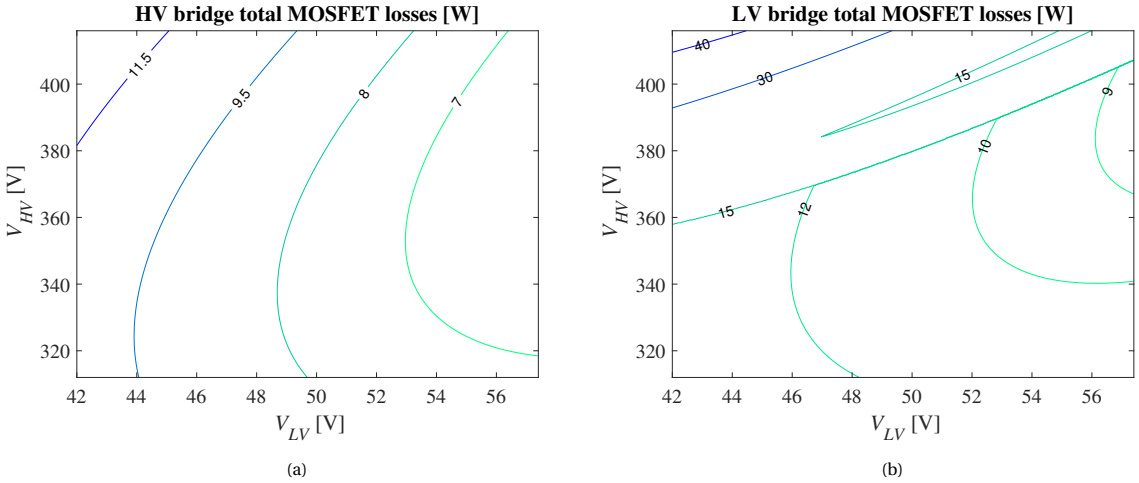



Figure 3.8: MOSFET losses for the optimal DAB converter design according to table 3.7 at an output power of $P_{LV} = 2.5$ kW. (a) shows the total HV bridge losses and (b) the total LV bridge losses.

As can be seen from fig. 3.8a, the HV switch losses remain fairly constant but change with increasing currents (when the voltages get lower). For the LV bridge switch losses though, there is a considerably increase in losses above a certain line. This is the boundary of ZVS for the lagging LV bridge, where the bridge goes into hard switching for operating points above the line, as can be seen in fig. 3.9.

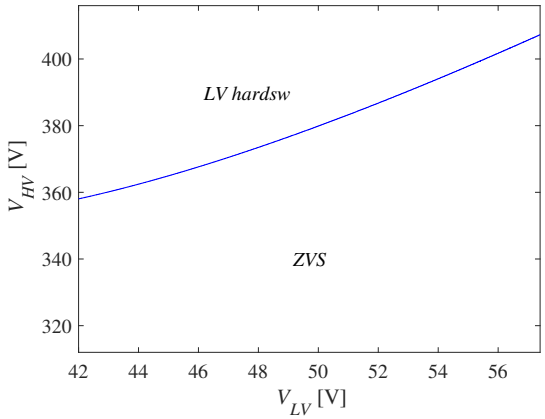



Figure 3.9: Hard switching region, depicted as LVhardsw, of the LV full bridge at a power of $P = 2.5$ kW.

For the LV bridge, depicted in fig. 3.8b, the overall losses are higher than for the HV bridge. This is as expected, since the LV switches need to handle high currents. These high inductive currents are the reason that the total losses increase when the voltage transfer ratio $M$ differs from unity. This can be seen in the bottom right region of fig. 3.8b, where the losses increase again, while there is no hard switching of the LV bridge. The hard switching of the LV full bridge occurs in the top left region, which is where $V_{HV}$ is high, as can be seen in fig. 3.9. Here, only an analysis has been shown for a positive power transfer. It was found that for a negative power transfer, again the lagging bridge experiences hard switching, in that case the HV bridge. For both bridges this hard switching introduces additional losses.

### 3.3.3. Magnetics losses

For the inductor a similar loss plot can be made as has been done for the switches. The inductor losses consist of the core losses and the conduction losses. The loss map is shown in fig. 3.10.

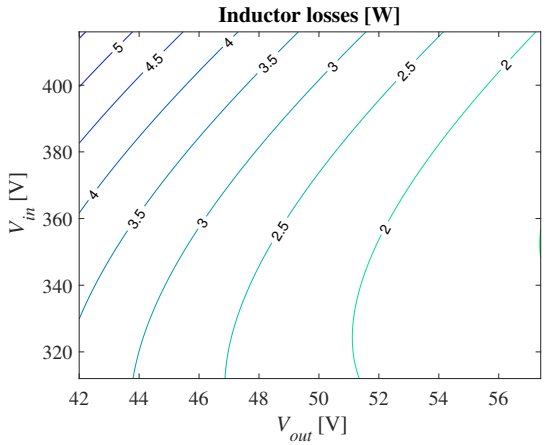



Figure 3.10: Inductor losses for the optimal DAB converter design at an output power of $P_{LV} = 2.5$ kW.

As can be noticed from the inductor loss map, there are very limited losses for most operating points. Only when the voltage transfer ratio $M$ significantly differs from unity, then the inductor losses start to increase. This is due to the large peak currents that result from a varying $M$, which induces high peak flux densities that negatively influence the total core losses, as shown by eq. (3.16).
The transformer losses are larger as compared to the inductor losses, as is shown in fig. 3.11a. Next to that, the RMS current through the transformer, and thus through the inductor too, has been plotted, as can be seen in fig. 3.11b.

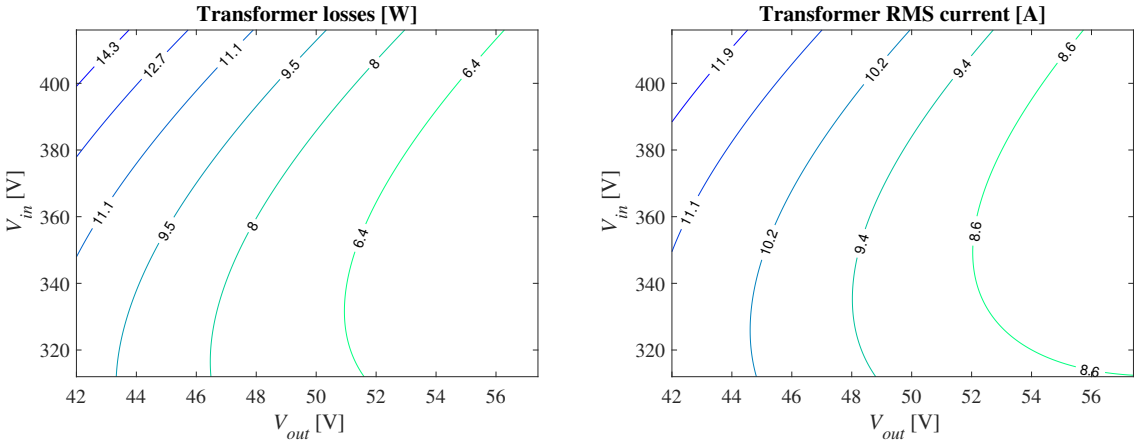



Figure 3.11: (a) Transformer losses for the optimal DAB converter design according to table 3.7 at a power of $P_{LV} = 2.5$ kW and (b) the RMS current through the transformer for different operating points.

## 3.4. Conclusion

In this chapter a minimum search script has been developed based on loss models for the converter components. Using these models, an initial selection of switches and inductors has been made. By using the minimum search script and an elaborate trade-off analysis afterwards, an optimal converter design was presented with an average efficiency of 98.41 % over the 90 % operating range for $P = 2.5$ kW. For $P = -2.5$ kW the average efficiency was 97.87 %. To further improve on the presented results, a more profound understanding of the DAB zero voltage transitioning is needed, after which an improved modulation scheme can be implemented to further decrease the conduction losses of the DAB converter.

# 4

# DAB Converter Modulation

Now that it was shown that the DAB converter experiences additional losses for the wide HV and LV bus voltage ranges, the operation principle and modulation strategy of the DAB has to be investigated further. The origin of the ZVS capability of the DAB and the current flow during transitioning will be analyzed in section 4.1. Then, alternative modulation schemes are shown in section 4.2. After that, an optimal combination of modulation schemes will be discussed in order to improve total converter efficiency, which will be done in section 4.3. Using this optimal combination, a new version of the minimum search script of section 3.2 is discussed right after in section 4.4, where the new component choices are shown. Finally, the resulting plots and loss maps will be discussed in section 4.5.

## 4.1. ZVS transition

Before the operation principle of the modulation methods can be analyzed in detail, the zero voltage transitioning of the DAB needs to be investigated. The primary reason that SPS modulation is not efficient over the whole operating range of the converter is because of hard switching. Soft switching capabilities will be lost when the voltage transfer ratio, as defined by eq. (2.12), significantly differs from the transformer turn ratio $n$, as was shown in fig. 2.13. To analyze what happens in the period shortly before switching, a closer look at the currents in switching region I and region II will be given. The voltage waveforms and inductor current for SPS modulation have been depicted once again in fig. 4.1 together with the instantaneous HV bus input power. Here, only the positive power direction will be described, for the reverse power transfer direction the exact same steps apply.

From the figure it can be seen that for region I the voltage $v_{ab}(t)$ is equal to $V_{HV}$ and the voltage $v_{pq}(t)$ is $-nV_{LV}$, in accordance with eq. (2.4) and eq. (2.5). During period I the inductor current changes sign, meaning that a reversal of the current direction is achieved. After $t_1$, the current is positive and the voltages $v_{ab}(t)$ and $v_{pq}(t)$ are $V_{HV}$ and $nV_{LV}$, respectively.

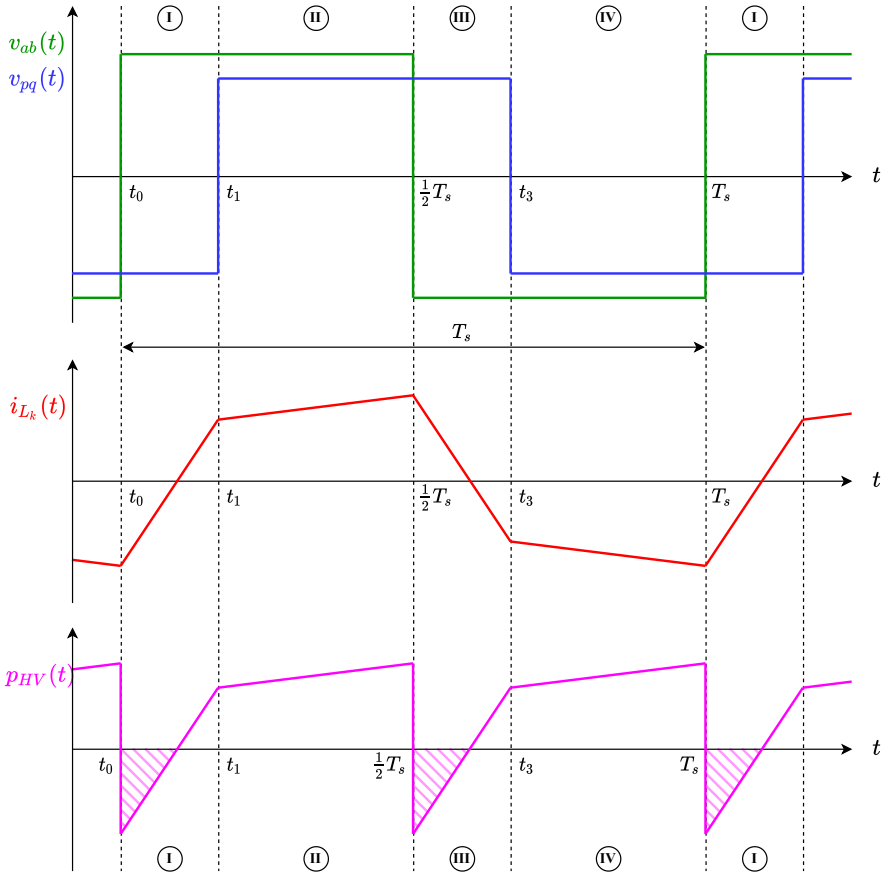



Figure 4.1: Region definition of the waveforms of the simplified DAB converter using SPS modulation, including converter power as supplied by the HV bus.

Based on this descriptive analysis, the current flow of the DAB converter can be derived. The current flow for region I and region II can be seen in fig. 4.2a and fig. 4.2b.
It can be seen that during period I, switch pair $S_1$ and $S_4$ as well as pair $S_6$ and $S_7$ are conducting current. The diodes parallel to the switches model the intrinsic body diode of the MOSFETs, meaning that current sharing between the transistor and its parasitic diode occurs if the current direction is correct. Additionally, the switches in the figures do not represent one single switching device, such as one MOSFET. The switches can be implemented by using multiple devices in parallel.

For period II, the switch pair $S_6$ and $S_7$ are turned off and switch pair $S_5$ and $S_8$ are activated, as can be seen in fig. 4.3.
In between switching period I and II, the resonant transition of the DAB takes place. Before the ZVS transition itself is explained, it should be mentioned that between the switching periods a dead time has to be incorporated. Since the real DAB converter does not consist of ideal switches with an infinite response time, dead time is needed. Real switches like MOSFETs have a finite turn-on and turn-off time. When there is no blank time between two switching periods, during which none of the switches receive a gate voltage, the possibility of shorting a leg arises. Dead time prevents overlapping of the turn-on of the lower leg switch and turn-off of the upper leg switch and vice versa. Without dead time, both switches will be on at the same time, effectively shorting the DC bus. Without proper control, massive current spikes can be the result, leading to damage of all components without proper protection. To prevent this from happening, dead time is introduced. The ZVS transitioning that is explained in this section will assume a proper dead time control. In fact, the ability of the DAB converter to have ZVS comes from the current flows during this dead time.

During the transition period the remaining energy in the leakage inductance $L_k$ ensures that the parasitic capacitances of the switches that will turn on are discharged, and the parasitic capacitances of the switches that are turned off get charged. As an example, the LV bridge is considered here. The resonance takes place during

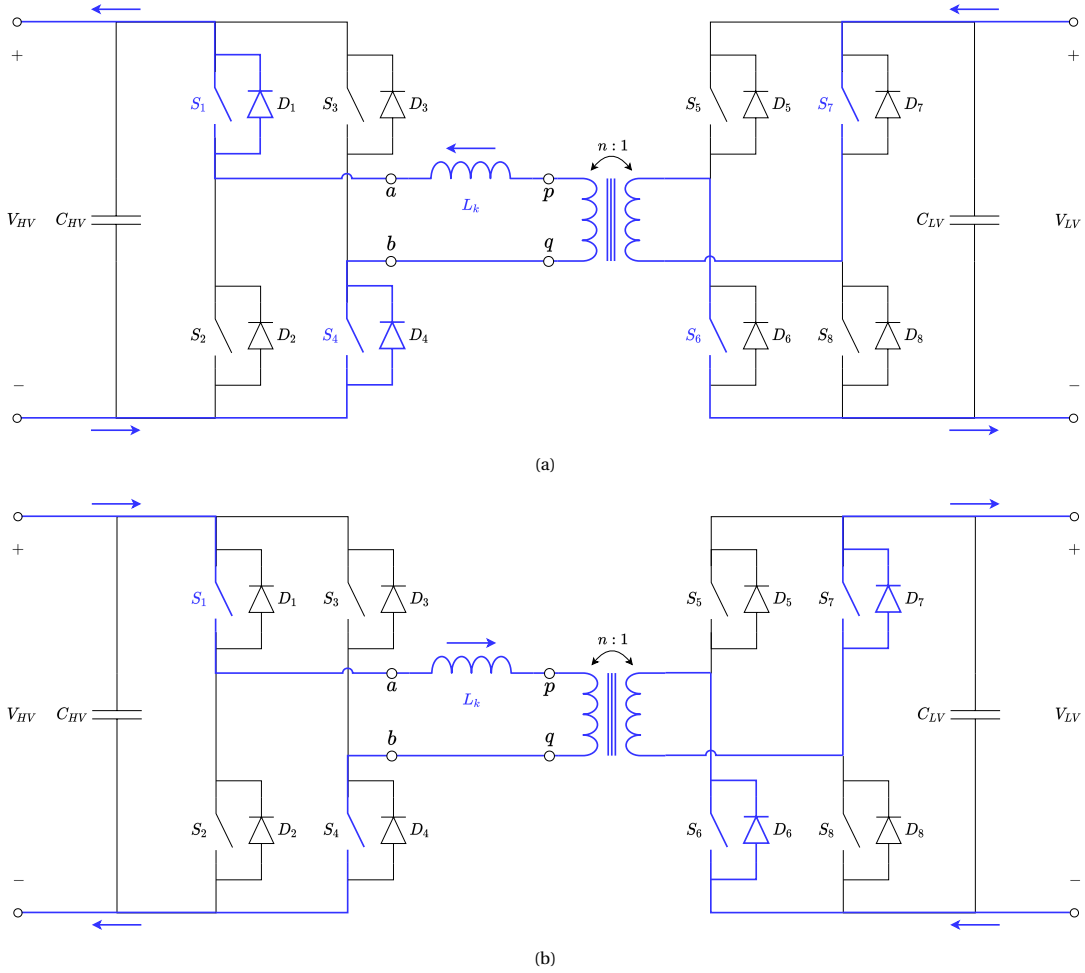



Figure 4.2: (a) The current flow, depicted with a blue conduction path, during period I for a negative inductor current and (b) for a positive inductor current.

the dead time between the switching action of the bridge. Without this dead time, there is the possibility of shorting the LV side. At the moment that all switches of the LV bridge are open, the current commutation takes place, as is shown in fig. 4.4.

In order to simplify the analysis, the transformer is taken out of the circuit and the voltage of the LV bridge is $nV_{LV}$. All further LV quantities are referred to the high side and it is assumed that during the transition period the HV and LV bus voltages are constant. Additionally, the parasitic capacitances of the switches and (optional) parallel diodes have been depicted as one parallel capacitors. The dotted lines represent the current flow that ensures the proper charging and discharging of these capacitors.
As stated before, during the dead time at $t_1$ in fig. 4.1, the remaining inductor current ensures a soft turn-on for switch pair $S_5$ and $S_8$. At the end of switching period I the inductor current is positive and switch pair $S_6$ and $S_7$ need to turn-off. Because of the present inductor current, the switches need to break this current, resulting in hard switching. As the gate voltage of switches $S_6$ and $S_7$ drops, the current through them starts to decrease. The current through an inductor cannot be interrupted instantaneously and therefore an alternative current path has to be present. This alternative path runs the current via the parallel capacitors as shown in fig. 4.4. The inductor current is split into one path running via the capacitors across $S_5$ and $S_7$, and one path via the parallel capacitors of $S_6$ and $S_8$.

The result of this alternative current path is that the parallel capacitors of $S_5$ and $S_8$ are discharged. If the top of all depicted capacitors in fig. 4.4 is set to be the positive terminal, it can be seen that the current is flowing out of the positive terminals of the capacitors across switches $S_5$ and $S_8$, thereby discharging them. These capacitances were blocking the full LV bus voltage before, thus the stored energy is carried away by the

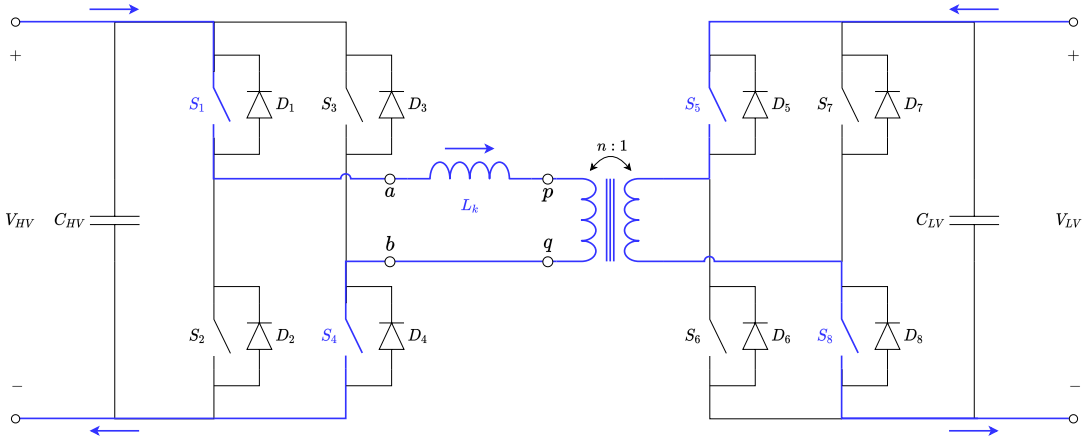



Figure 4.3: The current flow during period II.

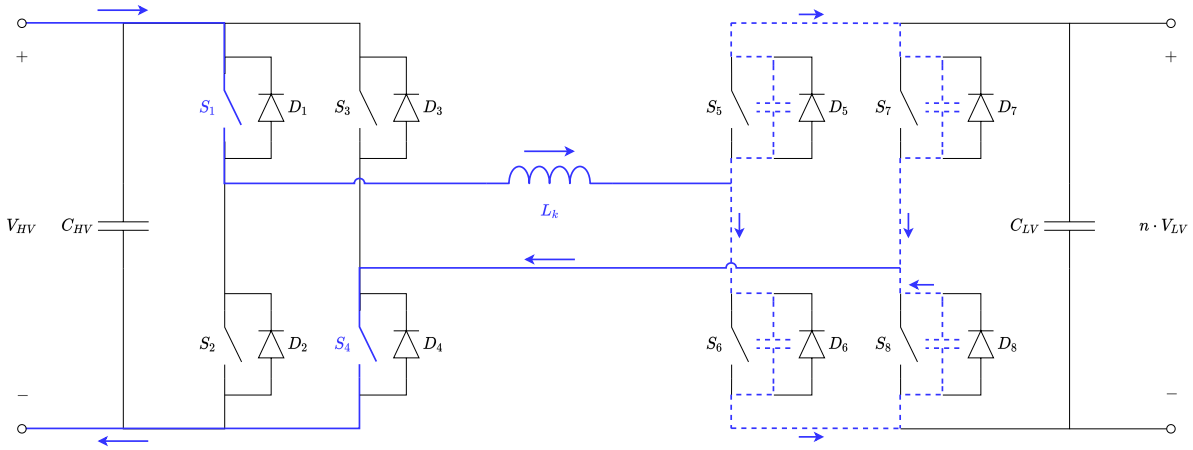



Figure 4.4: The current flow during the transition from period I to period II.

current flow. In a similar way, it can be seen that the current direction for the parallel capacitors of $S_6$ and $S_7$ is charging those capacitors. Since these switches were conducting during period I, there is no stored energy in the capacitors. Considering the fact that similar switches and devices will be used to implement all LV bridge switches, it can be concluded that the current of the inductor fully discharges the capacitors across $S_5$ and $S_8$, and fully charges the parasitic capacitance of switches $S_6$ and $S_7$.
At the end of this energy exchange, there might still be remaining energy in the inductor, meaning that the current still has to flow. Now, the diodes $D_5$ and $D_8$ will carry this current, thereby clamping the voltage across switches $S_5$ and $S_8$ to zero[1], respectively. When the gate signal of these switches rises, the switches will be turned on with zero voltage, resulting in a soft turn-on, thereby eliminating otherwise accompanied switching losses.

## 4.2. Alternative modulation schemes

As shown in detail in section 2.2.3 there is a limited region in which ZVS can be realized. This region is defined by means of SPS modulation, having only one parameter to manipulate. SPS is the most straightforward and most used modulation scheme [5, 8, 36, 37]. Alternative modulation schemes are extended phase shift modulation [38], triangular current mode modulation [39], triple phase shift modulation and optimal modulation [40], which is a combination of slightly adjusted versions of aforementioned modulation schemes. Each modulation method will be discussed individually in order to get a thorough understanding of the optimal modulation method, which will be implemented in the final converter.

[1] In reality, the voltage across the switch will not be clamped to zero, but to the forward voltage drop of the diode. Depending on whether an external parallel diode is placed, this voltage drop will be smaller than when the internal body diode of the MOSFETs is used for this purpose. The turn-on losses will not reduce to zero completely, but will be negligibly low.

### 4.2.1. Extended phase shift

The first modulation method is the extended phase shift (EPS) modulation. The difference with SPS modulation is that it does not require the duty cycles of both bridges to be 0.5. Instead, the leading bridge can be operated with a duty cycle smaller than 0.5, leading to a three-level voltage output of that bridge as can be seen in fig. 4.5 for $v_{ab}(t)$.

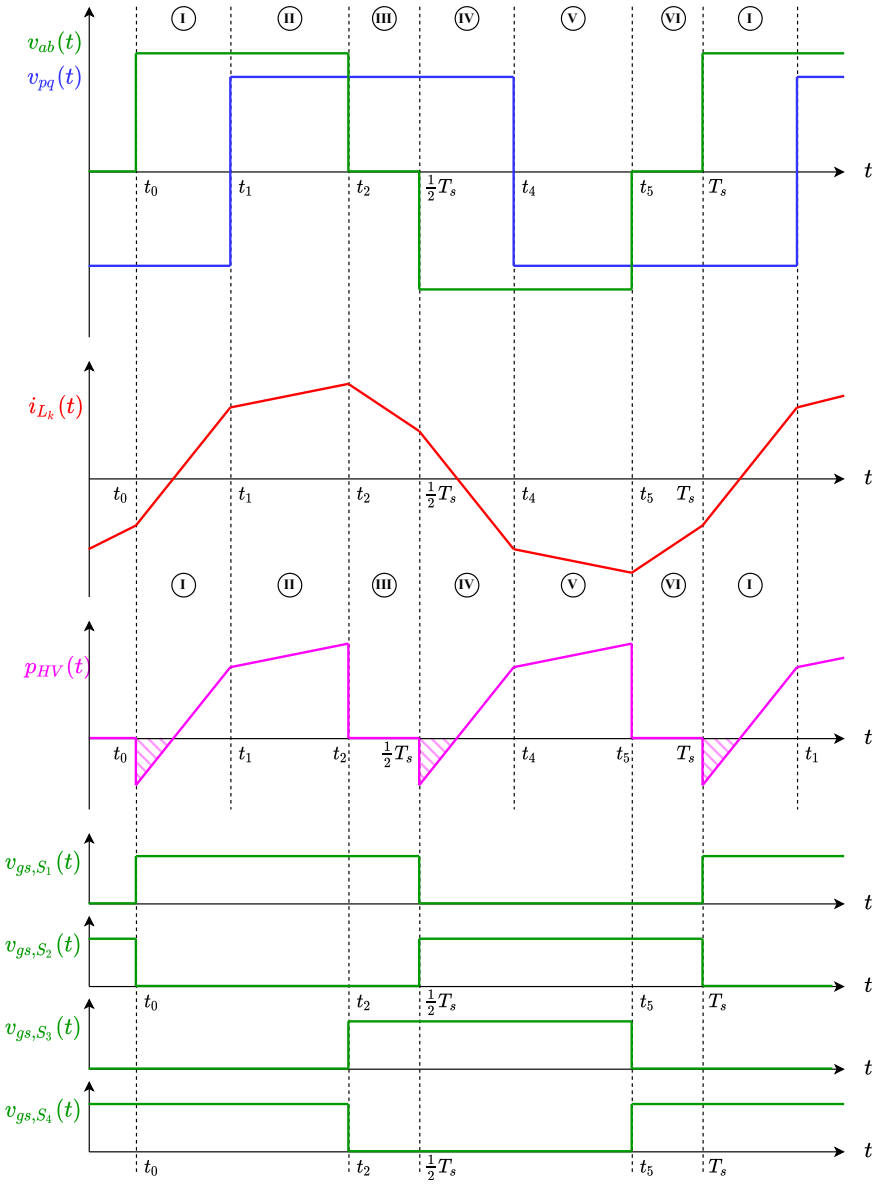



Figure 4.5: The waveforms of the DAB converter for EPS modulation, including HV bus power and gate signals for the leading HV bridge.

The leading bridge is able to create three voltage levels as defined by:

$$v_{ab}(t) = \begin{cases} +V_{HV}, & \text{for } t_0 \le t < t_2 \\ 0, & \text{for } t_2 \le t < \frac{1}{2}T_s \\ -V_{HV}, & \text{for } \frac{1}{2}T_s \le t < t_5 \\ 0, & \text{for } t_5 \le t < T_s \end{cases} \tag{4.1}$$

With this additional degree of freedom, one of the downsides of regular SPS modulation is tackled: reverse power flow [38]. When the instantaneous power as delivered by the HV bus is calculated by multiplying $v_{ab}(t)$ with $i_{L_k}(t)$ for the case of SPS, the pink waveform of fig. 4.1 is the result. The shaded area shows the total energy that flows back into the HV bus during half a switching cycle. This power is essentially not being delivered

to the LV side, however, it contributes to the total converter losses. Since this power is delivered by the HV bus and then retrieved again, it contributes to the total converter losses without delivering additional transferred power. With EPS modulation, the amount of energy that flows back into the source has dropped significantly, as can be seen in fig. 4.5. Here, the shaded area underneath the instantaneous HV side power is reduced due to the additional voltage level that the leading bridge can output.

A consequence of the additional voltage level is that there are more switching periods when compared to SPS modulation. Despite the additional period, the amount of switching for each switch remains the same. Before, with SPS, the 4 switches $S_1$-$S_4$ were divided into two switching pairs; $S_1$ with $S_4$ and $S_2$ with $S_3$. Then, both switching pairs would have to turn on once and turn off once per switching period. For the implementation of EPS, new switching pairs are made: $S_1$ with $S_2$ and $S_3$ with $S_4$. Instead of simultaneously switching both switches of one pair on and off, the switches of a switching pair are switching inverted. This means that when $S_1$ turns on, $S_2$ turns off and vice versa. Switching pair $S_3$ and $S_4$ will be controlled in a similar way. By controlling the switching pairs in such a way, a short in one of the bridge legs is prevented.
In order to obtain the third voltage level of the HV bridge, a phase shift between the rising edge of $S_1$ and $S_3$ is introduced, as shown in fig. 4.5. The phase shift can be expressed as the difference between $t_0$ and $t_1$. To realize $v_{ab}(t)$ to be zero, both HF transformer inputs on the HV side need to be clamped to either the positive or the negative bus. In switching period II, the terminals $a$ and $b$ are both clamped to the positive bus, thereby resulting in a voltage difference of 0 V. For period III, both terminals are clamped to the negative voltage bus, again resulting in 0 V over the terminals $a$ and $b$. By implementing this strategy, the same amount of switching actions per total switching period $T_s$ are needed as for SPS modulation.
With a similar number of switching moments, the total switching losses decrease for the EPS modulation. Similarly, the reduction of circulating power flow reduces the conduction losses too [41]. For that reason, EPS outperforms SPS when considering converter efficiency.

### 4.2.2. Triangular current mode

Another popular modulation scheme is triangular current mode (TCM) modulation as introduced in [39]. The name of this modulation scheme comes from the waveform of the inductor current $i_{L_k}(t)$, which is shaped as a triangle as can be seen in fig. 4.6.

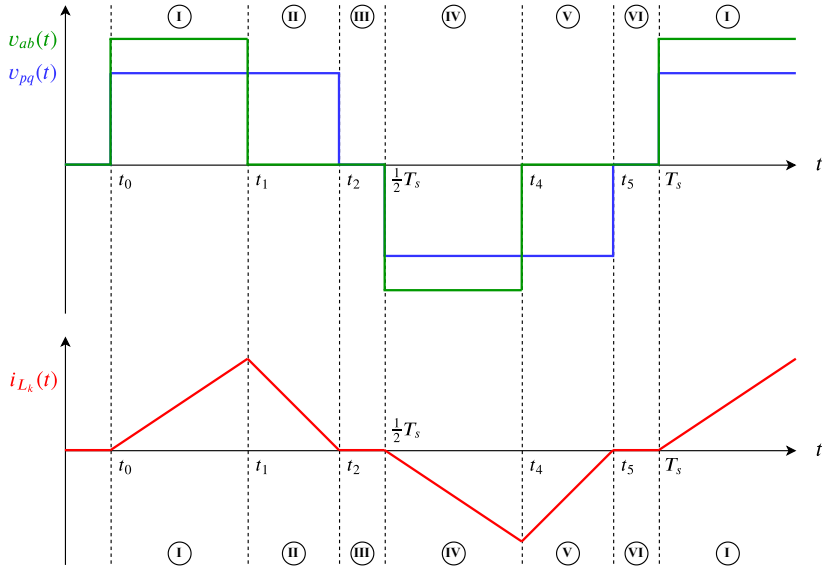



Figure 4.6: The waveforms of the DAB converter for TCM modulation with gate signals for the leading HV bridge.

The key advantage of this modulation scheme is that the inductor current returns to zero at the moment that the LV bridge switches. Having zero current switching (ZCS) is of interest,since switching off high (inductive) currents will lead to excessive switching losses due to parasitic inductances in the device packages [29].

The main operating principle of TCM is that the total energy that is stored in the inductor in period I, between $t_0$ and $t_1$, is retrieved again in period II, between $t_1$ and $t_2$. It can be seen that TCM is only possible when the amplitude of $v_{ab}(t)$ is not equal to $v_{pq}(t)$, or in other words, when $V_{HV}$ is different from $nV_{LV}$.
Only then, a voltage difference is present over the inductor and its current will change. At time instance $t_1$ the HV side bridge switches off and reduces the voltage to zero. This switching happens with ZVS, since the conditions for ZVS are met as derived in section 2.2.3. However, for the HV turn-on at $t_0$, switching losses are present,since there is no exchange of energy as discussed in section 4.1 due to zero inductor current at $t_0$.
For period II, when $v_{ab}(t)$ is reduced to 0 V, the inductor current starts decreasing until it reaches 0 A. Then, the LV switches change state such that the voltage $v_{pq}(t)$ becomes zero.
After period II, a third period is introduced, in which no energy transfer is present. Here, the voltage over the leakage inductance is zero. The length of this period depends on the required power transfer and the voltages of both buses of the converter. When a high power is demanded, period I and II will be extended until period III is non existing. Besides the power transfer, period III is also influenced by the voltage transfer ratio $M$. When $M >> 1$, the inductor current will increase rapidly during period I. Because of this increased current slope, the required amount of transferred energy from HV side to the LV side is obtained earlier than when $M$ is close to 1. Consequently, period I will be significantly shorter, with a slight increase of period II due to the higher inductor peak current at $t_1$. The total duration of period III will still decrease.

It can be concluded from this descriptive analysis that TCM modulation cannot satisfy all operating points. When either the required power is too high and/or the voltage transfer ratio approaches unity, TCM does not function anymore. Still, TCM provides advantages over regular SPS. The first and foremost being that the LV switching losses are reduced significantly. Secondly, the transformer RMS currents are reduced considerably when compared to SPS modulation [9]. However, to transfer a similar amount of power as SPS for a given operating point, the peak current of TCM increases, leading to higher component criteria [41].

### 4.2.3. Triple phase shift

Another modulation scheme that is often used is the triple phase shift (TPS) control [5]. As the name suggests, this modulation scheme adds another level of freedom to the control of the converter, compared to EPS and TCM. Apart from the phase shift of the leading bridge and the phase shift between the two bridges, with TPS the phase shift of the lagging bridge can also be controlled. Adding another level of freedom also increases the complexity of the control [9]. However, with the use of the additional degree of freedom, the total converter efficiency for all operating points can be improved [42]. The typical waveforms for TPS modulation are shown in fig. 4.7.

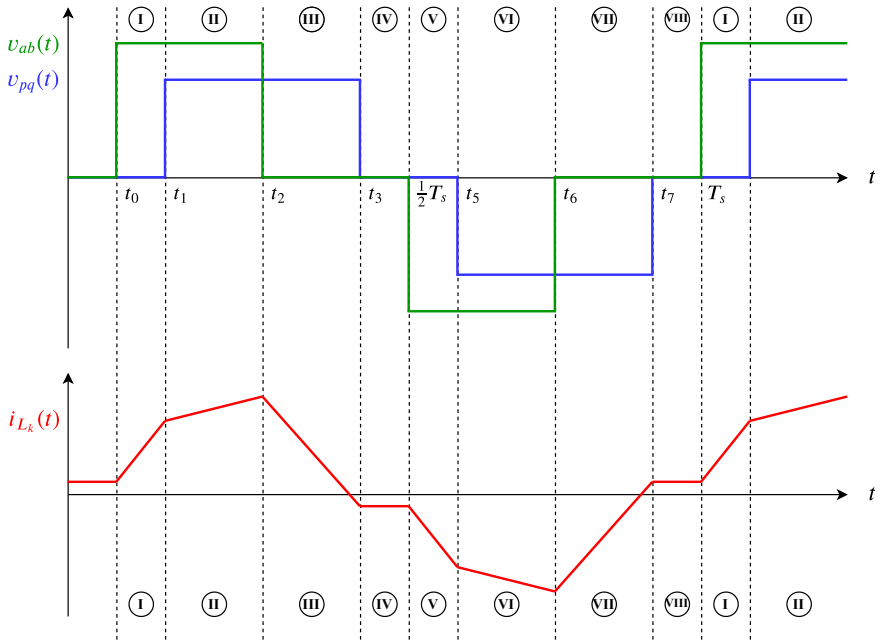



Figure 4.7: The waveforms of the DAB converter for TPS modulation.

As can be seen, the waveform of the inductor current looks somewhat similar to the current waveform for SPS modulation. The difference between the two mainly has to do with switching period IV. Here, for TPS, the current will be kept at a constant negative value, thereby enabling ZVS for the leading bridge, which is the HV bridge in this case. Similarly, during period VIII the inductor current will be a constant positive value. Again, ZVS of the HV bridge is possible since the constant value of the inductor current is controlled to be larger than the minimum current needed for ZVS, as defined in section 2.2.3.
For TPS, three parameters can be controlled to modify the current waveform as desired. First, the duty cycle of the leading bridge can be controlled, which happens at $t_2$ in fig. 4.7. Second, the duty cycle of the lagging bridge can be adjusted, to alter the moment when both bridges are switched to 0 V, depicted as $t_3$. Finally, the phase shift between the two waveforms can be adjusted by altering the moment when the lagging bridge has its rising edge.
So, the additional degree of freedom gives full control over the operation and thus performance of the converter. This means that the highest efficiency can be obtained by integrating TPS modulation, at the cost of a more complex control. It should be noted that TPS can lead to EPS and SPS for certain operating points. Similarly, EPS can sometimes be operated SPS, since the duty cycle of the leading bridge can be put to 50 %. SPS is the most restrictive modulation strategy, with the simplest control of all of them.

## 4.3. Optimal modulation

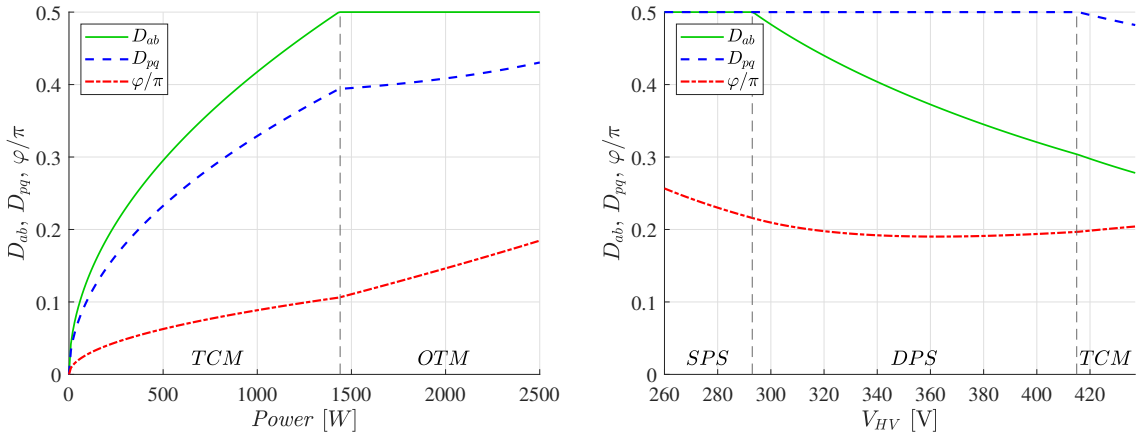
The modulation schemes so far have been alternatives to the basic SPS modulation scheme. The main reason for implementing different modulation schemes is that SPS causes high peak and RMS currents through the leakage inductor and transformer windings, together with a limited ZVS region, as shown in section 3.3. The alternative modulation methods as briefly introduced in sections 4.2.1–3 all have advantages and disadvantages. Additionally, they have an optimum operating range, in which these modulation methods outperform other modulation schemes. To optimally make use of the previously introduced modulation techniques, an optimal modulation scheme is introduced in [40]. The principle of this optimal scheme will be explained and implemented.

The main objective of the optimal modulation scheme is to minimize the inductor current $i_{L_k}$ as much as possible. The magnitude of this inductor current is directly correlated to the conduction losses of the total converter. Since the conduction losses are one of the major contributors to the total converter losses, as long as ZVS is maintained, it is important to reduce the inductor current to a minimum.
In order to do so, three parameters can be controlled. These three parameters are the duty cycle $D_{ab}$ of the HV bridge, the duty cycle $D_{pq}$ of the LV bridge and the phase shift $\varphi$ between the two bridges. The operating ranges of these control parameters are given by:

$$\begin{aligned} 0 < D_{ab} &\leq \tfrac{1}{2} \\ 0 < D_{pq} &\leq \tfrac{1}{2} \\ -\tfrac{1}{2} \leq \varphi/\pi &\leq \tfrac{1}{2} \end{aligned} \tag{4.2}$$

The ranges of these parameters hold for both directions of power transfer. The duty cycles cannot exceed 0.5 (or 50 %). Regarding the phase shift, smaller values than $-\frac{1}{2}$ and larger values than $\frac{1}{2}$ are possible to achieve, however, they lead to excessive losses [5].
The control parameters as listed by eq. (4.2) are the outcome of the optimal modulation scheme. They are computed based on the operating point of the converter, given by a unique combination of $V_{HV}$, $V_{LV}$ and $P_{LV}$, in case of positive power transfer. For a specific operating point there is one modulation scheme that results in the highest converter efficiency for that point.
In theory, a control strategy can be employed that computes what modulation scheme is the best for a given point and execute it. This approach is feasible for steady state operation when the converter has a set operation point. However, when one of the bus voltages or power setpoint changes, a new control strategy could be needed to get the highest converter performance. This can lead to a step change of control parameters $D_{ab}$, $D_{pq}$ and $\varphi$, which is generally undesirable. Such jumps in parameters can lead to unstable behavior.

To overcome this problem, an optimized closed form control solution [2] can be derived. The advantage is that the control parameters will not have discrete steps when switching between modulation schemes, but are rather a piecewise continuous function. This simplifies the control and transition between schemes significantly [9]. The change of parameters for different modulation strategies is shown in fig. 4.8a, where the three control parameters are displayed for an increasing power level. For the converter that has to be designed in this thesis, it is more interesting to look at a sweep of voltages, since the power will be kept constant. This can be seen in fig. 4.8b, where the control parameters are shown for different HV bus voltages. From the graphs it can be seen that the control parameters have no jumps or steps when transitioning between two modulation schemes.




(a) (b)

Figure 4.8: The control parameters of the optimal modulation scheme for (a) changing LV side power with $V_{HV} = 260$ V and $V_{LV} = 55$ V and (b) changing HV bus voltage with $P_{LV} = 2.5$ kW. The DAB converter parameters are $L_k = 25$ $\mu$H, $n = 6$ and $f_s = 100$ kHz.

In order to create the optimal modulation that leads to the control parameters as seen in fig. 4.8, it needs to be known in what area which modulation method should be active. First, small adjustments have to be made to the previously introduced EPS modulation, called optimal transition mode [9], which will be introduced in section 4.3.1. Together with standard SPS modulation and TCM modulation, a final modulation scheme can be composed, focused at increasing total converter efficiency by aiming at minimum conduction losses [40]. This will be discussed in section 4.3.2.

### 4.3.1. Optimal transition mode

Optimal transition mode (OTM) modulation, as introduced by [9], is similar to the earlier discussed EPS modulation, however, the way the duty cycle of the bridge is calculated is different. Additionally, OTM ensures a seamless transition to SPS and TCM modulation, resulting in the plots as seen in fig. 4.8.

The principle of OTM is similar to EPS: only one of the two bridges will have a reduced duty cycle, which is less than 0.5. The other bridge continuous to operate with a duty cycle of 0.5. Next to that, the phase shift between the two bridges can be controlled as an additional parameter. To determine what bridge has to be operated with a 50 % duty cycle, several conditions apply. First of all, standardization variables are introduced to reduce the complexity of formulae, as defined as follows:

[2] A closed form expression is a mathematical expression that only contains standard operations, such as multiplications, additions etc. In this context it does not contain any differentiation, integration or limit.

| | |
|---|---|
| $V_{ref}$ | Arbitrarily selected reference voltage |
| $Z_{ref} = 2\pi f_s L_k$ | Reference impedance |
| $P_{ref} = V_{ref}^2 / Z_{ref}$ | Reference power |
| $\overline{V}_{ab} = V_{HV} / V_{ref}$ | Normalized voltage of the HV side |
| $\overline{V}_{pq} = nV_{LV} / V_{ref}$ | Normalized voltage of the LV side |
| $\overline{P}_{LV} = P_{LV} / P_{ref}$ | Normalized LV power |
| $D_{ab}$ | Duty cycle of the HV bridge |
| $D_{pq}$ | Duty cycle of the LV bridge. |

Next, a transformation of variables is needed to standardize the computation of the duty cycle of the bridges [40]:

$$\left[\overline{V}_1 \;\; \overline{V}_2 \;\; D_1 \;\; D_2\right] = \begin{cases} \left[\overline{V}_{ab} \;\; \overline{V}_{pq} \;\; D_{ab} \;\; D_{pq}\right] & \text{for } \overline{V}_{ab} \leq \overline{V}_{pq} \\ \left[\overline{V}_{pq} \;\; \overline{V}_{ab} \;\; D_{pq} \;\; D_{ab}\right] & \text{for } \overline{V}_{ab} > \overline{V}_{pq}. \end{cases} \tag{4.3}$$

Now that the new variables have been introduced, the inequality $\overline{V}_1 \leq \overline{V}_2$ always holds, reducing the amount of formulae needed to describe the modulation scheme.
As mentioned before, one of the duty cycles is always clamped to 0.5, where the other duty cycle is lower than that. The full bridge that has the duty cycle of 0.5 is determined as follows:

$$\begin{aligned} D_1 &= \tfrac{1}{2} \\ D_2 &< \tfrac{1}{2}. \end{aligned} \tag{4.4}$$

From the combination of conditions given by eq. (4.3) and eq. (4.4), six possible waveforms can be sketched. All of the derived possible combinations are given in fig. 4.9 and numbered accordingly.

### 4.3.2. Modulation scheme distribution

The combination and transition points of the three different modulation schemes that will be implemented, being TCM, OTM and SPS, needs to be determined. As mentioned before, every modulation scheme has its optimal operation point. A combination of these schemes leads to a minimized inductor current $i_{L_k}$, thereby reducing the overall conduction losses of the converter.
Since the control parameters $D_{ab}$, $D_{pq}$ and $\varphi$ cannot be analytically found, an analysis has been done in [40], where a numerical search is used to to find the best modulation scheme for a range of operating points. From that analysis the optimal operating range of the three modulation schemes has been determined.

**TCM**

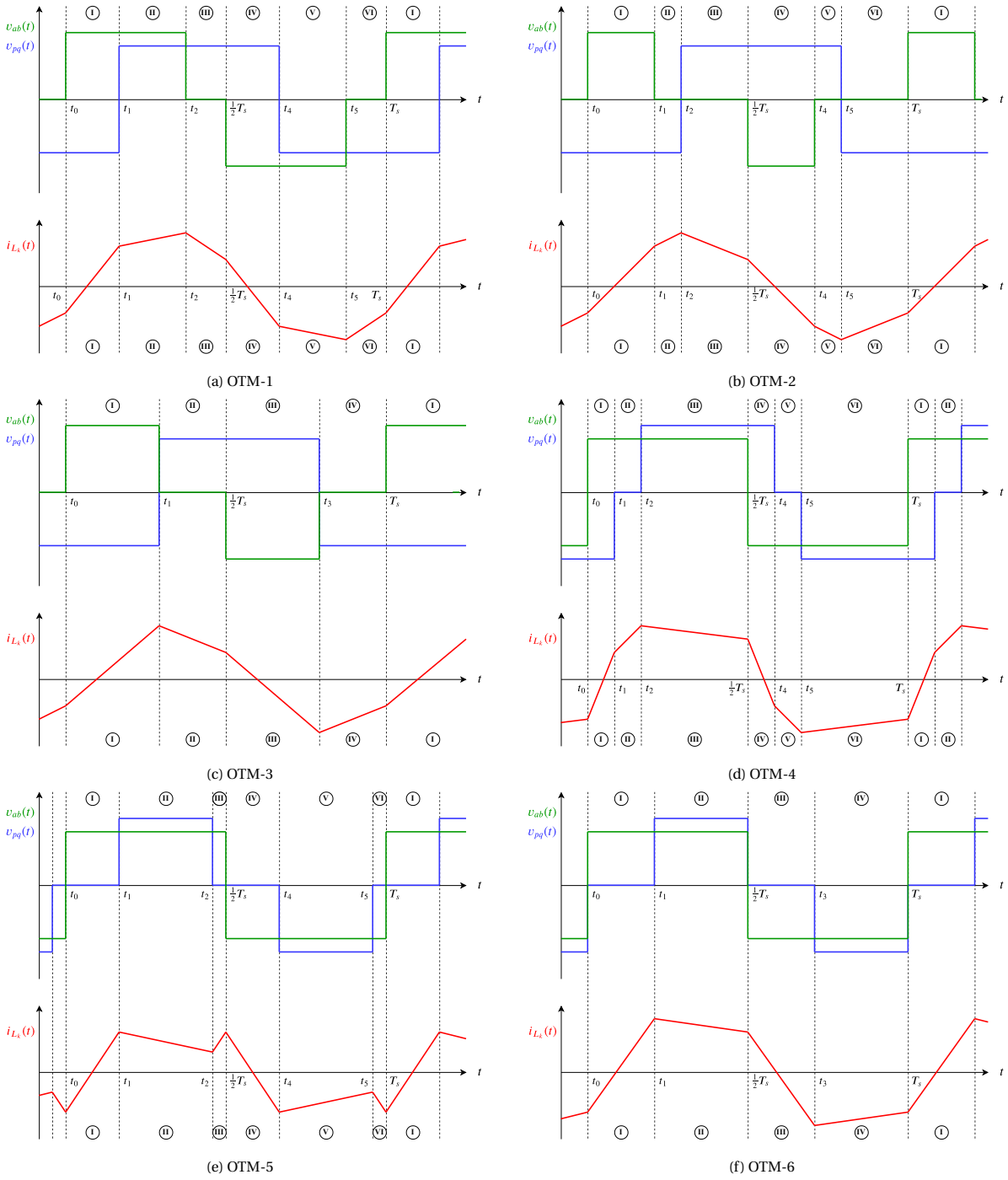
For low power ranges TCM is the preferred method up to a certain maximum power, labelled with $P_{\Delta,max}$. As explained in section 4.2.2, there is a maximum power that can be achieved with TCM. This maximum power can be computed using the maximum power as given in [39] for $V_{HV} < nV_{LV}$:

$$P_{\Delta,max} = \frac{V_{HV}^2 \left(1 - 2\tau_{blank} f_s\right)^2 \left(nV_{LV} - V_{HV}\right)}{4L_k f_s n V_{LV}} \tag{4.5}$$

where $\tau_{blank}$ is the dead time between switching. Under the assumption that the DAB uses ideal switches, the blanking time can be made 0. Rewriting the equation based on the introduced standardized variables is done in Appendix A.3 and results in:

$$\overline{P}_{\Delta,max} = \frac{\pi}{2} \frac{\overline{V}_1^2 \left(\overline{V}_2 - \overline{V}_1\right)}{\overline{V}_2} \tag{4.6}$$

Up and until this power level is achieved, TCM can be utilized as the optimal modulation scheme. As can be seen from eq. (4.6), the maximum power of TCM is also dependent on the voltages $\overline{V}_1$ and $\overline{V}_2$ and consequently the voltage transfer ratio $M$. For that reason, TCM is still optional in the higher power regions, where $M$ is not close to unity.




(a) OTM-1

(b) OTM-2

(c) OTM-3

(d) OTM-4

(e) OTM-5

(f) OTM-6

Figure 4.9: Schematic representation of different waveform options for OTM modulation for positive power flow, with a leading HV bridge. For (a)-(c) it holds that $\overline{V}_{ab} > \overline{V}_{pq}$, resulting in $D_{pq} = 0.5$. For (d)-(f) it can be seen that $\overline{V}_{ab} \leq \overline{V}_{pq}$, resulting in $D_{ab} = 0.5$.

**OTM**

When the operating power exceeds the maximum power of TCM for a given operating point, OTM will be used as the modulation scheme. For OTM, one of the bridges will be clamped to a duty cycle of 0.5, which will naturally happen when TCM reaches its maximum power. This has been shown in fig. 4.8, where, depending on the HV and LV bus voltages, one of the bridges its duty cycle reaches the maximum value. After this, OTM seamlessly takes over and the other control parameters will continue to vary depending on the operating point.

**SPS**
The final modulation scheme is SPS, which has both bridges operating at the maximum duty cycle. The remaining control parameter that can be adjusted is the phase shift between the two bridges. For given HV bus voltages, the phase shift will increase with increasing power. For a given power, the phase shift will decrease with increasing $M$, as can be seen in fig. 4.8b. Eventually, OTM can take over from a certain limit and one of the bridges its duty cycle will be reduced.

## 4.4. Implementation of the optimal modulation scheme

With the three modulation schemes and their distribution being discussed, the implementation into the minimum search script will be described. The working principle of the minimum search script is not changed, however, the control parameter computation has become more complex, as is shown in section 4.4.1. Additionally, the calculation of the inductor current waveform adds another level of complexity to the total optimal modulation implementation, which is discussed in section 4.4.2. Finally, in section 4.4.3 a new component selection will be made based on the new specifications that follow from the new modulation scheme.

### 4.4.1. Calculation of the control parameters

Before the inductor currents can be calculated, the operation mode needs to be known. As discussed in section 4.3.2, there is a distribution that ensures that the most efficient modulation scheme will be implemented. The first selection is done based on the operating power. Given a certain $V_{HV}$, $V_{LV}$ and $P_{LV}$ (still, positive power transfer is assumed here), $P_{\Delta,max}$ can be computed. When the normalized operating power, $\overline{P}_{LV}$, is lower than $\overline{P}_{\Delta,max}$, triangular current mode will be used. When $\overline{P}_{LV}$ is higher than $\overline{P}_{\Delta,max}$, OTM and/or SPS will be implemented. The formulae to calculate the control variables for OTM and SPS are the same, but for TCM different formulae apply. This is shown and derived in [40] and will be explained in this section. Before the calculation of the control parameters can start, an important difference in terms of the phase shift $\varphi$ has to be noted. In [40], the phase shift time, $T_\varphi = \varphi/2\pi f_s$, is defined as the difference between the middle of the duty cycle of the leading bridge, and the middle of the duty cycle of the lagging bridge, as shown in fig. 4.10.

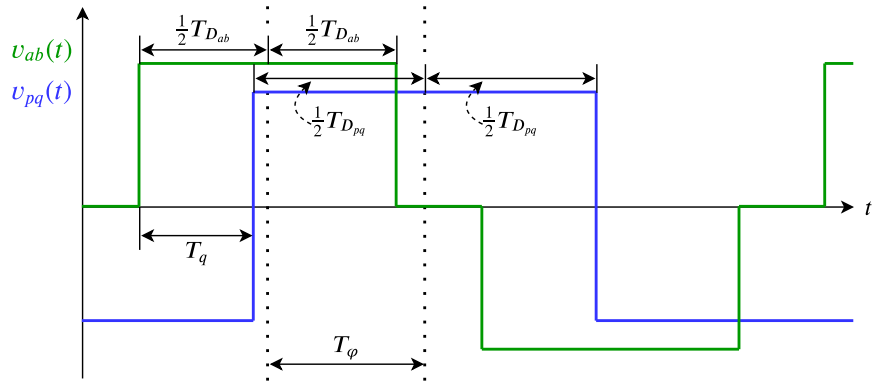



Figure 4.10: The definition of the phase shift time $T_\varphi$ as used in further formulae, shown for OTM-1.

In this thesis, the variable $T_q$ is introduced to define the phase shift in a similar way as for SPS, where the phase shift was defined as the difference between the rising edge of the leading bridge and the rising edge of the lagging bridge. Later, with the calculation of the inductor current, $T_q$ will be used over $T_\varphi$, as will be shown in section 4.4.2. Additionally, the gate driver signal generation requires less computation steps, since $T_q$ is the exact delay that should applied between the rising edge of $S_1$ and $S_5$.

**$\overline{\mathbf{P}}_{\mathbf{LV}} \leq \overline{\mathbf{P}}_{\Delta,\mathbf{max}}$**
In principle, TCM will be used for all operating points, unless the operating power is larger than the maximum power for TCM (given the operating conditions). If that is not the case, then the control variables $D_{ab}$, $D_{pq}$ and $\varphi$ can be calculated using [40]:

$$\begin{aligned}\varphi &= \pi \cdot \operatorname{sgn}\left(\overline{P}_{LV}\right)\sqrt{\frac{\overline{V}_2-\overline{V}_1}{2\overline{V}_1^2\overline{V}_2}\frac{|\overline{P}_{LV}|}{\pi}}\\ D_1 &= \frac{|\varphi|}{\pi}\frac{\overline{V}_2}{\overline{V}_2-\overline{V}_1}\\ D_2 &= \frac{|\varphi|}{\pi}\frac{\overline{V}_1}{\overline{V}_2-\overline{V}_1}.\end{aligned} \tag{4.7}$$

For the TCM control parameters, both duty cycles are smaller than 0.5, resulting in a free wheeling period, indicated as period III in fig. 4.6. When $\overline{P}_{LV}$ increases, $D_1$ and $D_2$ will increase, resulting in a decreasing period III. When $\overline{P}_{LV} = \overline{P}_{\Delta,max}$, $D_1$ reaches 0.5 and period III is no longer present as the free wheeling period. Additionally, when the operating voltages of the converter change, $\overline{P}_{\Delta,max}$ could be lowered until $D_1$ reaches 0.5, thereby transitioning into OTM modulation.

**$\overline{\mathbf{P}}_{\mathbf{LV}} > \overline{\mathbf{P}}_{\Delta,\mathbf{max}}$**

For all operating points where TCM is not sufficient to deliver the power, OTM and SPS will be implemented. The calculation of the control variables for OTM is computationally heavy. The full expression to compute $D_2$ is listed in Appendix A.4. Here, the resulting final expressions for the control parameters will be given, resulting in [40]:

$$\begin{aligned}D_1 &= \tfrac{1}{2}\\ D_2 &= \tfrac{1}{4}\left(2\sqrt{e_7}-2\sqrt{e_8}-e_1\right)\\ \varphi &= \pi\cdot\operatorname{sgn}\left(\overline{P}_{LV}\right)\cdot\left[\frac{1}{2}-\sqrt{D_1\left(1-D_1\right)+D_2\left(1-D_2\right)-\frac{1}{4}-\frac{|\overline{P}_{LV}|}{\pi\overline{V}_1\overline{V}_2}}\right],\end{aligned} \tag{4.8}$$

where $e_1$, $e_7$ and $e_8$ are intermediate variables used in the calculation of $D_2$, as given by Appendix A.4. For certain $\overline{V}_1$ and $\overline{V}_2$, $D_2$ will get larger than 0.5, as can be seen in fig. 4.11.

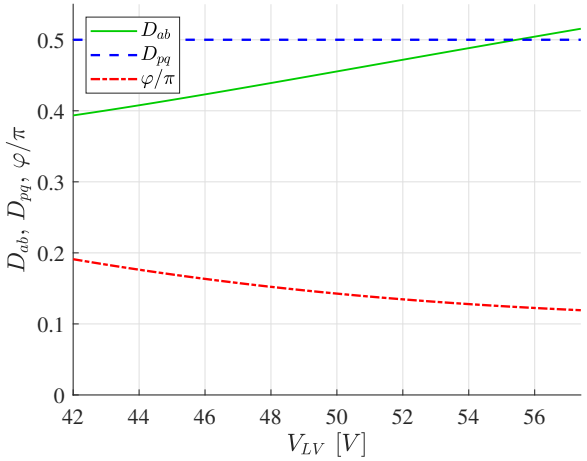



Figure 4.11: The calculated control variables for OTM for a full sweep over $V_{LV}$ with $V_{HV}$ = 346 V.

It can be seen that in this case for large $V_{LV}$ the duty cycle of the HV bridge goes over 0.5, reaching up to 0.52. This duty cycle is not possible, and therefore the duty cycles will be limited to 0.5. In [40] the power is being calculated at which this happens, using a computationally heavy numerical solver. However, in this thesis the transition from OTM to SPS is implemented by a simple minimum statement:

$$D_2 = \min\left(\tfrac{1}{4}\left(2\sqrt{e_7}-2\sqrt{e_8}-e_1\right), 0.5\right). \tag{4.9}$$

The exact power at which OTM transitions to SPS is not of interest for the operation of this converter. The control variables have a seamless transition between the two modes, and therefore the implementation given by eq. (4.9) is sufficient.

### 4.4.2. Calculation of the inductor current

In order to generate loss maps for the optimal modulation scheme, the loss models require the new RMS currents. For SPS modulation, a formula to determine $I_1$ and $I_2$ was derived. However, the derivation of such a formula for all possible waveforms of the three modulation schemes will quickly get complex. Instead, an alternative method is implemented, that makes use of the slope of the current waveform and the time of a switching region. The method will be worked out for one particular case of the OTM scheme: OTM-1. For the other remaining cases and schemes the same approach will be implemented.
First, the slopes of all switching regions has to be determined. All possible slopes can be listed according to:

$$\frac{di_{L_k}}{dt} = \begin{cases} 0 & \text{for } V_{ab}=0,\ V_{pq}=0 \\ \frac{V_{HV}}{L_k} & \text{for } V_{ab}>0,\ V_{pq}=0 \\ \frac{-V_{HV}}{L_k} & \text{for } V_{ab}<0,\ V_{pq}=0 \\ \frac{-nV_{LV}}{L_k} & \text{for } V_{ab}=0,\ V_{pq}>0 \\ \frac{nV_{LV}}{L_k} & \text{for } V_{ab}=0,\ V_{pq}<0 \\ \frac{V_{HV}-nV_{LV}}{L_k} & \text{for } V_{ab}>0,\ V_{pq}>0 \\ \frac{V_{HV}+nV_{LV}}{L_k} & \text{for } V_{ab}=0,\ V_{pq}<0 \\ \frac{-V_{HV}-nV_{LV}}{L_k} & \text{for } V_{ab}<0,\ V_{pq}>0 \\ \frac{-V_{HV}+nV_{LV}}{L_k} & \text{for } V_{ab}<0,\ V_{pq}<0 \end{cases} \tag{4.10}$$

To calculate the absolute increase in current for each period of the waveform, next to the slopes, the duration of each period has to be known. Since there are many possible waveforms with different slopes and periods, only one per modulation scheme will be worked out. The principle of the other waveforms is similar and can be derived using the same steps.

**TCM**

To analyze the waveforms of the TCM modulation, a zoomed version with important parameters is shown in fig. 4.12.

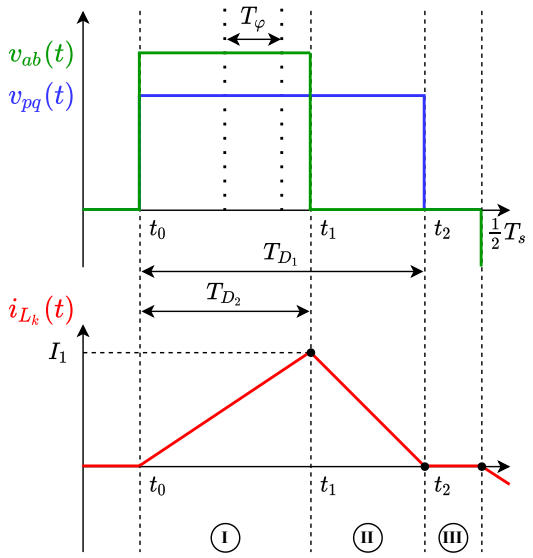



Figure 4.12: Zoomed half period waveforms for TCM modulation.

Because of the half cycle symmetry in steady state operation, the displayed waveform has been reduced, since for the negative half cycle the results will be similar. As an example, at $i_{L_k}(t_0) = i_{L_k}\left(\frac{1}{2}T_s\right)$ and $i_{L_k}(t_1) = -i_{L_k}(t_4)$,

where $t_4$ can be seen in fig. 4.6. The conditions for each period as defined by fig. 4.12 have been summarized in table 4.1.

Table 4.1: Operating conditions for TCM modulation.

| **Property** | **Region I** | **Region II** | **Region III** |
|---|---|---|---|
| Slope of inductor current | $\frac{V_{HV}-nV_{LV}}{L_k}$ | $\frac{-nV_{LV}}{L_k}$ | 0 |
| Duration of region | $T_{D_2}$ | $T_{D_1}-T_{D_2}$ | $\frac{1}{2}T_s-T_{D_1}$ |
| Peak inductor current | $I_1$ | | |

Using the values derived in table 4.1, the absolute difference in current per region can be calculated, by multiplying the slope of the inductor current with the duration of the region. Then, $I_1$ is known for TCM and the RMS current can be calculated by using eq. (3.1).

**OTM-1**

In a similar way, the currents for OTM-1 can be derived. First, a zoomed version of the waveform is shown in fig. 4.13, in which the current points and important times are made visible.

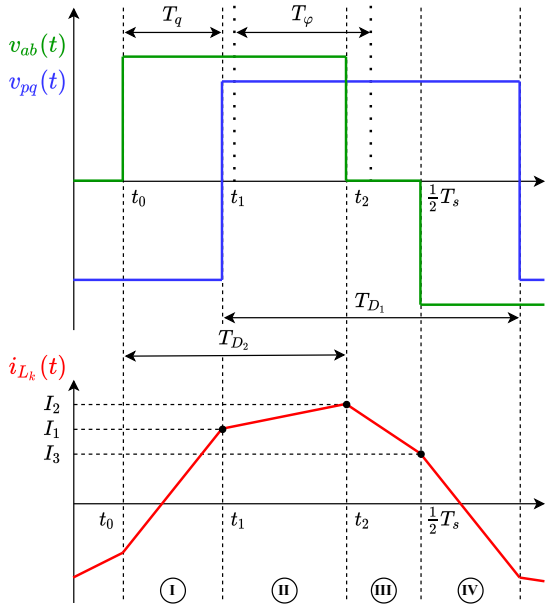



Figure 4.13: Zoomed half period waveforms for OTM-1 modulation.

As can be seen from the figure, for OTM the alternative phase shift variable can be used, where the alternative phase shift time can be expressed as:

$$T_q = \tfrac{1}{2}T_{D_1} + T_\varphi - \tfrac{1}{2}T_{D_2}. \tag{4.11}$$

For all OTM waveforms under positive power transfer eq. (4.11) is valid. However, when power is transferred from LV side to the HV side, $T_{D_1}$ and $T_{D_2}$ should be swapped. Again, the conditions for each period as defined by fig. 4.13 have been summarized in table 4.2.

Table 4.2: Operating conditions for OTM-1 modulation.

| **Property** | **Region I** | **Region II** | **Region III** |
|---|---|---|---|
| Slope of inductor current | $\frac{V_{HV}+nV_{LV}}{L_k}$ | $\frac{V_{HV}-nV_{LV}}{L_k}$ | $\frac{-nV_{LV}}{L_k}$ |
| Duration of region | $T_q$ | $T_{D_1}-T_q$ | $\frac{1}{2}T_s-T_{D_1}$ |
| Peak inductor current | $I_2$ | | |

Now that the slope and duration of each period are known, the difference in current per period can be calculated. For OTM-1, the peak inductor current $I_2$ can be calculated by:

$$I_2 = \frac{I_{pp}}{2} = \frac{|\Delta i_{L_k}1| + |\Delta i_{L_k}2| + |\Delta i_{L_k}3|}{2}, \tag{4.12}$$

where $\Delta i_{L_k 1-3}$ are the change in current for each period. Equation 4.12 is valid because of the symmetry of the waveforms. For other OTM waveforms a similar approach can be followed by replacing $I_2$ in eq. (4.12) by the respective peak current of that waveform.

**SPS**

Finally, a similar approach to SPS modulation will be done in this part, starting with the zoomed waveforms in fig. 4.14. For SPS there are two different waveforms, depending on $V_{HV}$ and $V_{LV}$. For consistency, the waveforms that will be discussed here are for $V_{HV} > nV_{LV}$, labelled as SPS-1. For SPS-2, where $V_{HV} < nV_{LV}$, and SPS-3, where $V_{HV} = nV_{LV}$, a similar approach can be used as described below.

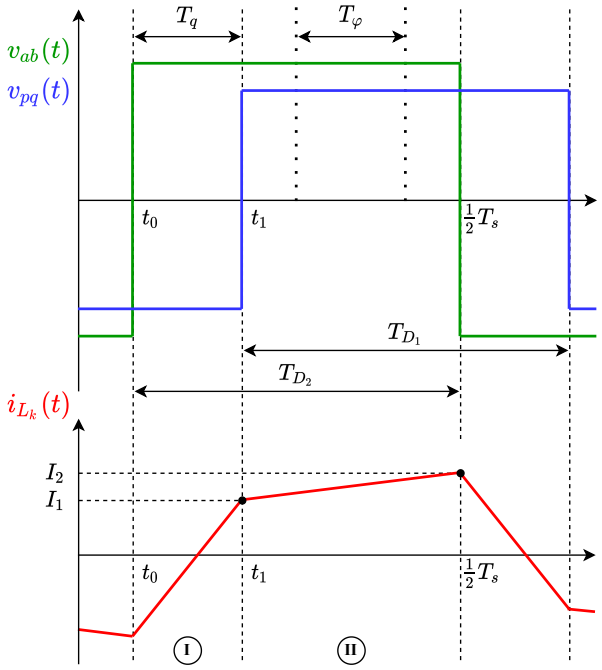



Figure 4.14: Zoomed half period waveforms for SPS-1 modulation.

For SPS it holds that $T_\varphi = T_q$ as can be seen from the figure. Additionally, $T_{D_1} = T_{D_2}$, meaning that the duty cycle of both bridges is 0.5. From fig. 4.14 the operating conditions can be extracted and are summarized in table 4.3.

Table 4.3: Operating conditions for SPS-1 modulation.

| **Property** | **Region I** | **Region II** | **Region III** |
|---|---|---|---|
| Slope of inductor current | $\frac{V_{HV}+nV_{LV}}{L_k}$ | $\frac{V_{HV}-nV_{LV}}{L_k}$ | 0 |
| Duration of region | $T_q$ | $\frac{1}{2}T_s - T_q$ | 0 |
| Peak inductor current | $I_2$ | | |

The values of $I_1$ and $I_2$ are calculated in the same way as for the other switching schemes, rather than using eq. (2.10) and eq. (2.11), to keep the implementation in the minimum search script standardized. Instead of defining a different way to calculate the currents for SPS, the same method can be used as for TCM and OTM.

### 4.4.3. Component selection

Since the new modulation schemes result in different current levels for all components, the MOSFET selection and inductor designs have been updated compared to the ones in section 3.2.1. The newly chosen MOSFETs will briefly be introduced together with an overview of their specifications. After that, the new inductor designs will be shown, after which they can be implemented in the minimum loss script.

#### MOSFET selection

Now that a different modulation scheme has been implemented, different MOSFETs can be added to the selection of table 3.2. The adjusted HV MOSFET requirements are listed in table 4.4. Simultaneously, the requirements for the LV MOSFETs have been updated according to the new modulation schemes. The LV bridge MOSFETs will remain the Si variants, since at the moment of writing there are no competitive SiC switches available for that voltage level.

Table 4.4: The updated selection criteria for the HV and LV bridge MOSFETs. These values are calculated for $L_k = 25\ \mu$H and $n = 6$.

| | **HV bridge** | **LV bridge** |
|---|---|---|
| Qualification | AEC-Q101 | |
| Technology | SiC | Si |
| Max. operating voltage [$V$] | 437 | 57.4 |
| Min. breakdown voltage [$V$] | 610 | 100 |
| Max. RMS current [$A_{RMS}$] | 8.5 | 51 |
| Max. peak current [$A$] | 20.6 | 124 |

When comparing table 4.4 with table 3.1, it can be seen that both the RMS currents as well as the peak currents have dropped due to the new modulation schemes. This reduces the device stress and may lead to different trade-offs for the variables of the minimum search script. Using the listed requirements, additional HV MOSFETs are selected and added to the existing list. The new ones are listed in table 4.5. The selection of LV MOSFETs has not changed and can therefore still be found in table 3.3.

Table 4.5: The selected additional SiC MOSFETs for the HV bridge.

| **MPN** | **$R_{ds,ON,max}$** | **$Q_g$** | **$V_{gs,max}$** | **$V_{dss}$** | **$C_{oss}$** | **$Q_{rr}$** |
|---|---|---|---|---|---|---|
| SCT3040KLHR | 52 mΩ | 107 nF | 22 V | 1200 V | 122 pF | 115 nC |
| E3M0065090D | 90 mΩ | 30.4 nF | 15 V | 900 V | 60 pF | 150 nC |
| NVHL080N120SC1 | 162 mΩ | 56 nF | 20 V | 1200 V | 120 pF | 212 nC |

#### Updated inductor designs

For the inductor design, the same strategy is used that was discussed in chapter B. With the updated RMS and peak currents, the new designs are listed in table 4.6.

Table 4.6: The specifications of the three newly designed series inductors.

| **Core size** | **Number of turns n** | **Air gap length $l_g$** | **Core volume $V_e$** | **Average turn length $l_{turn}$** | **Operating point $B_{max}$** |
|---|---|---|---|---|---|
| ETD39-3F3 | 20 | 2.5 mm | 11500 mm$^3$ | 69 mm | 250 mT |
| ETD44-3F3 | 15 | 1.9 mm | 17800 mm$^3$ | 77 mm | |
| ETD49-3F3 | 12 | 1.5 mm | 24000 mm$^3$ | 85 mm | |

## 4.5. Minimum loss design

The minimum search script from section 3.2 has been updated with the new formulae for control parameters and the new current calculation method. Furthermore, the databases with different MOSFETs and inductor designs have been filled with the newly selected and designed components.
It should be mentioned that two parameters were eliminated from the minimum search script: $L_k$ and $n$. The leakage inductance and transformer turn ratio were discussed and communicated to the magnetics partner,

meaning that they could not be changed anymore. The specifications that were given are the ones from SPS modulation. Lightyear wanted to test the DAB first with SPS only. So, therefore, to keep the results of OTM modulation as realistic as possible, the same transformer and inductor design will be used as for SPS. In that way, Lightyear can implement OTM modulation without requiring a new inductor and/or transformer in the future.
The final outcome of the minimum search script for $L_k = 25\ \mu$H and $n = 6$ is summarized in table 4.7. Here, the 90 % operating region is used.

Table 4.7: Outcome of the minimum search script for the optimal modulation over the 90 % operating region.

| **Item** | **Value** |
|---|---|
| Average efficiency $\eta_{avg}$ | 98.0 % |
| Peak efficiency $\eta_{pk}$ | 98.98 % |
| Transformer turn ratio $n$ | 6 |
| Leakage inductance $L_k$ | 25 $\mu$H |
| HV MOSFET | E3M0065090D |
| Number of parallel HV MOSFETs $N_{par,HV}$ | 2 |
| LV MOSFET | SUM70030E-GE3 |
| Number of parallel LV MOSFETs $N_{par,LV}$ | 3 |
| Most efficient inductor design | ETD39-3F3 |

From a first comparison with the results for SPS modulation as given in table 3.7, it can be seen that the average efficiency of the power stage has decreased. The average efficiency went from 98.67 % to 98.0 %. The reason for this is that the optimal modulation does not optimize for ZVS region, only for minimum inductor current. However, not all operating points have a similar decrease in efficiency. For SPS modulation only, the efficiency was fairly low for high HV bus voltages as was shown in fig. 3.4. Now, the high efficiency area has been increased, but a band of lower efficiency remains within the OTM-1 modulation region, as can be seen in fig. 4.15. For a more detailed discussion of the results, the same efficiency plots and loss maps will be given for the optimal modulation as have been shown in section 3.3 for SPS modulation only.

### 4.5.1. Overall converter efficiency

First, the overall converter efficiency will be discussed. It is shown in fig. 4.15 for positive power transfer and in fig. 4.16 for negative power transfer.

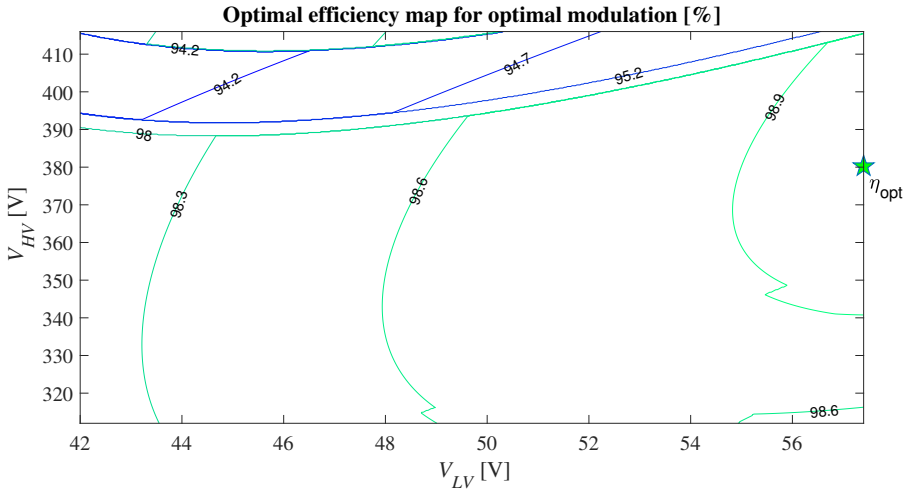



Figure 4.15: Contour plot showing the DAB power stage efficiency with optimal modulation at an output power of $P_{LV} = 2.5$ kW. The peak efficiency is depicted with a green star, which reaches 99.32 % for $V_{HV} = 375.2$ V and $V_{LV} = 57.4$ V over the 90 % operating region.

From a first observation, it can be seen that there are many visible areas throughout the contour plot. Before, with SPS modulation, only one clear line was visible, which is the line from which one of the bridges loses ZVS. However, for fig. 4.15 the lines have a different origin, namely the division between the different modulation

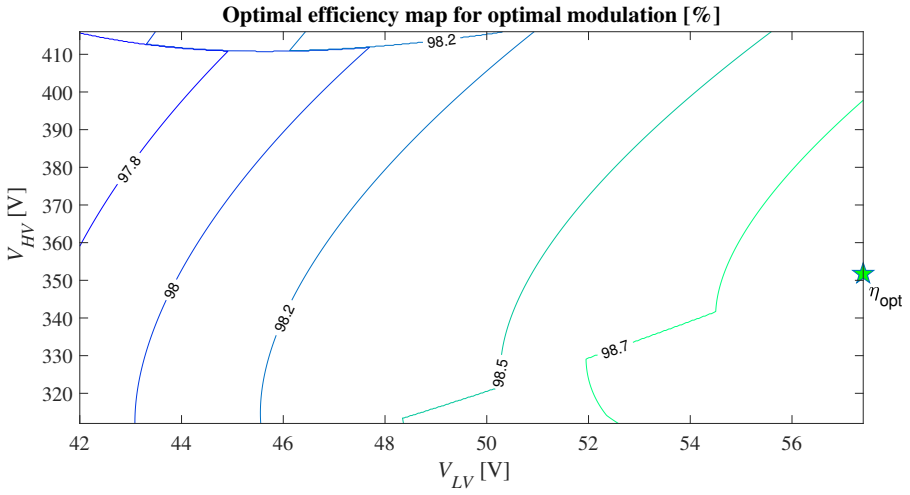



Figure 4.16: Contour plot showing the DAB power stage efficiency with optimal modulation at an output power of $P_{LV} = -2.5$ kW. The peak efficiency is depicted with a green star, which reaches 98.92 % for $V_{HV} = 351.7$ V and $V_{LV} = 57.4$ V over the 90 % operating region.

schemes. This has been made visible in fig. 4.17, where the boundaries of the modulation schemes have been made visible for positive power transfer.

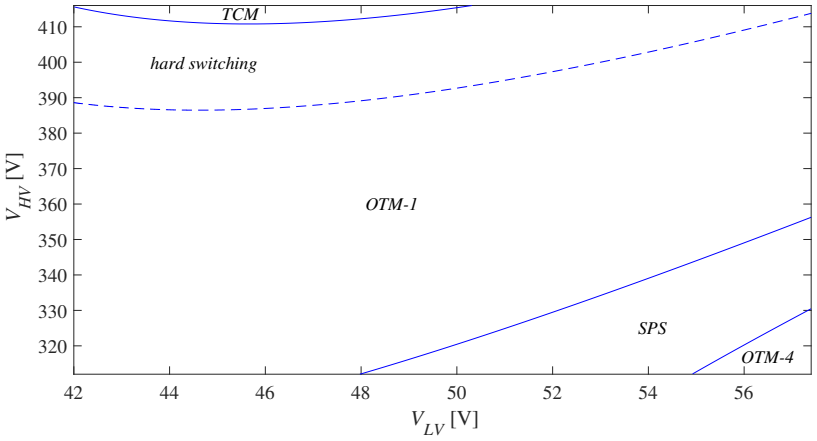



Figure 4.17: The boundaries of the different modulation schemes for $P_{LV} = 2.5$ kW.

It can be seen that for high HV bus voltages and low LV bus voltages TCM is the modulation scheme that results in lowest inductor currents. For the remaining area, OTM-1 is the dominant modulation scheme. A small band of SPS is still present, as well as a corner where OTM-4 is used.
As was mentioned before, this optimal modulation design does not optimize the ZVS region of the DAB. This can be clearly seen from the hard switching region of fig. 4.17. This hard switching band, for positive power transfer, is even larger than the one for SPS. This is one of the drawbacks of the optimal modulation strategy. Together with the fact that it is computationally heavy, as can be seen from the formulae in section A.4, makes OTM less attractive for this converter implementation.
However, when the power transfer is negative, so when power flows from the LV side to the HV side, it can be seen that there is little to no hard switching. The average efficiency for negative power using OTM is 98.34 %, as opposed to the 97.79 % for SPS modulation. So, for negative power transfer the optimal modulation outperforms SPS significantly.

### 4.5.2. MOSFET losses

When the total switch losses per bridge are plotted, fig. 4.18a and fig. 4.18b are the result.
From fig. 4.18a it can be seen that the losses in the HV switches have increased in the area where hard switch-

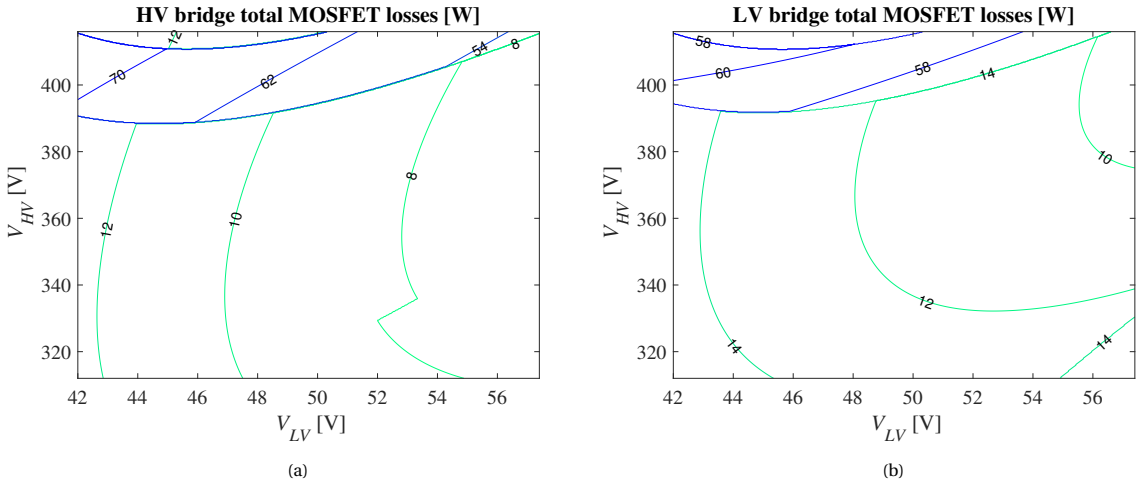



Figure 4.18: Switch losses for the optimal DAB converter design according to table 4.7 at an output power of $P_{LV}$ = 2.5 kW. (a) shows the total HV bridge losses and (b) the total LV bridge losses.

ing occurs. In the region where there is no hard switching, the switch losses are comparable to the ones of SPS modulation. Another observation is that the transition from SPS to OTM-1 is also visible in the HV switch losses plot. The same is true for the transition from OTM-1 to TCM. The change in modulation scheme leads to a decrease in switching losses, since no hard turn-on and turn-off switching occurs anymore.
For the LV bridge, the switch losses have increased too, again because of the hard switching that takes place. It can be seen that the hard switching area for the LV switches is slightly smaller than for the HV switches. This is also visible in fig. 4.15, where the line with 98 % efficiency is located. Above that line, first the HV bridge loses ZVS, leading to a small decrease in efficiency. When the input voltage is increased further, the LV bridge goes into hard switching too, thereby lowering the total converter efficiency even more.
Where for the HV bridge the transition between SPS and OTM-4 was not visible, in the switch losses plot of the LV bridge this boundary is clearly visible. The reason is that the duty cycle of the LV bridge is changed when transitioning from SPS to OTM-4, whereas the duty cycle of the HV bridge stays 0.5. In a similar way, the transition from SPS to OTM-1 is only visible in the HV bridge switch losses, since that duty cycle changes. The duty cycle of the LV bridge remains constant at 0.5.

### 4.5.3. Magnetics losses

The inductor losses have been calculated with the updated designs and are shown in fig. 4.19.

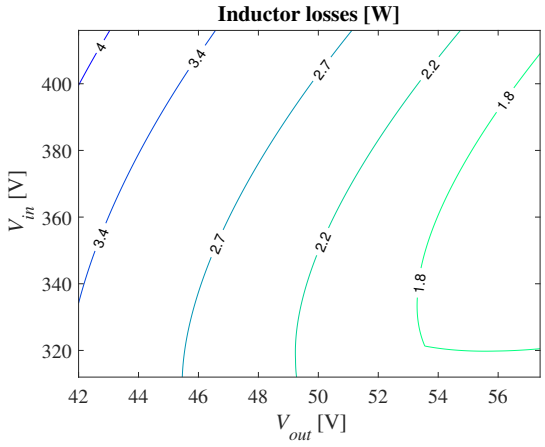
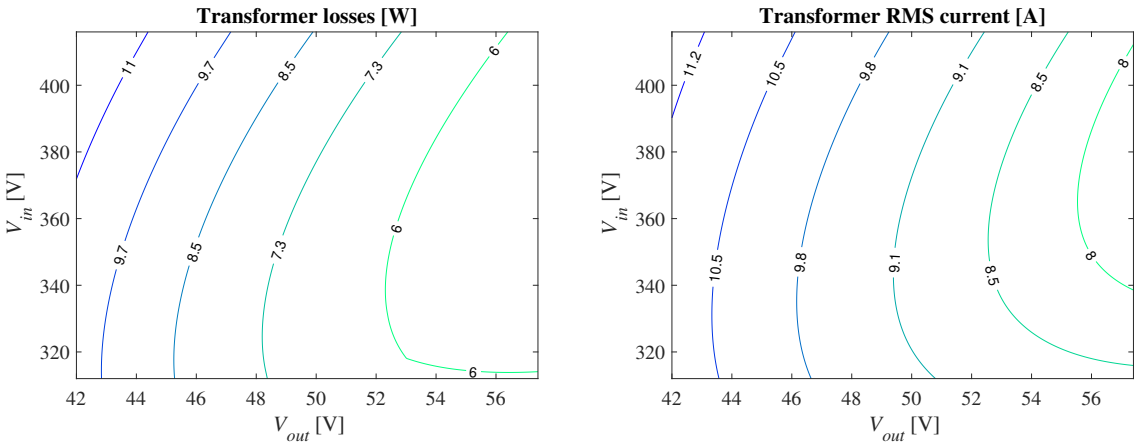



Figure 4.19: Inductor losses for the optimal DAB converter design according to table 4.7 at an output power of $P_{LV}$ = 2.5 kW.

As can be seen, the overall inductor losses are very limited. Still, the optimal modulation scheme has reduced the inductor losses significantly. In fig. 3.10 the maximum losses reached up to 5 W, for OTM the losses have

decreased by 20 % to only 4 W max. In absolute watts that might seem negligible, but in percentage the difference is substantial. This will also be visible in the transformer losses, as is shown in fig. 4.20a. Next to that, in fig. 4.20b, the RMS current through the transformer and inductor is plotted.




(a) (b)

Figure 4.20: (a) Transformer losses for the optimal DAB converter design according to table 4.7 at a power of $P_{LV} = 2.5$ kW and (b) the RMS current through the transformer for different operating points.

When comparing the RMS current through the transformer using optimal modulation to the RMS currents using SPS modulation in fig. 3.11b, it can be clearly seen that the RMS currents have been reduced by roughly 10 %. This decrease in RMS current results in a larger decrease in conduction losses, since these losses depend quadratically on the RMS current. The transformer losses have been decreased by approximately 15 % when looking at the area with high HV bus voltages and low LV bus voltages.

### 4.5.4. Conclusion

As was shown in this section, optimal modulation has some advantages and disadvantages when compared to SPS modulation. Since it is only focused at decreasing the inductor and transformer RMS currents, it does not account for ZVS capabilities. Therefore, under positive power transfer, a significant hard switching region was obtained, whereas for SPS modulation this region is smaller.
Even though for positive power SPS modulation is the preferred method, for negative power OTM outperforms SPS, as was shown in average efficiencies and by comparing fig. 3.7 to fig. 4.16. This increase in average efficiency comes at the cost of additional complexity, as well as lower performance for positive power transfer. So, SPS will be the modulation method that is used for the rest of this thesis. The efficiency requirements set by Lightyear are met using SPS, however, more performance could be achieved by implementing OTM and focusing on increasing the ZVS range under positive power transfer.

# 5

# Control of the DAB Converter

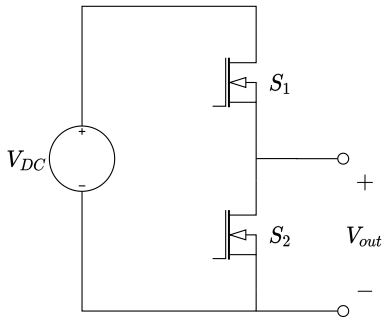
With a thorough investigation of the DAB converter in place, the control has to be written. To this end, first a converter model has to be derived that models the dynamic behavior of the DAB converter. This model will be used to design a controller that controls the power at any given operating condition. The dynamic model of the DAB is discussed in section 5.1 after which the controller implementation is given in section 5.2. Finally, in section 5.3 the derived controller is simulated, tuned and the results are shown. In this chapter, SPS modulation is used to operate the converter, which will simplify the derivation and analysis of the model. SPS modulation has excellent performance and simplicity compared to the optimal modulation as derived in chapter 4.

## 5.1. Dynamic DAB model

The DAB converter operation as discussed in section 2.2.2 is not yet presented in a way that control can be written for it. To this end, the dynamic behavior of the DAB should be derived. In literature, there are generally two groups of dynamic modelling present: models with state-space averaging and models with a fundamental power flow analysis [43].
With state-space averaging, the different states of the power converter are analysed and eventually averaged into one state-space model. In literature, many examples of such dynamic models can be found [44–46]. The main difference between the presented models is what state variables are used for the model. The lack of proper explanation why those specific variables have been used makes the presented models difficult to compare. Additionally, the models are computationally complex when the accuracy of the model needs to be high.
The alternative, fundamental power flow analysis, results generally in less complex models. To get to the model, the assumption is made that the fundamental components of waveforms inside the converter are sufficient to create a dynamic model. The higher order harmonics are disregarded and considered not to contribute to the operation of the converter. Thus, the model will lack accuracy, especially across a large variation in operating conditions (input and output voltages in the case of the DAB).
In this thesis, a different strategy is followed, as is presented in [43]. The dynamic model that will be derived is based on the different harmonics present in the converter. Generally, it follows the derivation of fundamental power flow analysis, however, there is the option to easily include more or less harmonics to tune the accuracy and complexity. To obtain this model, first the DAB converter operation has to be written in terms of harmonics, using the Fourier transform. Then, the relevant number of harmonics is investigated and validated.

### 5.1.1. Harmonic model of the DAB converter

The basis of the operational principle of the DAB converter can be built around the switching patterns of the full bridges, which creates a voltage over the transformer leakage inductance. In turn, a current will be induced which eventually leads to power being transferred between the bridges. First, a single switching leg is investigated, which can then be extended to the full bridges of the DAB. A schematic representation of a switching leg is shown in fig. 5.1a.




(a) Schematic of a switching leg.

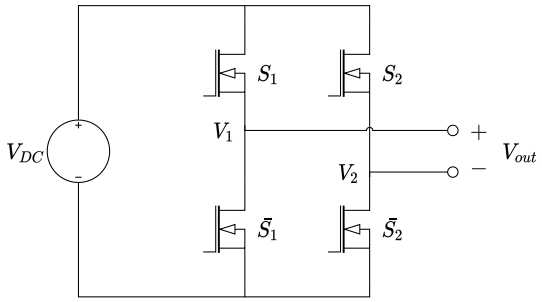
| $S_1$ | $V_{out}$ |
|---|---|
| 0 | 0 |
| 1 | $+V_{DC}$ |

(b) Switching state table of the single leg.

Figure 5.1: Schematic representation and switching table of a single switching leg.

The switches in a single leg are switched complementary, meaning that when the top switch $S_1$ is closed, the bottom switch $S_2$ will be opened. The output of the switching leg, $V_{out}$, will thus change between $+V_{DC}$ and 0 V. Since the bottom switch will always switch complementary to the top switch, the behavior of the complete switching leg can be simplified by only considering the switching pattern of the top switch $S_1$. This can be summarized in a table, as shown in fig. 5.1b.

Now, the single leg can be extended with another single leg, creating four possible states, which can be seen in fig. 5.2a and fig. 5.2b, respectively. There, the figure and table have been simplified by substituting the bottom switches by the inverted signal of the top switch.




(a) Schematic of a full bridge.

| $S_1$ | $S_2$ | $V_1$ | $V_2$ | $V_{out}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | $+V_{DC}$ | $-V_{DC}$ |
| 1 | 0 | $+V_{DC}$ | 0 | $+V_{DC}$ |
| 1 | 1 | $+V_{DC}$ | $+V_{DC}$ | 0 |

(b) Switching state table of the full bridge.

Figure 5.2: Schematic representation and switching table of a single switching leg.

Now, the table of fig. 5.2b can be simplified into one formula:

$$V_{out} = V_{DC} \cdot \{S_1 - S_2\}, \tag{5.1}$$

where $S_1$ and $S_2$ are the logic signals, representing the states of the switches of the corresponding switching leg. Now, the logic function can be extended to include time into the equation. With time added, one formula can describe the complete function of the full bridge. First, the switching states are redefined as:

$$S_k(t) \in \{0,1\}, \text{ where } k = 1,2,... \tag{5.2}$$

The output of the full bridge can now be described as

$$v_{out}(t) = V_{DC} \cdot \{S_1(t) - S_2(t)\}. \tag{5.3}$$

With this expression for the output voltage of a full bridge, the voltages across the leakage inductor of the DAB converter can be expressed. The simplified circuit of the DAB converter is repeated here for convenience in fig. 5.3, where the transformer is added as well.

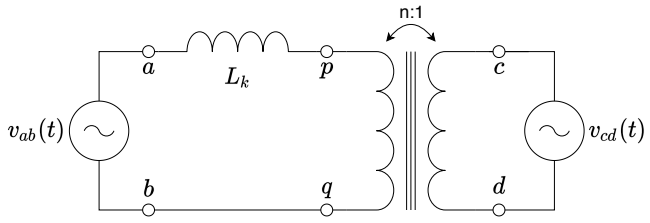



Figure 5.3: Simplified circuit of the DAB converter.

Using the same convention as fig. 5.3, the voltage over the complete transformer (including leakage inductance) can be described as:

$$\begin{aligned} v_{ab}(t) &= v_{HV}(t) \cdot \{S_1(t) - S_2(t)\} \\ v_{cd}(t) &= v_{LV}(t) \cdot \{S_3(t) - S_4(t)\} \end{aligned} \tag{5.4}$$

Here, the full bridge on the LV side is made up of half bridges $S_3$ and $S_4$. In order to facilitate a power transfer from one bridge to the other, the waveforms of $v_{ab}(t)$ and $v_{cd}(t)$ are phase shifted.
Now that the principle operation is described in appropriate terms, the dynamic equations describing the behavior of the DAB can be derived. For now, only positive power transfer is considered, which means that the HV bus is seen as input and the LV bus as output. The exact same derivation can be followed for negative power transfer.

First, the output capacitor behavior is of interest, since it is an important part of the dynamic equations. Its voltage can be described as

$$\frac{dv_{LV}(t)}{dt} = \frac{i_C(t)}{C_{LV}}. \tag{5.5}$$

To determine the capacitor current, a current loop is evaluated at the LV bus, resulting in:

$$i_C(t) = i_{LV}(t) - i_{LVbus}(t), \tag{5.6}$$

where $i_{LV}(t)$ is the current flowing from the LV full bridge to the LV capacitors and $i_{LVbus}(t)$ is the current flowing to the LV bus, or in this case the output current. This current is measurable by a current sensor, but the current before the output capacitors, $i_{LV}(t)$, is not. It is dependent on the switching states of the LV bridge as well as the current through the leakage inductor. Therefore, it can be calculated, since it simply follows the amplitude of the inductor current, as has been summarized in table 5.1.

Table 5.1: Switching state table for $i_{LV}(t)$.

| $\mathbf{S_3}$ | $\mathbf{S_4}$ | $\mathbf{i_{LV}(t)}$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | $-i_{L_k}(t)$ |
| 1 | 0 | $+i_{L_k}(t)$ |
| 1 | 1 | 0 |

Now, using the table, an expression for the currents can be made:

$$i_{LV}(t) = i_{L_k}(t) \cdot \{S_3(t) - S_4(t)\}. \tag{5.7}$$

Next, an expression for the inductor current $i_{L_k}(t)$ has to be derived, which is done using a Kirchoff voltage loop (KVL) in fig. 5.3, where the internal resistance of the leakage inductor is also taken into account:

$$v_{ab}(t) - n \cdot v_{cd}(t) - R_{L_k} \cdot i_{L_k}(t) - L_k \frac{di_{L_k}}{dt}(t) = 0. \tag{5.8}$$

Since the switching functions are described as instantaneously changing signals, the resulting system description of eq. (5.8), which is continuous, forms a mixed-mode dynamic system. Such a system consists of both continuous and discrete signals and is complex to solve and interpret.

To overcome this issue, the discrete switch equations, as defined by eq. (5.2), can be expressed into Fourier series using a Fourier transform. By doing so, the switching functions are made continuous and the expression of the dynamic operation of the DAB converter can be easily solved.
The Fourier series of a waveform is essentially the summation of the dominant waveform at a certain fundamental frequency together with its harmonics. In mathematical terms, any signal can be expressed as a series of sinusoids as [6]:

$$f(x) = \frac{a_0}{2} + \sum_{k=1}^{\infty} \{a_k \cos(kx) + b_k \sin(kx)\}, \tag{5.9}$$

where $a_k$ and $b_k$ are the harmonic coefficients and are expressed as:

$$a_k = \frac{1}{\pi} \int_{-\pi}^{\pi} f(x) \cos(kx)\, \mathrm{dx},\ k \geq 0 \tag{5.10a}$$

$$b_k = \frac{1}{\pi} \int_{-\pi}^{\pi} f(x) \sin(kx)\, \mathrm{dx},\ k \geq 1. \tag{5.10b}$$

Using the Fourier transform on a square wave signal with 50 % duty cycle and an amplitude of 1 results in [47]:

$$S_i = \frac{1}{2} + \frac{2}{\pi} \sum_{k=0}^{\infty} \frac{\sin\left([2k+1]\{\omega_s t - \alpha_i\}\right)}{[2k+1]},\ i = 1,2,3... \tag{5.11}$$

where $\omega_s$ is the switching frequency of the switch in radians per second and $\alpha_i$ is the delay of the phase of the waveform with respect to a reference waveform.
According to the Fourier theory, if more harmonics are added to the summation, the resulting Fourier series representation will get closer to the original signal. This has been made visible in fig. 5.4, where more harmonics result in a better match with the ideal square wave.

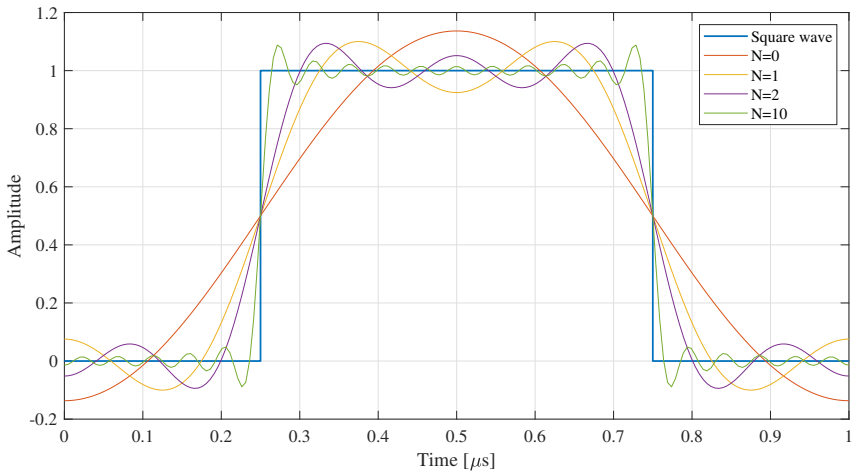



Figure 5.4: Ideal square wave signal approached by Fourier series with different number of harmonics.

Now, each switching signal can be written in the same form as eq. (5.11). Additionally, the infinite summation has been replaced by a finite summation that includes $N$ harmonics. The results from eq. (5.11) give rise to the idea that the waveforms can be approximated accurately enough by only including $N$ harmonics. This results in:

$$S_1 = \frac{1}{2} + \frac{2}{\pi} \sum_{k=0}^{N} \frac{\sin\left([2k+1]\{\omega_s t\}\right)}{[2k+1]} \tag{5.12a}$$

$$S_2 = \frac{1}{2} + \frac{2}{\pi} \sum_{k=0}^{N} \frac{\sin\left([2k+1]\{\omega_s t - \pi\}\right)}{[2k+1]} \tag{5.12b}$$

$$S_3 = \frac{1}{2} + \frac{2}{\pi}\sum_{k=0}^{N}\frac{\sin\left([2k+1]\{\omega_s t-\varphi\}\right)}{[2k+1]} \tag{5.12c}$$

$$S_4 = \frac{1}{2} + \frac{2}{\pi}\sum_{k=0}^{N}\frac{\sin\left([2k+1]\{\omega_s t-\varphi-\pi\}\right)}{[2k+1]}, \tag{5.12d}$$

where $\varphi$ is the phase shift between the two bridges of the DAB converter in radians.

### 5.1.2. Number of included harmonics

As shown before, the square wave as produced by the switches can be approximated by the Fourier series, which includes up to $N$ harmonics. There is a trade-off to be made between the complexity of the final dynamic model and the accuracy of the model. Including more harmonics will lead to a better representation of the actual signal, however, the complexity of the dynamic model will increase. For that reason, the optimal number of harmonics will be investigated in this section.

Since the main objective of the DAB converter as designed in this thesis is to transfer a certain amount of power, the accuracy of the model is validated by looking at the transferred power. The power transfer between the two full bridges of the DAB can be expressed in a similar summation of harmonics as the switches. Then, the transferred power for $N$ included harmonics can be compared to the actual transferred power. The number of relevant harmonics will be increased up till the point that the accuracy of the dynamic model is high enough to be used, without getting too complex.

To start, first the voltages across the transformer terminals, $v_{ab}(t)$ and $v_{cd}(t)$, need to be expressed in harmonics. The switching functions of eq. (5.12) can be used for this, which can be substituted into eq. (5.4), leading to:

$$v_{ab}(t) = V_{HV}\cdot\frac{4}{\pi}\sum_{k=0}^{N}\frac{\sin\left([2k+1]\{\omega_s t\}\right)}{[2k+1]} \tag{5.13}$$

$$v_{cd}(t) = V_{LV}\cdot\frac{4}{\pi}\sum_{k=0}^{N}\frac{\sin\left([2k+1]\{\omega_s t-\varphi\}\right)}{[2k+1]}. \tag{5.14}$$

For an inductive transmission line, connected to two voltage sources on each end, the power transfer is given as [6]:

$$P_{transfer} = \frac{V_1 V_2 \sin(\delta)}{\omega L}, \tag{5.15}$$

where $V_1$ and $V_2$ are the RMS voltages of the sinusoidal voltage sources, $\delta$ is the phase difference between the waveforms and $L$ is the line inductance of the transmission line. For the DAB converter the exact same transmission principle applies, since it consists of similar voltage sources, connected through an inductive connection. For the DAB that inductive connection is formed by the leakage inductance of the transformer. Taking the RMS voltage of eq. (5.13) and eq. (5.14) and combining it with eq. (5.15), results in:

$$P_{DAB,harmonics} = \frac{8}{\pi^2}\frac{nV_{HV}V_{LV}}{\omega_s L_k}\sum_{k=0}^{N}\left\{\frac{1}{[2k+1]}\frac{1}{[2k+1]}\frac{\sin\left([2k+1]\varphi\right)}{[2k+1]}\right\}, \tag{5.16}$$

where $n$ is the transformer turn ratio. Now, to determine the power transfer accuracy for a certain $N$ amount of harmonics, the computed power is compared to the analytical expression for power transfer as was given by eq. (2.2), which is repeated here for convenience:

$$P_{DAB,analytical} = \frac{nV_{HV}V_{LV}}{2\pi^2 f_s L_k}\varphi\left(\pi-\varphi\right). \tag{5.17}$$

The resulting transferred power difference for a given HV bus voltage, LV bus voltage, leakage inductance, switching frequency and phase shift are given in table 5.2.

Table 5.2: Difference in computed power transfer between the analytical expression of eq. (5.17) and the harmonics expression of eq. (5.16).

| Number of harmonics $N$ | Difference in power |
|---|---|
| 0 | -3.66 % |
| 1 | 0.81 % |
| 2 | -0.28 % |
| 3 | -0.12 % |
| 4 | -0.08 % |
| 5 | 0.03 % |

From the results of table 5.2 it can be seen that for $N = 3$ a point of diminishing returns is achieved. Increasing the number of significant harmonics further will result in a insignificant increase in accuracy, at the cost of more complexity. An error of 0.12 % in power, which corresponds to 3 W at its operating power of 2500 W, is determined to be negligible. Therefore, the number of included harmonics will be $N = 3$.

### 5.1.3. Final harmonic model

With the number of harmonics in place, the complete model can be constructed. First, the switching functions of eq. (5.12) have to be substituted into the converter equation given by eq. (5.8), which has been extensively described in [43]. Rearranging the terms and solving for the derivative of the LV bus voltage results in:

$$\frac{dv_{LV}(t)}{dt} = -i_{LVbus}(t) + \frac{8n}{C_{LV}\pi^2}\sum_{k=0}^{N}\frac{1}{[2k+1]^2}\frac{V_{HV}}{|Z[k]|}\left\{\cos\left([2k+1]\varphi - \theta_z[k]\right) - \frac{nv_{LV}(t)}{|Z[k]|}\cos\left(\theta_z[k]\right)\right\}, \tag{5.18}$$

where $Z[k] = \sqrt{R_{L_k}^2 + ([2k+1]\omega_s L_k)^2}$, which is the magnitude of the (AC) impedance, and where $\theta_z[k] = \text{atan}\left(\frac{[2k+1\omega_s L_k}{R_{L_k}}\right)$, which is the phase of the AC impedance between the two DAB full bridges.
This non-linear model still needs to be linearized such that a state-space model can be created. This linearization is done around the typical operating point to which a small disturbance is added. In this case, the change in LV bus voltage is determined based on its current LV bus voltage, LV bus current and phase shift. Linearization leads to [48]:

$$\frac{d\left(V_{LV_0} + \Delta V_{LV_0}(t)\right)}{dt} \approx f\left(V_{LV_0}, \varphi_0, I_{LVbus_0}\right) + \left.\frac{\partial f}{\partial V_{LV}}\right|_0 \Delta V_{LV}(t) + \left.\frac{\partial f}{\partial \varphi}\right|_0 \Delta\varphi(t) + \left.\frac{\partial f}{\partial I_{LVbus}}\right|_0 \Delta I_{LVbus}(t) \tag{5.19}$$

Solving these partial differential equations gives the final linearized model [43]:

$$\frac{d\Delta V_{LV}(t)}{dt} = A\Delta V_{LV} + B_\varphi \Delta\varphi + B_i \Delta I_{LVbus} \tag{5.20a}$$

$$A = -\frac{8n^2}{C_{LV}\pi^2}\sum_{k=0}^{N}\frac{\cos\left(\theta_z[k]\right)}{[2k+1]^2\,|Z[k]|} \tag{5.20b}$$

$$B_\varphi = \frac{8nV_{HV}}{C_{LV}\pi^2}\sum_{k=0}^{N}\frac{\sin\left(\theta_z[k] - [2k+1]\varphi_0\right)}{[2k+1]\,|Z[k]|} \tag{5.20c}$$

$$B_i = \frac{-1}{C_{LV}} \tag{5.20d}$$

Note that the change in LV bus current $\Delta I_{LVbus}$ is seen as a disturbance, whereas $\Delta V_{LV}$ is chosen as the state variable and $\Delta\varphi$ functions as the input of the model.

The importance of the correct choice of the number of included harmonics can be proven once again. The calculation of the $B_\varphi$ term changes with changing phase shift $\varphi$. This has been made visible in fig. 5.5, where it is shown that higher order harmonics still contribute to the converter operation.

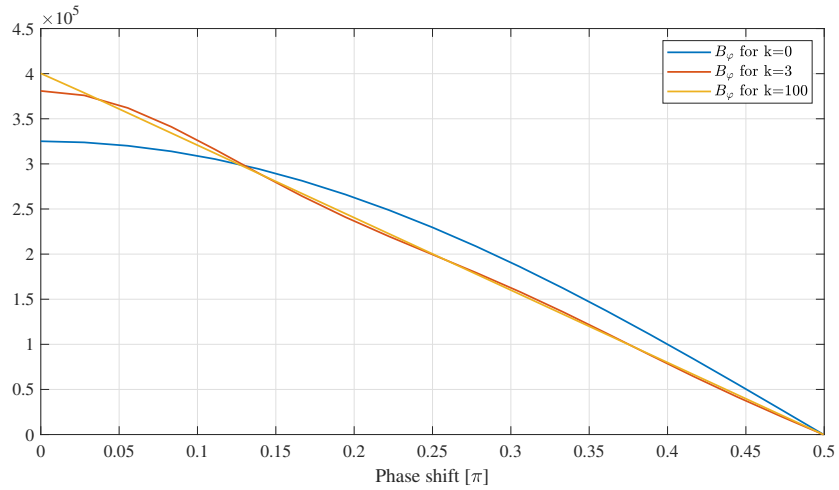



Figure 5.5: Influence of the higher order harmonics on the $B_\varphi$ term for changing phase shift $\varphi$.

Another conclusion that can be drawn from fig. 5.5, is that the model will only be accurate around its linearization point at a given phase shift ($\varphi_0$). For a small step change in the phase shift, the model will closely resemble the real converter, however, for large variations in the phase shift, the model becomes inaccurate.

## 5.2. Controller implementation

With the model of the DAB converter in place, the controller design can be created. The controller will have one parameter that it can adjust, which is the phase shift in case of SPS modulation. The goal of the controller is to obtain a certain constant power output of the DAB converter, given any operating point. Since on both ends of the DAB converter a battery is placed, the voltage of the HV bus and LV bus is given. In order to be able to transfer power, the voltage of that bus should be increased slightly over the steady state voltage of the battery. In that way, the battery will be charged and thus power is transferred. Again, only the positive power transfer is described. Because of the symmetry of the DAB converter, the exact same steps can be taken to design the controller for negative powers.
With this descriptive analysis in place, it becomes clear that the controller can be simply implemented by a closed loop negative feedback design. The output voltage has to be measured and can be fed back to the input of the controller, which will adjust its outputs to the plant accordingly. This closed loop system is shown in fig. 5.6.

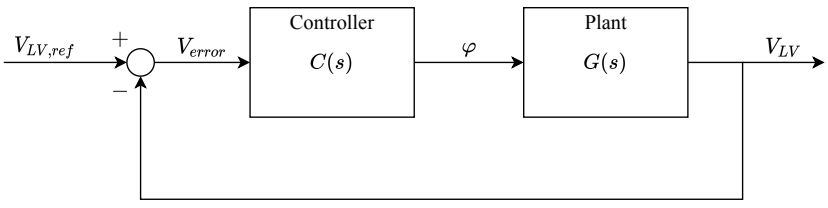



Figure 5.6: Schematic representation of a closed-loop controller implementation.

As can be seen, a certain voltage reference for the LV bus is given at the input. Then, the current output voltage is subtracted from it, feeding the voltage error into the controller. The controller will adjust the phase shift $\varphi$ as such that the LV bus voltage will converge towards the reference voltage.
So far, no reference voltage is known yet, since the converter has to operate based on a power setpoint. Therefore, a slightly different approach is followed in this thesis, which makes use of the reference power and actual power output of the converter. Then, that power error is divided by the expected LV bus current, which results in the voltage error on the output of the converter. This has been made visible in fig. 5.7.

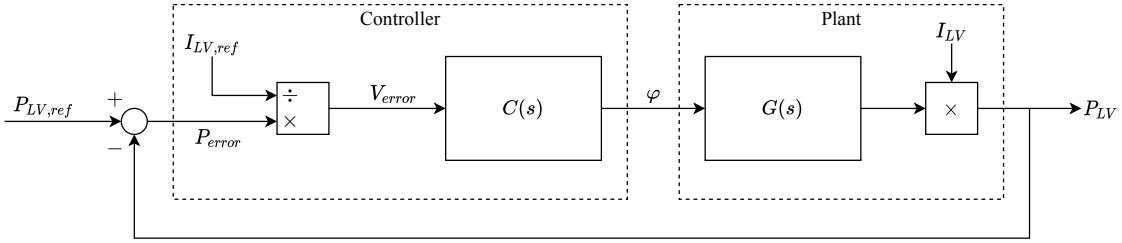



Figure 5.7: Schematic representation of the implemented closed loop system.

As can be seen, the control loop of fig. 5.6 has been altered to be able to control the DAB based on its power output. The reference current $I_{LV,ref}$ is obtained by dividing the reference power $P_{LV,ref}$ by the battery voltage. This leads to a theoretical current that should be obtained to transfer the desired power into the battery. The actual regulating part of the controller, $C(s)$ in fig. 5.7, is implemented using a PI-controller. The PI-controller is deemed sufficient since the derived DAB model of section 5.1 is a first order SISO system. The integrating part of the controller is required to reduce the steady state error to zero. Finally, a saturation block is added to prevent the phase shift of becoming too large. The limits for the saturation are $-\frac{1}{2}\pi$ and $+\frac{1}{2}\pi$. The implementation of the controller can be seen in fig. 5.8.

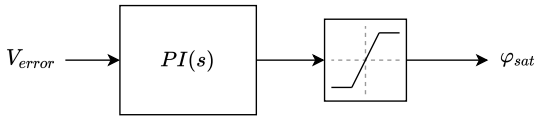



Figure 5.8: Implementation of the regulator $C(s)$, using a PI-controller and saturation block.

## 5.3. Tuning of the controller

Now that the controller has been designed, it should be tuned. First, to get an indication of the PI controller tuning, the derived DAB models will be simulated and roughly tuned using the automatic Simulink PID Tuner App. Then, a functional model of the designed DAB converter will be build, on which the controller will be validated and fine-tuned. The simulation time for the full model will be extremely long compared to the simple model that will be derived in this section. The complexity of all the switching actions and parasitics makes it good practice to get an initial tuning using the model as derived in section 5.1.3.

### 5.3.1. Initial tuning of the PI controller

For the tuning, first the DAB model has to be made. This has been done by calculating the converter parameters as given by eq. (5.20) using the parameters of table 5.3.

Table 5.3: DAB converter parameters for the calculation of the DAB model for positive power transfer.

| Parameter | Value |
|---|---|
| $N$ | 3 |
| $V_{HV}$ | 378 V |
| $f_s$ | 100 kHz |
| $L_k$ | 25 $\mu$H |
| $R_{L_k}$ | 20 m$\Omega$ |
| $n$ | 6 |
| $\varphi_0$ | 0.136 $\pi$ |
| $C_{HV}$ | 360 $\mu$F |
| $A$ | -6.66 |
| $B_\varphi$ | $2.90 \cdot 10^5$ |
| $B_i$ | $-2.78 \cdot 10^3$ |

The resulting parameters for the positive power transfer model can now be put into a transfer function. To do so, a Laplace transform has to be applied to eq. (5.20). For simplicity, the influence of the load current change

$\Delta I_{LVbus}$ will be left out of the equation, since that greatly simplifies the design of the controller. The load disturbance contribution, weighted by $B_i$, is accounting for sudden load disturbances. For this DAB converter, both ends of the converter terminals will be connected to batteries. This means that the converter will not face abrupt load changes, since the batteries will provide the required power. This validates the removal of the $B_i$ term for an initial PI tuning. However, for a converter design where no batteries are present to compensate for sudden load disturbances, this $B_i$ term cannot be omitted. The PI controller cannot respond quickly enough to provide the necessary energy during an abrupt load change. Therefore, either the output capacitor banks should be made sufficiently large to counter the first voltage spike or sag, or the controller should be adjusted to counter for sudden load changes. This can, for instance, be done by using a feed-forward path for the load current disturbance, as presented in [43].
Applying the Laplace transform to eq. (5.20) results in:

$$s \cdot \Delta V_{LV}(s) = A\Delta V_{LV}(s) + B_\varphi \Delta\Phi(s). \tag{5.21}$$

Rearranging the terms gives the plant transfer function

$$G(s) = \frac{\Delta V_{LV}(s)}{\Delta\Phi(s)} = \frac{B_\varphi}{s - A}. \tag{5.22}$$

In Simulink, a closed loop model has been built according to fig. 5.6. A reference voltage is given to the model, which the PI controller tries to regulate to. The set-up can be seen in fig. 5.9.

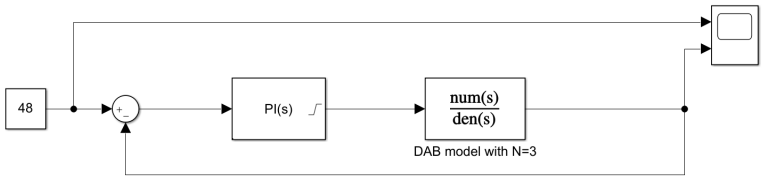



Figure 5.9: Implementation of the PI tuning loop.

The automatic tuner of Simulink is set to reach steady state within 5 ms when applying a step function. This 5 ms is required for the DAB converter to be able to quickly respond to little variations in voltage on the bus. Even though the batteries will stabilize most of the transients, the bus voltage will still change when, for example, the motors are regenerating and store the energy into the batteries. Such voltage fluctuations might introduce an unwanted nonzero transformer current if not handled appropriately. This can lead to saturation, which should avoided to ensure proper behavior of the converter and prevent damage to the components.
After the automatic tuning the resulting PI parameters are $K_{p,pos} = 3.0 \cdot 10^{-3}$ and $K_{i,pos} = 1.7$, with the corresponding step response as shown in fig. 5.10.

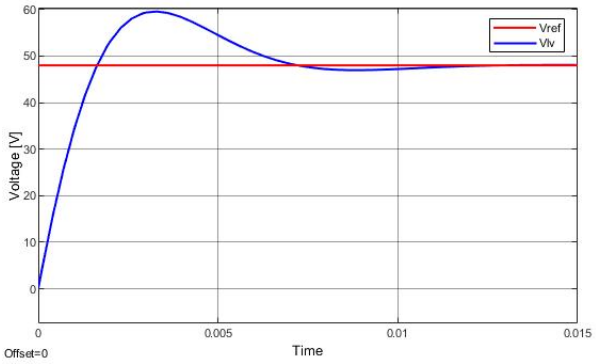



Figure 5.10: Start-up response of the converter model for positive power transfer.

It can be seen that there is an overshoot, which will be fine-tuned in the complete converter model. A small overshoot is allowed, however, care should be taken not to damage any of the components.
The exact same procedure has been followed for the negative power direction, where the resulting PI variables are $K_{p,neg} = 5.4 \cdot 10^{-3}$ and $K_{i,neg} = 0.5$.

### 5.3.2. Fine-tuning of the PI controller

With the initial tuning of the converter in place, the full-scale DAB model is built to finalize and verify the tuning of the PI controller. It has been built in Simulink according to the components as chosen in section 3.3, which can be seen in fig. 5.11.

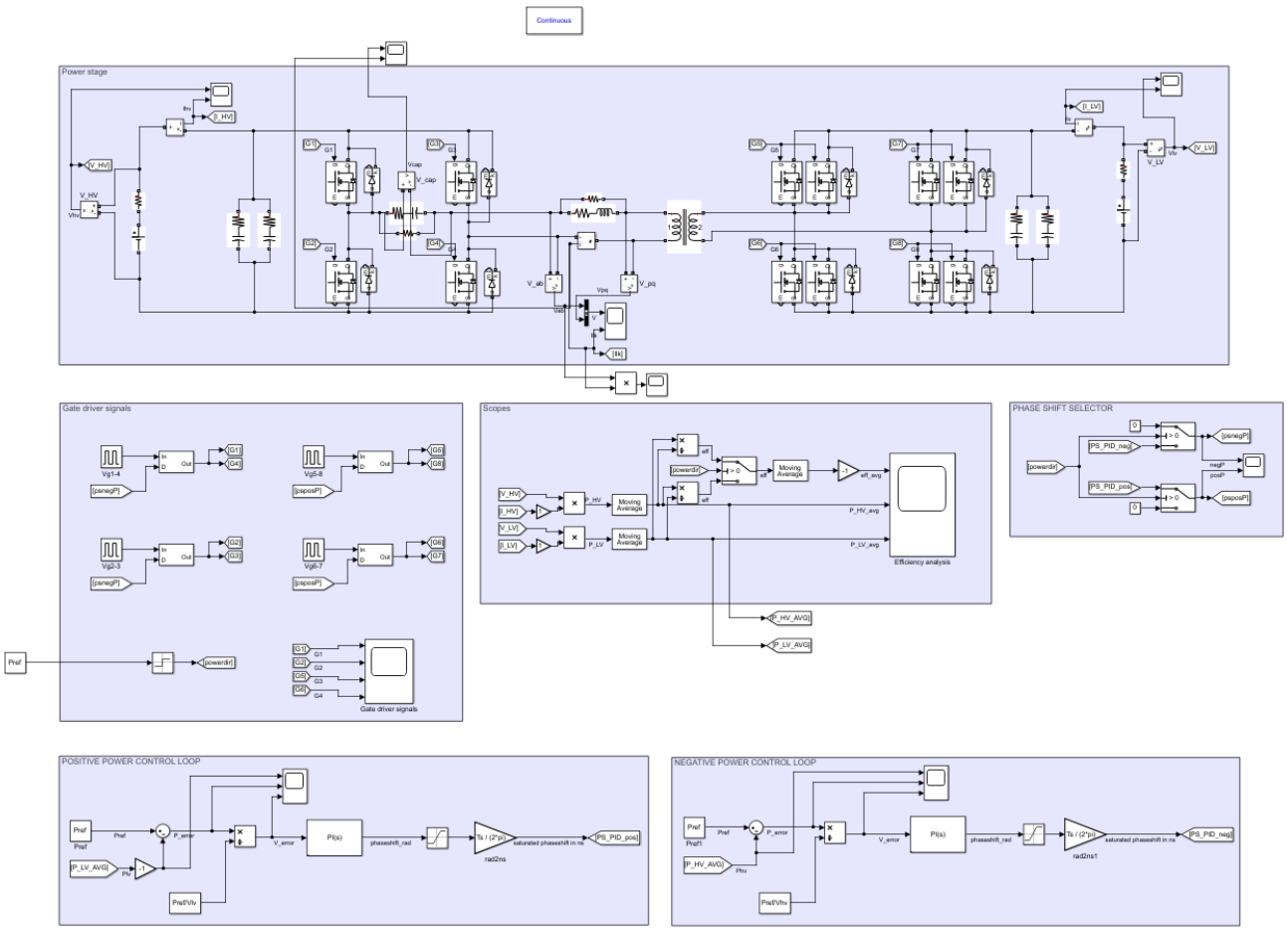



Figure 5.11: Implemented Simulink model of the designed DAB converter with control loop.

A reference power is given as an input for the model, which is set to 2500 W. Then, depending on the direction of the desired power transfer, either the positive power control loop or the negative power control loop is activated. The phase shift from either of the two is given to the corresponding gate drivers, which will then lead to a change in power of the complete converter.

To simulate the eventual behavior of the microcontroller which will control the DAB, a discrete implementation of the control loop has been made. The frequency of the control loop is set at 1 kHz, which is a good middle ground between processor load and converter operation. This analysis has been carried out by an external company, which writes the software for the microcontroller for Lightyear. They did the analysis for the microcontroller that will be equipped for the prototype of this converter, which is the S32K144 of NXP. They calculated a microcontroller utilization of 23 % with the control loop operating at 1 kHz. This leaves enough overhead to schedule other tasks, such as communication, sensor readout etc. A lower control loop frequency will result in slower response of the converter with less computational load for the microcontroller. However, the slower dynamic response of the converter results in poor transient behavior.

Another effect that should be taken into account is the discrete steps in phase shift that the microcontroller can realize. The microcontroller its clock frequency of 80 MHz means that it can realize up to 800 steps in one switching cycle. Thus, the minimum step size for a phase shift it can realize is 12.5 ns. As a safety factor and to leave some headroom for the microcontroller, a factor 4 is applied, which limits the minimum phase shift step to 50 ns. This has been implemented in the discrete time step block in the detailed converter model as seen in fig. 5.11.

The response of the final converter implementation has been tuned to provide a fast response to changes without any overshoot, as can be seen in fig. 5.12 for positive power and in fig. 5.13 for negative power.

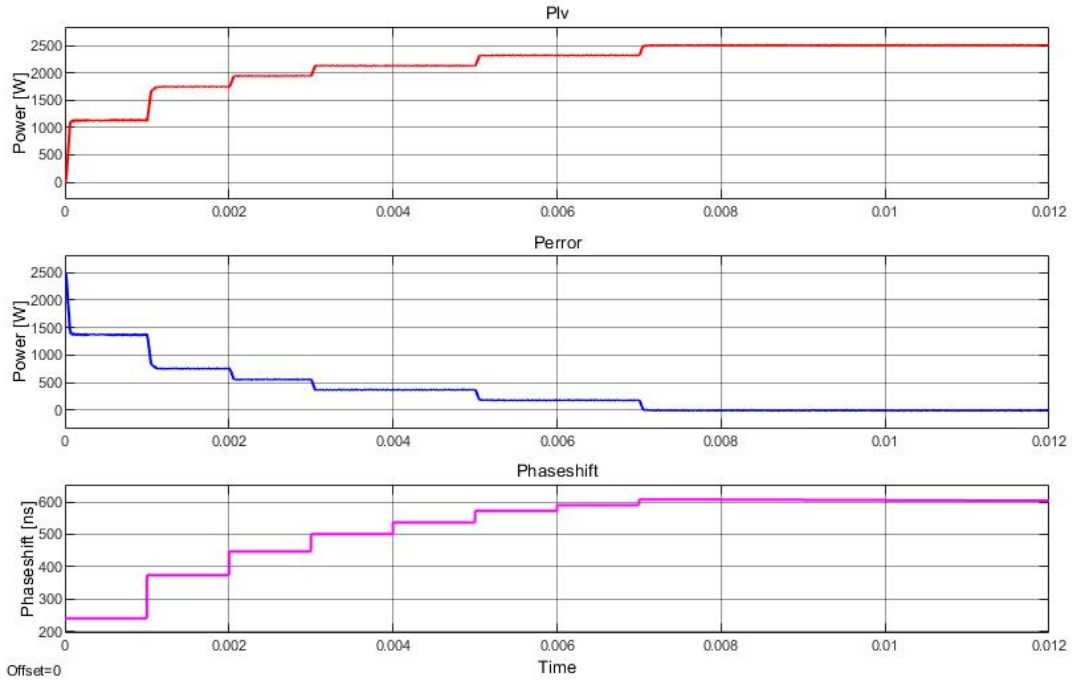



Figure 5.12: Start-up behavior of the DAB converter for $P = 2.5$ kW, $V_{HV} = 378$ V, $V_{LV} = 50.4$ V, $K_{p,pos} = 3 \cdot 10^{-3}$ and $K_{i,pos} = 3$.

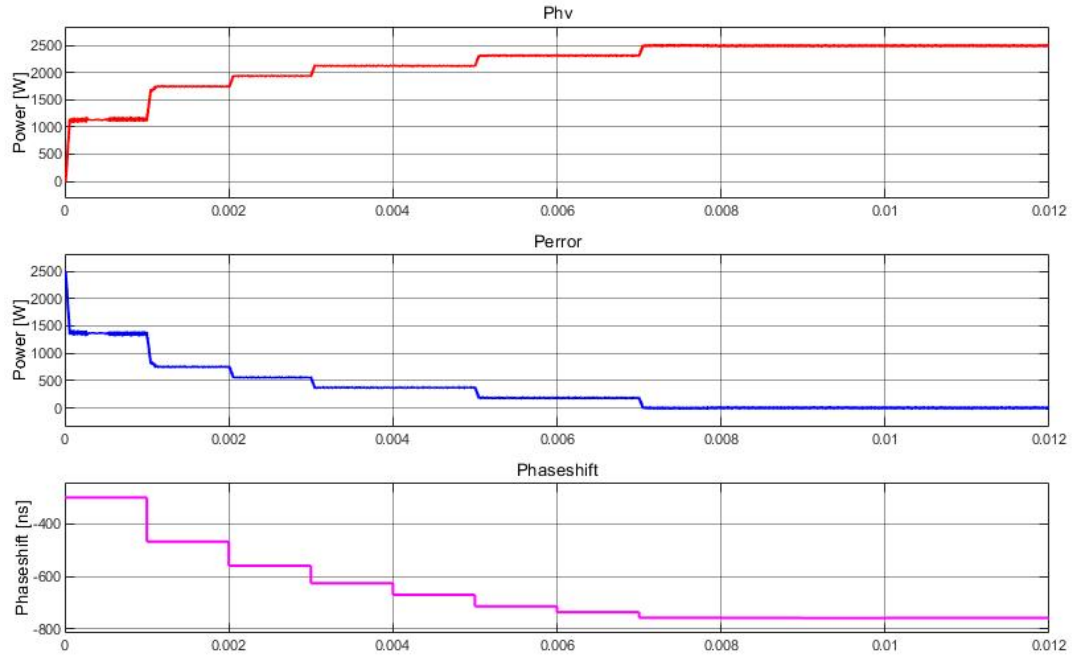



Figure 5.13: Start-up behavior of the DAB converter for $P = -2.5$ kW, $V_{HV} = 378$ V, $V_{LV} = 50.4$ V, $K_{p,neg} = \cdot 10^{-4}$ and $K_{i,neg} = 0.5$.

As can be seen from the figures, the power out of the converter reaches the target without overshoot within 7 ms. Since the converter is designed to deliver 2.5 kW of power, overshoot may put too much stress on components. Therefore, the initial PI parameters have been changed until the desired response was achieved. Without the initial tuning parameters, time consuming trial-and-error tuning would have been necessary,

since the automatic tuning tool does not work for the full-scale implementation. The new controller parameters are given in table 5.4.

Table 5.4: Final PI controller parameters for positive (subscript pos) and negative (subscript neg) power direction.

| **Parameter** | **Value** |
|---|---|
| $K_{p,pos}$ | $3 \cdot 10^{-3}$ |
| $K_{i,pos}$ | 3 |
| $K_{p,neg}$ | $5 \cdot 10^{-4}$ |
| $K_{i,neg}$ | 0.5 |

## 5.4. Conclusion

In this chapter a model has been derived to describe the dynamic behavior of the DAB converter. Afterwards, the model was used to provide initial tuning for a controller design, which was implemented using a PI controller, with separate control loop for different power directions. Finally, the controller performance was fine-tuned and eventually verified using a detailed Simulink model of the designed DAB converter.

# 6

# Conclusion and recommendations

The goal as stated at the beginning of this thesis was to investigate, design, simulate and build a prototype of an isolated bidirectional DC-DC converter for an automotive application. The most important design criteria was to have the design optimized with respect to efficiency, one of the key components in the development of the Lightyear One. One peculiarity of the converter requirements was that it had to be optimized for one specific power level.

With the goal of having an average efficiency of at least 94 % over all operating points for the 90 % operating region, first a topology study was performed. Here, all converters that satisfied the requirements were listed and compared. Eventually, the three most promising candidates have been selected, which were the dual active bridge converter, the LLC resonant full bridge converter and a two stage converter with a buck-stage at the HV side. These three candidates were then analyzed further, explaining the operating principle and showing their advantages and disadvantages. A specific focus was placed on the regions where zero voltage switching could be achieved. It was shown that the DAB converter was the best topology given the requirements and operating conditions for the converter design. A small adjustment was added to the original DAB topology, which was the addition of a DC blocking capacitor in series with the leakage inductance of the transformer. In that way, potential saturation of the transformer will be prevented when there is a slight unbalance in applied voltage to the transformer.

Then, a loss model was created for the DAB topology based on the single phase shift modulation. Before the exact losses per component could be calculated, first the operating currents were determined. Following that, corresponding loss models were made for all components. It was shown that the LV switches would switch at high peak currents that would induce losses even when ZVS was obtained, and therefore a separate loss model was implemented. Afterwards, a minimum search script was created that evaluates all possible component combinations based on a provided database of suitable components. The user can simply select a list of, for example, MOSFETs that meet the requirements, after which the script will generate the set-up of components that leasd to the highest average power stage efficiency.
With the outcome of the script, the converter with highest possible efficiency is created, which resulted in an average efficiency of 98.67 % for an operating power of 2.5 kW and an average efficiency of 97.79 % for an operating power of -2.5 kW. Next, a sensitivity analysis was done to investigate the loss in efficiency when less parallel MOSFETs were placed, as well as implementing automotive rated MOSFETs. The final converter design equipped one MOSFET per switch for the HV bridge and two parallel MOSFETs per switch for the LV bridge. Additionally, the choice was made to go with the automotive rated MOSFETs, leading to an average power stage efficiency of 98.41 % and 97.87 % for positive and negative power transfer, respectively.

Even though the average efficiency of the power stage is already up to the requirements, it was thereafter investigated whether the converter operation can be more optimized in terms of efficiency by equipping different modulation methods. Three potential candidates were introduced: triangular current modulation, extended phase shift modulation and triple phase shift modulation. It was shown that a combination of triangular current modulation, single phase shift modulation and extended phase shift modulation can reduce the RMS current of the inductor and transformer. The reason of interest is that when ZVS is achieved, the

DAB converter mainly suffers from conduction losses, which are quadratically correlated to the RMS currents. Results showed that even though the RMS current dropped by as much as 10 % for the most operating conditions, the total converter losses for positive power transfer increased. The reason was that the optimal modulation scheme resulted in a hard switching region, whereas SPS modulation only had a smaller hard switching region. For the negative power transfer though, the average efficiency was improved from 97.87 % to 98.34 %. This was not enough to implement the optimal modulation, as it greatly increased the complexity of the converter, without many benefits.

Lastly, the control of the DAB converter has been written. To this end, first a dynamic model was derived, which makes use of a harmonic model. The eventual system was a simple, linear first order equation, of which the complexity and accuracy was directly influenced by adding additional harmonics. It was shown that including more harmonics would increase the accuracy of the model, but there was a point of diminishing returns.
With the dynamic model in place, a controller was designed for it. The controller implementation was done using a PI controller. It was then tuned using the derived DAB model, after which a detailed converter model was created in Simulink. The PI controller parameters were fine-tuned on this detailed model and a adequate response was obtained that can be implemented on the first prototype of the converter.

As a final remark, a lot of work has been put into the realization of a prototype PCB for the DAB converter, which was one of the original goals of this thesis. Due to the COVID-19 outbreak, manufacturers and suppliers of parts closed their doors, with long lead times as a consequence. The control of the converter dropped in as a replacement for all the planned validation measurements and analyses. However, the work on the prototype PCB is briefly shown in Appendix section C.2, together with screenshots of the PCB.

## 6.1. Recommendations

Due to the delays because of COVID-19 and therefore elimination of the validation steps in this thesis, these are the obvious next steps for this project. The prototype is ready to be ordered and once assembled and arrived, the work of this thesis can be validated. All the work has already been extensively simulated in both LTSpice and Simulink using detailed models, however, actual measurements will verify the calculations and efficiency outcomes in this thesis.

Furthermore, more research should be done into increasing the ZVS region of the designed DAB converter. Especially in combination with the optimal modulation as derived in chapter 4 will result in even higher efficiencies over the whole operating range. One interesting idea is to add so-called AC-link commutation inductors, as introduced in [17]. Small inductors are added to the terminals that connect the AC-link to the bridges. Effectively they increase the commutation current that is present in the leakage inductor during the dead time of the switching cycle. By doing so, the ZVS limit is raised, as can be seen by considering eq. (2.18).

Another topic that should be improved is the control of the converter. In this thesis a simple controller is presented that performs acceptably for the prototype implementation. However, many improvements can be made to it. The first one being an adaptive PI controller. As was explained in chapter 5, the harmonic model and its corresponding tuning are only accurate around the linearization point of the model. One can easily derive multiple models for the converter using the presented method, and get an initial tuning for the corresponding models. These $K_p$ and $K_i$ parameters can then be stored in a lookup table. Then, based on the operation conditions of the converter, these P and I variables can be loaded to ensure a similar response (similar rise times for example) under all converter conditions.
Secondly, a simple feed forward implementation can be added to eliminate the influence of the disturbance of the current $\Delta I_{LVbus}$.
Lastly, an inner control loop should be added that monitors the DC bias current through the transformer. This can be implemented by a high-speed current sensor in the circuit, which measures and compares the positive and negative amplitude of the transformer current. When these are not the same, a DC bias is present, which should be countered by adjusting the voltage waveforms. With this addition, together with the DC-blocking capacitor, transformer saturation will not occur.

# Appendices

# A

# Derivations

This chapter contains the details of derivations that have been used in this thesis. Rather than placing the derivations in the text, they are explained step-by-step in this chapter.

## A.1. RMS currents

In order to calculate the RMS currents through the inductor in buck mode, the currents of the inductor have to be split into two separate currents: the continuous current $I_{L,min}$ and the time varying triangular waveform $i_{L,ripple}(t)$. In formula form this means that

$$i_L(t) = i_{L,ripple}(t) + I_{L,min} \tag{A.1}$$

The waveforms can be seen in fig. A.1.

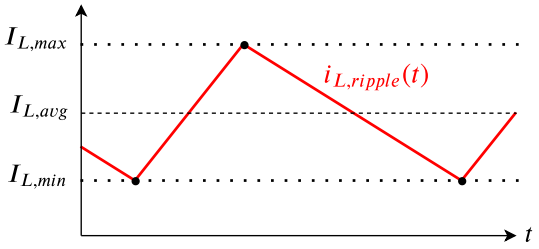



Figure A.1: Ideal inductor current waveform of a buck converter.

Now, according to the definition of RMS (root-mean-square), we can define:

$$\begin{aligned} I_{L,RMS}^2 &= \text{avg}\left[\left(i_{L,ripple}(t) + I_{L,min}\right)^2\right] \\ &= \text{avg}\left[i_{L,ripple}^2(t)\right] + 2I_{L,min} \cdot \text{avg}\left[i_{L,ripple}(t)\right] + I_{L,min}^2 \end{aligned} \tag{A.2}$$

We know that for a triangular waveform the RMS value can be expressed as:

$$I_{RMS} = \frac{i(t)}{\sqrt{3}} \tag{A.3}$$

By making use of eq. (A.3), and realizing that the average value of $i_{L,ripple}(t)$ can be expressed as

$$\text{avg}\left[i_{L,ripple}(t)\right] = \frac{I_{L,max} - I_{L,min}}{2} \tag{A.4}$$

From here, eq. (A.2) can be rewritten as:

$$I_{L,RMS}^2 = \frac{\left(I_{L,max} - I_{L,min}\right)^2}{3} + I_{L,min} \cdot \left(I_{L,max} - I_{L,min}\right) + I_{L,min}^2 \tag{A.5}$$

Now, by defining $I_{pp} = I_{L,max} - I_{L,min}$ eq. (A.5) can be simplified to:

$$I_{L,RMS}^2 = \frac{1}{3} I_{pp}^2 + I_{pp} \cdot I_{L,min} + I_{L,min}^2 \tag{A.6}$$

Finally, by substituting $I_{L,min} = I_{L,avg} - \frac{1}{2} I_{pp}$ gives

$$I_{L,RMS}^2 = \frac{1}{3} I_{pp}^2 + I_{pp} \left( I_{L,avg} - \frac{1}{2} I_{pp} \right) + \left( I_{L,avg} - \frac{1}{2} I_{pp} \right)^2 \tag{A.7}$$

which can be simplified into:

$$I_{L,RMS}^2 = \frac{1}{12} I_{pp}^2 + I_{L,avg}^2 \tag{A.8}$$

By taking the root of both sides, delivers the final expression for the RMS current through the inductor of a buck converter in CCM:

$$I_{L,RMS} = \sqrt{\frac{1}{12} I_{pp}^2 + I_{L,avg}^2} \tag{A.9}$$

## A.2. Maximum leakage inductance

Starting off with the transferred power of the DAB for SPS modulation, as described by eq. (2.2):

$$P = \frac{n V_{HV} V_{LV}}{2\pi^2 f_s L_k} \varphi \left( \pi - \varphi \right). \tag{A.10}$$

First, a substitution is introduced to simplify the derivation:

$$\alpha = \frac{n V_{HV} V_{LV}}{2\pi^2 f_s L_k}. \tag{A.11}$$

The only control parameter of the DAB for SPS is the phase shift $\varphi$. The maximum achievable power that is transferred can thus be found by deriving eq. (A.10) with respect to $\varphi$, resulting in:

$$\frac{dP}{d\varphi} = \alpha \left( \pi - 2\varphi \right). \tag{A.12}$$

Then, by equating the derivative of the power to zero, a maximum or minimum can be found. This results in:

$$2\alpha\varphi = \alpha\pi, \tag{A.13}$$

which then can be rewritten into

$$\varphi = \tfrac{1}{2}\pi. \tag{A.14}$$

With eq. (A.14) a local peak is found, meaning that when $\varphi = \frac{1}{2}\pi$, the maximum power transfer of the DAB is found. Combining eq. (A.14) with eq. (A.10) results in:

$$P_{max} = \frac{n V_{HV} V_{LV}}{8 f_s L_k}. \tag{A.15}$$

eq. (A.15) describes the maximum transferable power for a DAB converter, given a certain operating point (combination of $V_{HV}$ and $V_{LV}$. Then, in order to find the maximum leakage inductance $L_{k,max}$ that still enables to transfer a certain desired power $P_{des}$, eq. (A.15) can be rewritten into:

$$L_{k,max} = \frac{n \cdot \min\left(V_{HV}\right) \min\left(V_{LV}\right)}{8 f_s P_{des}}. \tag{A.16}$$

## A.3. Maximum TCM power

The maximum power transfer for the triangular current mode modulation has been given in [39] and can be expressed as:

$$P_{\Delta,max} = \frac{V_{HV}^2 \left(1 - 2\tau_{blank} f_s\right)^2 \left(nV_{LV} - V_{HV}\right)}{4L_k f_s n V_{LV}}. \tag{A.17}$$

In order for this formula to be used with the introduced standardized variables in section 4.3.2, it needs to be rewritten. First, the blanking time $\tau_{blank}$ is put to zero, since the DAB converter is still assumed to be ideal in the analysis of the modulation methods. This results in:

$$P_{\Delta,max} = \frac{V_{HV}^2 \left(nV_{LV} - V_{HV}\right)}{4L_k f_s n V_{LV}}. \tag{A.18}$$

Now, by substituting $Z_{ref} = 2\pi f_s L_k$ into eq. (A.18) gives

$$P_{\Delta,max} = \frac{V_{HV}^2 \left(nV_{LV} - V_{HV}\right)}{\frac{2}{\pi} Z_{ref} n V_{LV}}. \tag{A.19}$$

Then, the voltages have to be normalized by dividing them by the reference voltage $V_{ref}$. Inserting the normalized voltages according to

$$\begin{aligned} V_{HV} &= \overline{V}_1 \cdot V_{ref} \\ nV_{LV} &= \overline{V}_2 \cdot V_{ref} \end{aligned} \tag{A.20}$$

results in:

$$P_{\Delta,max} = \frac{\pi}{2} \frac{\overline{V}_1^2 V_{ref}^2 \left(\overline{V}_2 V_{ref} - \overline{V}_1 V_{ref}\right)}{Z_{ref} \overline{V}_2 V_{ref}}. \tag{A.21}$$

When the resulting formula is rearranged, the following is obtained:

$$P_{\Delta,max} = \frac{\pi}{2} \frac{\overline{V}_1^2 \left(\overline{V}_2 - \overline{V}_1\right)}{\overline{V}_2} \frac{V_{ref}^2}{Z_{ref}} = \frac{\pi}{2} \frac{\overline{V}_1^2 \left(\overline{V}_2 - \overline{V}_1\right)}{\overline{V}_2} P_{ref}. \tag{A.22}$$

Finally, $P_{ref}$ can be brought to the left hand side, resulting in the normalized maximum power and the final formula:

$$\overline{P}_{\Delta,max} = \frac{\pi}{2} \frac{\overline{V}_1^2 \left(\overline{V}_2 - \overline{V}_1\right)}{\overline{V}_2} \tag{A.23}$$

## A.4. Formulae to calculate control variables for OTM modulation

The formulae that will be given in this section are the result of calculations done in [40]. For completeness, they are listed below, since the interim values have been used in this thesis work and are needed to compute $D_2$ for OTM modulation.

$$e_1 = -\frac{2\overline{V}_1^2 + \overline{V}_2^2}{\overline{V}_1^2 + \overline{V}_2^2} \tag{A.24}$$

$$e_2 = \frac{\overline{V}_1^3\overline{V}_2 + \frac{|\overline{P}_{LV}|}{\pi}\left(\overline{V}_1^2 + \overline{V}_2^2\right)}{\overline{V}_1^3\overline{V}_2 + \overline{V}_1\overline{V}_2^3} \tag{A.25}$$

$$\begin{aligned} e_3 =& 8\overline{V}_1^7\overline{V}_2^5 - 64\frac{|\overline{P}_{LV}|^3}{\pi^3}\left(\overline{V}_1^2 + \overline{V}_2^2\right)^3 \\ &- \frac{|\overline{P}_{LV}|}{\pi}\overline{V}_1^4\overline{V}_2^2\left(4\overline{V}_1^2 + \overline{V}_2^2\right)\left(4\overline{V}_1^2 + 13\overline{V}_2^2\right) \\ &+ 16\frac{\overline{P}_{LV}^2}{\pi^2}\overline{V}_1\left(\overline{V}_1^2 + \overline{V}_2^2\right)^2\left(4\overline{V}_1^2\overline{V}_2 + \overline{V}_2^3\right) \end{aligned} \tag{A.26}$$

$$\begin{aligned} e_4 =& 8\overline{V}_1^9\overline{V}_2^3 - 8\frac{|\overline{P}_{LV}|^3}{\pi^3}\left(8\overline{V}_1^2 + \overline{V}_2^2\right)\left(\overline{V}_1^2 + \overline{V}_2^2\right)^2 \\ &- 12\frac{|\overline{P}_{LV}|}{\pi}\overline{V}_1^6\overline{V}_2^2\left(4\overline{V}_1^2 + \overline{V}_2^2\right) \\ &+ 3\frac{\overline{P}_{LV}^2}{\pi^2}\overline{V}_1^3\overline{V}_2\left(4\overline{V}_1^2 + \overline{V}_2^2\right)\left(8\overline{V}_1^2 + 5\overline{V}_2^2\right) \\ &+ \left(\frac{3|\overline{P}_{LV}|}{\pi}\right)^{\frac{3}{2}}\overline{V}_1\overline{V}_2^2\sqrt{e_3} \end{aligned} \tag{A.27}$$

$$e_5 = \frac{2\overline{V}_1^6\overline{V}_2^2 + 2\frac{|\overline{P}_{LV}|}{\pi}\left(4\overline{V}_1^2 + \overline{V}_2^2\right)\left[\frac{|\overline{P}_{LV}|}{\pi}\left(\overline{V}_1^2 + \overline{V}_2^2\right) - \overline{V}_1^3\overline{V}_2\right]}{3\overline{V}_1\overline{V}_2\left(\overline{V}_1^2 + \overline{V}_2^2\right)(e_4)^{\frac{1}{3}}} \tag{A.28}$$

$$e_6 = \frac{4\left(\overline{V}_1^3\overline{V}_2^2 + 2\overline{V}_1^5\right) + 4\frac{|\overline{P}_{LV}|}{\pi}\left(\overline{V}_1^2\overline{V}_2 + \overline{V}_2^3\right)}{\overline{V}_1\left(\overline{V}_1^2 + \overline{V}_2^2\right)^2} \tag{A.29}$$

$$e_7 = \frac{(e_4)^{\frac{1}{3}}}{6\overline{V}_1^3\overline{V}_2 + 6\overline{V}_1\overline{V}_2^3} + \frac{e_1^2}{4} - \frac{2e_2}{3} + e_5 \tag{A.30}$$

$$e_8 = \frac{1}{4}\left(\frac{-e_1^3 - e_6}{\sqrt{e_7}} + 3e_1^2 - 8e_2 - 4e_7\right) \tag{A.31}$$

# B

# Inductor design method

For the series inductor design, a method has been used that calculates the inductor parameters based on the circuits magnetic reluctance. It is an iterative process that assumes that the core material and inductance are known. First, a brief introduction to magnetic circuits is given, from which basic formulae are derived. Then, the operating point of the inductor can be selected, followed by the calculation of the total air gap length. Finally, the iterative process is described.

## B.1. Introduction to magnetic circuits

To start with, the magnetic circuit has to be analyzed. To this end, a typical magnetic circuit for an inductor with air gap is depicted in fig. B.1.

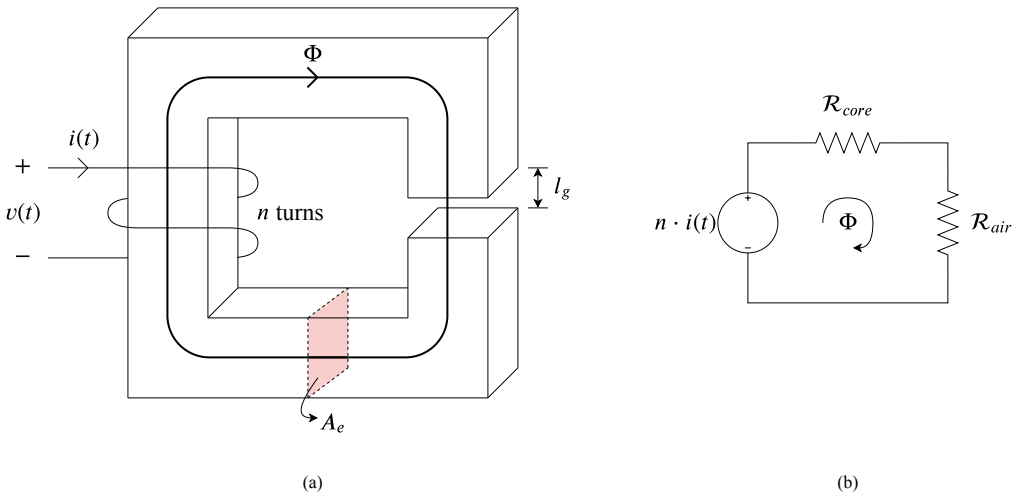



Figure B.1: Magnetic diagram for an inductor with air gap depicted as (a) a structure and (b) a equivalent circuit. Φ is the flux through the structure and $\mathscr{R}$ the reluctance of the magnetic circuit.

As can be seen from the figure, the physical structure of the inductor can be represented in a schematic circuit. The current through the wire wrapped around the magnetic core induces a magnetic flux, Φ. This flux flows through the core and air gap and experiences some resistance, called reluctance. Different materials have a varying reluctance as can be seen in the equivalent circuit. The complete core has a reluctance $\mathscr{R}_{core}$ and the air gap has a reluctance $\mathscr{R}_{air}$. The product of the turn ratio $n$ and the current through the wires $i(t)$ is known as the magnetomotive force, or MMF in short and can be expressed as

$$\mathscr{F} = \Phi \cdot \mathscr{R} = n \cdot i(t). \tag{B.1}$$

For the magnetic flux it is known that it can be described as the product of the magnetic field and the area that is perpendicular to the magnetic field. In fig. B.1 this area has been depicted as $A_e$, which is the effective

area of the core, given by the manufacturer of the core in the datasheet. Mathematically this can be expressed as

$$\Phi = B \cdot A. \tag{B.2}$$

Now, the inductance of the inductor can be expressed as

$$L = \frac{n^2}{\mathscr{R}_{tot}}, \tag{B.3}$$

where $\mathscr{R}_{tot}$ is the total reluctance of the magnetic circuit. In the case of the circuit depicted in fig. B.1 it is the sum of $\mathscr{R}_{core}$ and $\mathscr{R}_{air}$. Combining eqs. (B.1–3) and rewriting them leads to

$$Li = nBA, \tag{B.4}$$

which is the basic equation that will be used for the further calculation of the inductor parameters.

## B.2. Operating point

Now that the basic magnetic formulae are known, a first iteration can be made to get the inductor variables. Based on the design of the DAB converter, a specific value of $L_k$ will be desired. Together with this first constraint, a core material should be chosen. Depending on the operating conditions, such as temperature, saturation characteristics and frequency, one core material can be more suitable than others.
For this inductor design, 3F3 has been selected due to its low losses at the operating frequency. It has one of the lowest losses for the core materials that fall in the 100 kHz region [49]. Combined with its high permeability, 3F3 is selected as the basis of the inductors.
Using the core material, a maximum operating point on the B-H curve can be selected. The selection of this maximum magnetic flux density, $B_{max}$, should be chosen such that saturation of the core is prevented. For the DAB converter, saturation of the core is possible, since no DC coupling capacitors are placed near the transformer. For that reason, a large margin is used for the selection of the maximum operating point. Moreover, a low $B_{max}$ automatically leads to a low power dissipation, as can be seen from the datasheet of the core material [50]. The operating point is chosen to be $B_{max} = 250$ mT, which is significantly lower than the saturation point of $B_{sat,3F3} \approx 440$ mT.
Using the selected operating point, the core permeability, $\mu_{core}$, has to be determined. The permeability of a core is not constant and depends on the operating point. Therefore, an average $\mu_{core}$ is used and calculated according to

$$B_{max} = \mu_{core} H_{max}, \tag{B.5}$$

where $H_{avg}$ is the average magnetic field strength for the operating point $B_{max}$. From the datasheet, it can be seen that for $B_{max}$ with a temperature of 25 °C, the average can be computed as $H_{avg} = \frac{50-18}{2} = 34$ A/m. Using this value in eq. (B.5) gives a core permeability of $\mu_{core} = 7.35 \cdot 10^{-3}$ H/m.
From here, a certain core will be selected to demonstrate the calculations. When a new core is selected, the same steps can be taken from here. For now, the ETD44-3F3 is selected as a first size [51]. The required number of turns can now be computed by rewriting eq. (B.4). Rewriting the equation results in

$$n = \frac{Li_{max}}{B_{max} A_e} = \frac{19 \cdot 10^{-6} \cdot 35}{0.25 \cdot 173 \cdot 10^{-6}} \approx 15.4. \tag{B.6}$$

Obviously, it is not possible to have a non integer amount of turns, so it is rounded up to the nearest integer, which is 16 in this case. The additional winding will eventually result in a slightly lower $B_{max}$, since the other variables of eq. (B.4) are fixed.
The last step is to check whether the number of windings fit inside the core. Usually, in the datasheet of the core the appropriate bobbin is given, which is the plastic spindle that is used to wind the windings around. Depending on the total outer diameter of the winding that will be used, the number of windings can fit inside the chosen core or not. A simple, yet very conservative method to see whether the number of turns fit, is to divide the width of the winding area of the bobbin by the outer diameter of the winding:

$$N_{width} = \left\lfloor \frac{l_w}{d_o} \right\rfloor, \tag{B.7}$$

where $N_{width}$ is the number of full windings that fit in the width of the bobbin, $l_w$ is the length of the winding width and $d_o$ is the outer diameter of a winding. The $\lfloor\rfloor$ indicates that the outcome of the division is rounded down to the closest integer. In a similar way, this is done for the winding height:

$$N_{height} = \left\lfloor \frac{l_h}{d_o} \right\rfloor, \tag{B.8}$$

where $N_{height}$ is the number of full windings that fit in the height of the bobbin and $l_h$ is the height of the bobbin in which the windings can be placed. Finally, by multiplying the outcomes of eq. (B.7) and eq. (B.8), the total number of windings that fit in the total winding area of the bobbin can be calculated.
As indicated before, this is a very conservative method, since the conductor of which the winding is made usually is a round wire. Rather than stacking the windings on top of each other, they can be placed slightly offset of each other, as has been shown in fig. B.2, which results in a more efficient use of the winding area.

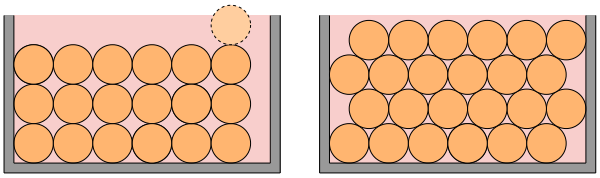


Figure B.2: Cross section view of the winding area utilization, showing the conservative method on the left and the realistic method on the right. The orange circles are the conductors, the grey bounds the bobbin walls and the red background shows the unused area.

To this end, a more precise method can be used to estimate whether the windings fit inside the windings area of the bobbin. This method is described in [26] and will be briefly discussed such that the application can be used.
First, the total area of the round conductor needs to be known. Assuming that the outer diameter is known, this can be easily calculated. Then the total cross sectional area that is occupied by the windings is:

$$A_{wind} = n \cdot A_{cond}, \tag{B.9}$$

where $A_{cond}$ is the cross sectional area of the conductor (including isolation material). Then, this area is compared with the total available area in the bobbin. To compensate for the unused area in between the windings, a factor, $K_u$, is introduced, which is called the window utilization factor. For a simple inductor, the value of $K_u$ is approximately 0.4. Then, the following inequality has to be valid in order for the windings to fit in the selected core:

$$K_u W_a \geq n A_{wind}, \tag{B.10}$$

where $W_a$ is the winding area of the bobbin.

## B.3. Air gap length

Next is to determine the length of the air gap. To this end, the total reluctance needed to ensure a certain inductance can be computed, using eq. (B.3). The total reluctance is then found to be $\mathscr{R}_{tot} = 16^2/19 \cdot 10^{-6} \approx 13.5 \cdot 10^6$ H$^{-1}$.
As explained before, the total reluctance of the magnetic circuit is the sum of the reluctance of the core and that of the air gap. The reluctance of the core can already be determined now that a specific core has been selected. The equation for reluctance, where core variables have been used, is known as

$$\mathscr{R}_{core} = \frac{l_e}{\mu_0 \mu_r A_e}, \tag{B.11}$$

where $l_e$ is the effective length of the path of the flux through the core, $\mu_0$ is the permeability of vacuum, $\mu_r$ is the relative permeability of the core material. In eq. (B.5) the product $\mu_0\mu_r$ has been written as $\mu_{core}$. This results in a total core reluctance for the ETD44-3F3 core of $\mathscr{R}_{core} = 103 \cdot 10^{-3} / \left(7.35 \cdot 10^{-3} \cdot 173 \cdot 10^{-6}\right) \approx 81 \cdot 10^3$ H$^{-1}$.
To obtain the air gap reluctance, a simple subtraction of the total reluctance minus the core reluctance results in $\mathscr{R}_{air} \approx 13.4 \cdot 10^6$ H$^{-1}$. Using eq. (B.11) and using $\mu_r = 1$ for air, the total air gap length is found to be $l_g = \mathscr{R}_{air} \cdot \mu_0 \cdot 173 \cdot 10^6 = 2.9$ mm.

A small remark should be made regarding the length of the air gap. Because of the presence of an air gap, fringing effect might introduce severe losses. Flux fringing is the effect that near the air gap the magnetic field lines tend to turn outwards. In the presence of a metal object within these field lines, eddy currents will be induced, resulting in high additional losses. Care should be taken that the single air gap does not become too large. Since the windings will be placed around the air gap for an ETD core, the flux fringing can lead to excessive copper losses. As a rule of thumb for a uniform air gap, there should be no windings placed within a distance of $l_g$ from the air gap [52].
This limits the maximum reasonable air gap, since the bobbin has a finite thickness. As an example, if the bobbin wall thickness is around 2 mm and there is a small gap of 1 mm between the wall of the bobbin and the core material, the length of the air gap should not exceed 3 mm in order to prevent additional copper losses due to the fringing effect. Alternatively, one could place a non-magnetic spacer before starting to wind around the bobbin. By doing so, the winding area of the bobbin is reduced, however, a larger air gap and reduced copper losses can be achieved.

# C

# Prototype design

As has been briefly touched upon in the introduction of this thesis, due to the COVID-19 situation the (original) plans for this thesis were changed. Because of PCB manufacturers and component suppliers closing down, the prototype could not be delivered in time. Therefore, the work done on designing and working out a fully functioning prototype PCB was put to a stop. However, a lot of work has been put into realizing this PCB, which is the reason that only the results will be shown in this appendix chapter. Together with the component selection and design of the PCB, time was spent on designing a proper thermal system for the converter, based on its losses. Again, this work does not contribute to this thesis anymore since it could not be validated by measurements on the final prototype.

## C.1. Thermal design of the converter

The thermal design is done using a linear model consisting of thermal resistances. First, the worst case losses have to be determined. Then the thermal design can be analyzed for a specific MOSFET. To perform thermal calculations, a Matlab script has been created.
The requirements from Lightyear as listed in section 1.2 that are of importance here, are the weight requirement of 5 kg and the requirement that either natural or forced convection can be used. In other words, no liquid cooling is allowed for the converter to remain functional and within specifications of the components. For the script, the following assumptions are used:

- SPS modulation will be used, with the converter parameters as listed in table 3.7 and the MOSFETs as selected in table 3.9.
- The area for heat transfer from the HV SiCFET to the solder is 119 mm2 (12.2 x 9.75 mm die size).
- The area for heat transfer from the LV SiFET to the solder is 81 mm2 (10.1 x 8 mm die size).
- The area for heat transfer from the top layer of the PCB onwards for the HV SiCFETs is 400 mm2, assuming a 20 x 20 mm copper heat spreader in copper layer 1. For the LV SiFETs it is 169 mm2, assuming a 13x13 mm heat spreader. The sizing of the heat spreader is made 2-3 times the size of the die size, which is the optimum. Any larger would not lead in improved heat spreading performance [53].
- A thermal interface material (TIM) with a thermal conductivity of 7 W/mK will be used between PCB and casing.
- A 0.1 mm thick layer of thermally conductive glue with a thermal conductivity of 1.8 W/mK will be used between the casing and heatsink.
- A natural convection heat sink will be used with a 200x300 mm footprint and a thermal resistance of 0.3 K/W.
- The maximum allowed PCB temperature is 120 °C.
- The ambient air temperature around the enclosure of the converter is 65 °C at maximum.

The goal of the thermal design is to show that the maximum temperatures will not exceed the 120 degrees PCB limit. Since this is a prototype, no in-depth simulations will be done, only a simple proof-of-concept calculation. First, a design is made using a large heatsink with natural convection.

### C.1.1. Maximum power loss

In table C.1 the maximum power loss is shown, which is calculated using the minimum search script. The numbers are the cumulative power loss for all components belonging to that category.

Table C.1: Maximum power loss for the designed DAB converter per component for both power directions.

| Component | Power loss at P = 2.5 kW | Power loss at P = -2.5 kW | Maximum (rounded) |
|---|---|---|---|
| HV SiCFETs | 14.5 W | 72 W | 72 W |
| LV SiFETs | 56.9 W | 31 W | 57 W |
| Transformer | 18.1 W | 21.7 W | 22 W |
| Inductor | 6.42 W | 8.12 W | 8.2 W |
| DC blocking capacitors | 0.88 W | 0.943 W | 1 W |
| PCB traces | 6.58 W | 7.05 W | 7.1 W |

It can be seen that the largest losses occur in the switches. A one dimensional schematic overview of the thermal circuit for one single MOSFET is given in fig. C.1. For the calculations an 8-layer PCB is assumed, with a copper thickness of 35 $\mu$m and a FR4 thickness of 200 $\mu$m (based on an 8-layer PCB from Eurocircuits). The heat of the MOSFETs will be transferred through the PCB to the casing, to which a heatsink is mounted. Additionally, throughout the PCB vias will be added to transfer the heat of the MOSFET(s) to the heatsink at the other side of the PCB. The number of required vias will be calculated in the next sections.

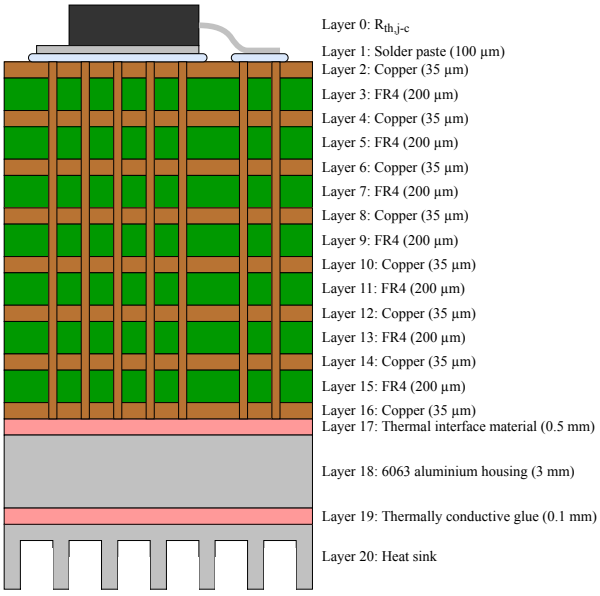



Figure C.1: One dimensional schematic representation of the thermal circuit for one MOSFET (not to scale).

### C.1.2. HV SiCFETs thermal design

For the HV SiCFETs the largest losses occur for negative power transfer. Assuming that only the HV and LV MOSFETs, the transformer and the inductor need to transfer heat to a heatsink, the total losses of the HV SiCFETs are a fraction of 72 / 159.2 = 0.45 of the total losses for negative power flow. To provide an estimation on the performance of the heatsink, this fraction of 0.45 will be assigned to the cooling of the HV SiCFETs, meaning that only 11.3 % of the heatsink is assigned to one individual HV SiCFET.

The cooling performance is not sufficient without vias. Therefore, the maximum allowable number of vias is implemented in the 20x20 mm area. For the vias a plating thickness of 20 $\mu$m is assumed, with a minimum

distance of 0.25 mm between via holes (rules from Eurocircuits [54]). The via outer diameter (including plating) to be used to determine the number of vias in an area should be the actual via diameter plus 0.1 mm, which accounts for the tooling size for the hole drilling.
Now, the thermal resistance of one via can be determined, using:

$$R_{th,via} = \frac{l_{PCB}}{k_{Cu} A_{via}}, \tag{C.1}$$

where $l_{PCB}$ is the total PCB thickness, and thus the length of one via, $k_{Cu}$ is the thermal conductivity of copper and $A_{via}$ is the total area of copper of the via. So, only the contribution of the copper plating of the via is considered, since the contribution of the air inside the via is negligible. To get the total copper area per via, it can be simply calculated by:

$$A_{via} = \frac{1}{4}\pi\left(d_{via}^2 - \left(d_{via} - 2d_{Cu,via}\right)^2\right), \tag{C.2}$$

where $d_{via}$ is the outer diameter of the via (incl. copper) and $d_{Cu,via}$ is the copper plating thickness per via. Using eq. (C.1), the equivalent thermal resistance for the maximum amount of each via size within the 400 mm$^2$ has been calculated and can be found in table C.2. To determine the maximum number of vias in an area, this calculator has been used (with a triangular pattern).

Table C.2: Equivalent thermal resistance for different via hole sizes.

| **Via outer diameter [mm]** | **Drill size [mm]** | **Number of vias in 400 mm$^2$** | **$R_{th,eq}$ [K/W]** |
|---|---|---|---|
| 0.3 | 0.4 | 1033 | 0.24 |
| 0.4 | 0.5 | 765 | 0.23 |
| 0.5 | 0.6 | 608 | 0.24 |
| 0.6 | 0.7 | 480 | 0.25 |
| 0.7 | 0.8 | 378 | 0.27 |

It can be seen that the optimal via diameter is 0.4 mm, which will be used for the HV SiCFETs. Note that the vias will also lie in the die area of the MOSFET. Those via holes need to be filled with resin. Using the 765 vias, in combination with the power dissipation of one SiCFET of 18 W and a 0.113 part of the total heatsink, leads to a maximum junction temperature of 128 °C, with a maximum PCB temperature of 120 °C. The total thermal resistance from junction to ambient is 3.5 K/W. The equivalent resistor network for one individual MOSFET with thermal resistances per layer is shown in fig. C.2.

### C.1.3. LV SiFETs thermal design

A similar approach as for the HV SiCFETs has been followed for the LV switches. The maximum power loss for the LV SiFETs happens during positive power transfer, leading to 57 W of losses. This is approximately 36 % of the total losses, meaning that for each LV MOSFET 4.47 % of the heatsink is reserved in the calculations. The optimal via diameter analysis for 169 mm2 is shown in table C.3.

Table C.3: Equivalent thermal resistance for different via hole sizes.

| **Via outer diameter [mm]** | **Drill size [mm]** | **Number of vias in 400 mm$^2$** | **$R_{th,eq}$ [K/W]** |
|---|---|---|---|
| 0.3 | 0.4 | 418 | 0.58 |
| 0.4 | 0.5 | 314 | 0.57 |
| 0.5 | 0.6 | 247 | 0.58 |
| 0.6 | 0.7 | 188 | 0.62 |
| 0.7 | 0.8 | 161 | 0.62 |

From the table it can be seen that the lowest $R_{th,eq}$ can be achieved with a via size of 0.4 mm and 314 vias. Eventually, the maximum junction temperature for the LV MOSFET will be 123 °C and the maximum PCB temperature is 120 °C. The total thermal resistance from junction to ambient is 8.12 K/W. The resistor network for one individual MOSFET can also be seen in fig. C.2.

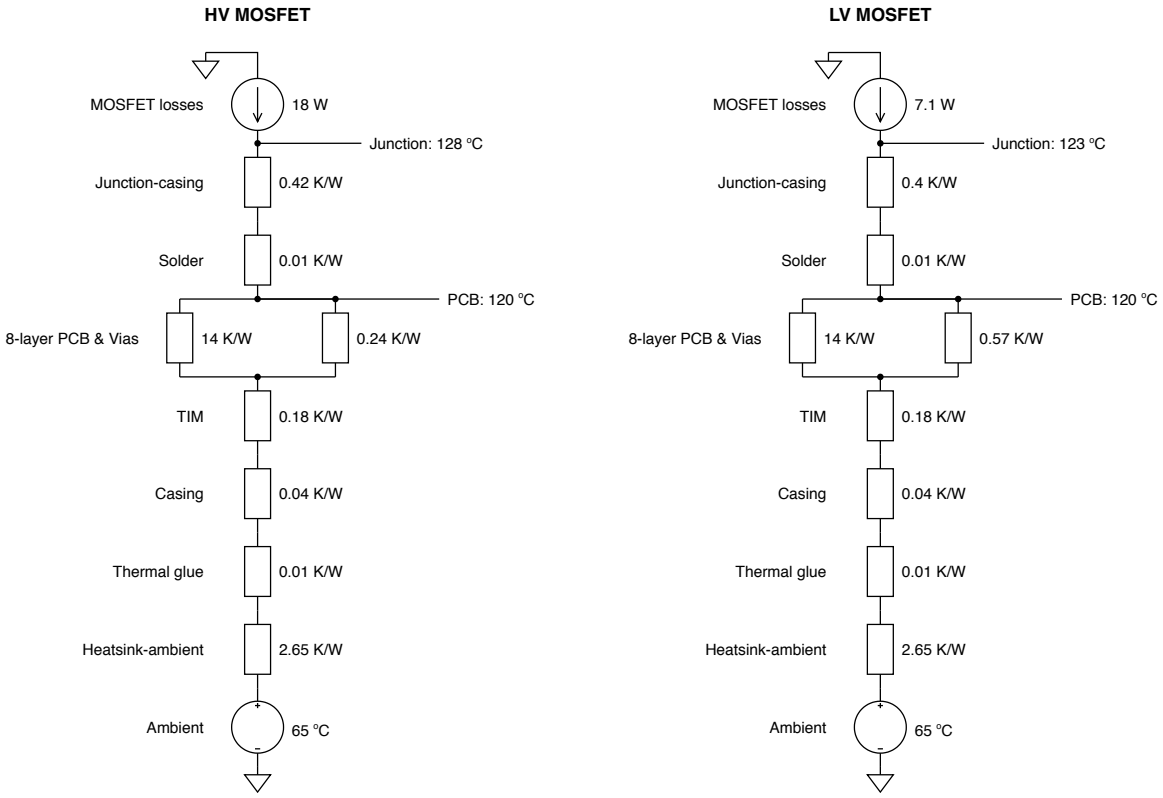



Figure C.2: Equivalent resistor network with thermal resistance per layer for one single HV and LV MOSFET.

### C.1.4. Conclusion

With the simplified thermal model in place, it can be seen that the converter is able to maintain within the maximum temperatures, even for the worst case scenarios. The resistor network model does not take thermal mass into account and as such can not be used to simulate transient temperature behavior. It does give insight in the maximum steady state temperature of all devices for the given operating point.

## C.2. PCB design

Screenshots of the final PCB design can be found below. The details about the design process as well as detailed component selection for auxiliary circuits, such as measurement circuits, microcontroller circuits, hardware protection circuits etc. will not be given in this thesis, as they fall out of the (adjusted) scope of this work. The top view of the PCB can be seen in fig. C.3 and the bottom view in fig. C.4. Finally, there is a 3D render that shows the PCB and its components in space, which can be seen in fig. C.5.

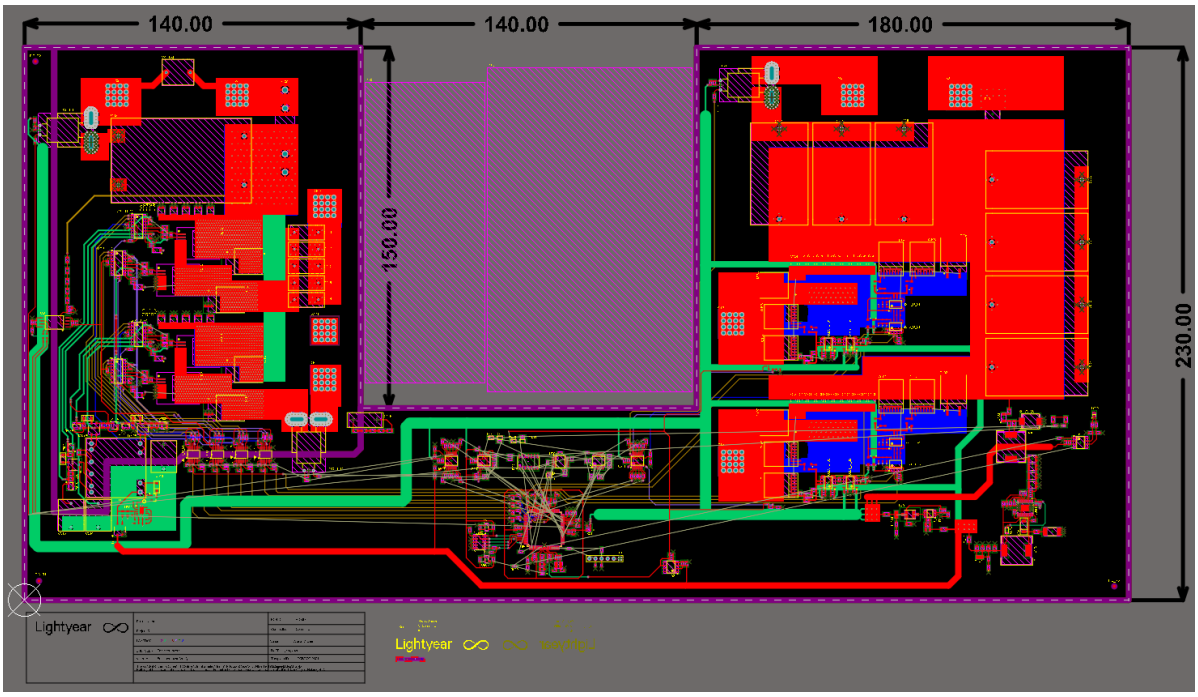



Figure C.3: Top view of the designed prototype PCB. The red planes are the top layer of the 8-layer PCB.

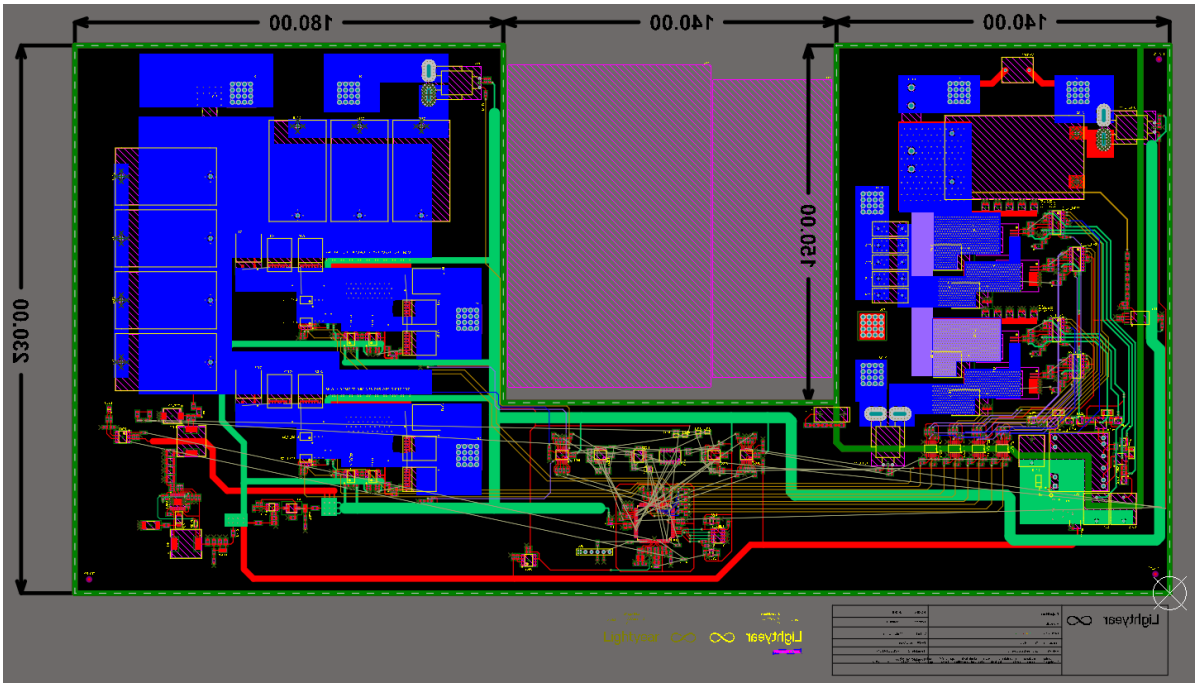



Figure C.4: Bottom view of the designed prototype PCB. The blue planes are the bottom layer of the 8-layer PCB.

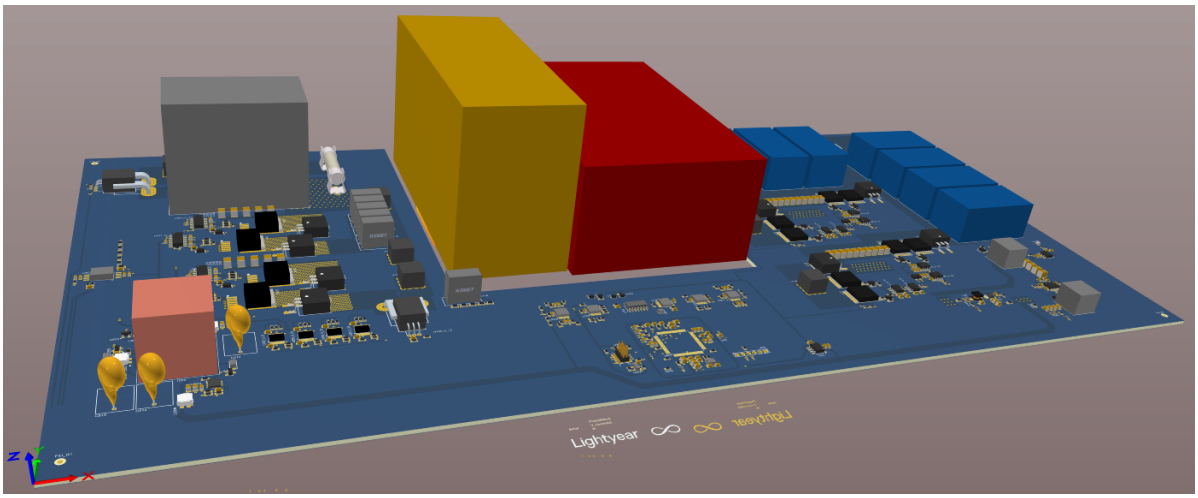



Figure C.5: Three-dimensional view of the designed prototype PCB. The yellow block is the inductor placeholder, the red block the transformer placeholder.

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