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DOI
10.4233/uuid:0f80a5f1-d81f-4f1d-b6ae-01289f8dfef0

Publication date
2016

Document Version
Final published version

Citation (APA)
Xu, J. (2016). *Low-Power Active Electrodes for Wearable EEG Acquisition*. [Dissertation (TU Delft), Delft University of Technology]. https://doi.org/10.4233/uuid:0f80a5f1-d81f-4f1d-b6ae-01289f8dfef0

Low-Power Active Electrodes for Wearable EEG Acquisition

Jiawei Xu

Low-Power Active Electrodes for Wearable EEG Acquisition

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof.ir. K.C.A.M. Luyben;
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op
maandag 27 juni 2016 om 10:00 uur

door

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CHAPTER 1

INTRODUCTION

1.1 Wearable EEG Devices

In modern clinical practice, scalp electroencephalography (EEG) measurement is the most important non-invasive procedure to measure brain electrical activity and evaluate brain disorders. Electroencephalograms (EEGs) represent the brain's spontaneous electrical activities by measuring scalp potentials over multiple areas of the brain (Figure 1.1), so the strength and distribution of such potentials reflects the average intensity and position of a group of underlying neurons. As a non-invasive method, EEGs play a vital role in a wide range of clinical diagnosis, such as epileptic seizures, Alzheimer's disease and sleep disorders [2]. Furthermore, EEGs are also finding increasing popularity in non-clinical neuroscience and cognitive research [3]. Typical applications are Brain Computer Interfaces (BCI), neurofeedback or brain function training.

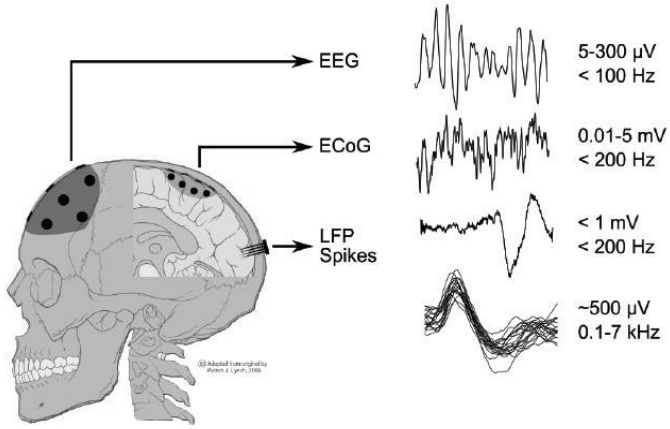

Figure 1.1 Different signals from the brain [1], including macroscopic signals, namely EEG and Electrocorticography (ECoG), and microscopic signals, namely local field potentials (LFPs), and action potentials or spikes.

During the last decade, there is a growing need towards continuous monitoring of brain activities in remote patient monitoring, health and wellness management due to the increased prevalence of chronic diseases, and the need to decrease the length of hospital stays [4]. The huge market demand, together with the advances in electronic manufacturing techniques, has accelerated the evolution of power-efficient and miniaturized wearable devices for biomedical applications (Figure 1.2), with long-term monitoring and user-friendliness being the key drivers.

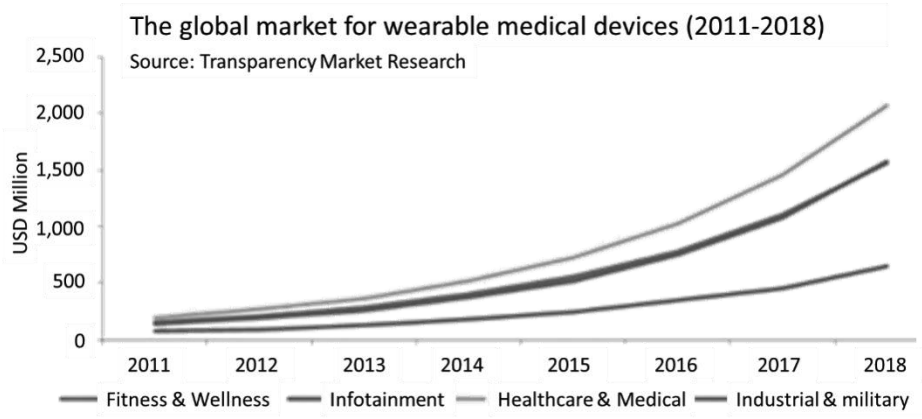

Figure 1.2 Market growth trends of wearable technology [5]. The global market for wearable medical devices was valued at USD 750 million in 2012 and is expected to reach a value of USD 5.8 billion in 2018, growing at a compound annual growth rate (CAGR) of 40.8% from 2012 to 2018.

Although the first human EEG recording system was invented in 1924, a personalized EEG device (Figure 1.3 a) for residential monitoring was not available until the 1970s [6]. Later, ambulatory EEG systems (Figure 1.3 b) and portable EEG devices (Figure 1.3 c) in principle gave users sufficient mobility during the recording. However, these devices are still bulky and power hungry, and are therefore unsuitable for long-term and continuous EEG recording.

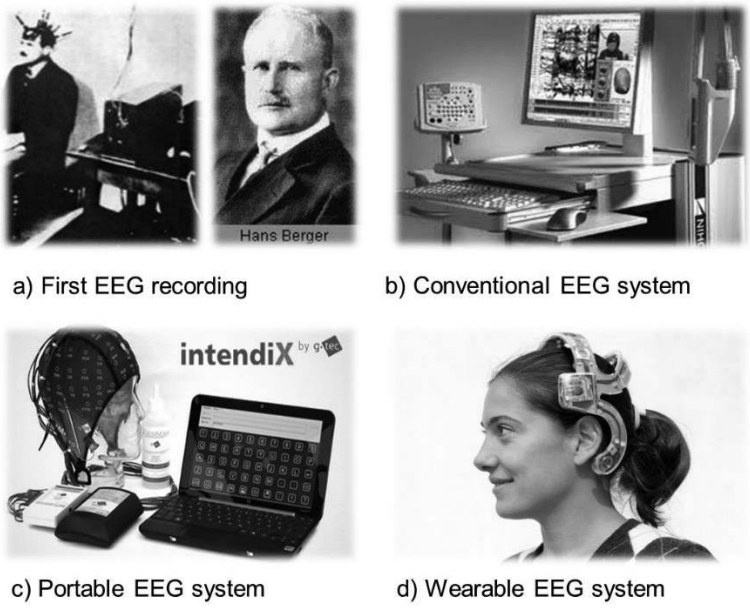

Figure 1.3 Evolutions in EEG readout systems: a) the first recording of human EEGs by Hans Berger [7], 1924; b) a 192-channel EEG system [8], Nihon Kohden, 1999; c) a portable EEG-based BCI system [9], g.tec, 2003; (d) a 4-channel wireless EEG headset [10], imec/Holst Centre, 2013.

Most recent advances in biomedical techniques, sensors, integrated circuits (ICs), batteries, and wireless communication have sped up the development of real "wearable" EEG monitors. For example, a miniature, lightweight, battery-powered wireless EEG recording unit (Figure 1.3 d) can be implemented inside various easy-to-use form factors [10]-[12], such as caps, headsets or helmets. These EEG units collect raw data of brain activities during a user's daily routine, which can then be used to extract biomarkers and to determine personal trends for emotion, behavior, disease management, and wellness applications.

This thesis presents a new generation of energy-efficient EEG signal acquisition ICs, which are typically the core of an EEG monitor and dominate its overall performance. The design methodologies and detailed implementation of the ICs towards wearable applications are discussed.

1.2 Prior-Art EEG Systems

As a standard practice, a basic EEG acquisition instrument contains three electrodes, three lead wires and an instrumentation amplifier (Figure 1.4). The instrument records the difference in voltage between one electrode and the reference electrode. Both electrodes convert ionic current into electric current, and so the EEG potential represents voltage fluctuations resulting from ionic current within brain neurons. Via two lead wires, an instrumentation amplifier amplifies the differential EEG potential between these two electrodes.

A third electrode, namely the bias electrode or ground electrode, helps keep the body's DC voltage level in-line with the readout circuits to properly amplify the EEG signal. Without the bias electrode connected to the body, the electrode potentials may drift and, eventually, saturate the IA's input.

In the electrical domain, the electrode-tissue interface can be modeled as a complex impedance in series with a DC voltage source, which represents the polarization voltage between skin and electrode (Figure 1.5).

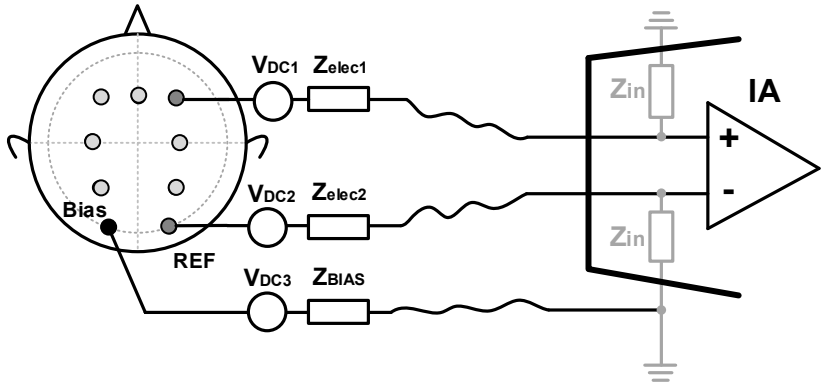

Figure 1.4 Acquiring an EEG signal using (passive) electrodes and a differential instrumentation amplifier.

The biggest challenge facing designers of wearable EEG systems is achieving improved user comfort, long-term monitoring capability with medical-grade signal quality. Unfortunately, prior-art EEG systems rarely meet all these requirements.

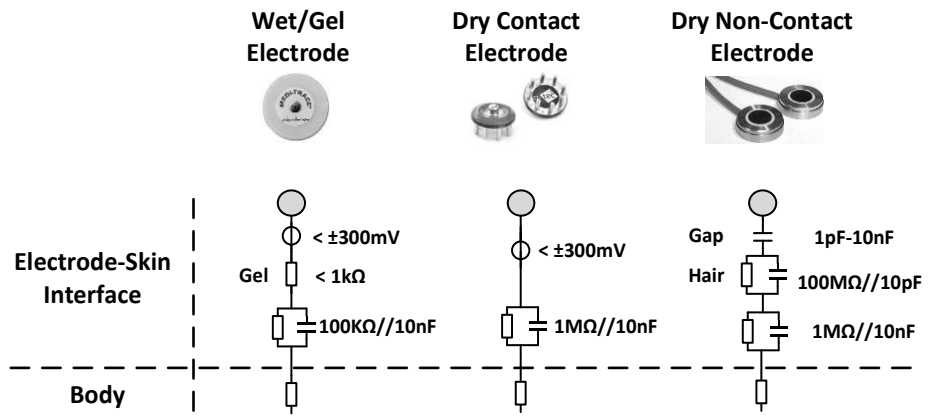

Figure 1.5 Equivalent electrical model of the electrode-tissue interface [13].

One major drawback of prior-art EEG systems is their dependence on gel or Ag/AgCl electrodes. Wet conductive gel reduces skin-electrode impedance and the associated artifacts or interference induced by cable motion. Therefore, wet electrodes are extensively used in clinical practice. However, wet electrodes require skin preparation and professional personnel to place them properly. In addition, the gel can dry out and therefore requires frequent replacement of electrodes to maintain signal integrity. These drawbacks really limit the use of wet electrodes in wearable EEG applications.

Dry electrodes, on the other hand, facilitate long-term EEG measurements as well as greater user comfort. However, this comes at the expense of reduced signal quality due to the larger skin-electrode impedance (Figure 1.5), which can be as high as a few MΩ at 50/60Hz [14][15] and which significantly increases interference pickup from the environment. Dry electrodes thus need to be buffered or shielded in order to approach the performance of wet electrodes [16]. Directly connecting dry electrodes to an EEG amplifier via lightweight non-shielded cables will not ensure good signal quality. Hence, conventional EEG systems (Figure 1.6 a), i.e., passive electrodes connected to differential biopotential amplifiers through long cables, are ill-suited for the use with dry electrodes and wearable devices.

1.3 A Promising Solution: Active Electrodes

Active electrodes (AEs) with co-integrated amplifiers solve this incompatibility problem (Figure 1.6 b). The close proximity of the electrodes to the amplifier

reduces interference pickup, while the amplifier's low output impedance improves signal robustness to cable motion [16]. Moreover, the signal quality of dry electrode EEG recording can be maintained without using conventional shielded cables, which is an attractive feature for low-volume wearable devices.

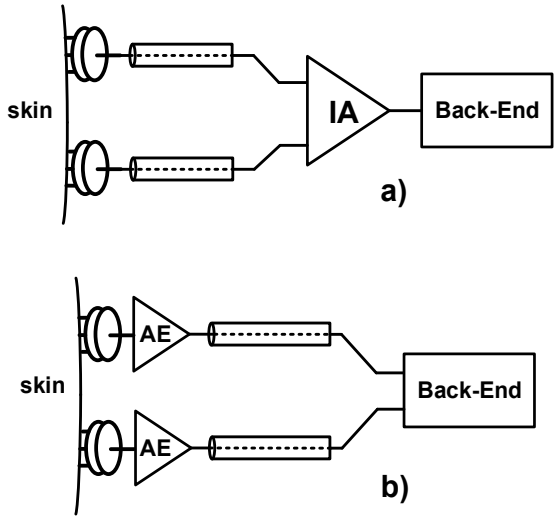

Figure 1.6 Illustration of EEG readout circuits: a) a conventional solution based on an IA, and b) a proposed solution based on active electrodes.

Early AEs consisted of simple analog buffers, i.e., voltage followers. Improved designs achieved higher input impedance [17], or required fewer cables [18][19]. The main limitation of this classic AE topology is its power inefficiency, as an analog buffer only performs impedance conversion without providing any voltage gain. The succeeding readout circuits still need to meet the same requirements of low-noise and electrode offset tolerance, leading to additional power consumption [20].

In contrast, this thesis presents several generations of AE based ICs implemented with power-efficient instrumentation amplifiers (IA). Although interfacing with dry electrodes and reducing the overall system power are the primary motivations for selecting AE architecture and for adding gain to the AEs, respectively, the proposed AE systems also aim to achieve performance that is comparable with that of medical grade systems.

1.4 Challenges in Active Electrode Systems

AEs constitute the first stage of a wearable EEG system, and thus determine its overall performance. Therefore, AEs have to cope with the same challenges as conventional differential amplifiers (Figure 1.7):

- Amplifying low-frequency low-amplitude EEG signal
- Interfacing with high impedance between skin and electrode
- Tolerating large electrode polarization voltages
- Suppressing environmental artifacts
- Minimizing system volume and power dissipation

In addition, the AEs also need to solve various practical challenges:

- Reducing the component mismatch between AEs.
- Minimizing the number of connecting wires

The sections below discuss these challenges in detail.

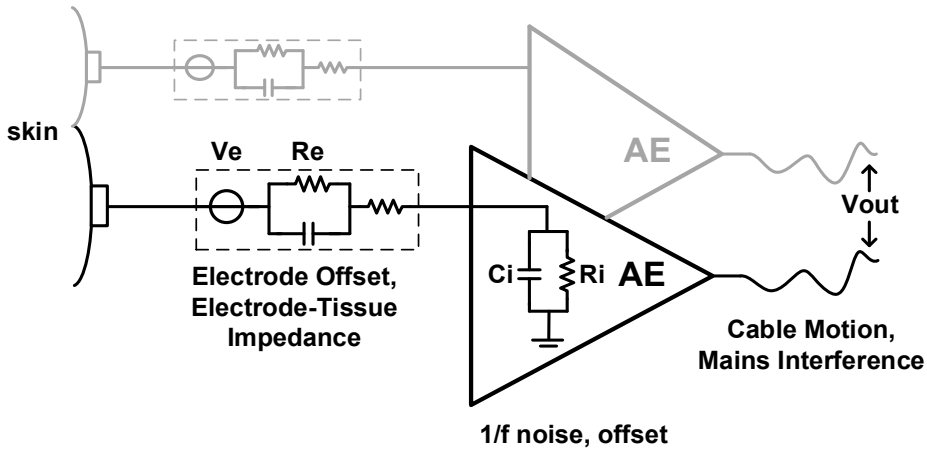

Figure 1.7 Aggressors in the skin-electrode interface and active electrodes.

EEG activity reflects the summation of the electrical activity of thousands or millions of neurons under the scalp. A typical adult EEG has an amplitude of about 10μV to 100μV when measured on the scalp and is about 10–20mV when measured by subdural electrodes [21]. Most of the cerebral signal observed in a scalp EEG falls in the range of 1–30Hz (activity below or above

this range is likely to be caused by artifacts, under standard clinical recording conditions). The EEG rhythmic activity is divided into frequency bands, such as Delta (<4Hz), Alpha (8-15Hz) and Beta (16-31Hz), which are used to detect various physiological behaviors. In order to amplify such low-frequency and low-amplitude potentials, an IA should be carefully designed for low-noise performance. According to an IEC standard [22], an EEG amplifier should have a maximum input referred noise of $6\mu V_{PP}$.

The use of dry electrodes comes with large and variable skin-electrode impedance, as well as large electrode polarization voltages. To minimize signal attenuation, AEs must then have very high input impedances. Electrode polarization voltage, or half-cell potential, develops across the electrolyte-electrode interface due to an uneven distribution of anions and cations [15]. This offset voltage can be as large as a few hundreds of mV and may saturate the IA. As a result, the IA should be able to tolerate at least 300mV DC offset [22] while still maintaining its performance.

Mains interference can be picked up from the environment during EEG acquisition, because a high impedance (dry) electrode behaves like an antenna. Although this issue can be mitigated by the use of AE architectures with low output impedance, AE mismatch can still convert any common-mode interference and motion artifact into a differential signal. Such signals can be larger than the EEG signals, thus reducing the dynamic range of the AE and requiring complex post-filtering. This can be avoided by designing AE pairs with a high common mode rejection ratio (CMRR).

A miniaturized multi-channel AE system requires a minimal number of wires connected to a back-end circuit. This reduces the overall cable weight, which is especially important when tens of AEs are used for multi-channel EEG acquisition, or when additional wires are needed for a multi-parameter measurement [23][24]. A nice example of multi-parameter measurement involves recording EEG and electrode-tissue impedance (ETI) signals simultaneously, the latter provides extra information that can be used for impedance based motion artifact reduction or simple lead-on/off detection.

Finally, an AE system should consume ultra-low-power to maximize battery life. For example, to realize 24 hours continuous operation with a 3.6V coin cell battery [25], an AE system, including multiple AEs and a back-end readout circuit, must consume less than 5mA. Although a battery with more

energy capacity can be used, its size and weight will be a major determinant of the system's form factor.

In summary, a good AE system should balance the tradeoff among different parameters to maximize overall performance, even in the presence of dry electrodes and the aforementioned aggressors.

1.5 Thesis Contributions and Organization

A complete EEG signal processing chain for emerging body area network (BAN) applications contains several major building blocks: analog front-ends (AFE), digital signal processing (DSP), a wireless transmitter and power management units (PMU). This thesis focuses on the design of AE-based EEG readout circuits for wearable interfaces, with a special emphasis on instrumentation amplifier (IA) architecture and design for AEs.

The main contributions of this work include the following:

• Analysis of capacitively-coupled IA architectures. Three types of chopper IAs are used in AE architectures that balance the tradeoff between noise, electrode offset tolerance, input impedance, and power consumption. The overall performance of these AEs is competitive with state-of-the-art biopotential IAs through the use of various circuit design techniques, such as positive feedback, which increases input impedance by a factor of 5-10 (Chapter 3); digitally-assisted ripple and offset calibration, which reduces these IA non-idealities by a factor of 10 (Chapter 3); and a functionally DC-coupled IA, which enables an input dynamic range of up to ±350mV while consuming very low power (Chapter 6).

• Development of CMRR boosting techniques that overcome the CMRR limitations imposed by AE gain mismatch. These techniques include a common-mode feedback (CMFB) circuit that processes the AEs' outputs, and feeds their common-mode signal back to each AE (Chapter 3); a power-efficient common-mode feedforward (CMFF) technique that creates a voltage averaging node to reduce the AEs' common-mode current (Chapter 4); and a more generic CMFF approach that utilizes an analog buffer to drive the AE's negative input, thus cancelling input common-mode interference before amplification (Chapter 6).

• Investigation of current noise, which can be a significant noise contributor of chopper amplifiers. Chopping was observed to cause excess current noise, which, at high impedance nodes, is converted into voltage noise with a slope of $1/f^2$. The origin of this noise is hypothesized to be the charge injection and clock feed-through of the input chopper. This current noise theory has been analyzed and experimentally verified (Chapter 5).

• Design of a single-chip digital active electrode (DAE) architecture, which combines an IA, an ADC and an I²C interface for on-chip analog signal processing and digitization (Chapter 6). This DAE architecture enables a daisy chain connection of all DAEs and a generic μC on a two-wire I²C bus, significantly reducing system complexity and cost.

The thesis is organized as follows. Chapter 1 introduces the basics of scalp EEG measurement, dry-electrode interfaces, active electrodes and the associated design challenges. Chapter 2 reviews the architectures of active electrodes and biopotential IAs, discussing their performance tradeoffs. Chapter 3 presents the use of an AC-coupled inverting IA as an AE. Chapter 4 presents a complete 8-channel AE-based EEG system, including both AEs and a back-end analog signal processor (ASP). Chapter 5 describes an experimental investigation of current noise in chopper amplifiers. Chapter 6 presents a highly integrated digital active electrode (DAE), with built-in IAs, an ADC and a digital interface on a single chip. Chapter 7 concludes the thesis and gives directions for future work.

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CHAPTER 2

REVIEW OF BIO-AMPLIFIER ARCHITECTURES

2.1 Introduction

Biopotential amplifiers (or simply bio-amplifiers) are the most critical building blocks of an EEG readout circuit. This is because they constitute its first stage and so largely determine its noise level, input impedance and CMRR. The major specifications of bio-amplifiers for clinical EEG applications are defined and driven by medical standards (Table 2-1). For wearable EEG devices with dry electrodes, the electrode-tissue impedance (ETI) can get quite large. As a result, the required input impedance, electrode offset tolerance, and power dissipation specifications are even tighter, while the CMRR and noise specifications of the bio-amplifier itself can be slightly relaxed.

This chapter presents an overview of state-of-the-art biomedical IAs that can be used as AEs for wearable EEG acquisition, discusses the advances and drawbacks of different architectures and describes several key circuit techniques to optimize critical specifications such as noise level, input impedance, electrode offset tolerance, CMRR and power dissipation.

2.2 Bio-Amplifier Design Techniques

2.2.1 Chopper Modulation

1/*f* noise, or flicker noise is usually the dominant voltage noise source of a biopotential amplifier, because the bandwidth of 1/*f* noise is typically in the order of a few kHz, which is far beyond the EEG signal bandwidth of 100Hz. 1/*f* noise can be reduced by enlarging the size of input transistors. However, using extremely large input transistors not only increases the chip area but also induces significant parasitic capacitance, causing concerns for reduced input impedance and CMRR.

Chopper modulation [26] is a widely used technique for reducing an IA's low frequency noise and offset without disturbing continuous-time operation. In addition, by periodically swapping its inputs, chopping increases an IA's CMRR by averaging its gain mismatch. The operating principle of chopper modulation is shown in Figure 2.1, where a low frequency input signal is up-modulated to a chopping frequency (f_c) by a square wave modulator, then this signal is amplified by an IA and demodulated back to original baseband by another square wave modulator. On the other hand, the intrinsic offset and 1/*f* noise (below the chopping frequency) of the IA are up-modulated to f_c by the second square wave modulator. These residual signals at f_c, known as ripple, can be filtered by a low-pass filter (LPF) or otherwise suppressed by a ripple reduction loop [27].

Table 2-1: Medical standards and proposed specification.

	IEC60601-2-26* [28]	IFCN** [29]	Design Target for Wearable EEG
Supply Voltage	--	--	< 3.3V
Input Voltage Range	$1mV_{pp}$	--	$>1mV_{pp}$
Input Referred Noise (per channel)	$6\mu V_{pp}$	$1.5\mu V_{pp}$ $0.5\mu V_{rms}$ (0.5-100Hz)	$1\mu V_{rms}$ (0.5-100Hz)
HPF Cutoff Frequency	< 0.5Hz	< 0.16Hz	< 0.5Hz
Electrode Offset Tolerance	±300mV	--	±300mV
Input Impedance at 50/60 Hz	--	>100MΩ	> 100MΩ
CMRR at 50/60 Hz	--	110dB	>80dB
Power Consumption (per channel)	--	--	<100μW
Applications	Wet electrodes Clinical	Wet electrodes Clinical	Dry Electrodes BCI, Lifestyle, Wellness

*IEC60601 is a series of technical standards for the safety and effectiveness of medical electrical equipment published by the International Electrotechnical Commission.
**IFCN stands for International Federation of Clinical Neurophysiology.

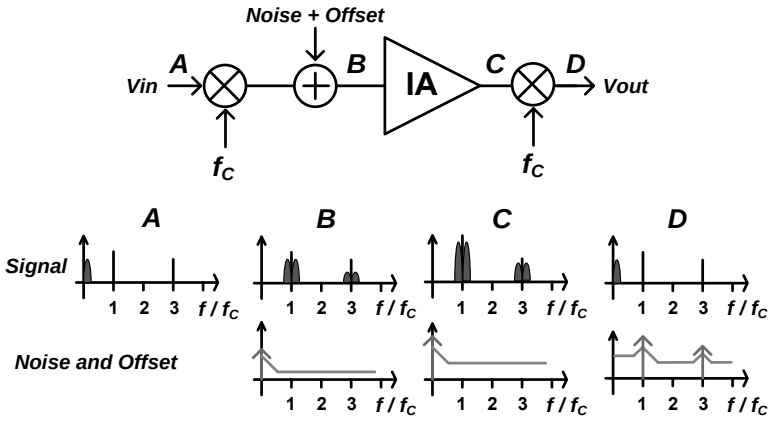

Figure 2.1 Chopper modulation technique to reduce IA's offset and 1/*f* noise.

2.2.2 Impedance Bootstrapping

AEs require high input impedance to minimize voltage division via skin-electrode impedance, especially in the case of a dry-electrode interfaces. Impedance bootstrapping has been used to improve IA input-impedance in various ways, but a proper positive feedback loop is always the fundamental element. In [30] and [31], the IA's output is fed back to bootstrap its input lead bias resistor (Figure 2.2 a), achieving very high input impedance suitable for non-contact EEG sensing. In [32], the input current is partially provided by a positive feedback loop (Figure 2.2 b), effectively increasing the IA's input impedance. In both cases, the input impedance can be bootstrapped to be infinitely large. Nevertheless, the amount of the positive feedback, either current or voltage, must be carefully controlled in order to maintain loop stability.

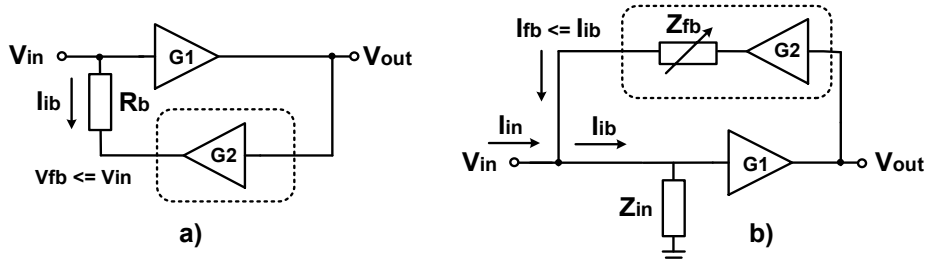

Figure 2.2 Impedance boosting techniques: a) voltage feedback based, and b) current feedback based.

2.2.3 Offset Compensation

Electrode offset, up to a few hundreds of mV, can easily saturate an instrumentation amplifier and therefore must be rejected or compensated. AC-coupling via RC components is the most obvious way of electrode offset rejection, as it ensures a rail-to-rail electrode offset tolerance without consuming any power. However, in order to eliminate the use of large passive components for better area efficiency, or to further compensate the residual offset, a DC-servo loop (DSL) is usually needed.

A DSL is a very effective and probably the only option for electrode offset compensation when passive AC coupling is not available. A DSL is based on negative feedback: the output offset is tracked and fed back to the input amplifier via current feedback (Figure 2.3 a) [33], or via voltage feedback (Figure 2.3 b) [34]. Both can compensate a certain amount of input electrode offset, from a few tens of mV to several hundreds of mV.

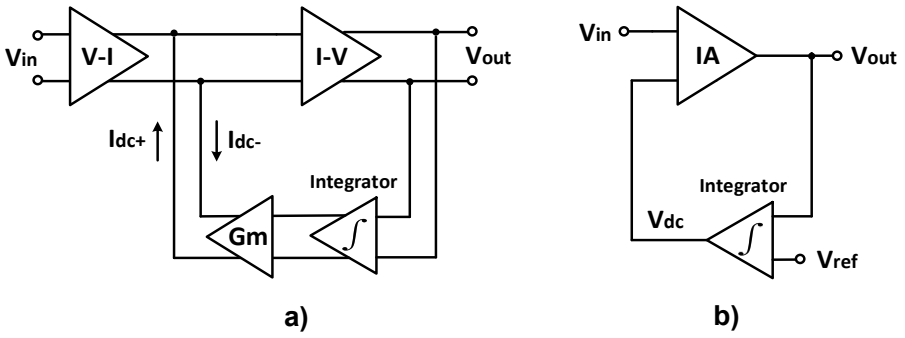

Figure 2.3 Electrode offset compensation techniques: a) current feedback based, and b) voltage feedback based.

2.2.4 Driven-Right-Leg (DRL)

There are two mechanisms that limit the practical CMRR of an EEG acquisition system: mismatch of electrode-tissue impedance (ETI) and gain mismatch of the AEs. The former can be mitigated by maximizing the AE's input impedance, while the latter can be reduced by chopping. Unfortunately, chopping between two AEs is not practical for an AE-based system, where the AEs are mounted on separate electrodes and are placed far from each other. As a result, the component mismatch of the AEs usually leads to a low CMRR (< 60dB).

The most well-known circuit for CMRR enhancement is the Driven-Right-Leg (DRL) circuit (Figure 2.4) [35], where the common-mode (CM) input signal is tracked and fed back to the subject through a third electrode, i.e., the bias electrode. Since the electrode-tissue impedances (Z_e and Z_{rl}) are also in the feedback loop, the DRL technique improves CMRR by reducing the common mode impedance to the IA, resulting in less pickup of common mode signals from the human body. However, large (external) capacitors (a few nF) and current limiting resistors (a few 100kΩ) are required to make the loop stable. When dry electrodes are used, it becomes difficult to achieve stability over a wide impedance range (100kΩ-10MΩ), when both electrode offset and electrode impedance mismatch exist.

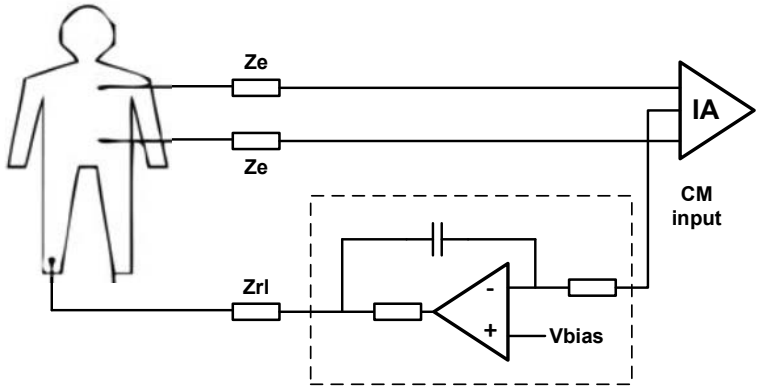

Figure 2.4 Driven-Right-Leg (DRL) circuit for CMRR enhancement.

2.3 Bio-Amplifier Architectures

2.3.1 Analog Buffers

Most AEs have been simple analog buffers. This confers advantages in terms of large input dynamic range, low output impedance, and low gain variation. Without any added functionality, a buffer requires only a 3-wire connection (V_{dd}, V_{ss} and V_{out}) to the back-end electronics. Several variants have been published with even fewer wires. In [36], the buffer's analog output is shared with the negative supply voltage of the buffer in a single wire through a current driver, at the cost of less input dynamic range (Figure 2.5 a). Similarly, in [37], the analog output is shared with the positive supply voltage (V_{dd}) of the buffer, however, this requires higher supply voltage and power dissipation (Figure 2.5 b).

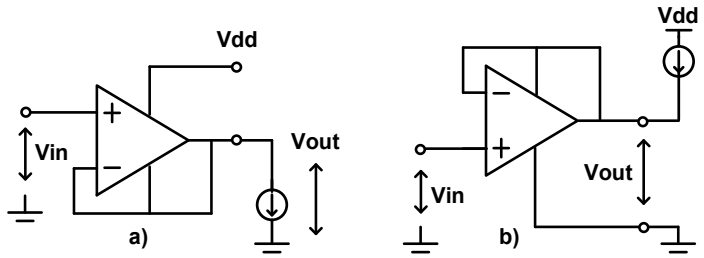

Figure 2.5 IC techniques to reduce the number of wires of an AE: a) analog output shared with the negative supply voltage of the buffer, and b) analog output shared with the positive supply voltage of the buffer.

A major drawback of buffer-based AE systems is their power efficiency: the buffer requires significant power to meet a low noise specification. However, the buffer only performs impedance conversion without providing any voltage gain nor rejecting electrode offset. The subsequent back-end circuit still needs to tackle the same challenges of low noise and large DC tolerance, leading to additional power consumption. A detailed power comparison of AEs, implemented with buffers or amplifiers, will be presented in Chapter 3.

2.3.2 Inverting AC-coupled Amplifiers

An inverting amplifier with resistive feedback (Figure 2.6 a) is rarely used in biomedical application because the input resistors generate noise and determine IA's input impedance. Compared to resistive feedback IAs, AC-coupled amplifiers with capacitive feedback (Figure 2.6 b) [38] have been widely used for wearable and implantable medical devices [39][40] because of their rail-to-rail offset rejection capability[1], area efficiency and low power consumption. The input coupling capacitor C_1 rejects any electrode offset from the leads. Resistors R_2 can be implemented with pseudo resistors [38], resulting in resistances of tens of GΩ. This feature makes it easy for such IAs to achieve low cutoff frequencies (< 0.5Hz) with small on-chip capacitors, in the order of several pF.

The power efficiency of a bio-amplifier can be quantified by the noise efficiency factor (NEF) [41], which represents an IA's noise and power tradeoff in a certain bandwidth:

[1] Except when using chopper modulation scheme in Figure 2.7 (a)

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \tag{2-1}$$

where $V_{ni,rms}$ is the input-referred root mean square (rms) noise voltage, I_{tot} is the total supply current, U_T is the thermal voltage kT/q, and BW is the IA's (-3dB) bandwidth. A state-of-the-art IA with capacitive feedback achieves an NEF of 1.74 [42] by combining a low supply voltage with current reuse techniques. It exploits the fact that the amplifier's input is at virtual ground and so the core amplifier only needs to have a small input dynamic range.

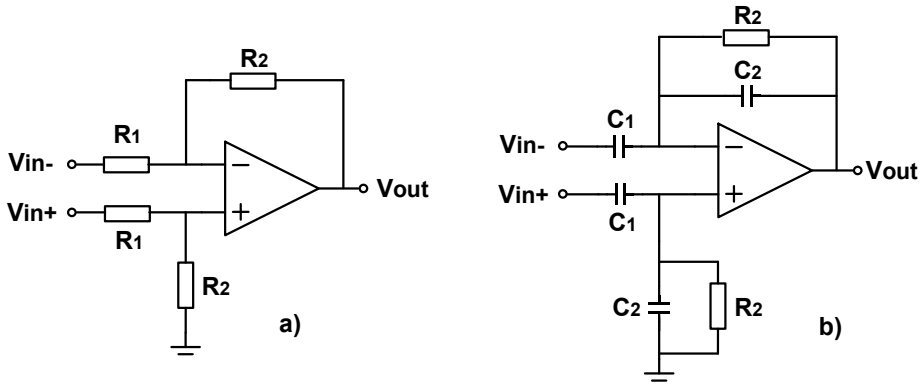

Figure 2.6 Inverting amplifiers: a) resistive feedback, and b) capacitive feedback.

Chopping can further reduce the 1/*f* noise of this type of IAs. As shown in Figure 2.7, chopper modulation can be applied at location (a) or (b) to mitigate 1/*f* noise and improve the NEF.

The IAs in [32][43] apply input chopper modulation before the input capacitor (Figure 2.7 a) to mitigate 1/*f* noise. One major drawback of this chopper IA topology is its limited tolerance to electrode offset, because it is basically a high-gain DC-coupled amplifier. Although the input DC signal can be partially cancelled by a DC feedback loop (Figure 2.8) [32][43], the tradeoff between the amount of feedback current and the input noise still limits the maximum DC tolerance to a few tens of mV. Furthermore, the input impedance of this chopper IA is limited by the switched capacitor impedance associated with its input capacitors. To address these issues, an alternative chopper modulation

approach places the input chopper inside the capacitive feedback loop (Chapter 3), i.e., at the virtual ground (Figure 2.7 b) [44]. This architecture retains the benefits of a non-chopped capacitive feedback IA, in terms of high input impedance, large electrode offset tolerance and low power, while mitigating 1/*f* noise through chopping. In addition, an impedance boosting loop, a ripple reduction loop and an offset calibration loop can be added for even better performance (Chapter 3). A single-ended version of such IAs can also be used as an AE [45].

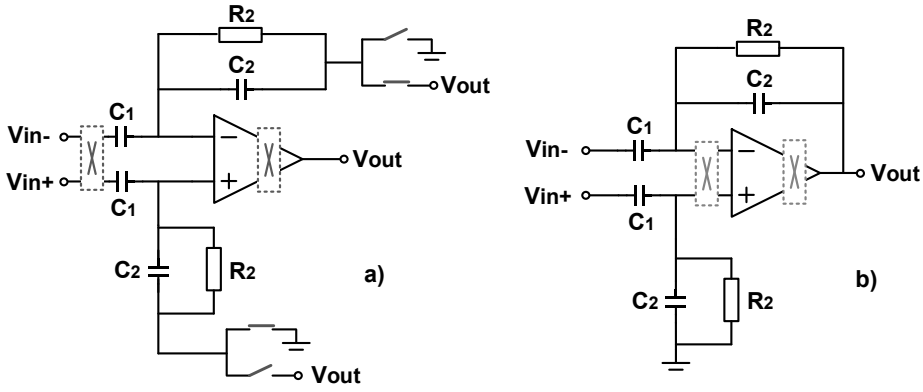

Figure 2.7 AC-coupled inverting amplifier with alternative chopping schemes: a) before the input capacitor, and b) after the input capacitor.

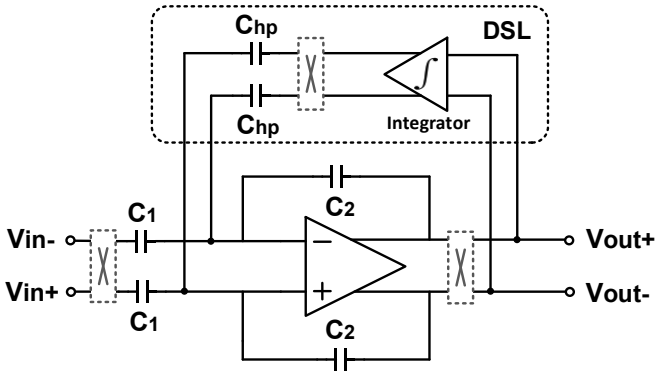

Figure 2.8 Capacitively-coupled chopper amplifier with a DC servo loop.

2.3.3 *Non-inverting AC-coupled Amplifiers*

A non-inverting IA (Figure 2.9 (a)) has a single-ended input and, since its input impedance is determined by parasitic capacitance (C_p), a higher input-impedance than an inverting IA. AEs utilizing resistor feedback were published in [46][47]. However, this is not an area-efficient solution because it requires large and accurate resistors. Moreover, these resistors also increase the input noise. An alternative solution is a capacitive feedback network (Figure 2.9 (b)) [48][49], which improves the tradeoff between low noise and area efficiency. Moreover, the resulting IA has a DC gain of 1 and so can accommodate relatively large electrode offsets. However, when chopping is utilized, the increased input bias current, due to charge injection, may create a significant offset voltage via the feedback resistor [44]. Therefore, a non-inverting chopper IA usually incorporates a DC-servo loop (DSL) (Figure 2.9 (c)) for electrode offset compensation [48][49] (Chapter 4).

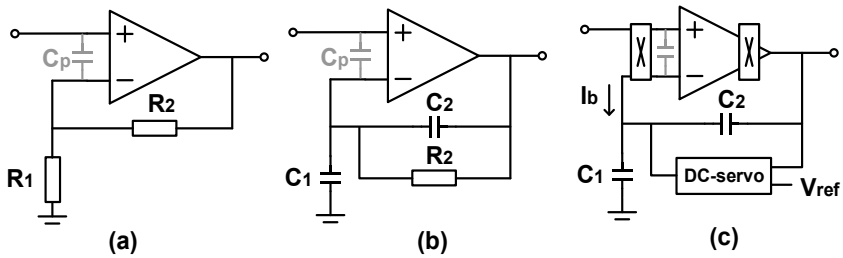

Figure 2.9 Non-inverting amplifiers with (a) a resistive feedback, (b) a capacitive feedback, and (c) a DC servo loop.

2.3.4 *Instrumentation Amplifiers*

Instrumentation amplifiers (Figure 2.10) are also widely used in biopotential measurements because of their high input impedance. However, a DC-coupled IA [50][51] has limited electrode offset tolerance; therefore, conventional IA architectures are not directly applicable to dry-electrode EEG measurement. A DC-coupled current-balancing IA equipped with a DC-servo loop [33] solves this problem (Figure 2.11) by effectively creating an AC-coupled IA. The IA's noise is further improved through chopping. However, this IA's electrode offset tolerance is still limited to a few tens of mV because the DC-servo loop is implemented as a voltage-to-current feedback loop, where a significant amount of feedback current will be required to compensate a large electrode offset.

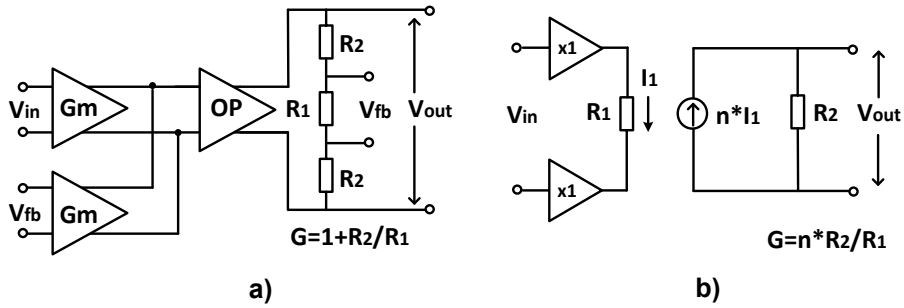

Figure 2.10 Instrumentation amplifiers: a) current feedback architecture, and b) current balancing architecture.

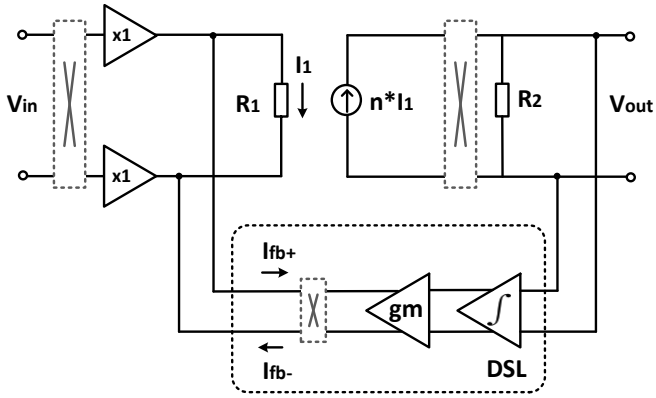

Figure 2.11 Current-balancing instrumentation amplifier with a DC-servo loop.

2.3.5 "Functionally" DC-coupled Amplifiers

An AC-coupled IA achieves large electrode offset tolerance, but this comes at the cost of filtering out low frequency signals, which may contain useful information, such as low frequency surface potentials [52]. In contrast, a DC-coupled IA, such as an inverting IA with resistive feedback, a non-inverting IAs with resistive feedback, or a current feedback IA, preserves such information. However, its voltage gain is constrained by electrode offset and supply voltage and will typically be quite low (<10). As a result, achieving a wide input dynamic range requires a high-resolution ADC (>16b). This, in turn, significantly increases the system's power dissipation, especially when multi-channel (>24) EEG acquisition is required, as each channel needs a power-hungry ADC [53].

A “functionally” DC-coupled IA (Figure 2.12) [34] combines the merits of an AC-coupled IA and a DC-coupled IA, i.e., compensating for large electrode offsets with low power while still being DC-coupled. This is realized by using a voltage-to-voltage feedback (Figure 2.3 b) instead of a voltage-to-current feedback (Figure 2.3 a), which suffers from the tradeoff between electrode tolerance, noise, and power consumption [43]. Although an external capacitor is used in the feedback loop to achieve a very low cutoff frequency, the “functionally” DC-coupled IA (Chapter 6) can cope with a few hundred mVs of electrode offset, while retaining the same transfer function as a standard DC-coupled amplifier, except for the DC signal not being amplified.

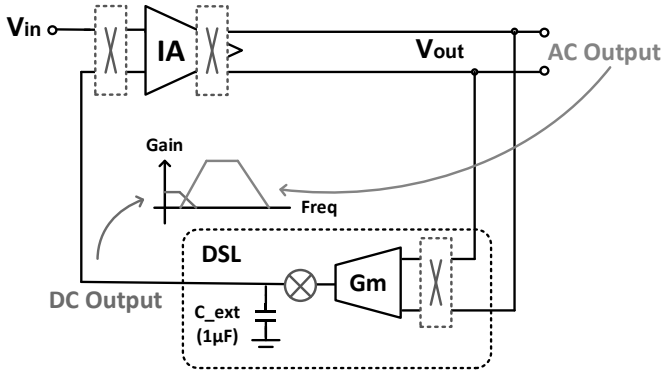

Figure 2.12 “Functionally” DC-coupled IA.

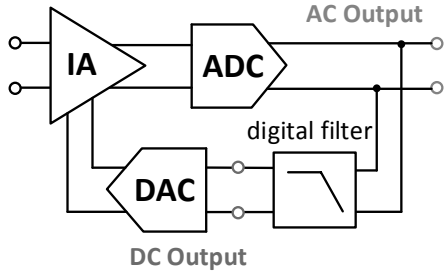

Figure 2.13 IA with a digitally-assisted offset compensation.

This architecture is also applicable to a differential EEG amplifier [54], and the DSL can be implemented in a digitally-assisted manner [55]. Low-pass filtering in the digital domain has the advantage of power and area efficiency. However, the electrode offset is fed back to the IA through a DAC, which needs to be carefully designed to reduce its quantization noise. The digital out-

put containing the information of electrode offset and extremely low frequency signals is directly available at the DAC's input (Figure 2.13).

2.3.6 Summary

Table 2-2 summarizes the advantages and limitations of different bio-amplifier architectures to evaluate their usability for wearable EEG acquisition. There is clearly no golden IA architecture with optimum performance because of the tradeoffs between its various specifications. In addition, when IAs are used as AEs, the CMRR of a pair of AEs will be limited by the gain mismatch of their IAs, which is independent of the IAs' intrinsic CMRR, and therefore must be compensated at the system level. A major goal of this thesis is to explore the circuit design techniques to maximize the IAs' overall performance, at both block level and system level, in order to make them suitable for AE-based EEG acquisition.

Table 2-2: Comparison of IA Architectures for Active Electrode based EEG Acquisition.

AE Architectures	Buffer	AC-coupled IA		DC-coupled IA	
		Inverting	Non-inverting	DC-coupled	"Functionally" DC-coupled
Electrode Offset Tolerance	High	High	Medium*	Low	High
Noise (with chopping)	Low	Low**	Low**	Low	Low
Input Impedance	High	Medium***	High	High	High
CMRR**** (of two IAs)	High	Low	Low	Low	Low
System Power Efficiency	Low	High	High	High	High

* Electrode offset tolerance is limited by the input dynamic range of the IA.

** Low-frequency noise (<10 Hz) is high due to $1/f^2$ noise contribution.

*** Input impedance is limited by the input coupling capacitors.

**** Without CMRR enhancement techniques.

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CHAPTER 3

AN ACTIVE ELECTRODE READOUT CIRCUIT[2]

3.1 Introduction

In this chapter, an AE with gain is presented, which results in a better noise-power tradeoff than an analog buffer. The AE is based on an instrumentation amplifier (IA), which achieves state-of-the-art analog performance, making it suitable for dry- electrode EEG acquisition.

The IA utilizes an AC-coupled chopper amplifier topology, equipped with impedance boosting and digitally-assisted offset trimming for improved performance. As a result, the AE's input impedance (at 1Hz) is increased by a factor of 5 and the residual ripple and offset is reduced by a factor of 20 and 14, respectively. Thanks to the chopping technique, each AE achieves an input referred noise of $0.8\mu V_{rms}$ (0.5-100Hz).

Mismatch between AEs is a dominant contributor of a low CMRR. This problem is addressed by a back-end common-mode feedback (CMFB) circuit, which improves the CMRR of a pair of AEs by 30dB.

The AE-based EEG readout circuit is also benchmarked with a conventional EEG acquisition system, demonstrating the AE's benefits, namely reduced sensitivity to cable motion artifacts and mains interference.

3.2 IC Architecture Overview

The proposed EEG readout circuit (Figure 3.1) consists of eight front-end AEs implemented with eight chopper IAs and one back-end voltage summing amplifier for common-mode feedback (CMFB).

[2] This chapter is derived from a journal publication of the authors: J. Xu, R.F. Yazicioglu, et al., "A 160μW 8-channel active electrode system for EEG monitoring," *IEEE Trans on Biomed Circuits and Systems*, vol. 5, no. 6, pp. 555-567, Dec. 2011.

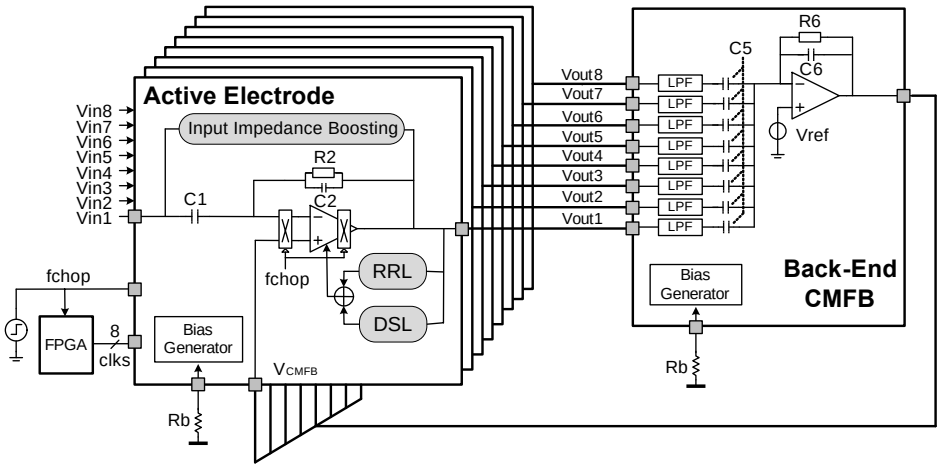

Figure 3.1 Block diagram of the 8-electrode readout circuit.

The front-end AEs are responsible for transparent pre-amplification of EEG signals. To achieve this goal, several popular design techniques of bio-amplifiers are combined. Firstly, the AE utilizes a capacitive feedback IA architecture for rail-to-rail tolerance of electrode offset. Secondly, chopper modulation is performed at the amplifier's virtual ground to mitigate 1/*f* noise [56]. Thirdly, the AE includes an input-impedance boosting loop for high input impedance [57]. Lastly, a ripple reduction loop (RRL) and a DC servo loop (DSL) compensate the intrinsic non-idealities of the chopper IA [58].

The back-end summing amplifier (Figure 3.1) is responsible for CMRR improvement between multiple AEs. This back-end amplifier performs common-mode (CM) signal extraction and feeds the input CM voltage of all eight AEs back to their non-inverting inputs (via V_{CMFB}). As a result, the CMFB scheme reduces the CM gain of these AEs for a high CMRR (see section 3.4).

3.3 Active Electrode ASIC

The AEs, modeled as single-ended IAs, must achieve balanced analog performance, i.e., balancing input impedance, electrode offset tolerance, noise, CMRR and power to facilitate dry-electrode EEG recording. However, state-of-the-art IAs are not well suited for this application. The capacitively-coupled IA in [57] has limited input impedance, formed by input switched-capacitor impedance. Moving the chopper to the amplifier's virtual ground solves this problem at the cost of reduced CMRR [56]. A current feedback IA has good input impedance

and CMRR, but its DC-servo loop limits the maximum electrode offset tolerance to 50mV.

This section proposes a capacitively-coupled chopper IA similar to [56], with inherent capability for large offset rejection and low integrated noise (100Hz bandwidth). Furthermore, several additional circuit techniques are employed to enhance its input impedance, output dynamic range and CMRR.

Detailed implementations of the core IA, including the offset trimming loops (RRL and DSL) and the impedance boosting loop, are discussed in section 3.3.1, 3.3.2 and 3.3.3, respectively.

3.3.1 An AC-coupled Inverting Chopper IA

The IA's voltage gain is determined by the ratio of its feedback capacitors C_1/C_2 (Figure 3.1). Variable gains (3, 10, 50 and 100) can be realized by switching between different values of C_2. The pseudo-resistor R_2 and capacitor C_2 determine the AE's high-pass cutoff frequency [59]. The coupling capacitor C_1 rejects any electrode offset in a power efficient manner. Furthermore, the IA (Figure 3.2) must have a large output dynamic range to accommodate (large) input motion artifacts and interference, superimposed on an EEG signal. Therefore, the core IA utilizes a folded cascode OTA, known for a good balance between output voltage swing and power consumption.

Chopper modulation is used to achieve low noise. The input modulator is placed before input transistors (M_1 and M_2), up-modulating the IA's input signals. The output modulation is performed at the low impedance nodes before the dominant pole (at V_{out}), such that the chopping frequency is not limited by the IA's bandwidth [60].

The IA also consists of two pairs of auxiliary current steering DACs (CA_1-CA_4) to compensate the chopper IA's non-idealities. The motivation and detailed operation of these DACs are discussed in section 3.3.2.

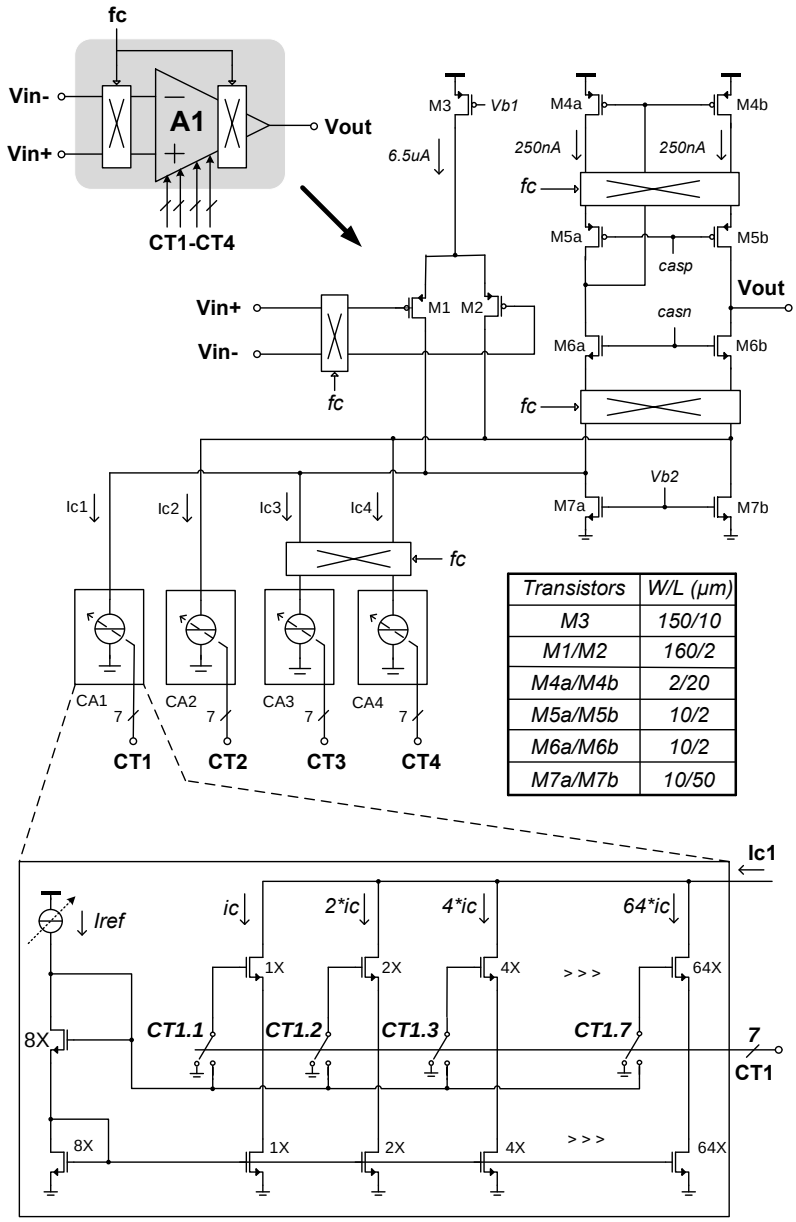

Figure 3.2 Chopper IA with current steering DACs.

3.3.2 Digitally-Assisted Ripple and Offset Reduction

Two challenges associated with a chopper IA are how to reduce its output ripple and residual offset (Figure 3.3). The output ripple is generated by the IA's up-modulated offset voltage (V_{off}) and resembles a low-pass filtered square wave. Compared to the μV level EEG signals, the ripple can have a much larger magnitude and will, therefore, limit the IA's output headroom. The ripple magnitude is proportional to the IA gain, as shown in (3-1). For instance, a 5 mV input offset can cause a large output ripple of 500mV$_{pp}$ (when C_1/C_2=100).

$$\left|V_{ripple,pp}\right| = \left|V_{off}\right| \cdot \left(\frac{C_1 + C_2}{C_2}\right) \tag{3-1}$$

The residual offset $V_{off,out}$ of the IA is caused by its input offset current I_{os} (Figure 3.3) [61], which in turn is mainly due to the charge injection of the input chopper. The residual output offset is derived as (3-2), where I_{os} is the offset current that flows through the pseudo-resistor R_2 and R_p, and C_i is IA's input capacitance, R_p is IA's parasitic switched-capacitor resistor formed by input chopper and C_i.

$$V_{off,out} = I_{os}R_2 = \frac{V_{os}R_2}{R_p} = f_c C_i R_2 V_{os} \tag{3-2}$$

The residual offset can be compensated by a DC servo loop [62], where an off-chip capacitor (>10μF) and an OTA realize a low-pass cutoff frequency of around 0.5Hz. In the proposed AE, however, the ripple and the offset are suppressed by two foreground calibration loops: a ripple reduction loop (RRL) and a DC servo loop (DSL). It should be noted that the EEG input signal should not be present during the calibration.

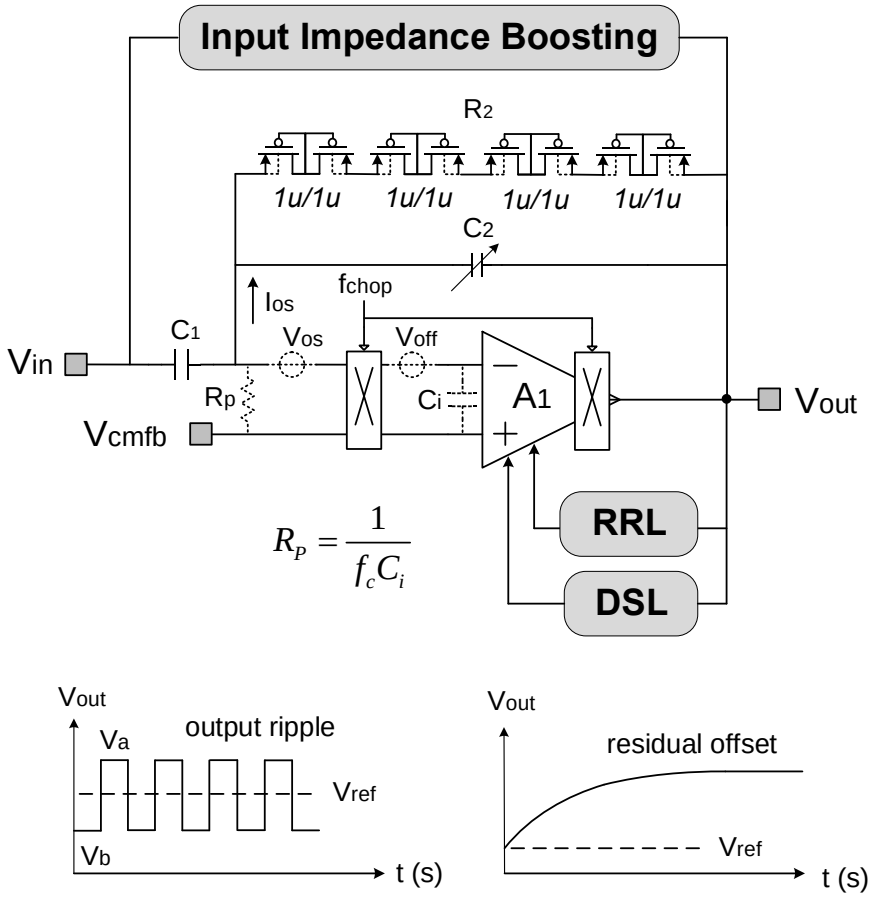

Figure 3.3 Chopper-associated output ripple and residual offset.

The calibration starts with the RRL (Figure 3.4): the ripple V_a and V_b are synchronously sampled, and the polarity (CMP_1) is determined by a comparator. A fully-integrated successive approximation algorithm (SAR) generates a pair of 7-bit binary outputs (CT_1 and CT_2) to control a pair of 7-bit current steering DACs (CA_1 and CA_2 in Figure 3.2), respectively. The outputs of the SAR have inverse polarity, so that either a segment from the left DAC (CA_1) or from the right DAC (CA_2) is switched on after each comparison. Therefore, the DACs generate compensation currents (I_{C1} and I_{C2}) to minimize the output ripple in seven clock cycles. The timing of the RRL's operation is illustrated in Figure 3.5.

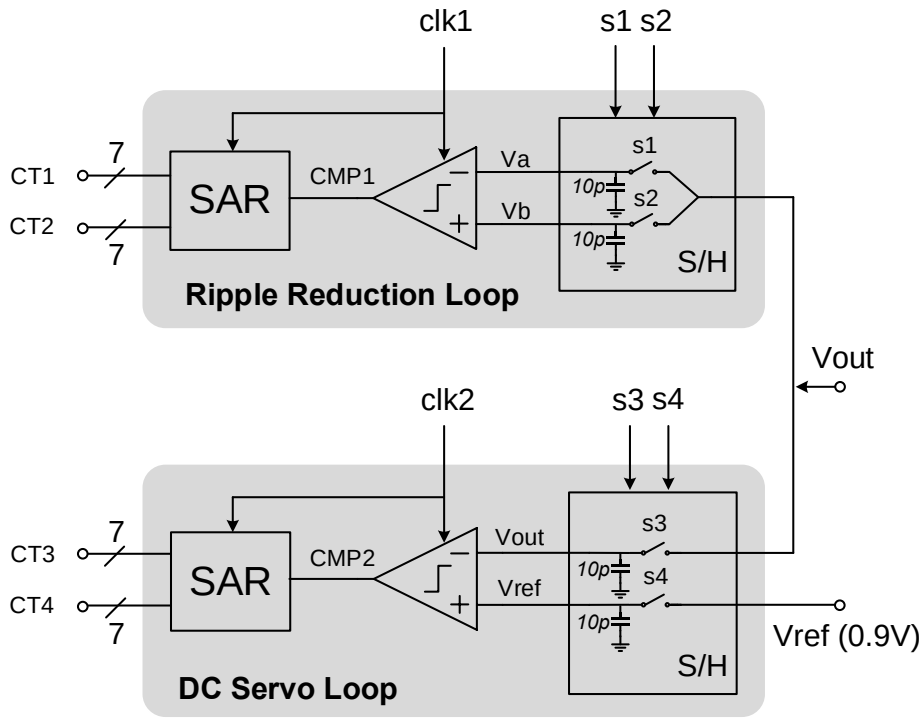

Figure 3.4 Block diagrams of the RRL and the DSL.

The DSL starts after the RRL and operates in a similar manner (Figure 3.4): the output offset voltage (V_{out}) is sampled and compared to a reference voltage V_{ref}. The comparator output (CMP_2) is sent to the SAR, whose outputs control another pair of DACs (CA_3 and CA_4 in Figure 3.4). Their outputs are chopper modulated in order to generate a modulated compensation current. The timing of the DSL's operation is also illustrated in Figure 3.5.

Once both the RRL and the DSL calibration are finished, the inputs to the DACs are frozen, both calibration loops are shut-down, and normal operation starts. In addition, the calibration loops can be reset when necessary, in case there is any offset drift. The total power dissipation (<400nW) of the RRL and the DSL is determined by the DAC's static current.

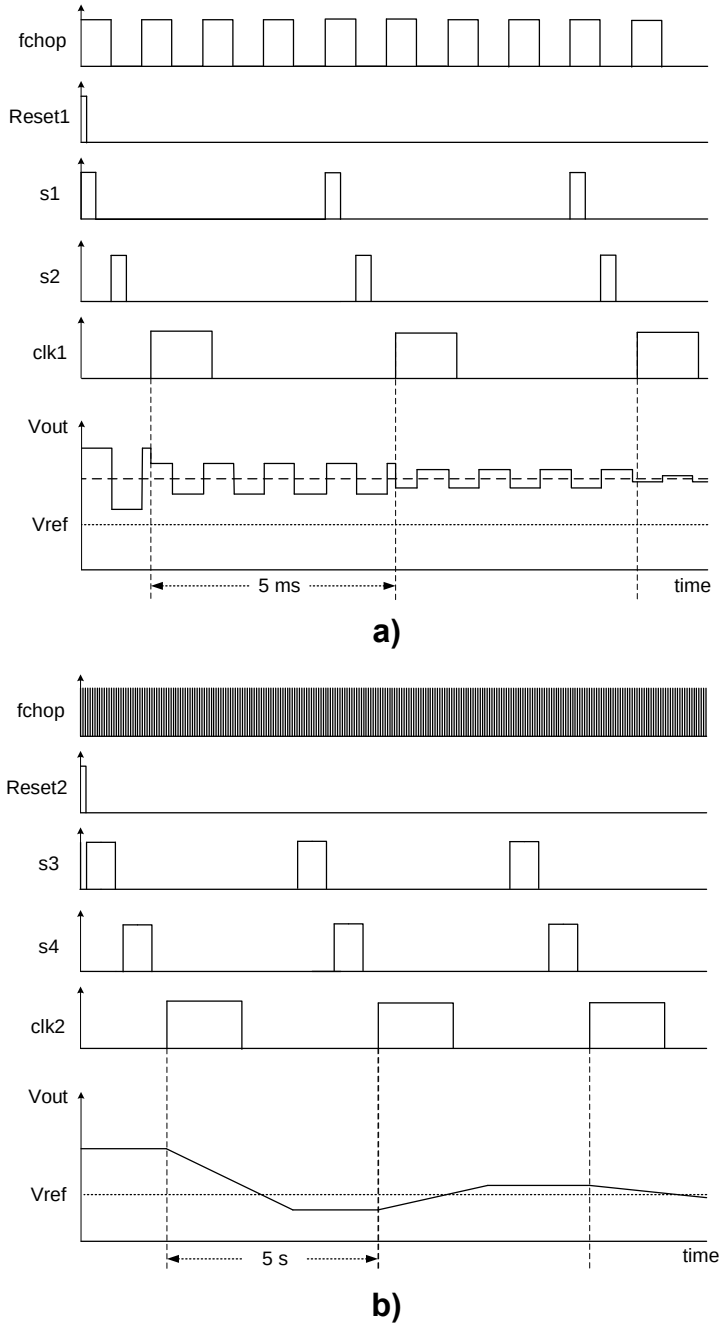

Figure 3.5 Timing diagrams of a) the RRL, and b) the DSL.

3.3.3 Input Impedance Boosting

Without an input-impedance boosting loop, the input impedance of the inverting IA is dominated by C_1 (Figure 3.6). This is shown in (3-3), where C_p is the input parasitic capacitance of the IA, and R_s is the electrode-tissue impedance.

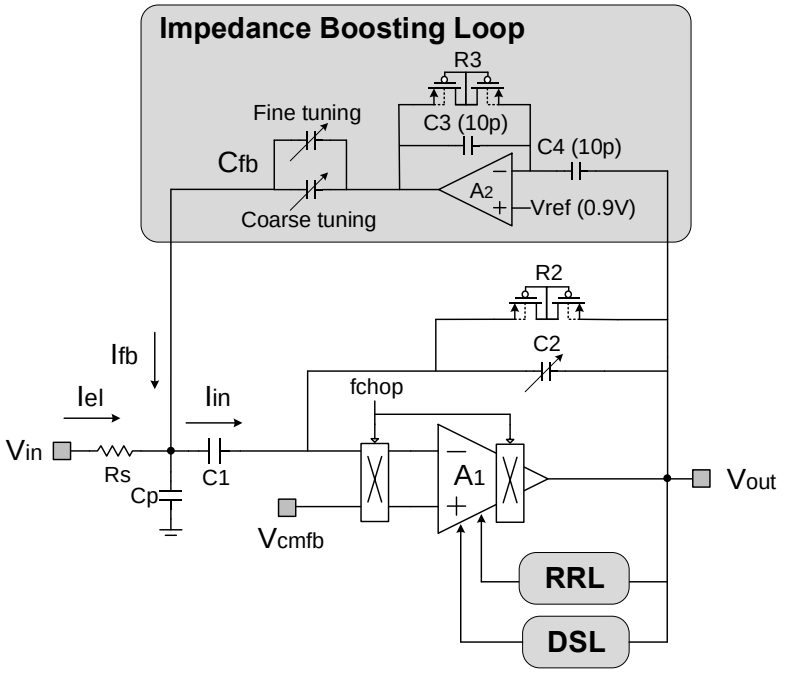

Figure 3.6 Input-impedance boosting via positive feedback.

$$Z_{in} = \frac{1}{s(C_1 + C_p)} + R_s \approx \frac{1}{sC_1} \tag{3-3}$$

In case C_1 is large (300pF) for low-noise operation (see section 3.3.4), the input impedance is around 10MΩ at 50Hz. This may lead to a poor CMRR when an electrode impedance mismatch exists. In order to increase the input impedance, a positive feedback loop (Figure 3.6) is implemented by feeding

back an input bias current [57]. This loop consists of an inverting amplifier and a capacitor C_{fb}, which includes C_{fb_coarse} and C_{fb_fine}. C_{fb} converts the inverted output into an input bias current (I_{fb}), which is a portion of the total input current I_{in}. Therefore, the current (I_{el}) drawn from the recording electrode is reduced.

$$Z_{in} = \frac{V_{in}}{I_{el}} = \frac{1}{s(C_1 + C_p) - sC_{fb}\left[\frac{s^2 C_1 C_4 R_2 R_3}{(sC_2R_2+1)(sC_3R_3+1)} - 1\right]} \tag{3-4}$$

The input impedance Z_{in} of the AE, after utilizing the impedance boosting loop, can be expressed as in (3-4). Compared to (3-3), the equivalent input impedance has been increased by a factor of β, as shown in (3-5).

$$\beta = \frac{Z_{in}^{'}}{Z_{in}} = \frac{C_1 + C_p}{C_1 + C_p - C_{fb}\left(\frac{C_1 C_3}{C_2 C_4} - 1\right)} \approx \frac{C_1 + C_p}{C_1 + C_p - A_{V,IMP} C_{fb}} \tag{3-5}$$

where β is the impedance boosting factor, Z_{in} is the AE's input impedance of without impedance boosting, Z'_{in} is the AE's input impedance with impedance boosting and $A_{V,AMP}$ is the effective voltage gain of the impedance boosting loop (excluding C_{fb}). Ideally, the input impedance of the AE can be infinite (β is infinite large, and $I_{el} = 0$). However, the boosting factor is limited by stability constrains. Making C_{fb} too large will result in $\beta < 0$, which translates into negative input impedance and an unstable feedback loop, because a portion of the feedback current (I_{fb}) then flows out into the electrode (i.e., $I_{el} < 0$). Therefore, the maximum value of C_{fb} must be limited as in (3-6) to maintain $\beta > 0$:

$$C_{fb,\max} = \frac{C_1 + C_p}{A_{V,IMP}} \tag{3-6}$$

An additional remark of (3-5) and (3-6), is the variation of C_1 and the input parasitic capacitances C_p. Both can reduce the effective boosting factor β, and may even lead to instability ($\beta < 0$). Therefore, C_{fb} is implemented as a combination of a coarse and a fine capacitor array in order to be able to trim the amount of positive feedback to compensate the effects of these process variation and ill-defined parasitic capacitance. At variable gain settings, the coarse array C_{fb_coarse} is switched in tandem with the value of C_2. The fine array C_{fb_fine} can then be adjusted to further compensate for the current that flows into C_1 and C_p, thus ensuring that β is high enough to guarantee stability. The selected C_{fb_fine} array (25pF) can compensate for a 20% variation in C_1 (at the lowest gain of 3), and tolerate a large C_p of up to 15pF.

3.3.4 Noise Analysis

The equivalent circuit for input noise derivation is shown in Figure 3.7, the total input referred noise PSD of a Front-End AE (FEAE) can be derived as

$$\begin{aligned}\overline{V_{in,FEAE}^2} &= \left(\overline{V_{in,OTA1}^2} + \overline{V_{in,cmfb}^2}\right)\cdot\left(1+\frac{C_2}{C_1}+\frac{2\pi f_c C_i}{sC_1}\right)^2 \\ &+ \overline{V_{in,FEAE}^2}\cdot\left(\frac{1}{sC_1R_2}\right)^2 + \left(\overline{V_{in,OTA2}^2} + \overline{V_{in,ref}^2}\right)\cdot\left(2sR_sC_{fb}\right)^2 \\ &+ \left(\overline{V_{in,RRL}^2} + \overline{V_{in,DSL}^2}\right)\cdot\left(\frac{g_{m,DAC}}{g_{m1}}\right)^2\end{aligned} \tag{3-7}$$

where $V_{in,FEAE}$ is the total input referred noise of an AE; $V_{in,OTA1}$ and $V_{in,OTA2}$ are the input referred noise of the amplifier A_1 and A_2, respectively; $V_{in,cmfb}$ is the (common-mode) noise of the back-end CMFB amplifier; $V_{n,R2}$ is the noise contribution of the pseudo-resistor R_2; $V_{in,ref}$ is the noise of the reference voltage, which biases the inverting amplifier in the impedance boosting loop; $V_{in,RRL}$ and $V_{in,DSL}$ are the noise from the RRL and the DSL, respectively; $g_{m,DAC}$ is the transconductance of the current steering DACs; and g_{m1} is the input transconductance of the core amplifier A_1.

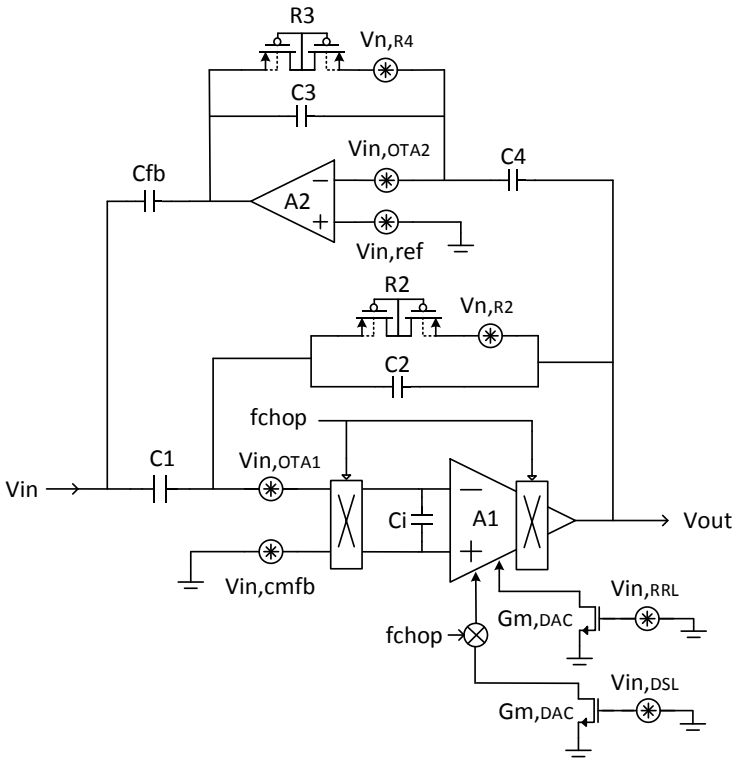

Figure 3.7 Input equivalent circuit for calculating the input referred noise of the front-end active electrode.

The noise of the impedance boosting loop ($V_{in,OTA2}$ and $V_{in,ref}$) is negligible as long as $1/sC_{fb} >> R_s$. The noise generated from the pseudo-resistor R_2 is also very small as $sC_1R_2 >> 1$. The noise of the RRL and the DSL is not dominant either because $g_{m1} >> g_{m,DAC}$. The noise from the CMFB loop is common-mode noise for multiple AEs. Hence, the total input referred noise of a single AE can be approximated as

$$\overline{V_{in,FEAE}^2} = \overline{V_{in,OTA1}^2} \cdot \left(1 + \frac{C_2}{C_1} + \frac{2\pi f_c C_i}{sC_1}\right)^2 \tag{3-8}$$

This noise approximation is equal to the thermal noise of the core chopper IA, multiplied by a shaping factor (Figure 3.8). This factor has its origins in the fact that the combination of the input chopper and the input capacitor C_i behaves like a parasitic switched-capacitor resistor, and so $V_{in,FEAE}$ exhibits a $1/f^2$ frequency characteristic. However, this approximation does not include the current noise contribution from the input chopper. The current noise can be converted into significant $1/f^2$ voltage noise as well when chopping is performed at a very high impedance node, i.e., at the virtual ground of this inverting IA. A detailed discussion of this current noise can be found in Chapter 5.

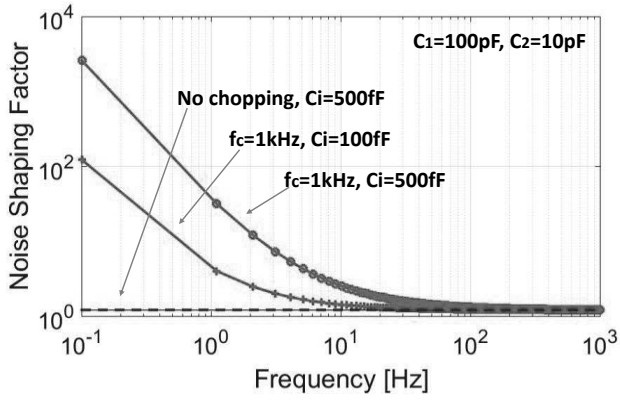

Figure 3.8 Noise shaping factors on various conditions of chopping frequency (fc) and differential input parasitic capacitance (Ci).

Several design considerations should be taken into account to reduce the noise-shaping factor in (3-8). A large coupling capacitor C_1 should be used as long as the input impedance still meets the design requirements. The chopping frequency f_c should be selected very close to the $1/f$ corner of the core IA. In this design, a minimal f_c of 500Hz is selected without significantly compromising the noise floor of the chopper IA. Moreover, the input parasitic capacitor C_i can be reduced by careful layout.

3.4 Back-End CMFB IC

Mismatch between AEs usually dominates their CMRR. This can be improved by a back-end common-mode feedback (CMFB) circuit. Figure 3.9 shows the equivalent circuit of a simplified two-AE system and its CMFB circuit. Without the CMFB circuit, the reference inputs of AEs are connected to ground. There-

fore, the CM gain is determined by the AEs' gain mismatch (ΔA_V), leading to a low CMRR as shown in (3-9).

$$CMRR = 20\log\left(\frac{A_V}{\Delta A_V}\right) \tag{3-9}$$

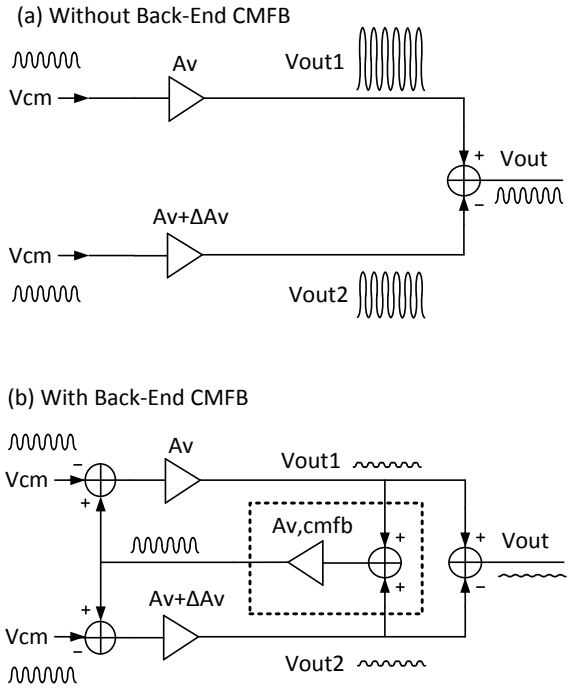

Figure 3.9 Equivalent circuits of the proposed AE system, (a) without CMFB (b) with CMFB.

With the CMFB, however, the reference inputs of the AEs are connected to the output of the CMFB, which is approximately equal to the input CM of all AEs. Thanks to the CMFB, which reduces the CM gain, the residual CM outputs V_{out1} and V_{out2}, as well as the differential output (V_{out}). The new CMRR', by using the CMFB, is derived in (3-10), where the CMRR is improved by a factor of 20log (A_V). In (3-10), A_V is the close-loop voltage gain of the AE, and $A_{V,CMFB}$ is the CM gain of the capacitive summing amplifier.

$$CMRR' = CMRR \cdot 20\log\left(\frac{2A_V}{2+\frac{1}{A_{V,CMFB}}}+1\right) \approx CMRR \cdot 20\log\left(A_V\right) \quad (3\text{-}10)$$

The back-end CMFB circuit (Figure 3.10) consists of a capacitive summing amplifier with a gain of $A_{V,CMFB} = 8\times(C_5/C_6)$, and eight unit-gain low-pass filters to reject high-frequency interference. The coupling capacitors (C_5) block the residual output offsets of the AEs, thus avoiding summing amplifier's saturation. Via a pseudo resistor R_6, the summing amplifier provides a bias voltage to (V_{ref}) to all AEs. In an 8-electrode EEG readout circuit, any two AEs can be used to form a bipolar EEG acquisition channel. The summing amplifier only feeds the average CM voltage of all 8 AEs back to their reference inputs while rejecting any differential-mode (DM) signals. Therefore, the back-end CMFB circuit does not disturb the differential EEG amplification.

The practical CMRR improvement is limited by the stability constrains of the CMFB loop. In order to balance the tradeoff between CMRR and the loop stability, the gain of AE and the summing amplifier is set to 100 and 16, respectively.

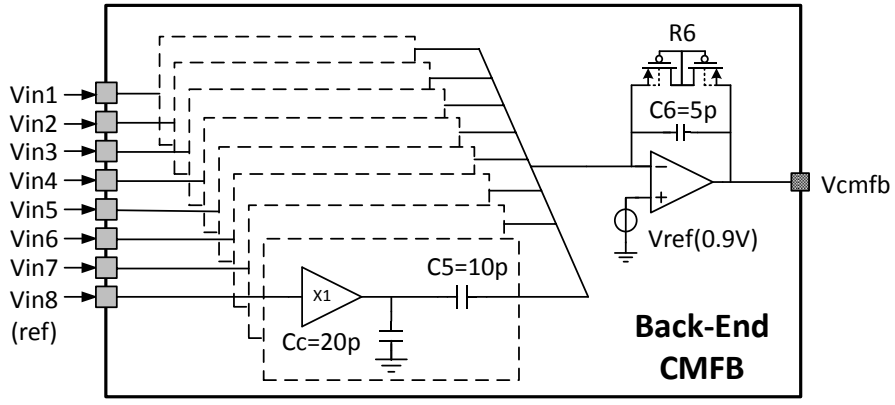

Figure 3.10 Block diagram of the back-end CMFB circuit.

In practice, electrode impedance mismatch is another mechanism further reducing the CMRR of a pair of AEs, especially when dry electrodes are used. In the case of CMFB not being used (Figure 3.11), the CMRR of an AE pair is derived in (3-11), where ΔR_d is the electrode impedance mismatch and ΔA_V represents AEs' components mismatch.

$$CMRR = 20\log\left(\frac{A_V}{\Delta A_V + \frac{A_V \Delta R_d}{R_d + R_i}}\right) \tag{3-11}$$

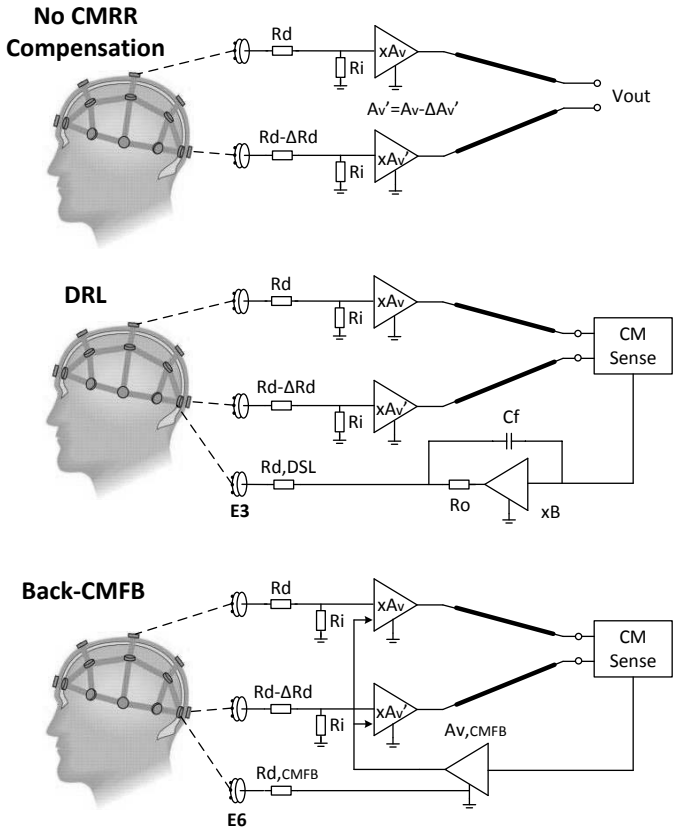

Figure 3.11 Block diagrams of the DRL and the proposed CMFB.

Compared to the well-known Driven-Right-Leg (DRL) circuit [63], which feeds back the CM signal to the subject (Figure 3.11) through recording electrodes, the proposed CMFB circuit feeds the CM signal back to the AEs' inputs. Therefore, the CMFB circuit only compensates for the AEs' components mismatch. Even if the mismatch is perfectly minimized, the maximum CMRR that the CMFB circuit can help to achieve will ultimately be limited by the electrode impedance mismatch, as shown in (3-12), whereas the maximum CMRR with a DRL circuit is theoretically infinite.

$$CMRR_{CMFB,MAX} = 20\log\left(\frac{R_d + R_i}{\Delta R_d}\right) \tag{3-12}$$

However, due to the variability of the electrode impedances $R_{d,DSL}$ (10kΩ-10MΩ) and the stray capacitance, the DRL circuit must be carefully designed to ensure that it is always stable [64], which requires a large feedback capacitor C_f (a few tens of nF) for stability compensation [65]. Dry electrodes may further exacerbate the instability since the electrode impedance is even more variable. In contrast, this is not an issue for the proposed CMFB circuit, as the electrode impedance is out of the feedback loop, and a third electrode (E_6) always biases the subject to the circuit ground.

3.5 Measurement

3.5.1 IC Measurement

The IC has been implemented in a 0.18μm standard CMOS process and occupies about 6.5mm² (Figure 3.12). Each fabricated die contains one AE and one back-end CMFB amplifier. An 8-electrode EEG readout circuit can be built up with eight chips as AEs, and a separate chip operating as back-end CMFB. The 8-electrode readout circuit consumes 160μW from 1.8V.

Figure 3.13 shows the measured AE gain as it changes from 3 to 100. Figure 3.14 shows the AE's input-referred noise with and without chopping. Chopping at 500Hz leads to an integrated noise of 0.8μV_{rms} (0.5-100Hz), which is reduced by almost half compared to 1.5μV_{rms} without chopping. Figure 3.15 shows that the input impedance is improved from 400MΩ @1Hz to 2GΩ @1Hz by utilizing the impedance boosting loop. Figure 3.16 shows the CMRR of a

pair of AEs (with a gain of 100). An 82dB CMRR has been measured at 50Hz by enabling the back-end CMFB, which improves the initial CMRR by more than 30dB. Figure 3.17 shows the output waveforms before and after applying ripple and offset trimming. The residual output ripple is less than 2mV compared to the initial 40mV, and the output offset is reduced from 280mV to 20mV.

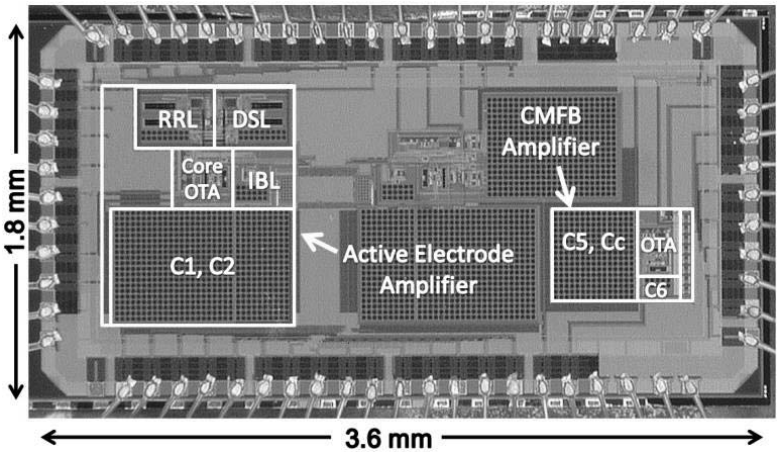

Figure 3.12 Chip photograph.

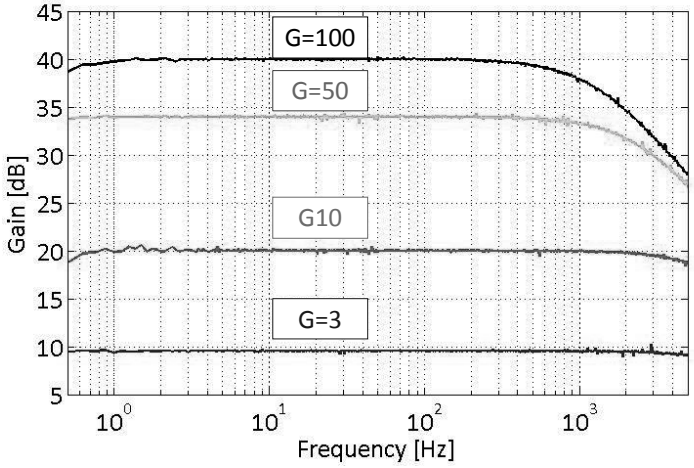

Figure 3.13 Measured gain of an AE as a function of frequency for various gain factors G.

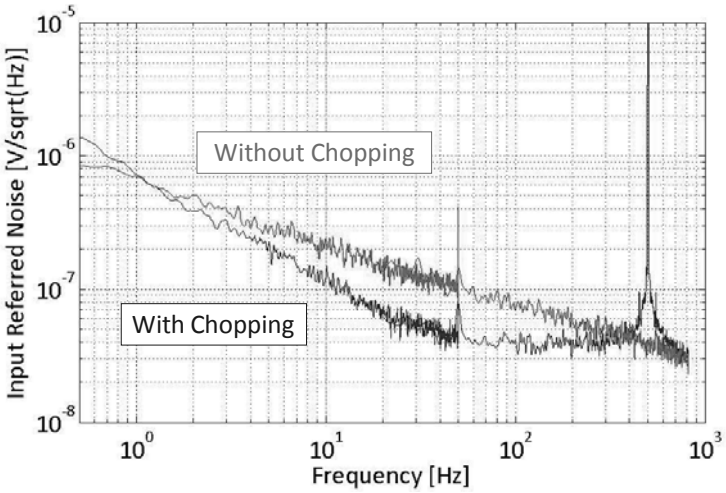

Figure 3.14 Measured input referred noise of an AE.

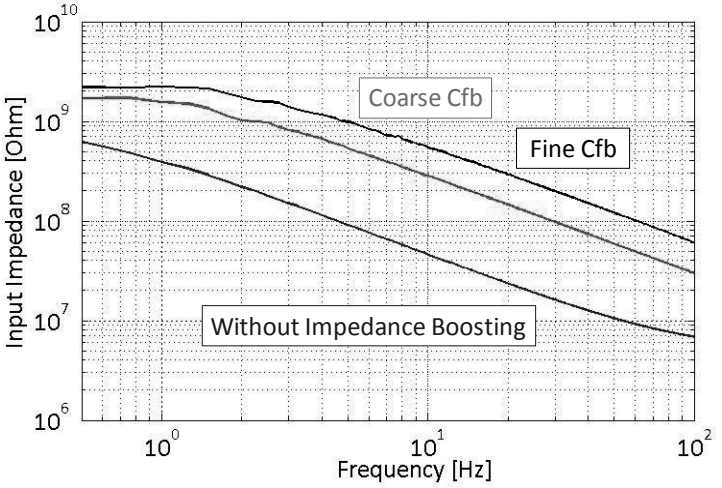

Figure 3.15 Measured input impedance of an AE.

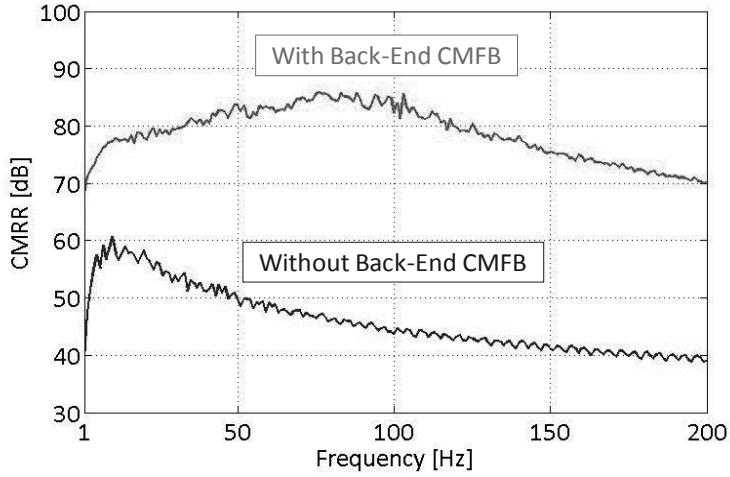

Figure 3.16 Measured CMRR between an AE pair.

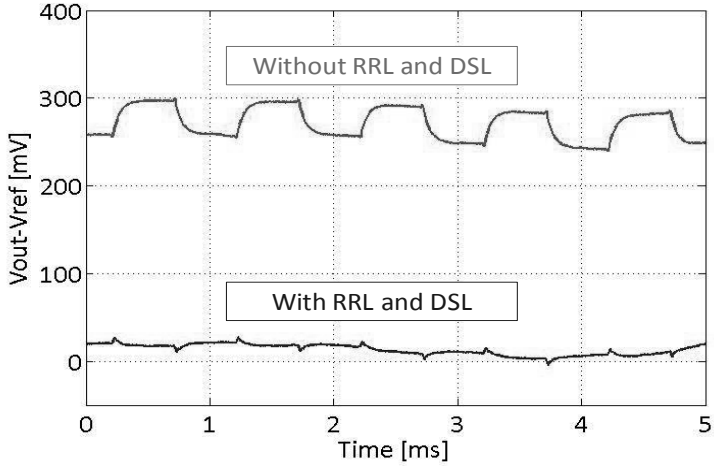

Figure 3.17 Measured output ripple and residual offset of an AE.

Table 3-1 summarizes the analog performance of the AE system, and compares it with other state-of–the-art AEs. The proposed AE system achieves the highest input impedance, comparable input referred noise, electrode offset rejection, and CMRR. The problem of achieving high CMRR between single-ended AEs is essentially solved by using a back-end CMFB circuit. All these

features make the proposed AE system suitable for dry-electrode EEG measurement.

Table 3-1: Comparison table of the proposed AE system with state-of-the-art biopotential IAs.

Parameters	[66]	[62]	[67]	[56]	This work
Supply Voltage	1.8V	3V	1V	1V	1.8V
AE Gain	100	10	190-1000	100	3-100
Input Impedance (DC)	>7.5MΩ	>100MΩ	--	>700MΩ	2GΩ
Noise per Channel	0.95μV_{rms} (0.05-100Hz)	0.6μV_{rms} (0.5-100Hz)	2.5μV_{rms} (0.05-460Hz)	1.3μV_{rms} (0.5-100Hz)	0.8μV_{rms} (0.5-100Hz)
Electrode Offset Tolerance	50mV	50mV	Rail-to-rail	Rail-to-rail	Rail-to-rail
CMRR	100dB	120dB	71dB	60dB	82dB
NEF	4.6	9.2	3.3	9.5	12.3
Power per Channel	2μW	33.3μW	337nW	3.5μW	20μW (AEs only)

3.5.2 Cable Motion and Interference

This section demonstrates the benefits of an AE system by comparing its performance with a conventional EEG readout circuit, implemented with two passive electrodes and a differential IA. The comparison includes their robustness to cable motion artifacts and interference. In Figure 3.18, two resistors of 1MΩ are placed at the IA's and the AEs' inputs to mimic the dry-electrode impedance. A low-noise (3μV_{pp} in 0.1-10Hz), high input-impedance (2GΩ) and high CMRR (>90dB) IA [68] is selected as a conventional EEG IA. The cables connected between this IA and EEG electrodes are attached to a vibration device that vibrates at 10Hz. A similar measurement setup is used for the AE system proposed in this chapter, while the IA is connected to the AEs' outputs through cables.

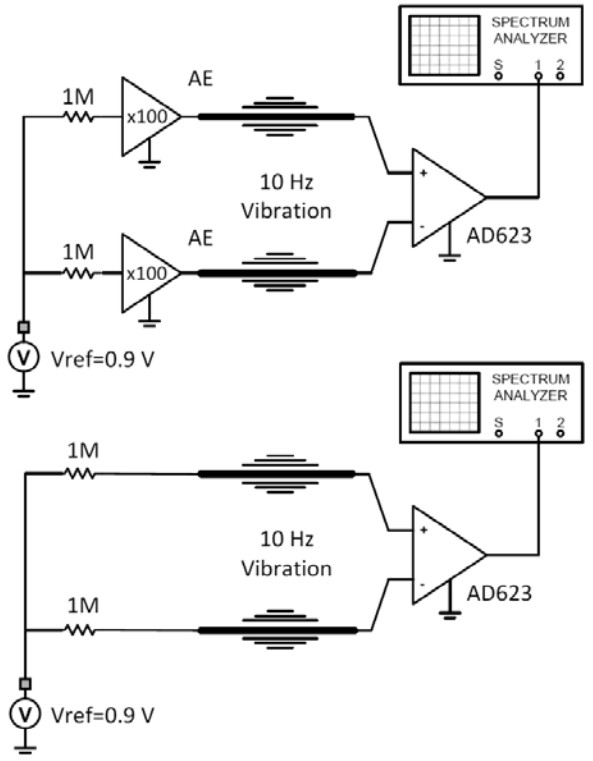

Figure 3.18 Cable motion artifacts reduction test by introducing cable vibration.

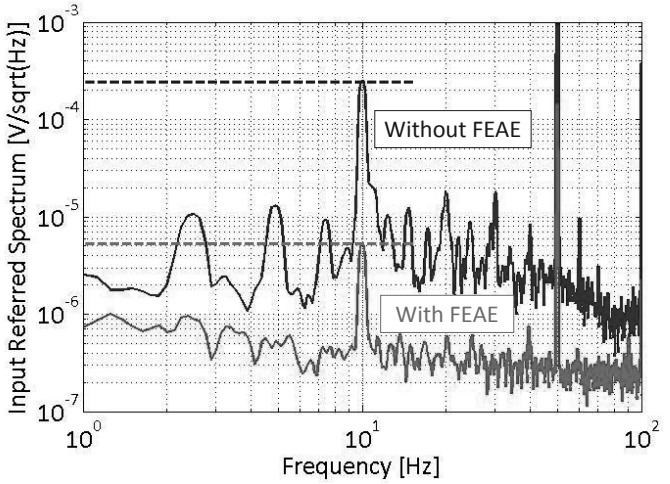

Figure 3.19 Comparison of measured cable motion artifacts.

Figure 3.19 shows the measured input referred signal PSD, and the AE readout shows a significant reduction of cable motion pickup at 10Hz due to its relatively low output impedance.

Figure 3.20 illustrates the block diagrams of two systems for interference reduction test. The cables of both systems are placed on top of a power plug which can be considered as an "interference generator". In addition, a pair of variable resistors is placed at both systems' inputs to mimic the electrode impedance. Figure 3.21 shows the measured input-referred 50Hz signal versus the electrode impedance R_S. Thanks to the AEs' low output impedance, the input-referred 50Hz signal has a low and almost constant magnitude. In the conventional EEG readout circuit, the input-referred 50Hz signal linearly increases with the electrode impedance (till 1MΩ). Particularly, the benefits of AEs are more valued for dry electrodes, where R_S is more than 10kΩ [69].

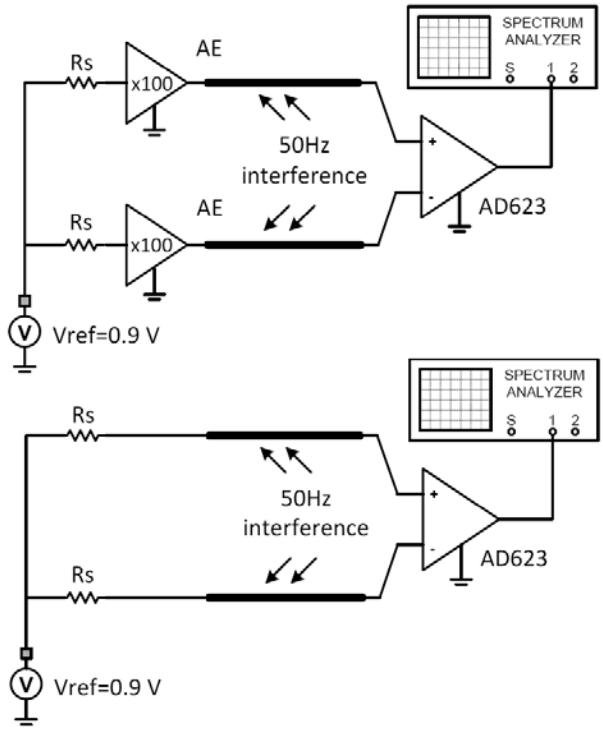

Figure 3.20 Interference reduction test by introducing a 50Hz interference source.

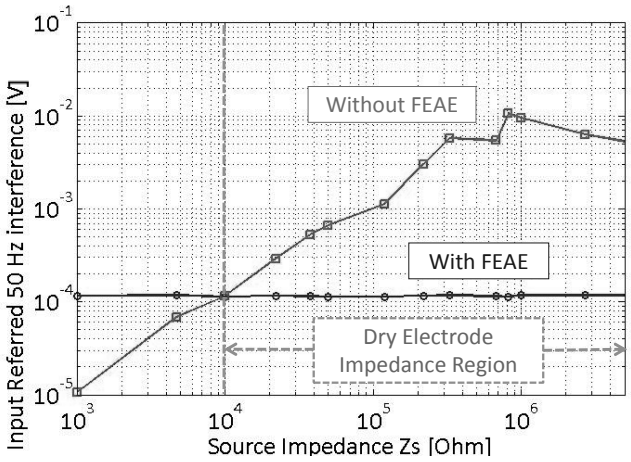

Figure 3.21 Comparison of measured interference at 50Hz.

3.5.3 Biopotential EEG Measurement

Figure 3.22 shows the scalp EEG measurement setup. For simplicity, EEG signals are measured between two pairs of electrodes, which are both placed in positions of O_1 and C_z. A first pair is connected to two AEs (G=100) via short wires. The outputs of these AEs are connected to a commercial EEG system (channel 1) [70]. For comparison, another pair of electrodes is placed very close to the first pair. The outputs of these electrodes are directly connected to the same EEG system (channel 2). In this way, the EEG measurement results can be compared simultaneously between the two types of systems.

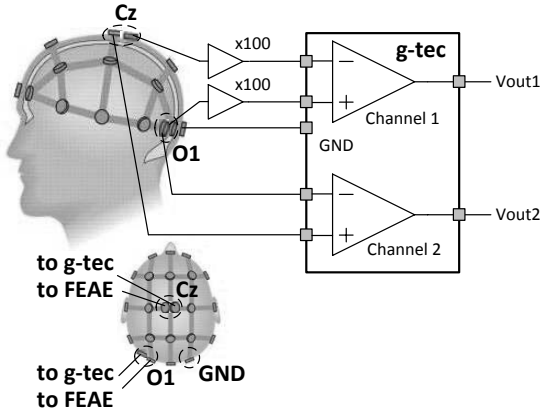

Figure 3.22 Scalp EEG measurement setup.

In the first measurement, both systems use wet electrodes. Figure 3.23 shows the spectrogram of the measured EEG signal. Alpha waves around 10 Hz are clearly visible when eyes are closed. In Figure 3.24, the spectrum correlation coefficient (ϱ) between the (wet-electrode) AE readout and the (wet-electrode) conventional EEG readout is higher than 0.99.

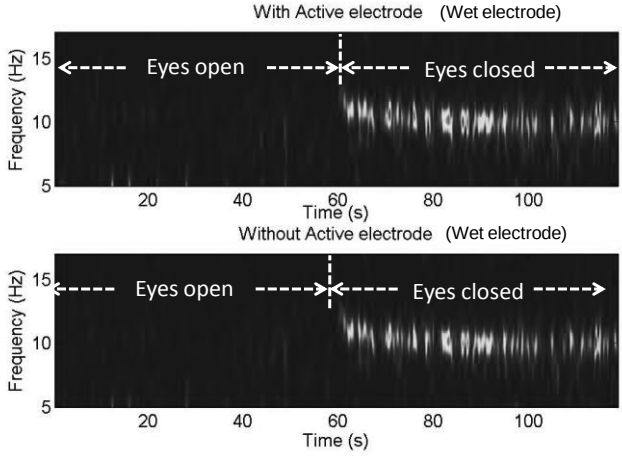

Figure 3.23 EEG spectrogram with AE (upper trace, wet electrodes) and without AE (bottom trace, wet electrodes).

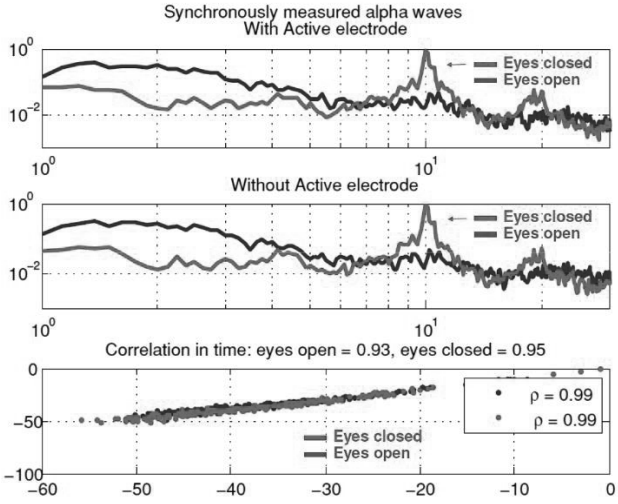

Figure 3.24 EEG normalized spectrum with and without AE (both with wet electrodes). Eyes open (blue curve) and eyes closed (red curve).

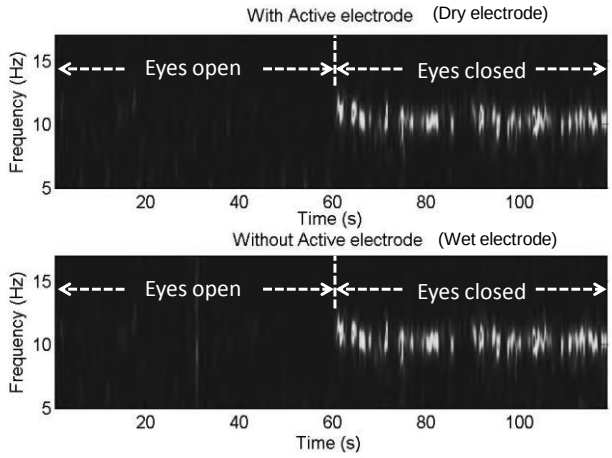

Figure 3.25 EEG spectrogram with AE (upper trace, dry-electrode headset) and without AE (bottom trace, wet electrode).

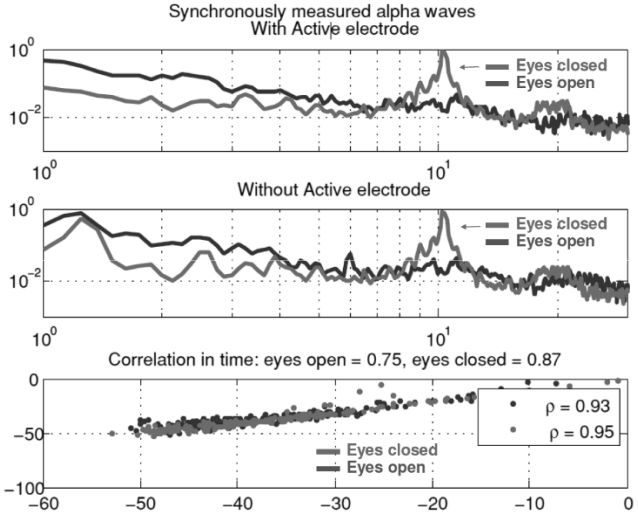

Figure 3.26 EEG normalized spectrum with AE (dry-electrode headset) and without AE (wet electrode). Eyes open (blue curve) and eyes closed (red curve).

In the second measurement, wet-electrode AEs are replaced with dry-electrode AEs [71], while the commercial EEG readout channel still uses wet electrodes. Figure 3.25 shows the EEG spectrogram. For both systems, alpha waves around 10Hz are still clearly visible when eyes are closed. In addition,

Figure 3.26 shows that the spectrum correlation coefficient (ϱ), between the dry-electrode AE readout and the wet-electrode commercial EEG readout, is higher than 0.93. This number is high in comparison to other works on dry-electrode sensing, such as [72]: $\varrho > 0.9$, [73]: $\varrho = 0.8 – 0.96$, and [74]: $\varrho = 0.83$.

3.6 Conclusions

A wearable EEG system requires both user-friendly dry electrodes and low-power high-performance readout circuits. However, state-of-the-art IAs, implemented with differential amplifiers, are not well suited for such applications.

This chapter presented a low-power AE based readout circuit suitable for dry-electrode EEG measurement. The readout circuit includes eight IAs as AEs and one back-end CMFB amplifier for CMRR improvement. The AE utilizes AC-coupled chopper IA architecture, equipped with input-impedance boosting and offset trimming, for optimized performance between noise, offset tolerance, input impedance, and large output swing.

The AE-based readout circuit shows significant benefits in terms of the robustness to cable motion and interference than a traditional EEG readout circuit. The proposed AE system can detect alpha waves when either wet or dry electrodes are used on the scalp. Moreover, this AE system also shows a highly correlated result compared to an existing commercial EEG system.

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CHAPTER 4

AN 8-CHANNEL ACTIVE ELECTRODE SYSTEM[3]

4.1 Introduction

The previous chapter (Chapter 3) presented an active electrode (AE) based readout circuit for dry-electrode EEG acquisition. However, this system only has analog outputs, while a back-end CMFB circuit was used for CMRR enhancement without facilitating analog-to-digital conversion. This makes the system difficult to interface with digital processors for advanced digital signal processing and feature extraction. In addition, foreground offset and ripple calibrations were used to improve the AE's precision, but at the cost of interrupting EEG measurement.

To fulfill the needs of digitization and continuous EEG recording, this chapter presents a complete 8-channel AE system, including an ADC, a standard digital interface and a background calibration scheme. Furthermore, the system can also measure electrode-tissue impedance (ETI), i.e., the complex impedance between an electrode and skin. Therefore, an in-phase and quadrature signal processing scheme is necessary to measure the ETI's resistive and capacitive components, respectively. ETI measurement extends an AE system's functionality by enabling the remote assessment of electrode status and recording ETI-related motion artifacts. The whole AE system consists of nine AEs and one back-end (BE) analog signal processor (ASP). The AEs, based on a non-inverting chopper IA architecture, amplify the low-level EEG signals with a good tradeoff between input impedance and noise. The BE ASP post-processes and digitizes the AEs' analog outputs, such that the system can be connected to a microcontroller through a serial-to-parallel interface (SPI). At the system level,

[3] This chapter is derived from a journal publication of the authors: J. Xu, S. Mitra, et al., "A 700μW 8-Channel Active Electrode EEG/Contact-impedance Acquisition System," *IEEE J. Solid-State Circuit,* vol.49, no.9 pp 2005-2016, Sept. 2014.

an innovative common-mode feed-forward (CMFF) technique improves the CMRR of differential measurements, made with a pair of AEs, by 25dB.

4.2 IC Architecture Overview

Figure 4.1 shows the block diagram of the proposed 8-channel EEG/ETI acquisition system. An EEG measurement is obtained as the differential output of two AEs, and so the system consists of 9 AEs. A bias electrode provides a DC bias (at ½ V_{dd}) for all the AEs. Each AE connects to the BE via six wires: 32 kHz clock (CLK), power supply (VDD and VSS), digital control bits (PWM), analog output of EEG/ETI (ANA) and common-mode feed-forward (CMFF). The AE utilizes a non-inverting chopper IA for pre-amplification and a built-in square-wave current source for ETI measurement [75].

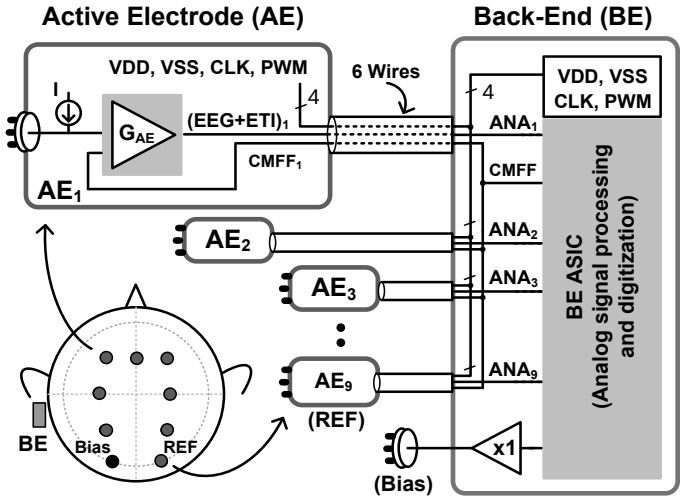


Figure 4.1 Block diagram of an 8-channel AE based EEG/ETI system.

The BE is responsible for analog signal processing and digitization. In Figure 4.2, the BE signal chain starts with two chopper IAs, each consisting of a transconductance (TC) stage and a transimpedance (TI) stage. The two TI stages in an ETI channel are used to demodulate and separate the EEG signal from the ETI signals, and each ETI channel consists of an in-phase (I) channel and a quadrature (Q) channel. Programmable gain amplifiers (PGA) provide variable gain, and low-pass filters (LPF) enable anti-aliasing. Both EEG and ETI channels are simultaneously sampled at 500Hz by respective sample-and-hold (S/H)

stages. The result is a total of 24 channels, including 8-channel EEG, 8-channel ETI-I and 8-channel ETI-Q, whose outputs are multiplexed and digitized by two 12-bit SAR ADCs operating at 1kSps.

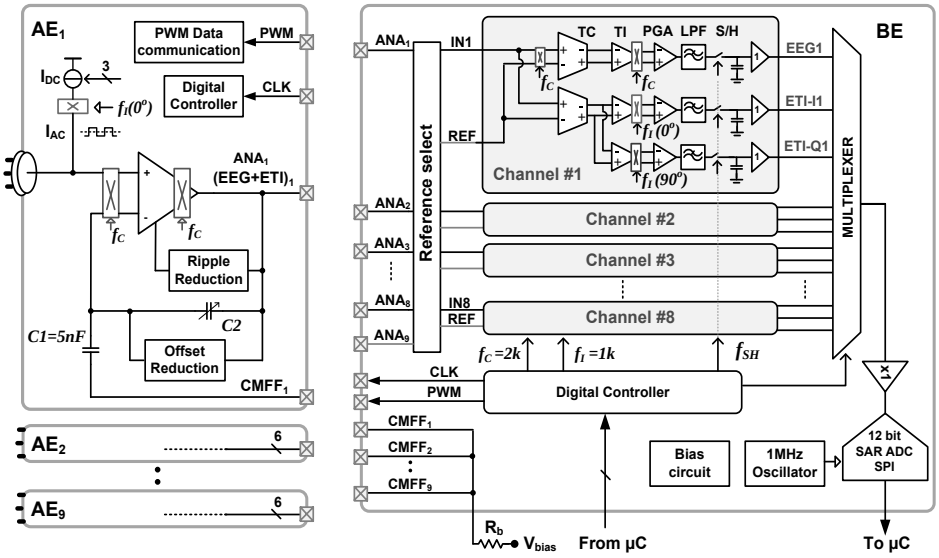


Figure 4.2 Architecture of the 8-channel EEG/ETI acquisition system (TC and TI represent transconductance and transimpedance IAs, respectively).

4.2.1 EEG and ETI measurement

The proposed 8-channel system can simultaneously measure EEG and ETI signals (Figure 4.3). A DC current (I_{DC}) is up-modulated to the ETI measurement frequency (f_I=1kHz) and injected into the subject through each recording electrode. This current is then converted into a square wave voltage (ETI_{in}) over the electrode impedance. As a result, the EEG and ETI signals are both present at the input of an AE, but are located at different frequencies. At the output of an EEG channel, the amplified EEG signal is still at baseband, and the residual ETI signal at f_I can easily be removed by a LPF. The ETI-I/Q channels up-modulates the EEG signal to f_I and filters it out, while they demodulate in-phase f_I (0^o) and quadrature f_I (90^o) components of the ETI signal back to DC, respectively. Typically, the ETI-I is much larger than the ETI-Q at the ETI measurement frequency (at a few kHz). For instance, 51kΩ//47nF, the standard (wet) electrode impedance, has 51kΩ and 3.3kΩ at 1kHz, respectively.

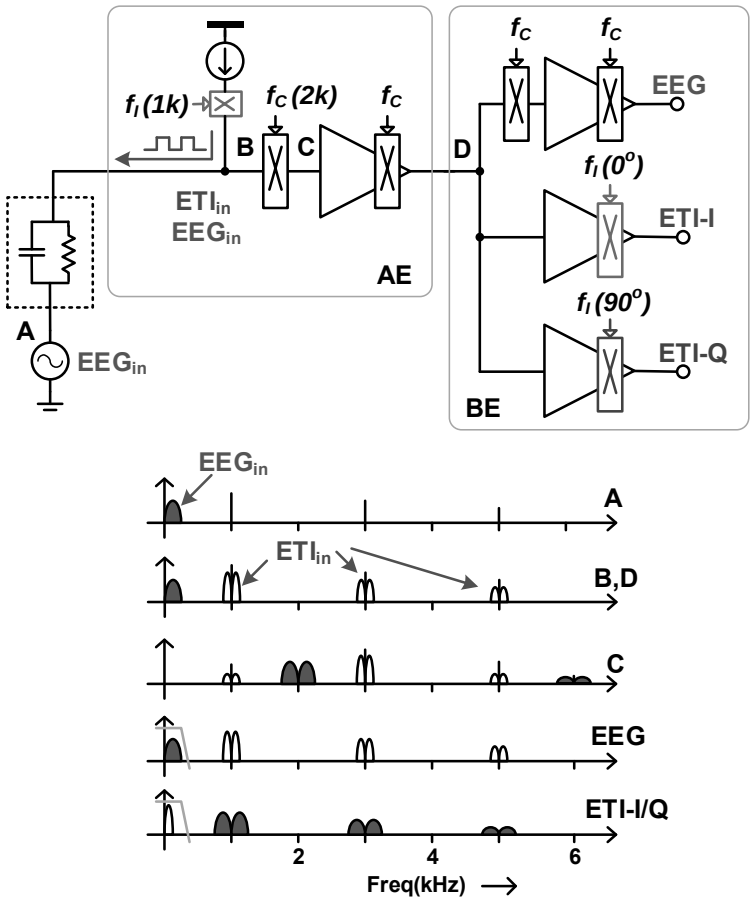


Figure 4.3 Block diagram and spectrum to illustrate the principle of EEG/ETI measurement.

4.2.2 A CMFF technique for CMRR enhancement

Gain mismatch between AEs typically limits their intrinsic CMRR to less than 60dB. A driven-right-leg (DRL) circuit can improve CMRR at the cost of potential instability [76]. The back-end CMFB proposed in the previous chapter can solve this issue by feeding the CM signal back to the AEs' reference inputs, instead of the subject. However, the CMFB requires a summing amplifier for CM extraction and uses large capacitors for stability, leading to increased chip area and power. Alternatively, a digitally-assisted DRL technique [77] improves its

stability, where digital notch filtering ensures that high loop gain is only available at the major interference frequency (at 50/60Hz). However, this improvement is at the expense of complex digital signal processing and more power.

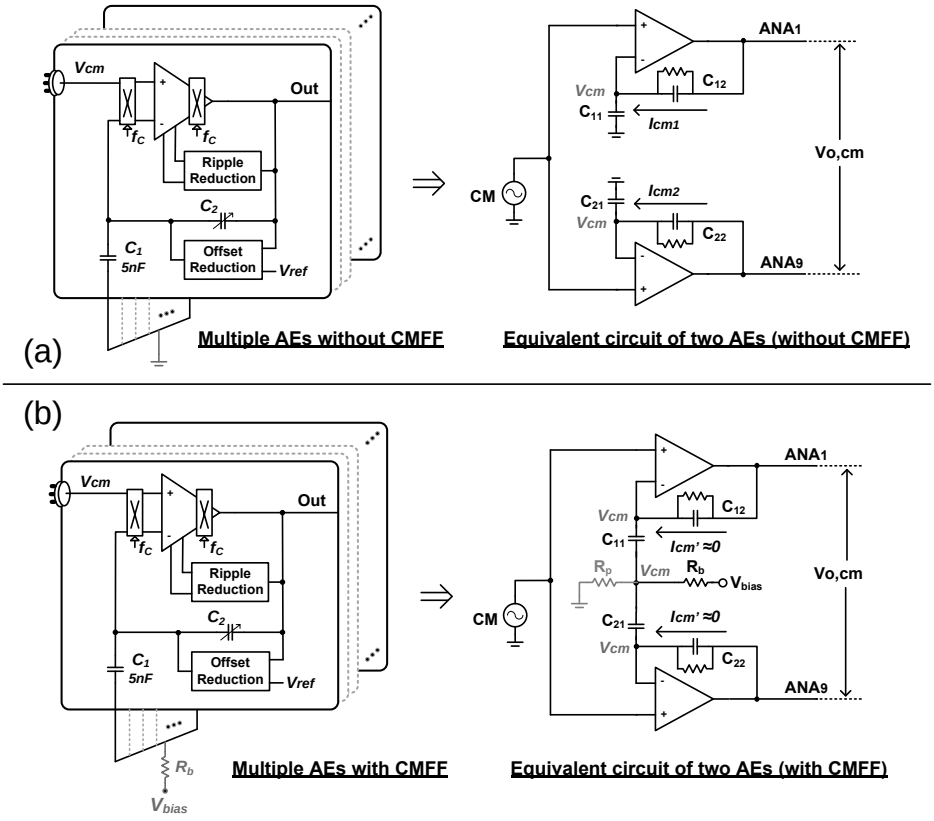


Figure 4.4 (a) Conventional AEs without CMFF, and equivalent circuit diagram of two AEs, and (b) AEs with CMFF for CMRR enhancement, and equivalent circuit of two AEs.

This section introduces a CMFF technique for CMRR improvement of multiple AEs [78]. Conventionally, the non-inverting AEs are referred to the system ground (Figure 4.4 a). As a consequence, the CMRR of a pair of AEs is limited by their voltage gain error, as shown in (4-1), where G_{AE} is the voltage gain of an AE, and ΔG_{AE} is the gain difference of two AEs. Although the matching of AEs can be improved by implementing both C_1 and C_2 with a common-

centroid layout with dummies, the maximum CMRR will still be typically less than 60dB. This issue can be solved by a CMFF technique, where the AEs' reference node (now dubbed the CMFF node), which was previously connected to the circuit ground, is capacitively connected together to a well-defined DC reference voltage (V_{bias}) through a very large bias resistor R_b (Figure 4.4 b). As a result, the CMFF node becomes an averaging node for all the input signals, and as a result, its voltage is equal to the CM input. Furthermore, no CM current will flow through capacitors C_{11} and C_{21}. This effectively reduces the CM gain and thus increases the CMRR of an AE pair, as shown in (4-2), where CMRR is the initial CMRR of two AEs without using CMFF, C_1 is the input capacitor (C_{11} or C_{21}) and R_b is the bias resistor.

$$CMRR = 20\log\left(\frac{G_{AE}}{\Delta G_{AE}}\right) \tag{4-1}$$

$$CMRR^{'} = CMRR + 20\log\left(1 + sC_1R_b\right) \tag{4-2}$$

However, increasing R_b will make the DC voltage at the CMFF node sensitive to leakage due to the voltage divider formed by R_b and the parasitic resistance R_p (Figure 4.4 b). Furthermore, it will significantly reduce the amplitude of the DC voltage at CMFF node, thus limiting the maximum CM swing that the CMFF can handle. As a reasonable requirement, the actual DC voltage at the CMFF node should be larger than the AE's maximum input CM voltage ($V_{in,pk}$), as given by

$$V_{DC,CMFF} = V_{bias} \cdot \frac{R_p}{R_p + R_b} > \left|V_{in,pk}\right| \tag{4-3}$$

Equation (4-3) sets an upper limitation of R_b. On the other hand, decreasing R_b will limit the maximum CMRR that the CMFF can achieve, as shown in (4-2). A small R_b increases the high-pass frequency at the CMFF node and thus prevents any CM voltage extraction. For instance, when R_b=0, the CMFF will be biased to ground and the CMFF will stop working. In this design, V_{bias}=1.8V and R_b=100MΩ are selected to accommodate a CM input range of 50mV while maintain a good CMRR (>80dB).

One remaining limitation of the CMFF is its robustness to the "leads off" condition. Disconnecting any electrode will cause the failure of the CMFF loop, because a floating input of any AE pollutes the CM averaging [78]. This problem can be solved by connecting the positive input of each AE to a well-defined bias voltage (at V_{dd}/2) via a large resistor. As a result, the AE in the lead-off condition will be biased, while CMFF is then performed among the other AEs.

4.2.3 PWM communication

In an AE based system, each AE receives the configuration register bits from the BE to define its operation modes, such as the AE's gain and bandwidth, and the amplitude and frequency of the ETI current source. Data communication between the BE and the AEs could be done via a 3-wire SPI interface. However, this would lead to an increased number of wires in a multi-channel system, increasing the system's complexity and weight. In this design, the BE-to-AE interface utilizes a single-wire self-clocked PWM data transmission [79], which combines the clock and data signals to reduce the number of connecting wires.

4.3 Active Electrode ASIC

4.3.1 Instrumentation Amplifier (IA)

As the analog front-end of the EEG system, an AE should provide high input-impedance and low noise, as well as the capability to reject large electrode offsets. To meet these requirements, the AE (Figure 4.5) consists of a non-inverting chopper IA equipped with a DC servo loop (DSL) and a ripple reduction loop (RRL), respectively. These requirements are discussed in the following sections in detail.

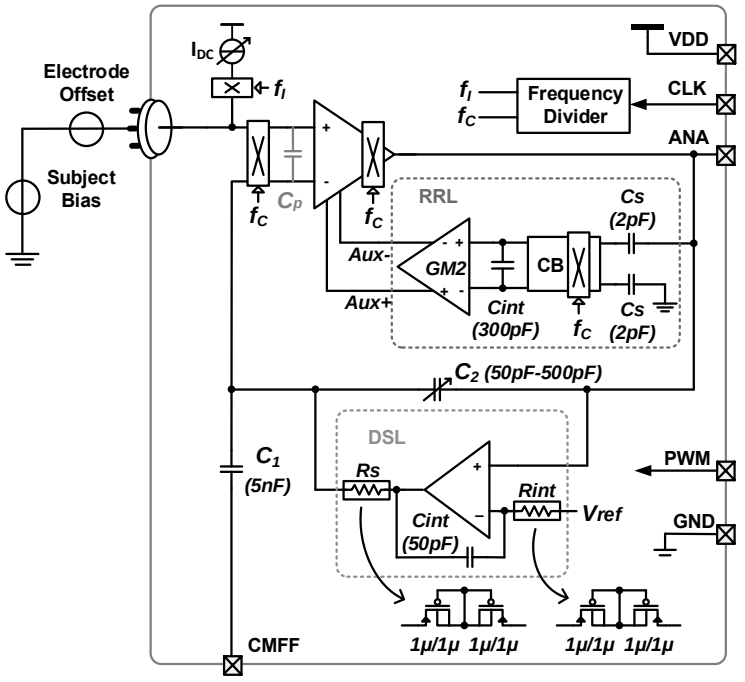


Figure 4.5 Block diagram of the IA used as an AE.

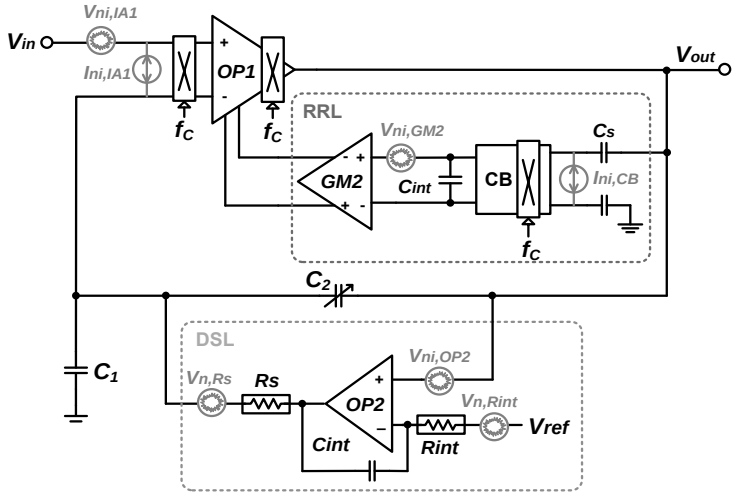


Figure 4.6 Equivalent noise model of the AE.

Input Impedance: A non-inverting IA has much higher input impedance than that of an inverting IA [80] because the input impedance of the former architecture is determined by input parasitic capacitance, instead of the large coupling capacitor (C_1). In this design (Figure 4.5), the core amplifier itself has an input impedance of 2GΩ at 20Hz, while the output resistance ($R_{out,IDC}$) of the ETI current source is 3.2GΩ at 20Hz. This gives the AE an equivalent input impedance of more than 1.2GΩ at 20Hz.

$$Z_{in} = \left(\frac{1}{2 f_c C_p} + \frac{1}{sC_1} \right) // R_{out,IS} \tag{4-4}$$

Electrode Offset Rejection: To reject a large electrode offset (EO), which may otherwise saturate the AE, the built-in IA implements a continuous-time DC-servo loop (DSL). The DSL stabilizes the output DC voltage to a reference voltage (V_{ref}) via an active RC integrator, which feeds the IA's output offset back to its inverting input via a large pseudo resistor (R_s). The maximum electrode offset rejection of each AE, i.e., ±250mV with respect to subject bias, is ultimately determined by the input biasing range of the core amplifier.

Ripple Reduction: The intrinsic offset of the core amplifier will be up-modulated by the output chopper modulator. This generates a square wave, namely ripple, thus reducing the IA's output headroom. A ripple reduction loop (RRL) (Figure 4.5) [81] first converts the output ripple into a DC current via a capacitor (C_s) and a chopped current buffer (CB). This DC current is then integrated on a capacitor (C_{int}), and the resulting voltage is converted into a DC feedback current via a transconductance stage (GM2). The DC feedback current compensates the IA's intrinsic offset and reduces the output ripple approximately by a factor of 10.

4.3.2 Noise Analysis

In this work, the target input-referred noise of an EEG channel (including two AEs and one BE) is 75nV/sqrt(Hz). Neglecting the noise contribution from the BE, the input-referred noise of a single AE should be about 53nV/sqrt(Hz), which comes from three major contributors (Figure 4.6): the core amplifier, the ripple reduction loop (RRL), and the DC-servo loop (DSL).

$$\overline{V_{in,AE}^2} = \overline{V_{in,IA}^2} + \overline{V_{in,RRL}^2} + \overline{V_{in,DSL}^2} \tag{4-5}$$

The noise contribution of the core IA can be expressed by

$$\overline{V_{in,IA}^2} = \overline{V_{in,OP1}^2} \cdot \left[1 + \frac{C_2}{C_1} + \left(\frac{f_c}{f_{in}} + 1 \right) \cdot \frac{C_p}{C_1} \right]^2 + \overline{I_{in,OP1}^2} \cdot \left(\frac{1}{2\pi f_{in} C_2} \right)^2 \tag{4-6}$$

where $V_{ni,OP1}$ and $I_{ni,OP1}$ are the input-referred voltage noise and current noise of the core amplifier, respectively, C_1 and C_2 are the feedback capacitors which define the AE's gain, f_c is the operating frequency of the chopper modulators, f_{in} is the frequency of the input signal, and C_P is the input parasitic capacitance.

The first component in (4-6) refers to the $1/f^2$ voltage noise of the non-inverting chopper IA because of its parasitic switched-capacitor resistance. Although chopper modulation mitigates $1/f$ noise of the core amplifier (OP1), this parasitic resistance reduces the input impedance of the amplifier and thus increases its current noise. The current noise is converted into $1/f^2$ voltage noise in the presence of external capacitive feedback. The second component in (4-6) refers to another $1/f^2$ voltage noise source associated with the current noise $I_{ni,OP1}$, which is due to the charge injection and clock feed-through of the input chopper [82]. The current noise PSD linearly increases with the chopping frequency [83] and induces significant $1/f^2$ voltage noise, especially when chopping is performed at a high-impedance node. This problem will be discussed in more detail in Chapter 5.

The proposed IA utilizes several methods to minimize the total noise in (4-6). Firstly, to reduce the thermal noise of $V_{ni,OP1}$, the core amplifier employs a two-stage amplifier (Figure 4.7), whose input pair consists of NMOS and PMOS differential pairs connected in parallel [84]. This method doubles the input transconductance of the core amplifier without consuming extra bias current, while still achieving a good input CM range from 0.7V to 1.2V. Secondly, in order to reduce $I_{ni,OP1}$, the input chopper modulator utilizes a low chopping frequency (f_c=2kHz) and minimum size transistors [82]. Thirdly, the use of a

non-inverting topology means its input impedance is not dominated by the feedback capacitors. As a result, very large capacitors C_1 (5nF) and C_2 (50pF to 500pF) are used to reduce the impedance of the chopping node, as shown in (4-6). This topology reduces the $1/f^2$ voltage noise without compromising IA's input impedance. This is a clear advantage of a non-inverting chopper AE, as the inverting IA (Chapter 3) suffers from the tradeoff between noise and input impedance [80][85].

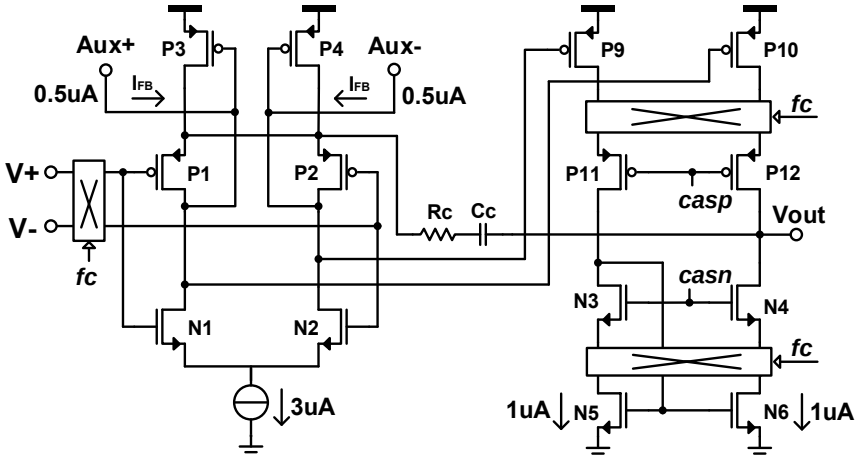


Figure 4.7 Schematic of the core amplifier of an AE.

The RRL's noise contribution is negligible since it is located between the two choppers of the core amplifier (OP1). The $1/f$ noise from G_{M2} and current buffer (CB) are effectively chopped out, while their thermal noise is suppressed by the input stage of OP1. The DSL does not induce significant noise in the EEG bandwidth either, as its low-pass cutoff frequency is well below 0.5Hz.

4.3.3 Current Source for ETI Measurement

The current source employs a self-biased triple-cascode architecture to boost its output impedance (>3.2GΩ@20Hz) (Figure 4.8). The magnitude of the reference current (I_{dc}) is configurable from 10nA to 2μA to cover a wide range of electrode impedances. This reference current is mirrored either to a NMOS or PMOS triple-cascode stage, enabling current injection or current sink. An output chopper then generates a square-wave current at the ETI measurement frequency (f_I =1kHz).

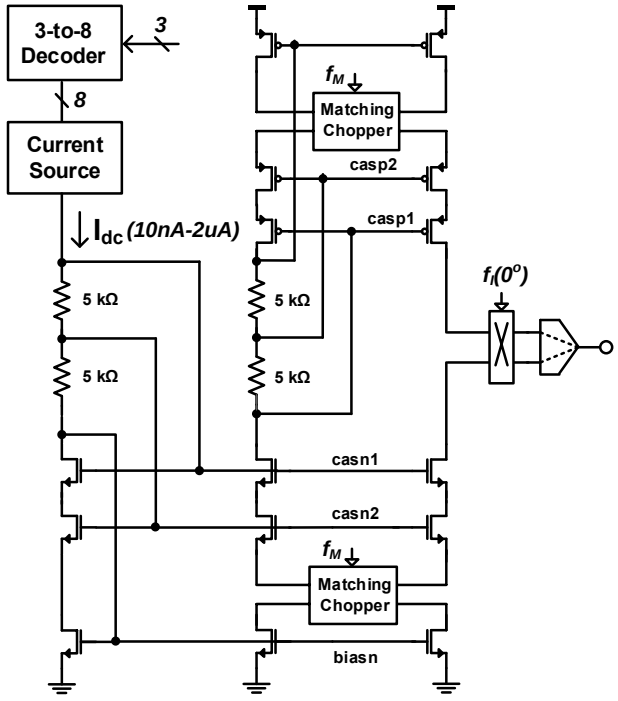


Figure 4.8 Triple-cascode, self-biased, square-wave current source.

4.4 Back-End Analog Signal Processing ASIC

4.4.1 Instrumentation Amplifiers (IA)

In the BE, one EEG channel and two ETI channels use the same IA architecture, but with different chopping schemes to separate EEG and ETI from each other. The IA of the EEG channel (Figure 4.2) utilizes both input and output choppers to reduce its 1/*f* noise, while two ETI channels share the same TC stage of the EEG channel for low power and use only output choppers in their TI stages to demodulate the ETI signal.

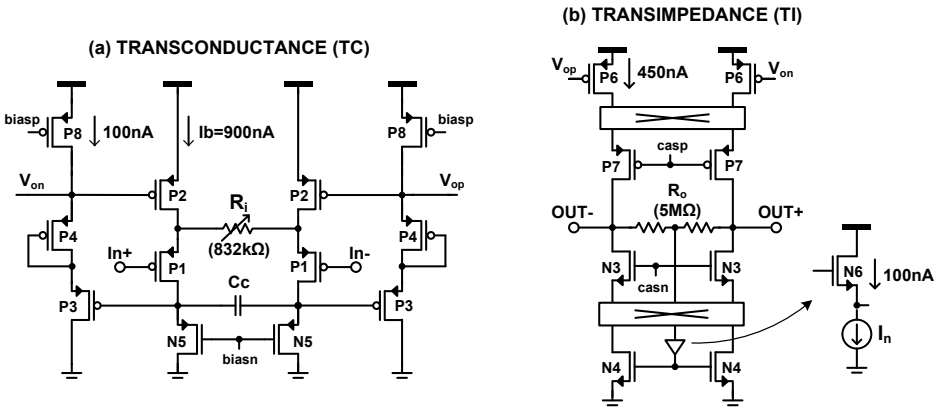


Figure 4.9 Schematic of TC and TI stages of IA in the BE.

The IA is based on a current-feedback instrumentation amplifier (CFIA) (Figure 4.9) [86]. The TC stage utilizes input voltage followers for high input impedance. The differential input voltage applies across the input resistor R_i and creates a signal dependent current. This current is mirrored (via P_8 and P_6) to the TI stage and converted back to a voltage through a resistor R_o. The voltage gain of the IA is given by

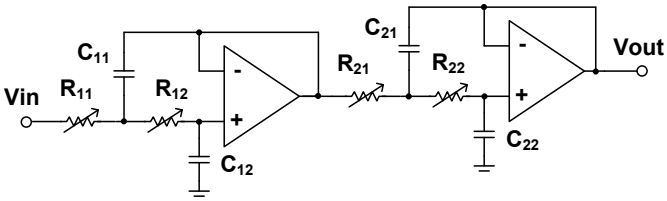
$$G_{IA} = \frac{R_0}{R_i}\left(\frac{W_6/L_6}{W_2/L_2}\right) \tag{4-7}$$

The level shifters (P_3 and P_4) help to keep the voltages V_{on} and V_{op} at reasonable values for a wide range of input common-mode voltages. In this architecture, the maximum input swing of the IA is determined by R_iI_b.

4.4.2 Low-Pass Filter and ADC

The anti-aliasing LPFs separate the EEG signal and the ETI signal (at 1kHz), and reject chopping spikes. The LPF is a 4th-order unity-gain Bessel filter realized with a Sallen-Key architecture (Figure 4.10) [87], which provides tunable bandwidth (100Hz to 300Hz), as well as sufficient attenuation (>60dB at 1kHz) of residual ETI signal. In addition, the use of a Bessel filter ensures that the EEG and ETI channels all have a constant group delay of about 1ms. The sample-and-hold circuits thus sample all channels at more or less the same time.

Both constant group delay and synchronized sampling improve the accuracy of temporal correlation across channels. This is important for brain-computer-interface (BCI) applications, where the ETI output can be used for impedance-related motion artifact reduction [88].



R_{11} , R_{12}	8.8 MΩ
R_{21} , R_{22}	4.8 MΩ
C_{11}	58.5 pF
C_{22}	53.7 pF
C_{21}	139.3 pF
C_{22}	53.7 pF

Figure 4.10 Schematic of the 4th-order Sallen-Key low-pass filter (LPF).

Two time-multiplexed 12-bit SAR ADCs, conceptually similar to the ones used in [89], digitize all 24 analog outputs (EEG, ETI-I and ETI-Q from 8 channels), at 1kSps per channel.

4.5 Measurement

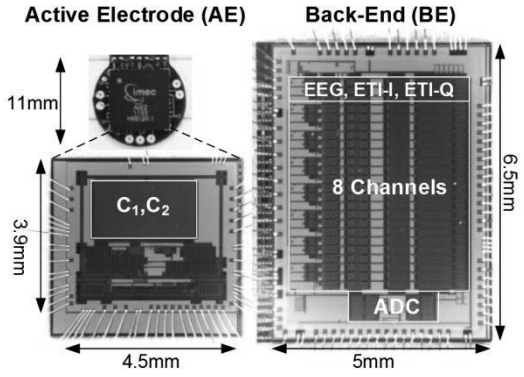


Figure 4.11 Chip photographs: (left) the AE, (right) the BE.

The 8-channel AE system, including the AEs and the BE, is implemented in a 0.18μm standard CMOS process. Figure 4.11 shows the photographs of both chips and the packaged AE placed on an 11mm diameter electrode. The 8-channel system consumes less than 700μW from 1.8V. Table 4-1 shows the system power breakdown.

Table 4-1: Power breakdown of the 8-channel AE system.

Active Electrode (AE)	11.1μA×9=100μA
Core Pre-amplifier	5μA
DSL	1.5μA
RRL	0.7μA
Bias	1.9μA
Current Source	2μA
Back-End (BE) Readout	265μA
Bias	10μA
8-channel EEG	56μA
16-channel ETI	83.2μA
ADC+SPI	115.2μA
Total Power of the System	365μA@1.8V=657μW

Figure 4.12 shows the measured original PWM data sent from the BE and the demodulated serial data received by the AE, which demonstrates a proper recovery of the register bits.

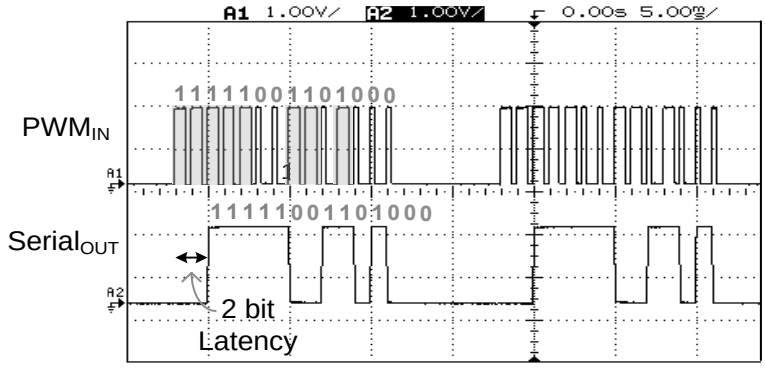


Figure 4.12 Measured PWM input data (PWM_{IN}) and demodulated output ($Serial_{OUT}$).

Figure 4.15 shows the measured voltage gain of one EEG channel at various PGA gain settings (3, 9, 12 and 18). The measured bandwidth of 200Hz is determined by the LPF.

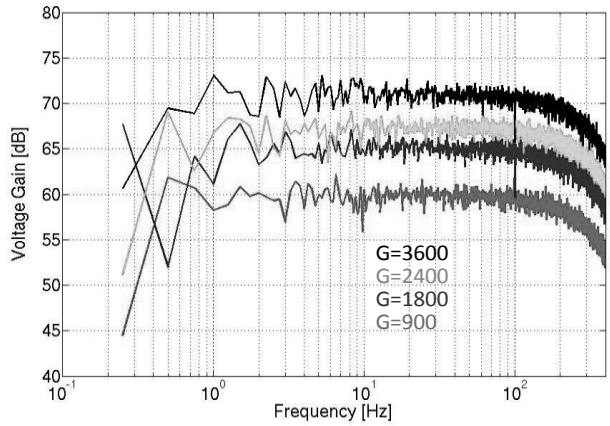


Figure 4.13 Measured EEG channel gain as a function of frequency for various gain factors G (G=900, 1800, 2400, 3600).

Figure 4.14 shows the measured input impedance of an AE, which is 1.2GΩ at 20Hz and above 300MΩ at 50Hz.

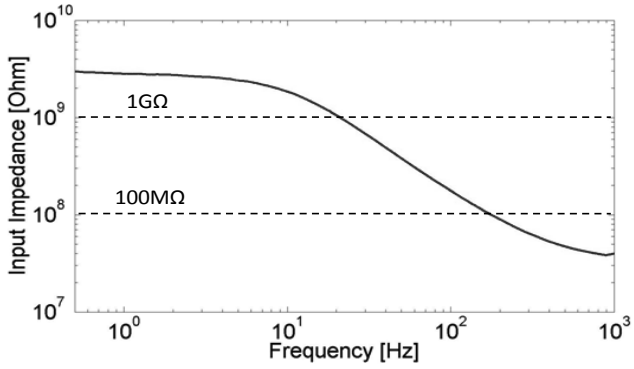


Figure 4.14 Measured input-impedance of an AE as a function of frequency.

Figure 4.15 shows the input-referred noise of one EEG channel (including two AEs and one BE) versus frequency. When chopping is disabled, $1/f$ noise is clearly visible; when chopping is enabled at 2kHz, $1/f^2$ noise dominates

till 20Hz. Above 20Hz, the input noise density is constant at 75nV/sqrt(Hz). The integrated noise is 1.75μV_{rms} from 0.5Hz to 100Hz.

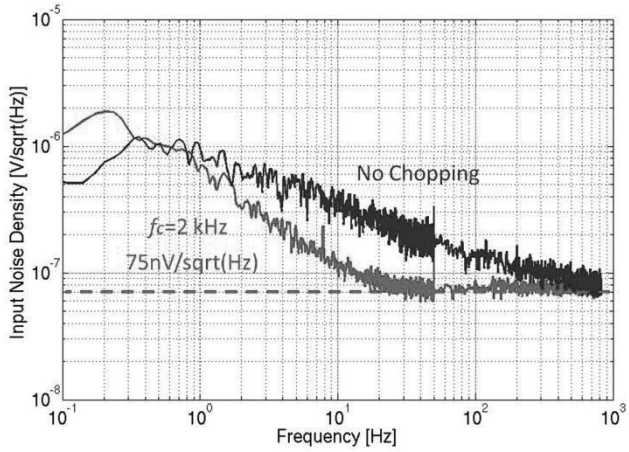


Figure 4.15 Measured input referred noise density per channel (two AEs and one BE).

Figure 4.16 shows the measured CMRR of one EEG channel (including two AEs and one BE). In this measurement, the input common-mode signal is made of a 100mV_{pp} chirp from 1Hz to 200Hz, and it was applied to both AEs directly without any electrode impedance. At 50Hz, enabling the CMFF improves the CMRR by 25dB (from 60dB to 85dB). Figure 4.17 shows that the measured CMRR between several pairs of AEs is always above 84dB.

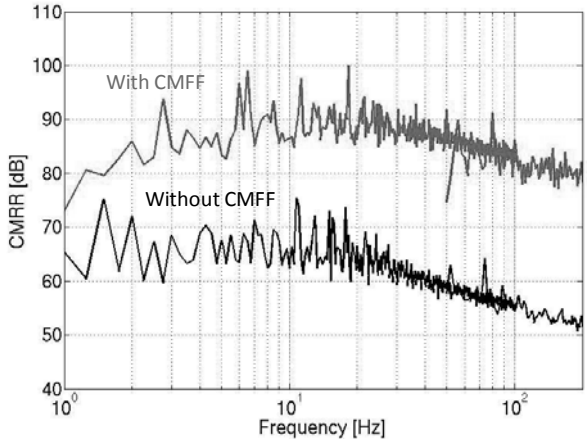


Figure 4.16 Measured CMRR (with and without CMFF).

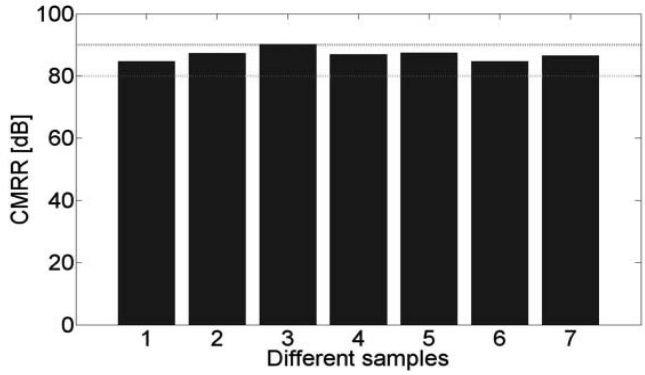


Figure 4.17 Measured CMRR @50Hz from different samples.

Figure 4.18 shows the AE's output voltage as a function of time. When a large transient electrode offset of 200mV is applied to the input of AE, its output first saturates and then recovers to the reference voltage in about 20 seconds.

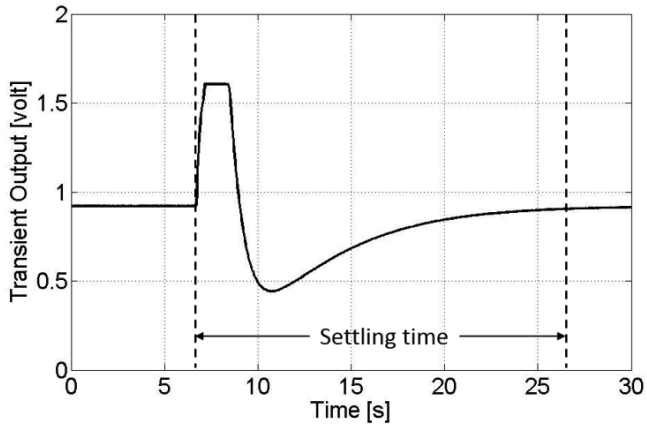


Figure 4.18 Measured Settling time of the DC servo loop (DSL).

Figure 4.19 and Figure 4.20 show the measured ETI resistance and capacitance versus their actual values, respectively. In these measurements, either a test resistor (110Ω to 280kΩ) or a test capacitor (100pF to 1μF) was connected to the input of one AE, while the other AE was connected to the subject bias voltage of $V_{dd}/2$ directly. The gain of the AE and BE were set to 101 and 9, so that both the EEG and ETI channels have the same gain (≈900). In this de-

fault setting, the maximum differential ETI signal that the system can linearly measure is approximately 60kΩ or 2nF (at f_I=1kHz). This is limited by the output swing of the PGA in the BE (0.35V-1.45V), and the amplitude of the injected current (10nA). By lowering the gains of the AE and BE to 11 and 9, respectively, ETIs of up to 550kΩ can be measured at the expense of less gain (≈100) in the EEG channel. In principle, even larger ETIs can be measured by lowering the amplitude of the injected current.

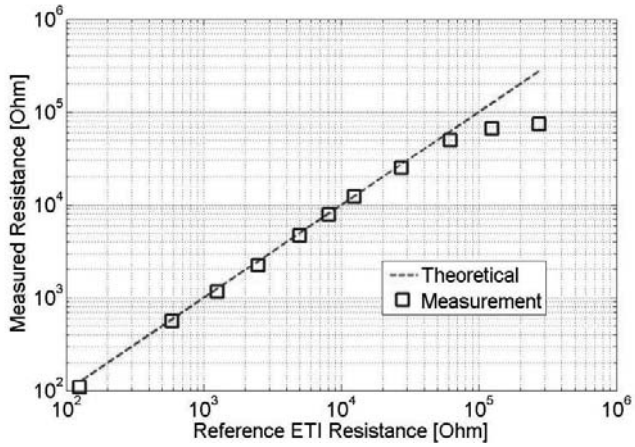


Figure 4.19 Measured differential ETI resistance.

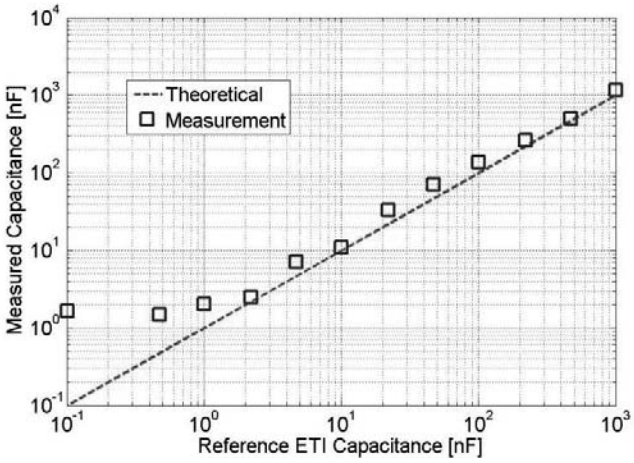


Figure 4.20 Measured differential ETI capacitance.

Table 4-2 compares the analog performance of the proposed 8-channel AE system with state-of-the-art AE systems. The proposed system is able to measure EEG and ETI signals simultaneously while still achieving very competitive performance on input impedance, noise, electrode offset tolerance, and CMRR. When it was published in [90], the proposed AE system also achieves the lowest power dissipation per channel.

Table 4-2: Comparison table with the state-of-the-art AE System for biopotential signal acquisition.

Parameters	[80]+[91]	[92]	[93]	[94]	This work
Technology	0.18µm	N/A	0.35µm	N/A	0.18µm
Supply	1.8V	5V	3V	3.3V	1.8V
AE Gain	3-100	100	N/A	11	11-101
Input Impedance	0.6GΩ@10Hz	1TΩ@DC	N/A	N/A	1.2GΩ@20Hz
Noise per Channel	1.2µV_{rms} (0.5-100Hz)	7.49µV_{rms} (1-1kHz)	0.9µV_{rms} (0.5-100Hz)	2.4µV_{rms} (0.5-100Hz)	1.75µV_{rms} (0.5-100Hz)
Electrode Offset Rejection	Rail-to-rail	±250mV	N/A	Rail-to-rail	±250mV
CMRR	82dB	78dB	105dB	90dB	84dB
ETI Measurement	No	No	Yes	No	No
Power per Channel (including ADC)	20µW (excl. [91])	7.5mW	1mW	600µW	82µW (EEG + ETI)

4.6 A 4-Channel Wireless EEG Headset

The low-power highly-integrated AEs and BE are well suited for a battery-powered wearable EEG device. A 4-channel wireless EEG headset using these chips has been implemented (Figure 4.21). The headset consists of four record-

ing AEs, one reference AE, and one bias electrode. Two mechanical bridges cover all the electrode positions and have compartments for sensor node electronics and battery. The recording AEs are positioned at predefined positions C_3, C_4, C_z and P_z according to a 10-20 electrode EEG system. The reference AE and bias electrode are positioned behind the ears on the mastoid bone. All these electronics are connected via flat cables and embedded in the headset.

The digital outputs of BE ASIC are streamed out to a low-power microcontroller [95] via a SPI protocol and stored in local memory. The data is then transmitted wirelessly to a PC through a low-power radio [96]. The data transmission of microcontroller and radio occupies more than 80% of the system power, while AEs and BE only consume 5%.

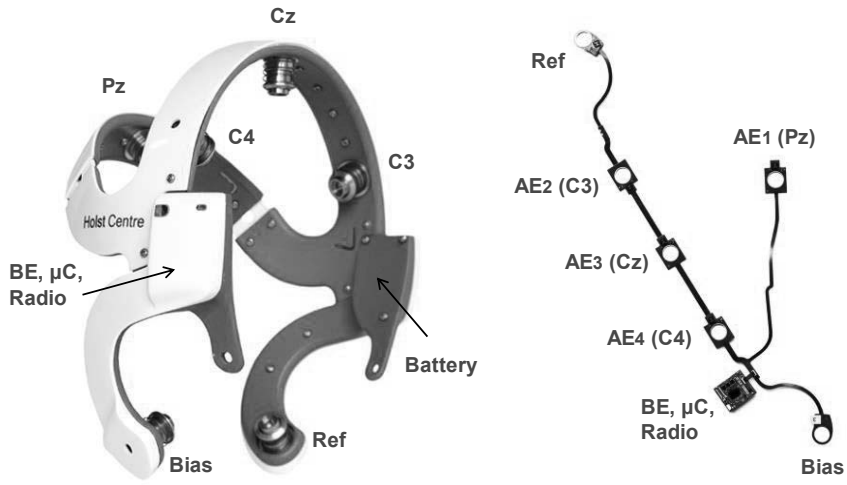


Figure 4.21 Wireless EEG headset and its internal electronics.

Figure 4.22 shows the spectrogram of 4-channel EEG signals measured from a subject whose eyes were alternately opened and closed. There is no alpha wave during the eyes-open period for all channels, except some artifacts due to blinking. During the eyes-closed period, the alpha waves at 10Hz are clearly visible on all four channels.

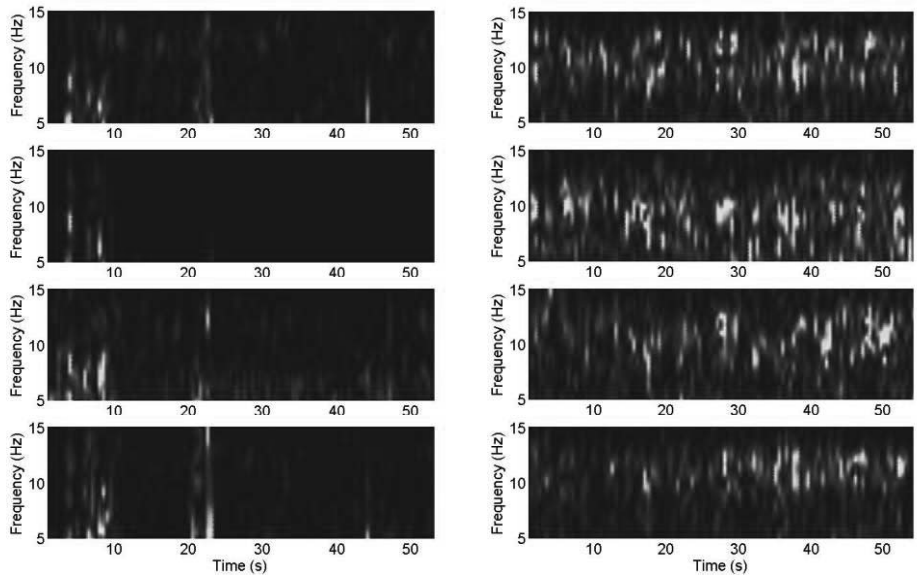


Figure 4.22 4-channel real-time EEG recording using a dry-electrode wireless headset, during eyes open (left) and eyes closed (right). Output channels from top to bottom: C3, C4, Cz, Pz.

4.7 Conclusions

This chapter presents a complete 8-channel active electrode (AE) system for simultaneous EEG/ETI measurement with dry electrodes. The whole system consists of nine AEs for high performance pre-amplification, and a low-power highly configurable BE for analog signal processing and digitization. Several techniques were implemented to improve the system performance. At the AE level, electrode offset is rejected by a low-power DSL around a non-inverting chopper IA, whose input stage utilizes improved transconductance for greater noise efficiency. At the system level, a CMFF technique improves the CMRR of an AE pair by 25dB; a single-wire PWM modulation reduces the number of wires between the AEs and the BE; and a continuous-time ETI measurement can sense electrode impedances up to 550kΩ. To demonstrate its functionality, the AE system was used to realize a battery-powered wireless EEG headset.

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CHAPTER 5

CURRENT NOISE OF CHOPPER AMPLIFIERS[4]

5.1 Introduction

Two types of AE architectures have been proposed, namely an inverting chopper IA (Chapter 3) and a non-inverting chopper IA (Chapter 4). The former architecture provides rail-to-rail electrode offset tolerance at low power consumption, while the latter has a better tradeoff between input impedance and noise. However, a remaining issue for both of these architectures is the occurrence of extra $1/f^2$ noise at low frequencies.

This chapter investigates the root cause of $1/f^2$ noise of chopper amplifiers through a theoretical analysis and measurements of several chopper IAs. It is well known that the charge injection and clock feed-through associated with the MOSFETs of the input chopper give rise to significant input current and current noise, which may then be a significant contributor to the amplifier's total input-referred voltage noise. Furthermore, the chopper noise has a white power spectral density, whose magnitude is roughly proportional to the chopping frequency. Design guidelines are proposed to reduce the chopper noise. A further proposal is the use of a clock-bootstrapped chopper, which exhibits less noise than a traditional chopper.

5.2 Chopping and Current Noise

Chopping is a continuous-time technique in which polarity-reversing switches, known as choppers, are used to modulate amplifier offset and $1/f$ noise to a certain chopping frequency, thus enabling the realization of precision amplifiers with low voltage noise and low offset [97]. As a result, chopper amplifiers

[4] This chapter is derived from a journal publication of the authors: J. Xu, Q. Fan, et al., "Measurement and Analysis of Current Noise in Chopper Amplifiers" *IEEE J. Solid-State Circuit*, vol.48, no.7, pp. 1575-1584, July. 2013.

are often used in applications where precision signal conditioning is required, e.g., in smart sensors, sensor interfaces [98], medical instruments [99], and precision voltage references [100].

In CMOS, the switches of a chopper are usually implemented as MOSFETs. Although it is well known that the transient spikes caused by charge injection and clock feed-through of these periodically switched devices will give rise to a net input current [101][102], not much is known about the associated current noise. In [103], the current noise of a chopper amplifier was attributed to the shot noise associated with this input current. In [104], measurements of the current noise of a chopper amplifier are described. Although the cause of this noise was not explained, it was observed that the measured noise density was proportional to the square root of the chopping frequency and was in the order of several tens of fA/sqrt(Hz). This is roughly a hundred times higher than the current noise of conventional CMOS- or JFET-input amplifiers [105][106]. Some commercially available chopper amplifiers exhibit even higher current noise densities (≥100fA/sqrt(Hz)) [107]-[109]. When used with high impedance sensors such as dry electrodes, photodiodes and piezoelectric sensors, this current noise will be converted to voltage noise, which will then add to, and may even dominate, the IA's total input-referred voltage noise [110].

5.3 Current Noise Analysis

Figure 5.1 shows the equivalent input circuit of a chopper IA connected to a differential voltage source. The IA's noise is modeled by an input-referred voltage noise source ($v_{n,IA}$) and an input-referred current noise source ($i_{n,IA}$), while the IA itself is considered to be ideal and noiseless. $R_{s1,2}$ models the source resistances. The total input-referred voltage noise can then be written as

$$\overline{V_{in,amp}^2} = \overline{V_{in,IA}^2} + \overline{I_{in,IA}^2} \cdot \left(R_{s1} + R_{s2}\right)^2 + 4kT\left(R_{s1} + R_{s2}\right) \tag{5-1}$$

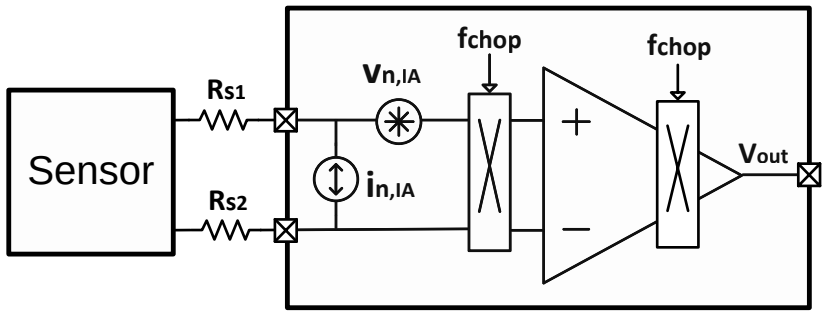

Figure 5.1 Equivalent circuit model which describes the excess voltage noise due to the source impedance and input current noise of a chopper amplifier.

The input bias current of a CMOS amplifier is usually quite low (in the order of a few pA [105]) and is dominated by the gate leakage current of the input transistors and the leakage current of the ESD protection circuit. The associated current noise ($i_{n,IA}$) is mainly due to shot noise, and so is also quite low (<1fA/sqrt(Hz)) [105][106]. Hence, the current noise of a CMOS amplifier is usually a negligible contributor to its total input-referred noise.

However, CMOS chopper amplifiers exhibit substantially higher levels of current noise [107]-[109]. This excess noise must therefore be related to the periodic switching of the MOSFET switches of the input chopper. The rest of this section presents an analysis of the major noise sources associated with this activity.

5.3.1 Charge Injection and Clock Feed-Through

Charge injection and clock feed-through are well-known error sources associated with MOSFET switches. In a chopper, one pair of switches will be "on", while the other is "off". As shown in Figure 5.2, when a pair of NMOS switches is turned off, their channel charge and some of the charge in their overlap capacitance (C_{ol}) will be injected into the circuitry connected to their drain and source terminals (modeled by the capacitors C_s and C_i) [111].

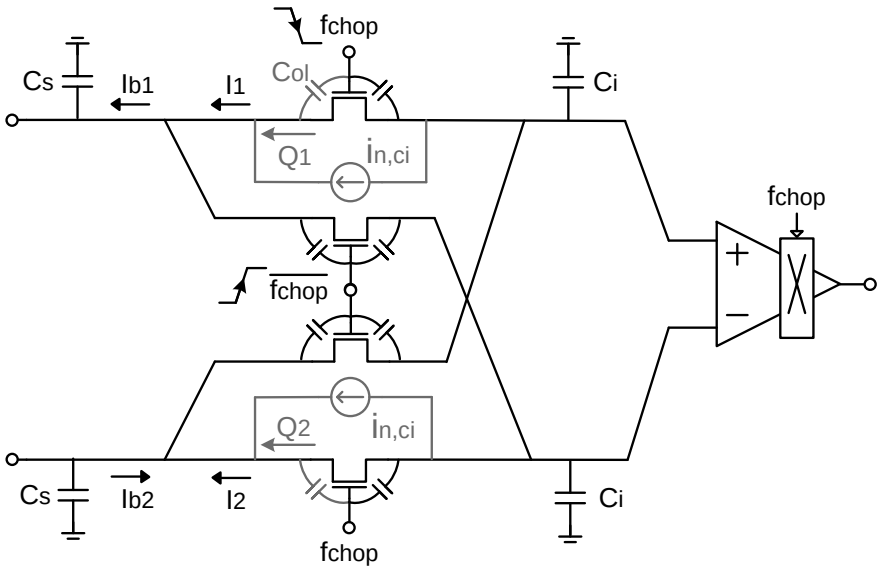

Figure 5.2 Charge injection and clock feed-through of the input chopper switches.

The total charge ($Q_{1,2}$) that is injected into the source (or drain) circuit is given by (5-2), where W and L are the width and length of the chopper switches, C_{ox} is the gate oxide capacitance, C_{ol} is the overlap capacitance between gate and source (drain), V_{od} is the overdrive voltage, and V_{clk} is the clock swing.

$$Q_{1,2} = WLC_{ox}V_{od} + C_{ol}V_{clk} \tag{5-2}$$

This periodic charge injection and clock feed-through at the chopping frequency causes transient current spikes (Figure 5.3), whose average value ($I_{1,2}$) is given by

$$I_{1,2} = \frac{Q_{1,2}}{T_{chop}/2} = 2f_{chop}\left(WLC_{ox}V_{od} + C_{ol}V_{clk}\right) \tag{5-3}$$

Ideally, the transient current spikes caused by a pair of chopper switches turning off should be compensated by the charge required to turn on

the other pair, leading to a net zero input current. However, mismatch between the switches and slight differences in their turn-on and turn-off times results in a net input current with a typical magnitude of several tens of pA [112][113]. This is much larger than the gate leakage currents of the MOSFETs or the leakage currents of the ESD diodes. The right-hand side of (5-3) may thus be regarded as an upper bound, especially since the exact amount of input current will also depend on the relative magnitudes of the capacitances C_i and C_s connected to the chopper. From (5-3), the input current should be proportional to the chopping frequency, which is in good agreement with the measurements reported in [104].

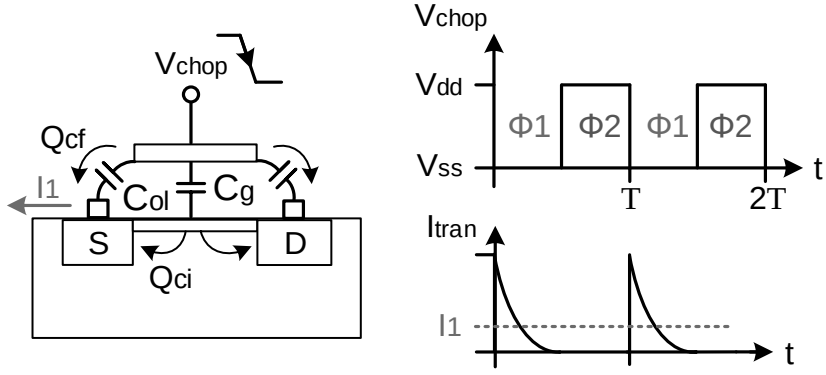

Figure 5.3 Periodic charge injection and associated transient current of an input chopper switch.

5.3.2 Shot Noise due to the MOSFETs Channel Charge

Shot noise is associated with the non-uniform flow of charge carriers in semiconductors. This noise has a white noise spectrum, whose PSD is proportional to the average current [114][115]. Since the current spikes associated with the charge injection of the MOSFETs in the periodically-switched MOSFETs give rise to a net input current, the hypothesis is that this current will also be accompanied by shot noise [103]. The PSD of this current noise should then be linearly dependent on the average current $I_{1,2}$ through the chopper switches, as shown in (5-4), where $q=1.6e^{-19}$ C is the electron charge. The average noise density of this impulse noise can then be expressed as

$$\overline{i_{n,ci}^2} \propto 2qI_{1,2} \qquad \overline{i_{n,ci}^2} \propto 4qf_{chop}WLC_{ox}V_{od} \tag{5-4}$$

This indicates that the current noise PSD associated with charge injection should also be linearly dependent on the chopping frequency.

5.3.3 KT/C Noise from the Clock Driver

The clock driver circuit is another possible source of noise. As shown in Figure 5.4, it can be modeled as a resistance (R_g) in series with the gate-source capacitance (C_{gs}). Since this resistor (and any other series resistance in the gate charging circuit) will generate thermal noise, the channel charge will fluctuate, and so a certain noise charge will be injected into the surrounding circuitry every time the MOSFET is turned off. The root mean square (rms) value of this noise charge ($Q_{n,rms}$) can be expressed as

$$Q_{n,rms} = \sqrt{kTC_{gs}} = \sqrt{kTWLC_{ox}} \tag{5-5}$$

As before, this periodically injected noise charge will give rise to an average RMS noise current of

$$\overline{i_{n,rms}} = 2f_{chop}Q_{n,rms} = 2f_{chop}\sqrt{kTWLC_{ox}} \tag{5-6}$$

Assuming that this impulse noise is approximately white and distributed over the fundamental interval between 0 and $f_{chop}/2$, then its PSD is given by

$$\overline{i_{n,cd}^2} = \frac{\overline{i_{n,rms}^2}}{\Delta f} = 8 f_{chop} kTWLC_{ox} \tag{5-7}$$

This PSD is also a linear function of the chopping frequency.

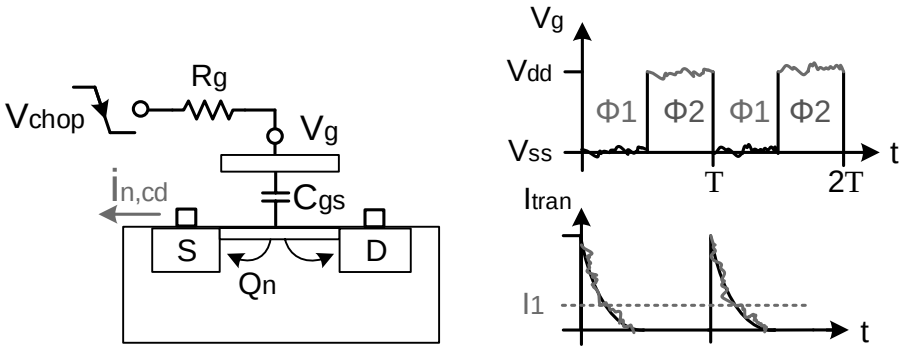

Figure 5.4 Periodical noise charge injection and associated noise current of an input chopper switch.

5.3.4 Parasitic Switched-Capacitor (SC) Resistance

Due to the action of the input chopper, the amplifier's input parasitic capacitances (C_P) will be charged and discharged by the input voltage and give rise to a net DC current [101][102]. As shown in Figure 5.5, this effect can be modeled by a switched-capacitor resistor (R_{sc}) at the amplifier's input [116][117]. This resistance generates current noise in the same manner as a physical resistor [118].

$$\overline{i_{n,sc}^2} = \frac{4kT}{R_{sc}} \qquad R_{sc} = \frac{1}{2 f_{chop} C_p} \tag{5-8}$$

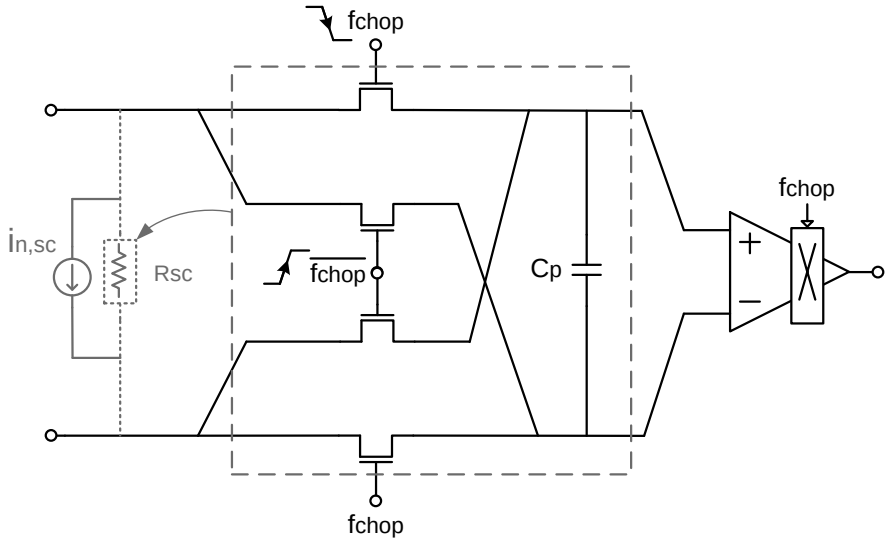

Figure 5.5 Input parasitic SC resistance of a chopper amplifier.

The resulting current noise PSD is again proportional to the chopping frequency (f_{chop}) and to the input parasitic capacitance (C_P) of the amplifier. Since the switched-capacitor resistor is usually quite large (tens or even hundreds of MΩ), the magnitude of the current noise PSD is usually negligible.

5.3.5 Summary

The total chopper noise PSD ($i_{n,IA}$) is obtained by summing the contributions of all the above-mentioned current noise sources. Table 5-1 shows the parameters of the MOSFET switches (in an ON Semiconductor 0.5μm CMOS process) used in the input chopper of a CMOS chopper IA [99]. Also shown is the calculated contribution of each noise source, assuming that eight of these transistors (four NMOS and four PMOS) are used to realize the four complementary switches of its input chopper. The results show that the total current noise is dominated by the contribution of charge injection, and so from (5-4), the chopper noise PSD should be linearly proportional to the chopping frequency.

Table 5-1: Parameters of a typical MOSFET switch in 0.5μm CMOS technology and calculated current noise-induced contribution to voltage noise density of a CMOS chopper consisting of eight MOSFETs (T=25°C or 298K).

Parameters	Explanations	Typical Value	Unit
W	Width	30	μm
L	Length	0.5	μm
C_{ox}	Gate oxide capacitance	2.5	fF/μm^2
V_{gs}	Gate-source voltage	1.9	V
V_{th}	Threshold voltage	0.7 (NMOS) 0.9 (PMOS)	V
f_{chop}	Chopping frequency	4	kHz
C_p	Input parasitic capacitance	125	fF
$i_{n,ci}$	Current noise density (charge injection)	30.4	fA/sqrt(Hz)
$i_{n,cd}$	Current noise density (kT/C noise)	1.1	fA/sqrt(Hz)
$i_{n,sc}$	Current noise density (parasitic SC resistance)	4.1	fA/sqrt(Hz)

5.4 Current Noise Measurement

5.4.1 A Conventional Chopper Modulated IA

Figure 5.6 shows the schematic used to measure the current noise of a chopper IA. Its input chopper consists of 4 complementary CMOS switches, whose characteristics are shown in Table 5-1. The IA is configured with a voltage gain of 800 and a bandwidth of 200Hz. Since it was intended for biomedical applications, an internal DC-servo loop ensures that the amplifier has a high-pass characteristic with a corner frequency of approximately 0.5Hz.

A low-noise input bias voltage, V_b, is generated from a 3.3V battery. Two large resistors (R_s=10MΩ) ensure that the chopper IA's current noise is the dominant contributor to its total input-referred noise; i.e., that equations in (5-9) are satisfied [119].

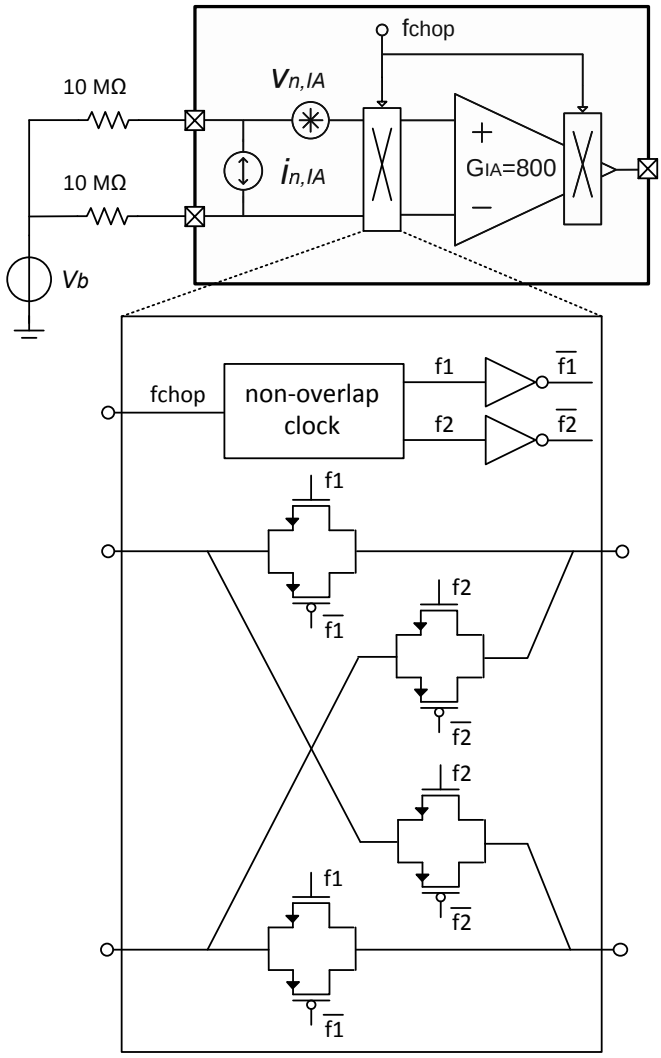

Figure 5.6 Schematic illustration of current noise measurement of a chopper IA.

$$\overline{i_{n,IA}^2}R_s^2 > \overline{v_{n,IA}^2} \qquad \overline{i_{n,IA}^2}R_s^2 > 4kTR_s \tag{5-9}$$

The input current noise PSD can then be determined from (5-10), where $v_{n,out}$ is the measured output noise voltage, G is the IA's voltage gain, and the IA's voltage noise $v_{n,IA}$ and source resistance R_s are known. Note that the thermal noise of the choppers' on-resistance is included in the measured $v_{n,IA}$.

$$\overline{i_{n,IA}^2} = \left(\frac{\overline{v_{n,out}^2}}{G^2} - \overline{v_{n,IA}^2} - 8kTR_s \right) \Big/ 2R_s^2 \qquad (5\text{-}10)$$

Figure 5.7 and Figure 5.8 show the measured voltage gain (G) and the input-referred voltage noise density ($v_{n,IA}$) of the chopper IA, respectively. These results were used to determine the input-referred current noise density and confirm the proper operation of the IA at the various chopping frequencies.

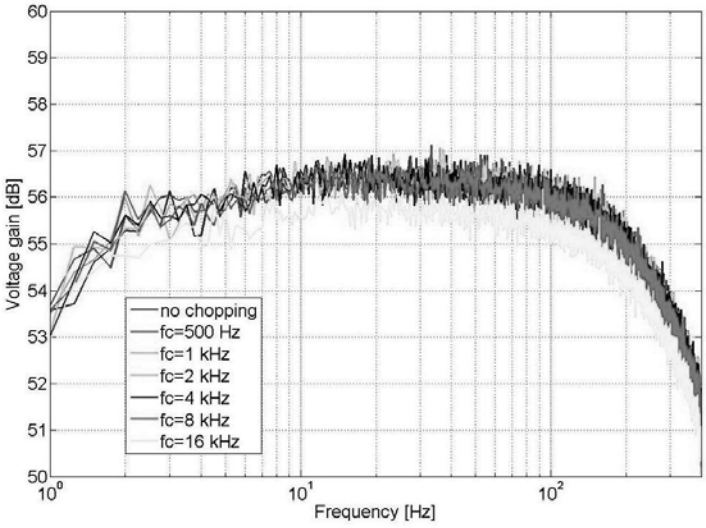

Figure 5.7 Measured voltage gain (G) of the chopper IA.

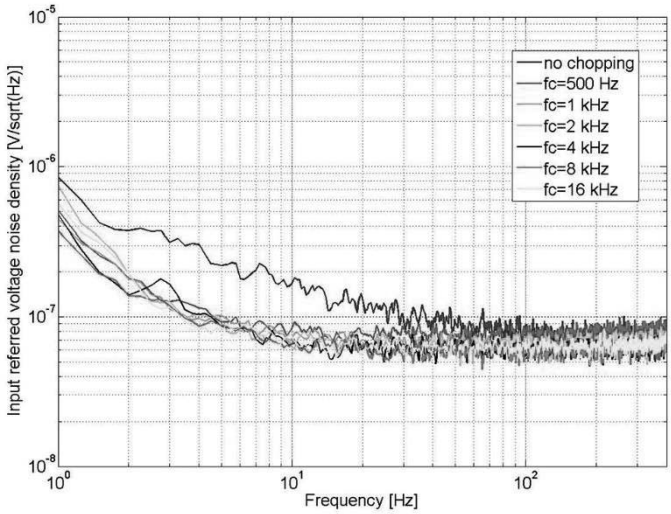

Figure 5.8 Measured input-referred noise ($v_{n,IA}$) of the chopper IA.

The measured input-referred current noise PSD at various chopping frequencies is shown in Figure 5.9 and Figure 5.10. As predicted by (5-4), the PSD of this chopper noise is linearly proportional to f_{chop}. Figure 5.11 shows that, the measured input current noise density is independent of the value of source resistance, as expected.

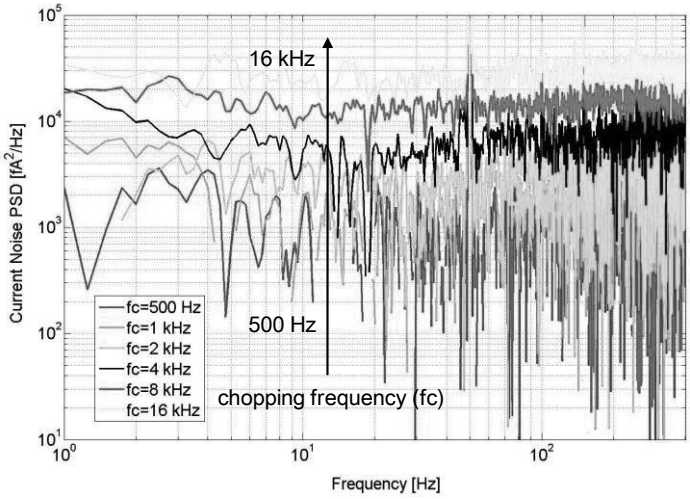

Figure 5.9 Measured input current noise PSD ($i_{n,IA}$) of the chopper IA.

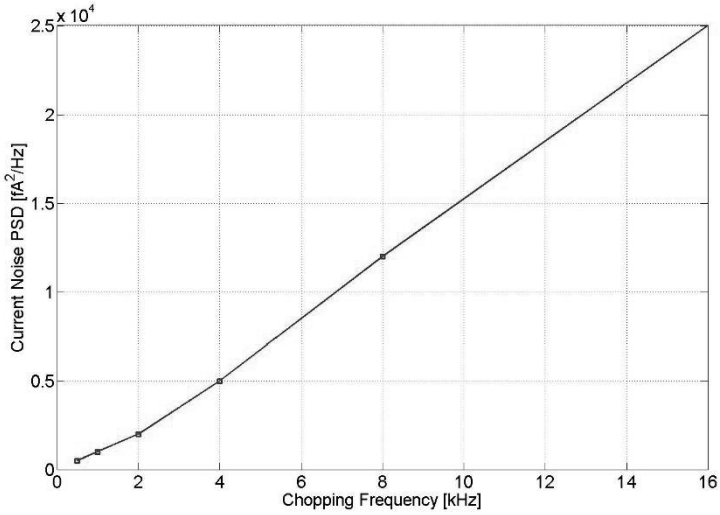

Figure 5.10 Input current noise PSD versus chopping frequencies.

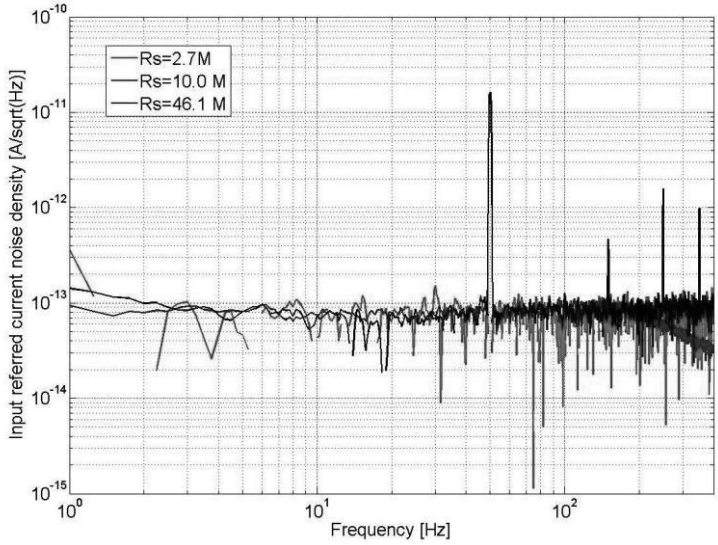

Figure 5.11 Measured input noise current density (in,IA) with different source resistors (fchop= 4kHz).

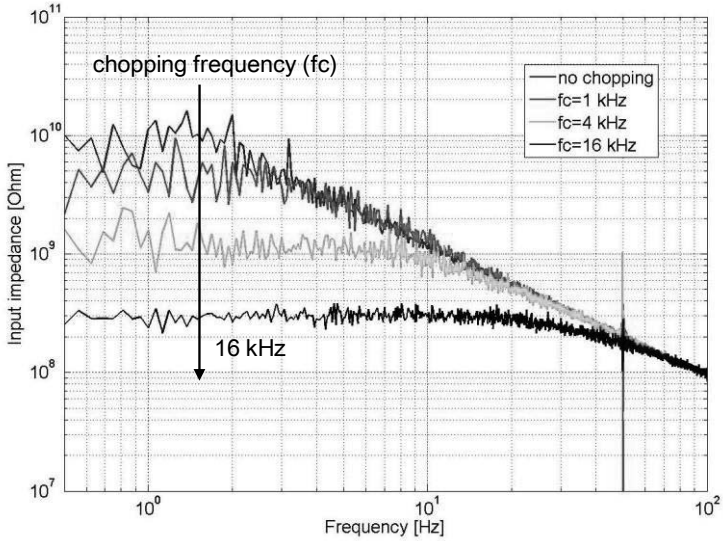

Figure 5.12 Measured SC input impedance of the chopper IA.

Figure 5.12 shows the measured SC input impedance of the chopper IA at different chopping frequencies. The smallest input impedance is about 250MΩ, which corresponds to the highest chopping frequency of 16kHz. Hence, the maximum current noise density associated with this SC input impedance is only 8fA/sqrt(Hz), which is negligible compared to the measured total current noise density of 158fA/sqrt(Hz) at this chopping frequency.

5.4.2 Chopper Amplifiers with Capacitive Feedback

In other IA architectures, chopper noise will also cause significant excess voltage noise when the input chopper is located at a high-impedance internal node. For example, consider the inverting IA shown in Figure 5.13, which has been presented in Chapter 3. This IA utilizes a coupling capacitor (C_1) to block the input DC offset, while using a pseudo resistor (R_2) and a capacitor (C_2) in the feedback path to define its voltage gain and establish a high-pass corner at about 0.5Hz. As a result, the IA's virtual ground is a high-impedance node, which converts chopper noise into a significant amount of excess voltage noise. The IA was implemented in a standard 0.18μm process, and its input chopper consists of four NMOS devices (W/L=0.5/0.18).

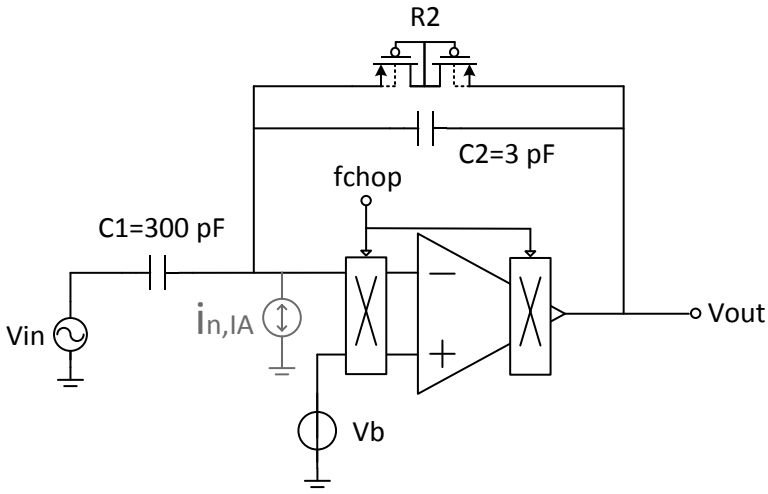

Figure 5.13 Inverting chopper IA.

Due to the presence of C_2 in the feedback path, the excess voltage noise PSD exhibits a $1/f^2$ spectrum (with a pole at $1/R_2C_2$), which is given by

$$\overline{i_{excess,ICA}^2} \approx \overline{i_{n,IA}^2} \cdot \left(\frac{R_2}{1+sR_2C_2} \right)^2 \tag{5-11}$$

With chopping disabled, the current noise is quite low, and so any $1/f^2$ noise is buried in $1/f$ noise. This has been verified by periodic noise simulations and measurements (Figure 5.14), where P_{noise} refers to the periodical noise simulation, and I_{ns} is the noise density of the additional current noise source. As can be seen, the simulation results match the measurement results well.

With chopping enabled, however, the ensuing chopper noise results in an excess of $1/f^2$ voltage noise, which dominates the IA's noise performance (Figure 5.15). In order to simulate the effect of chopper noise, a current noise source at the high-impedance chopping node (Figure 5.13) was added. As shown in Figure 5.15 to Figure 5.18, its magnitude was then adjusted to fit the measurements obtained at different chopping frequencies. The resulting current noise densities range from 7.5fA/sqrt(Hz) at f_{chop}=500Hz (Figure 5.15) to

21fA/sqrt(Hz) at f_{chop}=5kHz (Figure 5.18) and are in line with (5-4), and are roughly proportional to the square root of the chopping frequency.

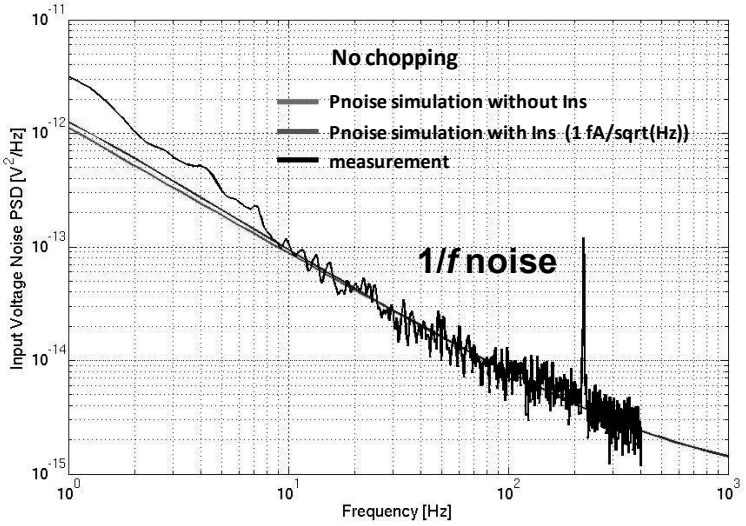

Figure 5.14 Measured and simulated input referred noise of an inverting IA without chopping.

A similar effect occurs in the non-inverting chopper IA [120] shown in Figure 5.19, which was also implemented in a 0.18μm process and has been presented in Chapter 4. The IA utilizes a CMOS chopper with equally sized PMOS and NMOS devices (W/L=2/0.18). With chopping disabled, the IA's 1/*f* noise is dominant, and the measured noise is again in good agreement with simulations (Figure 5.20). With chopping enabled, $1/f^2$ noise becomes dominant since the IA's inverting input is a high-impedance node. The measured noise corresponds to a current noise density that ranges from 12fA/sqrt(Hz) at f_{chop}=500Hz to 32.5fA/sqrt(Hz) at f_{chop}=5kHz, as shown in Figure 5.21 to Figure 5.24, respectively. Similarly, the current noise density is roughly proportional to the square root of the chopping frequency. In this design, the feedback capacitors were much larger (16x) than those in the inverting IA, and so, although the $1/f^2$ corner is still dominant, its corner frequency is significantly lower.

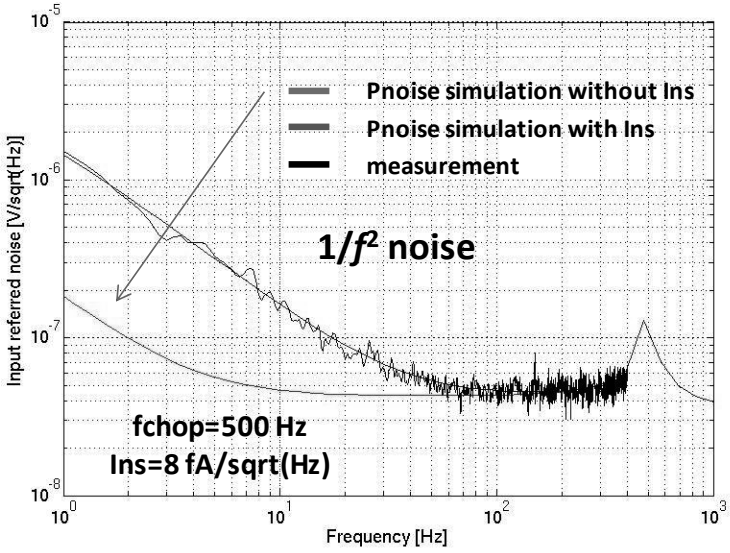

Figure 5.15 Measured and simulated input referred voltage noise of an inverting chopper IA at f_{chop}=500Hz.

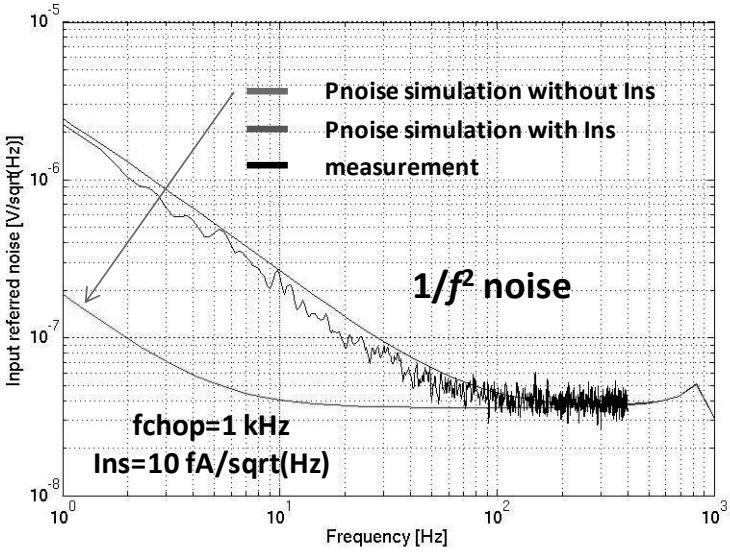

Figure 5.16 Measured and simulated input referred voltage noise of an inverting chopper IA at f_{chop}=1kHz.

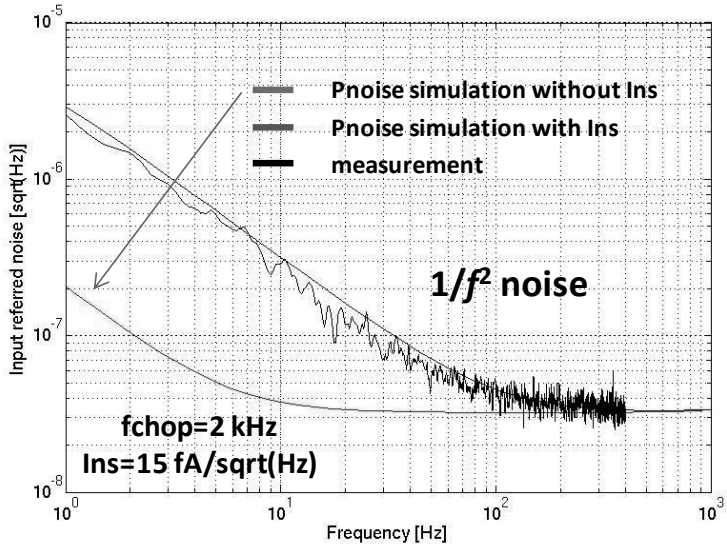

Figure 5.17 Measured and simulated input referred voltage noise of an inverting chopper IA at f_{chop}=2kHz.

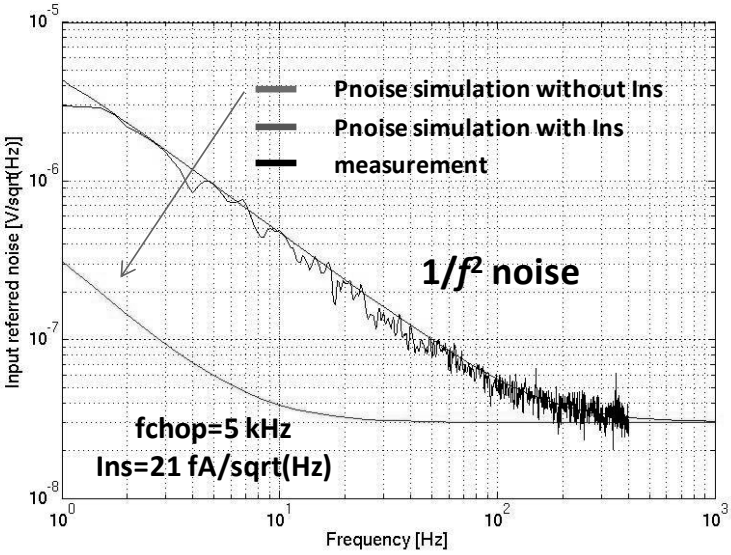

Figure 5.18 Measured and simulated input referred voltage noise of an inverting chopper IA at f_{chop}=5kHz.

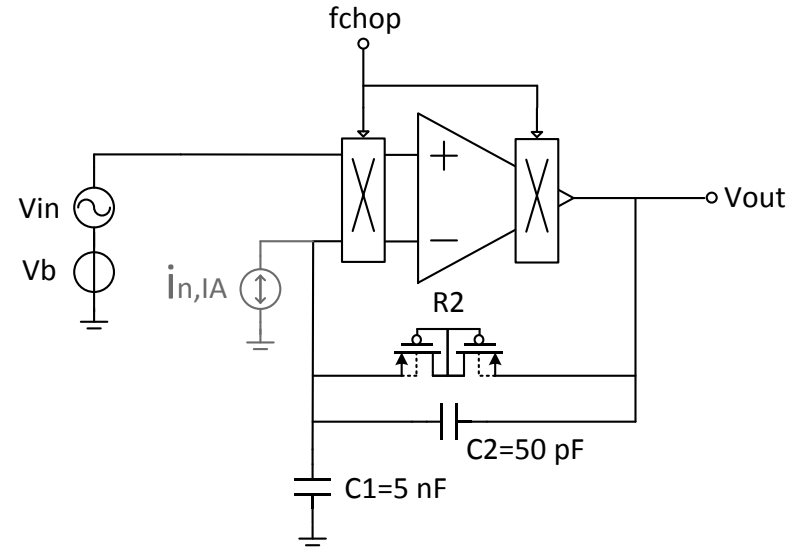

Figure 5.19 Non-inverting chopper IA.

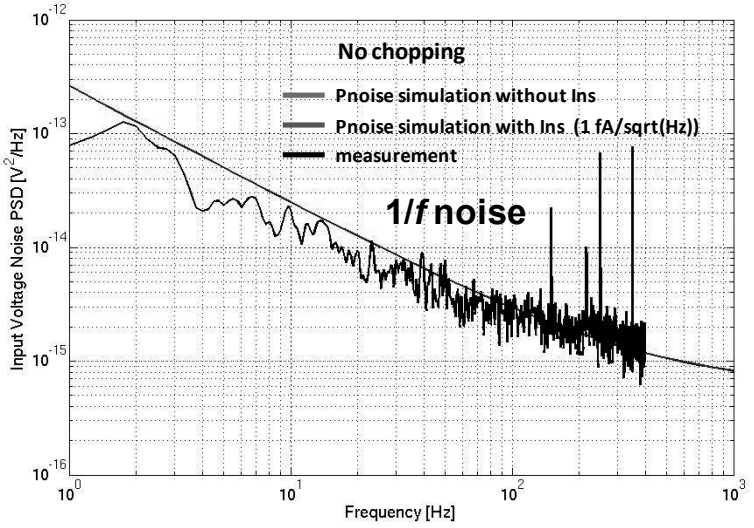

Figure 5.20 Measured and simulated input referred voltage noise of a non-inverting IA without chopping.

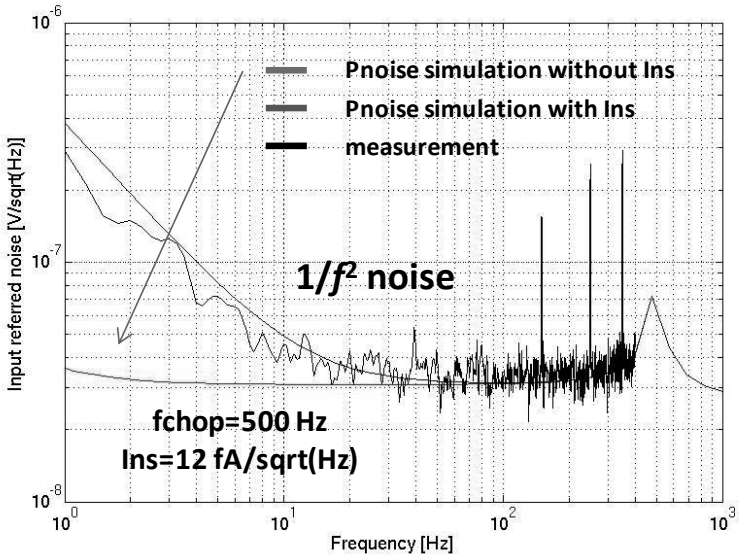

Figure 5.21 Measured and simulated input referred voltage noise of a non-inverting IA at f_{chop}=500Hz.

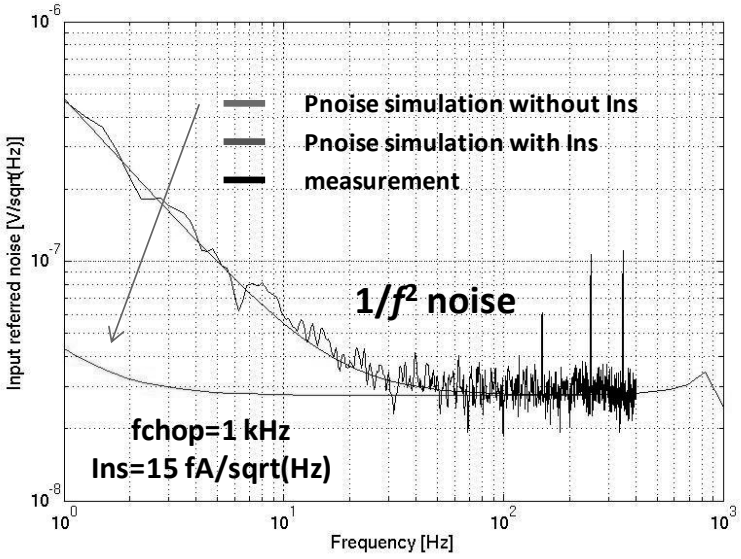

Figure 5.22 Measured and simulated input referred voltage noise of a non-inverting IA at f_{chop}=1kHz.

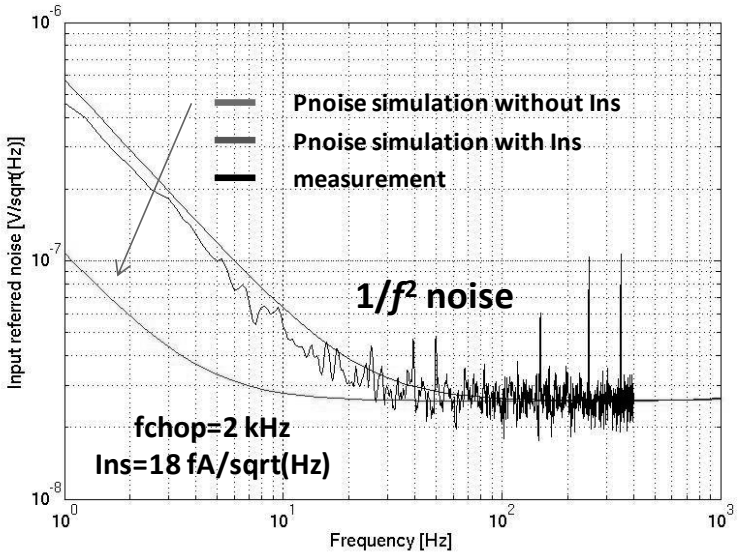

Figure 5.23 Measured and simulated input referred voltage noise of a non-inverting IA at f_{chop}=2kHz.

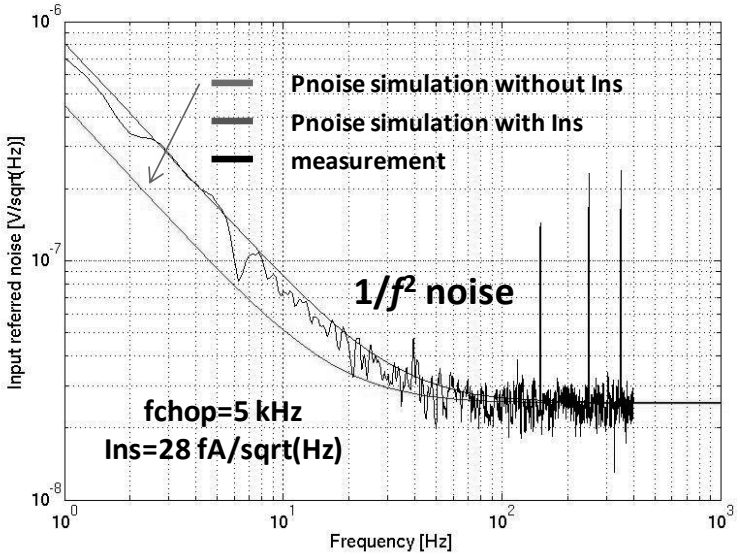

Figure 5.24 Measured and simulated input referred voltage noise of a non-inverting IA at f_{chop}=5kHz.

5.5 A Dedicated Noise-Testing Chip

In order to investigate the relationship between chopper noise, charge injection and clock feed-through, a dedicated noise-testing chip was implemented in a 0.18μm CMOS process (Figure 5.25). The chip consists of four chopper IAs, similar to the one described in [99], but each equipped with four different types of input choppers (Figure 5.26): an NMOS chopper, an NMOS chopper with dummy switches, a CMOS chopper, and a bootstrapped NMOS chopper with a low-swing chopper clock. The NMOS chopper was used as a reference, while the other three types of choppers represent various known methods of reducing charge injection and clock feed-through errors.

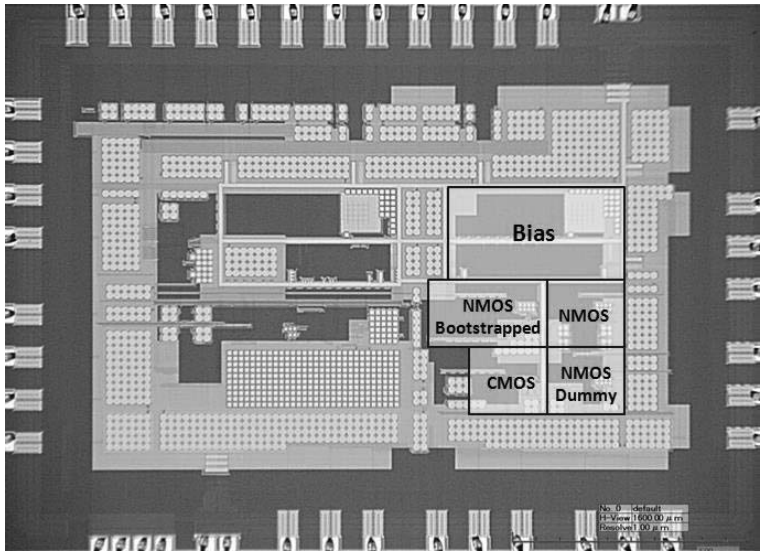

Figure 5.25 Chip photograph of the noise-testing chip.

As in [121], the bootstrapped NMOS chopper uses a capacitively-coupled clock driver to ensure that the MOSFETs are driven at a constant overdrive voltage that is independent of input CM variations. This can also be achieved with a switched-capacitor scheme proposed in [122]. The coupling capacitors and the chopping clock amplitude are chosen such that the amplitude of the resulting V_{gs} is reduced by a factor of 2. To maintain the IA's high input impedance, a voltage follower is used to buffer the input CM voltage and supply the current spikes required by the clock drivers [122].

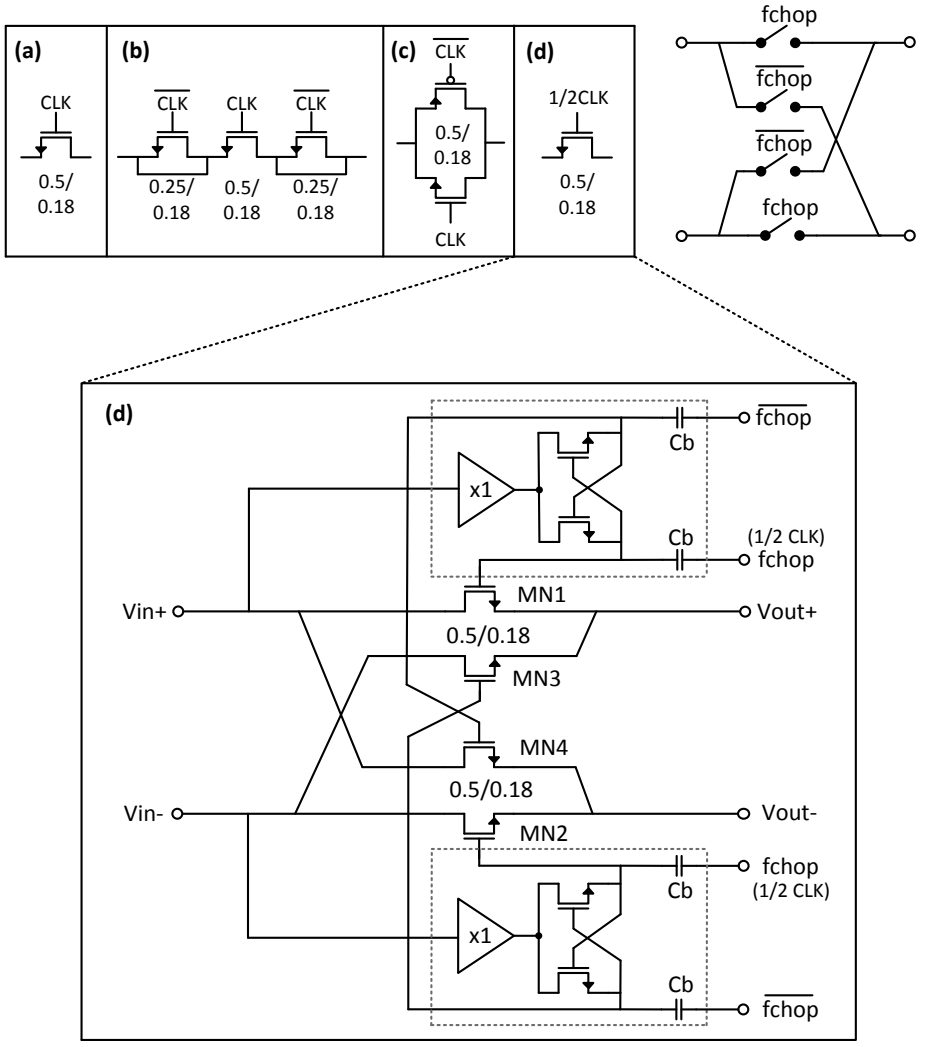

Figure 5.26 Four types of input chopper switches: a) NMOS, b) NMOS with dummy switches, c) CMOS, and d) NMOS with bootstrapped clock drivers.

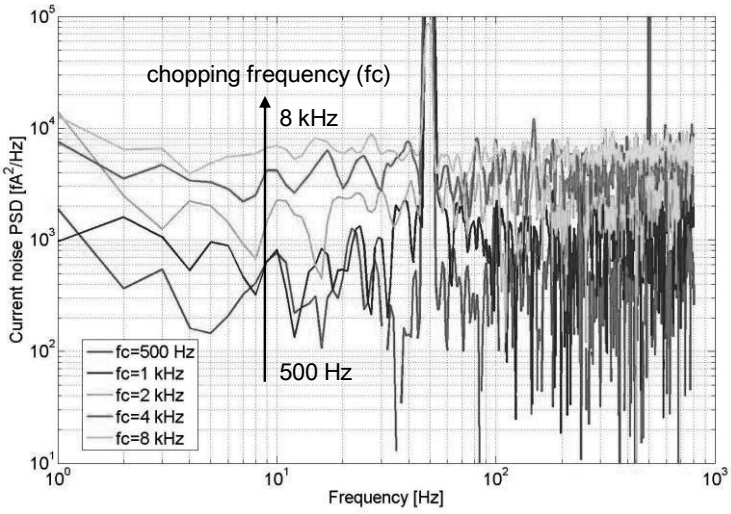

Figure 5.27 Current noise PSD comparison of NMOS chopper IAs at various chopping frequencies.

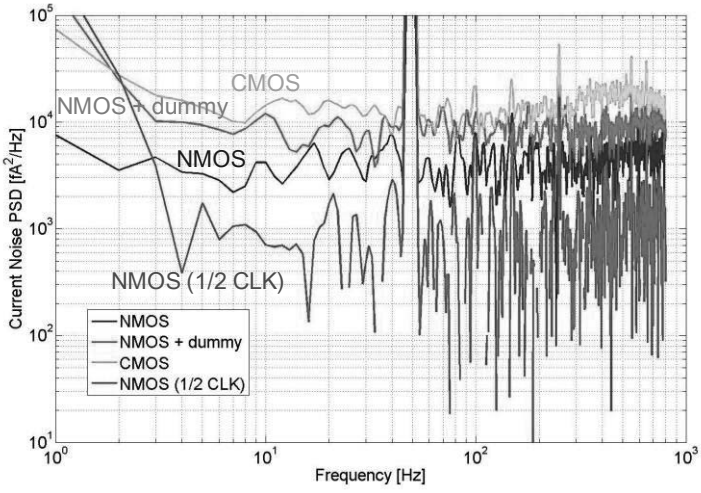

Figure 5.28 Current noise PSD comparison of four chopper IAs (f_c=4kHz).

The current noise PSD of the reference NMOS chopper shows the expected linear relation with the chopping frequency (Figure 5.27). The current noise PSD produced by the four input choppers is compared in Figure 5.28. It is interesting to note that both the CMOS chopper and the NMOS chopper with

dummy switches generate more current noise than the reference NMOS chopper, while the bootstrapped NMOS chopper generates the lowest current noise. The reason for this is that chopper noise is related to the charge injection, and hence the shot noise, which is associated with the individual chopper switches. As such, it cannot be cancelled by using dummy or complementary MOSFETs. In fact, the use of additional MOSFETs only increases the total amount of charge injection and hence the total amount of current noise. However, the bootstrapped NMOS chopper is driven by a low-swing clock, which reduces its charge injection and thus leads to less current noise.

As shown in Figure 5.29, all the alternative chopper architectures do reduce the IA's DC input current to various degrees. Apparently, the charge injection of the main NMOS switches can be significantly reduced by a low-swing clock driver, and effectively cancelled by the use of simultaneously-clocked PMOS or dummy switches, thus leading to lower input currents. As expected from (5-3), the input current of all four chopper IAs increases monotonically with f_{chop}.

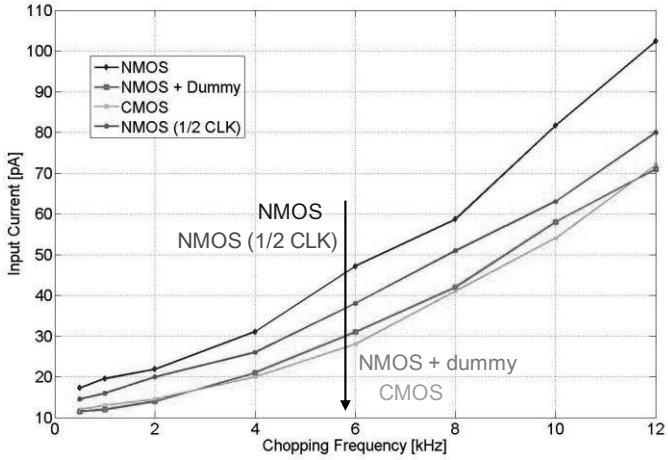

Figure 5.29 Input current comparison of four chopper IAs.

5.6 Methods of Reducing Current Noise

From the measurements on the noise-testing chip, reducing the charge injection associated with the individual chopper switches is the best way to reduce chopper noise. This observation suggests the use of minimum-size NMOS or PMOS switches (subject to on-resistance considerations), the lowest possible

chopping frequency (subject to $1/f$ noise considerations), and the use of a low-swing clock driver (again subject to on-resistance considerations) to achieve this reduction. In this chapter, a bootstrapped clock driver uses a constant overdrive voltage to drive the MOSFETs of the input chopper. In some cases, it may be possible to simply avoid chopping at high impedance nodes [123]. In a chopper IA with capacitive feedback, for instance, the input chopper can be located at the output, rather than at the input, of the input stage. This will eliminate the excess voltage noise $1/f^2$ caused by chopper noise. Although the $1/f$ noise of the input stage will now not be chopped, its effect can be somewhat reduced by increasing the size of the input MOSFETs.

5.7 Conclusion

This chapter presents a theoretical analysis and experimental verification of the current noise generated by chopper IAs. This current noise is associated with the charge injection of the input chopper's MOSFET switches, which, in turn, gives rise to a net input current and, we hypothesize, to shot noise. The resulting chopper noise has a white noise spectrum, and its PSD is roughly linearly proportional to the chopping frequency. When chopping is performed at very high-impedance nodes, e.g., in IAs with capacitive feedback networks, chopper noise can cause significant amounts of voltage noise, which may then dominate the amplifier's overall noise performance. The use of a bootstrapped clock driver, which drives the input chopper's MOSFETs with reduced overdrive voltages, is shown to significantly reduce chopper noise.

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CHAPTER 6

A DIGITAL ACTIVE ELECTRODE SYSTEM[5]

6.1 Introduction

Previous chapters present several AE architectures with analog outputs. These analog AEs achieve good performance at a low power consumption. However, there are still limitations remaining. The major one is the use of multiple ASICs (AEs and BE), which increase the total cost of an AE system. In addition, the maximum number of recording channels can be practically limited by the number of connecting wires required by the various AEs. A multi-channel AE based EEG system typically requires tens of wires connected to the BE, thus increasing system bulk and leading to poor user acceptance.

This chapter presents a digital active electrode (DAE) system (Figure 6.1) for multi-parameter biopotential signal acquisition in portable and wearable devices. Each DAE is built around an ASIC that performs analog signal processing and digitization with the help of on-chip instrumentation amplifiers (IAs), a 12-bit ADC, and a digital interface. Via a standard 2-wire I^2C bus, up to 16 DAEs (15-channels) can be connected to a commercially available microcontroller, thus significantly reducing the system's complexity and cost. At the circuit level, each DAE utilizes an innovative "functionally" DC-coupled amplifier for extremely low frequency biopotential signal measurements while still achieving state-of-the-art performance. At the system level, a generic common-mode feedforward (CMFF) technique improves the CMRR of an AE pair from 40dB to maximum 102dB.

[5] This chapter is derived from a journal publication by the authors: J. Xu, B. Büsze, et al., "A 15-Channel Digital Active Electrode System for Multi-Parameter Biopotential Measurement," *IEEE J. Solid-State Circuits*, vol.50, no.9, pp. 2090-2100, Sept. 2015.

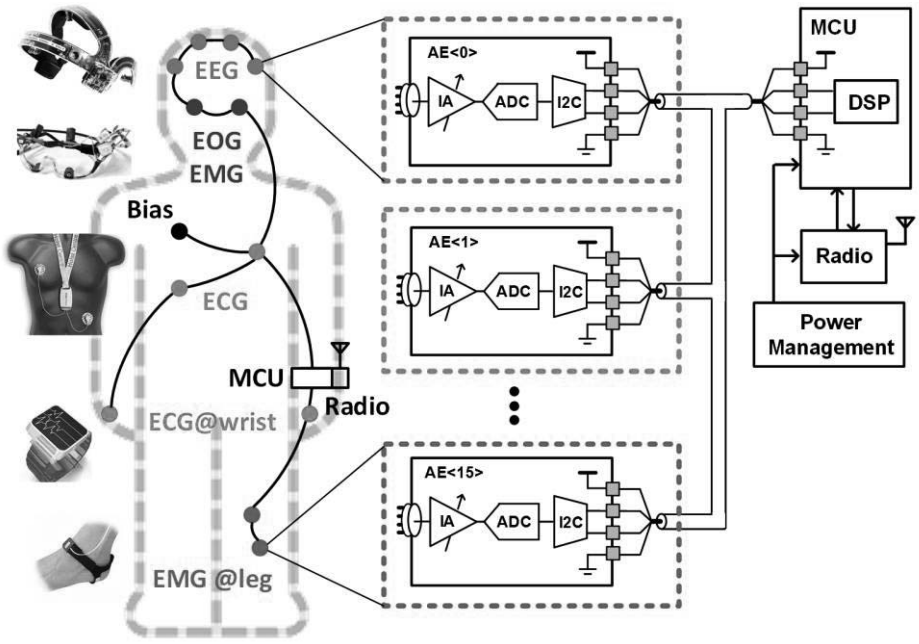

Figure 6.1 Wearable digital active electrode (DAE) system for multi-parameter physiological measurement.

6.2 IC Architecture Overview

The DAE chip (Figure 6.2) can simultaneously measure biopotential signals (in the ExG channel), real and imaginary ETI signals (in the IMP and IMQ channels), and DC and extremely low frequency biopotential signals (in the DC channel). The signal chain starts with a chopper IA configured for a voltage gain of 70, which improves the noise/power tradeoff of the following programmable gain amplifiers (PGA). The IA contains a ripple reduction loop (RRL) [124] and a DC-servo loop (DSL) [125] to attenuate chopper ripple and reject electrode offset, respectively. The IA's output is split into two channels for separate demodulation of the ETI and ExG signals.

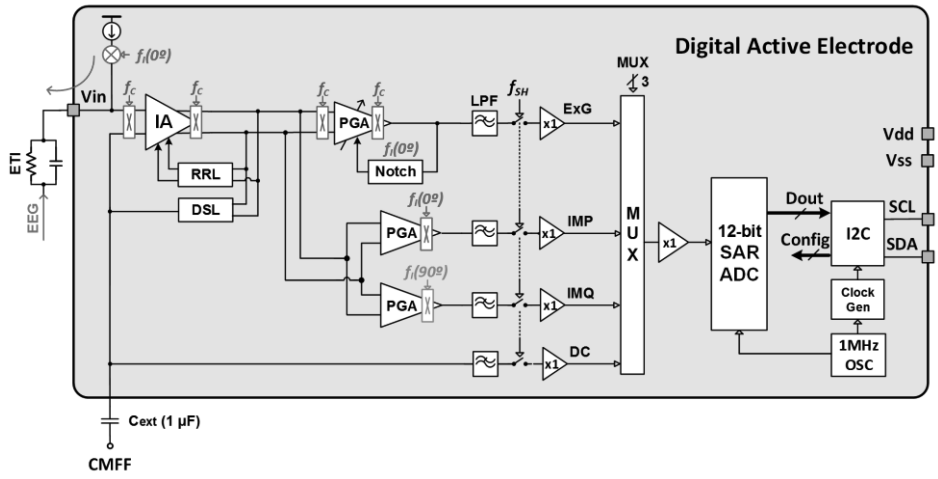

Figure 6.2 Architecture of a digital active electrode (DAE) chip.

The ETI channel is implemented in a similar manner as in the AE described in Chapter 4. Each ETI channel consists of two chopper PGAs that demodulate the ETI signals with in-phase f_I (0°) and quadrature-phase f_I (90°) clocks, with respect to a square-wave current injected into the electrode. The DC outputs of IMP and IMQ then represent the real and imaginary components of the ETI, respectively. Compared to the previous implementation, the new PGA of the ExG channel includes a notch filter to reject the ETI signals at f_I (0°). This prevents the PGA's saturation, resulting from the (large) ETI signals that may occur when dry electrodes are used. The detailed operation of the PGA is explained in section 6.3.2.

The DC channel acquires the DC and extreme low frequency signals present at the output of the DSL. In the frequency domain, the normalized gain and phase of the DC channel complements that of the ExG channel, making it possible to reconstruct DC-coupled ExG signals by combining the outputs of the ExG and DC channels [126][127].

These four measurement channels are simultaneously sampled by f_{SH} and connected to an 8-to-1 analog multiplier, through which a back-end microcontroller (µC) selects the channels of interest. A 12-bit SAR ADC [128] digitizes the outputs of these selected channels at 250Sps to 2kSps, and the digital outputs are transmitted to the back-end µC through an I²C interface.

6.3 Analog Signal Processing

6.3.1 A "Functionally" DC-Coupled Instrumentation Amplifier (IA)

IAs used in EEG application should tolerate at least ±300mV electrode offset. For an AE system, each AE should handle the same amount of offset with respective to the subject bias voltage. As discussed in Chapter 2, previous IAs suffered from the tradeoff between electrode offset, input impedance, noise, and power [130]-[132]. To tolerate a large electrode offset, the gain of a truly DC-coupled amplifier will be reduced by the need to avoid clipping [130]. Therefore, a high resolution ADC will be required to digitize the small (μV) biopotential signals superimposed on a much larger (mV) electrode offset, leading to high power dissipation on each channel. In contrast, AC-coupled amplifiers, implemented with passive coupling capacitors, enable low-power rail-to-rail offset rejection [125][131][132]. But this comes at the cost of filtering out the DC and low frequency signals. Capacitively-coupled chopper IAs mitigate 1/*f* noise by chopping the input signal before the coupling capacitor [133][134], but their input-impedance is limited by switched-capacitor resistance. AC-coupled IAs with voltage-to-current DC-servo loops solve this problem [126][135]. However, these IAs only compensate for a few tens of millivolts of electrode offset, limited either by noise considerations or by the maximum current provided from the feedback loop.

This section presents a "functionally" DC-coupled chopper IA architecture with a voltage-to-voltage feedback (Figure 6.3) to facilitate (large) electrode offset tolerance while still optimizing the IA's performance tradeoff. The core IA is implemented with a current feedback IA [135], chopped at 4kHz to reduce its flicker noise. This IA architecture provides high input impedance (100MΩ at 50Hz) and wide input CM range (0.5V-1.2V), making it robust to electrode impedance mismatch and DC polarization from dry electrodes. The DSL consists of a gm-C integrator that monitors the output offset and then cancels it by driving the core IA's inverting input. As a result, the IA can reject up to ±350mV of electrode offset, which is determined by the amplifier's input CM range and noise specification.

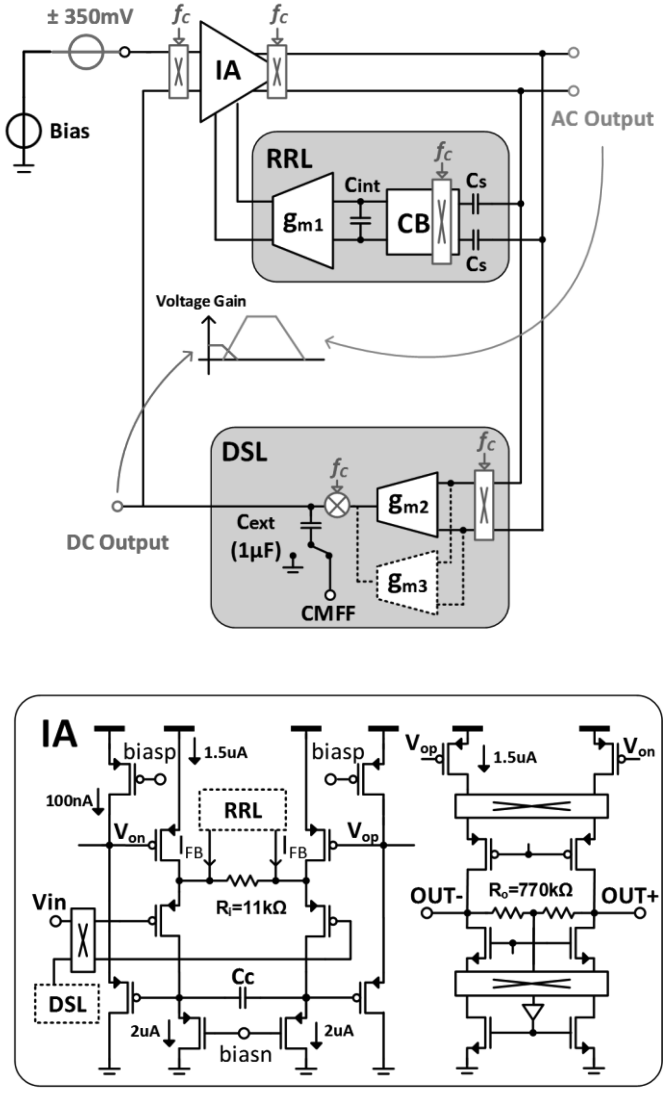

Figure 6.3 “Functionally” DC-coupled chopper IA and its core amplifier.

An interesting feature of this IA architecture, as well as of any IA equipped with a DSL configured in voltage-to-voltage feedback, is the preservation of the DC and low frequency information, which is available at the output of the DSL. The IA’s normalized AC and DC outputs have complementary

gain and phase characteristics, so these two outputs can be combined to implement a "functionally" DC-coupled IA. It has the same transfer function as a truly DC-coupled IA (Figure 6.4), but with a much wider DC dynamic range (±350mV) in conjunction with a high AC gain (>40dB). The wide DC dynamic range mitigates electrode offset from dry electrodes, while the high AC gain relaxes the required ADC resolution.

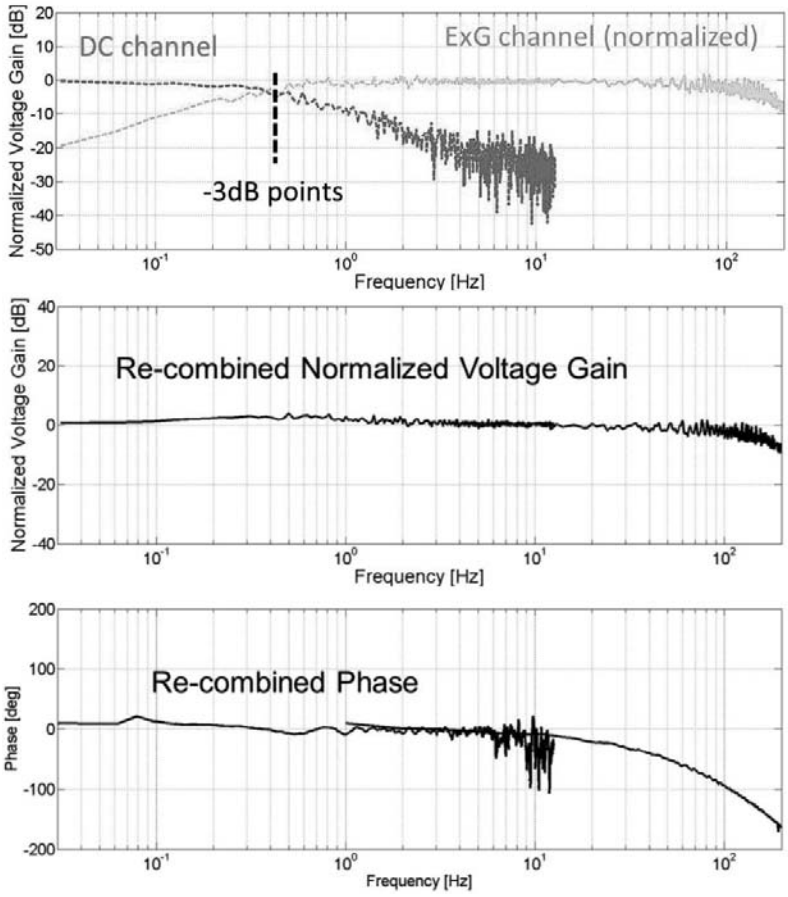

Figure 6.4 Measured normalized gain of ExG and DC channel (by dividing the respective channel gain measured at analog outputs), and the re-combined gain and phase.

The DSL utilizes a weak transconductance (g_{m2}=3μS) [136] and an external capacitor (C_{ext}=1μF) to achieve a low cutoff frequency (<0.5Hz). In addition, a large C_{ext} reduces the impedance at the input chopping node, reducing

the $1/f^2$ noise generated by the IA's input current noise [137]. To suppress the $1/f$ noise of the DSL and the RRL, both loops are chopped.

The thermal noise PSD of the core IA, the RRL and the DSL, respectively, is given by

$$\overline{V_{n,IA}^2} = \frac{\overline{V_{n,\text{core}IA}^2}}{\left(1+\frac{C_s g_{m1} R_o}{C_{\text{int}}}\right)^2} \tag{6-1}$$

$$\overline{V_{n,RRL}^2} = \left(\overline{V_{n,gm1}^2} + \frac{\overline{I_{n,CB}^2}}{s^2 C_{\text{int}}^2}\right) \cdot g_{m1}^2 R_i^2 \tag{6-2}$$

$$\overline{V_{n,DSL}^2} = \overline{V_{n,gm2}^2} \cdot \frac{g_{gm2}^2}{s^2 C_{ext}^2} \tag{6-3}$$

where $V_{n,coreIA}$, $V_{n,gm1}$ and $V_{n,gm2}$ are the input referred noise of the core IA, transconductance g_{m1} and g_{m2}, respectively, $I_{n,CB}$ is the input current noise of the current buffer, R_i and R_o are the input and output resistors that determine the gain of the core IA, and C_s is the RRL's input capacitance for voltage-to-current conversion. The total input referred noise of an AE is dominated by the core IA as shown in (6-1). Large integrator capacitors (C_{int}=150pF and C_{ext}=1μF) are selected to minimize the noise contribution of the core IA as well as of the RRL and the DSL.

At start-up, the circuit takes tens of seconds to settle due to the large time constant of the weak g_{m2} and the external C_{ext} (Figure 6.5). To overcome this issue, the AE includes a foreground fast-settling path, so that a stronger g_{m3}

(=100g_{m2}) in parallel can be temporarily switched on during the start-up, ensuring a settling time of less than 1 second.

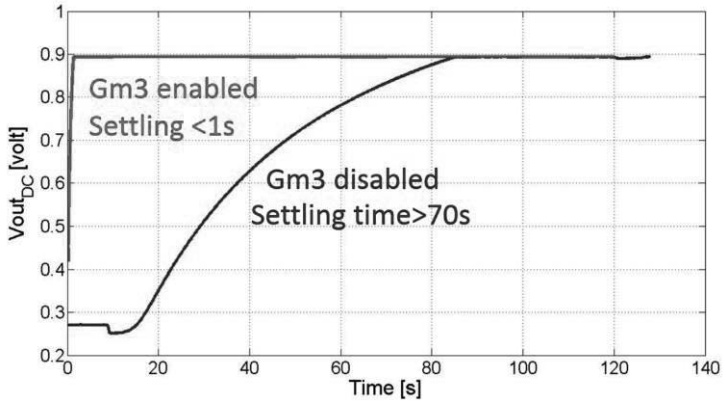

Figure 6.5 Measured settling time with and without g_{m3}.

6.3.2 Programmable Gain Amplifier (PGA)

In the ExG channel, the PGA (Figure 6.6) provides a programmable gain that facilitates both EEG and ECG applications. Chopper modulation is used to mitigate the low-frequency 1/*f* noise. A notch filter attenuates the ETI signal before it is filtered by the succeeding low-pass filter (LPF). The operating principle is similar to the RRL. Any in-phase ETI signal at the PGA's output is first converted to an AC current via C_s, which is then demodulated back to DC and integrated on capacitor C_{int}. Transconductor g_{m4} up-converts the DC voltage to an AC current and feeds it back to the PGA (Figure 6.7). This feedback current compensates for the ETI current flowing through R_i. On the other hand, the ExG signal at the PGA's output is up-modulated to 1kHz, and so is suppressed by C_{int}. The PGA can attenuate the output ETI signal by

$$A_{V,PGA@1kHz} = \frac{G_{PGA}}{\frac{R_{out,CB} \cdot g_{m4} \cdot R_{o,PGA}}{Z_{s@1kHz}} + 1} \approx \frac{Z_{s@1kHz}}{R_{out,CB} \cdot g_{m4} \cdot R_{i,PGA}} \tag{6-4}$$

where Z_s=C_s//$R_{in,CB}$, $R_{in,CB}$ and $R_{out,CB}$ are the input and output DC resistance of the current buffer (CB), respectively. $R_{i,PGA}$ and $R_{o,PGA}$ are the PGA's internal

feedback resistors. To maximize the attenuation, the PGA utilizes a cascode current buffer and a large input resistor ($R_{i,PGA}$=1MΩ). Figure 6.8 shows that the notch filter can reduce the output ETI signal (f_{ETI}=1kHz) by a factor of 40.

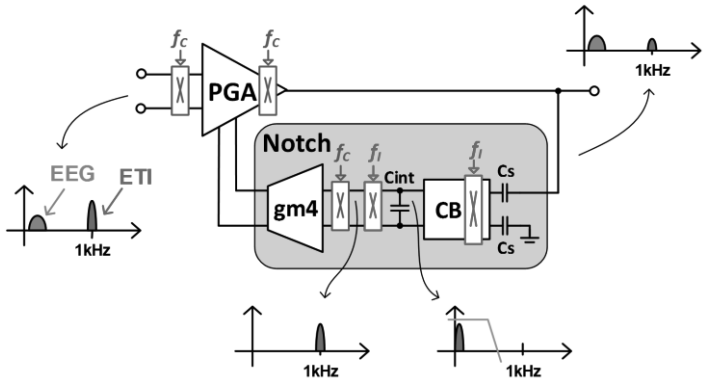

Figure 6.6 PGA with a notch filter for ETI signal rejection.

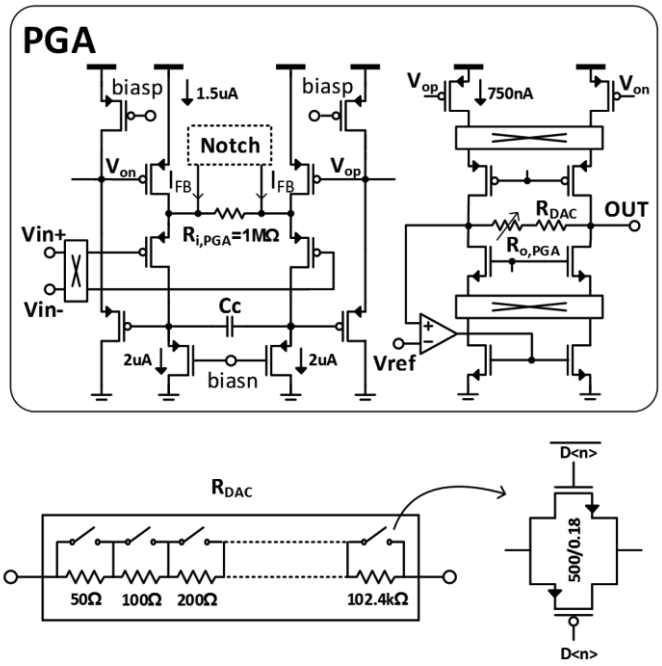

Figure 6.7 Core PGA with a programmable resistor load.

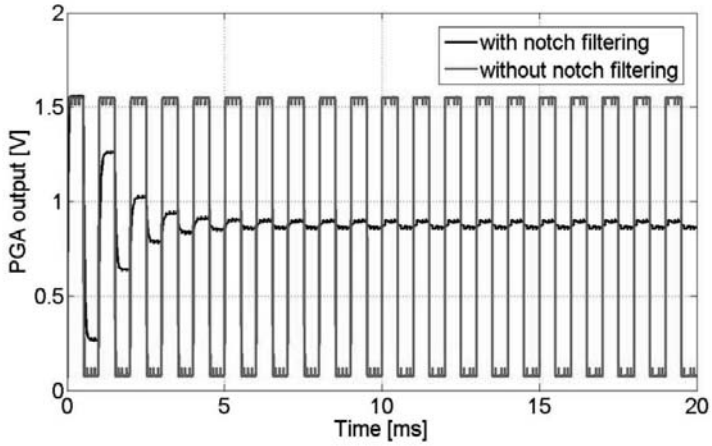

Figure 6.8 Simulated ETI signal at PGA's output (G_{PGA}=5, V_{ETI_input} = 280mV_{pp}@1kHz).

The core PGA utilizes the same IA architecture but with single-ended output. The coarse gain (2, 10 and 20) is selected via $R_{o,PGA}$, while R_{DAC} is implemented with a 12-bit programmable resistor array and can be trimmed with 50Ω resolution. To achieve this goal, very large CMOS switches (W/L=500/0.18) are used. R_{DAC} can be used to trim the channel gain of two DAEs, and so can improve the CMRR at the analog outputs by about 5dB. However, the CMRR improvement at the digital outputs is obscured by the 12-bit ADC's quantization [138]. Instead of trimming, a common mode feedforward (CMFF) technique can also improve the CMRR of two DAEs. This will be discussed in detail in section 6.5.

The IMP and IMQ channels also include PGAs for a wide range of the ETI measurements. The PGA does not have a notch filter and only contains an output chopper for ETI demodulation, because an ExG signal typically has a lower magnitude than an ETI input signal.

6.4 Digital Interfaces

The built-in digital interface is responsible for data transmission between the AEs and the digital back-end (DBE), as well as for clock signals generation of the AEs. An I²C interface is selected because it only requires two wires (SCL and SDA) for bi-directional communication (Figure 6.9), and it is compatible with many commercially available μCs. Although the equally popular SPI interface can operate at higher clock speeds (up to tens of MHz), it requires four

wires (MISO, MOSI, clock, and a separate chip selection to each IC), which would substantially increase the system's wiring bulk.

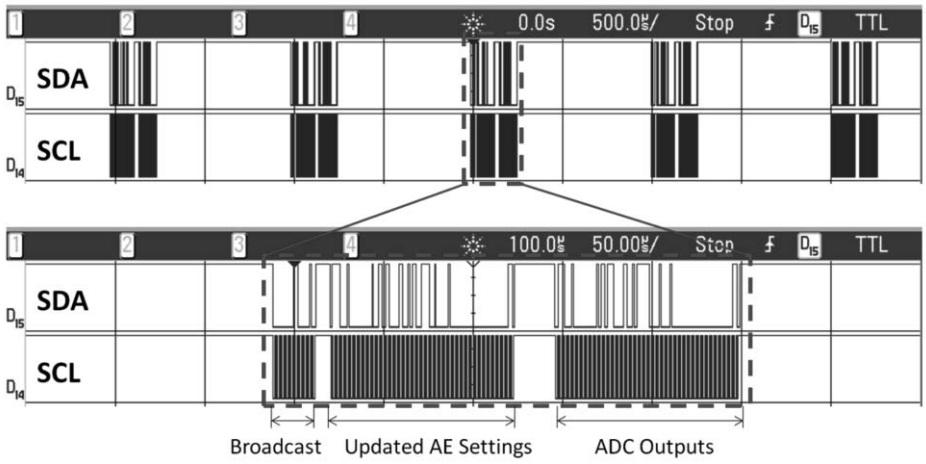

Figure 6.9 Data (SDA) and clock (SCL) signals of an AE's I²C bus.

Compared to a standard I²C interface, the proposed digital interface allows a global read and write to all DAE sensors. The global write configures and synchronizes DAEs at each I²C cycle. The global read enables DAEs to sequentially transfer the data back to the master node with only a single command. This avoids the need for the I²C master to address each DAE individually, thus reducing the control overhead and the amount of data toggling on the bus.

Each individual DAE chip can be given a 4-bit address via four external pins, allowing up to 16 DAEs to be connected to a single μC. In order to align the sampling moments of the individual DAE nodes, the back-end μC first sends a broadcast packet to all ICs (Figure 6.10). This broadcast packet (I²C address=0) is identified by each DAE chip independent of its base address on the I²C bus. The broadcast packets align the sample-and-hold (f_{SH}) and ADC sampling clocks of each DAE and also select two internal measurement channels of each IC (via MUX<1:0> in Figure 6.2), whose outputs will be sent to the μC in the next I²C cycle. In this way, the back-end μC has full control of the DAE and can flexibly select any channel of interest. The broadcast packet is followed by configuration settings from the μC, including various measure-

ment modes of the DAE. The digital outputs of each IC are then transmitted to the μC during the next I²C cycle.

The internal clocks of each DAE IC are derived from a 1MHz master clock, which is generated by a ring-oscillator on each AE. The clock generation module outputs configurable 1kHz to 32kHz clock, synchronized at each broadcast packet, for internal use by the chopper amplifier, ADC, ETI measurement, and digital logic. For flexibility, both internal clocks and DAE's sample rates are programmable. Although the 1MHz master clocks and the down-converted internal clocks (1kHz to 32kHz) of the DAEs suffer from frequency variations (~10%) due to the oscillators' PVT variations, the internal clocks for chopping and ETI measurements among different DAEs do not need to be synchronized. On the other hand, the sampling clocks of all DAEs are synchronized at every I²C interval (1ms in default) by the 5MHz I²C clock shared by all DAEs.

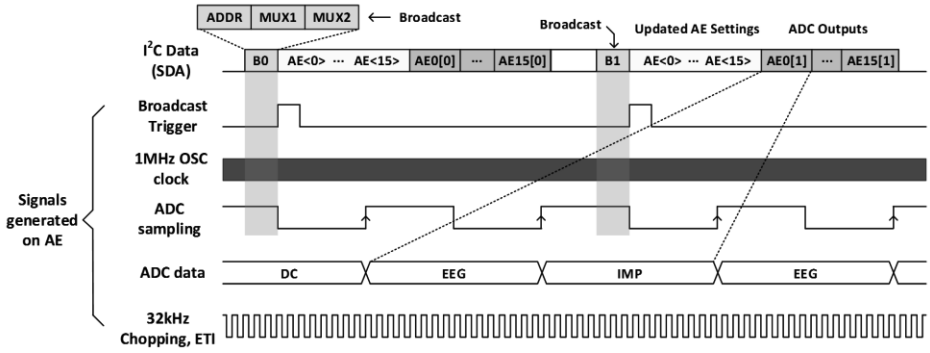

Figure 6.10 Timing diagram of the I²C interface and internal clocks.

6.5 CMRR Enhancement

There are two different AE mismatch mechanisms that limit the CMRR between a pair of AEs. The first is an electrode impedance mismatch, which is actually more of a problem with dry electrodes. In this case, the AE should maintain very large input impedance over the entire ExG bandwidth to mitigate any voltage division. The second is the AEs' gain mismatch. Compensating for these mismatches can significantly improve the CMRR and signal quality.

A further challenge of the DAE system is the need to achieve a wide CM input dynamic range for each AE. This is because each DAE can be modeled as a single-ended amplifier with a large gain (up to 1400), followed by a 12-bit ADC. As a result, any CM aggressor (e.g., mains interference, motion artifacts) that appear at the DAE's input can easily distort or saturate its readout circuits, even in the absence of any gain mismatch between the DAEs.

Previous designs have employed feedback techniques to improve CMRR and input CM dynamic range. The driven-right-leg (DRL) approach [139], for instance, has been widely used to compensate for CM interference by feeding the CM signal back to the subject through a bias electrode (or ground electrode). However, the resulting feedback loop may suffer from instability because the loop gain is not well defined, especially with the large and ill-defined electrode impedance associated with the use of dry electrodes. Common-mode feedback (CMFB) circuits can solve this problem by feeding the CM signal back to the amplifier's input, instead of the subject. However, an analog CMFB circuit [131] relies heavily on large passive components and results in poor flexibility and area-efficiency. Alternatively, a digitally-assisted CMFB scheme [138] extracts the CM signal of all DAEs in the digital domain, converts it back to an analog signal via a DAC, and then feeds it back to each DAE. However, the latency induced by the I^2C bus significantly shifts the phase of the analog CMFB signal relative to the input CM signal. This results in reduced phase margin and may destabilize the CMFB loop. To mitigate this stability problem, the bandwidth and gain of the CMFB loop has to be sacrificed [138]. Another major issue with all these "feedback-based" techniques is their instability during the electrode "lead off" condition. Since the common-mode extraction loop is broken, any electrode making poor electrical contact can cause the failure of the system [140].

The system utilizes a new and more generic CMFF technique to improve the CMRR of two AEs, providing advantages over a previous CMFB technique [138] in terms of higher CMRR bandwidth, better power-efficiency, and stability. Furthermore, this CMFF technique is generic and applicable to different types of AE architectures, such as inverting amplifiers or non-inverting amplifiers, whereas the CMFF technique proposed in [141] is only suitable for non-inverting amplifiers. The key idea of the new CMFF technique (Figure 6.11) is to apply an input CM signal to all the DAEs before pre-amplification. The input CM signal is applied to the inverting inputs of all IAs

via a buffer and their capacitively-coupled DSLs. Therefore, the input CM signal to a pair of AEs is compensated at their differential outputs, although their differential ExG amplification is not affected. This new CMFF technique has another major advantage: the buffered CM signal is applied to all DAEs through a very low impedance, which reduces the noise and interference pickup from the environment, similar to the noise reduction principle of an active electrode.

In the detailed implementation strategy (Figure 6.11), the input CM signal can be acquired from an additional electrode, or simply from the reference electrode, or from any one of the recording electrodes. This flexible selection is based on the fact that the DAEs' input CM signals picked up from the environment are quite similar. In extreme cases where the electrodes are placed far from each other, several local CMFF schemes can be used for different groups of DAEs.

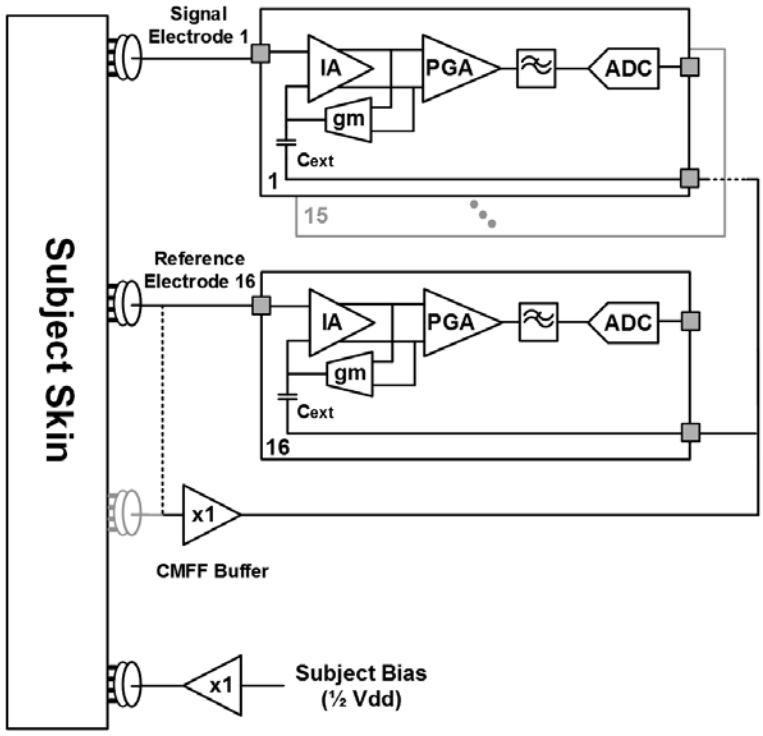

Figure 6.11 CMRR improvement through the use of a CMFF electrode.

Figure 6.12 illustrates the setup of CMRR measurement with various electrode impedance mismatch scenarios. Figure 6.13 to Figure 6.15 show the measured differential-mode gain and common-mode gain of a pair of DAEs, with different resistors R_e (0Ω, 50kΩ, and 800kΩ) to mimic different electrode types and their impedance mismatch [142]. The CMFF technique significantly boosts the CMRR of an AE pair from 40dB to 102dB (at 50Hz). When R_e increases, the CMFF is less effective due to the attenuation of the input CM signal and the larger gain mismatch between AEs.

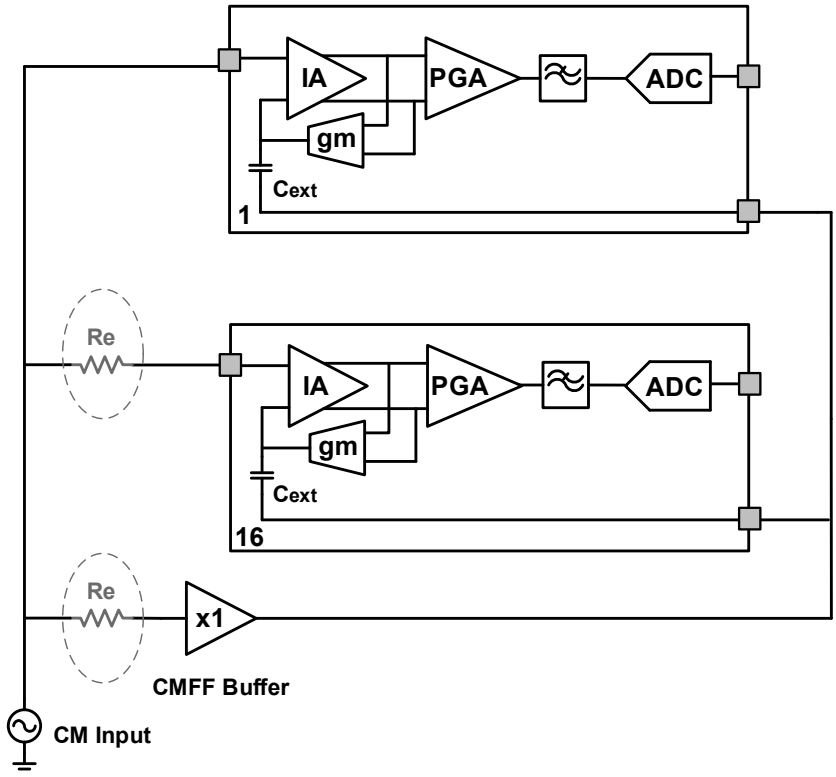

Figure 6.12 CMRR Measurement at various electrode impedance conditions.

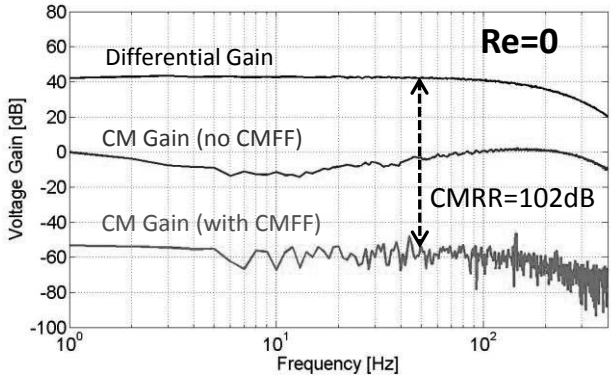

Figure 6.13 Measured DM gain and CM gain versus frequency (R_e=0).

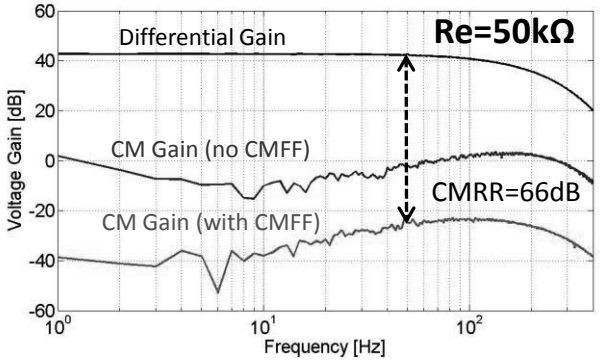

Figure 6.14 Measured DM gain and CM gain versus frequency (R_e=50kΩ).

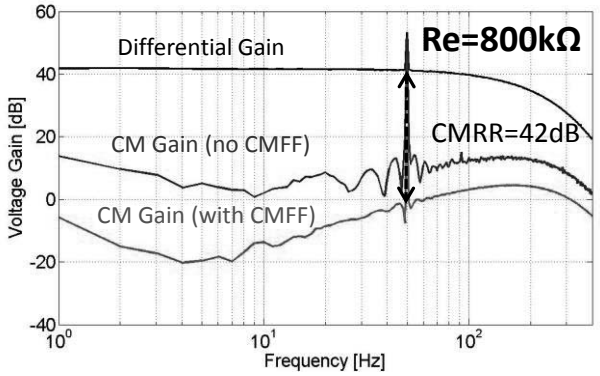

Figure 6.15 Measured DM gain and CM gain versus frequency (R_e=800kΩ).

6.6 Measurement

6.6.1 Measurement of Performance

The DAE was implemented in a standard 1P6M 0.18μm CMOS process and occupies an area of 15.8mm² (Figure 6.16). Each chip consumes 58μA from a 1.8V core supply, excluding the I²C interface.

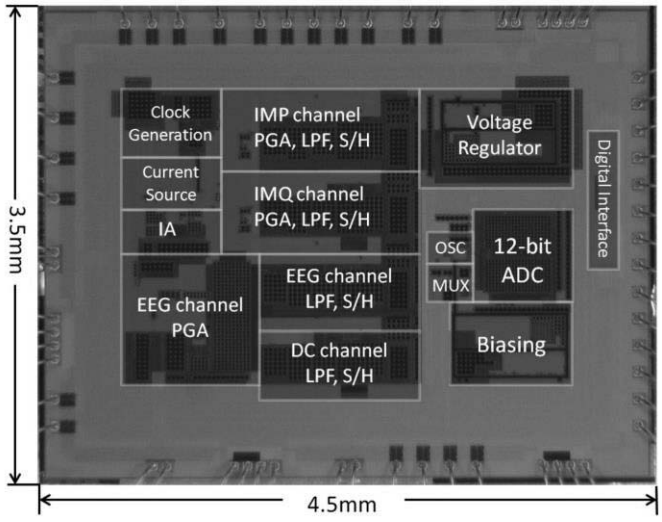

Figure 6.16 Chip photograph.

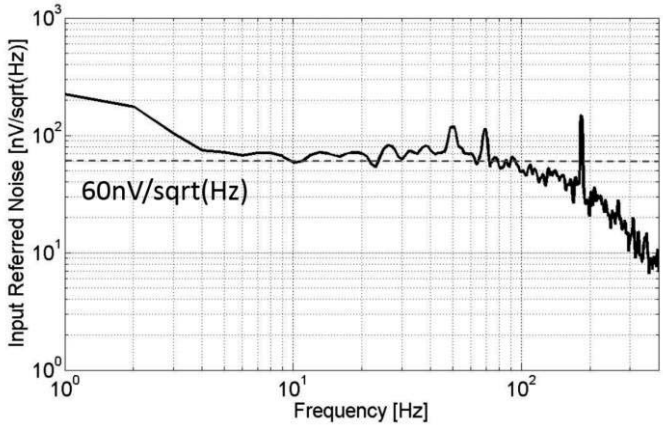

Figure 6.17 Measured input-referred noise per ExG channel (G=700).

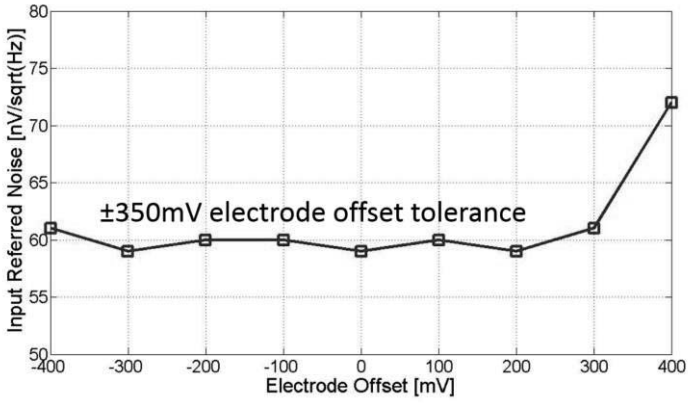

Figure 6.18 Measured input noise per ExG channel versus electrode offset.

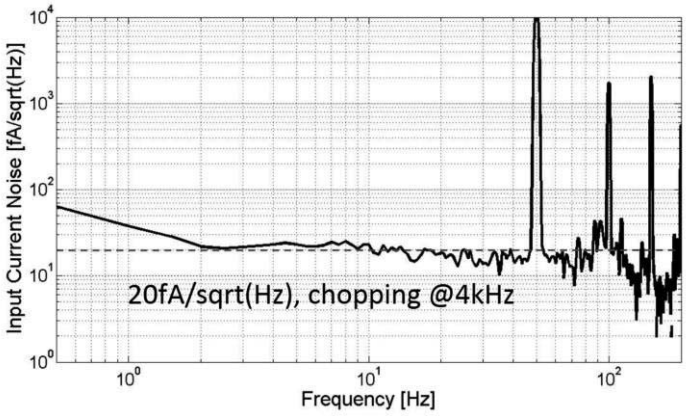

Figure 6.19 Measured input current noise of a digital AE.

Each ExG channel (consisting of two DAEs) shows a 60nV/sqrt(Hz) input-referred noise density (Figure 6.17), which stays constant over ±350mV electrode offset with respect to the subject bias (Figure 6.18). Each DAE has an input current noise density of 20fA/sqrt(Hz) at a chopping frequency of 4kHz (Figure 6.19), and an input impedance of 100MΩ at 50Hz (Figure 6.20). Each DAE can measure up to 400kΩ resistance (Figure 6.21) at 1kHz (at gain of 140) when measured by connecting multiple test resistors to the input of a DAE.

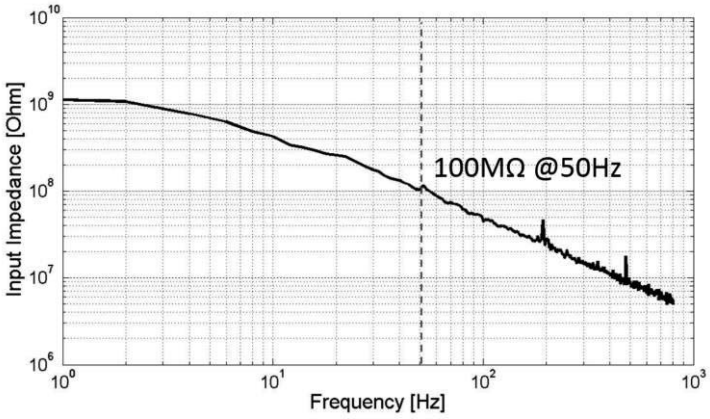

Figure 6.20 Measured input-impedance of a digital AE.

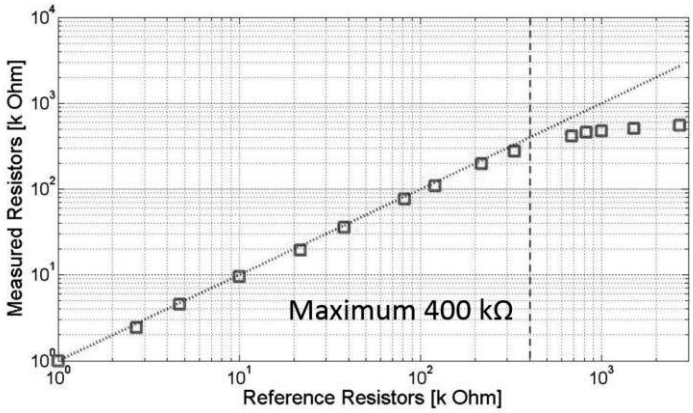

Figure 6.21 Measured resistor values versus reference resistor values, showing the dynamic range of ETI.

Table 6-1 summarizes the IC's performance. The analog performance is competitive to that of state-of-the-art biopotential IAs. The DC-coupled IA achieves a good balance between noise, electrode offset tolerance, and CMRR. Furthermore, the major merits of the proposed DAE system are the AE-based architecture for low interference, a built-in digital interface for high integration, and an inter-chip CMRR boosting technique. These features eliminate the need for an additional analog back-end (BE) circuit, leading to a cost-efficient solution for multi-channel ExG acquisition.

Table 6-1: Performance summary compared to the state-of-the-art EEG systems.

Parameters	[141]	[125]	[130]	This work
Supply Voltage	1.8V	1V	2.7-5.25V	1.8V
Active Electrode	Yes	No	No	Yes
DC-coupled IA	No	No	Yes	Yes
Input Referred Noise	1.75μV_{rms} (0.5-100Hz)	1.3μV_{rms} (0.5-100Hz)	0.7μV_{rms} (DC-131Hz)	0.65μV_{rms} (0.5-100Hz)
Input Impedance	1.2GΩ @20Hz	0.7GΩ (DC)	1GΩ (DC)	1GΩ@1Hz , 300MΩ@20Hz
Electrode Offset Tolerance	±250mV	Rail-to-Rail	±250mV	±350mV
CMRR	84dB	60dB	115dB	102dB
Impedance Measurement	Yes	No	Yes	Yes
ADC	12-bit SAR	12-bit SAR	24-bit SDM	12-bit SAR
Number of Channels	8	18	8	15
Dry Electrode Applications	Yes	No	No	Yes
Current (per channel)	48μA	> 3.5μA	250μA	58μA

6.6.2 Multi-Parameter ExG Measurement

Simultaneous single-channel ECG, EMG, and EOG measurements are performed to demonstrate the DAEs' capability of multi-parameter acquisition. Five (wet) electrodes are attached to a subject's chest and forehead (Figure 6.1) and connected to DAE test boards via cables. These five electrodes include one bias electrode, two electrodes for ECG recording and two electrodes for EMG and EOG recording. For simplicity, the CMFF buffer's input is connected to the reference electrodes in all measurements. Figure 6.22 shows several types of physiological behaviors acquired by the DAE system, such as heartbeat (ECG), face muscle movement (EMG), and eyes blinking (EOG).

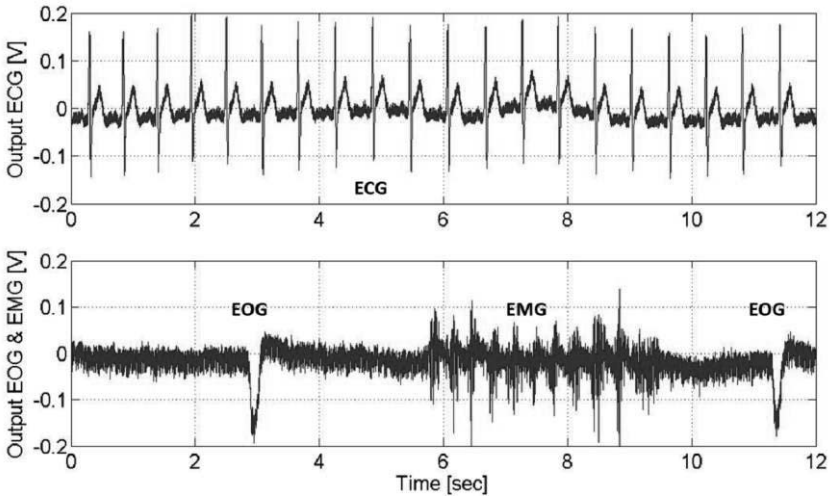

Figure 6.22 Simultaneous ExG recordings of the DAE system.

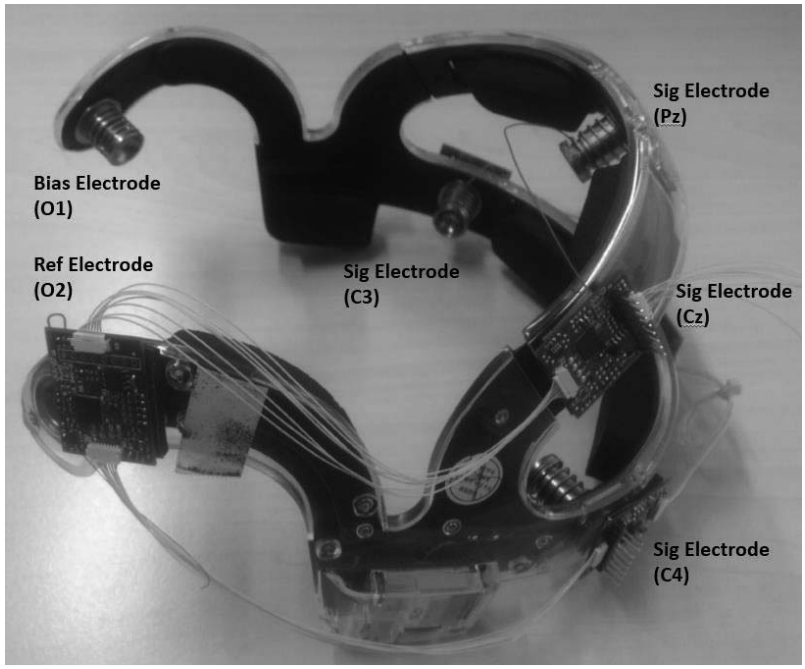

Figure 6.23 4-channel EEG headset with DAE test boards attached.

In order to measure EEG on the scalp, five DAE test boards (each board contains a DAE ASIC, level shifters, analog test buffers, and jumpers for I^2C address) are connected in a daisy chain and attached to an EEG headset (Figure 6.23). The bias electrodes, reference electrodes, and (signal) recording electrodes are placed at O_1, O_2, Cz, Pz, C_3, and C_4, respectively, based on a standard 10-20 electrodes EEG system. Figure 6.24 shows that alpha activity at approximately 12Hz clearly allows distinguishing between periods of "eyes open" and "eyes closed" when dry electrodes are used.

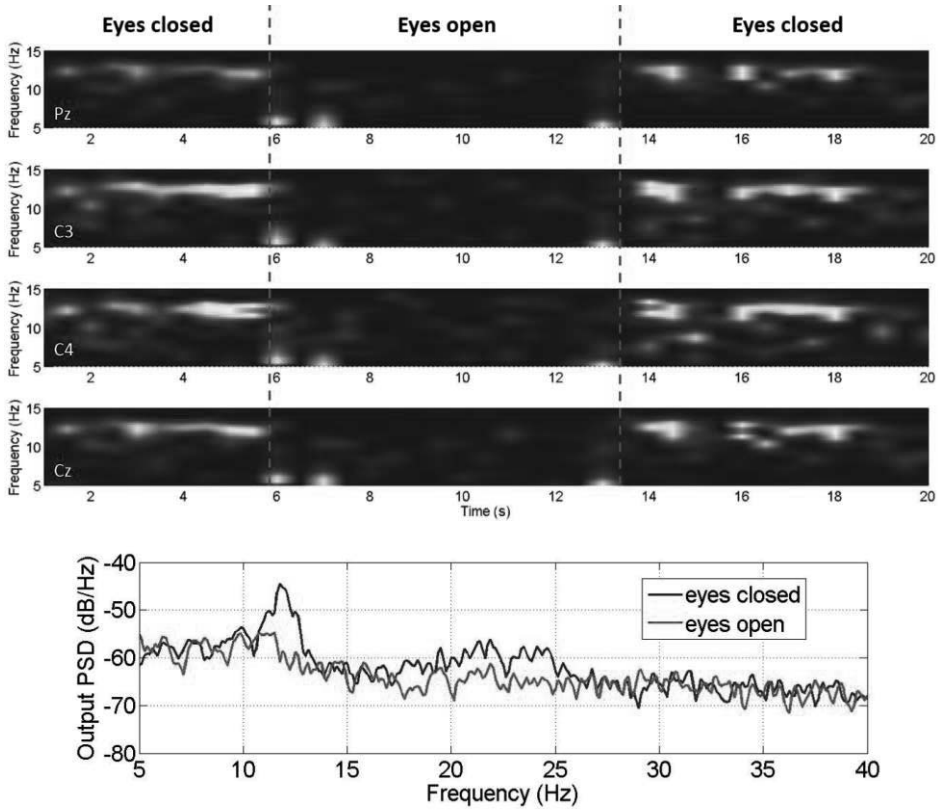

Figure 6.24 4-channel EEG recording with dry electrodes during periods of eyes closed and eyes open.

Figure 6.25 shows a 1-lead ECG measured on the subject's wrists, demonstrating the benefit of the CMFF: after enabling the CMFF scheme, the 50Hz interference, picked up from the same environment, is significantly reduced.

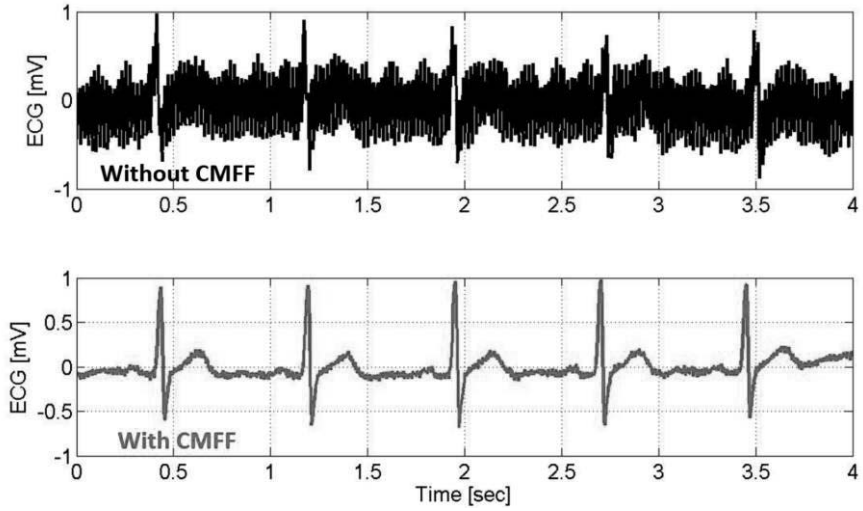

Figure 6.25 1-lead ECG recording with wet electrodes placed on wrists.

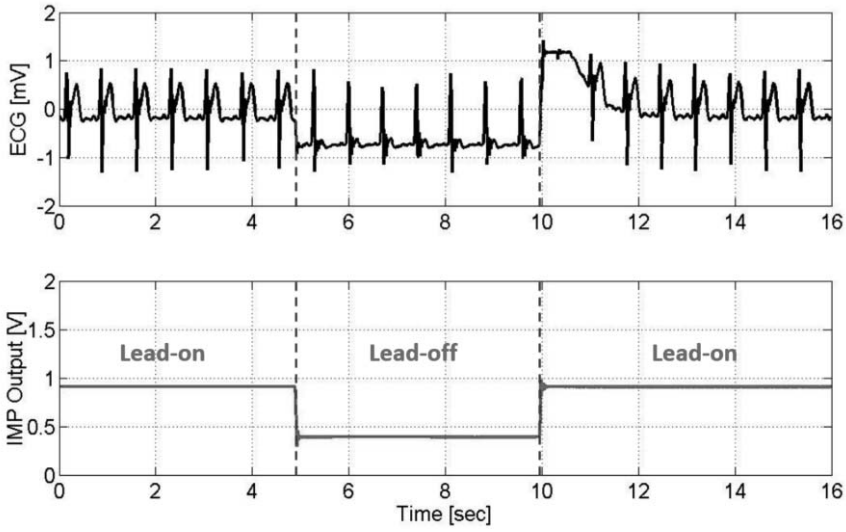

Figure 6.26 Lead-off and lead-on detection by monitoring the ETI output.

Figure 6.26 shows a simultaneous recording of the ECG and ETI (on the chest). When one electrode is disconnected from the subject, the ECG output shows incorrect results and the ETI output saturates. After re-connecting the electrode, both the ECG and ETI recover. This indicates that the ETI output can also be used for instant lead-on and lead-off detection.

6.7 Conclusion

A digital active electrode (DAE) incorporates amplifiers, an ADC, and a digital interface on a single chip. A "functionally" DC-coupled IA optimizes performance tradeoffs (between noise, electrode offset tolerance, input impedance, and power) and enables the practical use of dry electrodes. A generic CMFF technique ensures a maximum 102dB CMRR of two DAEs at 50Hz. The highly integrated DAE chip eliminates the needs for a back-end analog signal processor and facilitates multi-channel multi-parameter biopotential signal acquisition. These features significantly reduce the DAE system's complexity and cost and enable a highly modular ExG acquisition system.

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CHAPTER 7

CONCLUSIONS

7.1 Introduction

In the previous chapters, the design and implementation of different types of AEs have been described. In this chapter, conclusions will be drawn based on the experimental results obtained with these AE-based ASICs. In addition, suggestions for future work are presented.

7.2 Summary

The prototype ASICs described in Chapter 3, Chapter 4, and Chapter 6 demonstrate that active electrodes (AEs) can be successfully used for wearable EEG acquisition. The highly integrated and ultra-low-power AEs are compatible with dry electrodes, thus facilitating different form factors for wearable devices. From a user point of view, these user-friendly features are their principal advantages over conventional wet-electrode-based, bulky, and power hungry EEG instruments.

Apart from the improved user comfort, the proposed AE systems also achieve state-of-the-art performance through the use of advances in IC techniques. Various ultra-low-power IC design techniques have been implemented and verified in different types of AEs, whose analog performance are compared in Table 7-1. The combination of chopping and capacitive feedback IA architecture helps the AE achieve low noise amplification and rail-to-rail electrode offset rejection (Chapter 3). An AE's input impedance can be further improved through the use of an impedance boosting loop (Chapter 3) or a non-inverting IA topology (Chapter 4). To compensate for the AEs' mismatch, either a CMFB technique (Chapter 3 and Chapter 6) or a CMFF technique (Chapter 4 and Chapter 6) were implemented, improving the CMRR by at least 25dB. The non-idealities of a chopper IA, such as intrinsic offset and chopper ripple, can be reduced by digitally-assisted calibration techniques (Chapter 3) or by a

continuous-time ripple reduction loop (RRL) (Chapter 4 and Chapter 6). Furthermore, the AE systems described also introduce the electrode-tissue impedance (ETI) measurement (Chapter 4 and Chapter 6) and a "functionally" DC-coupled IA (Chapter 6), both of which aim to provide additional information of the brain-electrode interface beyond EEG recording. In general, the DAE presented in Chapter 6 achieves the best overall performance while also including the most features. Compared to this, state-of-the-art AE implementations either consume significant power [143][144], which requires mains power supplies, or have less analog performance, power efficiency or functionalities [145][146].

Table 7-1: Performance summary of the AE systems presented in Chapter 3, Chapter 4, and Chapter 6.

	Chapter 3	Chapter 4	Chapter 6
Technology / Supply	0.18µm / 1.8V	0.18µm / 1.8V	0.18µm / 1.8V
AE Gain	3, 10, 100	11, 51, 101	140, 700, 1200
Input Referred Noise (per channel)	$1.2\mu V_{rms}$ (0.5-100Hz)	$1.75\mu V_{rms}$ (0.5-100Hz)	$0.65\mu V_{rms}$ (0.5-100Hz)
Electrode Offset Rejection	Rail-to-rail	±250mV	±300mV
Input Impedance (DC) at 50Hz	2GΩ 120MΩ	1.2GΩ 400MΩ	1GΩ 100MΩ
CMRR	82dB (via CMFB)	84dB (via CMFF)	102dB (via CMFF)
Power Consumption (per channel)	20µW + g.tec (N/A)	82µW	105µW (excl. digital)
Integrated ADC	N/A	12-bit SAR	12-bit SAR
Ripple Reduction	Foreground	Background	Background
ETI Measurement	No	Yes	Yes
DC-coupling	AC-coupling	AC-coupling	"Functionally" DC-coupling
Integrated Digital Interface	No	No	I²C

In spite of these advantages, AE systems still have some drawbacks or limitations. For example, each EEG recording channel consists of two AEs, in-

herently resulting in a lower noise-power efficiency than conventional differential EEG amplifiers. Furthermore, chopping at a high impedance node may also generate significant $1/f^2$ noise because of the current noise of the chopper switches. Although general design guidelines have been discussed to mitigate this effect (Chapter 5), the $1/f^2$ noise was not completely eliminated. Lastly, although a DC-servo loop using voltage-to-voltage feedback (Chapter 6) represents an excellent balance between noise, input impedance, and electrode offset rejection, it requires the use of a large off-chip capacitor and is not suitable for low supply voltages (< 0.6V).

7.3 Future Work

In general, there are three major research objectives for the future development of wearable EEG ICs and systems: better suppression of motion artifacts, improved robustness and safety, and multimodal acquisition.

Dealing with motion artifacts is the one remaining challenge for improving signal quality. The dynamic range of an EEG readout circuit is typically limited to a few mV because of the IA's gain constraints. As a result, the IA can saturate during the presence of large motion artifacts, especially when the subject is moving. This can be a severe problem for wearable devices extensively used in lifestyle and wellness applications. One straightforward solution is to reduce the IA's gain; however, a high-resolution ADC (>=16 bit) with low power consumption would be needed. Another possible solution is to apply a motion artifact reduction (MAR) technique [143]. With this technique, the motion artifact signal can be partially extracted from electrode-tissue impedance (ETI) measurements and can be used to compensate the input motion artifact. However, the accuracy of the MAR not only depends on a high-quality ETI measurement, but also on digital signal processing to ensure that the original EEG signal is not polluted through the MAR.

Improving the robustness and safety of the existing wearable EEG systems in special medical environments is another interesting objective. One example of this is the use of an EEG headset during functional magnetic resonance imaging (fMRI). This simultaneous EEG-fMRI recording is a multimodal neuroimaging technique, which enables the measurements of both neuronal and hemodynamic activities. However, the fMRI environment can lead to particular problems for EEG acquisition. For instance, large currents induced by

the fMRI acquisition process may flow into and thus saturate the EEG readout devices.

Emerging EEG systems should also provide additional physiological modalities for improved diagnostic accuracy; for instance, measuring the blood oxygenation response through an optical sensor or estimating the fluid status and body composition through a bio-impedance measurement. This measurement can be combined with EEG recordings to examine the brain's functional activities more comprehensively [148]. Recently, multi-parameter biopotential signal acquisition systems [149][150] containing multiple types of sensors have been presented. These systems can be easily attached to people's heads, arms, chests or wrists for simultaneous measurement, from which various biopotential signals (ECG, ETI, bio-impedance or fNIRS) are recorded and wirelessly transmitted to medical professionals through a body area network (BAN).

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SAMENVATTING

Deze thesis beschrijft de toepassing, theorie, en implementatie van actieve elektrodes (AEs) voor EEG acquisitiesystemen. Deze systemen vereisen een lage ruis, een hoge ingangsimpedantie, een hoge tolerantie tegen electrode offset, een hoge CMRR en een laag vermogen. AEs verbeteren de robuustheid tegen omgevingsinterferentie en onderdrukken storingen door bewegingen van de kabel, en maken het hierdoor mogelijk om hoge-impedantie droge elektrodes te gebruiken. Droge elektrodes, op hun beurt, faciliteren langdurige EEG metingen met meer gebruikerscomfort. Verschillende generaties van AE-gebaseerde ASICs zijn geïmplementeerd met diverse architecturen en circuit ontwerptechnieken.

Hoofdstuk 1 introduceert de algemene basiskennis van EEG metingen op de hoofdhuid, de ontwikkelingsgeschiedenis, en de noodzaak voor persoonlijke EEG systemen. Het wordt aangetoond dat AEs een veelbelovende oplossing bieden voor EEG metingen met droge elektrodes, en de geassocieerde ontwerpuitdagingen worden samengevat.

Hoofdstuk 2 presenteert een overzicht van de nieuwste instrumentatieversterkers (IAs) en AEs voor draagbare gezondheidszorg. Verschillende architecturen en ontwerptechnieken worden gepresenteerd, welke als doel hebben om de belangrijkste specificaties, zoals ruisniveau, ingangsimpedantie, elektrode offset, CMRR en vermogensverbruik, te optimaliseren.

Hoofdstuk 3 presenteert een AE uitleescircuit gebaseerd op een AC-gekoppelde chopper versterker, die inherent elektrode offset blokkeert. Het gebruik van chopping onderdrukt 1/*f* ruis, resulterende in een ingangsruis van 0.8μVrms (0.5-100Hz). Een impedantieverhogingstechniek verhoogt de ingangsimpedantie met een factor 5 (bij 1Hz), terwijl digitaal-geassisteerde offsetcorrectie de overgebleven rimpelingen en offset met respectievelijk 20x en 14x vermindert. Verschillen tussen de AEs vormen de belangrijkste reden voor een lage CMRR. Een back-end common-mode feedback (CMFB) circuit verhelpt dit en verbetert de CMRR van een paar AEs met 30dB.

Hoofdstuk 4 presenteert een compleet 8-kanaals AE systeem voor het continue monitoren van EEG en elektrode-weefsel impedantie (ETI). De ETI metingen

breiden de functionaliteit zodanig uit dat de elektrodestatus op afstand bepaald kan worden. Het gehele AE systeem bestaat uit negen AEs en een back-end (BE) analoge signaal processor (ASP). De AE is gebaseerd op een niet-inverterende chopper versterker, welke EEG signalen versterkt met een goede balans tussen ingangsimpedantie en ruisniveau. De ASP bewerkt de analoge signalen van de AE na en digitaliseert deze. Een common-mode feedback (CMFB) techniek op systeemniveau verbetert de CMRR van een AE paar met 25dB.

Hoofdstuk 5 onderzoekt de oorzaak van $1/f^2$ ruis in chopper versterkers door theoretische analyse en metingen aan diverse chopper IAs. We veronderstellen dat ladingsinjectie en klokoverspraak van de MOSFETS in de chopper resulteren in ingangsstroom en dus stroom-gerelateerde ruis. In combinatie met een hoge ingangsimpedantie wordt deze ruisstroom naar een spanning geconverteerd, welke significant kan zijn (in de vorm van $1/f^2$ ruis) voor de totale ingangsruisspanning van de versterker. Bovendien heeft deze chopper ruis een witte spectrale vermogensdichtheid wiens amplitude ongeveer proportioneel is met de chopping frequentie. Ontwerprichtlijnen worden voorgesteld om de chopper ruis te reduceren. Een ander voorstel is om bootstrapping voor de chopper-klok toe te passen, wat minder ruis geeft dan een traditionele chopper.

Hoofdstuk 6 presenteert een digitaal AE (DAE) systeem voor multi-parameter bio potentiaal signaalacquisitie. Het systeem is opgebouwd rond een ASIC welke analoge signaalbewerking en digitalisering uitvoert met behulp van geintegreerde instrumentatieversterkers (IAs), een 12-bit ADC, en een digitale interface. Via een standaard I^2C bus kunnen tot 16 DAEs (15 kanalen) aangesloten worden op een microcontroller. Dit reduceert de complexiteit van de verbindingen in het systeem substantieel. Op circuitniveau gebruikt de DAE een "functioneel" DC-gekoppelde versterker om zeer laagfrequente biopotentiaal signalen aan te kunnen en tegelijkertijd tolerantie te bieden tegen grote elektrode offsets. Op systeemniveau verbetert een generieke common-mode feedforward (CMFF) techniek de CMRR van een AE paar van 40dB tot een maximum van 102dB.

Hoofdstuk 7 concludeert deze thesis door de algehele prestaties van de AEs uit de hoofdstukken 3, 4 en 6 te vergelijken en voordelen en beperkingen ten opzichte van conventionele EEG acquisitie ICs toe te lichten. Twee onderzoeksrichtingen voor toekomstig werk worden voorgesteld, namelijk: verbeterde robuustheid en veiligheid en multimodale acquisitie.

SUMMARY

This thesis describes the application, theory, and implementation of active electrodes (AEs) for EEG acquisition systems that require low noise, high input impedance, high electrode offset tolerance, high CMRR, and low power. The main motivation for using AEs is to enable the use of high-impedance dry electrodes by increasing their robustness to environmental interference and cable motion. In turn, dry electrodes facilitate long-term EEG measurements with greater user comfort. Several generations of AE-based ASICs were implemented with different architectures and circuit design techniques.

Chapter 1 introduces the basics of scalp EEG measurement, the history of its development, and the need for personal EEG devices. AEs are shown to be a promising solution for dry-electrode-based EEG measurement, and the associated design challenges are summarized.

Chapter 2 presents an overview of state-of-the-art instrumentation amplifiers (IAs) and AEs for wearable healthcare. Different architectures and design techniques are presented, which aim to optimize key specifications such as noise level, input impedance, electrode offset, CMRR, and power dissipation.

Chapter 3 presents an AE readout circuit that is based on an AC-coupled chopper amplifier, which naturally blocks electrode offset. The use of chopping mitigates 1/*f* noise, resulting in an input-referred noise of 0.8μV_{rms} (0.5-100Hz). An impedance-boosting technique increases its input impedance by 5x (at 1 Hz), while digitally-assisted offset trimming reduces residual ripple and offset by 20x and 14x, respectively. Mismatch between the AEs is the main cause of low CMRR. To mitigate this, a back-end common-mode feedback (CMFB) circuit improves the CMRR of a pair of AEs by 30dB.

Chapter 4 presents a complete 8-channel AE system for continuous monitoring of EEGs and electrode-tissue impedance (ETI). ETI measurement extends its functionality by enabling remote assessment of electrode status. The whole AE system consists of nine AEs and one back-end (BE) analog signal processor

(ASP). The AE is based on a non-inverting chopper amplifier, which boosts EEG signals with a good tradeoff between input impedance and noise level. The BE circuit post-processes and digitizes the AEs' analog outputs. At the system level, a common-mode feed-feedback (CMFB) technique improves the CMRR of an AE pair by 25dB.

Chapter 5 investigates the root cause of $1/f^2$ noise of chopper amplifiers through a theoretical analysis and measurements of several chopper IAs. We hypothesize that the charge injection and clock feed-through associated with the MOSFETs of the input chopper give rise to significant input current and current noise. In combination with high source impedances, this "chopper noise" is converted to voltage noise, which may then be a significant contributor (i.e., $1/f^2$ noise) to the IA's total input-referred voltage noise. Furthermore, the chopper noise has a white power spectral density, whose magnitude is roughly proportional to the chopping frequency. Design guidelines are then proposed to reduce the chopper noise. A further proposal is the use of a clock-bootstrapped chopper, which exhibits less noise than a traditional chopper.

Chapter 6 presents a digital active electrode (DAE) system for multi-parameter biopotential signal acquisition. It is built around an ASIC that performs analog signal processing and digitization with the help of on-chip instrumentation amplifiers, a 12-bit ADC, and a digital interface. Via a standard I^2C bus, up to 16 DAEs (15-channels) can be connected to a microcontroller, thus significantly reducing the system's connection complexity. At the circuit level, a DAE uses a "functionally" DC-coupled amplifier to handle extremely low-frequency biopotential signals while still tolerating high-levels of electrode offset. At the system level, a more generic common-mode feedforward (CMFF) technique improves the CMRR of an AE pair from 40dB to the maximum of 102dB.

Chapter 7 concludes the thesis by comparing the overall performance of the AEs presented in Chapter 3, Chapter 4, and Chapter 6, illustrating both their advantages and limitations with respect to conventional EEG acquisition ICs. Two research tracks, namely improved robustness and safety, as well as multimodal acquisition, are proposed for future work.

ACKNOWLEDGEMENTS

Undertaking this Ph.D. during the past six years has been a truly challenging experience for me. It has been a rocky road but definitely not a lonely journey, Thanks to the support and guidance of many people.

First I want to thank my promoter Prof. Kofi. A.A. Makinwa. It has been my good fortune and pride to have worked with him. I appreciate all his contributions of time, ideas, and even criticism to make my Ph.D. journey so productive and stimulating. His enthusiasm and enjoyment of research motivated me a lot.

I would like to say a very big thank you to my daily supervisor and former group leader: Dr. Firat Refet Yazicioglu, who convinced me to start my Ph.D. on this interesting and challenging topic. His consistent guidance and encouragement helped me to grow, not only as an IC designer, but also as an independent thinker.

My sincere thanks also goes to Prof. Chris Van Hoof for the funding and resources that made my Ph.D. work very well supported. As the department head, Chris has a brilliant vision on the R&D of biomedical devices, which has significantly increased the impact of my Ph.D. research in imec, as well as in the broad scientific community.

A very special thank you to Dr. Pieter Harpe for his amazing enthusiasm, patience, and willingness to discuss questions and help me, and most importantly, for our friendship for so many years.

It has been my great honor to acknowledge Prof. J.H. Huijsing for all our discussion and brainstorms on active electrodes and amplifiers. I am so impressed for the excellent examples he has provided as a great researcher and professor.

The members of Wearable Health Solution (WHS) group have contributed immensely to my personal and professional time at Holst Centre in the past 10 years. The group has been a source of friendships as well as good collaboration. Thanks Nick, for being an excellent technical lead on IC development. Thanks Srinjoy, Shrishail, Bernard, Vojkan for their support on EEG system's design, integration and evaluation. Thanks Ben, Hyejung for implementing the digital interfaces. Thanks Budi, Chris, Richard, Roland, Hyunsoo, Stefano, Samira, Shuang and Mario for all the technical reviews and discussions in the MUSEIC

project. Thanks to the former group members Mukul, Serena, Julia, Yifeng that I have had the pleasure to work with as an officemate. Thanks to my former managers Guy, Patrick, and the current manager Rik for the flexible research environment they have created for us. Thanks to Eugenio, Guus for the discussions on patent applications. Thanks to Li, Xiaoyan, Bo, Cui, Yao-Hong and Peng for their friendship and most of all, their humor.

My time at TU Delft was less than at Holst but also enjoyable, to a large extent due to many friendly colleagues. I am very grateful to our group secretary Joyce who kept us organized and was always ready to help. Thanks to Michiel, Qinwen, Saleh, Kamran, Fabio, Ugur, Junfeng, Caspar for the design reviews and conference rehearsals. Thanks to Zu-Yao, Lukasz for organizing the hands-on EEG demos.

For this dissertation I would like to thank my committee members for their time, interest, and helpful comments. I especially would like to thank Peter for proofreading my thesis during his holidays.

Lastly, I would like to thank my parents for always believing in me and supporting me to follow my dreams. And most of all for Liangliang who has been by my side with great patience, understanding, and encouragement.

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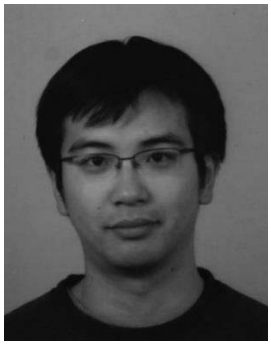

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