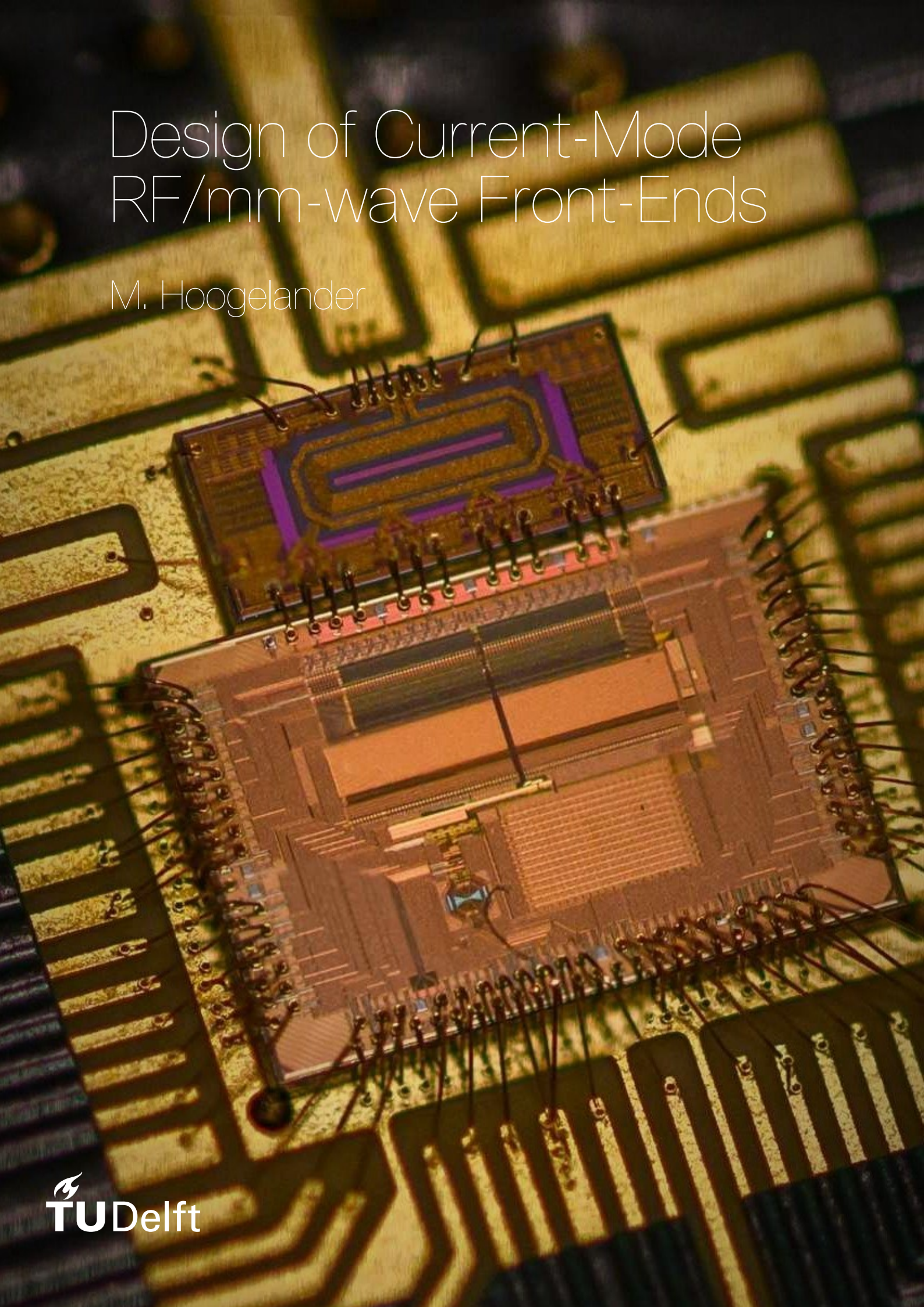
Design of Current-Mode RF/mm-wave Front-Ends

M. Hoogelander



TU Delft

Design of Current-Mode RF/mm-wave Front-Ends

by

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Abstract

This thesis investigates the performance limits and design challenges of two current-mode front-end concepts that target WiFi and mm-wave 5G applications, respectively. The first concept is a power amplifier (PA), which operates at 2.4 GHz and is driven by a direct-digital RF modulator (DDRM). A design for the PA, which also includes a parallel-combining transformer (PCT), was proposed, taped and tested in the QUBiC Gen8 technology of NXP Semiconductors. The measured results yield a peak output power of 27 dBm, power efficiency of 20 %, and an adjacent channel power ratio (ACPR) of −33.05 dB c. In the other concept, the DDRM drives a power mixer (PMIX) which up-converts the DDRM signal to mm-wave frequencies. For the PMIX-based front-end, multiple linearity enhancement techniques were proposed and evaluated using simulations. For both current-mode front-end concepts, an extensive analysis on the theoretical output power and power efficiency limit was performed. Although current-mode operation has a high linearity potential, fully reaching this potential turns out not to be trivial, due to various device non-idealities and imperfect impedance matching.

Acknowledgements

For the entire duration of this MSc project, I have enjoyed a great amount of help and support from many people around me. This provided me with the motivation and inspiration that was essential in order to reach this endpoint. Therefore, I would like to express my gratitude here.

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Contents

1 Introduction

Every year, hundreds of millions of new devices connect to the internet, each one adding to the already tremendous amount of data traffic. This increase in devices also comes with a shift in the composition of the connections. In 2023, it is expected that machine-to-machine (M2M) connections and smartphones make up the majority of wireless communication [1]. To cope with this ever-increasing demand for bandwidth, industry is rushing to roll out the fifth generation (5G) of wireless communications. Although companies are squabbling about whose 5G network was deployed the first [2], their services do not live up to the promised power-efficiency potential of the 5G standards [3]. In fact, the current base stations for mmWave 5G communications are equipped with 4G-grade technology, causing their power-efficiency to be "even worse than the old-fashioned incandescent light bulb" [4]. What makes the problem of energy consumption even worse, is that mm-wave links operate on a far shorter distance than the previous generations, requiring many more base stations to realize the same coverage. These current conditions provide the perfect recipe for a fast and immense growth in CO_2 emissions by the telecommunications industry. Therefore, designing power-efficient (base station) front-ends should be a number one priority in the transition to 5G.

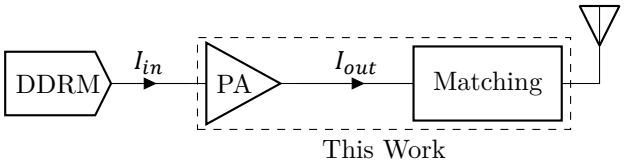
In order to communicate meaningful signals, the front-end must generate its signals with high quality. This requirement generally conflicts with the power-efficiency specification: a class A common-emitter/source (CE/CS) power amplifier (PA) is the most linear operating class, able to provide high signals quality. However, it has poor power efficiency as it conducts current during the entire cycle of the input signal. If the class of operation is shifted to AB, B or even C by making the PA conduct for a smaller fraction of the input signal cycle, the power-efficiency is increased at the cost of linearity. This makes it impossible to match the linearity of class A operation without spending additional energy on linearization techniques such as digital pre-distortion (DPD).
Besides, due to large signal effects, the linearity degrades when the output power approaches the limit of the PA, while the opposite is true for the power-efficiency. To ensure linear amplification of the signal, the PA is normally operated at a certain power back-off, again at the cost of power-efficiency. To compensate for the efficiency reduction at power back-off, one can resort to efficiency-enhancement techniques, such as envelope tracking (ET) [5] or the Doherty power amplifier (DPA) [6]. However, each of those introduce new complexities that can compromise the signal bandwidth and/or linearity. ET, for example, is bandwidth-limited by the speed at which the power supply can be modulated. Due to the high data rates required for 5G this becomes nigh impossible to achieve. The Doherty PA is a more interesting candidate, but also comes with its flaws. In the ideal Doherty concept, the main and peaking PAs are implemented using two ideal transconductances that respectively operate in class B and class C. In reality, the CE/CS stages that implement the transconductance behave highly nonlinear in these regimes (especially

in class C) and thus require linearity compensation schemes such as DPD [6]. The operation of a DPA also highly relies on its targeted load modulation profile, making its performance very susceptible to (external) deviations of the load impedance. Although it is definitely possible to design a DPA that has wideband power-efficiency [7–9], maintaining its linearity up to the same bandwidth using DPD becomes increasingly challenging and power-consuming [10].

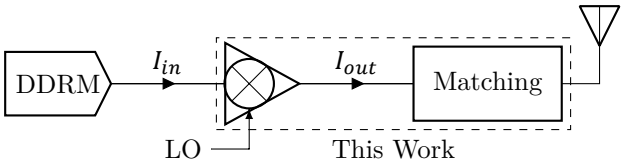
If the signal at the front-end input would be available in the current domain, the CE/CS gain stage could be replaced by a (current-mode) CB/CG gain stage. Besides omitting the nonlinear voltage-to-current conversion of a CE/CS stage, the CB/CG stage is known to provide linear amplification up to the f_T and is theoretically linear up to the edge of hard compression. Consequently, the transmitter should be able to operate at lower power back-off levels and thus yield a higher (average) system efficiency. The high linearity would also remove the need for DPD. In short, current-mode operation would be much more suitable for the design of a (Doherty) front-end that is wideband, linear and power-efficient.
For this approach to be realizable, the current driver at the input also needs to be linear and wideband. Additionally, the current driver must have a large current capability for the TX to enable a large output power, as a pure current-mode front-end only provides voltage gain. The direct-digital RF modulator (DDRM), as presented in [11], fits these requirements and therefore allows to investigate a practical current-mode front-end concept. Although this DDRM design is primarily designed to deliver an IQ-modulated signal at an operation frequency between 0.5 and 3 GHz, it also supports baseband signals. This flexibility gives the following two options for a digitally-enhanced front-end design:

1. Current-mode PA: The DDRM directly delivers a modulated current signal in the low-GHz range and the front-end provides power gain using a CB/CG stage. This concept is visualized in Fig. 1.1a.

2. Current-mode power mixer (PMIX): The DDRM delivers current signals in baseband and the front-end provides both up-conversion to mm-wave and power (voltage) gain. This concept is visualized in Fig. 1.1b.



(a) Current-mode PA concept



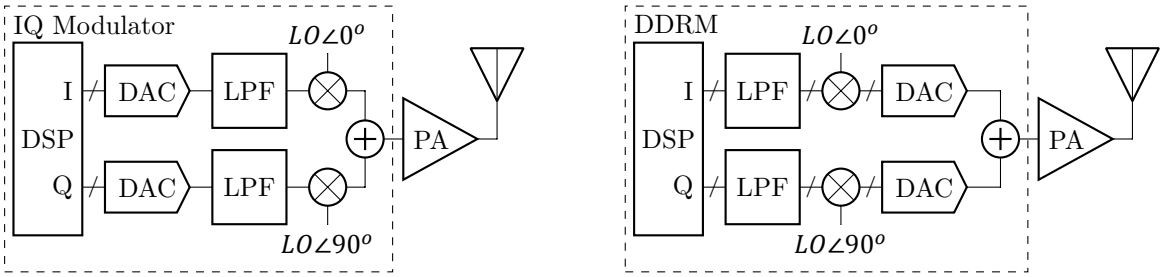
(b) Current-mode power mixer concept

Figure 1.1: System-level concepts of current-mode front-ends.

The exploration of the concepts shown in Fig. 1.1 by designing a front-end corresponding to each concept is the end-goal of this project. The DDRM specifications dictate the front-end operating class and current levels, and thus will be discussed in the next section. The basic topologies for current-mode front-ends will be introduced in Section 1.2 and provide the starting points of the designs. The design requirements will be presented in Section 1.3, after which the introduction is concluded with an outline of the other chapters in this thesis.

1.1. DDRM as a Current Driver

In contrast to a conventional IQ-modulator, a DDRM is digital-intensive, as is shown in Fig. 1.2. Pushing more of the modulator building blocks into the digital domain comes with a couple of advantages. First, a larger portion of the TX chain can be integrated in CMOS, saving area and cost. Secondly, the digital implementation offers flexibility with respect to carrier frequency and bandwidth, which is very useful for multi-channel communications. Finally, if the architecture of the DDRM comprises current-steering mixing-DACs, as is the case in the used DDRM architecture [11], the linearity becomes much better than its analog-intensive counterpart [12].



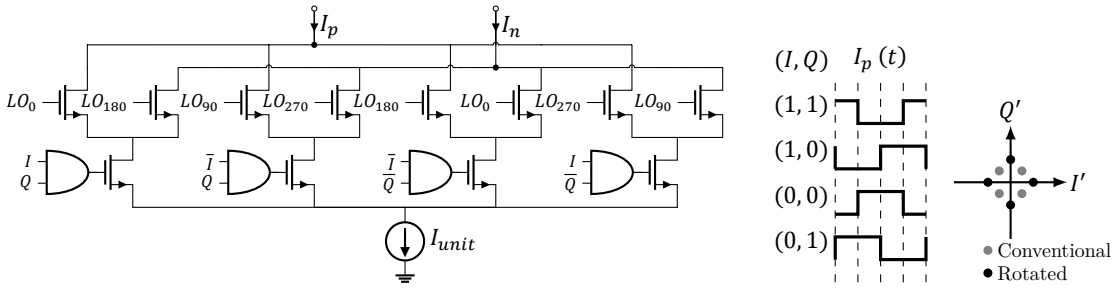
(a) Analog-intensive IQ-modulator in TX chain.

(b) DDRM in TX chain.

Figure 1.2: Architecture of conventional IQ-modulator vs. DDRM in TX chain.

The wideband DDRM from [11] provides the large (RF) output current capability required for a current-mode front-end, while also showcasing an impressive in- and out-of-band linearity and an efficient use of the current budget. To achieve this performance, methods such as dynamic element matching (DEM) [11], harmonic rejection and dynamic biasing [13] are utilized, but also a novel IQ-mapping technique that rotates the constellation diagram of the DDRM unit cell. The design concept of the latter is shown in Fig. 1.3a.

Normally, the up-converted I and Q currents are generated in different unit-cells and combined afterwards, thus requiring two unit cell current sources (I_{unit}). This has two major disadvantages. First, while two DC current sources are needed, the up-converted currents of the I and Q paths add up to just $\sqrt{2}$ times their individual value. In [11], the I and Q data is mapped such that the entire current I_{unit} is directed into only one of the four quadrature switching cores (see Fig. 1.3). As a result, current signals can be generated in all four quadrants using only a single current source. Therefore, when an identical current budget is available, a conventional DDRM produces $\sqrt{2}$ less output power than the IQ-mapping design. Secondly, the use of separate unit cells and current sources introduces I-Q mismatch, degrading the spectral purity at the output. This source of mismatch is absent in the architecture shown in Fig. 1.3a as only a single unit cell for both the I and Q paths is used.

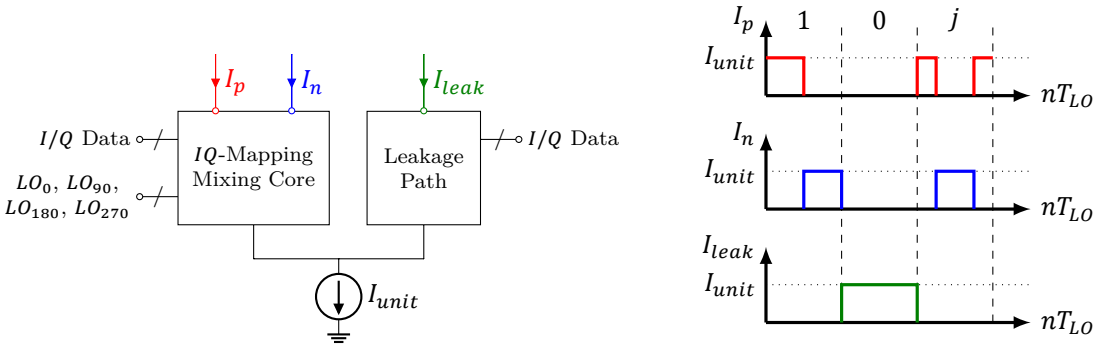


(a) Unit-cell schematic of IQ-mapping concept.

(b) Constellation of I_p

Figure 1.3: [11] IQ-mapping concept to rotate constellation diagram of the unit cell, as such generating a (differential) output current.

The power efficiency of the entire TX chain can be raised by selecting an operational class of the front-end that is class AB or B rather than class A. The first two classes are characterized by their output currents having a conduction angle below 360°, meaning that no current is flowing during a certain portion of the signal period. As a result, the currents of the classes AB and B (the latter being a half-rectified sinusoid) show clipping at the bottom of their waveforms.
For a current-mode front-end, which passes the input current linearly to the output, this would require an input current source that allows clipping at the bottom of the waveforms. In order for a DDRM to realize these waveforms, its unit cells must be able to be turned off. Unfortunately, this is not a very favorable option in DDRM designs, as turning off the unit cell current sources during the signal swing would significantly degrade the DDRM linearity [13].
In the DDRM used, this is solved by introducing an additional leakage path for every unit cell, to which I_{unit} can be provided in case that the waveform of interest requires the unit cell to deliver no external current. This concept is visualized in Fig. 1.4.

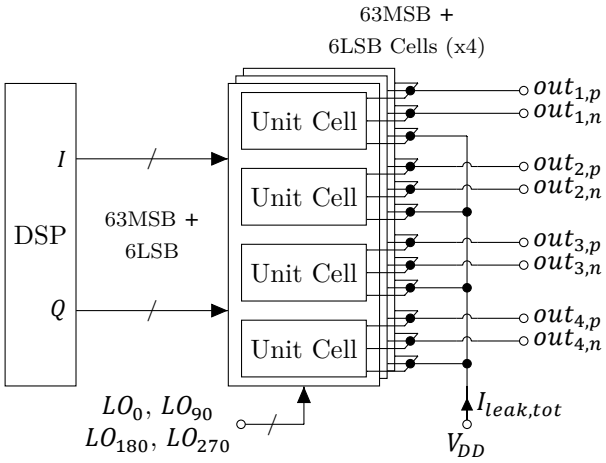


(a) Unit cell block diagram for leakage path concept.

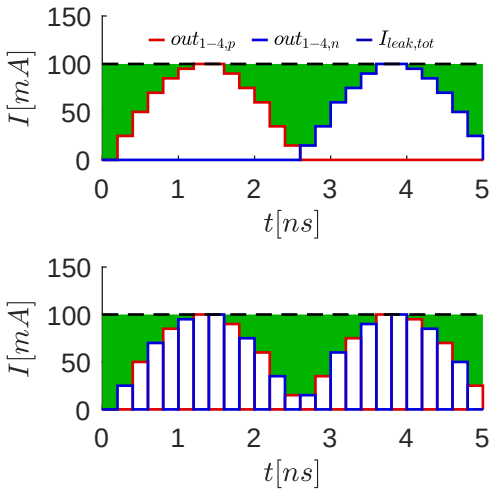
(b) Unit cell currents for various constellation points.

Figure 1.4: The addition of a current leakage path allows to keep the unit cell output current i class A-like conditions, while still be able to provide externally clipped, class B-like current waveforms [13].

The input impedance of the CB/CE stage drops significantly for high input current levels. This impedance drop enlarges the impact of any series inductance or resistance present between the DDRM output and the front-end. This can be avoided if the large DDRM current is distributed over multiple smaller, parallel CB stages in the PA and PMIX design. By presenting smaller currents to the multiple front-end inputs, their CG/CB stage input impedance levels remain higher, which lowers the impact of the interconnect parasitics and maintains broadband operation. The DDRM used for this work uses four differential output channels to distribute its output current, as is shown in Fig. 1.5a.
As stated before, the DDRM offers the option to disable the mixing function, allowing the output signal to be either at baseband or RF. Thanks to the additional leakage path, a wide variety of (clippling) waveforms is available. The two different waveforms shown in Fig. 1.5b are an example of possible output currents in RF and BB operation.



(a) High-current DDRM system-level block diagram featuring four differential outputs.



(b) The DDRM enables BB and RF output waveforms for the output channels.

Figure 1.5: System-level block diagram of the DDRM and example waveforms at the four channels. For the sake of simplicity, dynamic biasing and harmonic rejection are not shown in this figure[1].

The (performance) specifications of the DDRM intended for this project are summarized in Table 1.1. Compared to other designs in [14–16], the DDRM shows excellent linearity and can deliver a broadband and high-power output signal. From the point of view of system efficiency, however, the supply voltage level of 2.5 V may pose a challenge. In order to compensate for the combination of this V_{DD} level and the constant (leakage) current drawn by the DDRM, the entire RF front-end, being the combination of the DDRM and the PA/PMIX core, must operate at a much higher supply voltage and thus deliver a relatively large voltage swing to the antenna.

Table 1.1: Relevant specifications of the DDRM [11].

Parameter	Value	f_{LO}	Bandwidth
Supply Voltage V_{DD}	2-2.5 V		
Maximum current $I_{DDRM,max}$	4x100 mA		
Resolution	2x12 bit		
Peak P_{out} (50 Ω load)	14.1 dBm	2 GHz	
P_{DC} (50 Ω load)	340 mW	2 GHz	
Maximum Bandwidth	400 MHz		
Frequency	0.5-3 GHz		
Modulation Type	256 QAM	2.4 GHz	320 MHz
ACLR1	−43 dB c	2.4 GHz	320 MHz
EVM	−32 dB c	2.4 GHz	320 MHz
DPD	None		

[1]The interested reader is referred to [13]

1.2. Basic Current-Mode Front-End Topologies

This section introduces the basic topologies for the two current-mode front-ends. These include a differential CB stage for the PA ad a Gilbert cell-based quadrature mixer for the PMIX. The emphasis of this section lies on the main functionality of the front-end designs and their potential design challenges.

1.2.1. Power Amplifier

Fig. 1.6 shows the topology of the CB PA. The DDRM has four parallel, differential output ports. In order to lower the impact of interconnect parasitics, the PA output stage must also comprise four parallel PA cells.

A CB stage ideally has unity current gain. Note that, as the base voltage is fixed via V_B, the emitter node varies depending on the V_{BE} required for the input (and thus collector output) current to flow. The bias voltage V_B therefore has to be chosen such that the voltage on the emitter node lies between 2 and 2.5 V (see Table 1.1) at all times. As the CB stage acts as a current buffer for I_{DDRM}, the output power is determined by the voltage swing across Z_{load}. The larger Z_{load}, the larger this voltage swing and thus the power output of the CB stage.

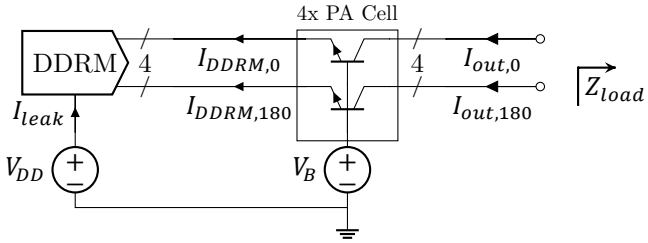
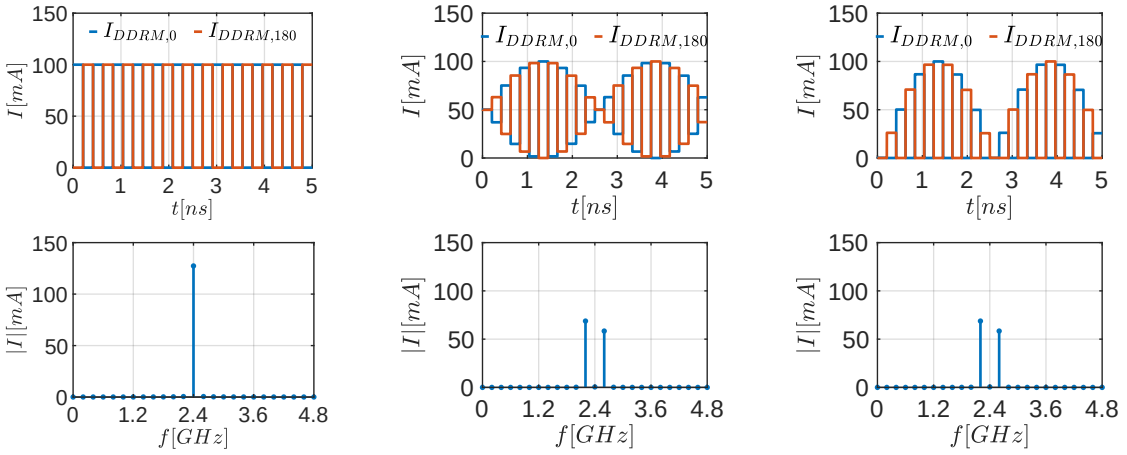


Figure 1.6: Current-mode PA implemented by a differential CB stage. The terms $I_{DDRM,0}$ and $I_{DDRM,180}$ represent the current flowing through one of the four channels coming out of the DDRM. This explanation also applies to $I_{out,0}$ and $I_{out,180}$.

Fig. 1.7 shows three ways the CB PA can be driven. The most basic driving method, a single-tone excitation, is shown in Fig. 1.7a. The single-tone drive does not address a particularly interesting application operation, since it is not a modulated signal. It is, however, useful to investigate the ideal performance of the PA. The class A and class B two-tone excitations shown in Fig. 1.7b and Fig. 1.7c, display the modulation capabilities of the DDRM better.



(a) single-tone signal. (b) Class A two-tone signal. (c) Class B two-tone signal.

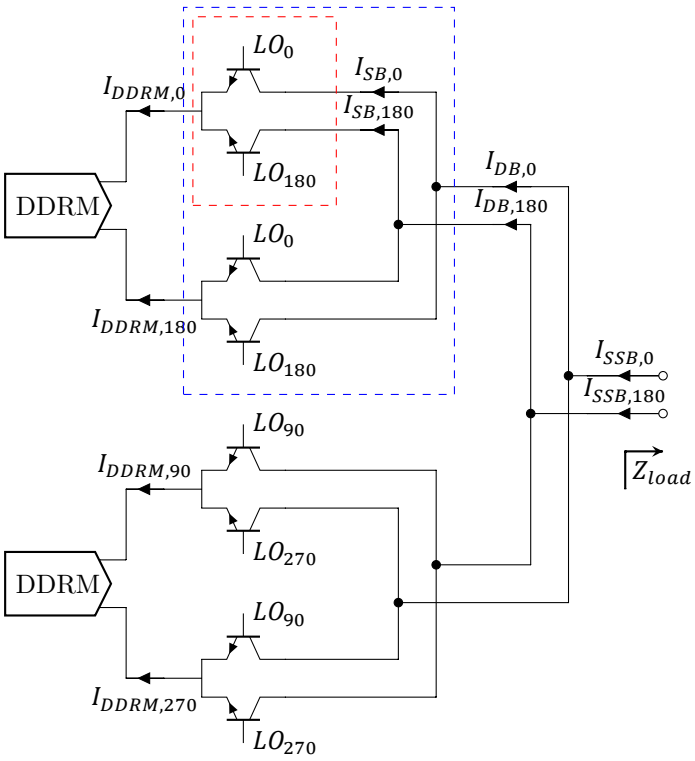
Figure 1.7: Examples of input current waveforms of the CB PA. Top: time-domain representation of single-ended signals. Bottom: spectrum of differential signal.

It is well-known that, due to its smaller DC component, a class B-like current profile can achieve higher (collector) efficiencies than its class A counterpart. For voltage-mode PA designs, this gain in power efficiency is paid for in PA linearity. This trade-off must also be investigated for the CB PA, even though the CB should be inherently linear due to its current-mode operation. In order to really benefit from the linear current-mode operation in terms of power efficiency (e.g. remove need for DPD or operation at low power back-off), great care should be given to investigate sources of nonlinearity in the front-end and how to mitigate these.

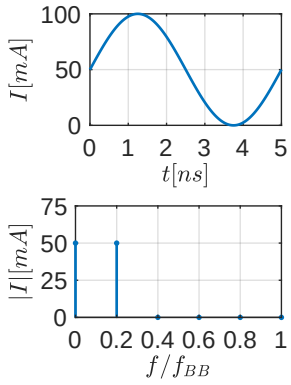
Another major point of attention in the PA design is stability. The large currents (order of 100 mA per device) involved in this design require large device dimensions, resulting in larger parasitics that in turn can result in reduced system stability.

1.2.2. Power Mixer

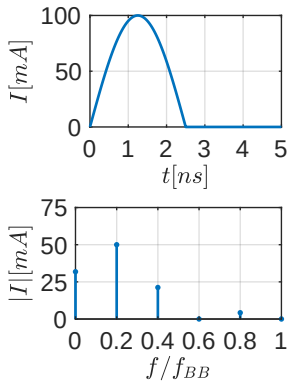
A standard architecture for a current-mode, single-sideband mixer is shown in Fig. 1.8. In contrast to the PA front-end, the PMIX does not rely on the up-conversion functionality of the DDRM, but performs this function itself. Although designing a power mixer rather than a power amplifier introduces additional complexity in the front-end, this approach does allow to up-convert the signal to higher frequency bands (such as mmWave) compared to the DDRM range (low-GHz). Again, there is a choice in the way the front-end is driven. Fig. 1.8b and Fig. 1.8c respectively show a class A and class B baseband drive. For the driving method, the same considerations regarding the trade-off between power efficiency and linearity apply to the PMIX as they did to the PA.



(a) Current-mode SSB mixer of which one of its internal double-balanced mixers and single-balanced mixers is indicated. For the sake of simplicity, the four parallel DDRM channels (and thus PMIX cells) are not shown.



(b) 200 MHz Class A drive ($I_{DDRM,0}$) in time (top) and frequency domain (bottom).



(c) 200 MHz Class B drive ($I_{DDRM,0}$) in time (top) and frequency domain (bottom).

Figure 1.8: Gilbert cell-based current-mode single-sideband architecture for PMIX and two different methods to drive the PMIX with a single-tone signal.

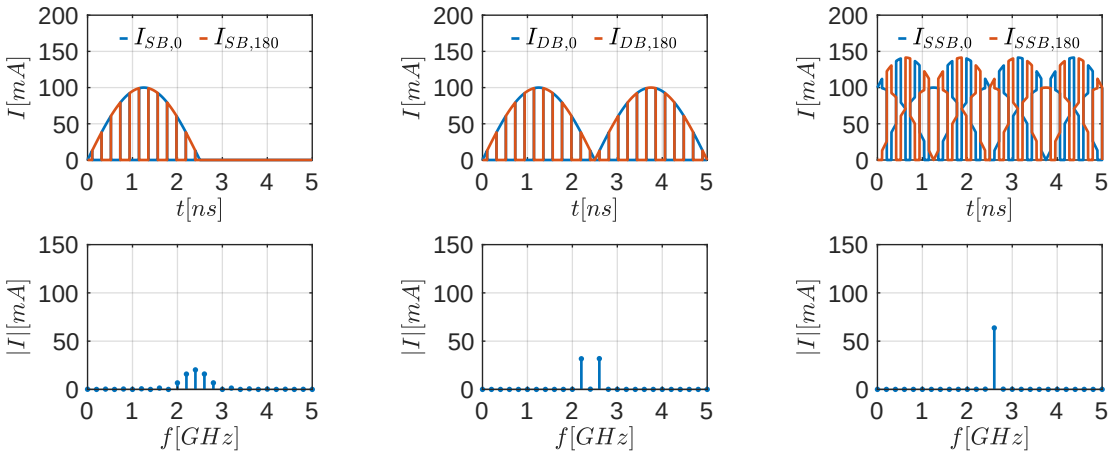
In Fig. 1.8a, three hierarchical levels can be recognized. The single-sideband (SSB) mixer is on the top-level and comprises two double-balanced (DB) mixers placed in quadrature configuration. These DB mixers on their own are constructed using two single-balanced (SB) mixers, of which both their LO and input are in opposite phase. These SB and DB mixers are, on itself, unable to generate the desired I/Q-modulated signal and thus are not interesting from a functional point of view. However, as fundamental building blocks of an I/Q or SSB mixer, it is very useful to analyze their power efficiency and linearity, which will be done in chapter 2. In the subsequent paragraphs, the functionality of the SB, DB and SSB mixers is qualitatively explained, as well as their contribution to the overall front-end functionality. For this discussion, it is assumed that the BJTs in Fig. 1.8a perfectly switch the current, i.e. in a square-wave manner, and have no parasitic capacitors. A more in-depth analysis on the system functionality can be found in [17].

SB mixer

The SB mixer switches the entire input current ($I_{DDRM,0}$) between its two BJTs. The collector current of a single BJT can therefore be described as a multiplication of the input current with a square wave toggling between 0 and 1. The collector current of a class B-driven SB mixer is shown in Fig. 1.9a. The differential nature of the circuit cancels all common-mode mixing products, i.e. terms that arise from the DC term of the square wave. Collector current components that originate from mixing with the square wave fundamental at the LO frequency f_{LO} are differential and thus do show up in the output spectrum. Unfortunately, this also comprises the component at f_{LO}, which is a mixing product of the square wave fundamental and the baseband DC term. In fact, all even harmonics in the baseband signal are up-converted and thus appear in the output spectrum around f_{LO}. Although these terms do not contribute to the transfer of information, they do contribute to the total power consumption and thus effectively lower the power efficiency.

DB mixer

Both the input currents and LO signals of the two individual SB mixers within the DB mixer are 180° out-of-phase with respect to each other. After the up-conversion, the resulting collector currents of the two SB mixers at $f_{LO} \pm f_{BB}$ become aligned and can be added constructively by connecting the outputs as shown in Fig. 1.8a. Though the fundamental components of the input currents are 180° apart, their even harmonics (and DC term) are still in-phase. Therefore, the mixing products of these components and the LO fundamental are in anti-phase between the two SB mixers and thus interfere destructively after the SB mixer outputs are summed. The differential output current spectrum of the DB mixer, as is shown in Fig. 1.9b, shows to be significantly cleaner than that of its individual SB mixers (Fig. 1.9a).



(a) single-balanced mixer (b) double-balanced mixer (c) single-sideband mixer

Figure 1.9: Time-domain representation of the mixer output currents (top) and their respective, differential spectra of the output currents (bottom)

SSB mixer

An SSB or I/Q mixer is constructed by combining the outputs of two DB mixers with quadrature LO signals. For an SSB mixer, the input signals of the DB mixers are identical, but $\pm 90°$ shifted in phase. Using basic goniometric analysis [17], it can be shown that the output currents of the two DB mixers are in phase at $f_{LO} \pm f_{BB}$ and out-of-phase at $f_{LO} \mp f_{BB}$. Whether the upper- or lower sideband is in phase depends on the sign of the $90°$ phase shift between the input signals. As a result, there is constructive interference of one sideband and destructive interference for the other after summing the outputs of the two DB mixers. Fig. 1.8a shows an upper-sideband mixer and Fig. 1.9c shows its output current waveform and corresponding spectrum. For an I/Q mixer, the inputs of the two quadrature DB mixers are two separate, independent signals. This makes the time domain representation of its branch signals somewhat more complicated.

The high current levels and thus large devices will pose severe design challenges for the PMIX. Tiny inductances may be required to resonate with the large parasitic capacitances at the LO frequency, which is much higher than the operation frequency of the PA.
Additionally, as will be shown later in chapter 3, the large parasitic capacitances at the device inputs introduce memory effects, which can be especially problematic for the linearity if (clipped) class B waveforms are used to drive the PMIX. The variation of the parasitic (diffusion) capacitances due to the continual changing collector current makes it even harder to properly solve these problems using standard impedance matching techniques.
Finally, large device sizes and high current levels contribute to smaller BJT output resistance [18], degrading the PMIX operation as a current source and additionally reducing its available output power.

1.3. Project Requirements

In this section, the project requirements and constraints will be given. To provide a clear background motivation for these, some earlier findings will be summarized and a few additional considerations will be given.
As mentioned at the beginning of this thesis, the end-goal of this project is to design a current-mode PA and PMIX in order to explore the performance limits and design challenges of current-mode front-ends. To give direction to the practical design of these front-ends, operation frequencies were selected corresponding to a potential application. Consequently, the DDRM-PA configuration is targeting the $2.4\,\text{GHz}$ band, aiming for the WiFi application. To show the potential of a DDRM-PMIX concept for future mmWave 5G networks, an operation frequency of $28\,\text{GHz}$ was chosen. Using this information, the functional requirements can be given:

- F1 Both the PA and PMIX must operate in current-mode.
- F2 Both the PA and PMIX must increase the voltage swing of their input signal.
- F3 The current-mode PA must operate at $2.4\,\text{GHz}$.
- F4 The current-mode PMIX must operate at $28\,\text{GHz}$.

The non-functional requirements are mainly driven by the performance parameters of interest. As stated before, the front-end should be inherently linear due to its current-mode operation, which also opens possibilities for a more power-efficient system. In other words, although high output power and power efficiency are unmistakably critical design requirements for the front-end of a TX chain, the overall performance of this concept relies on its linearity.
As the aim of this project is to investigate the practical potential of current-mode front-ends, no quantitative requirements will be formulated for the leading performance parameters, being the output power level, power efficiency and linearity. Both front-ends will be designed to maximize all of the aforementioned performance parameters, within the constraints of the DDRM driver and provided technology.
A final, non-functional requirement is related to the system video bandwidth, which follows from the DDRM specifications. As could be seen in Table 1.1, the DDRM is able to provide a broadband

output signal up to 400 MHz. In order to fully utilize the capabilities of the DDRM, the front-end bandwidth should be matched by that of the DDRM. Below, the non-functional requirements are summarized:

N1 Both the PA and PMIX front-ends must be as linear as possible.

N2 Both the PA and PMIX front-ends must have an output power, and thus voltage gain, that is as large as possible.

N3 Both the PA and PMIX must be designed to maximize system power efficiency.

N4 The bandwidth of both the PA and PMIX front-ends must match that of the DDRM.

Most constraints of the front-end are determined by the specifications of the DDRM, which can be found in Table 1.1. The input voltage of the front-ends must conform to the supply voltage requirements of the DDRM. Additionally, the DDRM output current is distributed over its four channels and thus the front-ends must handle four identical, differential input ports. To provide the output power at a single (differential or single-ended) output port, the front-end must combine the power of its four channels. The last constraint posed by the DDRM concerns the current-handling capability of the front-end. The peak current-handling of the front-end must be at least as high as the peak output current of the DDRM.
The final constraint is given by the technology used for this project. NXP Semiconductors, the sponsor of this MSc. project, has made their QUBiC Gen8 SiGe BiCMOS technology available for design and tape-out. The design challenges and considerations of the front-ends will therefore often specifically apply to the QUBiC Gen8 technology. A layout design and tape-out was done for the PA front-end only, due to the limited amount of time available and smaller complexity with respect to the mmWave PMIX. At the end of this thesis, the suitability of the QUBiC Gen8 technology for the design of high-power, linear and power-efficient current-mode front-ends will be reviewed. The list of constraints for this project, as discussed above, is given below:

C1 Both the PA and PMIX front-ends must have four differential signal input ports.

C2 Both the PA and PMIX front-ends must have a single output port that can be either differential (balun off-chip) or single-ended (balun on-chip).

C3 A voltage between 2 and 2.5 V must be present at the inputs of both the PA and PMIX front-ends.

C4 Both the PA and PMIX must have a peak input current-handling capability of 100 mA per channel.

C5 Both the PA and PMIX front-ends will be designed in the QUBiC Gen8 SiGe technology.

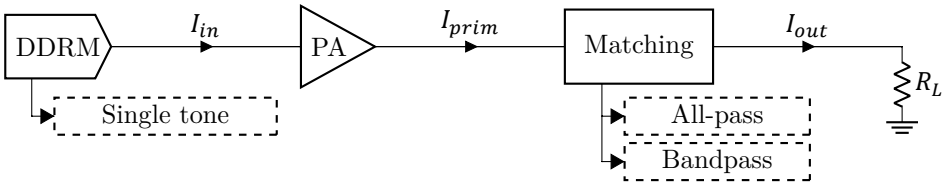
1.4. Outline of Thesis

The goal of chapter 2 is to provide theoretical performance references for the design of the two front-ends. This is achieved by analyzing the limits of the PA and PMIX output power and power efficiency when ideal BJTs would be used.
In chapter 3, non-ideal effect of the transistors and their impact on system performance will be discussed. The practical designs of the current-mode PA and PMIX, that deal with these practical BJT non-idealities, are presented and explained in chapter 4 and chapter 5, respectively. For the PA concept an IC was designed, taped and tested and so chapter 4 will also present the measurement results. The results of both the PA and PMIX designs will be discussed in chapter 6. This chapter will also pose recommendations to improve on the front-end designs. Finally, a conclusion of this thesis will be given in chapter 7.

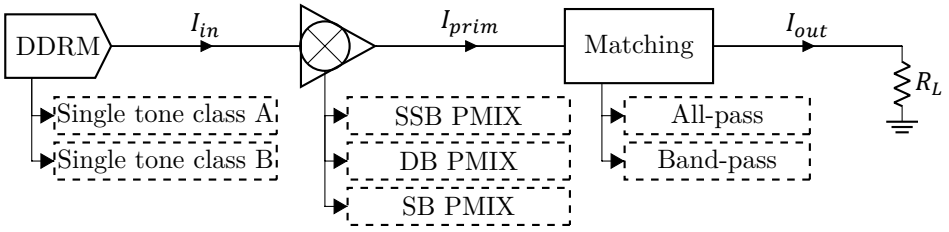
2

The Ideal Current-Mode Front-End

This chapter investigates the theoretical performance limits of the DDRM-PA and DDRM-PMIX front-end architectures in terms of peak power output and power efficiency. Additionally, different driving options and matching networks will be investigated. To provide an overview of these many variables in the system configuration, block diagrams of the front-end concepts are provided in Fig. 2.1.



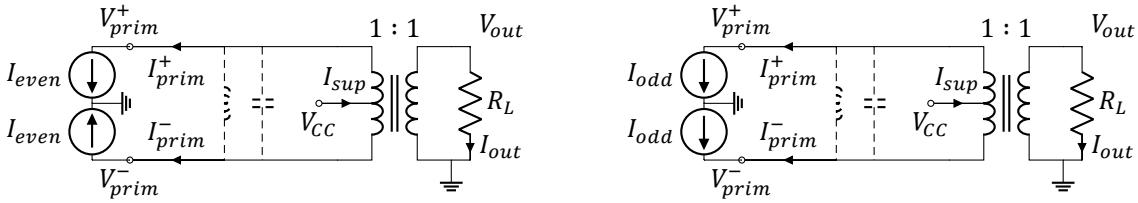
(a) PA-based current-mode front-end



(b) PMIX-based current-mode front-end

Figure 2.1: Block diagram of the current-mode front-end configurations, indicating the different options per building block

Whereas the driving options and PA/PMIX core architecture were already explained in the previous chapter, the matching/loading options do require some additional explanation. For the sake of simplicity, the four parallel channels of the DDRM (see Fig. 1.5a) are replaced by a single channel. Besides lowering the complexity of the PA/PMIX core, also the "Matching" block is simplified, as the need for power combining is removed. The differential PA/PMIX core output can then be connected to a load resistance R_L via an ideal (i.e. all-pass) 1:1 balun, as is shown in Fig. 2.2. This matching network transfers all (odd) harmonic content present from the modulated square-wave in $I_{prim}^{+,-}$ to the load, thus preserving the square-wave current (and voltage) waveforms.
Alternatively, a lossless LC-resonator, tuned to the operation frequency, can be connected to the primary side of the ideal balun. The band-pass characteristic of this matching network presents a more realistic impedance condition to the PA/PMIX output than the all-pass option. To get a



(a) Even-mode excitation

(b) Odd-mode excitation

Figure 2.2: Matching network in even- and odd-mode excitation. Including or excluding the LC-tank gives a band-pass or all-pass matching network, respectively.

complete impression of the truly ideal performance characteristics of the current-mode front-end, both the all-pass and band-pass matching networks will be considered in this chapter.

The ideal performance analysis will be carried out in four steps. First, the the current transfer from the DDRM to the load will be discussed in Section 2.1. Subsequently, expressions for the maximum output power at the frequency of interest (P_{max}) will be derived in Section 2.2.
The emitter voltage V_E (swing) will turn out to play a key role in determining the power efficiency limit of the entire front-end, but also in the intermodulation mechanisms within the PMIX that will be discussed in chapter 3. Therefore, the ideal characteristics of V_E will be briefly considered in Section 2.3. Finally, this chapter concludes with the derivation of the power efficiency limit of both the standalone PA/PMIX core and the entire front-end chain.

2.1. Current Gain

This section addresses the current gain, from the DDRM terminals at the input frequency f_{in}, to the load at the output frequency f_{out}. Ideal operation of all components is assumed during the entire analysis. This means that the BJTs in the PA/PMIX core have an infinite transit frequency, base-to-collector current gain and output impedance. The DDRM is assumed to act as an ideal current source.
Before diving into the different transfer characteristics of PA/PMIX core architectures, the transfer of the matching network is considered. The most intuitive derivation is obtained by driving the matching network in even and odd mode (see Fig. 2.2) and using superposition to find I_{out}. Note that, although a transformer with a unity windings ratio is used, the balun acts as a $1/2 : 1$ transformer for I^+_{prim} and I^-_{prim} individually. This becomes apparent when applying the superposition principle to Fig. 2.2. Upon disabling one of the two I_{even} or I_{odd} sources, only (the other) half of the primary winding remains for the current of the other source. The resulting expressions for I_{out} are given by Eq. 2.1. For the band-pass balun, these equations are only valid at f_{out}. Because the matching networks behave identically at f_{out} they will not be considered separately in this section. Throughout this chapter, I^+_{prim} and I^-_{prim} are used to describe the current output of the PA/PMIX core.

$$I_{out,odd} = \frac{1}{2}I^+_{prim,odd} - \frac{1}{2}I^-_{prim,odd} = I^+_{prim,odd} \tag{2.1a}$$

$$I_{out,even} = \frac{1}{2}I^+_{prim,even} - \frac{1}{2}I^-_{prim,even} = 0 \tag{2.1b}$$

$$V_{out,odd} = V^+_{prim,odd} - V^-_{prim,odd} = 2V^+_{prim,odd} \tag{2.1c}$$

$$V_{out,even} = V^+_{prim,even} - V^-_{prim,even} = 0 \tag{2.1d}$$

Now, the current gain of the PA and PMIX core architectures is considered. The current gain is defined by Eq. 2.2, which represents the ratio between the current component at f_{out} flowing through R_L and the equivalent input current component at f_{in} that flows from the DDRM into

the PA/PMIX core. $I_{in}(f_{in})$ refers to the total input current from all DDRM terminals combined.

$$A_I = \frac{I_{out}(f_{out})}{I_{in}(f_{in})} \tag{2.2}$$

For the PA, the input current is provided directly at the desired RF frequency f_{RF} by the two push-pull DDRM ports (see Fig. 1.6). The equivalent input current is given by the sum of these two ports, while taking into account their phase differences, yielding Eq. 2.3.

$$I_{in,PA}(f_{RF}) = I_{DDRM,0}(f_{RF}) - I_{DDRM,180}(f_{RF}) = 2I_{DDRM,0}(f_{RF}) \tag{2.3}$$

The ideal CB stages buffer $I_{DDRM,0}$ and $I_{DDRM,180}$ to I^{+}_{prim} and I^{-}_{prim}, respectively. At f_{RF}, the PA branch currents drive the balun in odd-mode, and thus $I_{out}(f_{RF})$ can be determined using Eq. 2.1a, yielding $I_{DDRM,0}(f_{RF})$. As this is half the value of $I_{in,PA}(f_{RF})$, the magnitude of A_I is $-6\,\mathrm{dB}$ for the PA. Although it seems strange that the used definition of the input current results the current gain of the PA not being unity, the used definition for the input current is convenient for the discussion of the SB PMIX, which only uses a single DDRM terminal.
The discussion on the PMIX current gain is more comprehensive as it involves the three different hierarchical levels of the SSB PMIX, which are subsequently explained in a bottom-up approach, i.e. starting with the SB PMIX and concluding with the SSB PMIX. The standalone operation of the SB and DB PMIX can be investigated by removing all DDRM/BJT components that are not highlighted in Fig. 1.8.
In the PMIX analysis, f_{in} and f_{out} in Eq. 2.2 are specified by f_{BB} and $f_{LO} \pm f_{BB}$.
The SB mixer, in contrast to the PA, draws its input current from a single DDRM port (see Fig. 1.8). $I_{in,SB}(f_{BB})$ Is therefore equal to $I_{DDRM,0}(f_{BB})$. As was explained in Section 1.2.2, an expression for $I^{+,-}_{prim}(t)$ can be acquired by multiplying $I_{DDRM,0}(t)$ by a square wave with range $[0, 1]$ and frequency f_{LO}. The multiplication with the fundamental sinusoid of this square wave leads to the magnitude of A_I being:

$$|A_I| = \frac{1}{\pi} \approx -9.9\,\mathrm{dB} \tag{2.4}$$

As was the case with the PA, the DB PMIX has a differential input current. Therefore, $I_{in}(f_{BB}) = 2I_{DDRM,0}(f_{BB})$, which is double the size as the input current of the SB PMIX. As the output current components of the internal two SB mixer cores within the DB PMIX add up constructively at f_{out}, $I^{+,-}_{prim}(f)$ is also doubled with respect to the SB PMIX. Subsequently, the SB and DB mixers have an identical current gain. However, as it will turn out later in this section, the DB PMIX has a better utilization of the DC current of the DDRM.
This leaves only the SSB mixer. As explained in Section 1.2.2, the outputs of the two I/Q DB mixers within the SSB PMIX are combined such that one sideband around f_{LO} disappears due to destructive interference, while the other sideband becomes twice as large due to constructive interference. However, the equivalent input current $I_{in,SSB}$, as a result of the quadrature DDRM currents, is given by Eq. 2.5. Overall, the current gain is elevated with $3\,\mathrm{dB}$ with respect to the SB and DB mixers.

$$\begin{aligned} I_{in,SSB}(f_{BB}) =& I_{DDRM,0}(f_{RF}) - I_{DDRM,180}(f_{RF}) + \\ & I_{DDRM,90}(f_{RF}) - I_{DDRM,270}(f_{RF}) = 2\sqrt{2}I_{DDRM,0}(f_{RF}) \end{aligned} \tag{2.5}$$

The concluding current transfers of the front-end architectures are summarized in Table 2.1. This table also provides the in- and output current components at f_{out} present at the maximum

Table 2.1: Output current and current gain per front-end type, in terms of their respective input currents

Front-End Type f_{in}	$I_{in,max}\,(f_{in})$	f_{out}	$I_{out,max}\,(f_{out})$	A_I [dB]	
PA	f_{RF}	$\frac{2I_{DDRM,max}}{\pi}$	f_{RF}	$\frac{2I_{DDRM,max}}{\pi}$	-6.0
SB PMIX	f_{BB}	$\frac{I_{DDRM,max}}{2}$	$f_{LO} \pm f_{BB}$	$\frac{I_{DDRM,max}}{2\pi}$	-9.9
DB PMIX	f_{BB}	$\frac{I_{DDRM,max}}{2}$	$f_{LO} \pm f_{BB}$	$\frac{I_{DDRM,max}}{\pi}$	-9.9
SSB PMIX	f_{BB}	$\frac{I_{DDRM,max}}{2}$	$f_{LO} + f_{BB}$	$\frac{2I_{DDRM,max}}{\pi}$	-6.9

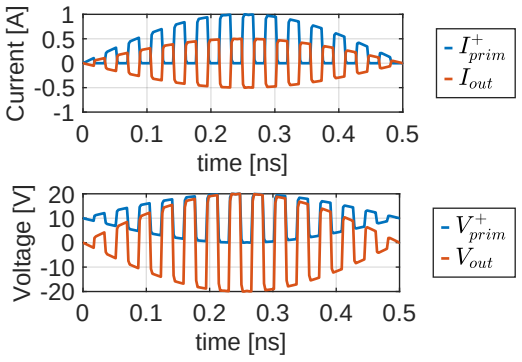
signal strength of the DDRM. For all driving methods under consideration, maximum DDRM signal strength means that $I_{DDRM}\,(t)$ swings between 0 and the maximum current capability of the DDRM $I_{DDRM,max}$. Note that classes A and B for the PMIX configuration have identical fundamental components, and are therefore not considered separately in Table 2.1.

2.2. Peak Output Power

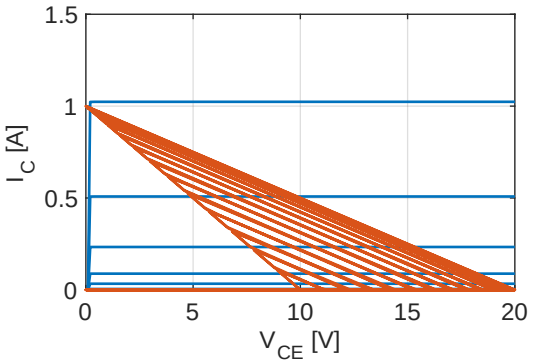
In chapter 1 it was stated that a current-mode front-end is linear up to hard compression, which corresponds to the maximum output power of the front-end, defined as P_{max}. This section focuses on obtaining expressions for P_{max} for all front-end configurations. P_{max} at f_{out} is given as:

$$P_{max} = \frac{1}{2} I_{out,max}\,(f_{out})^2\, R_L \tag{2.6}$$

In Eq. 2.6, $I_{out,max}\,(f_{out})$ can be looked up for all front-end configurations in Table 2.1. R_L, which was omitted from the discussions until now, still has to be determined. A (complex) conjugate match would theoretically achieve the maximum power output, but combination of the extremely high output impedance of the BJT and limited supply voltage eliminate this option. A loadline match produces a voltage swing of V_{CC} on the collector nodes at the maximum DDRM signal and is therefore the best option. Fig. 2.3 visualizes how this translates to a DB PMIX equipped with an all-pass matching network: at the point where $I^{+,-}_{prim}$ toggles between 0 and $I_{DDRM,max}$, the voltage swing yields V_{CC}. The example from Fig. 2.3 is the starting point in the determination of R_L and P_{max} of all front-end configurations.



(a) Voltage and current waveforms at the balun primary and secondary side.



(b) Loadline I^+_{prim} vs. V^+_{prim} in red, and the ideal BJT I_C characteristic in blue

Figure 2.3: Loadline analysis of a DB PMIX loaded with an all-pass matching network. A supply level V_{CC} of 10 V was used and the DDRM delivers a class B current waveform with a $I_{DDRM,max}$ of 1 A.

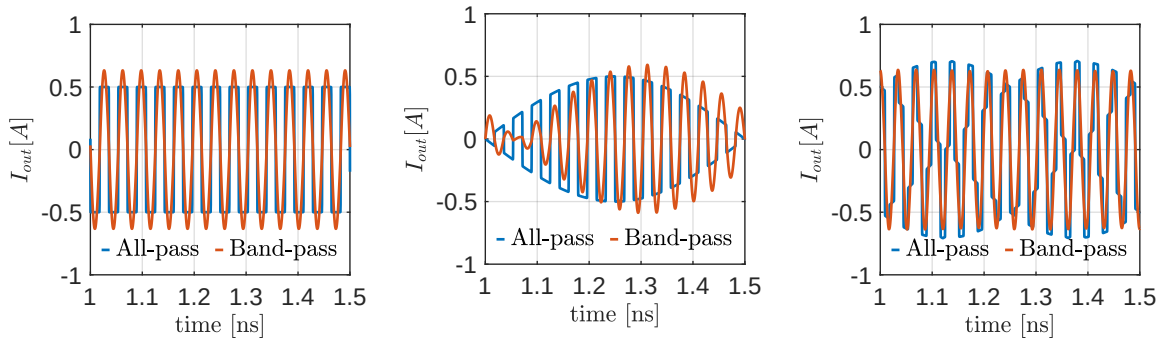
In the example of Fig. 2.3, a loadline match is achieved by choosing R_L according to:

$$R_L = \frac{4V_{CC}}{I_{DDRM,max}} \tag{2.7}$$

The factor 4 in Eq. 2.7 arises from the following observations and assumptions:

- $I_{prim}^{+,-}(t)$ is bounded between $[0, I_{DDRM,max}]$, which is the result of the input currents multiplied with the square-wave. The balun removes the common-mode components within $I_{prim}^{+,-}(t)$, which only includes mixing products from the input current and the square wave DC term. What remains, are the mixing products originating from the input currents and a $[-0.5, 0.5]$ square wave. As a result, I_{out} is bounded between $[-I_{DDRM,max}/2, I_{DDRM,max}/2]$.
- The voltage swing on the two $V_{prim}^{+,-}$ nodes is twice as small as the swing on V_{out} as a result of the voltage transfer of the balun (Eq. 2.1c).
- It is assumed that V_{CE} can be approximated by the collector voltage $V_{prim}^{+,-}$ only. This is possible if the knee voltage V_{knee} of the BJTs is small compared to the collector voltage swing, and the value of the emitter voltage V_E is small compared to the collector voltage swing.

Hence, in order for $V_{prim}^{+,-}(t)$ to have an amplitude of V_{CC}, R_L needs to correspond to Eq. 2.7. Eq. 2.7 does not apply to the SSB PMIX and all configurations that use the band-pass matching network. Fig. 2.4 that this is due to the the different ranges of the envelopes of $I_{prim}^{+,-}(t)$. In order to maintain the loadline match, R_L needs to be adjusted accordingly.
The envelope of $I_{prim}^{+,-}(t)$ of the SSB PMIX equipped with the all-pass matching network reaches a peak current level that is a factor $\sqrt{2}$ higher than $I_{DDRM,max}$ (see Fig. 1.9). Therefore, R_L must be lowered with a factor $\sqrt{2}$ with respect to Eq. 2.7 in order to maintain a loadline match.
In configurations that use a band-pass matching network, the envelope of $I_{prim}^{+,-}(t)$ is increased with a factor $4/\pi$. This increase arises from the fact that the amplitude of the fundamental component of the square fundamental is $2/\pi$, while the amplitude of the square wave is $1/2$. To compensate for this effect, R_L must be lowered with a factor $4/\pi$. Interestingly, if both are equipped with the band-pass matching network, the envelope of $I_{prim}^{+,-}(t)$ of the SSB PMIX reaches the same peak current as that of the DB PMIX and thus the same load can be used. This can be explained by the fact that the upper- and lower sideband in DB PMIX I_{out} spectrum together produce an envelope that reaches as high as the single-sideband in the SSB PMIX I_{out} spectrum on its own.



(a) PA with single tone drive.

(b) SB or DB PMIX driven in class A or B

(c) SSB PMIX driven in class A or B

Figure 2.4: Time-domain representation of I_{out} of all front-end configurations of Fig. 2.1.

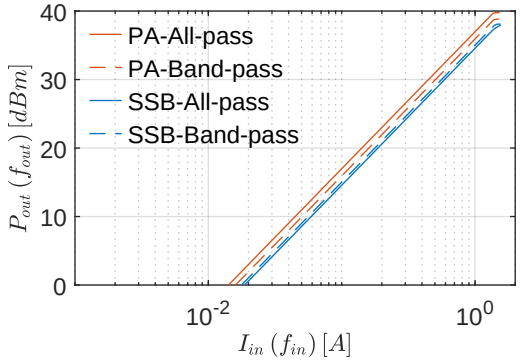
Finally, upon substituting the values of R_L in Eq. 2.6, the maximum output power P_{max} can be found for all configurations. Table 2.2 provides an overview of R_L per configuration, and the

corresponding P_{max}. A remarkable conclusion from Table 2.2 is that the SSB PMIX is the only architecture of which the configuration that uses an all-pass configurations is outperformed by the configuration equipped with a band-pass matching network.

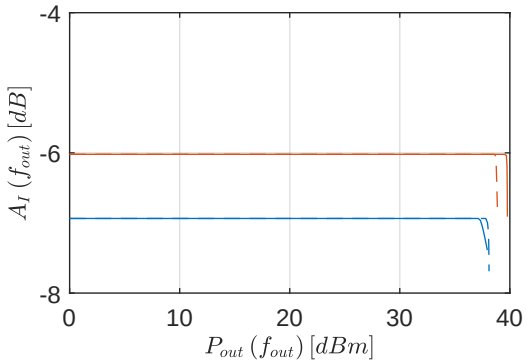
Table 2.2: Output power per front-end architecture, all matched using a class F network. PA driven using a single-tone, PMIX results apply to both class A and B.

	R_L		P_{out}	
	class F	bandpass	class F	bandpass
PA	$\frac{4V_{CC}}{I_{DDRM,max}}$	$\frac{\pi V_{CC}}{I_{DDRM,max}}$	$\frac{8I_{DDRM,max}V_{DD}}{\pi^2}$	$\frac{2I_{DDRM,max}V_{DD}}{\pi}$
SB PMIX	$\frac{4V_{CC}}{I_{DDRM,max}}$	$\frac{\pi V_{CC}}{I_{DDRM,max}}$	$\frac{I_{DDRM,max}V_{DD}}{\pi^2}$	$\frac{I_{DDRM,max}V_{DD}}{4\pi}$
DB PMIX	$\frac{4V_{CC}}{I_{DDRM,max}}$	$\frac{\pi V_{CC}}{I_{DDRM,max}}$	$\frac{2I_{DDRM,max}V_{DD}}{\pi^2}$	$\frac{I_{DDRM,max}V_{DD}}{2\pi}$
SSB PMIX	$\frac{2\sqrt{2}V_{CC}}{I_{DDRM,max}}$	$\frac{\pi V_{CC}}{I_{DDRM,max}}$	$\frac{2\sqrt{2}I_{DDRM,max}V_{DD}}{\pi^2}$	$\frac{2I_{DDRM,max}V_{DD}}{\pi}$

To visualize that the current-mode front-end configurations are perfectly linear up to P_{max}, the current (conversion) gain of the PA and SSB PMIX, including the balun, are plotted in Fig. 2.5b. Fig. 2.5a shows how the output power corresponds to the fundamental component of the input current signals and can be used to link the results from Table 2.2 to Fig. 2.5. Additionally, Fig. 2.5 shows the difference in output power between configurations that use an all-pass or band-pass matching networks.



(a) Output power vs. fundamental component of $I_{in}\,(f_{in})$

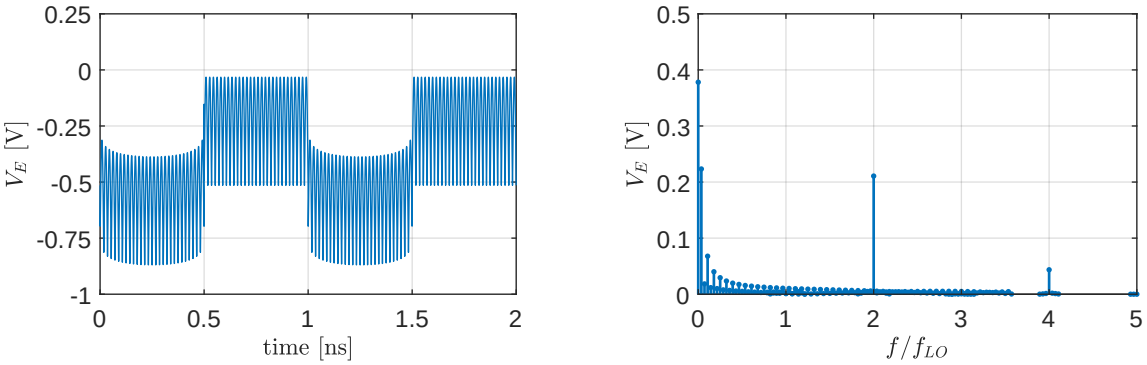


(b) Current gain vs. Output power at f_{out}

Figure 2.5: AM-AM conversion of the PA and SSB PMIX, loaded with either the all-pass or band-pass matching network, using a $I_{DDRM,max}$ of 1 A and a V_{CC} of 10 V.

2.3. Emitter Voltage Range

In the previous section, it was assumed that V_{CE} could effectively be approximated by $V_{prim}^{+,-}$ only. This assumption holds if either a very large V_{CC} is chosen such that $V_{prim}^{+,-}$ is much larger than V_E, or if the base voltage V_B is chosen such that V_E lies around 0 V. In reality, the DDRM requires a certain voltage headroom in order to function and the variation of V_E may not be negligible, as is shown by the example in Fig. 2.6. Additionally, transistor breakdown will limit the value of V_{CC} that can be used. To anticipate for these limitations, the ideal characteristics of V_E are briefly discussed in this section.



(a) Time-domain plot of V_E during two periods of the baseband input signal.

(b) Frequency Spectrum of V_E normalized to f_{LO}

Figure 2.6: Emitter Voltage V_E of a SB PMIX cell driven by a 1 GHz class B input current and a 28 GHz LO with a 0.5 V voltage swing.

For the PA, the emitter voltage is obtained by rearranging the ideal BJT collector current equation. The result is given by:

$$V_E(t) = V_{B,DC} - V_T \ln\left(\frac{I_{in}(t)}{I_S}\right) \tag{2.8}$$

in which V_T is the thermal voltage, I_S the saturation current and $V_{B,DC}$ the bias applied to the BJT bases. Eq. 2.8 shows that the V_E swing is controlled only by the input current.
For the PMIX, V_E is described by a more complex expression, and is obtained by adjusting the equations that describe the collector current of an ideal differential pair [19] to the special case of a SB mixer. The result is given in Eq. 2.9.

$$V_E(t) = V_{B,DC} - V_T \ln\left(\frac{I_{in}(t)}{2I_S \cosh\left(\frac{V_{LO}(t)}{V_T}\right)}\right) \tag{2.9}$$

$$= V_{B,DC} - V_T \ln\left(\frac{I_{DDRM,0}(t)}{I_S}\right) - V_t \ln\left(2\cosh\left(\frac{V_{LO}(t)}{V_T}\right)\right) \tag{2.10}$$

Eq. 2.9 shows that the V_E of a PMIX also largely depends on the (sinusoidal) $V_{LO}(t)$. If Eq. 2.9 is considered during a short time interval in which $I_{in}(t)$ can be assumed constant and $V_{LO}(t)$ is at its equilibrium state, the input current is equally split between the two BJTs. The second logarithm (containing the cosh term) then reduces to $V_t \ln 2$. In the situation in which $V_{LO}(t)$ is at its extremes, the input current flows entirely through one of the devices. In the latter case, the second logarithm can be simplified to $V_t \ln 2 + V_{LO}$. From this and Fig. 2.6 two observations can be made:

1. The voltage variation of $V_E(t)$ is identical to that of $V_{LO}(t)$.
2. Due to the rectifying operation of $\cosh(.)$, V_E contains harmonic content at (multiples of) $2f_{LO}$, and none at f_{LO}.

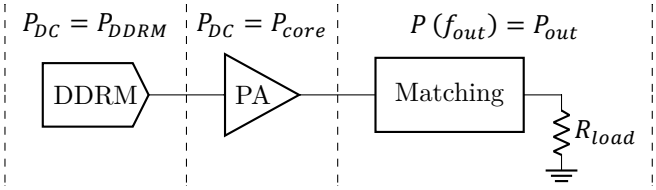
Note that both Eq. 2.8 and Eq. 2.9 fail to describe the emitter voltage when no current is presented to the PA/PMIX input. Fortunately, this problem can easily be omitted by adding a very small current offset (on the order of µAs) to the DDRM currents.

2.4. Ideal Power Efficiency

The general expression for the power efficiency at the frequency of interest f_{out} is given by:

$$\eta_{max} = \frac{P_{max}(f_{out})}{P_{DC}} = \frac{I_{out,max}(f_{out})^2 R_L}{2 I_{sup,DC} V_{CC}} \tag{2.11}$$

in which $I_{sup,DC}$ describes the average current drawn from the supply. Note that P_{max} is defined at a single frequency and thus considers only a single sideband of the SB and DB PMIX output spectra. It should be mentioned that taking the power of both sidebands into account is an equally valid approach. In this work however, the SB and DB PMIX are ultimately subsystems of an SSB PMIX and thus considering only a single-sideband was deemed to be more suitable.
In this section, the the power efficiency will be looked at from two perspectives: the efficiency of the standalone PA/PMIX core and that of the front-end system as a whole. The compositions of P_{DC} corresponding to those two perspectives are defined and visualized in Fig. 2.7.



$$P_{DC,core} = P_{core} \tag{2.12a}$$
$$P_{DC,sys} = P_{DDRM} + P_{core} \tag{2.12b}$$

Figure 2.7: Definition of power dissipation per building block at the relevant frequencies for the PA front-end. A similar distinction can be made for the PMIX architecture.

2.4.1. PA/PMIX Core Efficiency

In Section 2.2, it was mentioned that the voltage drop across the PA/PMIX core is identical to the collector voltage $V_{prim}^{+,-}$. This assumption still stands for the calculation of η_{core}, as a negligible V_E automatically results in zero power consumption of the DDRM.
Table 2.2 can be consulted for the values of P_{max} to substitute in Eq. 2.11. To find P_{DC}, first $I_{sup,DC}$ has to be determined. As all current flowing from the DDRM into the PA/PMIX core has to originate from the supply, $I_{sup,DC}$ is identical to the DC value of the equivalent input current $I_{in,DC}$. In Table 2.3, the DC component of the current flowing from a single DDRM terminal is given per driving class. These expressions can then be used in Eq. 2.13 to calculate the average current drawn from the supply $I_{sup,DC}$ per PA/PMIX core architecture.

Table 2.3: $I_{DDRM,0,DC}$ At maximum DDRM driving strength.

Drive	$I_{DDRM,0,DC}$
single-tone	$\frac{I_{DDRM,max}}{2}$
class A	$\frac{I_{DDRM,max}}{2}$
class B	$\frac{I_{DDRM,max}}{\pi}$

$$I_{sup,DC,PA} = 2 I_{DDRM,0,DC} \tag{2.13a}$$
$$I_{sup,DC,SSB} = 2 I_{sup,DC,DB} = 4 I_{sup,DC,SB} = 4 I_{DDRM,0,DC} \tag{2.13b}$$

Upon substituting the results from Table 2.2 and Eq. 2.13 in Eq. 2.11, the power efficiency limit of all front-end configurations is obtained. The results are summarized in Table 2.4 and Table 2.5.

Table 2.4: Core power efficiency limits of the different configurations of the front-end with a PA core.

	Single-tone Drive	
	all-pass	band-pass
PA	$\frac{8}{\pi^2} \approx 81.1\%$	$\frac{2}{\pi} \approx 63.7\%$

Table 2.5: Core power efficiency limits of all PMIX configurations.

	Class A Drive		Class B Drive	
	all-pass	band-pass	all-pass	band-pass
SB PMIX	$\frac{1}{\pi^2} \approx 10.1\%$	$\frac{1}{4\pi} \approx 8.0\%$	$\frac{1}{2\pi} \approx 15.9\%$	$\frac{1}{8} = 12.5\%$
DB PMIX	$\frac{2}{\pi^2} \approx 20.3\%$	$\frac{1}{2\pi} \approx 15.9\%$	$\frac{1}{\pi} \approx 31.8\%$	$\frac{1}{4} = 25\%$
SSB PMIX	$\frac{2\sqrt{2}}{\pi^2} \approx 28.7\%$	$\frac{1}{\pi} \approx 31.8\%$	$\frac{\sqrt{2}}{\pi} \approx 45.0\%$	$\frac{1}{2} = 50\%$

To provide a more visual representation of the conclusions from Table 2.4 and Table 2.5, the power efficiency of the PA/PMIX is plotted against the output power $P_{out}\,(f_{out})$ for the top-level architecture configurations (the PA and SSB PMIX) in Fig. 2.8.

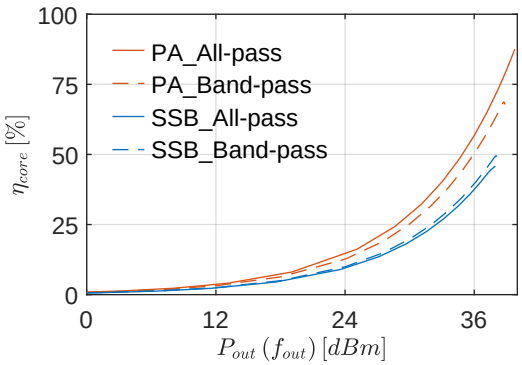


Figure 2.8: η_{core} of the PA and the SSB PMIX (driven in class B), using the same parameters as used to create Fig. 2.5.

2.4.2. System Power Efficiency

In reality, the voltage on the DDRM terminal must not drop below a certain value $V_{DDRM,min}$ in order for the DDRM to function properly. Therefore, P_{DDRM} might not be negligible with respect to P_{core}.

As the collector current flowing through the BJTs or the LO swing increases, V_E drops to lower values, as was explained in Section 2.3. To take care that V_E does not drop below $V_{DDRM,min}$, an offset must be given to the emitter node voltage, which is achieved by applying a positive DC bias V_B to the BJT base terminals. The elevated V_E results in the BJTs entering the saturation region for a collector voltage swing that is lower than V_{CC}. Therefore, to maintain the maximum amplitude of the output voltage and thus P_{max}, V_{CC} must be raised to $V'_{CC} = V_{CC} + V_B$. Unfortunately, the raised supply level also raises P_{DC} and thus lowers the power efficiency of the front-end. The maximum system power efficiency $\eta_{sys,max}$ can be obtained from $\eta_{core,max}$ (as provided in Table 2.4 and

Table 2.5) by applying a factor that compensates for the additional voltage headroom V_B, as is shown below:

$$\eta_{sys,max} = \eta_{core,max}\frac{V_{CC}}{V'_{CC}} = \eta_{core,max}\frac{V_{CC}}{V_{CC}+V_B} \tag{2.14}$$

Fig. 2.9 visualizes how the additional voltage headroom V_B translates to the maximum system power efficiency $\eta_{sys,max}$. Obviously, if no base voltage DC offset is required, $\eta_{sys,max}$ coincides with the maximum core efficiency $\eta_{core,max}$.

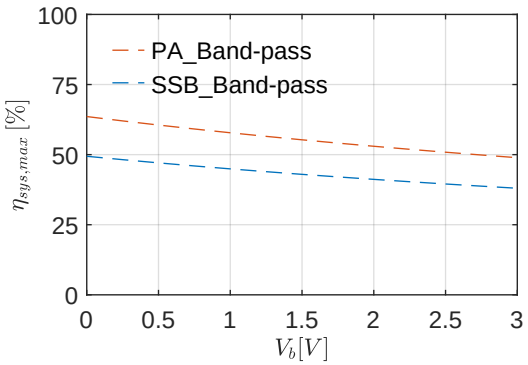


Figure 2.9: The maximum system power efficiency $\eta_{sys,max}$ drops as V_B and, correspondingly, $V'_{CC} = V_{CC} + V_B$ are increased.

2.5. Conclusion

In this chapter, the output power and power efficiency limits of the current-mode front-end configurations of interest were analyzed.

To maximize the output power at the desired operation frequency, the supply voltage V_{CC} and current capability $I_{DDRM,max}$ of the DDRM should be as high as possible.

While the method of driving (class A, B) does not affect the output power, it does have a large impact on the maximum power efficiency. As would be expected, a driving class with a low DC component (e.g. class B) should be selected to drive the PA/PMIX core to increase power efficiency. The loading condition should be selected such that the ratio between the fundamental component of the output current to the amplitude of the the output current is maximized, as this maximizes the output power for a given driving strength and thus lifts the efficiency. For the SSB PMIX, a band-pass matching network gives optimal performance, while for the other architectures the ideal, and therefore unrealistic, all-pass matching network gives the best results.

Finally, the portion of the supply voltage reserved for the DDRM headroom should be minimized to increase system power efficiency. Although this can be achieved by minimizing the emitter voltages in the PA/PMIX core (e.g. by using a smaller LO swing or using a DDRM that requires a small headroom voltage), the most straightforward approach is to select a large supply voltage. The ideal performance limits as provided in this chapter will serve as a useful benchmark when the design of the practical PA/PMIX cores is discussed in the coming chapters.

3

Technology Limitations

The results presented in chapter 2 are very useful to understand the fundamental limits of current-mode front-ends. However, they are not representative for the performance that can actually be achieved using practical devices. Up to now, the effects that make the front-end perform differently from the ideal case were largely left from the discussion. This chapter elaborates on the dominant non-ideal effects in a practical current-mode front-end and how they affect the performance.
The frequency limitations of the available HBT devices in the used QUBiC Gen8 technology are presented in the Section 3.1. In Section 3.2, the role of avalanche breakdown in a high output power design will be discussed. The output impedance of the devices is another critical element when designing for high output power, and will be discussed in Section 3.3. Finally, Section 3.4 investigates the consequences of the C_{BE} parasitic capacitor on the linearity of a PMIX-based current-mode front-end.

3.1. Device Speed

The transit frequency f_T is defined as the frequency at which the intrinsic current gain of a CE/CS stage drops to unity, and is a measure of the maximum achievable speed of a transistor. In many cases, the circuitry around the transistor limits its speed to lower frequencies. This statement is less applicable to transistors used in CB/CG configuration, as these an exhibit an input pole that lies very close to f_T and do not suffer from the Miller effect [19]. As a result, these configurations are well-known for their high speeds.
The f_T highly depends on the current density within the device. A higher current density results in a higher f_T, up to the point at which high-injection effects start to occur and the f_T starts decreasing again [20]. As a result, an optimum current level can be found that gives the maximum f_T for a given device size. By tailoring the size of the device, the maximum f_T can be placed at the desired current level. Fig. 3.1 shows that, if a device with the dimensions as given in Table 3.1 is used, the maximum f_T is reached at around $100\,\mathrm{mA}$, which corresponds to the maximum current capability of the DDRM.

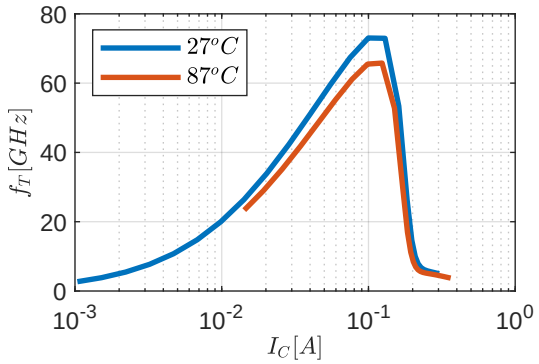


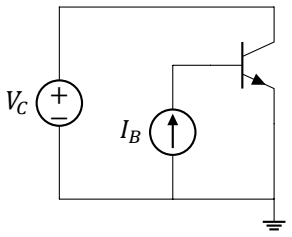
Figure 3.1: f_T of BNP EHV device, with a collector-emitter voltage V_{CE} of 1 V

Table 3.1: Device Dimensions used for Fig. 3.1

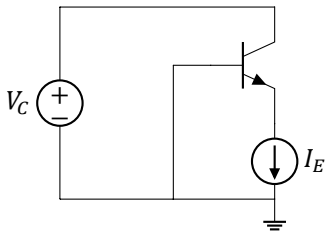
Parameter	Size
Emitter Length	16.5 µm
Emitter Width	0.4 µm
No. Emitters fingers	3
No. parallel devices	8
Tot. Emitter Area	158.2 µm^2

3.2. Avalanche Breakdown

When the collector-emitter voltage V_{CE} of the HBT exceeds the avalanche breakdown voltage V_{BD}, the collector current starts to increase rapidly and the transistor stops functioning as desired. Consequently, the V_{BD} poses a limit to the collector voltage swing and thus defines the maximum output power that can be delivered by the transistor. Avalanche breakdown starts to occur when the electric field in the B-C junction becomes so large that the charge carriers in the junction have sufficient energy to ionize atoms. The junction current will increase and the newly generated holes and electrons can partake in the ionization process of other atoms [20]. Interestingly, the value of V_{DB} is not constant and varies depending on the biasing, device temperature and the circuitry around the transistor. Understanding these dependencies is very crucial when designing circuits that can deliver high output power. Therefore, this section investigates the avalanche breakdown characteristics of a QUBiC Gen8 BNP EHV device in conditions relevant for the PA and PMIX. First, V_{BD} is studied in two extreme transistor configurations: a transistor biased using a current source at the base terminal (Fig. 3.2a) and a transistor biased with a current source at the emitter terminal (Fig. 3.2b). These configurations are referred to as the open-base condition and open-emitter condition, respectively. In the open-base condition, all generated avalanche current must flow into the B-E junction, as the base current is impressed by the current source. The additional emitter current increases the forward-bias of the B-E junction, which exaggerates the avalanche effect. This positive feedback loop results in the open-base biasing configuration having a very low avalanche breakdown voltage, defined as BV_{CEO}. In the open-emitter configuration, all generated avalanche current flows into the ground at the base terminal, preventing amplification of the the collector current via the transistor action. This gives the open-emitter configuration a very high breakdown voltage, defined as BV_{CBO}[20].



(a) Open-base configuration, yielding $V_{BD} = BV_{CEO}$

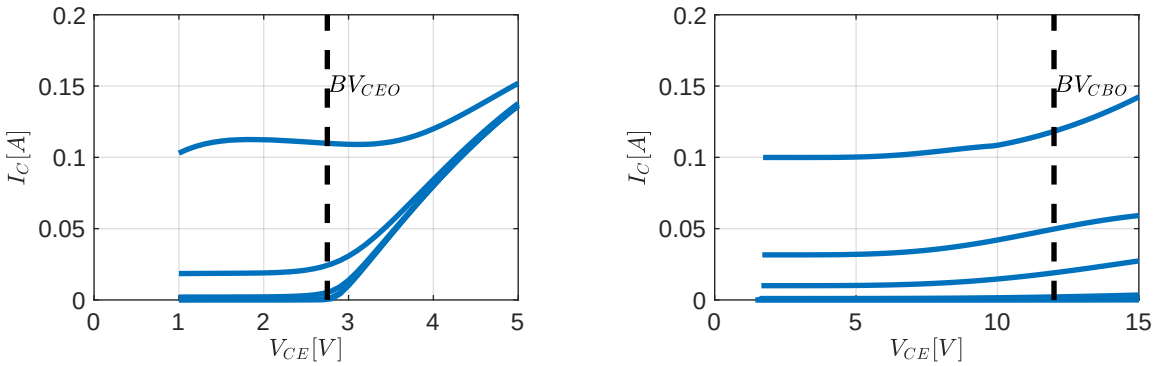


(b) Open-emitter configuration, yielding $V_{BD} = BV_{CBO}$

Figure 3.2: HBT configurations leading to minimal and maximal avalanche breakdown voltage.

Fig. 3.3 shows the breakdown characteristics of the open-base and open-emitter configurations. In this figure, it can be seen that BV_{CEO} increases for higher collector currents. This is partly the

result of reduced avalanche generation and device gain as the device heats up [21]. Another factor is the doping profile in the collector, which, in combination with the collector current, influences the electric field in the collector and thus the generation of avalanche current.

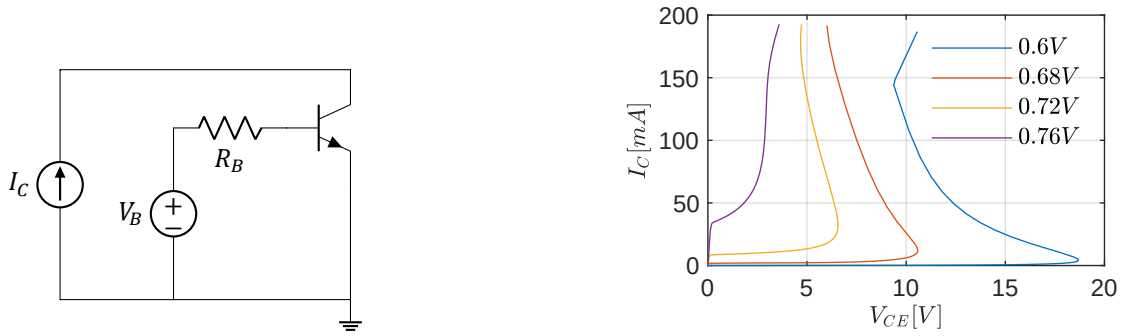


(a) Open-base breakdown voltage BV_{CEO}

(b) Open-emitter breakdown voltage BV_{CBO}

Figure 3.3: Avalanche breakdown voltages corresponding to the extreme open-base and open-emitter configurations

It can make a difference whether the breakdown performance of a more practical transistor configuration is analyzed near DC or at RF frequencies. Near DC, the high output impedance of the DDRM and the relatively low impedance path to the ground at the base terminal make that the devices in the PA and PMIX are practically in open-emitter configuration. At RF frequencies, there is not necessarily a high impedance at the emitter node, as (parasitic) capacitances can lower the impedance between the emitter and the ground. Furthermore, RF signals have practically no effect on the device temperature, as self-heating is a relatively slow process. These discrepancies between DC and RF operation necessitates the investigation of the avalanche breakdown in the transistor configuration shown in Fig. 3.4a.
The voltage source V_B and the resistor R_B are two external factors influencing the avalanche breakdown in the situation shown in Fig. 3.4a. Even with R_B set to zero, the breakdown voltage decreases with respect to BV_{CBO}, due to the internal base resistance r_B of the device and the absence of I_E from Fig. 3.2b. Any avalanche current traversing through r_B increases the internal base voltage of the device, increasing the forward bias of the B-E junction. This positive feedback loop becomes stronger for larger values of V_B as this increases the collector current which can create more avalanche current, resulting in a higher voltage drop across r_B. The dependence of the avalanche breakdown on V_B without R_B is shown in Fig. 3.4b.

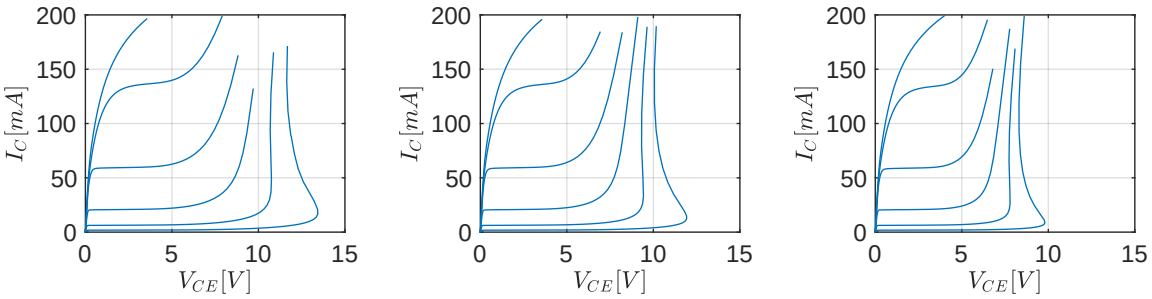


(a) Testbench for RF avalanche breakdown

(b) I_C versus V_{CE} for various V_B values and $R_B = 0\,\Omega$

Figure 3.4: Testbench for the avalanche breakdown analysis of QUBiC4 EHV BNP device at RF frequencies

The role of the resistor R_B is very similar to that of the internal base resistance r_B. For small values of R_B, the avalanche current in the B-C junction can easily flow to the ground and the breakdown behaviour is similar to Fig. 3.4b. For larger R_B, two similar effects can take place. First, the avalanche current flowing into the base path through R_B increases V_{BE}, thus magnifying the generation of the avalanche current via the transistor gain [22]. Secondly, more of the avalanche current will be injected into the B-E junction because of the higher impedance condition at the base, moving the breakdown voltage towards BV_{CEO} [21]. Fig. 3.5 shows how the avalanche breakdown voltage of a QUBiC Gen8 EHV BNP device decreases for larger values of R_B.
To prevent avalanche breakdown, the operating point of the device should always remain below both the DC and RF breakdown voltages. To prevent DC breakdown, this means that the average V_{CE} should always remain below BV_{CBO}. To prevent RF breakdown, the dynamic load line of the devices must remain below the avalanche operating conditions visible in Fig. 3.5. The exact RF breakdown limits are, however, highly dependent on external conditions such as the resistance in the base path.



(a) $R_B = 1\,\Omega$ (b) $R_B = 10\,\Omega$ (c) $R_B = 100\,\Omega$

Figure 3.5: Avalanche breakdown voltage for three different R_B values. Multiple V_B values, similar to those in Fig. 3.4, were used to provide a better overview.

3.3. Output Impedance

This section investigates what the consequences are of a finite R_0 and what effects limit the value of R_0 in the QUBiC Gen8 technology. The behaviour of a HBT in CB configuration can be modelled using a current-controlled current-source with unity current gain, as is depicted in Fig. 3.6.

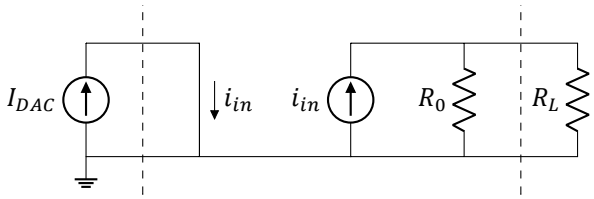


Figure 3.6: CB stage modelled as a current-controlled current source

Section 2.2 stated that a loadline match, bounded by the breakdown voltage V_{BD}, results in the optimum value for R_L. This matching condition makes sure that both the voltage-handling capability of the device and the current capability of the DDRM are fully utilized. The derivation in Section 2.2, however, assumed that the output impedance R_0 of the CB stage is infinite.

3.3.1. Effects of Finite Output Impedance

In many RF designs, the load impedance is chosen to be conjugately matched to the output impedance of the circuit as this results in maximum power transfer to the load. This poses the question of why a loadline match is preferred in the current-mode PA and PMIX design. To

analyze this, Eq. 3.1 is considered, which describes the output power of the circuit shown in Fig. 3.6.

$$P_{out} = \frac{1}{2} I_{DAC}^2 \frac{R_0^2 R_L}{(R_0 + R_L)^2} \tag{3.1}$$

It is well-known that P_{out} can be maximized if R_L is a conjugate match to R_0. Applying this condition to Eq. 3.1 results in:

$$P_{out,ML} = \frac{1}{8} I_{DAC}^2 R_L \tag{3.2}$$

Looking more closely to Eq. 3.1 leads to the conclusion that no value for R_S exists that maximizes P_{out}: the larger R_S becomes, the higher the output power. In the limit, P_{out} converges to:

$$P_{out,CS} = \frac{1}{2} I_{DAC}^2 R_L \tag{3.3}$$

In summary, a large R_0 increases the maximum power that can be drawn from the device in Fig. 3.6, while choosing R_L equal to R_0 makes sure that this maximum power is extracted from the device.
In a more practical situation, the voltage swing is limited by the breakdown characteristics of the device. This makes conjugate matching virtually impossible if R_0 is very large. In this case a loadline match is the best option and Eq. 3.3 applies. In this chapter, R_L required for a loadline match is defined as R_{opt}. In case $R_0 > R_{opt}$ and the approximation of Eq. 2.6 by Eq. 3.3 does not apply, R_L should be chosen according to Eq. 3.4 [18].

$$R_L = \frac{R_0 R_{opt}}{R_0 - R_{opt}} \tag{3.4}$$

However, if Eq. 3.4 results in $R_L > R_0$, the output impedance of the HBT will dissipate more power than the load, and thus conjugate matching is preferred. Evidently, this is also the case if $R_0 \leq R_{opt}$, in which a loadline match is not physically possible.
In short, the output impedance of the QUBiC Gen8 EHV BNP devices and subsequently the PA and PMIX must be as high as possible in order to provide a high output power.
Finally, Eq. 3.1 can be used to predict that the linearity off the CB stage may degrade if R_0 is sensitive to the transistor biasing, which changes during large signal operation.

3.3.2. Output Impedance of CB Stage

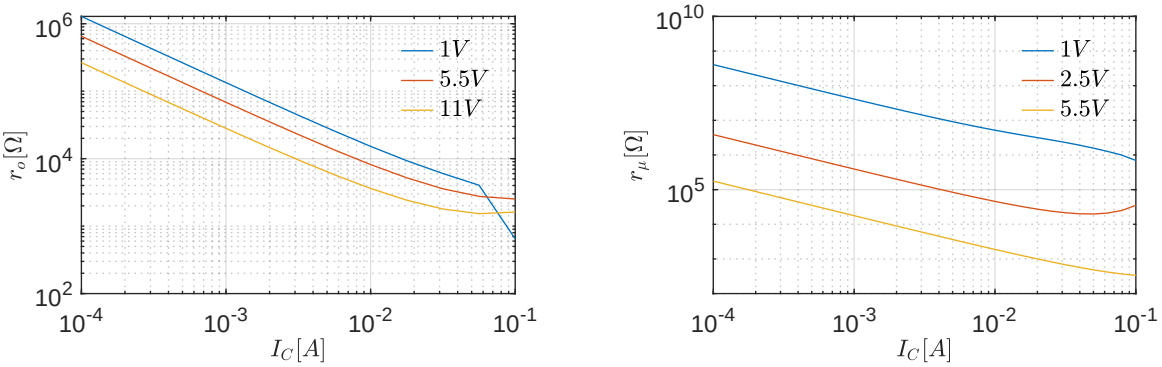
When the CB stage is driven by a current source and its base is grounded, it exhibits a very high output impedance, given by Eq. 3.5 [19]. In Eq. 3.5, r_π is the junction diffusion resistance and r_0 is the resistance primarily associated with the Early effect.

$$R_0 = g_m r_\pi r_o + r_\pi + r_o \tag{3.5}$$

In reality, the output impedance of the CB stage will be lower than the one given above. This section discusses three effects that can potentially reduce the output impedance of a QUBiC Gen8 EHV BNP device: the Early effect, avalanche current generation and high frequency effects.
First, the Early effect is briefly considered. As the voltage across the B-C junction increases, the depletion region moves further into the base, reducing the effective width of the base and thus resulting in a larger diffusion current. In other words, the collector current increases with V_{CE}. In

the hybrid-pi representation of the HBT, this Early effect is modelled by a resistance r_o between the collector and emitter terminals. The value of r_o is inversely proportional to the collector current, and can be found using Eq. 3.6 [20]. Fig. 3.7a shows r_o of the used EHV BNP devices for a range of collector current and voltage levels.

$$r_o = \frac{V_{CE} + V_A}{I_C} \approx \frac{V_A}{I_C} \tag{3.6}$$



(a) r_o versus I_C for different values of V_C

(b) r_μ versus I_C for different values of V_C.

Figure 3.7: r_o and r_μ of the QUBiC Gen8 EHV BNP device. Beware that V_{CE} can be several hundreds of millivolts higher than the displayed V_C depending on I_C.

The generation of avalanche current is the second effect that can influence the output impedance of the CB stage. In the avalanche operating region, the collector current increases rapidly as V_{CE} grows. As a result, the output impedance of the transistor drops dramatically. In the hybrid-pi model, shown in Fig. 3.8 for a HBT in CB configuration, r_μ is the resistance associated with the avalanche current generation. Normally, this resistor can be neglected as it represents the extremely large reverse-biased diffusion resistance of the C-B junction [20]. Only if r_μ decreases due to the avalanche effect, it could influence the output impedance of the CB stage. The dependence of r_μ on the collector current is shown in Fig. 3.7b.

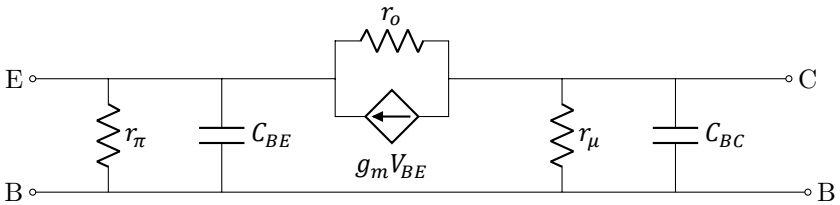


Figure 3.8: Hybrid-pi bipolar transistor model, including the B-C reverse-biased (diffusion) resistor.

The results above and Eq. 3.5 predict a very high level for the output impedance. Unfortunately, this is unrealistic to expect due to high-frequency effects. As the operation frequency increases, the following effects start to play a role:

- A finite impedance connected to the emitter node decreases the output impedance of a CB stage [19]. As a result of (parasitic) capacitances present at the emitter node (e.g. the base-emitter diffusion capacitance C_{BE}) Eq. 3.5 reduces to:

$$\lim_{\omega \to \infty} R_0 = \frac{(g_m + j\omega C_{BE})\, r_\pi r_0 + r_\pi + r_0}{1 + j\omega r_\pi C_{BE}} \approx r_0 \tag{3.7}$$

- Lower (internal) quality factors at high frequencies due to various device parasitcs result in internal device losses, which in turn results in a lower output impedance.

The seconed reason, proves to be the most problematic. In [18], [23] and [24] it was shown that the output impedance of the device decreases for high frequencies, as various parasitics lower the Q-factor at various nodes in the device model. These parasitics become more prevalent if the device size increases and/or more devices are connected to the output node. To characterize this effect, the test bench circuit shown in Fig. 3.9 was used. Using an AC analysis, both the output resistance and capacitance can be determined at the resonant frequency of the circuit.

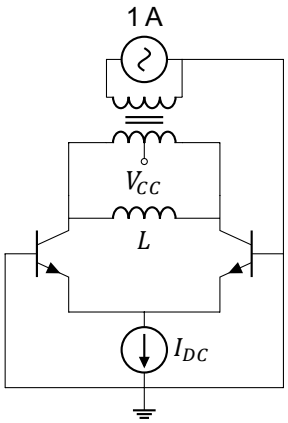
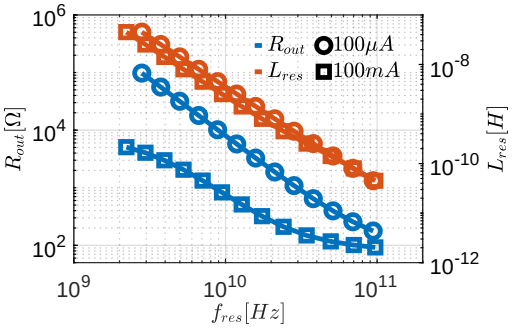
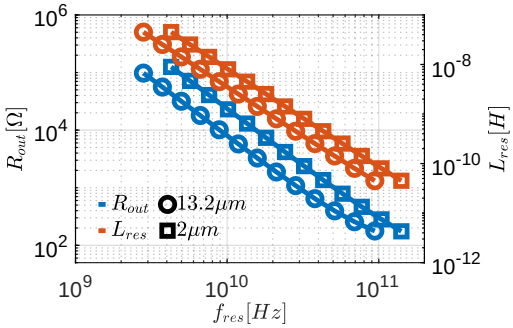


Figure 3.9: Test bench for measuring internal losses of a HBT pair. The inductor L is used to resonate with capacitances at the collector nodes.

The result in Fig. 3.10 proves that the output resistance at mm-wave frequencies is dominated by losses associated with internal device parasitics. The observed decrease in output resistance at high current levels cannot be attributed to the Early and avalance effects, as the decrease is too large compared to the r_o and r_μ values observed in Fig. 3.7.



(a) Output impedance characteristic for low and high current condition using an emitter length of 13.2 µm



(b) Output impedance characteristics for two emitter lengths at low current condition of 100 µA

Figure 3.10: Output impedance and corresponding tuning inductance of BNP transistor scaled for 100 mA. Avalanche effects were turned off in the model. A collector voltage of 5.5 V was used.

A better explanation for the reduced output resistance would be a higher impact from parasitic capacitances such as the C_{BE} capacitance. As could be observed in Eq. 3.7, this capacitance lowers the loop gain of the CB stage and decreases the impedance seen at the emitter node. A larger C_{BE} causes the output impedance of the CB stage to drop at lower frequencies. Finally, the Mextram transistor model (used in the QUBiC Gen8 PDK) does not take substrate losses into account [25]. Therefore, the output impedance may even be lower in reality.

3.4. Influence of Emitter Capacitances on PMIX Linearity

To provide a performance reference for a PMIX designer, the current gain of different ideal mixer cells was derived in Section 2.1. Section 3.3 already introduced effects that lower the device output impedance, which is one example of how the practical current gain can differ from the ideally predicted values in Table 2.1. A more complex mechanism, affecting the ideal current gain, arises from the presence of (parasitic) capacitances at the emitter node, such as the ones shown in Fig. 3.11. As a result of charge storage in these parasitic capacitances, the voltage waveform of the emitter node becomes dependent on the DDRM current I_{DDRM}, which in turn affects the mixer linearity. To provide a more comprehensive background for a PMIX designer, this mechanism is studied in more detail in this section.

The linearity in Gilbert cell mixers has been extensively studied in the past. In [26], it was shown using a small-signal analysis how charge storage around the emitter node affects the collector voltage waveform and the current conversion gain of a bipolar SB mixer. Although the intuitions in [26] are very useful to grasp the different processes in a PMIX design, the conclusions are not directly applicable to this work, as the (class B) waveforms from the DDRM result in large signal operation of the PMIX.

The studies [27], [28] and [29] focus on modelling and uses techniques like (time-variant) Volterra series to accurately predict the linearity performance of CMOS mixers. This is a complex and time-consuming procedure when applied to a strong nonlinear system, such as a current-mode SB mixer suffering from various parasitics, and yields complicated results that do not provide an intuitive understanding of the underlying mechanisms.

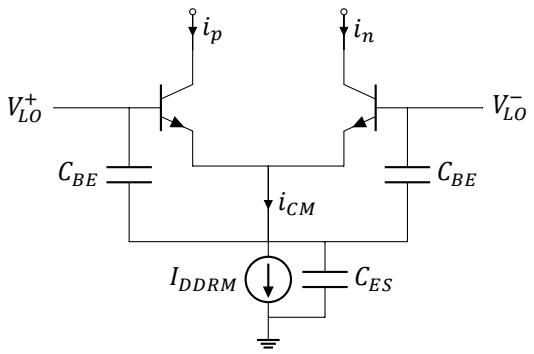


Figure 3.11: SB mixer structure, with various parasitics connected to the emitter node indicated.

An analysis that is more useful closer for this project is presented in [30], which discusses second order intermodulation mechanisms in CMOS down-conversion mixers. One of the conclusions of [30] is that a low-frequency current, drawn from the common-emitter node, will modulate the RC time constant formed by the $1/g_m$ of the device and the emitter capacitances. This effect resulted in intermodulation of the emitter voltage, the low-frequency currents and the LO signal, which directly affected the current gain.

To provide a more complete understanding of this intermodulation effect in a PMIX-based front-end, a similar, but simplified version of the analysis of [30] is presented in this section. Linearity degradation of the PMIX as a result of emitter capacitances can originate from effects at both baseband and mm-wave frequencies. First, the effects at baseband will be considered.

3.4.1. Linearity Degradation at Baseband Frequencies

As stated above, the capacitances at the emitter node, together with the input impedance of the HBTs, introduce a time constant at the input of the circuit shown in Fig. 3.11. To keep the equations in this section concise, all capacitances in Fig. 3.11 are replaced by a single capacitor to the ground, defined as C_{par}. The time constant at the emitter node is given by Eq. 3.8, which

shows a strong dependency on the currents flowing through the HBTs.

$$\tau_E = \frac{C_{par}}{g_m} = \frac{V_T C_{par}}{I_C} \tag{3.8}$$

Very small levels of I_{DDRM} inherently result in an increase of this time constant, which in turn causes a larger portion of I_{DDRM} to flow into the capacitor rather than the HBT. As a result, the current conversion gain diminishes with respect to the ideal values for smaller I_{DDRM}. A rough estimate of the quiescent input current required to maintain g_m at a sufficiently high level, and thus preventing this loss in conversion gain, is given by:

$$I_{DDRM} \geq 2\pi f_{BB} C_{par} V_T \tag{3.9}$$

3.4.2. Linearity Degradation at mm-Wave Frequencies

This section describes the high-frequency effects of the emitter capacitances on the current transfer of an SB PMIX. First, the relation between the emitter voltage and the input current I_{DDRM} will be derived. Then, it will be explained how this relation results in intermodulation products appearing in the V_E spectrum, which are then translated into parasitic currents flowing through the emitter capacitances. Finally, it will be discussed how these parasitic currents, after being down-converted by the PMIX, affect the current gain and linearity of the PMIX.

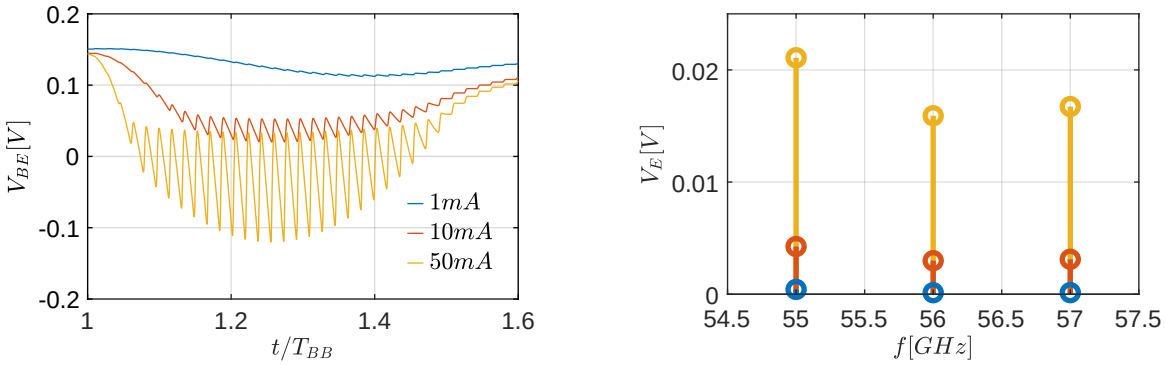
The dependence of V_E on I_{DDRM} is the result of the limited speed at the emitter node and subsequent slewing of the emitter voltage. As could be expected from Fig. 2.6, a significant amount of current may be required to (dis)charge the C_{BE} of the inactive device. This current can be delivered from the supply via the active device, which causes the waveform of the collector currents to strongly deviate from the ideal square wave-like shape [26]. Moreover, the charge dump from the C_{BE} of the inactive device can be so large that the collector current of the active device drops to zero. In this case, C_{BE} can only be discharged by the tail current source. As this source provides a fixed current I_{DDRM}, the charge/discharge speed of the emitter node is limited by the slew rate, given by:

$$SR = \frac{I_{DDRM}(t)}{C_{par}} \tag{3.10}$$

In Fig. 3.12, which shows the emitter voltage during one period of the baseband signal, the slewing behaviour and its dependence on the baseband current I_{DDRM} can be clearly observed. The waveform in Fig. 3.12 shows a high similarity to a modulated sawtooth wave, rather than the modulated, rectified sine wave from Fig. 2.6. An approximation of the required I_{DDRM} to prevent slewing can be found by calculating the average current required to charge C_{par}, in order for the emitter voltage to move between its ideal, extreme values (see Section 2.3). The result is given by:

$$I_{DDRM} = 8 V_{e,pk-pk} C_{par} f_{LO} \tag{3.11}$$

At the current level given by Eq. 3.11, the DDRM delivers enough current to (dis)charge C_{par} from/to the extreme values depicted in Fig. 2.6, within the time interval $T_{LO}/4$.



(a) Transient of V_E

(b) Spectrum of V_E

Figure 3.12: Emitter voltage characteristic of SB mixer, suffering from a constant C_{BE} of 2 pF. The mixer is driven by a 1 GHz Class B input current with its amplitude varying between 1-50 mA and a LO voltage swing of 0.9 V.

To describe the slewing effect and, more importantly, its relation to I_{DDRM}, V_E will be approximated using a sawtooth wave. The fundamental component of a sawtooth wave is given by the peak-peak swing of the waveform, divided by π. As a result, V_E could be approximated by Eq. 3.12a. Note that the phase of the sawtooth approximation of V_E is directly related to the phase LO, and the V_E frequency is twice f_{LO}. The intermodulation products of V_E and I_{DDRM} however, arise from a change in V_E as a result of a change in I_{DDRM}. The linearization of this dependency is given by Eq. 3.12b.

$$V_E\left(2f_{LO}, t\right) = -\frac{I_{DDRM}\left(t\right)}{2\pi f_{LO} C_{par}} \sin\left(2\omega_{LO} t\right) \tag{3.12a}$$

$$\frac{\partial V_E\left(2f_{LO}, t\right)}{\partial I_{DDRM}\left(t\right)} = -\frac{1}{2\pi f_{LO} C_{par}} \sin\left(2\omega_{LO} t\right) \tag{3.12b}$$

The relation given in Eq. 3.12b results in intermodulation terms appearing in the V_E spectrum at the frequencies $2f_{LO} \pm f_{BB}$. These components are translated into (common-mode) currents flowing from the emitter node to the ground via the total capacitance connected to the emitter node (i.e. C_{par}). The current flowing through C_{par} is defined as the parasitic current I_{par}. At the frequencies $f_{LO} \pm f_{BB}$, I_{par} is given by:

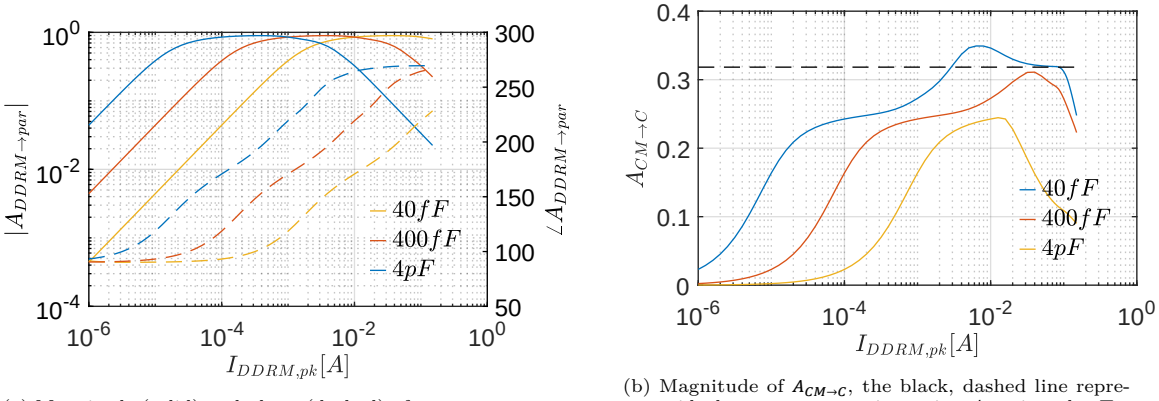
$$\begin{aligned} I_{par}\left(f_{LO} \pm f_{BB}, t\right) &= \frac{\partial}{\partial t}\left(2\pi C_{par}\left(2f_{LO} \pm f_{BB}\right) \frac{\partial V_E\left(2f_{LO}\right)}{\partial I_{BB}} \frac{I_{DDRM}\left(f_{BB}\right) \sin\left(\omega_{BB} t\right)}{2}\right) \\ &\approx -I_{DDRM}\left(f_{BB}\right) \sin\left(\left(\omega_{LO} \pm \omega_{BB}\right) t\right) \end{aligned} \tag{3.13}$$

An interesting conclusion from Eq. 3.13 is that the parasitic currents $I_{par}\left(f_{LO} \pm f_{BB}\right)$ and the input current fundamental $I_{DDRM}\left(f_{BB}\right)$ are identical of magnitude and opposite in phase.
The findings above were evaluated using an ADS simulation, in which external capacitors C_{BE} were applied to the ideal HBTs (modelled as explained in chapter 2) within an SB PMIX. The resulting conversion gain $A_{DDRM \to par}$, as defined in Eq. 3.14, is plotted in Fig. 3.13a.

$$A_{DDRM \to par} = \frac{I_{par}\left(2f_{LO} \pm f_{BB}\right)}{I_{DDRM}} \tag{3.14}$$

Besides a roll-off from the value given in Eq. 3.13 at small input current levels, also a roll-off at larger current input levels can be observed. For small input currents, the effects discussed in

Section 3.4.1 apply, meaning a large portion of the DDRM current (at the baseband frequency) flows into C_{par}, and very little current is up-converted by the switching core. The roll-off at large input currents is the result of a reduced accuracy of the sawtooth wave approximation of V_E. For larger input currents, V_E can follow its ideal, rectified sine wave shape more closely, and thus the dependency of V_E on I_{DDRM} diminishes. Therefore, the intermodulation of V_E and I_{DDRM} disappears, and less $I_{par}\,(f_{LO} \pm f_{BB})$ is generated. Additionally, the change in waveform shape also changes the phase alignment of $I_{par}\,(f_{LO} \pm f_{BB})$ and $I_{DDRM}\,(f_{BB})$.



(a) Magnitude (solid) and phase (dashed) of $A_{DDRM\to par}$

(b) Magnitude of $A_{CM\to C}$, the black, dashed line represents ideal current conversion gain $1/\pi$, given by Table 2.1.

Figure 3.13: The influence of C_{par} on parasitic current generation and gain associated with the switching action of an SB PMIX

Finally, the effect on $I_{par}\,(f_{LO} \pm f_{BB})$ on the current gain is considered. It is crucial to realize that the parasitic currents $I_{par}\,(f_{LO} \pm f_{BB})$ can only originate from the voltage supply connected to the collectors of the HBTs, before flowing into the ground via C_{par}. Consequently, $I_{par}\,(f_{LO} \pm f_{BB})$ is subjected to the frequency translation of the SB mixer cell. The down-conversion of $I_{par}\,(f_{LO} \pm f_{BB})$ and up-conversion of $I_{DDRM}\,(f_{BB})$ align their phases, resulting in the current gain expanding with respect to Table 2.1.
However, the slewing effect flattens the V_E waveform. As a result, the HBTs in the switching core are on for a shorter period of time than half of the LO period. Therefore, the collector current can no longer be calculated by multiplying the current flowing into the switching core with a square wave. At this point, it becomes complex to predict the behaviour of the SB PMIX using analytical tools.
To proceed, ADS is used to empirically find the current conversion gain from the (total) current drawn from the common-emitter node (defined as I_{CM}) to the collector currents ($i_{p,n}$), both at the respective frequencies of interest. This gain is defined in Eq. 3.15, and the result is shown in Fig. 3.13b.

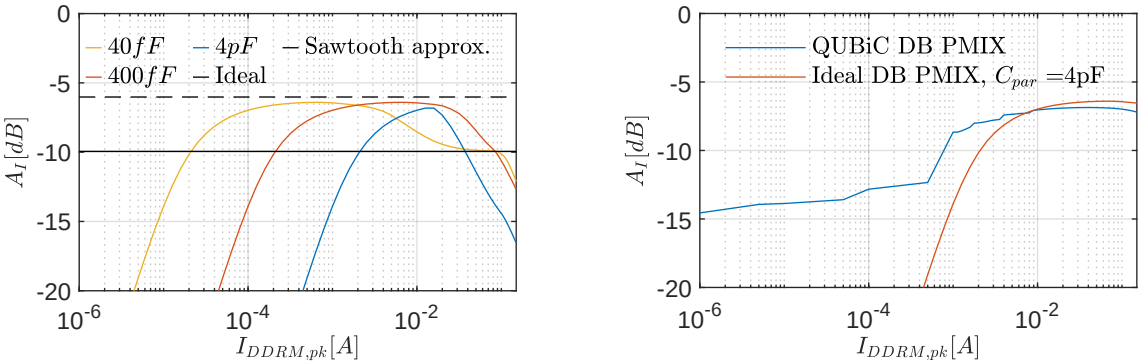
$$A_{CM\to C} = \frac{i_{p,n}\,(f_{LO} \pm f_{BB})}{I_{CM}} = \frac{i_p\,(f_{LO} \pm f_{BB})}{I_{DDRM}\,(f_{BB}) + I_{par}\,(f_{LO} \pm f_{BB})} \tag{3.15}$$

The current conversion gain in Fig. 3.13b is, approximately, 0.25 at the amplitude of the input current corresponding to the center of the curves in Fig. 3.13a. This point coincides best with the result obtained using the sawtooth wave approximation. This point is the most suitable to provide a conclusive result on the influence of C_{par} on the SB PMIX current conversion gain using the sawtooth wave approximation. Finally, using Eq. 2.2 as the definition for the current conversion gain, the following result is obtained:

$$|A_I| \approx \frac{0.25\left(I_{DDRM}\left(f_{BB}\right) + I_{par}\left(f_{LO} \pm f_{BB}\right)\right)}{I_{DDRM}\left(f_{BB}\right)} \approx -6.0\,\text{dB} \tag{3.16}$$

Fig. 3.14 shows the current conversion gain of a SB PMIX for various values of C_{par}, simulated using ADS. Depending on the value of C_{par}, the curves shown in Fig. 3.14 can be split in the following four regions:

1. At small I_{DDRM}, A_I is rising due to the baseband effects discussed in Section 3.4.1.
2. At medium I_{DDRM}, A_I is constant, but expanded with respect to the ideal level (Table 2.1), as a result of the intermodulation mechanism at the common-emitter node.
3. At larger I_{DDRM}, A_I drops as the intemodulation effect on the common-emitter node diminishes. If C_{par} is sufficiently small, A_I returns to its ideal level.
4. At very large I_{DDRM}, A_I drops dramatically due to hard compression.



(a) Current conversion gain for various C_{par}, black dashed lines indicate the ideal level and the level predicted by the sawtooth wave approximation of V_E

(b) AM-AM of a DB PMIX implemented in the QUBiC Gen8 technology (simulated in Cadence) and a DB PMIX with a fixed C_{par} of 4 pF (simulated in ADS)

Figure 3.14: Current conversion gain of SB (left) and DB PMIX (right) suffering from parasitic capacitances at the emitter node.

In Fig. 3.14b, the theory discussed in this section is compared to the current conversion gain of a DB PMIX, which is constructed using QUBiC Gen8 EHV BNP devices sized according to Section 3.1. To remove any influence of the device output impedance on the mixer linearity (Section 3.3), the load was set to 0 Ω. This eases the investigation of the discussed common-emitter intermodulation in a PMIX made using QUBiC Gen8 devices. Except for the region associated with small input currents, the shape of the QUBiC mixer resembles the predicted behaviour quite accurately.

3.5. Conclusion

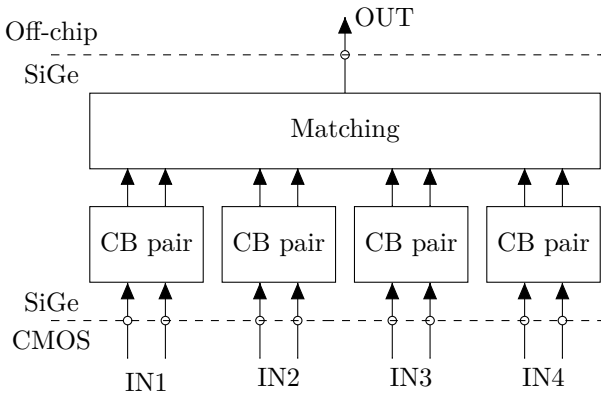
This chapter presented the device non-idealities that will pose the main design challenges during the design process of a current-mode front-end. In order to generate a high output power, a large supply voltage is preferred. For this reason, the conditions that determine the voltage-handling capabitlities of the QUBiC Gen8 EHV BNP device were discussed in Section 3.2. Section 3.1 showed that large device sizes are required in order to handle the large currents provided by the DDRM. Unfortunately, a large device come with an increase in parasitic effects, such as a drop in the output impedance of the device (Section 3.3). Finally, Section 3.4 elaborately studied an intermodulation effect associated with the capacitances at the common-emitter node of an SB PMIX. This intermodulation effect resulted in the current conversion gain expanding with respect to the ideal level predicted in Section 2.1, at the risk of linearity degradation.

4

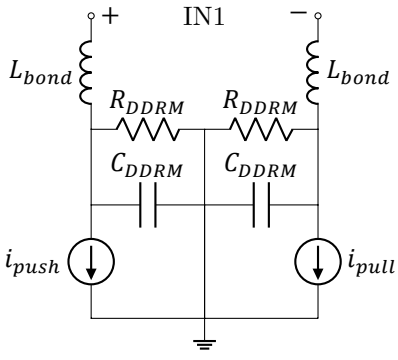
Current-Mode Power Amplifier Design

For the 2.4 GHz current-mode front-end concept, a PA IC was designed, taped and tested. This chapter elaborates on both the design and the simulated/measured perforances of this IC. A block diagram of the PA IC is shown in Fig. 4.1a. This figure shows that the two main building blocks of the PA are the four differential CB pairs and the matching block.

Fig. 4.1b shows the model for the DDRM current source used throughout this chapter. The components R_{DDRM} (10 kΩ) and C_{DDRM} (1.5 pF) represent the output impedance of the DDRM itself, while L_{bond} represent the inductance of the bonding wires. To minimize the detrimental effect of the bonding wires on the system stability and the current transfer to the PA, the CB pairs are aligned with the four DDRM outputs, each spaced 522 µm apart.
In Section 4.1, the design of the differential CB pairs is discussed. As chapter 3 already explained the main design challenges arising from device non-idealities, this chapter focuses more on the practical approach to these challenges. The 'Matching' block from Fig. 4.1 is implemented by a parallel-combining transformer (PCT) implements. The design considerations and characteristics of the PCT balun are introduced in Section 4.2.
The performance of the resulting PA design is presented in Section 4.3. Before continuing the discussion of the building blocks of the PA, it should be emphasized that the PCT and the CB pairs are co-designed. This is done because the inductive nature of the balun plays a big role in the overall circuit stability, and any compensation for instability is incorporated in the design of the CB pairs. As discussed in chapter 3, additional resistance in the base path of the transistors



(a) Block diagram of the CB PA core



(b) DDRM model used to drive each of the four input channels of the PA

Figure 4.1: Simplified diagram of the DDRM-PA current-mode front-end

reduces the breakdown voltage, which in turn affects the load required for a loadline match and thus the design of the balun. These effects make that the design flow of the PA needs to be iterative, as is illustrated in Fig. 4.2.

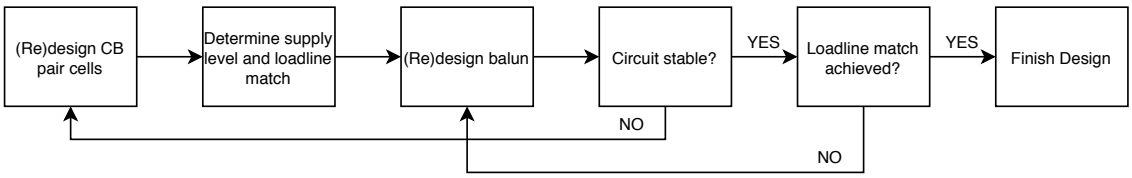
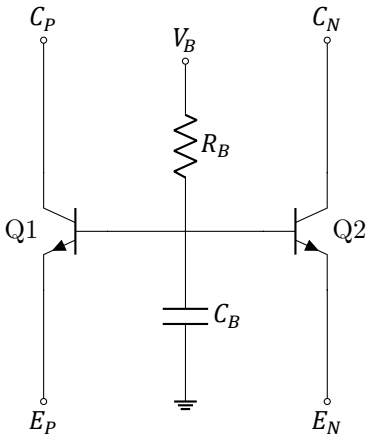


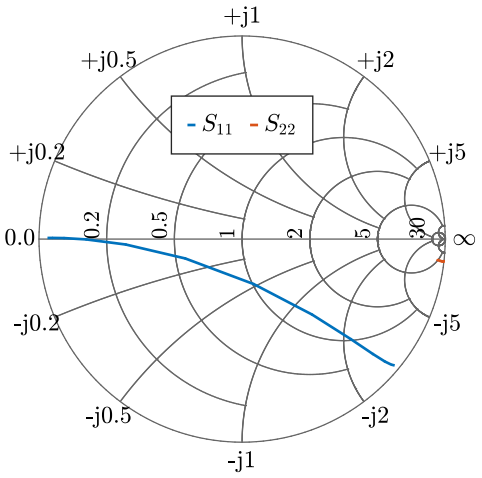
Figure 4.2: Design flow of the PA IC

4.1. Differential CB Pair Design

This section explains the design considerations of the four CB differential pairs within the PA, which mainly concern system stability and the prevention of avalanche breakdown.
Fig. 4.3a shows the circuit diagram of a single differential CB pair. The transistors $Q1$ and $Q2$ are implemented by two QUBiC Gen8 EHV BNP devices, which are sized such that their maximum f_T corresponds to a collector current value of $100\,\mathrm{mA}$ (in accordance with the DDRM specifications, see Table 1.1). To show the dependence of the input (and output) impedance of the CB pair on the collector current, S_{11} And S_{22} are plotted in Fig. 4.3b.



(a) CB differential pair, including stabilization network

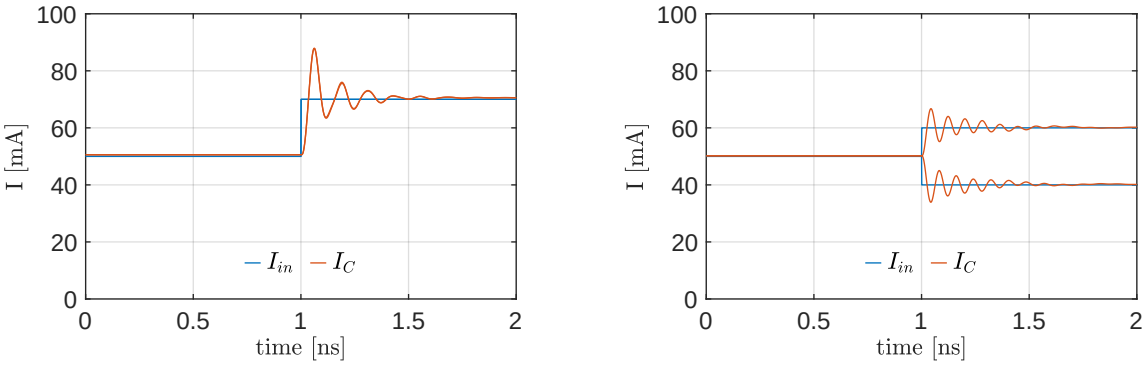


(b) S_{11} and S_{22} of differential CB pair

Figure 4.3: Schematic and S-parameters of CB pair at $2.4\,\mathrm{GHz}$ for collector current levels between $10\,\mu\mathrm{A}$, for which S_{11} lies near right hand side of unity circle, and $100\,\mathrm{mA}$, for which S_{11} lies near -1.

On a system-level, the large parasitic capacitances, gain and f_T of the active devices, combined with the (large) inductances of the PCT and the bonding wires, create a perfect environment for undesired oscillations. Two loops are especially problematic: the loop created by any inductance present at the base (bonding wire), C_{BE} and C_{DDRM}, and secondly the LC-tank created by the PCT and C_{BC}. An R_B of $12.5\,\Omega$ was added in the base bias path to provide some damping for these unstable loops. However, as shown in [31], a resistance of hundreds of ohms would be required to fully stabilize this circuit. This highlights an unfortunate trade-off between output power and

stability, as a large R_B lowers the device breakdown voltage and thus P_{max} and η_{sys}.
Luckily, stable operation can also be achieved by placing a large decoupling (MIM) capacitor C_B close to the base terminals of the devices [31]. This approach also succeeds in breaking the unstable loops and maintains the maximum allowed voltage swing across the devices. Therefore, besides mentioned R_B of 12.5 Ω, a C_B of 10 pF was used in the CB cell design (as depicted in Fig. 4.3a). The circuit stability was evaluated by examining the step response of the PA (Fig. 4.1). This test provides a quick, direct and definite conclusion on circuit stability. The result of a common-mode (CM) and differential-mode (DM) input step is shown in Fig. 4.4. The small, damped oscillations that are still left in the response originate from the small bonding wire inductance at the emitter nodes (Fig. 4.1b) as well as the limited damping provided by R_B.



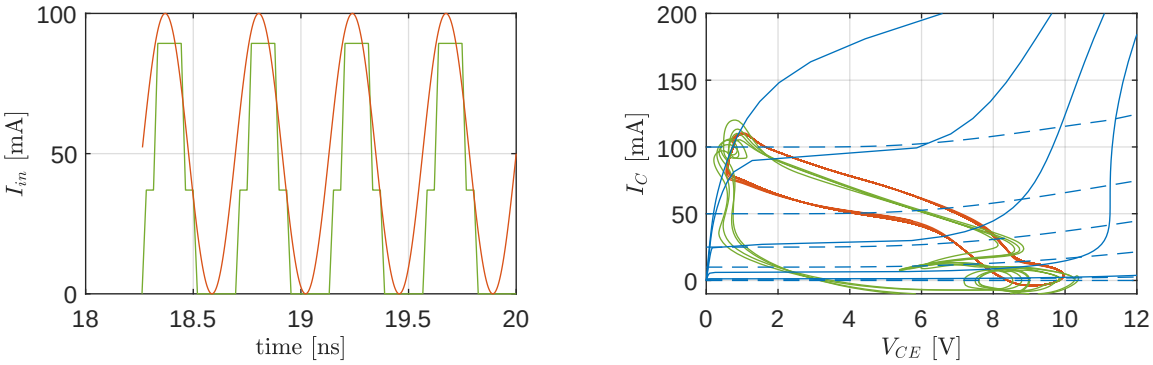
(a) Common-mode step response.

(b) Differential-mode step response

Figure 4.4: PA response a common-mode and differential-mode step input current.

Fig. 4.5 shows the loadline of a BNP device for two different input current waveforms: a class A waveform and a digital class B waveform, which more closely resembles the current waveform provided by the DDRM. From this figure, three important aspects can be distinguished:

1. The loadlines display asymmetric looping, especially the class B drive, indicating significant complex loading by the balun.
2. Current overshoot is visible around the saturation region in Fig. 4.5b, a result of the limited damping in the resonant loops in the PA.
3. For both drives, the device operation remains below the breakdown conditions.



(a) Single-tone current signals flowing from the DDRM

(b) Corresponding loadlines at the CB collector nodes

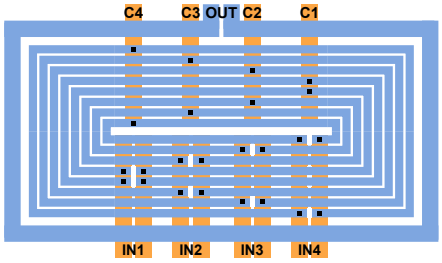
Figure 4.5: Loadline characteristics of the CB PA (including PCT) driven by class A and digital (harmonic-rejected) class B current waveforms with identical fundamental components. In blue, the DC (dashed) and RF (solid) I_C vs. V_{CE} characteristics of the CB stages are shown.

4.2. PCT Balun Design

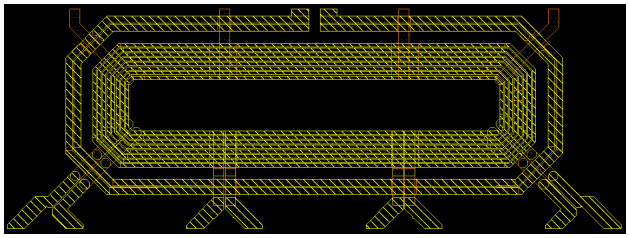
Combining the power of the outputs of the CB pairs is implemented using a parallel-combining transformer (PCT) that also fulfils the balanced-to-unbalanced operation. In this section, the PCT balun topology, detailed design and performance will be presented.

In contrast to many other IC designs, the available area for the balun is not a limiting factor in this project. The wide spacing (522 µm) of the CB pairs already requires a wide strip of silicon area and thus a wide balun is not considered to be problematic. Moreover, a narrow (small) balun design would create a strong asymmetry in the interconnection of the four CB pair collector nodes and their respective PCT input ports and is therefore not preferred. This makes A PCT topology as proposed in [32] undesirable, as the signal feeds of this transformer are placed at different sides of the transformer. A large, strongly interwound balun layout, as proposed in [33], [34] and [35], makes it increasingly difficult to tune the PCT dimensions. Therefore, given the limited time available for this project, these topologies are also not preferred.

A diagram of the topology of choice for the PCT is given in Fig. 4.6a. In the used topology, the primary winding lies entirely within the secondary winding, allowing for easy modification of both the distance between the two inductors and the size of the inductors itself. As the primary and secondary windings do not overlap, capacitive coupling between the input and output is also minimized. The spacing between the four input ports, connected to the primary winding, is tailored to the spacing between the CB pairs. However, the windings on the primary winding suffer from strong mismatch in inductance. In order to alleviate this issue, two inductors are used for every input port, each with identical spacing to the center line of the primary winding collection. As a result, eight inductors are required on the primary side, rather than four.



(a) Simplified topology diagram of PCT balun



(b) Cadence layout diagram of PCT balun (1786 µmx639 µm)

Figure 4.6: Layout diagrams of the PCT balun

The more detailed design choices for the PCT balun were motivated by three main objectives: achieving the bandwidth requirement (N4, Section 1.3), presenting a loadline match to the CB pairs and minimizing the losses within the balun. The design process of the balun will be illustrated using the transformer model shown in Fig. 4.7. By varying the different parameters of the transformer shown in Fig. 4.7, their impact on the transfer and impedance characteristics can be investigated. Throughout the investigation, default values that result in characteristics similar to the resulting balun apply: L_1 =1.13 nH, L_2 =2.12 nH, k =0.3, C_{in} =10 pF and C_{out} =6 pF.

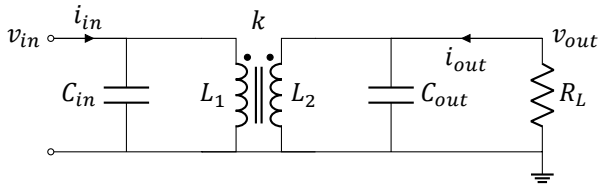
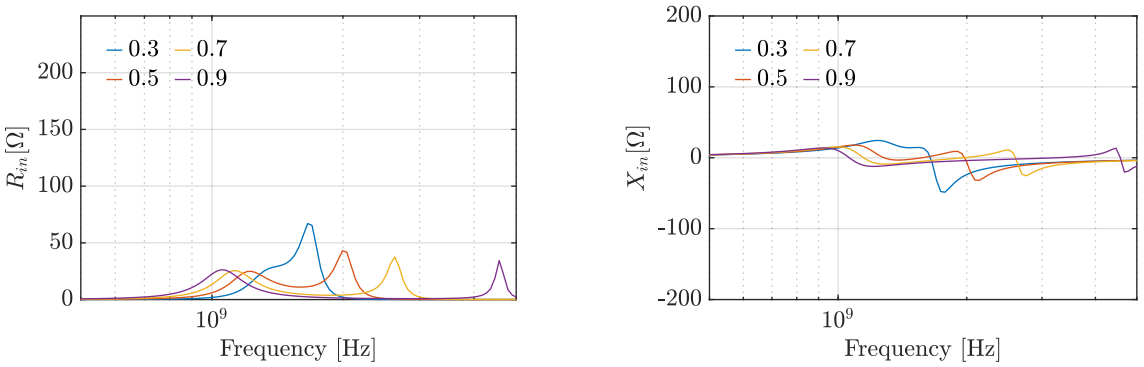


Figure 4.7: Simplified schematic of a transformer-based matching network.

First, it will be considered how wideband transfer can be achieved. As shown in Fig. 4.8 and [36], the bandwidth of a transformer can be controlled by tuning the coupling factor k. By changing the separation between the primary and secondary winding, various values of k can be achieved. A large k results in the widest bandwidth as well as an increased separation of the two resonant frequencies of the transformer. The selected balun topology however, suffers from an relatively small k, as the windings do not overlap and the innermost primary windings lie relatively far from the secondary winding. Fortunately, there is an approach to alleviate the bandwidth penalty resulting from the low k of this low topology. As k decreases, the bands around resonant peaks move towards each other and will eventually merge. This behaviour can be exploited to restore the transformer bandwidth and thus to achieve wideband transfer.

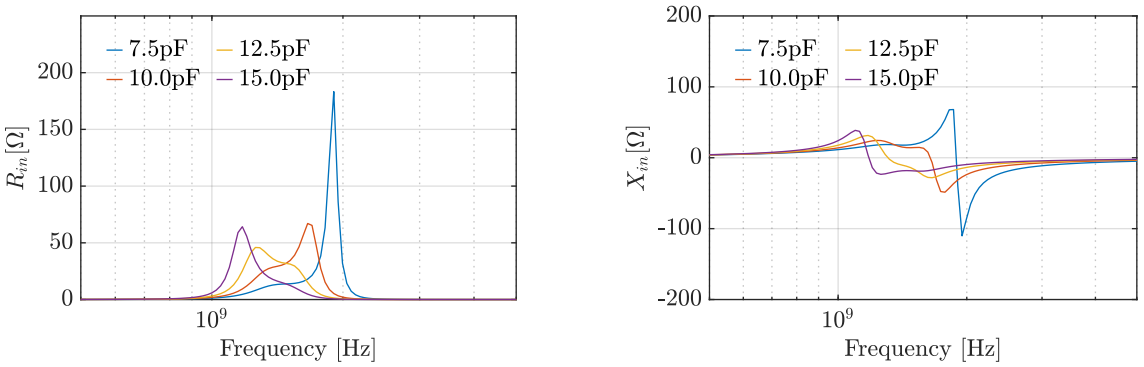


(a) Input resistance of the transformer for different k

(b) Input reactance of the transformer for different k

Figure 4.8: Input Impedance of the transformer for different k, when driven by an ideal AC current source

Using the capacitance C_{in} (and/or inductance L_1), the input impedance can be controlled around the resonant peaks. By carefully tuning these parameters, a flat, in-band (loadline) match can be achieved. Additionally, the parameters at the primary side (C_{in} and L_1) can be used to shift the center frequency of the pass-band, by changing the location of the resonance peak corresponding to the LC-tank at the input side. Both of the aforementioned effects are visible in Fig. 4.9. As a result of the asymmetry of the selected PCT topology, there will be a mismatch between the inductances connected to the four input ports, and so different values of C_{IN1-4} are needed.



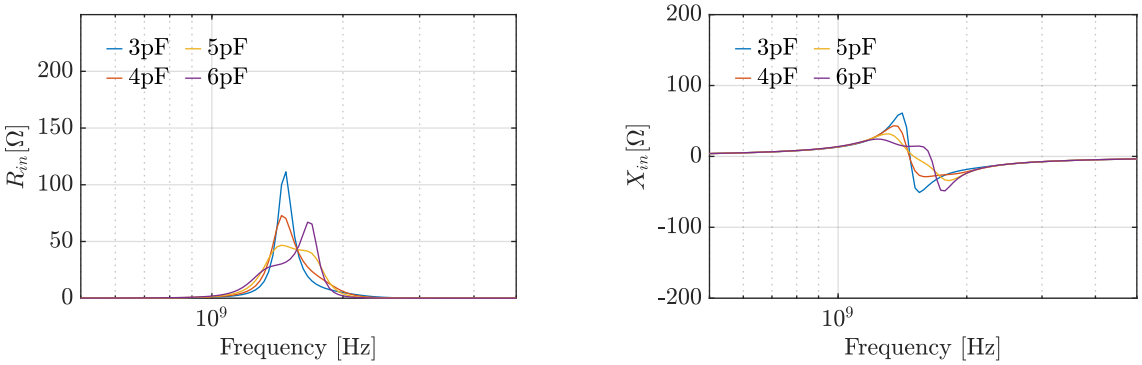
(a) Input resistance of the transformer for different C_{in}

(b) Input reactance of the transformer for different C_{in}

Figure 4.9: Input Impedance of the transformer for different C_{in}, when driven by ideal AC current source

The input impedance can also be controlled by tuning the parameters at the output side: C_{out} and L_2. As is visualized in Fig. 4.10, the location of the pass-band center frequency is less sensitive

to the parameters at the secondary side.



(a) Input resistance of the transformer for different C_{out}

(b) Input reactance of the transformer for different C_{out}

Figure 4.10: Input Impedance of the transformer for different C_{out}, when driven by ideal AC current source

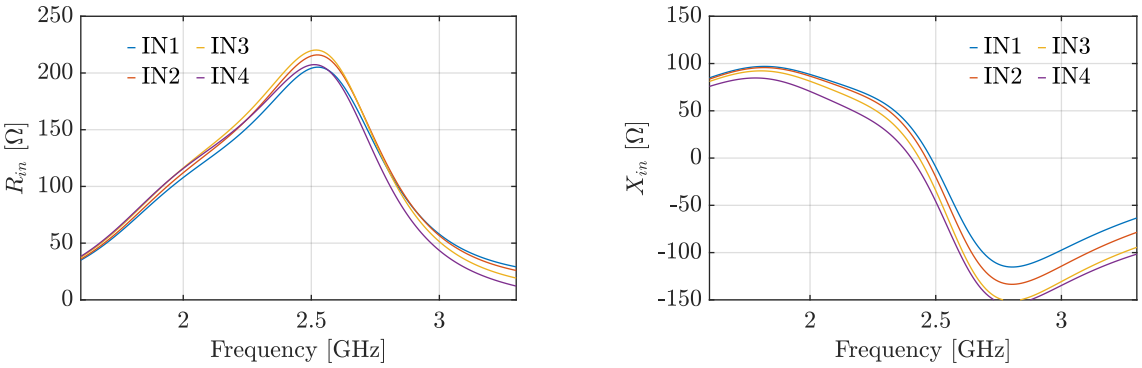
For the actual PCT balun design, the multi-port behaviour must be taken into account The magnetic interaction between the four coils on the primary side affects the observed input impedance at all inputs. As a result of the power combination, the voltage swing and thus the input impedance at the input ports is increased. Furthermore, the primary coils magnetically couple with each other, which also contributes to the complexity of the design process. This results in an iterative design process of the PCT balun. The final design is shown in Fig. 4.6b. The (extracted) parameters of the balun, corresponding to the those depicted in Fig. 4.7, are given in the tables below. Fig. 4.11 shows the input impedance of all four input ports.

Table 4.1: Winding inductances, coupling factors and capacitances of the PCT balun

Winding	[nH]
L_{IN1}	5.0
L_{IN2}	4.7
L_{IN3}	4.4
L_{IN4}	4.0
$L_{IN,tot}$	1.1
L_{out}	2.1

Coupling factor	
k_{IN1}	0.29
k_{IN2}	0.37
k_{IN3}	0.45
k_{IN4}	0.54
$k_{IN,tot}$	0.31

Capacitance	[pF]
C_{IN1}	0.6
C_{IN2}	1.6
C_{IN3}	2.6
C_{IN4}	3.6
C_{out}	6.0

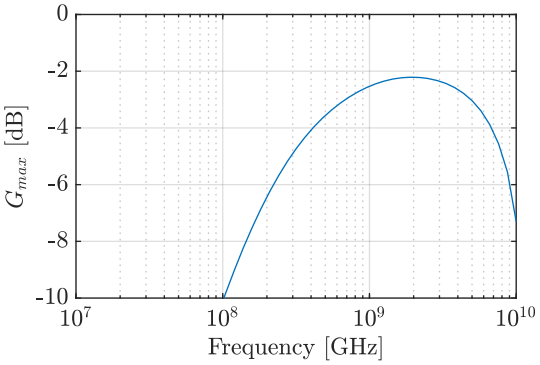


(a) Input resistance of the four balun input ports

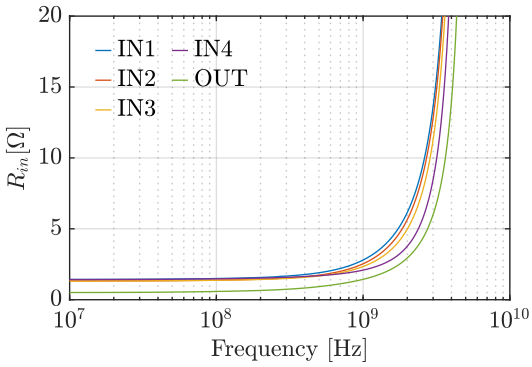
(b) Input reactance of the four balun input ports

Figure 4.11: Input Impedance of the four balun input ports, when all driven by ideal AC current sources

The resistive losses of the PCT balun were minimized using two measures: the parallel use of metal layers M4-M6 in the layout of all windings, and an appropriate design of width of these metal layers. Using the the sheet resistance of the metal layers provided by [37], the width of the windings can be chosen such that the resistive losses in the coils does not exceed 1 dB.
The resulting losses of the balun are plotted in Fig. 4.12, which shows the maximum gain G_{max} of the balun as well as the resistance of the balun itself. Unfortunately, the losses are larger than expected. This will be further discussed in chapter 6.



(a) G_{max}, simulated by shorting the four input ports IN1-4, such that the five-port network collapses into a two-port network.

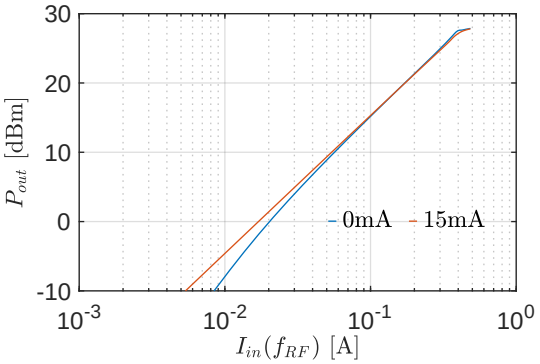


(b) Input resistance of the balun at IN1-4 (OUT left open) and OUT (IN1-4 left open)

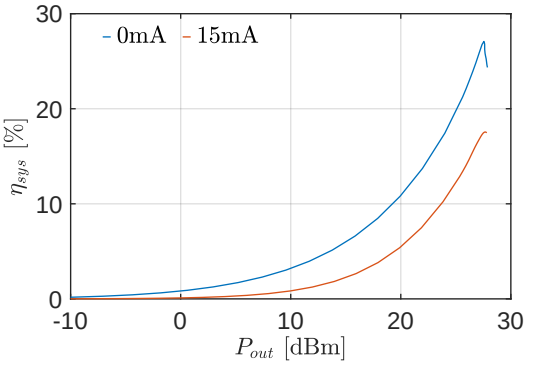
Figure 4.12: Overview of (resistive) losses of the PCT balun

4.3. Results

This section presents the simulated as well as the measured performance of the CB PA. The peak efficiency, bandwidth and AM-AM conversion of the PA were determined using two different continuous wave (CW) sweeps. Additionally, a two-tone power sweep was performed in order to simulate the linearity of the CB PA.
In Fig. 4.13, the simulated performance of the CW power sweep is shown. This simulation was performed by sweeping the amplitude of a digital, 2.3 GHz class B current waveform (including harmonic rejection, see Fig. 4.5a). Without any quiescent current, the peak power efficiency of the CB PA is 27.0 %. However, as it will turn out, some quiescent current is needed in order to linearize the PA, especially when producing very little output power. When a quiescent current of 15 mA is drawn from every CB stage, the peak power efficiency drops to 17.5 %.



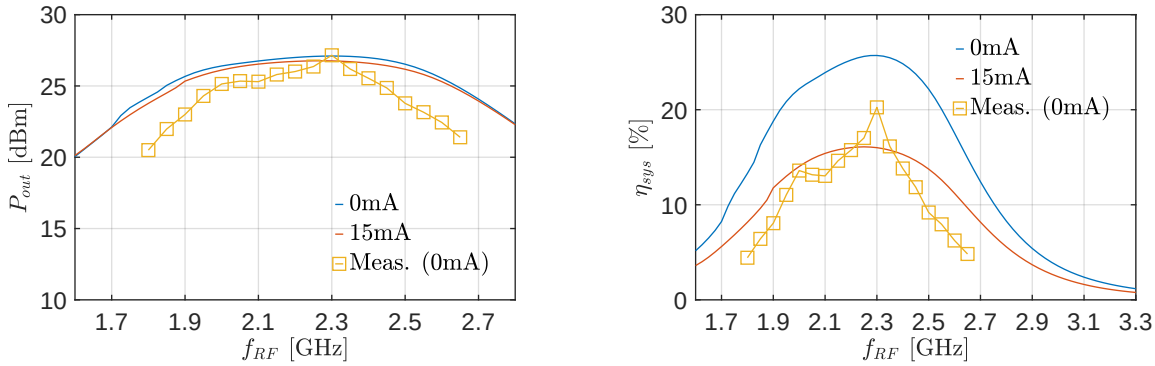
(a) Output power of the CB PA



(b) System efficiency of the CB PA

Figure 4.13: Output power and system efficiency of the CB PA, determined using a CW power sweep for two different quiescent current levels.

Fig. 4.14 shows the results of the CW frequency sweep simulation. The center frequency of the pass-band of the PA lies at 2.3 GHz rather than the required 2.4 GHz. The −3 dB frequencies lie at 1.8 GHz and 2.7 GHz, yielding a 3 dB-bandwidth of 900 MHz. As a result of the bandwidth being well beyond the required value, the offset in center frequency is not a problem. The yellow data points in Fig. 4.14 give the measured output power and efficiency of the DDRM-PA combination versus operation frequency. The measured maximum output power matches closely matches the value found by simulations, although the measured bandwidth is smaller (1.9 GHz- 2.5 GHz). The latter could be attributed to layout parasitics (e.g. ESD protection and bond pads) that were not taken into account in the simulations. The measured power efficiency is lower due to the fact that the DDRM leakage current (Section 1.1) is not taken into account in the simulated results. A much sharper decay of power efficiency is observed as the frequency moves away from the 2.3 GHz, which is the result of the decreased bandwidth with respect to the simulated performance.

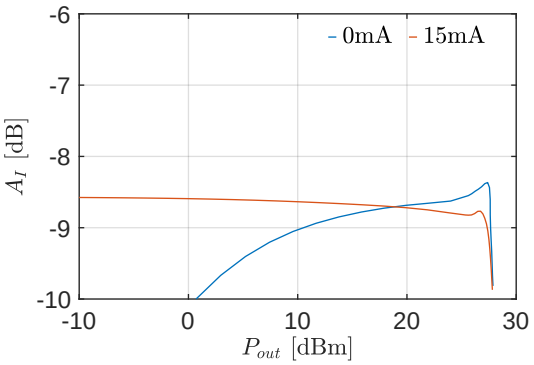


(a) Output power of the CB PA

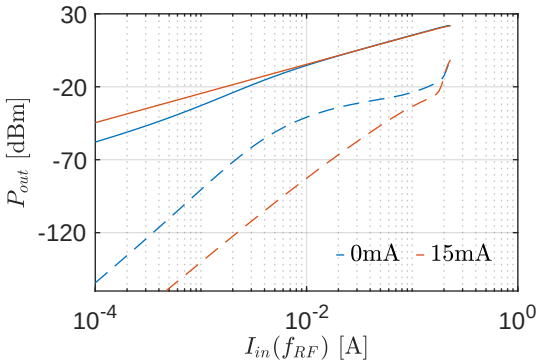
(b) System efficiency of the CB PA

Figure 4.14: Output power and system efficiency of the CB PA determined using a CW frequency sweep.

The simulated linearity performance of the CB PA is presented in Fig. 4.15. The AM-AM conversion characteristic of the PA (Fig. 4.15a,) clearly shows the need for a quiescent current. When no quiescent current is used, the input impedance of the CB stage is relatively large at lower input current amplitudes (i.e. low P_{out}) resulting in increasingly low gain and highly nonlinear behaviour. The AM-AM conversion shows that the CB PA is potentially linear up to the hard compression edge, provided that the appropriate quiescent current level is used. A more quantitative metric of linearity is provided by a two-tone test. This is shown in Fig. 4.15b, where the fundamental power and IM_3 level is plotted versus the total input current at the frequency of 2.3 GHz.



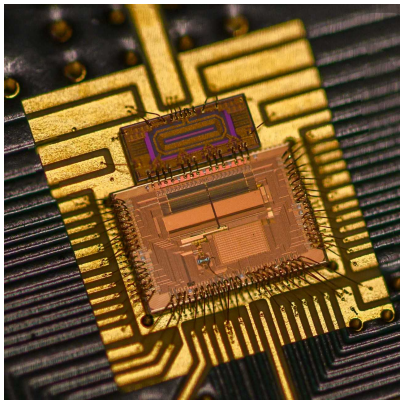
(a) AM-AM conversion, showing the point of hard compression



(b) Fundamental power and IM_3 power for a two-tone power sweep with a frequency spacing of 10 MHz

Figure 4.15: Linearity performance of the CB PA, both without quiescent current and a quiescent current of 15 mA.

Finally, the ACPR of the DDRM-PA combination was measured, using a 64-QAM input signal, and a total quiescent current of 100 mA (12.5 mA per CB stage). The result of this measurement is presented in Fig. 4.16b, showing an ACPR of −33.07 dB c. Clearly, the linearity of the current-mode PA could be improved.



(a) Photo of the bonded DDRM (bottom die) and PA (top die) combination

(b) ACPR with a total quiescent current of 100 mA

Figure 4.16: Die photograph and measured ACPR

4.4. Conclusion

This chapter presented the IC design of a CB PA core for a current-mode front-end concept operating at 2.4 GHz. The DDRM driving the PA core delivers its current in four parallel channels. The PA core therefore consists of four parallel, differential CB pairs, aligned with the DDRM output ports to minimize penalties arising from interconnect parasitics. The outputs of the four CB pairs were combined using a PCT balun. The topology of this PCT balun allows for quick prototyping, but suffers from increased asymmetry between its input ports compared to other PCT designs. Additionally, the losses of the PCT balun turned out to be higher than expected.
The simulated 3 dB-bandwidth of the resulting DDRM-PA front-end yields 900 MHz at a center frequency of 2.3 GHz, whereas the measured 3 dB-bandwidth was 600 MHz at the same center frequency. The simulated peak system efficiency of the DDRM-PA current-mode front-end, without any quiescent current, is 25 %, while this is only 20 % for the prototype. An ACPR of −33.07 dB c was reported, for a quiescent current of 100 mA.

5

Current-Mode Power Mixer Design

This chapter explores the design space of the mm-wave current-mode front-end concept, in which the DDRM signal is up-converted by a PMIX to the center frequency of 28 GHz. Because there was no tape-out for the PMIX concept, the emphasis was put on the design of the individual mixer cells, which are visualized in Fig. 5.1. The DDRM model used for this chapter is identical to that of Fig. 4.1, although the inductances modelling the effects of the bonding wires are omitted.

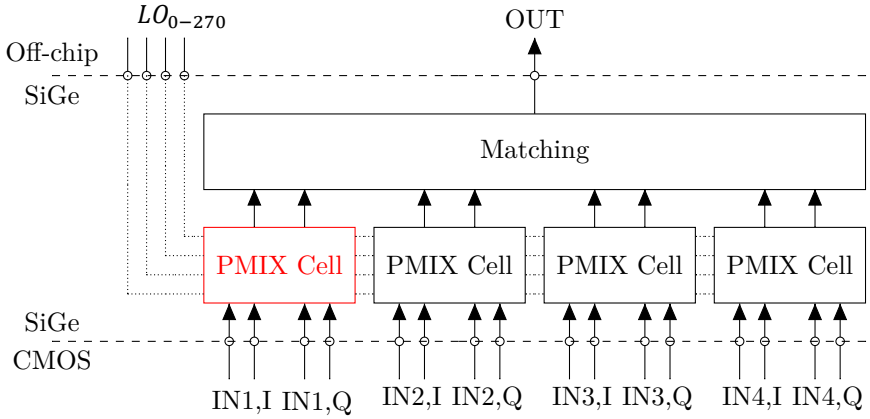


Figure 5.1: Simplified diagram of the DDRM-PMIX current-mode front-end. In red: scope of this project for the PMIX design.

The power efficiency design goal (Section 1.3), leads to a class B-like current waveform being the preferred mode of driving the PMIX. However, as was discussed in chapter 3, the combination of this clipped waveform and the presence of parasitic capacitances at the common-emitter node results in a pronounced intermodulation mechanism that affects the current conversion gain of the PMIX. With linearity being the primary performance criterion for a current-mode front-end, special attention was given to mitigate this source of linearity degradation during the design process.
This chapter is divided in three main parts. Section 5.1 introduces different design techniques that could potentially enhance the current-mode PMIX linearity. These techniques include conventional methods such as class A/B biasing and impedance matching, but also a novel architecture for an SB mixer cell. The implementation of these linearization techniques in the QUBiC Gen8 technology is discussed in Section 5.2. Finally, the practical effectiveness of the different (combinations of) linearization techniques are evaluated in Section 5.3.

5.1. PMIX Cell Linearization Techniques

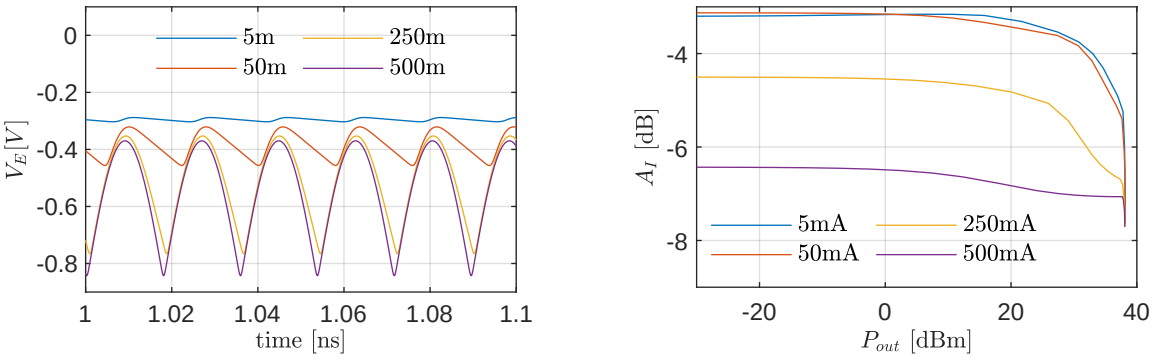
In this section, four concepts that potentially enhance the linearity of the current-mode PMIX are discussed. First, the considerations of using a cascode stage to load the PMIX are briefly discussed. The other three concepts are aimed to alleviate the effects of the C_{BE} capacitor, the main culprit of the intermodulation mechanism at the common-emitter node. The most straightforward of these concepts is biasing the PMIX in class A/B. The second method is to create an harmonic open condition at the second harmonic of the LO frequency, and positioned between the common-emitter node and the bases of the HBTs. The third presented technique is the use of a quasi-subharmonic (QSH) mixer architecture. This novel mixer architecture will be implemented on the SB mixer cell level (see Fig. 1.8) and does not exhibit any harmonic content at $2f_{LO}$ on its common-emitter node, thus omitting the intermodulation mechanism around $2f_{LO}$.
The concepts discussed in this section will be explained in the context of mixer cells that consist of ideal BJT devices, but with an externally applied C_{BE}. This make sure that the effects arising from C_{BE} are the only non-idealities present in the system, and thus allows for a clear view on the matter. The figures used to illustrate the concepts are created using ADS simulations of the mixer cells. By default, an $I_{DDRM,max}$ of $1\,\mathrm{A}$, V_{CC} of $10\,\mathrm{V}$, LO swing of $0.5\,\mathrm{V}$ and C_{BE} of $2\,\mathrm{pF}$ were used in these simulations.

5.1.1. Cascoding

In Section 3.3, it was shown that the output impedance of an SB mixer cell rapidly decreases with frequency. The output impedance is further lowered by the fact that four SB mixer cells are connected to the output node of an SSB PMIX (Fig. 1.8). As the output current is divided between the load R_L and the output impedance of the mixer, the current gain drops, and so does the output power. Furthermore, as was shown in Fig. 3.10b, the output impedance also drops significantly as the collector current grows. It is realistic to expect that this, will result in gain compression, as the input current from the DDRM increases. This becomes even more likely if the effect of finite device output impedance on the current transfer could not be neglected to begin with.
These issues could be alleviated by loading the switching core with a cascode stage. This approach would increase the output impedance of the overall PMIX (now including the cascode), while the low input impedance of a cascode stage can be easily driven by the switching core itself.
However, the placing of a cascode would come at the cost of increased power dissipation. This is both due to a higher required supply voltage and, as seen in Section 4.3, a significant quiescent current is needed in order to linearize the CB stage.

5.1.2. Biasing

In chapter 3, it was explained that the intermodulation mechanism at the common-emitter node of the PMIX originates from the fact that the emitter voltage cannot keep up with its ideal waveform, which has a fundamental frequency of $2f_{LO}$ and a voltage swing close to V_{LO}. By applying a quiescent current, which changes the bias condition from class B to class A/B or even class A, the C_{BE} parasitics can be (dis)charged more quickly and the speed of the common-emitter node is increased. Furthermore, this additional charge is not related to the signal, and so the intermodulation effect of the common-emitter voltage component at $2f_{LO}$ and the input signal fundamental vanishes.
However, Eq. 3.11 estimates that large devices require quiescent current levels of hundreds of mAs to (dis)charge their C_{BE} at mm-wave frequencies. This is also confirmed by Fig. 5.2, which shows the result of a CW power sweep of a $28\,\mathrm{GHz}$ SSB PMIX.



(a) Emitter voltage

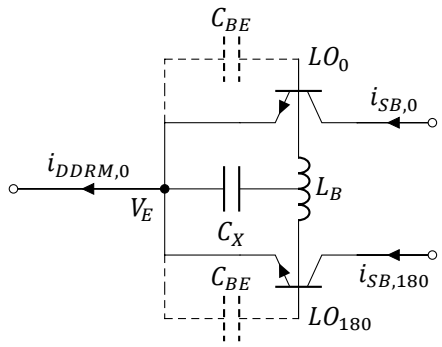
(b) AM-AM conversion

Figure 5.2: Emitter voltage and AM-AM conversion of SSB PMIX, biased using different quiescent currents with a C_{BE} of 2 pF present at every BJT.

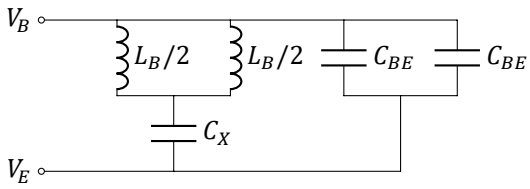
5.1.3. Resonating Out the Common-Emitter Node Capacitances

Another approach to prevent the intermodulation mechanisms on the common-emitter node is to resonate out the low, capacitive impedance present on the common-emmitter node. This can be achieved by the SB mixer design shown in Fig. 5.3.

The inductor L_B, although not shown previously, should also be used in a standard SB mixer cell to minimize the current drawn from the LO source. If L_B is chosen according to Eq. 5.1a, the resonant frequency of the circuit as seen by the LO sources is placed at f_{LO}.



(a) Circuit schematic of SB PMIX cell resonating out the C_{BE} parasitics



(b) Common-mode circuit equivalent of Fig. 5.3a, with only the reactive components shown.

Figure 5.3: SB PMIX cell circuit with common-mode harmonic open at the common-emitter at $2f_{LO}$ and differential harmonic open between the bases

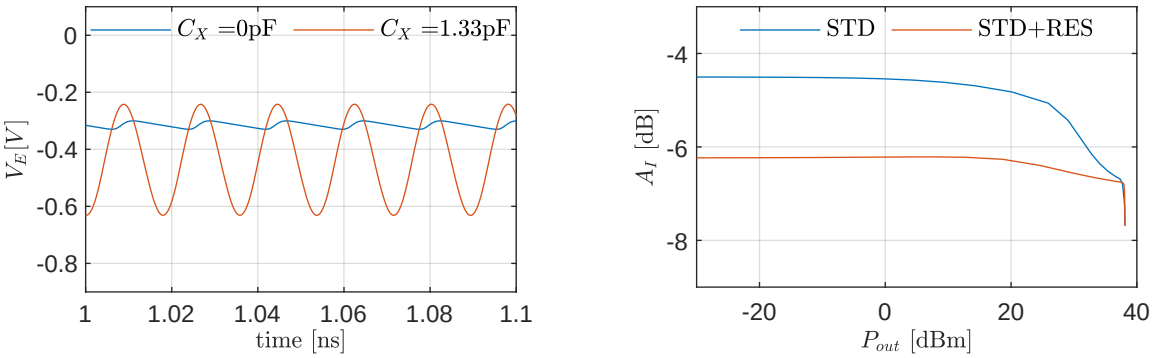
By placing the capacitor C_X, L_B can be incorporated in the common-mode loop that is present between the emitter node and the common-mode ground at the BJT bases. Note that this loop, schematically shown by Fig. 5.3b, is responsible for the slow speed of the common-emitter node and thus for the expansion of the current conversion gain, as explained in Section 3.4.

The capacitor C_X is connected to the center tap of L_B and will (ideally) not affect the impedance match for the LO port, as it the symmetry of the circuit is not not affected. If C_X is chosen according to Eq. 5.1b, the resonant frequency of the common-mode loop can be placed at the nth harmonic of f_{LO}.

$$L_B = \frac{2}{(2\pi f_{LO})^2 C_{BE}} \tag{5.1a}$$

$$C_x = \frac{2C_{BE}}{n^2 - 1} \tag{5.1b}$$

For $n = 2$, the current required to (dis)charge C_{BE} at the frequency $2f_{LO}$ will be provided by the LC-resonator formed by L_B and C_X (see Fig. 5.4a), rather than the by the DDRM, preventing the slewing effect. As the emitter voltage now becomes independent of the DDRM current, the generation of parasitic current components around $2f_{LO}$ is prevented, and thus the associated gain expansion is greatly reduced. This explanation is confirmed by Fig. 5.4b.



(a) Emitter voltage

(b) AM-AM conversion

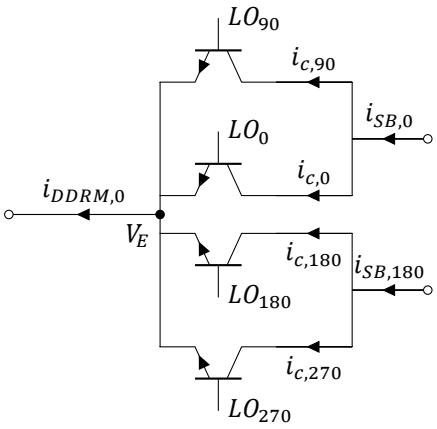
Figure 5.4: Emitter voltage and AM-AM conversion of an SSB PMIX both with and without an harmonic open condition at the common-base nodes to compensate for an (externally applied) C_{BE} of 2 pF present at every BJT.

5.1.4. Quasi-Subharmonic Mixer Architecture

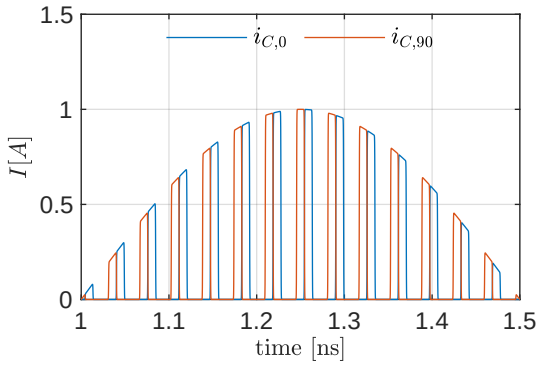
The final method that was investigated to prevent the intermodulation mechanism at the common-emitter node relies on intrinsically removing the $2f_{LO}$ component from the emitter voltage spectrum. This can be achieved by adjusting the architecture of a subharmonic mixer to the one depicted in Fig. 5.5a.

The input current to the switching core of many subharmonic mixer designs [38], [39], [40] is commutated between four, quadrature-controlled BJTs, which is also the case in Fig. 5.5a. The resulting (ideal) collector currents of the four BJTs can then be found by multiplication of the input current $i_{DDRM,0}$ with a 25 % duty-cycle pulse train, rather than a square wave. This is visualized for the collector currents of the BJTs connected to the 0 deg and 90 deg LO signals in Fig. 5.5b.

In subharmonic mixers, the collector currents of the BJTs controlled by the LO signals with a 180° phase differernce are combined in order to acquire an output current switching at twice the LO frequency. This is not the case in the circuit shown by Fig. 5.5a, in which the collectors of the BJTs controlled by LO signals with a phase difference of 90 deg are connected. As can be deduced from Fig. 5.5b, the sum of these collector currents does not differ at all from the output current of a conventional SB mixer core (Fig. 1.9). Due to this principal difference with a subharmonic mixer, this architecture will be referred to as a quasi-subharmonic mixer (QSH mixer).



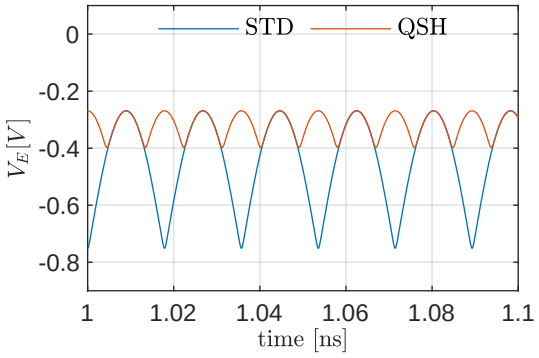
(a) Quasi-subharmonic SB mixer cell circuit



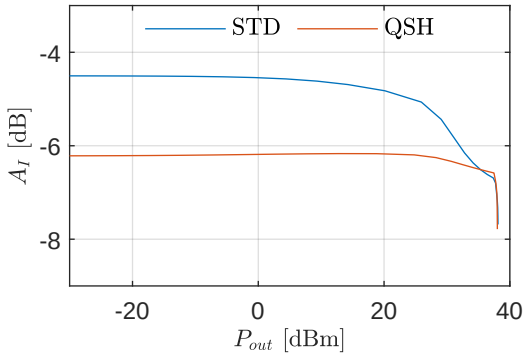
(b) Collector current waveform of single-balanced QSH mixer

Figure 5.5: Quasi-subharmonic mixer concept. The sum of the collector currents plotted in Fig. 5.5b gives the output current $I_{SB,0}$ of the SB QSH mixer cell.

Although the SB QSH mixer output current is identical to that of a standard SB mixer, a clear difference exists at their output ports. The current commutation between four devices results in the fundamental frequency of the emitter voltage waveform increasing from $2f_{LO}$ to $4f_{LO}$ [41]. This is also shown in Fig. 5.6a.
As a result, no intermodulation products can be created around $2f_{LO}$.
Intermodulation around $4f_{LO}$ is hot prevented by this measure. However, the effect of these intermodulation products on the output current around f_{LO} is heavily reduced due to the increased separation between the desired output band and the fundamental frequency of the emitter voltage. In order to result in in-band components, the intermodulation products around f_{LO} rely on down-conversion via the third harmonic of the LO. This stands in contrast to the standard SB mixer cell, in which the intermodulation products around $2f_{LO}$ are down-converted by the (much larger) fundamental component of the LO.
The principles of this concept are confirmed in Fig. 5.6b, which shows that the current conversion gain of a QSH-based SSB mixer lies closer to the ideally predicted value of $-6.9\,\mathrm{dB}$ and remains flat up to a higher output power level, compared to a standard (STD) SSB PMIX.



(a) Ideal (no C_{BE}) emitter voltage of STD SB PMIX ad QSH SB PMIX.



(b) AM-AM conversion with a static C_{BE} of $2\,\mathrm{pF}$ included in the PMIX circuits.

Figure 5.6: Emitter voltage and AM-AM conversion of an SSB PMIX implemented using standard SB mixer cells and SB QSH mixer cells.

Another interesting observation, apparent from Fig. 5.6a, is that the emitter voltage of the QSH

SB mixer cell is reduced with respect to the STD SB mixer cell. To investigate why this is the case, an expression for $V_{E,QSH}(t)$ can be derived, using an approach similar to the determination of Eq. 2.9. The result is given by:

$$V_{E,QSH}(t) = V_{B,DC} - V_T \ln\left(\frac{I_{DDRM,0}(t)}{2I_S\left(\cosh\left(\frac{V_{LO,I}(t)}{2V_T}\right)\cosh\left(\frac{V_{LO,Q}(t)}{2V_T}\right)\right)}\right) \tag{5.2}$$

Upon finding the extreme values of Eq. 5.2, the following emitter voltage swing is found for the ideal QSH mixer:

$$V_{E,QSH,pk-pk} = -V_T \ln 2 + \frac{V_{LO}\left(2\sqrt{2}-1\right)}{4\sqrt{2}} \tag{5.3}$$

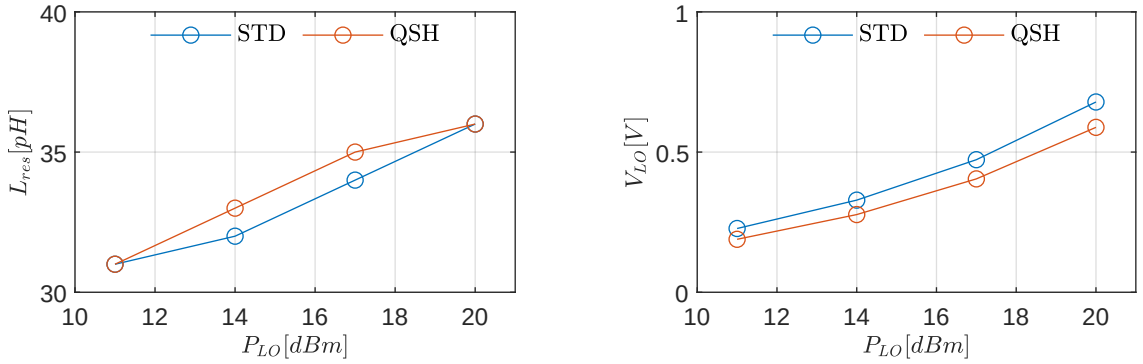
The value given by Eq. 5.3 is almost four times as small as the emitter voltage swing of the standard SB mixer cell, which was determined to be $-V_T \ln 2 + V_{LO}/2$. This means that, ideally, less voltage headroom is required on the emitter node to comply with the voltage requirements of the DDRM. This allows for a lower V_B and V_{CC} and thus boosts the system power efficiency. In reality, the presence of C_{BE} already heavily reduces the emitter voltage swing, and so this apparent becomes less significant.

5.2. PMIX Cell Design in QUBiC Gen8

This section describes the practical design steps for a mm-wave PMIX cell that implements the techniques presented in Section 5.1.

The PMIX cell is designed in four subsequent steps. The first step is to place an inductance L_B between the bases of the HBTs in a SB mixer cell (see Fig. 5.3a). This resonates out the capacitive impedance components present at the HBT bases, which ensures that the LO power is maximally utilized for the switching action of the mixer cell.

Fig. 5.7 shows the L_B required to reach the maximum base voltage swing for various values of provided LO power. The HBTs used in the SB mixer cells are of a identical size to those used in the CB PA, as the PMIX has to deal with the same current levels. The figure shows that the use of QSH SB mixer cells in the SSB PMIX requires almost 3 dBm more LO power to match the base voltage swing of an STD SSB PMIX. This should not be a surprising result, as twice the amount of (identically sized) HBTs are connected to the LO source when employing the QSH SB mixer architecture. A value of 34 pH was chosen for L_B in the circuit of both the STD SB mixer cells and QSH mixer cells. This gives a base voltage swing of around 0.5 V, if 17 dBm and 19 dBm of LO power are used to drive the STD and QSH architecture, respectively.



(a) Inductance L_B leading to the maximum base voltage swing, given the power P_{LO} drawn from the LO source.

(b) Base voltage swing achieved, given that the optimal L_B for a given P_{LO} is applied in the SB mixer cell.

Figure 5.7: Required L_B for maximum base voltage swing V_{LO} for various LO power levels. The LO power is delivered to an SSB PMIX constructed using standard (STD) SB mixer cells and QSH SB mixer cells, respectively.

The second design step is to create the desired impedance match at the output port of the SSB PMIX architecture of choice. This can be realized by connecting a shunt inductance L_C to the output ports of the individual SB mixer cells within the SSB PMIX. In case a cascode stage is used, another inductance is required to match the load to output port of cascode.

For the STD- and QSH-based PMIX topologies inductances of respectively 270 pH and 135 pH suffice. The realized output reflection coefficient (normalized to 50 Ω) of these two topologies are shown for different collector currents in Fig. 5.8. This figure shows that the SSB PMIX architecture comprising of QSH SB mixer cells shows a heavily reduced output impedance, compared to its STD counterpart. Additionally, the output impedance of the QSH architecture shows more variation over different current levels. In case a cascode stage is used to load the SSB PMIX, an inductance of 400 pH should be connected to its output nodes, if the output impedance is to be made purely real.

The third design step is to determine the required load R_L of the SSB PMIX, such that output power is maximized. Ideally, a loadline match conform Table 2.2 can be used. In case of a finite output impedance of the SSB PMIX, R_L should be chosen according to Eq. 3.4. Unfortunately, as can be deduced from Fig. 5.8 and Section 3.3, a conjugate match is the best option for all topologies. This corresponds to a load R_L of 70 Ω, 150 Ω and 200 Ω for the QSH-based, STD and cascoded architectures, respectively.

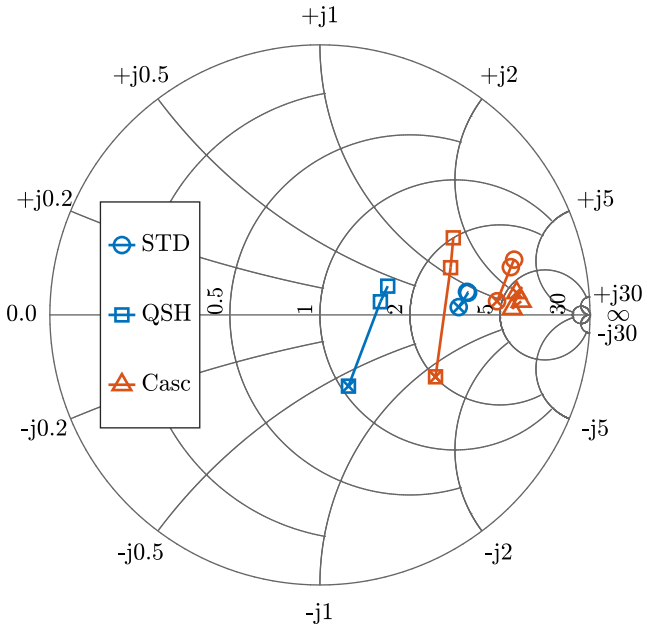
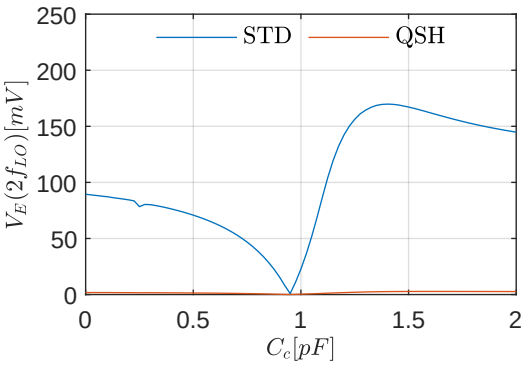
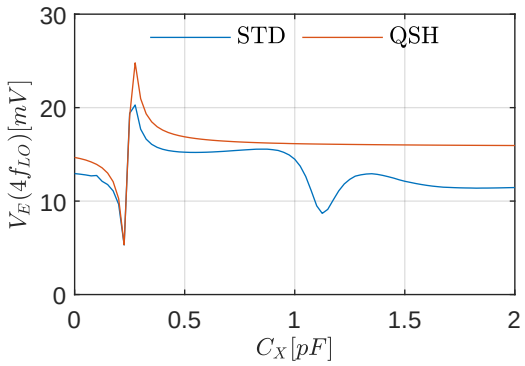


Figure 5.8: Resulting reflection coefficients at 28 GHz after impedance matching, determined using a periodic S-parameter analysis. The different data markers describe the different stages (STD SSB PMIX, QSH SSB PMIX and cascode stage). The red data points correspond to their respective output reflection coefficients, while the blue points correspond to the reflection coefficient as seen by the LO. The three data points of each curve correspond to a quiescent current level of 1, 10 and 100 mA, the latter indicated by the marker containing a cross.

The final design step is to determine C_X (Fig. 5.3) to resonate out C_{BE}. A convenient method is to sweep the value of C_X and inspect which value of C_X maximizes the emitter voltage component at the fundamental frequency of the emitter voltage. For the STD SSB PMIX and QSH PMIX architectures, respectively the voltage component at $2f_{LO}$ ad $4f_{LO}$ should be maximized. The results of this parameter sweep are shown in Fig. 5.9. Consequently, a C_X of 1.4 pF should be used for the STD PMIX, while a C_X of 0.26 pF is required for the QSH PMIX.



(a) Voltage magnitude of the second LO harmonic content at the emitter node



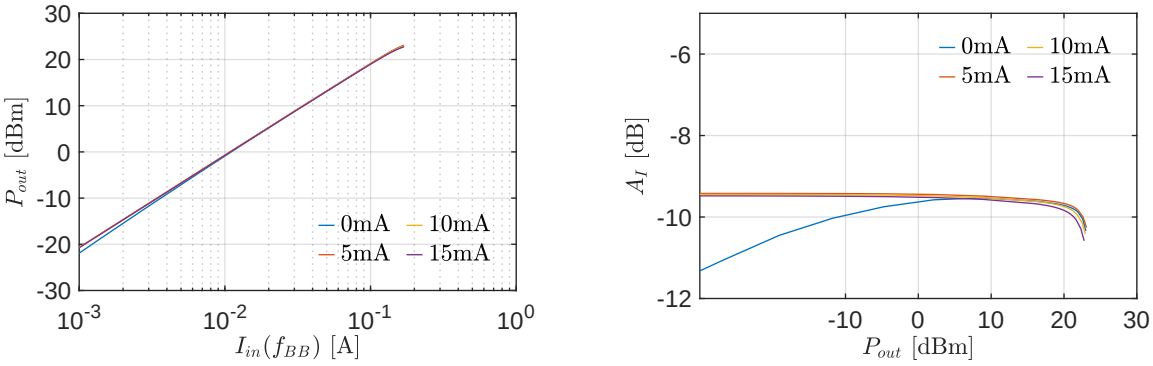
(b) Voltage magnitude of the fourth LO harmonic content at the emitter node

Figure 5.9: Harmonic content of interest of the emitter voltage versus capacitance C_X. A quiescent current of 30 mA was applied to the SB mixer core, which roughly corresponds to the DC component of a 100 mA class B current waveform.

5.3. SSB PMIX Performance

This section evaluates the impact of the linearity enhancement techniques as described in Section 5.1 on the performance of an SSB PMIX implemented in the QUBiC Gen8 technology. Note that, if the techniques successfully dispose of the gain expansion effect resulting from C_{BE}, the entire AM-AM characteristic must be shifted to $-12\,\mathrm{dB}$. This is different from the ideally predicted $-6\,\mathrm{dB}$ in Table 2.1, as the practical SSB PMIX is conjugately matched rather than loadline matched.

Fig. 5.10 shows the result of applying a (small) quiescent current on the output power and AM-AM conversion of an STD SSB PMIX. As could be expected from Fig. 5.2, small quiescent currents give no significant improvement in linearity. Therefore, a minimal quiescent current can be used, to ensure that the linearity degradation at low input current levels (Section 3.4) is mitigated.

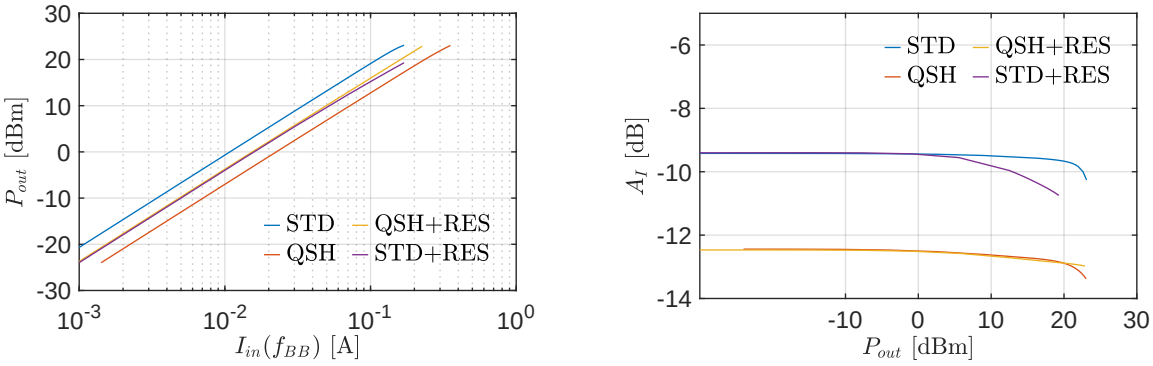


(a) Output power versus fundamental input current

(b) AM-AM conversion

Figure 5.10: Output power and current gain of a STD SSB PMIX biased using various quiescent currents

Fig. 5.11 shows the output power and current gain for the different combinations of the presented linearization techniques. Interestingly, resonating out the C_{BE} capacitances on the common-emitter node results in worse linearity if applied to a STD PMIX architecture. Possible explanations for this will be discussed in chapter 6. The current gain of the QSH-based SSB PMIX, does lie very close to the ideal value, and adding the resonator at the common-emitter node slightly improves its linearity. However, the maximum output power of the QSH-based SSB PMIX does not lie significantly higher if compared to the STD SSB PMIX.

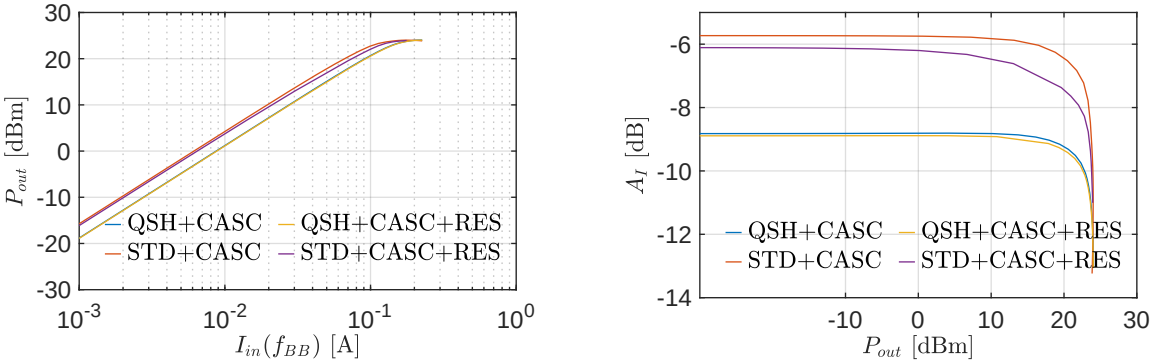


(a) Output power versus fundamental input current

(b) AM-AM conversion

Figure 5.11: Output power and current gain of the STD and QSH-based PMIX, not loaded by a cascode

The linearity performance of the SSB PMIX architectures equipped with a cascode stage is shown in Fig. 5.12. To linearize the cascode stage itself, a quiescent current of 25 mA is required. Again, resonating out the emitter capacitances results in linearity degradation in the case of the STD architecture.
Cascoding the QSH SSB PMIX does result in better linearity, as its −1 dB compression point lies between 1 and 2 dBm higher compared to the cascaded STD SSB PMIX. Adding an open condition to the common-emitter node does not result in significant performance improvement.



(a) Output power versus fundamental input current

(b) AM-AM conversion

Figure 5.12: Output power and current gain of the different SSB PMIX architectures loaded by a cascode stage

In Fig. 5.13, the system power-efficiencies of three SSB PMIX architectures with a high maximum output power and/or high linearity are shown. Although the output power of the cascoded, QSH-based PMIX is slightly higher than that of the STD PMIX, its higher quiescent current and supply voltage result in a lower power efficiency. The low power efficiency can partly be attributed to the voltage headroom requirements of the DDRM, which was taken taken into account during in the PMIX cell design.

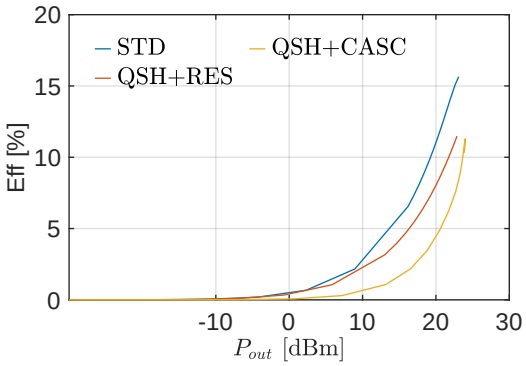


Figure 5.13: Efficiency of three SSB PMIX architectures

If a SSB PMIX is to be designed in the QUBiC Gen8 technology, the highest output power, linearity and power efficiency can be achieved if STD SB mixer cells are used. Resonating out the emitter node capacitances or the use of a cascode stage does not result in (significant) performance improvement. Apparently, C_{BE} is so large that the input current level at which the intermodulation effects at the common-emitter node start to vanish, lie well beyond the limits of the DDRM. As a result, the gain expansion due to intermodulation effects on the common-emitter nodes behaves linearly and work in the advantage of the designer.

5.4. Conclusion

This chapter introduced various design techniques to enhance the linearity of a current-mode SSB PMIX. These design techniques aimed to mitigate intermodulation effects on the common-emitter node and/or to increase the output impedance of the SSB PMIX. These techniques included the use of an additional cascode stage, the addition of a common-mode resonator at the emitter node, and the use of a quasi-subharmonic SB mixer cell.
Then, a design strategy was given for a QUBiC Gen8 SSB PMIX core, which included the required design steps to implement the proposed design techniques.
After evaluating the performance variations between the SSB PMIX core topologies, it turned out a standard SSB PMIX core without any additional techniques resulted in the best linearity performance. Therefore, it is recommended to use standard SB mixer cells when designing a mm-wave PMIX in this the QUBiC Gen8 technology.

6

Discussion

In this chapter, the performances of the designed current-mode PA and PMIX are reviewed. The emphasis lies on the results that did not reach the expected performance, for which possible explanations and recommended steps for future work will be given. For both the PA and the PMIX, this mainly concerns the realized linearity and power efficiency. The discussion will be divided in two sections, one for the PA and one for the PMIX-based front-end.

6.1. Current-Mode PA

For the current-mode PA, both the power efficiency and the linearity did not meet the performance as expected from the analysis from chapter 2 and the specification of the DDRM itself. The measured peak power efficiency of 20 % is significantly lower than the ideally expected 44 %, which can be derived from the conclusions of Section 2.4 and the designed bias conditions of the PA.

The main reason for the low power efficiency are the losses in the balun. The G_{max} of the balun, the model of which was generated using Momentum simulations, showed to be slightly below -2 dB. This level of insertion loss, although comparable to [33], [34] and [42], can definitely be improved upon. The simulated losses of the coil at DC were determined to be very low, and thus the high losses must be the result of the design being flawed at RF frequencies. Two possible reasons for the relatively high RF losses will be considered.

A first reason could be the assumption that the skin effect does not play a significant role in the value of the coil resistance, as the skin depth at 2.4 GHz is close to half the thickness of metal layer 6. Besides the fact that this may not be negligible, this assumption was not specifically validated, which have been done using a simple Momentum simulation setup. As a result, the width of the wires was not tailored to the RF frequencies, which could have resulted in increased losses in the coils.

The second reason could be the parallel configuration of metal layers 4 to 6 in the layout of the coils, which was used to lower the resistance of the coil. However, the increased proximity of the coils to the bulk silicon could significantly increase the losses in the substrate. Recognizing the massive size of the balun, this is definitely a realistic option. Investigating the substrate losses associated with the different metal layers beforehand would have been a better approach.

Besides the losses in the balun, also the combination of the limited breakdown voltage level of the QUBiC Gen8 EHV BNP devices and the large headroom voltage required by the DDRM play a substantial role in the low power efficiency. In order to achieve higher power efficiency levels, either a DDRM that requires a lower supply voltage, or a technology that can withstand higher voltage levels has to be used.

The linearity of the PA-based front-end also leaves room for improvement, with the ACPR being

measured being $-33.07\,\mathrm{dB\,c}$. This too could be attributed to the properties of the balun. First, there are large differences between the inductances, coupling factors and wire lengths of the four different coils at the primary winding. This results in a significant mismatch in the impedance seen by the four differential CB pairs (Fig. 4.11), which can certainly lead to reduced linearity. Secondly, both the real and imaginary parts of the four input impedances of the balun do not exhibit a flat characteristic over the frequency range of interest. This uneven loading of the CB stage in the desired band is another very likely source of nonlinearity.
By choosing a balun topology that provides more symmetry between the four input ports and by taking care its input impedance exhibits a more flat in-band characteristic, a more linear PA would be obtained.

6.2. Current-Mode PMIX

The discussion on the performance of the PMIX cell design is also focused on power efficiency and linearity. The power efficiency of the PMIX is relatively low (peak efficiency of $15\,\%$). Given the high operation frequency and, moreover, the inherent lower efficiency of a PMIX in comparison to a PA (Table 2.1), this is less of a surprise. Nevertheless, the power efficiency could be improved. The first possible solution is taking care that the high PMIX output impedance is maintained at mm-wave frequencies, which is easier said than done. Although this could be realized by cascoding the switching core, the subsequent increase in supply voltage results in degradation of the power efficiency. Another, more approach would be to use devices that maintain a higher output impedance at mm-wave frequencies. Another solution yielding increased power efficiency is to increase the voltage drop across the PMIX relative to that of the DDRM. As was the case for the PA, this could be achieved by using a DDRM that requires a lower supply voltage, or by resorting to a technology in which the devices have a higher (avalanche) breakdown voltage.

To enhance the linearity of the PMIX, Section 5.1 presented multiple techniques: creating an open impedance condition on the common-emitter node at $2f_{LO}$, implementing the SB mixer cells using the novel QSH mixer architecture, and/or using an additional cascode stage. Surprisingly, none of these techniques resulted in significant improvement of the PMIX linearity in the practical situation. For each of these methods, it will be discussed why this may be the case. Especially compensating the emitter node capacitances at $2f_{LO}$ by creating a resonating common-mode loop did not result in the predicted effect. The reason for this may be that the base-emitter capacitances, which dominate the capacitive loading at the emitter node, are largely diffusion capacitances and thus vary wildly for different (collector) current levels. As a result, the resonance frequency of the common-emitter node also changes, compromising the effectiveness of the proposed technique. Additionally, as the ideal emitter voltage swing (Fig. 2.6) can yield hundreds of mVs, a high Q-factor of the resonator is required to prevent the flow of parasitic currents resulting from the intermodulation effect at the common-emitter node. The presence of any (parasitic) resistance at the base or emitter terminals makes the implementation of a high-Q resonator very difficult.
The effectiveness of the QSH mixer architecture was reduced by both its low output resistance and strong variation in output reactance for different input current levels. The latter could also be the reason why cascoding the QSH-based SSB mixer did not really improve its linearity with respect to the cascoded, standard SSB mixer. However, the QSH architecture could still be very useful for systems with a lower operation frequency. At lower frequencies, mixer operation is less affected by parasitics, and thus the lower emitter voltage swing of the QSH mixer with respect to the standard SB mixer is much more pronounced. A more constant emitter voltage alleviates the loading conditions of the stage driving the switching core. Alternatively, the reduced voltage swing allows a lower voltage bias of the emitter node, resulting in increased power efficiency.

7

Conclusion

Due to its high linearity potential, current-mode operation is a very promising candidate for the design of front-ends that are able to operate at low power back-off, thus yielding a high power efficiency. In this thesis, the performance limits of two current-mode front-end concepts were explored. For both concepts, the ideal performance was analyzed, the potential design challenges were identified, and a design in the QUBiC Gen8 technology was proposed.

The first concept was a 2.4 GHz current-mode PA, driven by a highly linear DDRM. For this PA, a design was proposed, taped and tested. The design comprised four parallel CB stages and a PCT balun performing the power summation. The PA was able to deliver an output power of 27 dBm and reached a system efficiency of 20 %. The measured ACPR yielded −33.07 dB c, indicating that the linearity of the PA requires more attention in order to fulfill the potential of the current-mode operation. Most likely, the relatively low linearity is a result of port mismatch and in-band impedance variation of the PCT balun.

The second concept was aimed at the operation frequency of 28 GHz and comprised a current-mode PMIX driven by the same DDRM. For this concept, multiple methods were proposed to restore the linearity degradation associated with high-frequency effects such as a reduced device output impedance, and an intermodulation mechanism taking place at the common-emitter node. Interestingly, the standard SSB PMIX cell architecture showed to result in the best performance. The standalone PMIX cell yielded a simulated maximum output power of 22 dBm and a peak power efficiency of 15 %.

Both front-end designs suffer from a relatively low power efficiency, which could be solved either by moving to a technology that can handle higher supply voltages, or by the use of a DDRM that requires less voltage headroom.

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