A Reconfigurable Ultrasound Transceiver ASIC With 24 x 40 Elements for 3-D Carotid Artery Imaging

Kang, Eunchul; Ding, Qing; Shabanimotlagh, Maysam; Kruizinga, Pieter; Chang, Zu Yao; Noothout, Emile; Vos, Hendrik J.; Bosch, Johan G.; Verweij, Martin D.; de Jong, Nico

DOI
10.1109/JSSC.2018.2820156

Publication date
2018

Document Version
Accepted author manuscript

Published in
IEEE Journal of Solid State Circuits

A Reconfigurable Ultrasound Transceiver ASIC With 24 × 40 Elements for 3D Carotid Artery Imaging

Eunchul Kang, Qing Ding, Maysam Shabanimotlagh, Pieter Kruizinga, Zu-yao Chang, Emile Noothout, Hendrik J. Vos, Johan G. Bosch, *Member, IEEE*, Martin D. Verweij, *Member, IEEE*, Nico de Jong, *Member, IEEE,* and Michiel A. P. Pertijs, *Senior Member, IEEE*

***Abstract*—This paper presents an ultrasound transceiver ASIC designed for 3-D ultrasonic imaging of the carotid artery. This application calls for an array of thousands of ultrasonic transducer elements, far exceeding the number of channels of conventional imaging systems. The 3.6 × 6.8 mm^2 ASIC interfaces a piezo-electric transducer array of 24 × 40 elements, directly integrated on top of the ASIC, to an imaging system using only 24 transmit and receive channels. Multiple ASICs can be tiled together to form an even bigger array. The ASIC, implemented in a 0.18 µm high-voltage BCDMOS process, consists of a reconfigurable switch matrix and row-level receive circuits. Each element is associated with a compact bootstrapped high-voltage transmit switch, an isolation switch for the receive circuits and programmable logic that enables a variety of imaging modes. Electrical and acoustic experiments successfully demonstrate the functionality of the ASIC. In addition, the ASIC has been successfully used in a 3-D imaging experiment.**

***Index Terms*— 3-D ultrasound imaging, matrix transducer, reconfigurability, ultrasound application-specific integrated circuit (ASIC), high-voltage switches.**

I. Introduction

Atherosclerosis (the formation of plaques in the blood vessels) is the main source of cardiovascular events, such as stroke, infarct, and aneurysm and a main cause of death worldwide [1]. The left and right carotid arteries, that supply blood to the head, are very important in this respect. Plaque is known to build up especially near the bifurcation of the carotid. Such plaques may obstruct the blood flow or even be prone to rupture and are the major cause of stroke. Furthermore, the carotid arteries reflect the general progression of systemic atherosclerotic disease and are well accessible for assessing the arterial wall thickness and stiffness [2], [3].

The identification of vulnerable atherosclerotic plaques, which are susceptible to rupture and therefore candidates for intervention, is a central issue in vascular imaging. Plaque vulnerability is related to dimension, composition, mechanical stress distribution, and inflammation state, which are the targets for plaque assessment. Currently, no suitable method exists for large-scale early screening of patients at risk: 2D ultrasound imaging is too limited, X-ray exposure of CT is prohibitive, and MRI is too expensive and logistically unsuited. Real-time 3D ultrasound is an ideal tool for fast, complete, and highly effective carotid screening.

Currently, B-mode 2D ultrasound imaging is used to evaluate carotid artery disease. The degree of stenosis and its impact on the local blood flow distribution, the shape of a plaque and possible calcium deposits can be visualized by B-mode 2D ultrasound imaging. However, the 2D character of all these measurements is a serious limitation. They are performed in a single position or single plane, while, in fact, a complex three-dimensional situation needs to be assessed. Therefore, disease can be easily under- or overestimated [4].

Accurate assessment of carotid artery disease by measuring blood flow, plaque deformation and pulse-wave velocity using ultrasound requires real-time 3-D images [5]-[8]. To generate such images, the next generation of ultrasound probes for carotid artery imaging require matrix transducer arrays. It is highly challenging to build such probes, since the transducer array needs to cover a relatively large aperture (>2 cm) while operating at 5 MHz or higher, leading to arrays of thousands of transducer elements, far exceeding the number of channels that conventional imaging systems can handle and that can be connected using a manageable number of cables.

This problem can be addressed by building ASICs into the probe to reduce the number of cables. Various approaches have been reported to interface matrix transducer arrays using a reduced number of cables. Programmable pulsers have been

This work is part of the Open Technology Program with project number 13154 which is financed by the Netherlands Organisation for Scientific Research (NWO).

E. Kang, Z.Y. Chang and M. A. P. Pertijs are with the Electronic Instrumentation Lab, Delft University of Technology, Delft, The Netherlands (e-mail: e.kang@tudelft.nl).

Q. Ding was with the Electronic Instrumentation Lab, Delft University of Technology, Delft, The Netherlands and is now with Sony Depthsensing Solutions, Brussels, Belgium

M. Shabanimotlagh and E. Noothout are with the Laboratory of Acoustical Wavefield Imaging, Delft University of Technology, Delft, The Netherlands.

P. Kruizinga and J.G. Bosch are with the Thoraxcenter, Department of Biomedical Engineering, Erasmus Medical Center, Rotterdam, The Netherlands.

H.J. Vos, M. D. Verweij and N. de Jong are with the Laboratory of Acoustical Wavefield Imaging, Department of Imaging Physics, Delft University of Technology, Delft, The Netherlands, and also with the Thoraxcenter, Department of Biomedical Engineering, Erasmus Medical Center, Rotterdam, The Netherlands.

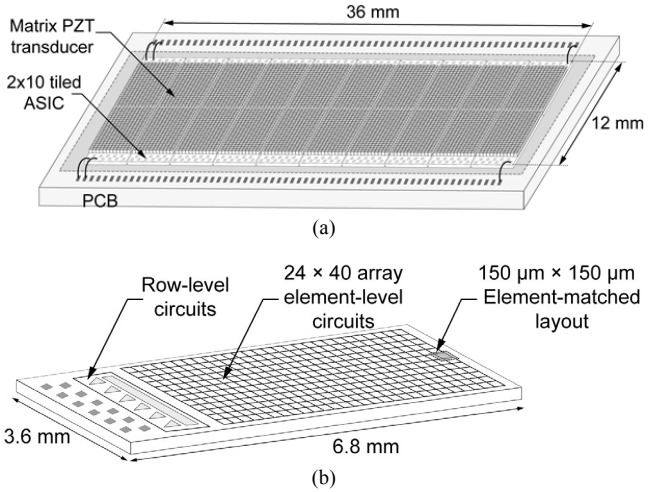


Fig. 1. (a) Overview of the proposed matrix transducer on tiled ASICs; (b) overview of a single ASIC.

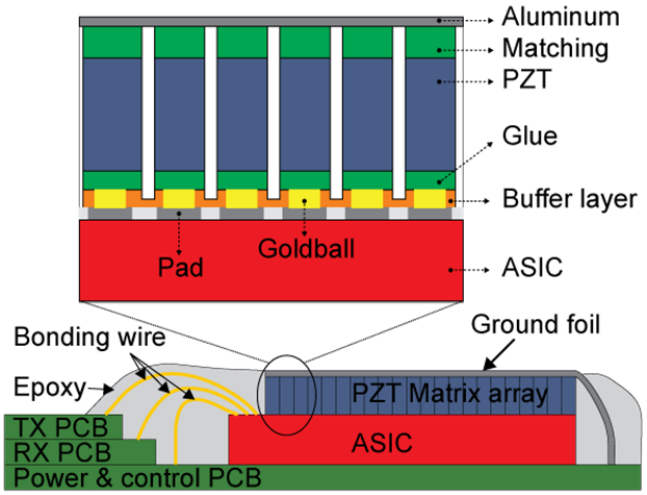


Fig. 2. Cross-sectional view of the transducer array mounted on top of the ASIC.

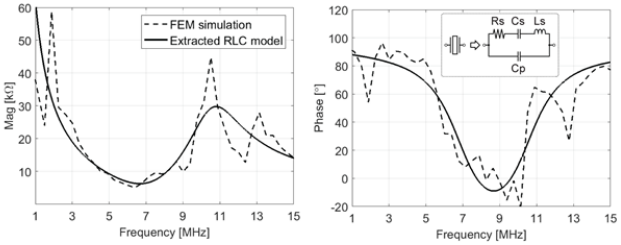


Fig. 3. Simulated electrical impedance characteristic of a transducer element, along with a Butterworth-Van Dyke lumped-element model.

used to locally generate the high-voltage pulses needed to drive the transducer elements [9]-[12], [17]-[19]. Part of the receive beamforming can be performed locally in the probe to combine the signals received by a sub-array into one output signal [12]-[14]. Switch matrices have been proposed that connect groups of elements that transmit and receive simultaneously [15], [16]. Row-by-row scanning schemes [17], [19], and reconfigurable row- or column-parallel connection schemes [18] have also been reported.

In this paper, we propose an ASIC with a row-level architecture for both RX and TX channels [20]. The ASIC consist of 24 × 40 element-level circuits, consisting of TX switches, RX switches and control logic, that allow each element to be selectively connected via row-level RX and TX buses to an imaging system. This leads to 40-fold channel reduction. The element-level circuitry fits in the 150 µm × 150 µm area occupied by a single 7.5 MHz transducer element, allowing the transducer array to be integrated directly on top of the ASIC. The chip-level layout allows for multiple ASICs to be tiled to form even larger transducer arrays. The on-chip logic allows a variety of different element selection patterns to be programmed.

This paper is organized as follows. Section II describes the architecture and functionality of the ASIC. Section III presents the circuit details of the element-level and row-level circuits. Section IV provides experimental results, and Section V concludes the paper

II. System Architecture

A. Matrix Transducer Configuration

To cover an aperture sufficient for carotid-artery imaging, the matrix transducer area targeted in our work is 12 × 36 mm^2. Since this area is rather large to cover with a single die, we propose to tile 2 × 10 ASICs, as shown in Fig. 1a. Each of these ASICs, as shown in Fig. 1b, has a die size of 3.6 × 6.8 mm^2, and interfaces with a (sub-)array of 24 × 40 transducer elements through element-level and row-level circuits. Connections to the transducer elements are made through an array of bondpads, which are positioned such that a contiguous 150 µm-pitch transducer array can be built on top of the tiled ASICs. The ASICs will be arranged in a head-to-head fashion, similar to that reported in [17], [19], so that bondpads on the periphery of each ASIC allow for row-level connections to an imaging system via a PCB substrate.

The transducer array is directly built on top of the ASICs using the PZT-on-CMOS integration scheme illustrated in Fig. 2 [21]. The bond pads on the ASIC that provide electrical connections to the transducer elements are equipped with gold bumps using a wire-bonding tool. After this, an epoxy buffer layer is applied to ASIC that is grinded down to expose the gold, thus providing reliable electrical contacts for the transducer elements. The acoustic stack consisting of a piezo-electric layer (PZT) and a matching layer is glued on top of the grinded epoxy layer, which is cut into the desired 150-µm-pitch array pattern using a diamond saw. Finally, the array is covered with an aluminum foil that forms the common ground electrode of the elements.

The transducers have a center frequency of 7.5 MHz and a bandwidth of about 45 %. The impedance characteristic of the transducer elements has been simulated using finite-element analysis software (PZFlex LLC, Cupertino). Their electrical impedance around resonance can be modelled with a Butterworth-Van Dyke model, as shown in Fig. 3, with an impedance of approximately 1.2 pF // 6.8 kΩ at resonance. The elements have an estimated transmit efficiency of 20 kPa/V at

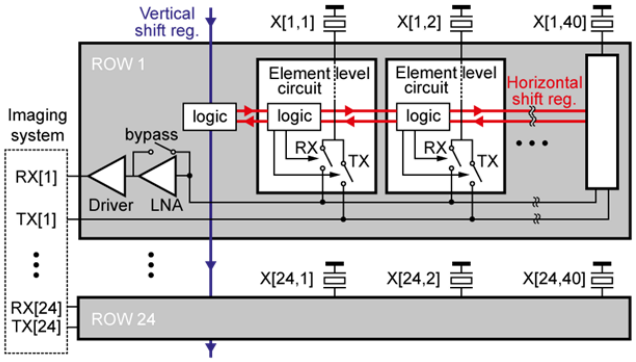


Fig. 4. Block diagram of the ASIC.

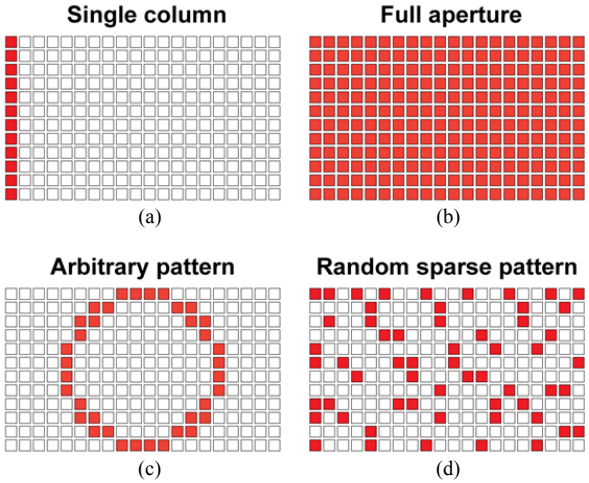


Fig. 5. Element-selection modes supported by the ASIC: (a) single-column selection; (b) full-aperture selection; (c) selection of arbitrary sets of elements; (d) pseudo-random element selection.

45 mm from the transducer, requiring transmit voltages in the order of tens of Volts to generate sufficient acoustic pressure to be useful for carotid imaging. Their receive sensitivity (estimated by referring the measured output voltage of the ASIC back to an equivalent voltage at the terminals of an unloaded transducer) is around 4 μV/Pa.

B. ASIC Architecture

Fig. 4 shows the top-level architecture of the proposed ASIC. To achieve channel count reduction, the 40 elements in each row of the matrix share a row-level RX and TX bus, thus reducing the number of channels by 40×. This approach is similar to that reported in [18]. These row-level RX and TX buses can be shared by neighboring head-to-head positioned ASICs in a tiled configuration, so that rows of 80 elements are formed that span two ASICs and share one RX and TX line. Thus, the channel count is manageable even for large arrays with tiled ASICs. Each transducer element is associated with a programmable element-level switch circuit that allows the element to be connected to the RX bus or the TX bus. The RX line connects to a shared row-level low-noise amplifier (LNA) and cable driver.

The ASIC enables rapid reconfiguration of the selection of elements used for RX and TX, aiming for application in high-frame-rate volumetric imaging of the carotid artery. Control logic, programmed through row-level and element-level logic, determines whether an element participates in a given transmit and/or receive cycle. Element-level memory, which can be pre-loaded through a shift register, allows the selection of active elements to be rapidly changed between successive transmit/receive cycles.

To enable pulse transmission on all elements in the array, we use high-voltage (HV) switches to connect the elements to pulse generators in the imaging system via the row-level TX bus. Compared to the use of integrated pulsers [9], [10], [11], [13], [22], [23] or high-voltage linear amplifiers [24], [25] per element, this approach consumes less die area, thus facilitating smaller pitch arrays, and reduces power dissipation in the probe. Moreover, it allows for a broader range of transmit waveforms. After transmission, each element can be connected through a RX bus, a row-level LNA and a cable driver to a receive channel of the imaging system. To extend the dynamic range of the receive path, the LNA can be bypassed at high signal levels, or enabled at low signal levels.

C. Reconfigurability

Through reconfigurable per-element logic, the ASIC supports a variety of aperture selections for different imaging schemes (Fig. 5), including column-by-column selection for synthetic aperture transmission and/or reception (Fig. 5a), full-aperture selection for plane-wave transmission (Fig. 5b), arbitrary element selections (Fig. 5c) and pseudo-random sparse element selections (Fig. 5d). Each element is equipped with memory bits that define whether the element participates in TX and in RX. These bits can be loaded in various ways, allowing different trade-offs between programming time and flexibility (Fig. 6). All element-level memory cells (flip-flops) are part of a shift register, which can be loaded in a daisy-chain fashion to be able to define arbitrary selections (Fig. 6a). If the selection pattern is identical in all rows (like in Fig. 5a and 5b), the shift register can also be loaded in a row-parallel fashion (Fig. 6b), thus significantly reducing the programming time. For even faster reconfiguration, each element is equipped with 9 memory bits for RX and 9 bits for TX, so that 9 arbitrary patterns can be pre-programmed and the ASIC can switch between these patterns with a single clock pulse (Fig. 6c). Finally, the memory content can also be shifted to neighboring elements, from left to right (Fig. 6d) or right to left (Fig. 6e), to laterally translate the selected aperture. This allows the matrix transducer to be operated as an electronically-scanned linear array. Each element is also associated with an enable bit (EL_EN) that is not shifted, allowing non-functional elements to be excluded.

The reconfigurability can be used to fulfill different imaging tasks. The plane wave transmission and column-by-column readout depicted in Fig. 5a provides excellent spatial, almost isotropic, resolution but it comes at the cost of lower temporal resolution because of the 40 transmit/receive events needed to obtain all the signals. If a higher temporal resolution is

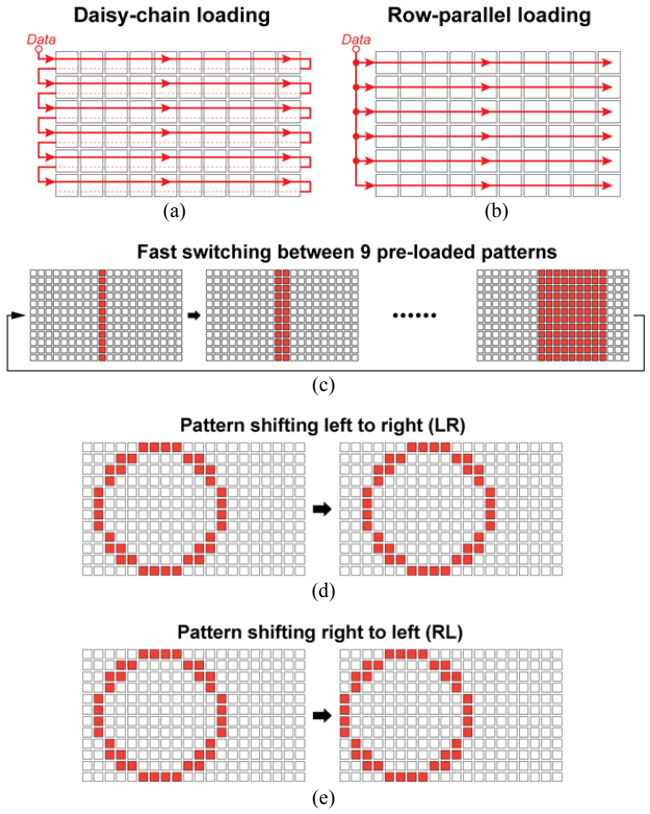


Fig. 6. Ways of reconfiguring the element selection: (a) daisy-chain loading; (b) row-parallel loading; (c) switching between 9 pre-loaded patterns; (d) pattern shifting from left to right and (e) from right to left.

TABLE I
UNITS FOR MAGNETIC PROPERTIES CONFIGURATION DATA AND LOADING TIME ASSOCIATED WITH THE DIFFERENT CONFIGURATION MODES

Mode	Bits/element	Total bits	Loading time
Row-parallel	RX, TX, EL_EN	3 × 40 = 120	2.4 µs
Daisy-chain	RX, TX, EL_EN	3 × 960 = 2880	57.6 µs
Row-parallel with 9 patterns	RX[1:9], TX[1:9], EL_EN	19 × 40 = 760	15.2 µs
Daisy-chain with 9 patterns	RX[1:9], TX[1:9], EL_EN	19 × 960 = 18240	365 µs

required, for example to capture fast transient phenomena in the carotid artery, an image mode may be selected where multiple columns are grouped together, such that fewer transmit/receive events are needed to address the complete array. Besides the gain in temporal resolution, this imaging mode would also offer a gain in SNR, since several elements signals are averaged. At the flipside, these gains come at the cost of lower spatial resolution in at least one direction. The imaging mode with random element grouping (Fig. 5d) will enable more advanced imaging methods. By predicting the pulse-echo signals and random grouping in a linear system matrix, we can formulate the reconstruction as an inverse imaging problem, as we have recently shown in [28] by imaging a 3D volume using only one transducer.

The shift register can operate at frequencies up to 50 MHz, and is buffered, so that it can be loaded during imaging without

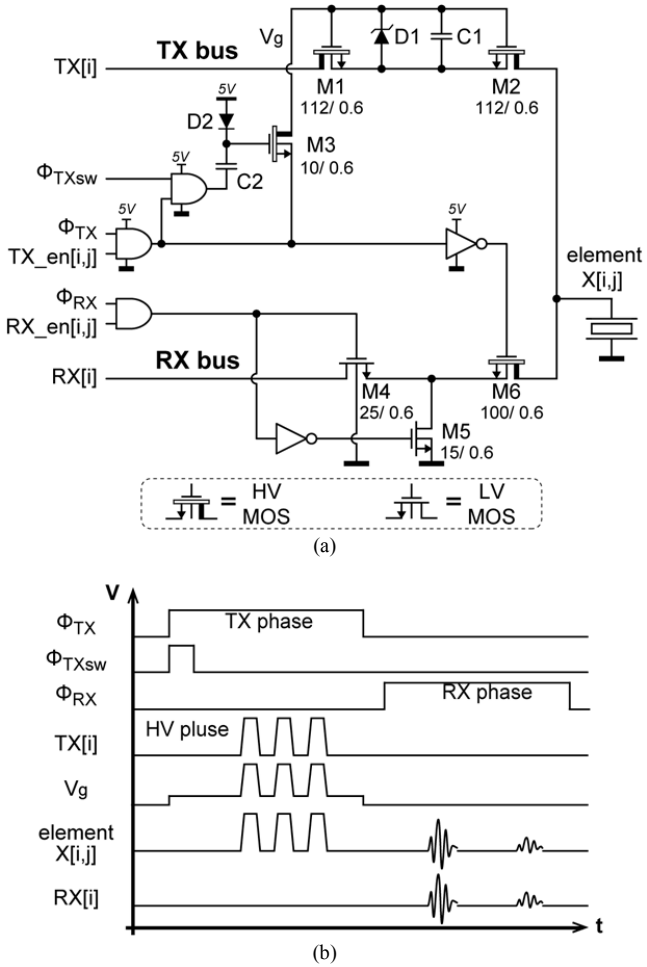


Fig. 7. (a) Simplified circuit diagram of the element-level switches, for an element located in row i, column j; (b) associated timing diagram.

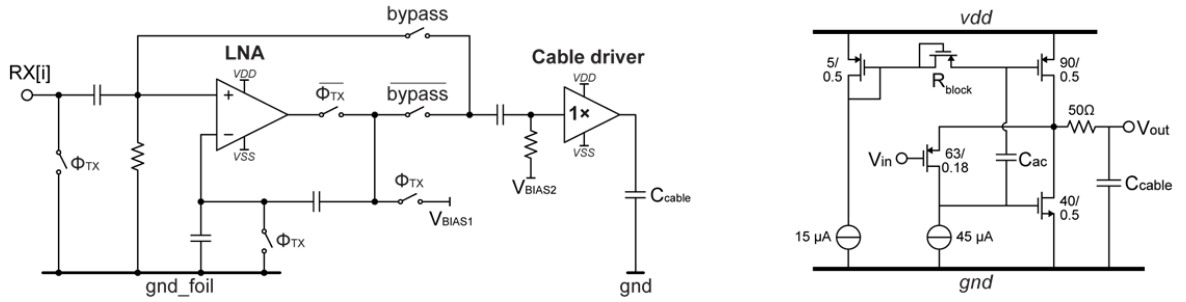
affecting the operation of the ASIC. Table I summarizes the amount of data that needs to be loaded in the different modes, and the associated loading time. Except when 9 arbitrary patterns are pre-loaded, the loading time is less than or comparable to a typical pulse-echo interval of 50 µs (which corresponds to an imaging depth of 35 mm), so that the imaging frame rate is not reduced by the loading operation. In the case of pre-loaded patterns, pattern switching can be done with a single clock pulse (i.e. < 1 µs), so that frame rate is also not affected.

III. CIRCUIT IMPLEMENTATION

A. Element-Level Switches

Fig. 7 shows a circuit diagram of the element-level switches with the associated timing diagram, for a transducer element X[*i*,*j*] located in row *i*, column *j*. This circuit connects the element to the row-level transmit bus TX[*i*] during the TX phase ϕ_{TX} if TX_en[*i*,*j*] = 1, and to the row-level receive bus RX[*i*] during the RX phase ϕ_{RX} if RX_en[*i*,*j*] = 1. The enable bits TX_en and RX_en are defined by the element-level memory (see Section III-C).

To be able to switch unipolar TX pulses with a peak value up



(a) (b)

Fig. 8. (a) Simplified circuit diagram of the row-level receive circuits; (b) Schematic of the cable driver. The transistor sizing is in µm.

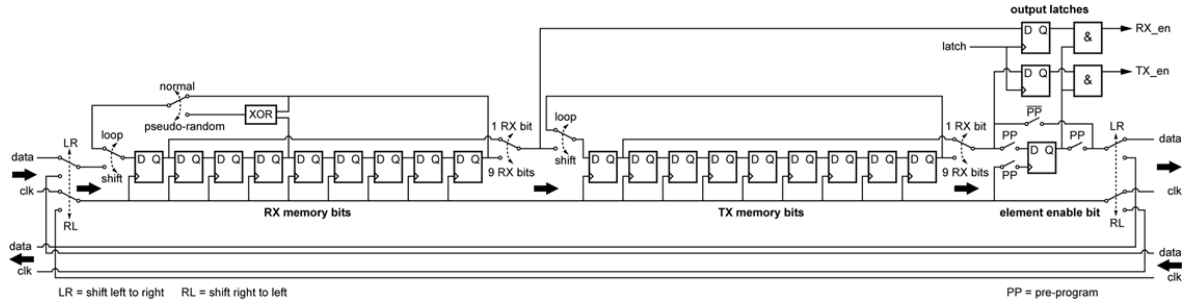


Fig. 9. Simplified circuit diagram of the element-level logic.

to 30 V, two back-to-back N-type HV LDMOS transistors (M1 and M2) connect the element to the TX bus. This structure is similar to the HV switch described in [26]. Compared to a switch based on a single HV transistor, the back-to-back configuration reduces the capacitive loading of the transducer element by the switch during the RX phase, which would cause undesired signal attenuation, to about 1 pF. Moreover, it is robust in the condition in which neighboring elements are shorted together, which may occur due to transducer fabrication issues. These advantages come at the cost of a larger layout area for a given on-resistance. In principle, this configuration also supports bipolar pulses, as in [26], but this is not supported by the gate-drive circuit in our design. The size of transistors M1 and M2 is maximized within the available die size, to minimize the power loss associated with their on-resistance, leading to a combined on-resistance of about 180 Ω.

Instead of using a latch circuit to turn on the switch transistors, as in [26], we use a more compact implementation. M1 and M2 are turned on by charging a bootstrap capacitor C1 connected between their source and gate through M3 at the beginning of ϕ_{TX}. Shortly after, M3 is turned off, leaving M1 and M2 turned on and allowing them to swing up with the transmit pulses on the TX bus. At the end of the TX phase, the source of M3 is pulled down to discharge C1 and turn off M1 and M2.

Due to parasitic capacitance to ground at the gate of M1 and M2, part of the charge stored on bootstrap capacitor C1 is lost as the voltage on the TX bus rises. To ensure that M1 and M2 maintain sufficient overdrive, C1 should be made sufficiently large, 7.2 pF in our case. A MIM capacitor is used, so that this capacitor can be placed on top of the HV devices and hence does not increase the die size.

Transistor M3 is turned on through C2 and D2. When ϕ_{TXsw} is low, D2 charges C2 to 5 V. During a short pulse of ϕ_{TXsw} at the beginning of ϕ_{TX}, the voltage at the gate of M3 is pumped above 5 V to turn on M3 and thus charge C1. C2 has sufficient capacitance (1.8 pF) compared to the capacitance at the gate of M3 to ensure sufficient gate-driving voltage. A diode-connected vertical NPN device is used to implement diode D2, so as to minimize the injection of current into the substrate when this diode is forward biased.

Transistors M4 and M6 prevent the HV pulses from reaching the RX bus and connect the element to the RX bus during ϕ_{RX}. When multiple elements are selected, they are connected in parallel to the RX bus, causing their signals to be averaged. M5 prevents the signal of non-selected elements from coupling to the RX bus. Moreover, in the TX phase, M5 turns on with M6 to connect the element to ground if it is disabled. Thus, capacitive coupling from the TX bus to the disabled elements is strongly reduced. To reduce the on-resistance of the HV switches, the element-level circuit uses a 5 V supply to drive the LDMOS, while the logic operates from a 1.8 V supply. Level-shifters (not shown) interface between these supply domains. The RX switch is sized to have an on-resistance of 280 Ω. This is well below the element's resistance, so that the noise contribution of the RX switch is negligible.

B. Row-Level Switches

To prevent signal attenuation due to the loading of the cables connecting the ASIC to the imaging system, the signal on the row-level RX bus is amplified by a row-level LNA, and buffered by a cable driver (Fig. 8a). The LNA consists of a PMOS-input folded-cascode amplifier with a non-inverting capacitive feedback, realizing a gain of 9 (19 dB) with a -3 dB bandwidth in excess of 20 MHz. To obtain an input-referred thermal noise below that of the transducer element, the input stage of the amplifier is biased at 580 µA, yielding a simulated input-referred noise level of 5.8 nV/√Hz at 7.5 MHz. The total

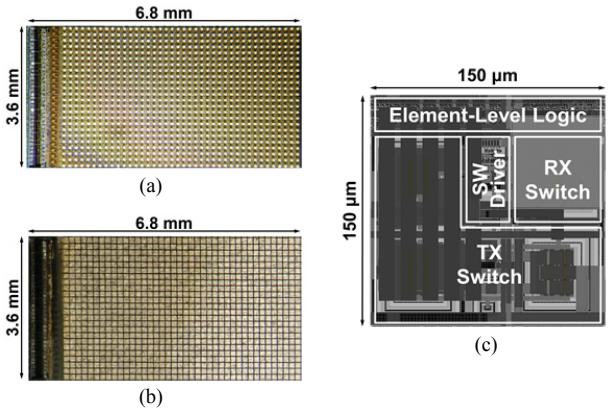


Fig. 10. (a) Chip photo of the ASIC; (b) with transducer array; (c) layout of the pitch-matched element-level circuit.

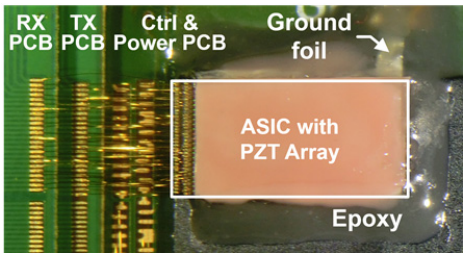


Fig. 11. Photograph of an ASIC with transducer array bonded to a stack of PCBs and protected with epoxy.

current consumption of the amplifier is 790 µA. To avoid noise coupling or interference, the capacitive feedback network is connected to the ground foil of the transducer array, rather than to the (analog) ground of the ASIC. The signal is AC coupled at the input of the LNA. During the transmit phase ϕ_{TX}, when the receive path is not active, the RX bus is grounded, and the capacitive feedback network of the LNA is pre-charged so that its output is biased close to mid-supply, to maximize signal swing. To prevent the LNA from limiting the dynamic range, it can be bypassed at high signal levels, at the cost of a higher input-referred noise level, to implement a rudimentary single-step time-gain compensation (TGC) function. A TGC implementation involving finer gain steps and a larger gain range, e.g. as in [14], would enhance the dynamic range and improve the image quality, but was not implemented in this prototype for simplicity.

The LNA is AC coupled to a unity-gain cable driver, based on a class-AB super source-follower topology [14], [27], shown in Fig. 8b. Biased at 285 µA, it is capable of driving the capacitive load of up to 300 pF of the cable connecting the probe to the imaging system. The complete receive path consumes 2 mW per row from a 1.8 V supply.

As the row-level architecture shares an LNA through RX switches and an RX bus, the associated parasitic capacitance at the input of the LNA results in signal attenuation. This capacitance includes the capacitance of the RX switch, of the TX switch, of the RX bus and of the RX switches of the non-selected elements in the row. This amounts to approximately 4.5 pF and causes about 5.6 dB signal attenuation in the band of interest if a single element is selected

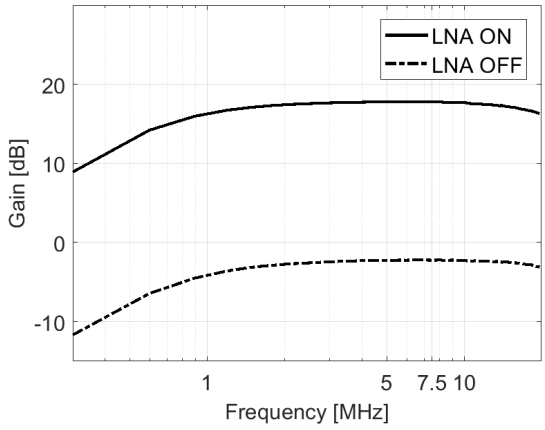


Fig. 12. Measured transfer function of the receive path.

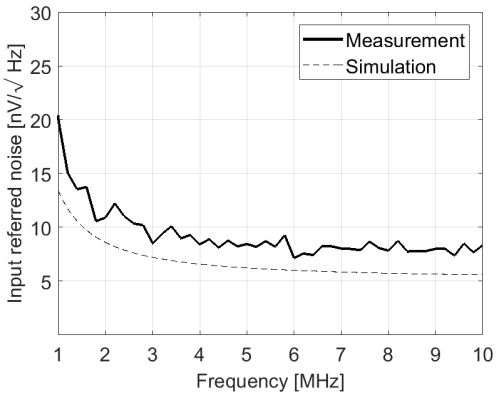


Fig. 13. Measured input-referred noise spectrum of the LNA, along with the corresponding simulation result.

per row. If multiple elements are selected, this attenuation becomes less. For instance, it decreases to 3.1 dB for four elements.

C. Logic

To implement the element-selection modes described in Section II-C, each element is equipped with a reconfigurable logic circuit (Fig. 9), which determines whether the element participates during transmit (TX_EN) and receive (RX_EN). The core of this circuit is a shift register consisting of 9 flip-flops for 9 RX-enable bits, 9 flip-flops for 9 TX-enable bits and 1 flip-flop for an element-enable bit (EL_EN), which allows a defective element to be disabled independent of the TX and RX enable bits. This element-enable bit is only part of the shift-register chain when PP=1, otherwise it is bypassed. This allows the element-enable bits to be pre-programmed only once, after which patterns can be updated without re-loading these bits. The output of the shift register is latched using two additional flip-flops, allowing the shift-register content to be updated without affecting the operation of the element. New content only becomes active after a rising edge of the latch signal.

The shift register is daisy-chained between neighboring elements in a row. The daisy-chain connection of the shift register allows the configuration bits to be shifted into a neighboring element, so as to realize the pattern-shifting

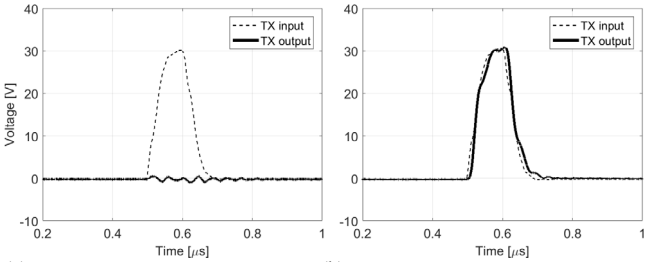


Fig. 14. Measured input and output of the transmit path, showing the operation of the high-voltage TX switch: (a) TX switch off; (b) TX switch on.

operation shown in Fig. 6. To be able to shift both left-to-right (LR) and right-to-left (RL) (cf. Figs. 6d and 6e), logic is included that can reverse the shift-register connections between neighboring elements, which is conceptually represented using switches in Fig. 9.

In the simplest mode of operation, only one of the 9 RX flip-flops and one of the 9 TX flip-flops is used; the remaining 8 bits are by-passed, so that only one RX bit and one TX bit need to be loaded per element to define whether the element is enabled during RX and TX. In order to pre-program 9 different patterns for fast pattern switching, as in Fig. 6c, this bypass is not used, allowing 9 bits to be loaded for RX and 9 bits for TX. After loading, the output of RX section of register is looped back to its input, as is the output of the TX section. Thus, the 9 pre-loaded enable bits can cyclically be applied.

Finally, the RX section of the register has a pseudo-random mode, in which this section is turned into a 9-bit linear-feedback shift register (LFSR) in which an XOR combination of two shift-register bits is fed back to the input. This causes the elements to be enabled for RX in a pseudo-random manner, which can be used to implement compressive sensing schemes. The 9 bits that are initially loaded into the RX-section act as a seed value for this LFSR. This allows different seed values to be used for different elements, causing them to exhibit a different pseudo-random pattern.

The various control signals needed to define the operating mode of the element level logic are provided by row-level logic. The row-level logic circuits together form a vertical shift register (see Fig. 4) through which each row can be configured independently.

IV. Experimental Results

A. Experimental Prototypes

The ASIC has been fabricated in 0.18 µm high-voltage BCDMOS process. Fig. 10 shows a photograph of a bare die and of a die after fabrication of the transducer array, and the floor-plan of a single element. The layout of the element-level TX and RX circuits is matched to the 150 µm transducer-element pitch.

The ASIC is wire-bonded to a stack of three printed-circuit boards (PCBs) with cable connectors (Fig. 11), which provide connections for the RX and TX channels as well as for power and control signals. After assembly, the prototype is covered by

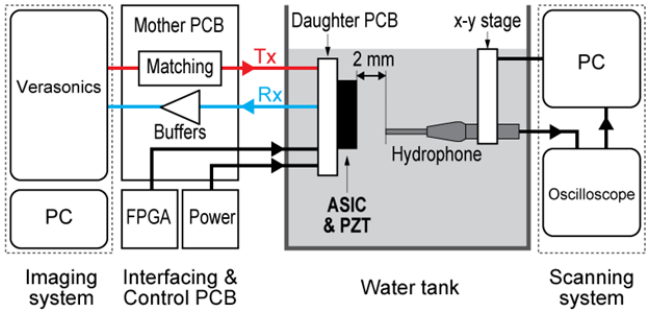


Fig. 15. Overview of the measurement setup used for acoustic characterization.

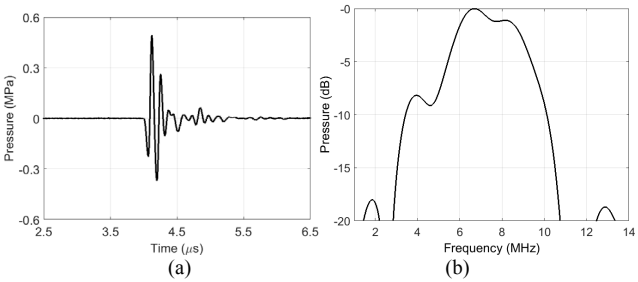


Fig. 16. Measured acoustic pressure recorded with a hydrophone: (a) time-domain waveform, (b) frequency spectrum.

a ground foil that forms the common ground electrode of the transducer elements, and by a moisture protection layer.

B. Electrical Characterization Results

For electrical characterization, a die without transducer array was used on which selected transducer bond pads were wire-bonded to the lowest PCB, to be able to apply external test signals to the ASIC and to measure the TX voltage produced by the ASIC.

Fig. 12 shows the measured transfer function of the receive circuit with the LNA in the signal path (LNA ON) and with the LNA bypassed (LNA OFF). The measured gains at the center frequency of 7.5 MHz are 18 dB and -2 dB, respectively. The gain step is in good agreement with the designed 20 dB gain of the LNA. The small attenuation observed for LNA OFF is due to capacitive division associated with the AC-coupling capacitors at the input of the LNA and the cable driver. The 1dB compression point is reached at a peak-to-peak input voltage of 74 mV with LNA on and at 750 mV with LNA off.

The noise performance of the LNA was measured by shorting the input of the LNA, measuring the output noise and referring this back to the input by dividing it by the transfer function. The resulting noise spectrum, shown in Fig. 13, is in good agreement with simulations. The measured input-referred noise density is 7.9 nV/√Hz at 7.5 MHz. Although this is higher than the noise level expected based on simulations, it is still less than the noise associated with the 6.8 kΩ impedance of the transducer (and substantially better than the noise level reported in [20], which was dominated by noise of off-chip components in the measurement setup). The difference with the simulated noise level may be due to noise picked up at the input of the LNA. In the electrical test, the LNA input was ground by

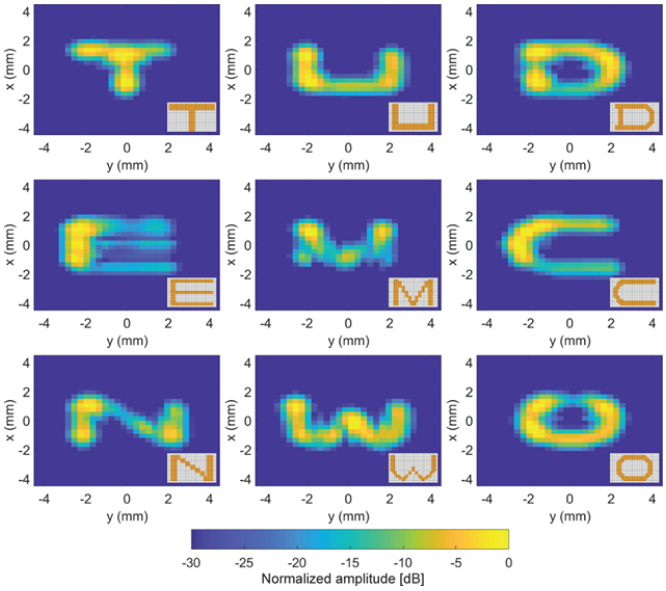


Fig. 17. Peak pressure recorded at 2 mm from the transducer array, using a hydrophone scanning a plane parallel to the array, for 9 pre-programmed transmit patterns.

wire-bonding a transducer bond pad to gnd on the PCB, instead of to gnd_foil, to which the LNA input is referenced (as shown in Fig. 8a). This was done because gnd_foil is not readily accessible for wire-bonding. We suspect that this different reference point is responsible for the additional noise. Integrated over the 40% fractional bandwidth of the transducer, the measured noise density leads to an input-referred rms noise of 13.7 μV, which is equivalent to an acoustic noise floor of 7.2 Pa.

To verify the operation of the bootstrap switch, we applied a 30 V peak-to-peak 200 ns pulse to one of the TX channels and probed the transducer bondpads. As Fig. 14 shows, the switch successfully propagates and isolates the HV signal.

C. *Acoustical Experiments*

The test-bench for acoustic experiments is shown in Fig. 15. The Verasonics imaging system generates the high-voltage TX signals. To prevent undershoot or overshoot voltages which could cause latch-up or junction breakdown, matching networks are included on the motherboard. The RX signals from the ASIC are buffered on the motherboard and fed into the Verasonics. The motherboard also provides supply voltages for analog, digital and 5V circuitry. The board also contains digital buffers to transfer control signals for row-level logic and element-level logic from the FPGA board.

Fig. 16 presents the acoustic pressure recorded with a 1 mm needle hydrophone placed at 50 mm when all elements are pulsed simultaneously. The TX signal is a unipolar half-cycle 7.5 MHz pulse with a peak value of 25 V. The recorded pressure has a maximum of 0.5 MPa. Its frequency spectrum shows a central frequency of 7.4 MHz and a -3 dB bandwidth of 44%. The measured bandwidth is in agreement with the expectation for a transducer built on top of an ASIC [21]. The measurement presents ringing after the main pulse due to acoustic reflection from the back side of the chip.

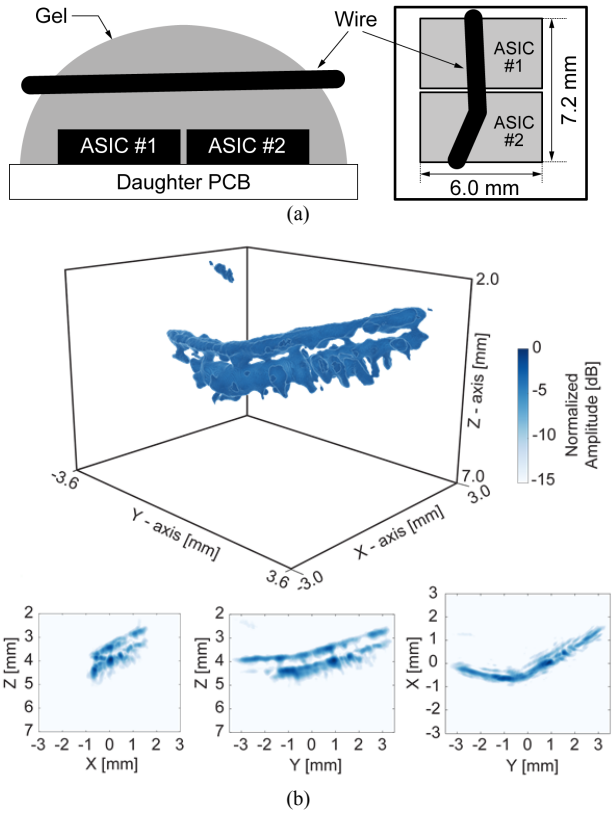


Fig. 18. (a) Setup with two ASIC tiled side-by-side for a 3D imaging experiment; (b) reconstructed volumetric images along with maximum projections.

To demonstrate fast reconfigurability of the ASIC, 9 different TX patterns were programmed in the element-level memory, allowing the ASIC to cyclically switch between these patterns in response to a single clock pulse (cf. Fig. 6c). The pressure in a C-plane (i.e. parallel to the transducer) at 2 mm from the transducer was recorded using a needle hydrophone placed on an x-y stage. Fig. 17 shows, for each of the 9 patterns, the measured peak acoustic pressure distribution in this plane, confirming that the ASIC is activating the elements in agreement with the pre-programmed patterns.

To demonstrate the 3D-imaging capability of the ASIC, an experiment with a prototype consisting of 2 × 1 tiled ASICs with a total of 1920 individual elements was performed. A bended metal wire phantom was placed above the prototype through acoustically transparent coupling gel, as illustrated in Fig. 18a. In this imaging experiment, we transmitted plane waves by enabling all elements for TX (cf. Fig. 5b), and received the echo signals column by column, by selecting one element per row for RX (cf. Fig. 5a), and shifting this pattern in 40 successive pulse-echo cycles (cf. Fig. 6d). Fig. 18b shows the volumetric image reconstructed from the recorded RX data set by means of standard delay-and-sum beamforming, envelope detection, log compression and 3D rendering using a 15 dB dynamic range. The wire is clearly visible, including strong acoustic reverberations behind the wire, attributed to the high acoustic-impedance mismatch between the metal and the gel. This imaging experiment successfully demonstrates the 3D-imaging capability of the prototype. Note that the imaging

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	[10]	[18]	[14]	**This work**
Transducer	CMUT	CMUT	PZT	PZT
Array size	32 × 32	16 × 16	32 × 32	24 × 40
Center freq.	5 MHz	5 MHz	5 MHz	7.5 MHz
Element Pitch	250 µm	250 µm	150 µm	150 µm
# of TX el.	960	256	64	960
# of RX el.	64	256	864	960
TX architecture	Element-level pulsers	Column/row parallel with element-level pulsers	Hard-wired TX sub-array	Row-parallel with element-level HV SW
RX architecture	Diagonal elements only	Column/row parallel with element-level LNAs	Sub-array beam-forming	Row-parallel with row-level LNAs
Pre-programmable element patterns	n/a	2	n/a	9 (shift pattern)
RX channel bandwidth	20 MHz	10.8 MHz	6.0 MHz	20 MHz
RX power/ch	4.5 mW	1.4 mW	0.27 mW	2 mW
RX input referred noise (mPa/√Hz)	-	2.3	1.0	4.2
TX amplitude	60 V	30 V	50 V	30 V
Process	0.25 µm HV	0.18 µm HV	0.18 µm LV	0.18 µm HV
ASIC size	9.2 × 9.2 mm^2	6 × 5.5 mm^2	6.1 × 6.1 mm^2	3.6 × 6.8 mm^2

quality of a complete 2 × 10 tiled array will be significantly better.

V. CONCLUSION

A reconfigurable ultrasound ASIC intended for 3-D volumetric imaging of the carotid artery has been presented in this paper. The ASIC, realized in a high-voltage 0.18 µm BCDMOS process, interfaces with an array of 24 × 40 transducer elements directly integrated on top of the ASIC, and can be tiled to realize larger apertures. Table II summarizes the ASIC's features and compares them with prior ASICs for 3D ultrasound imaging. This work stands out in its reconfigurability and integration density, with an element-matched layout with a 150 µm pitch. By using the proposed row-level architecture, the number of channels required to connect the 960 transducer elements to an imaging system is substantially reduced. Although the row-level architecture is less flexible in terms of possible element connections than the row-column-parallel architecture described in [18], it enables seamless tiling of multiple ASICs to realize large-aperture arrays. Every element is associated with a compact and power-efficient bootstrapped high-voltage TX switch and an RX switch. Compared to the pulsers used in [10], [18], [19], this allows for a broader range of transmit waveforms. The use of row-level LNAs rather than element-level LNAs, as in [18], [19], allows for more compact element-level circuits, at the expense of some attenuation associated with the loading presented by the RX bus. Element-level logic with programmable memory allows the selection of elements used for transmit and receive to be quickly reconfigured, allowing various imaging modes to be implemented. Compared to the design described in [18], which supports rapid switching between two pre-programmed patterns, more patterns can be pre-programmed, and more flexible pattern loading and shifting modes are supported, as well a pseudo-random selection mode. Acoustic measurements demonstrate the 3D-imaging capability of the implemented prototype.

ACKNOWLEDGMENT

The authors would like to thank Sofics for providing an ESD protection solution. The authors also acknowledge the help of Dr. Klaas-Jan de Langen of Sensixs for the valuable discussions.

REFERENCES

[1] T. G. Brott *et al.*, "2011 ASA/ACCF/AHA/AANN/AANS/ACR/ASNR/CNS/SAIP/SCAI/SIR/SNIS/SVM/SVS Guideline on the Management of Patients With Extracranial Carotid and Vertebral Artery Disease: Executive Summary," *Circulation*, vol. 124, no. 4, pp. 489–532, Jul. 2011.

[2] P. K. Shah, "Screening Asymptomatic Subjects for Subclinical Atherosclerosis," *Journal of the American College of Cardiology*, vol. 56, no. 2, pp. 98–105, Jul. 2010.

[3] S. Laurent *et al.*, "Expert consensus document on arterial stiffness: methodological issues and clinical applications," *European Heart Journal*, vol. 27, no. 21, pp. 2588–2605, Sep. 2006.

[4] P. Kruizinga, F. Mastik, J. G. Bosch, A. F. W. van der Steen and N. de Jong, "Carotid artery wall dynamics captured with multi-plane high-frame-rate imaging," *2015 IEEE International Ultrasonics Symposium (IUS)*, Taipei, 2015, pp. 1-4.

[5] M. Couade *et al.*, "Ultrafast imaging of the arterial pulse wave," *IRBM*, vol. 32, no. 2, pp. 106–108, Apr. 2011.

[6] H. Hasegawa, K. Hongo, and H. Kanai, "Measurement of regional pulse wave velocity using very high frame rate ultrasound," *J Med Ultrason (2001)*, vol. 40, no. 2, pp. 91–98, Apr. 2013.

[7] P. Kruizinga *et al.*, "High-Definition Imaging of Carotid Artery Wall Dynamics," *Ultrasound in Medicine & Biology*, vol. 40, no. 10, pp. 2392–2403, Oct. 2014.

[8] J. Provost *et al.*, "3D ultrafast ultrasound imaging in vivo," *Phys Med Biol*, vol. 59, no. 19, pp. L1–L13, Oct. 2014.

[9] I.O. Wygant, et al., "An integrated circuit with transmit beamforming flip-chip bonded to a 2-D CMUT array for 3-D ultrasound imaging," *IEEE Trans. on Ultrasonics, Ferroelectrics, and Frequency Control,* vol. 56, no. 10, pp. 2145-2156, Oct. 2009.

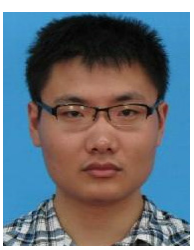
[10] A. Bhuyan et al., "Integrated Circuits for Volumetric Ultrasound Imaging With 2-D CMUT Arrays," *IEEE Trans. on Biomedical Circuits and Systems*, vol. 7, no. 6, pp. 796–804, Dec. 2013.

[11] K. Chen, et al., "Ultrasonic Imaging Transceiver Design for CMUT: A Three-Level 30-Vpp Pulse-Shaping Pulser With Improved Efficiency and a Noise-Optimized Receiver," *IEEE Journal of Solid-State Circuits,* vol. 48, no. 11, pp. 2734–2745, Nov. 2013.

[12] Y. Katsube, et al., "Single-Chip 3072ch 2D Array IC with RX Analog and All-Digital TX Beamformer for 3D Ultrasound Imaging," in *Int. Solid-State Circuits Conf. Dig. Techn. Papers,* pp. 458-459, Feb. 2017.

[13] B. Savord and R. Solomon, “Fully sampled matrix transducer for real time 3D ultrasonic imaging,” in *Proc. IEEE Ultrasonics Symp.*, pp. 945-953, Oct. 2003.
[14] C. Chen et al., “A Front-End ASIC With Receive Sub-array Beamforming Integrated With a 32 x 32 PZT Matrix Transducer for 3-D Transesophageal Echocardiography,” *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 994– 1006, Apr. 2017.
[15] S. Tamano, et al., “3D ultrasound imaging system using Fresnel ring array & high voltage multiplexer IC,” in *Proc. IEEE Ultrasonics Symp.,* pp. 782-785, Aug. 2004.
[16] R. Fisher, et al., “Reconfigurable Arrays for Portable Ultrasound,” in *Proc. IEEE Ultrasonics Symp.*, pp. 495–499, Sept. 2005.
[17] B.-H. Kim, et al., “Design and Test of A Fully Controllable 64x128 2-D CMUT Array Integrated with Reconfigurable Frontend ASICs for Volumetric Ultrasound Imaging,” in *Proc. IEEE Ultrasonics Symp.,* pp. 77–80, Oct. 2012.
[18] K. Chen et al., “A Column-Row-Parallel ASIC Architecture for 3-D Portable Medical Ultrasonic Imaging,” *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 738–751, Mar. 2016.
[19] S. J. Jung, J. K. Song and O. K. Kwon, "Three-Side Buttable Integrated Ultrasound Chip With a 16x16 Reconfigurable Transceiver and Capacitive Micromachined Ultrasonic Transducer Array for 3-D Ultrasound Imaging Systems," in IEEE Transactions on Electron Devices, vol. 60, no. 10, pp. 3562-3569, Oct. 2013.
[20] E. Kang, et al., “A reconfigurable 24 x 40 element transceiver ASIC for compact 3D medical ultrasound probes,” in *Proc. European Solid-State Circuits Conference (ESSCIRC)*. Sep. 2017, pp. 211-214.
[21] C. Chen, et al., “A prototype PZT matrix transducer with low-power integrated receive ASIC for 3D transesophageal echocardiography,” *IEEE Trans. on Ultrasonics, Ferroelectrics,and Frequency Control*, vol. 63, no. 1, p. 47-59, Jan. 2016.
[22] H.-K. Cha, D. Zhao, J.H.Cheong, B.Guo, H.Yu, and M. Je, “A CMOS high-voltage transmitter IC for ultrasound medical imaging applications,” *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 60, no. 6, pp. 316–320, Jun. 2013.
[23] D. Zhao *et al.*, “High-voltage pulser for ultrasound medical imaging applications,” in *Proc. 13th Int. Symp. Integrated Circuits (ISIC)*, 2011, pp. 408–411.
[24] M. Sautto, et al., “A CMUT transceiver front-end with 100-V TX driver and 1-mW low-noise capacitive feedback RX amplifier in BCD-SOI technology”, in *Proc. ESSCIRC*, Sept. 2014, pp. 407-410.
[25] D. Bianchi, F. Quaglia, A. Mazzanti and F. Svelto, "Analysis and Design of a High Voltage Integrated Class-B Amplifier for Ultra-Sound Transducers," *IEEE Trans. on Circuits and Systems I: RegularPapers*, vol. 61, no. 7, pp. 1942-1951, July 2014.
[26] K. Hara, *et al.,* "A New 80v 32x32ch low loss multiplexer LSI for a 3d ultrasound imaging system," in *Proc. Int. Symposium on Power Semiconductor Devices and ICs,* May 2005, pp. 359-362.
[27] A. J. Lopez-Martin, J. Ramirez-Angulo, R. G. Carvajal, and L. Acosta, “Power-efficient class AB CMOS buffer,” *Electron. Lett.*, vol. 45, no. 2, pp. 89–90, Jan. 2009.
[28] Kruizinga, Pieter, et al. "Compressive 3D ultrasound imaging using a single sensor." *Science advances* 3.12 (2017): e1701423.

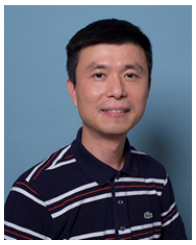
Eunchul Kang received the B.S. and M.S. degrees in electronic engineering from Sogang University, Seoul, Korea, in 2005 and 2007, respectively. He has working and researching experiences with Fairchild Semiconductor, Silicon Mitus, and Inter- university Semiconductor Research Center in Korea. Since February 2016, he has been a Ph.D candidate in the Electronic Instrumentation Laboratory at TU Delft, where he works on ultrasound ASIC design.



Qing Ding (S’14) received the M.Sc. degrees in microelectronic engineering from Tsinghua University, Beijing, China and in electrical engineering from Katholieke Universiteit Leuven, Leuven, Belgium respectively in 2014. He joined the Electronic Instrumentation Laboratory, Delft University of Technology, The Netherlands, as a researcher involving ASIC design for the ultrasound system from 2014 to 2016. Since 2016, he has been working as analog design engineer for Sony Depthsensing Solutions (formerly Softkinetic), Brussels, Belgium, where he works on 3D TOF image sensor design.

Maysam Shabanimotlagh was born in Iran on 26th July 1985. He received his BSc and MSc degree in Mechanical Engineering, both in Iran University of Science and Technology in 2008 and 2010, respectively. His focus was on of acoustical properties of smart material, especially the functionally graded materials and magnetorheological fluids/elastomers. During 2010 and 2013, as a researcher he worked on the sensor/actuator capabilities of magnetorheological and magnetostrictive materials, at mechatronics laboratory of Tarbiat Modares University, Tehran, Iran. In 2013 he moved to the Netherlands to start a PhD program in laboratory of Acoustic Wavefield Imaging at Technical University of Delft. He is now persuading his research on acoustical design, fabrication and characterization of ultrasound matrix transducers for medical imaging applications.

Pieter Kruizinga received his BSc degree in Biomedical Engineering at the University of Twente in 2006 and his MSc degree in Biomedical Engineering at the Delft University of Technology in 2010. For his master research he visited the Ultrasound Imaging and Therapeutics Research Laboratory at the University of Texas at Austin, USA for one year, where he worked on contrast enhancement in photoacoustic imaging. Pieter obtained his PhD, in 2015, at the Department of Biomedical Engineering of the Thorax Center, Erasmus MC, Rotterdam on the development of high frame rate ultrasound and photoacoustic imaging applied to the human carotid artery. His current postdoctoral research focusses on high frame rate imaging in 3D, compressive imaging and functional ultrasound.



Zu-yao Chang received the M.Sc. degree in electrical engineering from Delft University of Technology, Delft, The Netherlands, in 2003. Since 2003, he has been a Staff Member with the Electronic Instrumentation Laboratory, Delft University of Technology, working on impedance measurement systems and smart sensor systems.

Emile Noothout graduated from Intermediate Technical School for Mechanics, Dordrecht, The Netherlands, in 2004. Then, he studied for Research Instrument Maker at Leidse Instrumentmaker School, Leiden, The Netherlands, from 2004 to 2006.

From 2007 to 2013, he worked as a Research Instrument Maker with TNO, Delft, The Netherlands. Since 2013, he has been working with Delft University of Technology, Delft, The Netherlands, for the development of medical ultrasound transducers and research assistance.

Hendrik J. Vos received the M.Sc. degree in applied physics from Delft University of Technology, Delft, The Netherlands in 2004, and his Ph.D. degree with the Department of Biomedical Engineering at Erasmus MC, Rotterdam, The Netherlands, in 2010. He worked as a Postmaster Researcher with the University of Florence, Italy, and as a contract researcher for the petrochemical industry on cutting-edge ultrasonic solutions. He currently is assistant professor with Erasmus MC. His research interests include acoustical array technology for biomedical imaging in all its aspects: transducers, 2-D and 3-D beamforming, cardiac shear waves, ultrafast Doppler, contrast imaging, and related subclinical and clinical studies.

Johan G. Bosch is an Associate Professor and staff member at the Department of Biomedical Engineering, Thoraxcenter, Erasmus MC, Rotterdam. He is specialized in 2D and 3D echocardiographic image processing / analysis and transducer development. Main research interests are optimal border detection approaches, geometrical and statistical models, and anatomical and physical knowledge representations for border detection. He is currently leader of projects on 3D segmentation and 3D ultrasound guidance in electrophysiology and participates in several projects, e.g. on 3D transducer development, 2D and 3D carotid imaging, and 3D TEE imaging.

He obtained his MSc in Electrical Engineering at Eindhoven University of Technology in 1985. He performed ultrasound and image processing research at Erasmus University Rotterdam and Leiden University. From 1995-2005, he was Assistant Professor and head of the Echocardiography section at the Division of Image Processing (LKEB), Department of Radiology, Leiden University Medical Center, where he obtained his PhD in 2006.

Martin D. Verweij (M'10) received the M.Sc. (cum laude) and Ph.D. degrees in electrical engineering from Delft University of Technology, Delft, The Netherlands, in 1988 and 1992, respectively. From 1993 to 1997, he was a Research Fellow with the Royal Netherlands Academy of Arts and Sciences, Amsterdam, The Netherlands. In 1998, he became an Associate Professor with the Laboratory of Electromagnetic Research, Delft University of Technology, where he joined the Laboratory of Acoustical Wavefield Imaging in 2011. His research interests include dedicated transducer design, beamforming algorithms, and the theoretical modeling and numerical simulation of medical ultrasound. Dr. Verweij is an Associate Editor of the Journal of the Acoustical Society of America.

Nico de Jong (A'97–M'09) received the M.Sc. degree in physics from Delft University of Technology, The Netherlands, in 1978 and the Ph.D. degree for "Acoustic properties of ultrasound contrast agents" from the Erasmus Medical Center, Rotterdam, The Netherlands, in 1993.

Since 1980, he is a Staff Member with the Thoraxcenter, Erasmus Medical Center, Rotterdam, The Netherlands. In 2003, he became a part-time Professor with the University of Twente, Enschede, The Netherlands. Over the last 5 years, he has given more than 30 invited lectures and has given numerous scientific presentations for international industries. He teaches on Technical Universities and the Erasmus MC. He has been the promotor of 21 Ph.D. students and is currently supervising 11 Ph.D. students. Since October 2011, he is a Professor in Molecular Ultrasonic Imaging and Therapy with the Erasmus MC and the Technical University of Delft, Delft, The Netherlands.

Dr. de Jong is an Organizer of the annual European Symposium on Ultrasound Contrast Imaging, held in Rotterdam and attended by approximately 175 scientists from universities and industries all over the world. He is on the safety committee of World Federation of Ultrasound in Medicine and Biology (WFUMB), Associate Editor of UMB, and has been Guest Editor for special issues of different journals.

Michiel A. P. Pertijs (S'99–M'06–SM'10) received the M.Sc. and Ph.D. degrees in electrical engineering (both cum laude) from Delft University of Technology, Delft, The Netherlands, in 2000 and 2005, respectively. From 2005 to 2008, he was with National Semiconductor, Delft, where he designed precision operational amplifiers and instrumentation amplifiers. From 2008 to 2009, he was a Senior Researcher with imec / Holst Centre, Eindhoven, The Netherlands. In 2009, he joined the Electronic Instrumentation Laboratory of Delft University of Technology, where he is now an Associate Professor. He heads a research group focusing on integrated circuits for medical ultrasound and energy-efficient smart sensors. He has authored or co-authored two books, three book chapters, 12 patents, and over 85 technical papers.

Dr. Pertijs served as an Associate Editor of the IEEE Journal of Solid-State Circuits (JSSC). He is a member of the technical program committee the European Solid-State Circuits Conference (ESSCIRC), and also served on the program committees of the International Solid-State Circuits Conference (ISSCC) and the IEEE Sensors Conference. He received the ISSCC 2005 Jack Kilby Award for Outstanding Student Paper and the JSSC 2005 Best Paper Award. For his Ph.D. research on high-accuracy CMOS smart temperature sensors, he received the 2006 Simon Stevin Gezel Award from the Dutch Technology Foundation STW. In 2014, he was elected Best Teacher of the EE program at Delft University of Technology.