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# A 125 $\mu\text{m}$ -Pitch-Matched Transceiver ASIC With Micro-Beamforming ADC and Multi-Level Signaling for 3-D Transfontanelle Ultrasonography

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**Abstract**—This article presents a pitch-matched transceiver application-specific integrated circuit (ASIC) for a wearable ultrasound device intended for transfontanelle ultrasonography, which includes element-level 20-V unipolar pulsers with transmit (TX) beamforming, and receive (RX) circuitry that combines eightfold multiplexing, four-channel micro-beamforming ( $\mu\text{BF}$ ), and subgroup-level digitization to achieve an initial 32-fold channel-count reduction. The  $\mu\text{BF}$  is based on passive boxcar integration, merged with a 10-bit 40 MS/s SAR ADC in the charge domain, thus obviating the need for explicit anti-alias filtering (AAF) and power-hungry ADC drivers. A compact and low-power reference generator employs an area-efficient MOS capacitor as a reservoir to quickly set a reference for the ADC in the charge domain. A low-power multi-level data link, based on 16-level pulse-amplitude modulation, concatenates the outputs of four ADCs, providing an overall 128-fold channel-count reduction. A prototype transceiver ASIC was fabricated in a 180-nm BCD technology, and interfaces with a 2-D PZT transducer array of  $16 \times 16$  elements with a pitch of 125  $\mu\text{m}$  and a center frequency of 9 MHz. The ASIC consumes 1.83 mW/element. The data link achieves an aggregate 3.84 Gb/s data rate with 3.3 pJ/bit energy efficiency. The ASIC's functionality has been demonstrated through electrical, acoustic, and imaging experiments.

**Index Terms**—Application-specific integrated circuit (ASIC), micro-beamformer, pitch-matched analog front-end (AFE), sub-array beamforming, ultrasound imaging.

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## I. INTRODUCTION

INADEQUATE brain perfusion regularly shown in preterm infants exposes the developing brain to injury that could have severe consequences in later life [1]. Bedside monitoring of brain perfusion via trans-fontanelle ultrasonography (TFUS) has an added benefit, especially for high-risk neonates [2], [3]. To match fontanelle size and generate high-resolution 3-D images for visualizing the sub-millimeter vessels of neonates, a wearable probe with an aperture of  $20 \times 10 \text{ mm}^2$  and a 2-D array of  $>10\,000$  transducer elements would be required [4], featuring small pitch and high central frequency. This poses significant challenges for the electronics design of such a probe, such as interconnecting the transducer elements to power-efficient front-end circuits that interface with the elements to transmit (TX) acoustic pulses and receive (RX) the resulting high-frequency echo signals. A pitch-matched application-specific integrated circuit (ASIC) directly integrated with a 2-D transducer array is a proven solution to the interconnection problem [5]. However, techniques are still required that can effectively reduce the RX output channel count to much less than the number of transducer elements.

Various techniques have been reported to reduce the channel count. Time-division multiplexing (TDM), applied at the input of an RX analog front-end (AFE), allows the AFE to interface with multiple transducer elements in successive pulse-echo cycles at the cost of reduced frame rate [6]. When applied at the RX output, TDM allows multiple RX channels to share a single output by assigning each channel a dedicated time slot. However, the limited bandwidth of the output channel (e.g., PCB trace or cable) leads to inter-symbol interference (ISI) and deteriorates the signal-to-noise ratio (SNR) [7]. Frequency-division multiplexing (FDM) [8] also allows multiple RX channels to share an output by modulating the signal of each channel to a different frequency band, while it also suffers from crosstalk. Micro-beamforming ( $\mu\text{BF}$ ) [9], [10] divides the transducer array into sub-arrays of  $N$  elements, and combines the echo signals received in each sub-array by means of an analog delay-and-sum (DAS) operation, effectively reducing the channel count by a factor of  $N$ , at the cost of reduced frame rate and somewhat degraded image quality [11], [12], [13]. ON-chip digitization of the echo signals allows

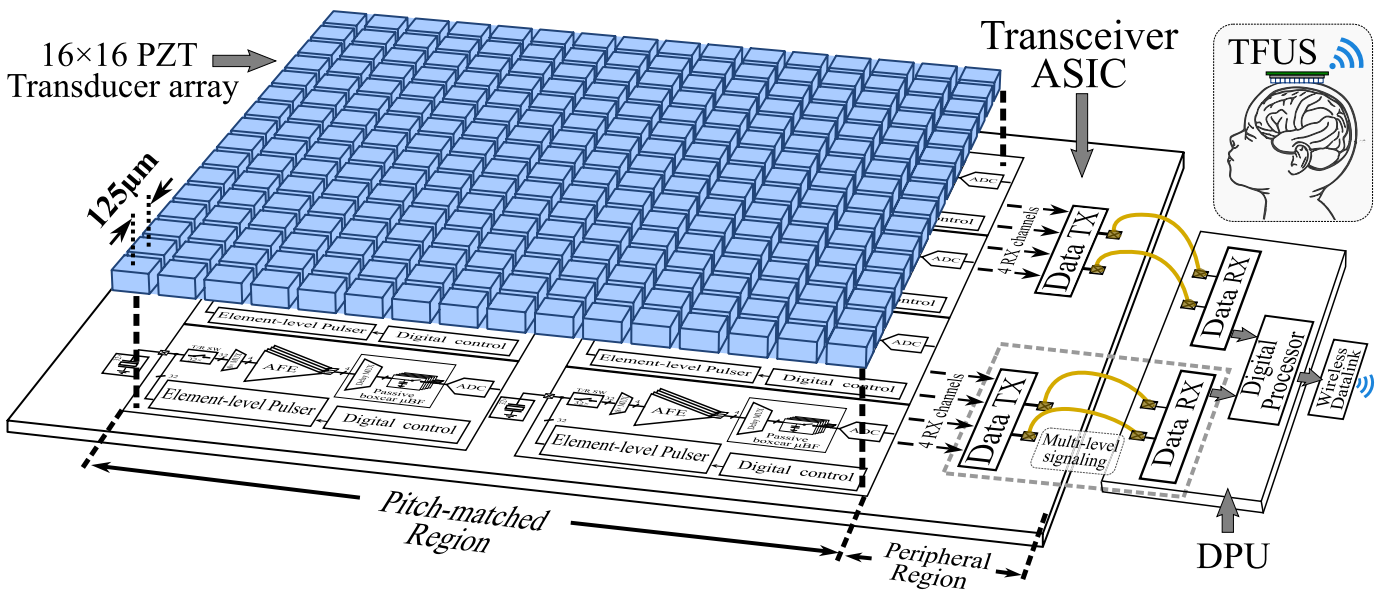


Fig. 1. System overview of the envisioned wearable device for TFUS, including a transceiver ASIC prototype connecting to a DPU as a proof of concept.

for concatenating multiple RX outputs to a serialized output, thus reducing the channel count, at the cost of increased power consumption [14], [15]. State-of-the-art designs often combine several of the aforementioned approaches to achieve an optimal balance between channel-count reduction, frame rate, image quality, and power consumption [14], [16], [17].

The performance of ON-chip digitization and subsequent digital processing is limited by the relatively mature high-voltage (HV) technology required to implement the HV pulsers needed to generate sufficient ultrasound pressure in TX [18], [19], since mainstream HV technology nodes still remain above 90 nm [20] and are not optimized for complex digital signal processing. Advanced packaging techniques, e.g., [21], allow for integrating an HV transceiver ASIC with a high-speed data processing unit (DPU), realized in a deeper sub-micrometer technology, in a single package. However, a low-power and compact ON-chip digitization scheme and a power-efficient data link are still prerequisites for such a transceiver ASIC.

An element-level digitization scheme was reported in [22], where  $\Delta\Sigma$  modulators directly digitize the echo signals from each transducer element, followed by digital beamforming in the chip's periphery, requiring  $I^2$  ADCs for a  $I \times I$  transducer array. The scheme is associated with high-power consumption as well as large areas. Alternatively, the digitization can be done at the output of a  $\mu\text{BF}$  [14], [15], effectively reducing the total channel count, the number of ADCs and the associated power consumption by a factor of  $N$ , where  $N$  is again the number of elements in a sub-array. The outputs of a group of  $M$  ADCs can be serialized by the following data link, e.g., employing low-voltage differential signaling (LVDS) [14], [15], realizing an additional  $M \times$  channel-count reduction. However, the LVDS data link consumes excessive power per channel in HV technologies, e.g., roughly 50% of the power is consumed by the LVDS data link in a 180-nm BCD technology in [14]. In ASICs for catheter-based systems, which are located at the catheter tip and TX data via a cable to an imaging

system, load modulation (LM) techniques have been used to reduce the power consumed in the ASIC at the expense of higher power consumption on the system side [6], [23]. This approach is not suitable for our system [4], [24], since data reception takes place in the local DPU and hence is also power constrained. A more suitable alternative is multi-level signaling (MLS) [25], which TXs and RXs multiple bits of data per symbol by using a multi-level signal that can be efficiently received in the DPU. Compared to LVDS, MLS compresses the bandwidth and the signal level, allowing for a decrease in dynamic power consumption proportional to  $fCV^2$ .

Fig. 1 depicts the envisioned wearable device for TFUS, comprising a transceiver ASIC, a companion DPU and other peripheral modules, such as a wireless module. The acquired ultrasound data is transmitted to the DPU, where it is further processed and compressed before being offloaded to a remote imaging system (not shown) via a wireless data link [24]. As a crucial step toward the final device, this work presents a pitch-matched transceiver ASIC prototype that is directly integrated with a  $16 \times 16$  transducer array with  $125\text{-}\mu\text{m}$  pitch and 9-MHz center frequency as depicted in Fig. 1, leading to an aperture of  $2 \times 2 \text{ mm}^2$ . A novel low-power RX architecture is implemented to reduce the number of RX channels by a factor of 128. The ASIC can be divided into two regions: a pitch-matched region where the ASIC layout needs to strictly match the transducer pitch, and a peripheral region where the layout requirement is more relaxed. Fig. 1 also shows that an envisioned DPU, consisting of data RX and the following digital processor, is connected to the transceiver ASIC via bonding wires, while other advanced packaging techniques such as through silicon vias (TSVs) is also a possible choice. In contrast with other ultrasound applications, such as catheter-based probes, in which the data transmitter (D-TX) drives a long coaxial cable [6], our application aims at processing all the ultrasound data inside the wearable device and transmitting the image volume data via a wireless link. Therefore, only a short-range data link is required in the transceiver ASIC.





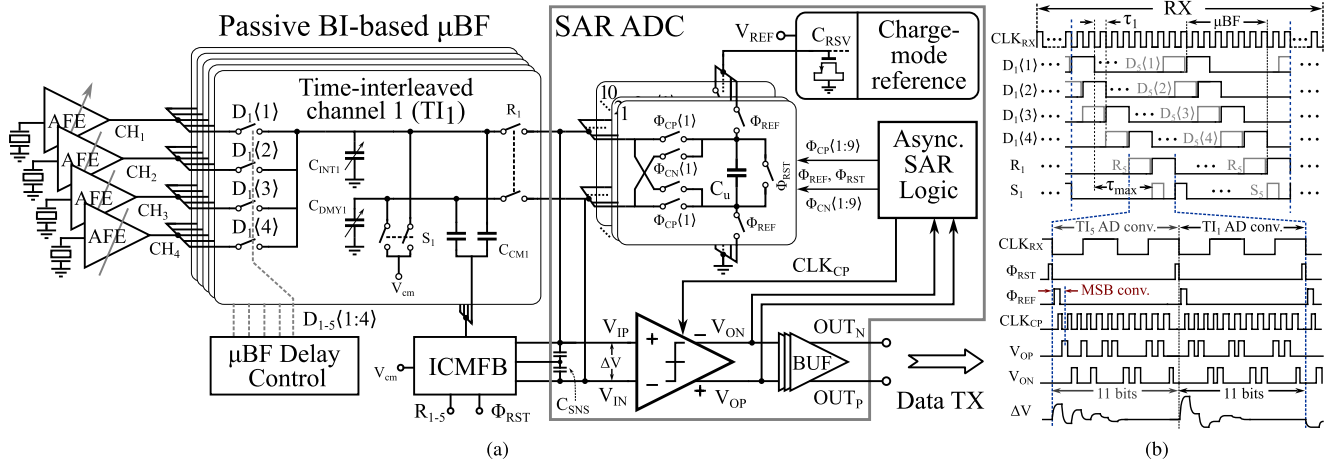


Fig. 4. (a) Circuit diagram of the passive BI-based  $\mu\text{BF}$  ADC and (b) related timing details.

### C. Passive BI-Based $\mu\text{BF}$ ADC

Fig. 4(a) shows a circuit diagram of the BI-based  $\mu\text{BF}$  ADC. Similar to the BI-based  $\mu\text{BF}$  described in [4], it implements a sum-and-delay operation, in which the output currents from four AFEs are cyclically steered into one of five integration capacitors  $C_{\text{INT}1-5}$  to realize boxcar integration. The  $\mu\text{BF}$  delays are defined through the relative timing of the switch control signals  $D_{1-5}\langle 1:4 \rangle$ . For instance, the delay between channel 1 ( $\text{CH}_1$ ) and channel 2 ( $\text{CH}_2$ ) is set by the time-shift  $\tau_1$  between  $D_{1-5}\langle 1 \rangle$  and  $D_{1-5}\langle 2 \rangle$ . The integration capacitors are cyclically connected to the ADC by read switches  $R_{1-5}$ .

The switch timing is orchestrated by an 80-MHz clock ( $\text{CLK}_{\text{RX}}$ ), providing a delay resolution of 12.5 ns and a boxcar integration time of 25 ns, corresponding to a sampling rate of 40 MS/s. To accommodate a maximum delay ( $\tau_{\text{max}}$ ) of 62.5 ns, five TI channels are used.

In contrast with the active integrators used in [4], our design employs passive boxcar integration to save area and power while retaining the merits of boxcar integration such as the built-in anti-alias filtering (AAF). Moreover, this passive-integration topology allows capacitors  $C_{\text{INT}1-5}$  to be connected directly to the following charge-sharing SAR ADC during the read phase  $R_{1-5}$  [14]. It is well-known that boxcar integration may be affected by clock skew and jitter [27]. However, a clean clock source is available in this system, thereby avoiding deterioration of the overall SNR. To convert the single-ended signal to a differential input for the ADC, a set of dummy capacitor  $C_{\text{DMY}1-5}$  is added, and an input common-mode feedback (ICMFB) circuit senses the common-mode (CM) voltage at the input of the ADC through capacitors  $C_{\text{SNS}}$  and regulates it to a CM reference  $V_{\text{cm}}$  through capacitors  $C_{\text{CM}1-5}$ , thus creating a differential signal charge on  $C_{\text{INT}1-5}$  and  $C_{\text{DMY}1-5}$ .

The ADC subsequently digitizes the  $\mu\text{BF}$  signal in the charge domain. It consists of a capacitive DAC (CDAC), a comparator, and SAR logic. It digitizes the signal charge by neutralizing it in a successive approximation process, in which the CDAC capacitors are connected in parallel or anti-parallel to the ADC's input [28]. During the MSB conversion as depicted in Fig. 4(b), the SAR comparator first decides polarity of the differential voltage ( $\Delta V$ ) on the integration capacitors

(e.g.,  $C_{\text{INT}1}$  and  $C_{\text{DMY}1}$ ). Meanwhile, during  $\Phi_{\text{REF}}$ , the CDAC array is quickly charged to  $V_{\text{REF}}$  by sharing charge with a pre-charged reservoir capacitor  $C_{\text{RSV}}$ . This charge-mode operation allows for very fast settling of the reference voltage within the MSB conversion, without adding extra time to the AD conversion. Afterward, the binary-scaled unit capacitors ( $C_u$ ) of 28-fF each, similar to those in [29], are sequentially connected to the input of the SAR comparator ( $V_{\text{IP}}$ ,  $V_{\text{IN}}$ ) in either parallel or antiparallel configuration for the next comparison, depending on the previous decision made by the comparator, until the next 9 bits plus 1 redundant bit have all been decided, providing a total 11-bit data in one conversion cycle of the ADC. The redundant bit provides immunity to settling errors, such as those of the ICMFB and the CDAC. The associated correction is carried out in the background by using the same algorithm as described in [29].

Finally, the CDAC array is reset ( $\Phi_{\text{RST}}$ ) in preparation for the next AD conversion. After digitization, the residual differential charge on the integration capacitors ( $C_{\text{INT}1-5}$ ,  $C_{\text{DMY}1-5}$ ) is nulled during reset phase  $S_{1-5}$ . Asynchronous SAR logic is employed to avoid distributing a high-frequency clock over the whole chip. This implementation combines the BI-based  $\mu\text{BF}$  with an SAR ADC in the charge domain, thereby eliminating the need for both a power-hungry ADC driver and an explicit AAF.

Channel-to-channel matching in this architecture is limited by capacitor matching, which is expected to be much better than the matching between the transducer elements. If required, correction for gain mismatch could be performed in the DPU, but this was not needed in our prototype.

### D. D-TX

In a mainstream BCD technology, the realization of an efficient D-TX can be challenging due to the relatively low cut-off frequencies of the MOS transistors. For example, in a 180-nm process, they are about 60/30 GHz for NMOS/PMOS, respectively [30], resulting in a quick drop of the data-link energy efficiency for an LVDS transceiver operating at sub-10 GHz frequencies [31]. MLS, e.g.,  $M$ -level pulse amplitude modulation (PAM- $M$ ) can significantly improve energy efficiency by transmitting multi-bit data per symbol. However,

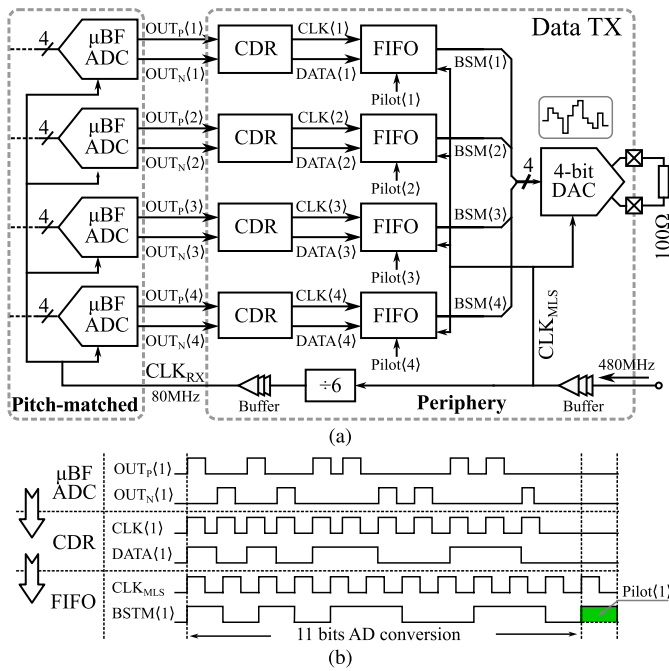


Fig. 5. (a) D-TX architecture consisting of CDR, FIFO, and a 4-bit DAC. (b) Associated timing diagram.

higher-order PAM reduces the signal level and the related SNR per bit, defined as the ratio of signal energy per bit to channel noise density ( $E_b/N_0$ ), resulting in a poorer bit error rate (BER) [32]. Insufficient channel bandwidth further reduces  $E_b/N_0$  and the associated eye width and causes ISI. All these restrict the use of high-order PAM for high-quality, middle/long-range communications. For example, A BER  $<10^{-12}$  is required for a long distance of  $>25$  m, according to the 1000BASE-X standard [33]. As a result, PAM-4/8 is more extensively used than PAM-16 or even higher order in the prior art [31], [34], [35].

However, PAM-16 is adopted in this work due to the fact that: 1) the data-link channel in our application, i.e., the inter-chip communication within a single package, is formed by very short interconnections such as bonding wires, which only inflict slight attenuation and ISI on the transmitted signals [36]; 2) a relatively poor BER objective of  $10^{-6}$  is quite tolerable for ultrasound imaging applications [37], thereby easing the requirement of the SNR per bit; and 3) a PAM-16 receiver with the reported energy efficiency of 1.5 pJ/bit could be realized, leveraged by more advanced technologies [38], [39], thus obtaining an overall data-link power optimization.

As depicted in Fig. 5(a), the differential outputs of four ADCs are transmitted to a D-TX at the chip's periphery where clock data recovery (CDR) circuits first recover the clock and data for each ADC, followed by four first-in, first-out buffers (FIFOs) that synchronize the data with the MLS clock signal ( $CLK_{MLS}$ ), and insert a pilot bit (e.g., Pilot(1)) periodically in every 11 ADC data bits, before concatenating four of such bitstreams into a 4-bit data [see Fig. 5(b)]. The pilot pattern facilitates a fast recognition of the data header on the data RX (D-RX) side. A 4-bit current-steering DAC then converts the 4-bit data into a 16-level current signal and drives a 100- $\Omega$  load resistor, allowing an external PAM-16 data RX to

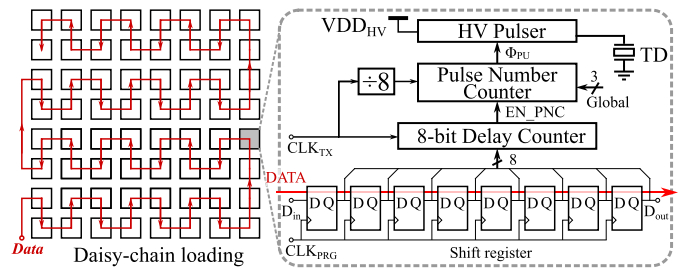


Fig. 6. Quadrant of daisy-chained shift register that stores the beamforming delays for  $8 \times 8$  transducer elements, and the associated element-level TX architecture.

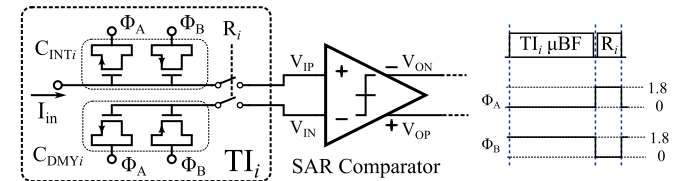


Fig. 7. Passive amplification and the associated timing diagram.

recover the 4-bit data, as will be elaborated in Section III-E. DC-coupled transmission is chosen instead of ac coupling, avoiding the need for a dedicated dc-balance encoder [40] and the related digital circuitry. Unlike an LVDS data link which would require a power-hungry PLL or DLL to generate the clock for an LVDS transmitter [14], [41], the PAM-16 D-TX is directly driven by a low-frequency, 480-MHz clock ( $CLK_{MLS}$ ), thus making it a compact and low-power data-link scheme.

### E. TX Architecture

As depicted in Fig. 6, to generate 20-V pulses with TX beamforming, an element-level TX comprising an 8-bit shift register, an 8-bit delay counter, a 3-bit pulse-number counter, and an HV pulser is employed. Controlled by a 72-MHz clock signal  $CLK_{TX}$ , it achieves a minimum delay resolution of 13.9 ns, a maximum number of 255 delay steps, and a programmable number of pulses from 1 to 8. The 8-bit shift register is daisy-chained in a quadrant of the pitch-matched layout, corresponding to  $8 \times 8$  transducer elements, and can be programmed by using a clock ( $CLK_{PRG}$ ) with a frequency up to 120 MHz, resulting in a total programming time of 4.8  $\mu$ s for loading the TX beamforming delay profile for all four of quadrants. At the start of the TX phase, the 8-bit delay counter loads the delay profile from the shift register and sends an enable signal (EN\_PNC) to the pulse-number counter after the counting ends. Controlled by a 9-MHz clock signal derived from  $CLK_{TX}$ , the pulse-number counter generates a number of pulses to drive the HV pulser, and provides a pulse duration of 55.6 ns. This TX scheme allows for transmitting various TX beam patterns, such as plane waves, diverging waves, or focused wave patterns.

## III. CIRCUIT DESIGN

### A. Passive Amplification of the $\mu$ BF ADC

Capacitors  $C_{INT1-5}$  and  $C_{DMY1-5}$  shown in Fig. 4(a) are all varactors built using NMOS and PMOS capacitors [29]. As depicted in Fig. 7, in each TI channel ( $TI_i$ ), these capacitors are driven into their inversion region during  $\mu$ BF by

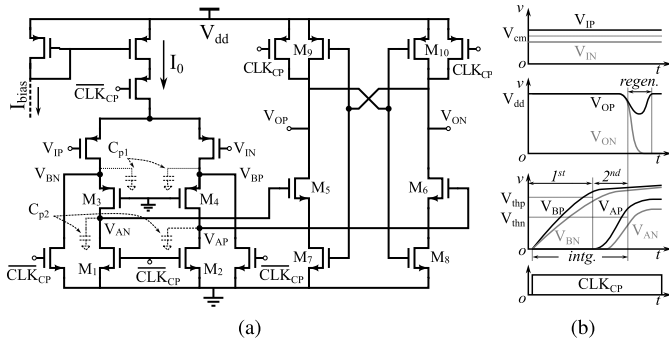


Fig. 8. (a) Circuit diagram of the dynamic comparator. (b) Associated waveforms as a function of time.

connecting the source/drain (S/D) of the NMOS to ground, while connecting the S/D of the PMOS to the supply, thus maximizing their capacitances and effectively reducing the voltage swing during the boxcar integration. The use of 6-pF MOS capacitors in their inversion region limits the voltage swing to below 300 mV at AFE's output in this work. In the following read phase  $R_i$ , when the capacitors are connected to the input nodes of the SAR comparator ( $V_{IP}, V_{IN}$ ), they are driven into their depletion region by reversing the S/D voltages, thus reducing the capacitances by a factor of about 3. Due to charge conservation, this causes the associated differential voltage on the capacitors to be amplified [42], which effectively relaxes the noise requirement of the SAR comparator [29].

### B. Dynamic Comparator of the SAR ADC

Fig. 8(a) shows that the dynamic comparator, consisting of a preamplifier and a regenerative latch, decides the polarity during the AD conversion, and operates in a two-step fashion: first, amplification of the differential input signal ( $V_{IP}-V_{IN}$ ) and then regeneration of the amplified signal ( $V_{AP}-V_{AN}$ ) via a latch structure.

The preamplifier is based on a dynamic integrator [43], that employs a cascoded structure, realizing a double integration in contrast with a single-integration-based preamplifier, such as that used in [44], thus effectively increasing the gain of the preamplifier. Moreover, in contrast with [44], a tail current  $I_0$  is employed in our design, which, in combination with the aforementioned ICMFB, rejects CM disturbances, such as those from the power supply.

As depicted in Fig. 8(b), the double integration scheme allows for an extended voltage headroom, and the resulting large gain mitigates the non-ideal components of the regenerative latch, such as the offset, noise, and metastability [45]. In addition, the extended voltage headroom allows for a large tail current to charge in a specific time period that is strictly limited by the AD conversion speed, thus effectively reducing the input-referred noise of the comparator.

### C. Charge-Mode Reference Generation

The ADC reference can be generated externally by using an OFF-chip voltage buffer [28], [29], which, however, is demanding with regard to distributing such a reference voltage for many ADCs throughout the whole chip. Instead, the voltage

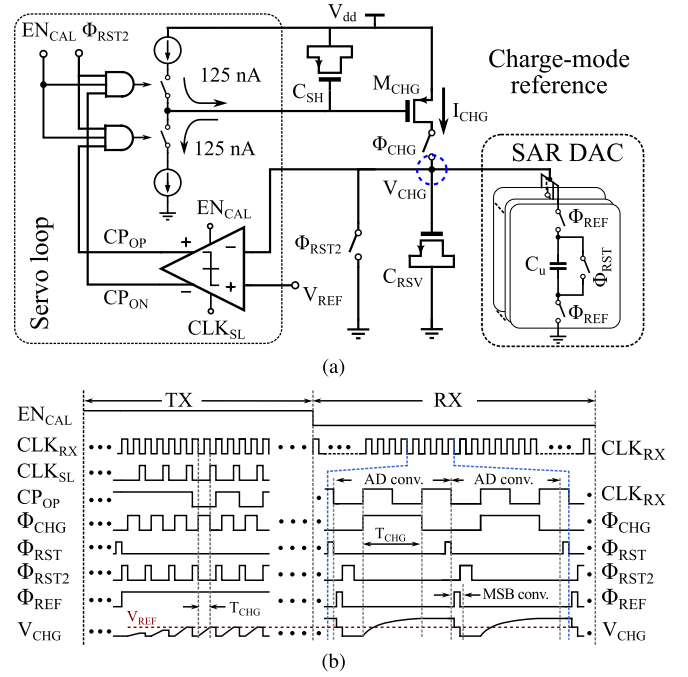


Fig. 9. (a) Circuit diagram of the charge-mode reference generator and (b) associated timing diagram.

reference can be generated locally by a fast but power-hungry voltage buffer [19] to achieve a very short pre-charge time for the CDAC array. The power consumption can be reduced by employing two TI CDAC arrays [14], allowing for precharging one of the arrays to a reference voltage while using the other to perform AD conversion, but at the expense of a  $2\times$  larger CDAC area.

Fig. 9(a) shows a charge-mode reference scheme that solves the power and area problems by employing an area-efficient, precharged MOS capacitor  $C_{RSV}$  as a reservoir to quickly set a reference for the subsequent AD conversion. A servo loop is activated during the TX period to calibrate the charge current  $I_{CHG}$  for the subsequent RX period. As shown in Fig. 9(b), during the charge phase  $\Phi_{CHG}$  of the TX period,  $I_{CHG}$  charges the parallel-connected CDAC and the reservoir NMOS capacitor  $C_{RSV}$  before a latch comparator compares the resulting voltage on these capacitors with a reference voltage  $V_{REF}$ , controlled by a clock signal  $CLK_{SL}$ . In the subsequent phase  $\Phi_{RST2}$ , the servo loop calibrates the current  $I_{CHG}$  by tuning the overdrive voltage of PMOS transistor  $M_{CHG}$  via a charge pump comprised of 125-nA sourcing and sinking current sources and a PMOS capacitor  $C_{SH}$ , in accordance with the decision made by the comparator. Meanwhile, CDAC and  $C_{RSV}$  are reset in readiness for the next charging. This process repeats until the voltage on these capacitors equals  $V_{REF}$ . At the end of the TX period, the total amount of charge  $Q_{REF}$  stored on these capacitors can be expressed as

$$\begin{aligned} Q_{REF} &= (C_{DAC} + C_{RSV}) \cdot V_{REF} \\ &= I_{CHG} \cdot T_{CHG} \end{aligned} \quad (1)$$

where  $C_{DAC}$  and  $T_{CHG}$  are the total capacitance of the CDAC array, and the charging time is accurately controlled by  $\Phi_{CHG}$ .

Throughout the RX period, the overdrive required to generate  $I_{CHG}$  is held on the PMOS capacitor  $C_{SH}$ , so that the



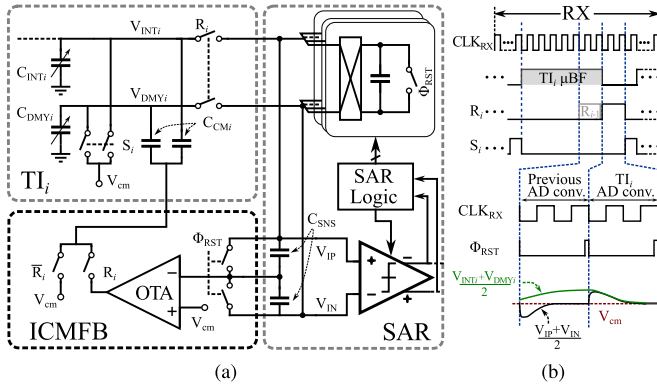


Fig. 10. (a) Circuit diagram of the ICMFB canceling out CM variations of TI channels and (b) related timing details of  $Ti_i$ .

same amount of charge is delivered to  $C_{RSV}$  during  $\Phi_{CHG}$ . During  $\Phi_{REF}$ , at the start of each AD conversion, this charge is redistributed with the CDAC. The charge as expressed in (1) is conserved during the charging and redistribution process, providing a well-defined reference voltage at the end of  $\Phi_{REF}$ .

A charging time  $T_{CHG}$  of 12.5 ns is adopted, which effectively filters out the high-frequency noise of the current source  $M_{CHG}$  owing to the boxcar filtering mechanism similar to that of the  $\mu$ BF, thereby reducing the associated reference noise. In this work, the total capacitance of the CDAC array is approximately 1.9 pF.  $C_{RSV}$  is set to a similar capacitance to avoid voltage clamping during  $\Phi_{CHG}$ , while it still occupies a very small area compared to the CDAC, which is made of metal–oxide–metal (MOM) capacitors in our design, thanks to the much higher capacitance density of MOS capacitors. The fast charge-mode operation allows the charge sharing between the CDAC and  $C_{RSV}$  to complete within the MSB conversion when the CDAC array is disengaged from the ADC's input, hence without affecting the total required AD conversion time. The active blocks in the servo loop are all deactivated ( $EN_{CAL} = 0$ ) during RX. These features lead to a very low-power, low-noise, and area-efficient reference scheme.

#### D. Input Common-Mode Feedback

As discussed in Section II-C, the single-ended output of the  $\mu$ BF on capacitors  $C_{INT1-5}$  is converted into a differential input to the ADC by means of dummy capacitors  $C_{DMY1-5}$ , this would result in large CM variations. Fig. 10(a) depicts the circuit diagram of the ICMFB, which cancels out the CM variations through a capacitive feedback loop formed by  $C_{CMi}$ ,  $C_{SNS}$  and an operational transimpedance amplifier (OTA).

Fig. 10(b) shows the timing diagram of  $Ti_i$ . The integration capacitor  $C_{INTi}$ , the dummy capacitor  $C_{DMYi}$  and the coupling capacitors  $C_{CMi}$  are first reset during phase  $S_i$ , followed by the  $\mu$ BF boxcar integration on  $C_{INTi}$ . During the boxcar integration, the CM voltage on  $C_{INTi}$  and  $C_{DMYi}$  gradually deviates from  $V_{cm}$ . During the subsequent read phase  $R_i$ , the SAR ADC starts to digitize  $Ti_i$ , and the CM voltage detected through capacitors  $C_{SNS}$  is fed to the negative input of the OTA, which adjusts the CM voltage on  $C_{INTi}$  and  $C_{DMYi}$  through the coupling capacitors  $C_{CMi}$  until the CM voltage equals  $V_{cm}$ . Once the AD conversion is completed,

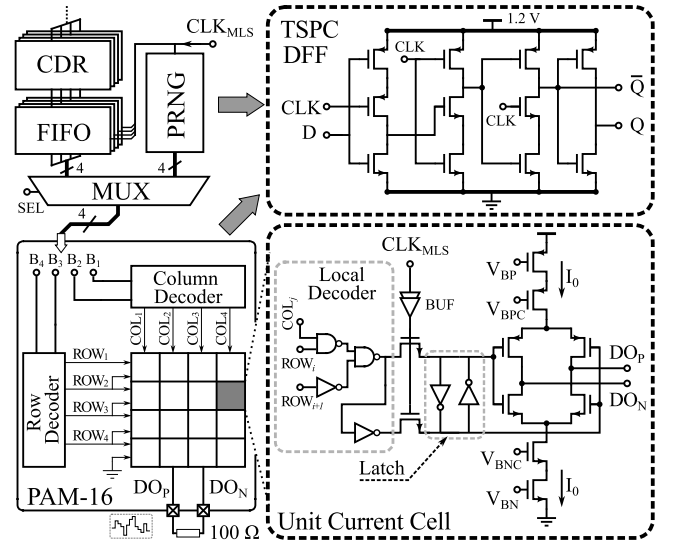


Fig. 11. Circuit diagram of the 4-bit current-steering DAC with insets showing a TSPC DFF used in the decoders and in the PRNG, and the details of a unit current cell.

capacitors  $C_{SNS}$  are reset in  $\Phi_{RST}$  as preparation for the CM cancellation of the next TI channel. Notably, the use of the 1-bit redundancy in the AD conversion significantly relaxes the settling requirement of the ICMFB loop to about one ADC conversion period, i.e., 25 ns. As a result, the power consumption of the OTA is also reduced.

#### E. PAM-16 DAC

As depicted in Fig. 11, a 4-bit current-steering DAC is used as the output driver of the D-TX, which RXs the 4-bit data from the FIFO (as discussed in II-D), or, for the test purposes, from a 4-bit pseudorandom number generator (PRNG). The DAC produces a differential output current ( $DO_P/DO_N$ ) to drive an OFF-chip 100-Ω load resistor, providing a 16-level voltage signal at the output. The PRNG, based on [46], generates the needed  $2^{10}-1$  random number sequence for a BER measurement, as will be discussed in Section IV-B.

The DAC consists of a matrix of  $4 \times 4$  unit current cells, and row/column decoders that convert the received binary code ( $B_{1-4}$ ) into two thermometer codes ( $ROW_{1-4}$  and  $COL_{1-4}$ ). The current cells comprise a complementary output stage and a local decoder which changes the output polarity in a thermometer fashion, according to the corresponding codes from the row/column decoders [47]. The logic cells of the decoders and PRNG are specially optimized for low-power operation and small areas. For example, all D flip-flops (DFFs) are built based on true single-phase-clock (TSPC) dynamic latches [48] which can steadily operate at a 1.2-V supply with much less power and area compared to a regular primary/secondary DFF.

The DA conversion is synchronized with a 480-MHz clock ( $CLK_{MLS}$ ), and the input latch of the current cells improves timing accuracy by speeding up the toggling of the differential switch [49] which diverts the currents of the cascaded current sources to the load resistor. Each current source provides a current  $I_0$  about 200-μA, resulting in a maximum 600-mV peak-to-peak amplitude with 40 mV per LSB step, at a 1.2-V power supply.

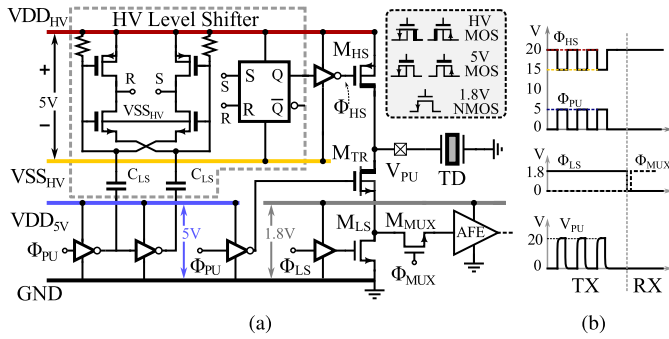


Fig. 12. (a) Circuit diagram of an HV pulser and (b) associated control clock signals and an output waveform of three-cycle pulses.

#### F. HV Pulser

An element-level HV pulser consisting of high-side/low-side MOS transistors  $M_{HS}$  and  $M_{LS}$ , a T/R switch  $M_{TR}$ , and the associated HV level shifter is shown in Fig. 12(a), where  $M_{HS}$  and  $M_{TR}$  are laterally-diffused metal-oxide-semiconductor (LDMOS) with a 20-V breakdown voltage between drain and source and a 5-V breakdown voltage between gate and source. The HV level shifter is powered by an external power supply  $V_{DD_{HV}}$  and an internal source follower located at the periphery, providing a  $-5$  V supply  $V_{SS_{HV}}$  relative to  $V_{DD_{HV}}$  [50]. The TX pulse signal  $\Phi_{PU}$  couples to two 5-V inverters with the cross-coupling to the sources of their NMOS transistors via two level-shifting capacitors  $C_{LS}$ , followed by a set-reset (SR) latch that holds the ON/OFF state for the high-side PMOS  $M_{HS}$  and introduces hysteresis to reject disturbances, thus making the pulser less sensitive to transients on  $V_{DD_{HV}}$ , e.g., the large switching transients caused by other pulsers toggling simultaneously during the TX beamforming.

Since the low-side  $M_{LS}$  is always on during TX, the HV MOS transistors  $M_{HS}$  and  $M_{TR}$  behave like an inverter controlled by the pulse signal  $\Phi_{PU}$ , hence generating the 20-V unipolar pulse to drive the transducer, as depicted in Fig. 12(b). In the following RX period, the T/R switch  $M_{TR}$  is kept on while  $M_{LS}$  is off, allowing the current signal of the transducer to be fed into the virtual ground of the AFE via the multiplexer  $M_{MUX}$  for subsequent signal processing.

### IV. EXPERIMENTAL RESULTS

#### A. ASIC Prototype

Fig. 13(a) shows a transceiver ASIC prototype fabricated in a 180-nm BCD process, in the center of which a  $16 \times 16$  pad array surrounded by two outer rings of dummy pads is located for bonding with a PZT transducer array, using a similar technique as described in [5]. Fig. 13(b) reveals the floor plan of the RX/TX circuitry that interfaces with one of the subgroups, occupying an area of  $500 \times 1000 \mu\text{m}^2$  with the area breakdown shown in Fig. 14(a). A tiling of eight such subgroup circuitries makes up the pitch-matched region for a  $16 \times 16$  transducer array, while two D-TXs each serving four subgroups, are situated at the periphery of the ASIC.

Per element, the RX circuitry occupies  $0.048 \text{ mm}^2$ , of which the  $\mu\text{BF}$  and ADC occupy  $0.0045$  and  $0.0054 \text{ mm}^2$ , respectively, revealing a compact solution for channel-count

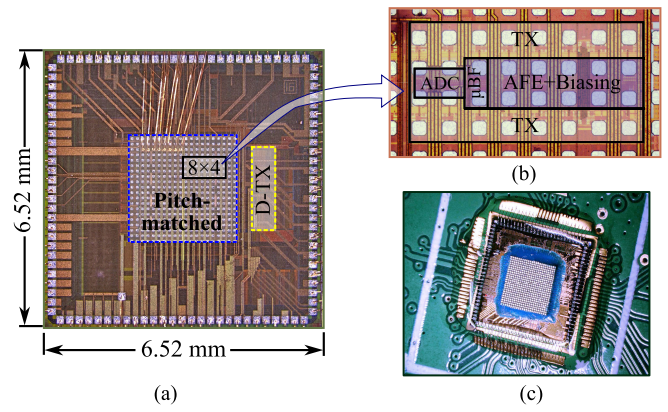


Fig. 13. (a) Micrograph of the transceiver ASIC showing the pitch-matched and the peripheral region, with inset and (b) showing the pitch-matched TX/RX circuitry for eight sub-arrays of  $2 \times 2$ . (c) Prototype of the transceiver ASIC with PZT array built on top.

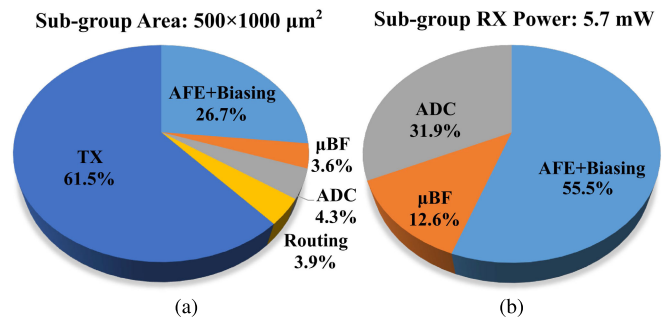


Fig. 14. (a) Area breakdown and (b) power breakdown per subgroup, i.e., per eight sub-arrays of  $2 \times 2$  elements.

reduction. It should be noted that the 8:1 multiplexing has not been taken into account for an objective comparison with state-of-the-art works that do not apply multiplexing, resulting in a division of 4 in the calculations of per-element area and power.

At the maximum AFE gain, the RX circuitry of a subgroup consumes 6.64 mW power, while the power is reduced to an average of 5.7 mW when the AFE is dynamically biased to perform TGC in a 36-dB gain range [26]. The power breakdown of the subgroup RX circuitry is shown in Fig. 14(b), in which the  $\mu\text{BF}$  and ADC consumes 0.72 and 1.82 mW, respectively, both operating at 1.8-V supplies. Compared to the RX circuitry, the power consumption of the TX circuitry is negligible as it operates in a very small duty cycle. As will be elaborated later, each D-TX consumes 6.4 mW at a 1.2-V power supply, resulting in an overall power consumption of 2.06 mW/element at maximum AFE gain, and 1.83 mW/element when performing the TGC.

A prototype of the transceiver ASIC with a PZT array built on top is shown in Fig. 13(c), connecting to each other via the aforementioned transducer bonding pads. The chip was wire bonded to a daughter board via the peripheral pads for both electrical and acoustic measurements. The daughter board was mounted on a mother board containing an FPGA, which controls the TX/RX of the ASIC during the measurements and also synchronizes the data TX and RX between the ASIC and an oscilloscope. Rather than a dedicated D-RX, as a proof of concept, an oscilloscope equipped with an active differential probe was used to acquire the PAM-16 output of

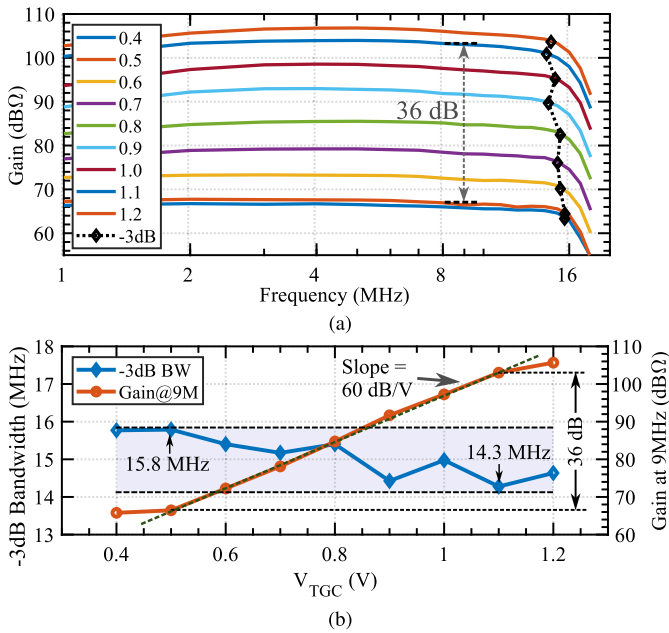


Fig. 15. (a) Measured RX gain transfer function. (b) Extracted  $-3$ -dB bandwidth and gain at 9 MHz as a function of the TGC control voltage  $V_{TGC}$ .

the D-TX. The D-TX output was connected to the probe via 1-mm bond wires to the daughter board and 32-mm FR4 PCB trace, terminated by a  $100\text{-}\Omega$  resistor. The acquired data was uploaded to a PC for the following data processing, such as data decoding and image reconstruction.

### B. Electrical Characterization

The gain transfer function of a subgroup RX channel was measured by applying voltage signals to four ON-chip capacitors of 1-pF, that emulate four transducer elements. The 16-level data of the D-TX captured by the oscilloscope was then uploaded to a PC for decoding and subsequent data processing. To quantify the transfer of the AFE, the readout of the ADC was converted to equivalent AFE output voltages using the 0.5-V reference voltage set by the internal charge-mode reference generator. Thus, the transfer function for different TGC control voltages ( $V_{TGC}$ ) was extracted as depicted in Fig. 15(a), together with a  $-3$ -dB curve showing the bandwidth variation for different TGC gains. The  $-3$ -dB bandwidth as a function of  $V_{TGC}$  is plotted separately in Fig. 15(b), showing a minimum bandwidth of 14.3 MHz at 1.1-V  $V_{TGC}$ , and a maximum bandwidth of 15.8 MHz at 0.5-V  $V_{TGC}$ . Since the bandwidth of the subgroup RX is about 120% around 9 MHz, which is much wider than the bandwidth of the transducer used in our application, the attenuation of the ultrasound signals is minimal. Fig. 15(b) also reveals that the RX gain at 9 MHz is a linear-in-dB function of  $V_{TGC}$  from 0.5 to 1.1 V, leading to a positive slope of 60 dB/V within the total 36-dB gain range. To ensure accurate TGC, the TGC control voltage is restricted between 0.5 and 1.1 V in our design (e.g., the maximum AFE gain is achieved at  $V_{TGC} = 1.1$  V).

Fig. 16(a) shows the normalized output spectrum obtained by measuring the output of a subgroup RX channel at the maximum AFE gain. The measurement was taken by feeding

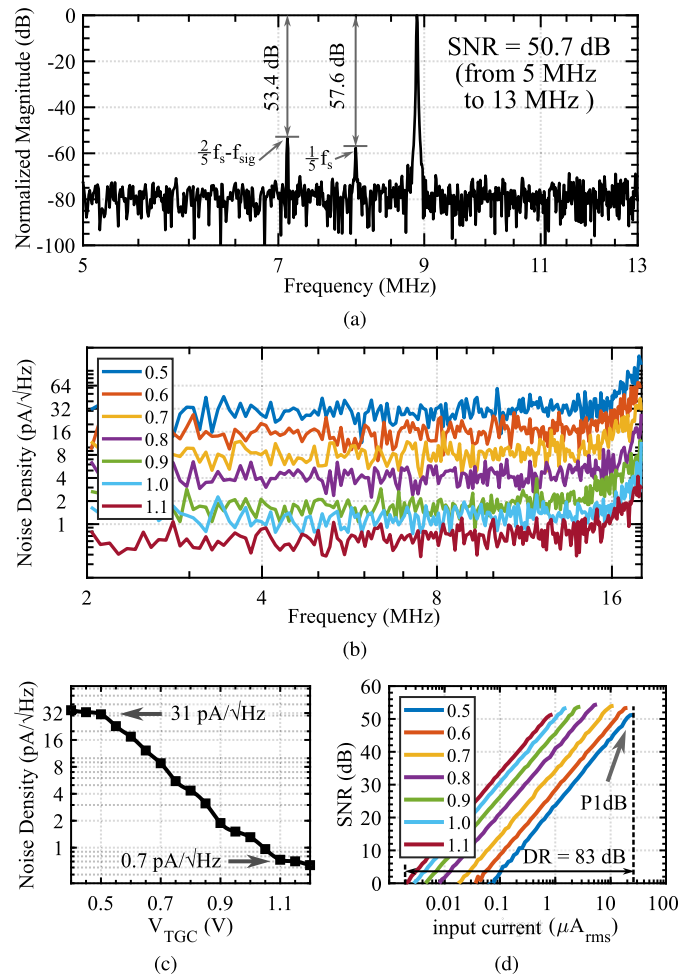


Fig. 16. (a) Measured output spectrum of an RX sub-array at the maximum TGC gain. (b) Measured input-referred noise spectra with 8-MHz tones removed. (c) Input-referred in-band noise as a function of  $V_{TGC}$ . (d) Measured SNR as a function of the input current for different TGC control voltages.

the four AFEs with 8.9-MHz sinusoidal currents, each with a peak value of 1 pA, via the same dummy capacitors mentioned earlier. A peak SNR of 50.7 dB was attained over a bandwidth of 5–13 MHz, representing an 89% bandwidth centered at 9 MHz. Two tones, located at  $(2/5) \cdot f_s - f_{sig}$  and  $(1/5) \cdot f_s$ , are observable, where  $f_s$  is the sampling frequency of the  $\mu$ BF ADC, and  $f_{sig}$  is the frequency of the input signals. The presence of a tone at  $(1/5) \cdot f_s$  can be attributed to mismatch in the five integration capacitors of the  $\mu$ BF, whereas the tone at  $(2/5) \cdot f_s - f_{sig}$  is caused by intermodulation between the input signal and the disturbance induced by this capacitor mismatch. Because of the low power of these tones, they have a negligible impact on image quality.

To calculate the input-referred noise, the noise density at the ADC output was first measured while grounding the four 1-pF capacitors connected to the inputs of the AFEs. The resulting output noise density was then divided by the measured gain transfer function to obtain the input-referred noise spectra shown in Fig. 16(b). It should be noted that the 8-MHz tone, resulting from the mentioned mismatch, has been removed to provide a clearer view of all the curves. Fig. 16(c) shows the input-referred in-band noise as a function of  $V_{TGC}$ , which was derived by averaging over the frequency range of



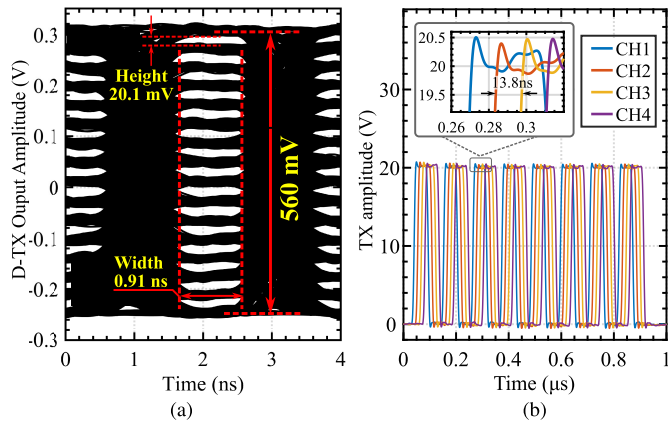


Fig. 17. (a) Eye diagram of D-TX at 1.92 Gb/s. (b) Measured outputs of four TX pulsers with uniform delays of 13.8 ns, and inset showing a delay of 13.8 ns and a maximum amplitude of 20 V.

TABLE I  
D-TX PERFORMANCE COMPARISON WITH PRIOR ART IN  
COMPARABLE TECHNOLOGIES

	This work	JSSC'09 [51]	JSSC'04 [31]	TCSI'13 [52]
Process	180 nm	180 nm	180 nm	180 nm
Modulation	PAM-16	PAM-2	PAM-4	
Data Rate	1.92 Gb/s	5 Gb/s	7 Gb/s	10 GB/s
D-TX Power	6.36 mW	57 mW	66 mW	120 mW
D-TX Energy Efficiency	3.3 pJ/bit	11.4 pJ/bit	9.4 pJ/bit	12 pJ/bit
Area	0.061 mm <sup>2</sup>	0.017 mm <sup>2</sup>	0.16 mm <sup>2</sup>	
Supply	1.2 V	1.8 V	1.7 V	2.0 V
BER	< 10 <sup>-10</sup>	< 10 <sup>-12</sup>	—	

\* Estimated from the layout.

5–13 MHz. The subgroup RX achieves a noise density of 0.7 and 31 pA/ $\sqrt{\text{Hz}}$  at the maximum and minimum TGC control voltage. The SNR as a function of input current for different TGC control voltages is shown in Fig. 16(d), revealing a dynamic range (DR) of 83 dB, defined as the ratio of the maximum input signal level at the 1-dB compression point (P1dB) to the minimum detectable input signal level, at which the SNR drops to zero.

To characterize the PAM-16 D-TX, the output signal of the D-TX was recorded using the oscilloscope for data analysis on a PC. As depicted in Fig. 17(a), the eye diagram, measured at a data rate of 1.92 Gb/s, distinctly shows 16 voltage levels and 15 eyes with a height of  $>20.1$  mV, and a width of  $>0.91$  ns, where the eye height is extracted at a sampling point at which the largest height can be found in the worst case of the 15 eyes. The measured peak-to-peak amplitude is about 560 mV. A BER of  $<10^{-10}$  was measured by selecting the PRNG (see Fig. 11) as the data source of the D-TX. The PRNG operates at 480 MHz and generates  $2^{10}$ -1 pseudorandom 4-bit word.

Table I summarizes the performance of the PAM-16 D-TX and gives a comparison with the prior art, all fabricated in similar 180-nm processes. The PAM-16 D-TX consumes 6.4 mW at 1.92 Gb/s data rate, and occupies 0.061 mm<sup>2</sup>, resulting in an energy efficiency of 3.3 pJ/bit, which is  $>2.8\times$  better than the other designs. As discussed in Section II-D, this

efficiency advantage partly relates to the relatively low data rate of our design, which still provides sufficient channel-count reduction while consuming lower overall power than a solution based on datalinks with higher data rate.

To evaluate the TX pulsers and TX beamforming, eight adjacent transducer bonding pads were wire-bonded to the daughter board. OFF-chip 1-pF capacitors were connected as loads to emulate the transducer capacitance during the measurement. Fig. 17(b) shows the outputs of four neighboring TX pulsers, which were programmed at a uniform delay of 13.8 ns, confirming that the TX beamforming accurately produces these delays. In addition, the pulsers successfully produce eight-cycle unipolar pulses with an amplitude of 20 V.

### C. RX $\mu\text{BF}$ Characterization

The RX beamforming filters incoming acoustic waves in terms of their arrival angles to selectively RX signals in a particular direction while minimizing interference from other directions. Fig. 18(a) shows an example of the beamforming, in which the RX  $\mu\text{BF}$  is steered to an angle of  $0^\circ$  by applying DAS on the data received by four AFEs, leading to a maximum sensitivity for signals arriving at an angle of  $0^\circ$  while suppressing those from other angles.

The RX  $\mu\text{BF}$  was evaluated both by electrical and acoustic measurements. To emulate the arrival of acoustic waves at different angles in electrical measurement, four time-shifted sinusoidal inputs were applied to the AFEs via the ON-chip dummy capacitors, and the outputs for different  $\mu\text{BF}$  steering angles were recorded and compared with the theoretical directivity. During the electrical measurement, the  $\mu\text{BF}$  was steered to four angles ( $0^\circ$ ,  $9^\circ$ ,  $18^\circ$ , and  $28^\circ$ ), corresponding to a minimum delay step of 12.5 ns, and a time shift step of 6.25 ns was applied to four 10-MHz sinusoidal inputs. The response of the  $\mu\text{BF}$ , as illustrated in Fig. 18(b), is consistent with the theoretical directivity curves.

The acoustic experimental setup for  $\mu\text{BF}$  directivity testing is shown in Fig. 18(c). A water tank was placed on top of the prototype chip with an unfocused single-element probe dipped into the water. To ensure accurate measurements, the probe, driven by a 10-MHz sinusoidal wave at its resonance frequency, is positioned at a sufficient distance to guarantee the chip is within its far-field, thus allowing for the arrival of an approximate plane wave at the transducer surface. A 3-D printed rotating handler (not shown) was employed to precisely manipulate the incidence angle of the incoming ultrasound wave, by positioning the probe on a circular trajectory centered at the location of the transducer array.

The transient output responses were recorded by an oscilloscope at incidence angles of  $0^\circ$ ,  $-9^\circ$ , and  $-18^\circ$ , for different  $\mu\text{BF}$  steering angles. As a demonstration, the response corresponding to an incidence angle of  $-9^\circ$  is illustrated in Fig. 18(e), with an inset confirming that the strongest response occurs at the expected  $\mu\text{BF}$  steering angle of  $-9^\circ$  and weaker responses at other angles. The normalized output amplitudes were extracted from the transient waves and then plotted as a function of the  $\mu\text{BF}$  steering angle as shown in Fig. 18(d), alongside the ideal response at the corresponding incidence angles. Again, a good agreement is evident between the

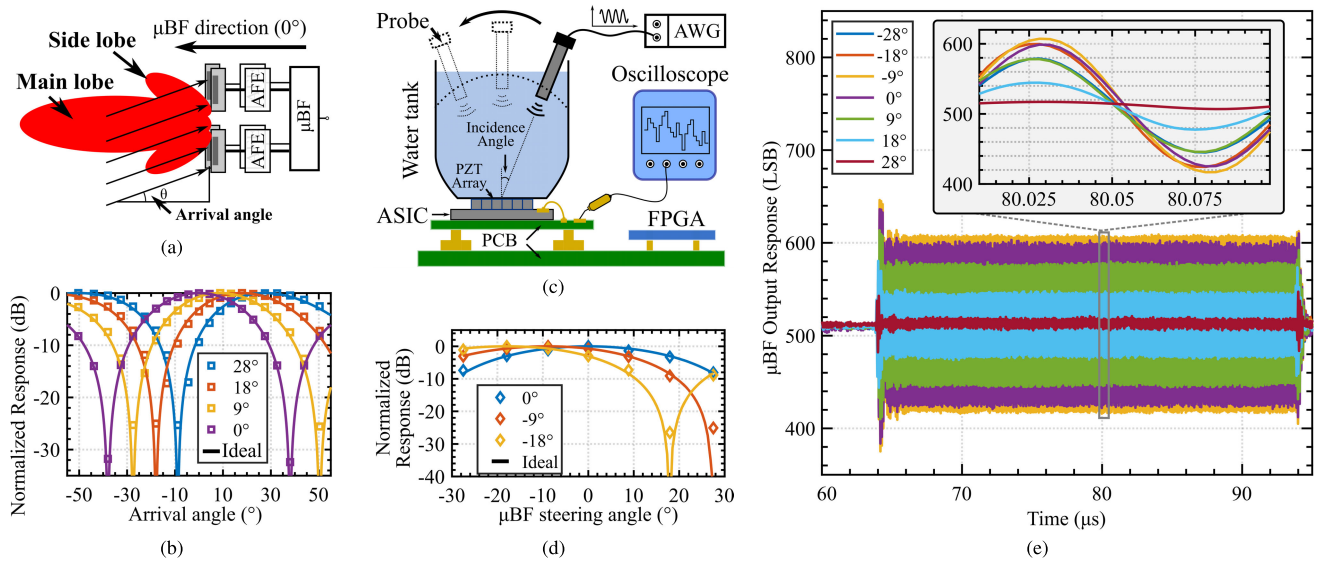


Fig. 18. (a) RX  $\mu$ BF steered at an angle of  $0^\circ$ , showing different sensitivity for ultrasound signals at different arrival angles. (b) Measured  $\mu$ BF directivity presented as normalized response as a function of emulated arrival angles. (c) Acoustic measurement setup for evaluating  $\mu$ BF directivity. (d) Extracted  $\mu$ BF directivity as a function of  $\mu$ BF steering angles, at incidence angles of  $0^\circ$ ,  $-9^\circ$ , and  $-18^\circ$ , combined with the ideal directivity curves for comparison. (e) Recorded output responses of the  $\mu$ BF relative to  $\mu$ BF steering angles of  $-28^\circ$ – $28^\circ$ , at a probe incidence angle of  $-9^\circ$ .

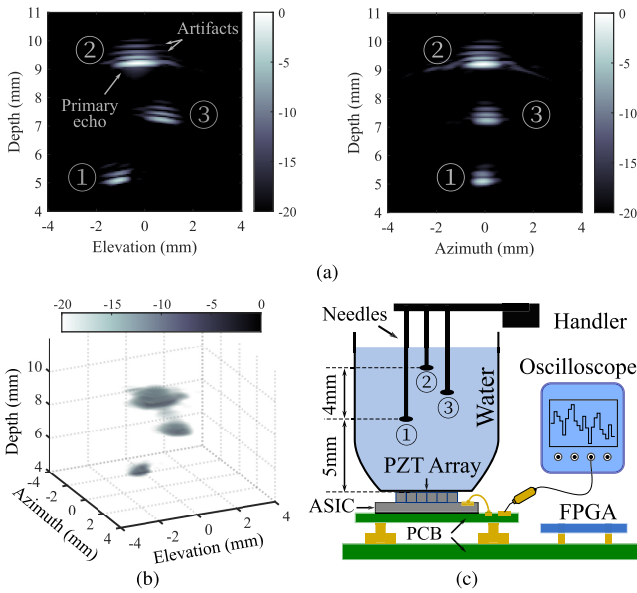


Fig. 19. (a) B-mode images in elevation and azimuth planes. (b) Rendered 3-D image. (c) B-mode imaging experiment setup.

measured data and the theoretical prediction, thus demonstrating the accuracy of the passive BI-based  $\mu$ BF.

#### D. Ultrasound B-Mode Imaging

Fig. 19(c) depicts the measurement setup used for reconstructing B-mode images, which is similar to the setup used for acoustic measurement of the  $\mu$ BF, whereas the probe was replaced by a three-needle phantom, positioned from 5 to 7 mm above the prototype chip. To produce a B-mode image, a plane wave was first generated by the chip via the internal TX circuitry to illuminate the phantom, the received echo signals were processed by the RX circuitry and then encoded by the PAM-16 D-TX. Subsequently, the 16-level outputs were recorded using the oscilloscope and uploaded to a PC before the data was decoded in software. Finally, post-beamforming

processing was applied to reconstruct the B-mode images as shown in Fig. 19(a), both in elevation and azimuth direction. Fig. 19(b) illustrates a 3-D image rendered from the same recording. Despite the relatively low spatial resolution caused by the small aperture of the prototype, all the images distinctly display the three-needle phantom at the correct position, with a clear contrast against the background.

The B-mode images reveal artifacts appearing after the primary echoes, which deteriorate the axial resolution. They are identified as reverberation artifacts, caused by the presence of the ASIC beneath the transducer array and the absence of a proper backing layer in the transducer manufacturing process [53]. As such, these artifacts are not related to the ASIC design and can be resolved by an improved transducer process.

The images are reconstructed from data acquired in 200 T/R cycles, corresponding to  $8\times$  multiplexing and RX  $\mu$ BF steering at 25 different angles, with a pulse-repetition frequency of 20 kHz, allowing for a theoretical volume rate of 100 volumes/s. The bottleneck of the current system is the data-transfer speed between the oscilloscope and the PC, which could be overcome by implementing the envisioned DPU. The DPU would comprise the needed high-speed PAM-16 D-RX, along with the following image reconstruction processing, thus reducing the data throughput and minimizing the data-transfer time.

Table II compares this work with state-of-the-art ASIC designs for different ultrasound systems. Among all the pitch-matched ASIC designs, this work achieves the smallest array pitch, the highest center frequency, and the largest RX channel bandwidth. Meanwhile, the PAM-16 data link provides a very fast data rate and high energy efficiency in comparison with other designs. Notably, the  $\mu$ BF and the ADC occupy a small per-element area, given that the ADC is shared within a relatively small sub-array of  $2\times 2$ . Despite the complexity of the AFE design, which includes a more



TABLE II  
COMPARISON WITH STATE-OF-THE-ART ULTRASOUND ASIC DESIGNS

	This work	JSSC'18 [14]	JSSC'22 [15]	JSSC'19 [54]	JSSC'17 [22]
Process	<b>180nm BCD</b>	180nm	180nm BCD	180nm SOI	28nm CMOS
Center Frequency	<b>9 MHz</b>	5 MHz	6 MHz	<5 MHz	5 MHz
Sub-array Size	<b>2 × 2</b>	3 × 3	3 × 2	4 × 6	4 × 4
Pitch-matched	<b>Y</b>	Y	Y	Y	Y
Transducer Pitch	<b>125 <math>\mu\text{m}</math></b>	150 $\mu\text{m}$	160 $\mu\text{m}$	300 $\mu\text{m}$	250 $\mu\text{m}$
Digitization	<b>Y</b>	Y	Y	N	Y
Sampling Rate	<b>40 MS/s</b>	30 MS/s	24 MS/s	40 MS/s	20 MS/s
Datalink Type	<b>PAM-16</b>	LVDS	LVDS	–	–
Data Rate	<b>1.92 GHz</b>	1.5 GHz	1.2 GHz	–	–
Datalink Power	<b>6.4 mW</b>	15.4 mW	7 mW	–	–
Datalink Efficiency	<b>3.3 pJ/bit</b>	10.3 pJ/bit	5.8 pJ/bit	–	–
Channel Reduction	<b>128-fold</b>	36-fold	12-fold	24-fold	16-fold
RX Bandwidth	<b>14.3 MHz</b>	11.9 MHz	8.1 MHz	5.9 MHz	–
AFE Type	<b>LNA with TGC</b>	LNA + PGA	LNA + PGA	LNA + PGA	LNA + PGA
$\mu\text{BF}$ Resolution	<b>12.5 ns</b>	33 ns	20.8 ns	25 ns	8.33 ns
$\mu\text{BF}$ +ADC Area/El.	<sup>†</sup> <b>0.01 mm<sup>2</sup></b>	<sup>*</sup> 0.011 mm <sup>2</sup>	<sup>*</sup> 0.006 mm <sup>2</sup>	–	<sup>‡</sup> 0.041 mm <sup>2</sup>
RX Area/El.	<sup>†</sup> <b>0.048 mm<sup>2</sup></b>	<sup>*</sup> 0.026 mm <sup>2</sup>	<sup>*</sup> 0.017 mm <sup>2</sup>	0.09 mm <sup>2</sup>	<sup>‡</sup> 0.049 mm <sup>2</sup>
RX Power/El.	<sup>†</sup> <b>1.83 mW</b>	<sup>§</sup> 0.91 mW	<sup>§</sup> 1.23 mW	0.43 mW	<sup>‡</sup> 33 mW
Input DR	<b>83 dB</b>	85 dB	91 dB	85 dB	–
Peak SNR	<b>54 dB</b>	52 dB	52 dB	–	60 dB
TX Voltage	<b>20 V</b>	–	65 V	138 V	–

<sup>†</sup> Not taking input multiplexing into account, sub-array numbers divided by 4, not by 32.

<sup>\*</sup> Including sub-group ADC. <sup>§</sup> Including datalink. <sup>‡</sup> Including element-level ADC.

sophisticated TGC function, the RX circuitry still achieves a low per-element power consumption for a high-center frequency transducer.

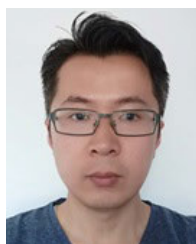
## V. CONCLUSION

This article has presented a transceiver ASIC that combines element-level pulsers and subgroup-level receivers in a pitch-matched fashion. The receiver incorporates an AFE with a continuous TGC function, a passive BI-based  $\mu\text{BF}$ , and a charge-sharing SAR ADC in a pitch-matched region to process incoming ultrasound signals, followed by a data link located in the periphery, that enables low-power, high-speed chip-to-chip communication. The proposed architecture allows for a power-efficient implementation of digitization and off-loading in a mature 180-nm BCD process that supports the required HV TX and implements further data processing in a companion chip made with an advanced process, thus optimizing the overall power consumption for a wearable ultrasound device. Meanwhile, a charge-mode reference effectively reduces the area consumption without compromising the speed of the ADC, hence allowing for a per-subgroup, low-power referencing scheme. The prototype ASIC offers a 128-fold overall channel-count reduction and consumes 1.83 mW/element RX power for a high center frequency, wide-bandwidth transducer array, thus laying the foundation for developing a medical ultrasound device with large aperture, high resolution, and good image quality.

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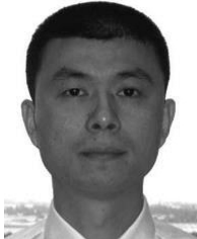
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