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# Improvements to the Co-simulation Interface for Geographically Distributed Real-time Simulation

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**Abstract**—As future power systems become increasingly complex and interconnected to other energy carriers, a single research infrastructure can rarely provide the required test-beds to study a complete energy system, especially if different types of real power hardware are expected to be in-the-loop. Therefore, virtual interconnection of laboratories for large-scale systems plays an important role for geographically distributed real-time simulation. This paper presents the improvements made in simulation fidelity as well as usability for establishing future simulator and laboratory connections. A general procedure is proposed and analyzed for geographically distributed real-time simulation, which allows users easily to adapt this procedure to specific test cases. A systematic and comprehensive analysis of a dynamic phasor based co-simulation interface algorithm and its improvements are provided to demonstrate the advantages as well as limitations of this approach.

**Index Terms**—Co-simulation, Dynamic phasors, Geographically distributed real-time simulation, Laboratory coupling, Real-time digital simulator.

## I. INTRODUCTION

The complexity of the present and future power system requires tools that are suited for simulations on a large scale. This is in order to study the interactions with newer energy sources and interoperability of new control methods. Advancement in power electronics, driven by the energy transition calls for high-fidelity simulation tools and a shift from static load flow simulations to dynamic ones. The stability of future power system operation with inverter dominated dynamics requires a matching assessment infrastructure.

With the advent of more powerful computational tools – Electromagnetic Transient (EMT) or Dynamic Phasors (DP),

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large-scale simulation becomes feasible and enables HIL testing through real-time simulation technologies. However, the required level of detail for such simulations cannot be concentrated in a single site for both technical and organizational reasons. Scaling digital real-time simulation in the power system domain to larger systems is a challenging task; not only limited by technical but also by financial and human factors.

GD-RTS presents an approach which solves these issues, by distributing both the simulation as well as human work load across a set of participants and Research Infrastructures (RIs). Small time steps, often in the range of micro to milliseconds, impose strict real-time computational burdens on the underlying computer and operating system. It is an advanced concept which enhances testing capabilities; Real-time simulation resources, Power Hardware in Loop (PHiL) setups and hybrid co-simulation frameworks may be interconnected to form a comprehensive research infrastructure that allows the sharing of resources and integration of facilities with different hardware setups located far from each other. Thus, virtual interconnection of laboratories will allow for expansion of capabilities of individual laboratories for studies of large-scale, system level and interdisciplinary scenarios.

This paper identified existing shortcomings and presents improvements made in the area of Geographically Distributed Real-Time Simulation (GD-RTS). An analysis of the improved Dynamic Phasor Interface Algorithm (DP-IA) is provided using a simple power system test case as an example. The analysis is based on power system transients, as well as characteristics of the communication setup between the real-time simulation laboratories at RWTH Aachen and TU Delft. An important contribution of this work is the development and release of a reusable library component and its demonstration in a demo model for the RTDS' RSCAD software. These

tests have been conducted as part of the H2020 ERIGrid Transnational Access (TA) research exchange [1].

## II. RELATED WORK

Virtual interconnection of laboratories applied for GD-RTS has been implemented in [2]–[6]. These publications address the requirements for the interconnection of large-scale simulation resources using real-time simulation at multiple labs for joint power system and HiL simulations. Additionally, its framework allows the participants to be flexibility and confidentiality due to indirect data sharing. A co-simulation of multi-area power systems was investigated in [7], which dealt with the requirement of large-scale simulation resources using real-time simulation at multiple institutions and the confidence for their grid models. In [8], a GD-RTS of HVDC systems were implemented using Ideal Transformer Model (ITM) Interface Algorithm (IA). This work showed that simulation fidelity is robust with large time delay. However, co-simulation IA should be improved to guarantee simulation fidelity of all quantities. Previous work [5], [9] has already demonstrated the use of Dynamic Phasors (DP) as a feasible approach to couple real-time simulators. The ACOSAR project developed the Distributed Co-simulation Protocol (DCP) [10]. DCP is aligned with the existing Functional Mockup Interface (FMI) specification and enables distributed co-simulation. Mainly driven by the automotive sector, DCP could be used in the energy sector in the future.

## III. ARCHITECTURE

This section describes the system architecture used for GD-RTS as illustrated in Fig. 1.

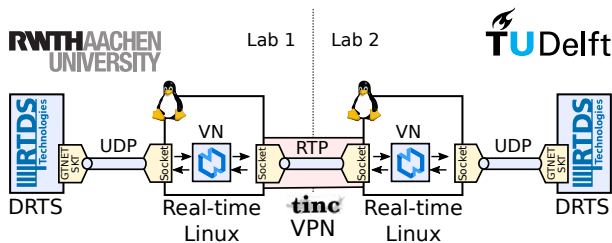


Fig. 1. Architecture

### A. Communication Network

Interface signals from the electrical domain are exchanged over the public internet between both Real-time Digital Simulators (RTDS). For best results, both laboratories are connected via their university networks to the national research and education networks (NRENs). Namely, Germany’s *Deutsches Forschungs Netzwerk (DFN)* and the Netherlands’ *SURFnet* are not-for-profit organizations which are itself interconnected the European GÉANT network. In contrast to special purpose computing networks such as the LHC Computing Grid (LGC) by CERN [11], the networks used in this paper are part of the public internet and thus, shared with other users, which may result in unpredictable spikes in communication latency or packet loss. In this paper, we demonstrate how the DP-IA

described in section V can mitigate the consequences of these disturbances.

1) *Virtual Private Network: Tinc*: For GD-RTS direct peer-to-peer (P2P) connectivity between the labs is crucial to maintain low latency and jitter. As in most cases, computing equipment in both laboratories is protected against external threats via a firewall which filters incoming network traffic and hinder the establishment of P2P connections. For this work a virtual private network based on the *Tinc-VPN* software has been used [12]. Tinc-VPN establishes a fully-meshed network of nodes to facilitate low latency peer-to-peer communication. Tinc accomplishes this with techniques known as *TCP/UDP hole punching* and employs an outstanding public node which facilitates connection establishment but not data exchange.

### B. Co-simulation Gateway: VILLASnode

Within each laboratory a Linux-based gateway server is deployed to establish VPN connections and handle data exchange between the local simulators and remote laboratories. For the data exchange *VILLASnode*, a component of the *VILLASframework*, is used [13]. *VILLASnode* is a C/C++ application tailored for the real-time exchange of simulation data in different formats and protocols. In this setup, it handles the collection of statistics on the communication link as well as the protocol conversion between the User Datagram Protocol (UDP), utilized for connection to RTDS’ GTNET card, and the Real-time Transfer Protocol (RTP) which has been used between the laboratories.

### C. Real-time Protocol: RTP / RTCP

The frequency with which simulators exchange their interface signals is one of the factors which affects accuracy of simulation results. The maximum rate is limited by the available bandwidth of the communication links. As the link is shared with other users, the available bandwidth varies with time, which may cause congestion. Congestion has to be avoided as it leads to packet loss and a degradation of simulation fidelity.

In the past, a static rate has been determined by empirical tests preceding the actual simulation runs. This approach is cumbersome as it needs to be repeated for every new communication link and possibly at different times of a day. To improve this situation, this paper implements a congestion avoidance scheme based on a real-time protocol which dynamically adjusts the sending rate.

For data exchange between the gateway nodes, the RTP and its sibling the Real-time Control Protocol (RTCP) are used [14]. Both protocols are used in conjunction: RTP handles data transfer whereas RTCP is used to exchange Quality of Service (QoS) reports which measure packet loss, delay and jitter. These reports are the main advantage of RTP over plain UDP packets, as they can be used by the sender to adjust its behaviour.

RTP and RTCP are widely used protocols in real-time multimedia streaming applications such as Voice-over-IP or Video-on-Demand streaming. In these applications, RTCP receiver

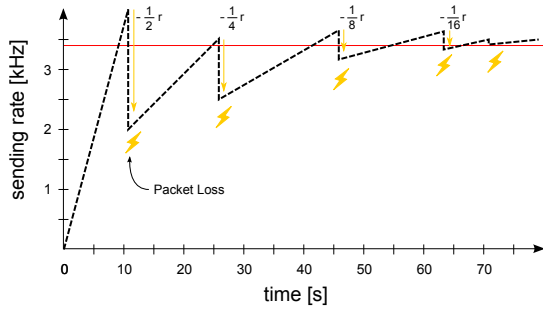


Fig. 2. AIMD sending rate adaption with decreasing impact over time.

reports are used to adjust the bit rate of multimedia codecs based on the current network conditions in order to avoid stuttering and lags the stream.

In the context of this work, the receiver reports are used to change the sampling (sending) rate of signals which are exchanged between the simulators as shown in Fig. 2. The congestion avoidance algorithm is implemented in the VILLASnode gateway. It is inspired by TCP Additive Increase, Multiplicative Decrease (AIMD) scheme which in the case of no congestion, increases the sending rate linearly and in case of congestion, reduces the sending rate by a multiplicative factor [15]. In order to avoid large changes in the sending rate which could affect the simulation results, the impact of the AIMD adaptation is reduced by half with every occurring congestion event.

RTP encapsulates the simulation signals in a raw IEEE 754 single-precision floating format and adds header fields for time-stamps as well as a sequence number. In this test, RTP uses UDP as the underlying transport protocol.

#### D. Real-Time Digital Simulators: RTDS

Both labs operate digital real-time simulators from RTDS Technologies. During this experiment, two Novacor chassis at RWTH and one PB5 rack at TU Delft have been used to simulate the system described in Section IV. For synchronization, both RTDS installations are equipped with GTSYNC extensions cards which use the Global Position System (GPS) to synchronize the time-steps as well as the simulation start to a common time reference. However, as seen later, synchronization is not an essential requirement for the fidelity of the simulation, but instrumental for the collection and alignment of results.

### IV. TEST CASES

#### A. Communication Tests

In addition to the transient power system simulations, the communication network has been analysed as it builds the foundations for the coupling of distributed simulators. The analysis focuses on the communication network topology and its characteristics such as packet loss, maximum packet rates, latency and jitter.

1) *Ping & Trace-route tests:* The most basic of communication tests, involves using the standard ping and trace-route tools to gain a basic idea about the network connecting the two sites. For the ping test, 10000 packets in total, in intervals of 10 ms are transmitted from one VILLASnode gateway machine to the other and average RTT, recorded. This is found to be in the range of 12.7 to 13 ms. Furthermore, using the trace-route tool, the routing path between RWTH Aachen and TU Delft is found to be as depicted in Fig. 3. The total number of hops is 17. Using the `mttr` (Matt's Traceroute) command, each individual hop is pinged with 1000 packets in intervals of 100 ms and the resulting statistics of the network can be analysed. These are presented in Section VII.



Fig. 3. Reconstructed routing path between Aachen and Delft.

2) *Between VILLASnode Gateways:* In this test, data is exchanged between the VILLASnode gateway machines in a *loop-back configuration*. As test data, a sine-wave with certain frequency is generated in the gateway at either location and every sample encapsulated in a UDP and is tagged with a time-stamp before being transmitted to the remote site. At the other side, received packets, are send back to the source without any changes to the encapsulated data. By comparing the time-stamps of the sent and returned packets, the communication latency between the sites is estimated by dividing the round-trip time by half. This test is carried out for the following combinations:

- With a fixed sending rate and variable data size
- With a variable sending rate and fixed data size

3) *Between Simulators using GTSYNC:* As the final step of communication testing, data exchange between both the real-time simulators is carried out. To achieve this, models which test the communication latency (RTT), jitter and maximum packet rate were developed. Using the GTSYNC cards at both labs, simulations can be started concurrently.

Simulation data is transferred from one RTDS to its local VILLASnode machine through the GTNET card and GTNET-SKT (socket) protocol as UDP traffic. The SKT protocol represents floating point numbers as single precision (32-bit) using IEEE754 format. The packet size is an integral multiple of 4 bytes, depending on number of data points sent. The IP

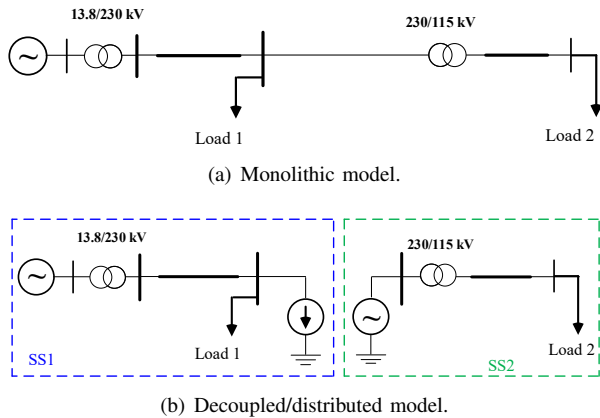


Fig. 4. Simple power system diagram.

addresses, ports and variables to be exchanged are specified in the RSCAD model files.

### B. Simulation Test Cases

The system used in this paper is a basic power system consisting of a voltage source connected to loads through a transmission line as shown in Fig. 4. This system represents the simplest version of a transmission-distribution network, in which the interface decouples the transmission from the distribution side. For validation, three different variants of the model have been compared:

1) *Monolithic model*: Monolithic model is modelled in real-time simulator using a single RTDS rack where the entire system is simulated in a single subsystem without any system partitioning as shown in Fig. 4(a). It serves as a reference with no time delay for the comparison of the decoupled and distributed model.

2) *Decoupled model*: The decoupled model shown in Fig. 4(b) is derived from the monolithic model where the system is separated into two subsystems at the 230 kV bus based on ITM approach for co-simulation as described in Section V. The simulation is executed across two RTDS racks but still contained and started by a single RSCAD/draft file. Signal exchange between the subsystems is handled by cross-rack signal import/exports.

3) *Distributed model*: The distributed model is derived from the decoupled model by moving one subsystem entirely to a separate RTDS simulation. The co-simulation now spans two independent RSCAD/draft files which are started separately. The signal exchange of the subsystems is handled by the VILLASnode gateway described in Section III-B.

## V. DYNAMIC PHASORS INTERFACE ALGORITHM

The co-simulation IA is based on ITM approach where, as illustrated in Fig. 4(b), controlled sources are utilized to impose voltage and current measured at the interface. RTDS systems perform transient simulation in time domain where current and voltage quantities are represented with its wave forms. Direct sampling and transfer of instantaneous values of the wave forms across a shared wide-area communication

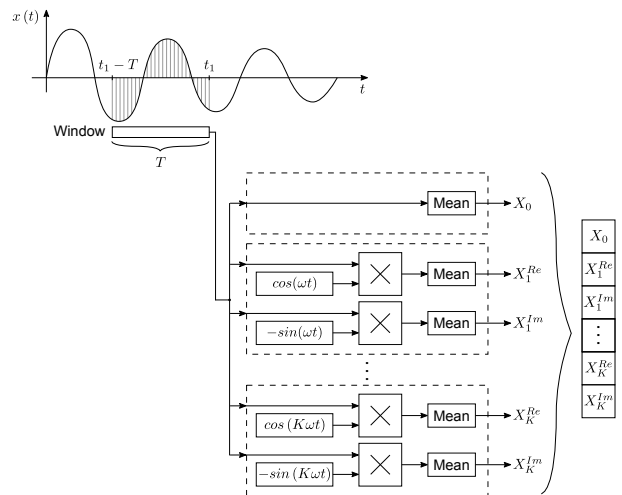


Fig. 5. Calculation of DP coefficients

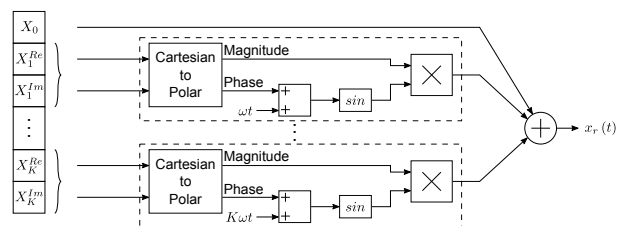


Fig. 6. Reconstruction of the time-domain waveform based on DP coefficients

network that is characterized by relatively large and time-varying delay would significantly deteriorate the wave forms and simulation fidelity. As a solution, two main approaches are proposed in literature. Representation of interface quantities in the form of Root Mean Square (RMS), frequency and phase angle is proposed in [16]. In this work, transformation of the interface quantities in the form of time-varying Fourier coefficients [5], known as DP, is utilized.

Fig. 5 illustrates transformation of wave forms to a DP-based representation before sampling and sending interface quantities to the remote DRTS system. At the receiving side, the DP quantities are transformed back to the time-domain waveform to provide reference for the controlled sources as illustrated in the Fig. 6. DP-IA allows for compensation of time-varying delay based on phase shift within reconstruction of time-domain waveform. This compensation approach has been proposed for PHIL in [17] and adapted for GD-RTS in [5]. Details of the implementation and comprehensive analysis of the DP-IA are given in the following Section VI.

## VI. IMPLEMENTATION DETAILS

This section describes key implementation aspects required to be considered for application of DP-IA in GD-RTS to achieve high degree of simulation fidelity. In particular, the focus is on implementation of DP-IA in RSCAD.



### A. DFT Window Length

In a DRTS, the power system is simulated in the time domain through discrete and equidistant time steps. As a consequence, the Fourier transform used to calculate DP must be a Discrete Fourier Transform (DFT).

The DFT is implemented as a series over the moving window of the product of signal  $x[n]$  with reference phasors:

$$X_k[m] = \frac{1}{N} \sum_{n=m-N}^m x[n] \cdot e^{-j2\pi f_0 kn} \quad (1)$$

As a result, the Fourier coefficients describe the harmonic components of the interface quantity. The length of the DFT window is chosen so that it covers one period of the fundamental frequency of the signal. For example, in a 60 Hz system which is simulated with a 50  $\mu$ s time step  $T_s$ , the window has a length of  $N \approx (1/f_0)/T_s = 333, \bar{3}$ . As this window length is not an integer number, the resulting Fourier coefficients do not represent the harmonic components of the 60 Hz system accurately. If this error is not properly taken into account, RMS values of interface quantities will not be identical and the power exchanged at the co-simulation interface will be imbalanced even in steady state. As indicated in the Table I, a possible solution to this issue is the adjustment of the simulation time step such that, the DFT window length is closer to an integer number:  $T_s = (1/f_0)/334 \approx 49,9 \mu$ s.

TABLE I  
IMPACT OF THE DFT WINDOW LENGTH ON INTERFACE QUANTITIES.

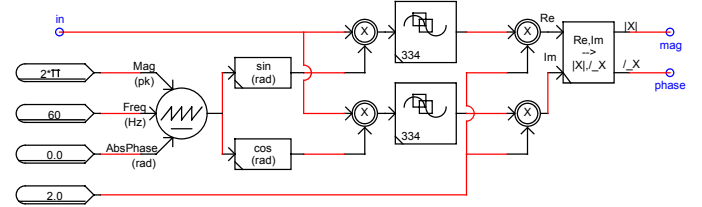
| DFT window       |     |             | Interface quantity |       |                 |       |
|------------------|-----|-------------|--------------------|-------|-----------------|-------|
| $T_s$ [ $\mu$ s] | $N$ | length [ms] | $V_{A,rms}$ [kV]   |       | $I_{A,rms}$ [A] |       |
|                  |     |             | SS1                | SS2   | SS1             | SS2   |
| 50               | 333 | 16.65       | 136.7              | 136.0 | 51.64           | 51.9  |
| 50               | 334 | 16.7        | 136.6              | 137.9 | 52.56           | 52.05 |
| 49.9             | 334 | 16.6666     | 136.6              | 136.6 | 52.56           | 52.56 |

This problem typically does not occur for simulations with a 50 Hz system frequency. Namely, for the most commonly used 50  $\mu$ s time step, the DFT window exactly spans 400 steps.

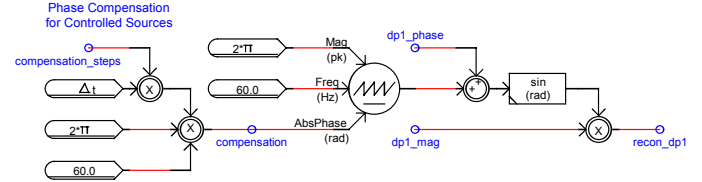
### B. DFT Calculation

A critical step for performance of the DP-IA is the calculation of complex-valued phasors from the real-value instantaneous voltage and current signals and their subsequent reconstruction to original form. Phasors are calculated by a DFT from which only certain harmonic components are selected. The calculation is continuously updated over a moving window, thereby producing a stream of *dynamic* phasor updates. Different approaches to calculate the phasors and the reconstruction have been considered:

1) *RSCAD: DFT control component*: The included DFT block in RSCAD supports a maximum sampling of 64 points per cycle. For the case of a 60 Hz system, this results in a maximum update rate of the phasors to  $60 \text{ Hz} \times 64 = 3840 \text{ Hz}$ . The execution time required for this block is  $0.18 \mu\text{s} \times 64 + 0.5 \mu\text{s} = 12,02 \mu\text{s}$  which is relatively high. In a standard co-simulation, 9 DFT blocks are required (3 phases  $\times$  3 harmonic



(a) DFT with moving average blocks.



(b) Signal reconstruction.

Fig. 7. RSCAD implementation of DP-IA for a single frequency component.

components). Given the execution time, this would result in a utilization of several control component processors which is unacceptable.

2) *RSCAD: Moving average window*: Fig. 7(a) shows a custom implementation of the phasor calculation which utilizes moving average blocks in RSCAD. This implementation produces an updated phasor in every simulation time step and has an execution time which is nearly half of that of the DFT block.

3) *VILLASnode*: Both RSCAD based DFT implementations suffer from the disadvantage that, changing the number of harmonic components is not feasible without extensive manual changes to the models and their large utilization of RTDS resources. Therefore, it is desirable to move the calculation of the DP-IA to the VILLASnode gateway and therefore reduce the amount of changes required to the initial model. The only modification necessary to adapt a model for co-simulation is then the addition of communication blocks (GTNET) and controlled sources. The simulation gateway has been updated to perform calculation and reconstruction of phasors to instantaneous values.

### C. Update Rate

In steady state, all three approaches provide correct results as the exchanged phasors remain constant.

During transients the update rate of the phasors becomes critical. There are currently three bottlenecks which limit the update rate of the phasors: First, the RSCAD DFT block is limited to 3840 Hz. Secondly, RTDS specifies the maximum sending rate of its GTNET card with 5 kHz. At last, the VILLASnode gateway might restrict the sending rate in order to avoid congestion on the communication link as described in Section III-C.

The first bottleneck has been solved by using the custom DFT implementation based on moving average windows. The second bottleneck is the current limiting factor and therefore the simulations in this paper have been conducted with a update rate of 5 kHz. In the future this bottleneck can be solved

by replacing the GTNET with a more powerful GTFPGA card. By utilizing the PCIexpress and Aurora interfaces of an FPGA board, a signal exchange between the gateway and the simulator in every time step becomes possible.

In any case, a sending rate less than the simulation time step ( $f_c < \frac{1}{T_s}$ ) during transients will result in discontinuities in the reconstructed signal. In order to be avoid system instabilities, the signal should be filtered with a low pass filter. Initial tests with a 3rd degree Butterworth filter with  $f_c = \frac{1}{2T_s}$  have shown promising results but entail a group delay of the reconstructed signal. This delay will add to the existing communication delay.

#### D. Signal reconstruction of time-domain waveform

The reconstruction of the instantaneous voltage/current wave forms is performed by multiplying the dynamic phasor coefficients  $X_k[n]$  with the same rotating reference phasor as in section VI-B. The resulting signal is then used to directly control a voltage/current source at the coupling point. Due to internals of RTDS scheduling, the resulting reconstructed waveform is always delayed by 1-3 time steps,  $n_c$  as the control components cannot control the sources in the same time step as they are executed. This demands for a constant phase compensation by  $\varphi_c = 2\pi f_0 n_c T_s$  which can be added to the absolute phase of the reference phasor as shown in Fig. 7(b):

$$x[n] = \sum_{k=0}^K X_k[n] \cdot e^{j(2\pi f_0 k n + \varphi_c)} \quad (2)$$

Table II shows the steady state power flow with respect to different compensation steps for the voltage and current sources in SS1 and SS2 respectively. Note that the apparent power and RMS of the voltage at the interface are matching in all cases. If internal delays of controlled sources are properly compensated, the power flow is identical for both sides of the interface ( $P_{SS1} = P_{SS2}, Q_{SS1} = Q_{SS2}$ ) which is given for  $n_{SS1} = 3, n_{SS2} = 2$ .

TABLE II  
IMPACT OF PHASE COMPENSATION OF SOURCE SIGNALS ON  
STEADY-STATE POWER BALANCE AT THE CO-SIMULATION INTERFACE

| $n_{SS1}$<br>[ $T_s$ ] | $n_{SS2}$<br>[ $T_s$ ] | $P_{SS1}$<br>[MW] | $Q_{SS1}$<br>[MVar] | $P_{SS2}$<br>[MW] | $Q_{SS2}$<br>[MVar] | $S$<br>[MVA] | $V_{rms}$<br>[kV] |
|------------------------|------------------------|-------------------|---------------------|-------------------|---------------------|--------------|-------------------|
| 0                      | 0                      | 19.16             | 9.846               | 20.0              | 8.003               | 21.54        | 227.7             |
| 1                      | 1                      | 19.52             | 9.118               | 20.0              | 8.003               | 21.54        | 227.9             |
| 2                      | 1                      | 19.69             | 8.749               | 20.0              | 8.003               | 21.54        | 227.9             |
| 3                      | 2                      | 20.0              | 8.003               | 20.0              | 8.003               | 21.54        | 228.1             |

## VII. RESULTS

### A. Communication Tests

The communication results between the VILLAS node gateways and the real-time simulators are presented here. Fig. 8 shows the statistical analysis of all the hops on the routing path. It can be observed that, there is a positive correlation between the actual physical distance between hops and the

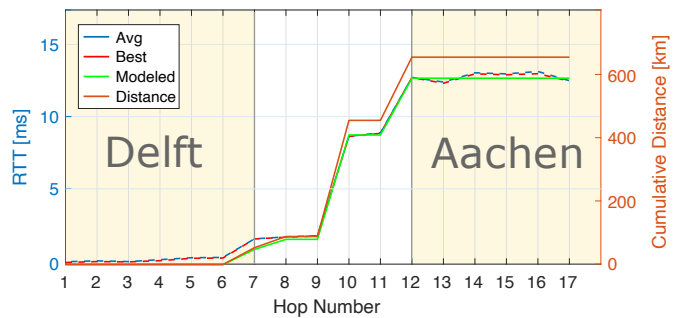


Fig. 8. Latency of Routing Path

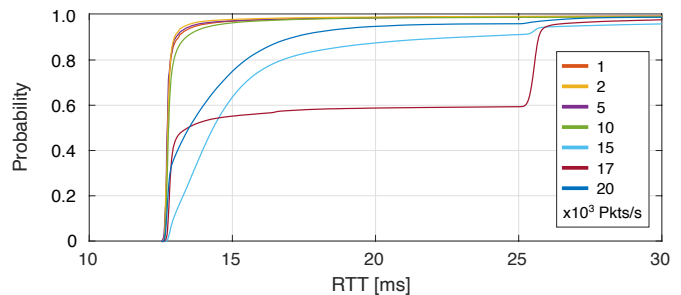


Fig. 9. Cumulative distribution of RTT for varying sending rates

modeled latency, calculated using  $T_m = a * D * (c/n)$  with  $a \approx 2$  as an air-line distance correction,  $D$  as the distance,  $c$  as speed of light and  $n \approx 1,5$  as the refractive index of a fiber optic.

To gain greater insight into the round trip times, a detailed statistical analysis is performed. Fig. 9 shows the cumulative distribution of Round Trip Times (RTT) for the transfer of a fixed number of data points—24 with variable sending rates between the gateway machines. 24 data points are chosen as they are relevant to the application/use-case. It can be inferred from Fig. 10 that, for sending rates greater than 10000 packets/sec, RTT is higher than average and they can be treated as outliers. Lower sending rates however, are tightly coupled. For instance, with a sending rate of 17000 packets/sec, there is only a 60% chance of the RTT being lesser or equal to 25 ms.

A similar analysis is carried out for RTT with a fixed sending rate of 2000 packets/sec with variable data points. This is seen through Fig. 11. Thus, it can be concluded that, neither higher sending rates nor large data sizes are preferable. This can be attributed to the fact that, the communication network between the two sites is not a dedicated one, but shared. Hence, this introduces a degree of stochasticity or unpredictability.

### B. Co-Simulation

1) *Limits of the co-simulation interface:* Fig. 12 shows the propagation of a  $90^\circ$  phase discontinuity of the ideal voltage source, with 'Original', 'dcpl' and 'dist' are for that of the monolithic, the decoupled and the distributed model, respectively. It shows that during this fault like event, the interface



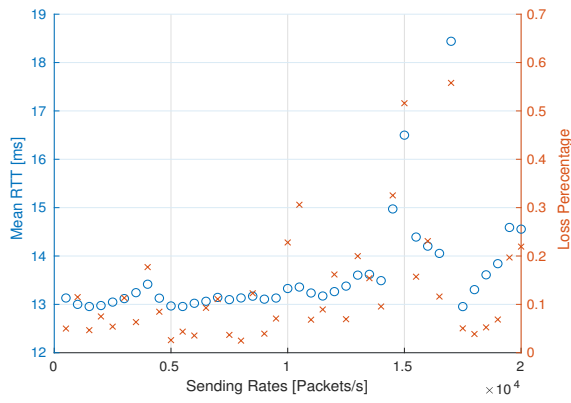


Fig. 10. RTT statistics for variable sending rates with fixed data point

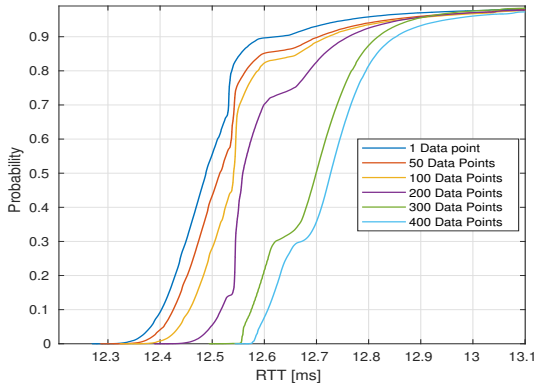


Fig. 11. Cumulative distribution of RTT for varying data sizes

quantities strongly differ from the monolithic reference signal. In the case of this simple and stiff power system which is used in this publication, the system quickly returns to steady state.

2) *Effects of Jitter and Congestion on Interface Fidelity:* Fig. 13 shows variations in the system frequency at the interface point which are correlated with spikes in the communication latency. It can be seen obviously that the simulation fidelity plays a vital role in the co-simulation quality.

### C. Validation of the Co-simulation Interface

Figs. 14 to 16 show instantaneous, RMS and power quantities on both sides of the interface. If compared against the original monolithic model as well as the decoupled version, only a slight delay of 6 ms is observable. It can be concluded that the proposed method enhances significantly the simulation fidelity for the co-simulation interface.

## VIII. CONCLUSION AND FUTURE WORK

This paper identified and addressed several issues in the co-simulation interface which has been used so far for GD-RTS. These issues have been solved and validated, using a distributed real-time simulation of a simple power system.

Significant differences in Quality of Service of the communication link have been observed in comparison to previous

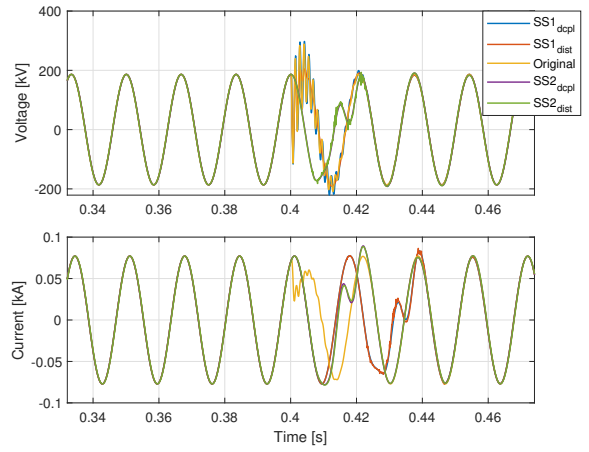


Fig. 12. Limits of DP-IA interface in case of 90 deg phase shift.

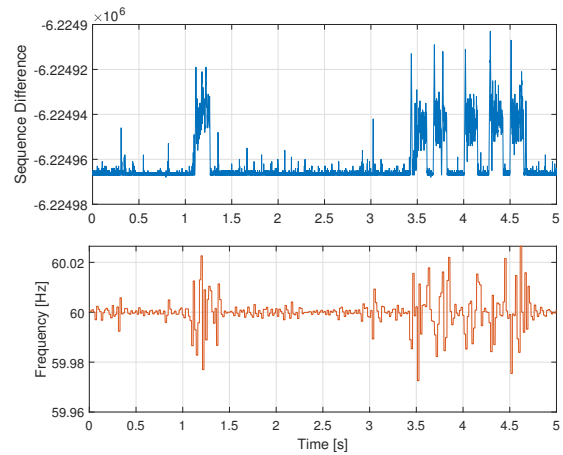


Fig. 13. Frequency variations at the interface caused by spikes in communication latency.

lab couplings. These demand for an automated approach to monitor the network and to adapt to network congestion. The paper introduces the application of RTP/RTCP protocols in the real-time simulation domain.

In the current state, GTNET cards cannot achieve the required sending rate which is necessary to move the IA into the VILLASnode gateway. In the future, GTFPGA cards could be used to work around this issue.

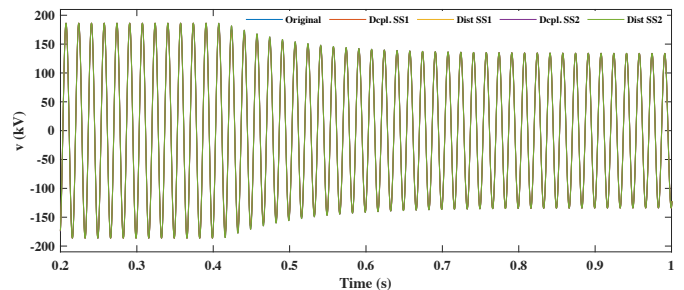


Fig. 14. Instantaneous signals at interface for change of source amplitude.

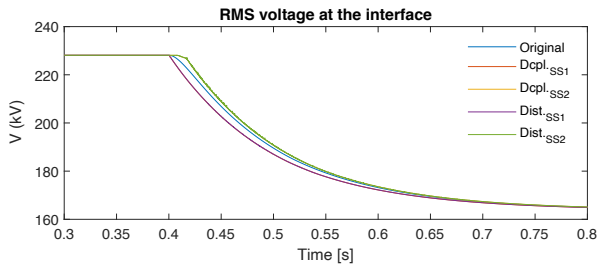


Fig. 15. RMS Voltage at interface for change of source amplitude.

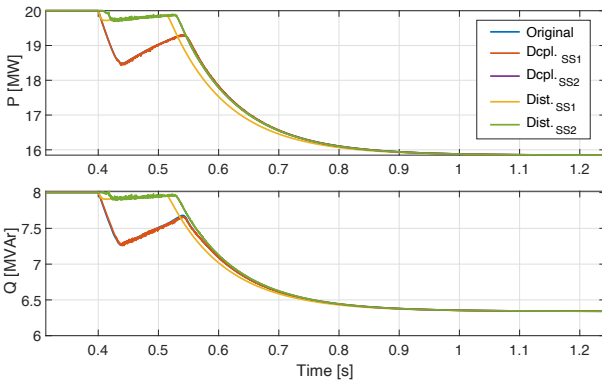


Fig. 16. Active / Reactive power flow at interface for change of source amplitude.

Two sources of error have been also identified: Firstly, DFT window lengths do not always match with the fundamental system period due to the usage of discrete time steps by the simulators. This error has been successfully reduced by adjusting the simulation time step to an integer factor of the period. Secondly, a constant phase offset caused by scheduling dependencies in the control system and network solution within the RTDS system have been identified and solved by applying a constant compensation to the phase of the reconstructed signal.

In a static system in which the system frequency is equal to its nominal frequency, the DP-IA generates no error. This is guaranteed as the exchanged phasors remain constant and even dropouts in the communication would have no consequences. In a system which deviates from its nominal frequency the exchanged phasors slowly rotate with  $f_r = f_0 - f$ . This rate of change is usually much slower than the actual system frequency and therefore is more robust against communication latency and jitter. However, due to down sampling and jitter on the communication link, rotating phasor updates will lead to small phase jumps of the controlled sources. This is another source of error which could be mitigated in the future by extrapolation.

Last but not least, a re-usable library block for RSCAD has been developed and tested [18]. RTP/RTCP support as well as a realization of the IA has been implemented for VILLASnode. Both contributions are released under an open-source licence to enable other researchers to easily adapt new models for GD-RTS and to setup future lab connections.

As follow-on work, a complex distributed power system simulation is planned, composed of a transmission (IEEE 9-bus system) and a distribution system (IEEE 34-node test feeder), to be implemented among three real-time simulation laboratories at RWTH Aachen university, Technical University of Denmark (DTU) and Delft University of Technology (TU Delft).

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