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Yu, Haoyuan; Zhang, Hanwen; Zhang, Qi; Wang, Yanbo; Qin, Zian; Chen, Zhe; Bauer, Pavol

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A Virtual Impedance-Based Active Damping Control Strategy for Triple Active Bridge Converter

Haoyuan Yu, *Graduate Student Member, IEEE*, Hanwen Zhang, *Graduate Student Member, IEEE*, Qi Zhang, *Student Member, IEEE*, Yanbo Wang, *Senior Member, IEEE*, Zian Qin, *Senior Member, IEEE*, Zhe Chen, *Fellow, IEEE*, and Pavol Bauer, *Senior Member, IEEE*

***Abstract*—Multiport dc–dc converters have been intensively concerned and studied in power electronics-based systems. However, the instability issue and its suppression method are rarely discussed. This article investigates the stability of the triple active bridge (TAB) converter with two constant power loads by impedance-based method, where the output impedance of the TAB converter is derived by the extra element theorem. Then, a virtual impedance-based active damping (AD) control is proposed, where the virtual impedance has four different positions at the output capacitor of the dc port. The effect of the proposed AD control on output impedance and system dynamic response is analyzed. Meanwhile, the range of the virtual impedance is specified. Simulation is performed in PLECS and experimental tests are conducted on a scale-down TAB prototype to verify the effectiveness of the proposed AD control.**

***Index Terms*—Active damping (AD), extra element theorem (EET), multiport dc–dc converter, stability analysis, triple active bridge (TAB) converter, virtual impedance.**

I. Introduction

THE multiport dc–dc converter, such as triple active bridge (TAB) converter, has been increasingly concerned in electrical vehicles [1], [2], renewable energy systems [3], [4], [5], and traction power supply systems [6], [7], [8]. The TAB converter features the symmetrical structure and can provide galvanic isolation in accessing aircraft with two engines [9], [10] and railways with two-phase traction power supply arms [11]. In such applications, adopting TAB converters can reduce the number of power electronics devices.

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Haoyuan Yu, Hanwen Zhang, Qi Zhang, Yanbo Wang, and Zhe Chen are with the Department of Energy, Aalborg University, 9220 Aalborg, Denmark (e-mail: hyu@et.aau.dk; hzha@et.aau.dk; qzg@et.aau.dk; ywa@et.aau.dk; zch@et.aau.dk).

Zian Qin and Pavol Bauer are with the Department of Electrical Sustainable Energy, Delft University of Technology, 2625 Delft, The Netherlands (e-mail: z.qin-2@tudelft.nl; p.bauer@tudelft.nl).

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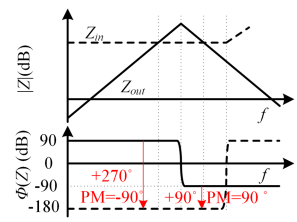

Fig. 1. Impedance feature of source converter and load converter.

Although various control methods have been proposed for different applications to achieve power management, the stability of the TAB converter-based system is another important point to be considered. In [9], the frequency characteristics of the voltage loop and current loop of the TAB converter are presented. In [12], the forward decoupling matrix and delay are considered in the loop gain. Besides the stability analysis for the controller, the stability of the TAB converter interfacing with other devices or systems is investigated. In [13], the stability is investigated through the impedance-based method when one port of the TAB converter connects with a constant power load (CPL) and another port connects with a resistive load or a battery. It shows that oscillation at the CPL port can be addressed by changing the operating status of other ports. In [6], the stability of the TAB converter with two CPLs is analyzed, where a potential oscillation issue is revealed. However, the solution to the oscillation issue is not involved in the existing literature.

Active damping (AD) is an effective solution to the instability problem which is widely used in two-port dc–dc converters. However, it is rarely investigated in the TAB converter due to its complicated model. The most used AD method is introducing virtual impedance. From the perspective of the impedance-based analysis methods [14], [15], [16], as shown in Fig. 1, the introduction of virtual impedance can reshape the impedance characteristics of the source or load converter and make them separated [17], [18], [19], [20]. It can be classified into the following three methods.

1) Elevating the input impedance of the load converter.
2) Reducing the output impedance of the source converter.
3) Making the phase margin (PM) of the intersection region larger than 0°.

For the input side of the load converter, a parallel-type and series-type virtual impedance is introduced in [17], [18], and [19] for a general two-port dc–dc converter. The virtual impedance is designed to modify the magnitude and phase of the input impedance of the load converter in the intersection region. However, the feedback loops of parallel-type and series-type are added to the voltage loop and modulation. It may cause voltage deviation and demands precise controller design. In [21], an input voltage loop is applied to emulate the parallel virtual impedance at the input side of the dual active bridge (DAB) converter. In [22] and [23], the virtual impedance is used to reshape the phase of the input impedance of the DAB converter and buck converter and make the PM larger than 0°.

For the output side of the source converter, the typical application is droop control, where the droop gain can be regarded as a virtual resistor to shape output impedance and regulate the output power [24], [25]. However, secondary control is needed to restore the voltage deviation. In [20], a source-side series virtual impedance control is proposed to reduce the output impedance, where the virtual impedance is derived from the load converter in [17] and [18]. The feedback loop is added to modulation which requires precise controller design, and the impact of different virtual impedances on systems is not involved. In [26], a parallel virtual *RC* damper is proposed for the boost converter, and the virtual *RC* damper is achieved by adding the feedback loop to the duty ratio. Besides the application for dc–dc converter, the AD method is proposed for inverter [27], where different positions of the virtual resistor at *LCL* filter are considered. Except for shaping output impedance by virtual impedance, a lead-lag controller can be added to the control loop to reshape the output impedance directly [28], [29]. However, the design of the lead-lag controller is not specified.

The virtual impedance method can effectively eliminate the oscillation of a two-port dc–dc converter in different applications. But it is rarely adopted to multiport dc–dc converters. In this work, the virtual impedance-based AD control is proposed for the TAB converter to eliminate the oscillation problem. The advantages and contributions of this work are presented as follows.

1) Four different positions of virtual impedance are proposed. The virtual impedance at each location is feedbacked to the inner current loop. Compared to adding to outer voltage and modulation, the proposed AD control would not cause voltage deviation and it is relatively not sensitive to controller parameters.
2) The derivation of the equivalent transfer function of virtual impedance in the controller is based on the output impedance. The output impedance of the TAB converter is derived by the extra element theorem (EET) in our previous work [6], which is more intuitive and concise than traditional methods in [30] and [31].
3) The impact of different values of virtual impedance on systems is investigated. The range of virtual impedance at different positions is specified.

The rest of this article is organized as follows. The system description and the output impedance of the TAB converter are elaborated in Section II. The AD control is proposed in Section III. The simulation verification is given in Section IV. Experimental results are shown in Section V. Finally, Section VI concludes this article.

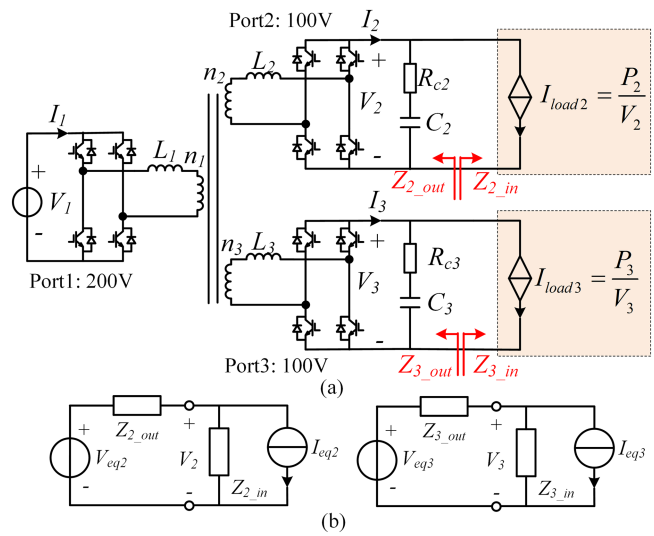

Fig. 2. Circuit diagram of the TAB converter with two CPLs.

II. System Impedance Modeling and Oscillation Phenomenon

A. System Description

Fig. 2(a) shows the circuit structure of the TAB converter with two CPLs. In this work, the impedance-based method is applied to analyze the system stability. Fig. 2(b) shows the equivalent impedance model of the TAB converter with CPLs. The stability of the proposed system can be determined by simultaneously identifying whether the ratio $(1+Z_{2\_\mathrm{out}}/Z_{2\_\mathrm{in}})$ and $(1+Z_{3\_\mathrm{out}}/Z_{3\_\mathrm{in}})$ meet the Nyquist criteria. This stability assessment method can also be implemented in frequency response by calculating the PM of ratio $Z_{2\_\mathrm{out}}/Z_{2\_\mathrm{in}}$ and $Z_{3\_\mathrm{out}}/Z_{3\_\mathrm{in}}$ [6]. Therefore, the output impedance (Z_{2_out} and Z_{3_out}) will be analyzed in the following sections.

B. Small-Signal Modeling of the TAB Converter

The TAB converter can be modeled as a three-port gyrator [3], [6]. Based on the law of superposition, the average power and current of each port over one switching period can be represented as follows:

$$\begin{aligned} P_1 &= \frac{n_1 V_1 V_2}{2 n_2 f_s L_{12}} d_{12}\left(1-|d_{12}|\right) + \frac{n_1 V_1 V_3}{2 n_3 f_s L_{13}} d_{13}\left(1-|d_{13}|\right) \\ P_2 &= \frac{n_1 V_1 V_2}{2 n_2 f_s L_{12}} d_{12}\left(1-|d_{12}|\right) - \frac{n_1^2 V_2 V_3 d_{23}}{2 n_2 n_3 f_s L_{23}}\left(1-|d_{23}|\right) \\ P_3 &= \frac{n_1 V_1 V_3}{2 n_3 f_s L_{13}} d_{13}\left(1-|d_{13}|\right) + \frac{n_1^2 V_2 V_3 d_{23}}{2 n_2 n_3 f_s L_{23}}\left(1-|d_{23}|\right) \end{aligned} \tag{1}$$

$$I_1 = P_1/V_1; I_2 = P_2/V_2; I_3 = P_3/V_3 \tag{2}$$

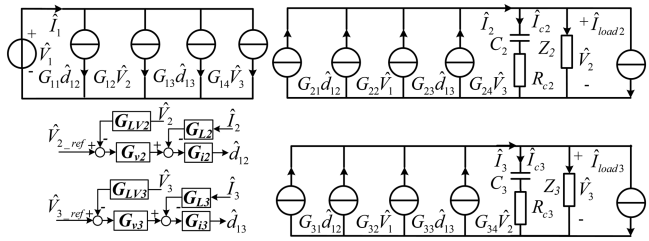

Fig. 3. Small signal model of the TAB converter with load Z_2 and Z_3.

TABLE I
SIMULATION PARAMETERS OF THE TAB CONVERTER

Symbol	Quantity	Value
V_1	Nominal voltage of Port1 (V)	200
$V_{2,3}$	Nominal voltage of Port2 and Port3 (V)	100
$L_{1,2,3}$	Leakage inductor of TAB converter (μH)	50
n_1:n_2:n_3	Windings turn ratio	2:1:1
$C_{2,3}$	Output capacitor (μF)	820
$R_{c2,c3}$	ESR of the output capacitor (Ω)	0.01
f_s	Switching frequency (kHz)	10
ω_c	Cut-off angular speed of current LPF (rad/s)	2π*1000
ω_{cl}	Cut-off angular speed of voltage LPF (rad/s)	2π*100
$G_{v2,3}$	Voltage controller	0.0806+10.63/s
$G_{i2,3}$	Current controller	0.0195+12.25/s
$G_{L2,3}$	Current LPF	$\omega_c^2/(s^2+2*s*0.707*\omega_c+\omega_c^2)$
$G_{LV2,3}$	Voltage LPF	$\omega_{cl}/(s+\omega_{cl})$

where d_{12} and d_{13} are phase shifting ratio, and the range of d_{12} and d_{13} is from -0.5 to 0.5. d_{23} represents the phase shifting ratio between Port2 and Port3, which equals d_{13}-d_{12}. f_s is the switching frequency. n_1, n_2, and n_3 are winding turns. L_{12}, L_{13}, and L_{23} represent the equivalent inductors of three-windings high-frequency transformers in Δ-connection mode.

The small signal model of the TAB converter, as shown in Fig. 3, can be derived as follows by linearization of (1):

$$\begin{bmatrix}\hat{I}_1\\ \hat{I}_2\\ \hat{I}_3\end{bmatrix}=\begin{bmatrix}0 & G_{12} & G_{14}\\ G_{22} & 0 & G_{24}\\ G_{32} & G_{34} & 0\end{bmatrix}\begin{bmatrix}\hat{V}_1\\ \hat{V}_2\\ \hat{V}_3\end{bmatrix}+\begin{bmatrix}G_{11} & G_{13}\\ G_{21} & G_{23}\\ G_{31} & G_{33}\end{bmatrix}\begin{bmatrix}\hat{d}_{12}\\ \hat{d}_{13}\end{bmatrix} \tag{3}$$

where the coefficients G_{11}–G_{34} are given in Table V in the Appendix.

Although the decoupling matrix is widely used for the controller design of the TAB converter, the decoupling matrix cannot guarantee singularity under each operation point [9]. In this work, the dual-loop control without decoupling is designed under the condition that the maximum power of Port2 and Port3 is 500 W. The simulation parameters of the TAB converter are given in Table I.

C. Output Impedance of the TAB Converter

The output impedance of the TAB converter can be derived by EET [6]. The uncoupled and coupled output impedance of Port2 under two-loop control can be represented as follows:

$$Z_{2\_\text{out}}(s)=H_r(s)\left(1+\frac{Z_N^3(s)}{Z_3(s)}\right)\Big/\left(1+\frac{Z_D^3(s)}{Z_3(s)}\right) \tag{4}$$

$$Z_{2\_\text{out}\_c}(s)=Z_{2\_\text{out}}(s)\Big/\left(1+\frac{Z_{2\_\text{out}}(s)}{Z_2(s)}\right) \tag{5}$$

where Z_2(s) and Z_3(s) represent the load impedance at Port2 and Port3. H_r(s) represents the output impedance of Port2 when Z_2 branch and Z_3 branch are opened. It can be represented as

$$H_r(s)=1\Big/\left[\frac{sC_2}{sC_2R_{c2}+1}-\frac{a_3}{1-b_3}\right] \tag{6}$$

$$\begin{aligned}a_3&=G_{24}a_1-G_{21}G_{LV2}G_{v2}G_{i2}-G_{23}G_{LV3}G_{v3}G_{i3}a_1\\&\quad-G_{23}G_{L3}G_{i3}a_2\\ b_3&=G_{24}b_1-G_{21}G_{L2}G_{i2}-G_{23}G_{LV3}G_{v3}G_{i3}b_1\\&\quad-G_{23}G_{L3}G_{i3}b_2\end{aligned} \tag{7}$$

$$a_2=\frac{sC_3}{sC_3R_{c3}+1}a_1;\ b_2=\frac{sC_3}{sC_3R_{c3}+1}b_1 \tag{8}$$

$$\begin{aligned}a_1&=\frac{\frac{G_{34}-G_{31}G_{LV2}G_{v2}G_{i2}}{1+G_{33}G_{L3}G_{i3}}}{\frac{sC_3}{sC_3R_{c3}+1}+\frac{G_{33}G_{LV3}G_{v3}G_{i3}}{1+G_{33}G_{L3}G_{i3}}};\\ b_1&=\frac{\frac{-G_{31}G_{L2}G_{i2}}{1+G_{33}G_{L3}G_{i3}}}{\frac{sC_3}{sC_3R_{c3}+1}+\frac{G_{33}G_{LV3}G_{v3}G_{i3}}{1+G_{33}G_{L3}G_{i3}}}\end{aligned} \tag{9}$$

$Z_N{}^3$ and $Z_D{}^3$ are null driving point impedance and driving point impedance seen looking into Port3, which can be represented as follows:

$$Z_N^3=1\Big/\left(\frac{sC_3}{sC_3R_{c3}+1}-e_2\right) \tag{10}$$

$$e_2=-G_{33}G_{LV3}G_{v3}G_{i3}/\left(1+G_{33}G_{L3}G_{i3}\right) \tag{11}$$

$Z_D{}^3$ can be represented as follows:

$$Z_D^3=1\Big/\left(\frac{sC_3}{sC_3R_{c3}+1}-\frac{e_5}{1-g_5}\right) \tag{12}$$

$$\begin{aligned}e_5&=G_{34}e_3-G_{31}G_{LV2}G_{v2}G_{i2}e_3-G_{31}G_{L2}G_{i2}e_4\\&\quad-G_{33}G_{LV3}G_{v3}G_{i3}\\ g_5&=G_{34}g_3-G_{31}G_{LV2}G_{v2}G_{i2}g_3-G_{31}G_{L2}G_{i2}g_4\\&\quad-G_{33}G_{L3}G_{i3}\end{aligned} \tag{13}$$

$$e_4=\frac{sC_2}{sC_2R_{c2}+1}e_3;\ g_4=\frac{sC_2}{sC_2R_{c2}+1}g_3 \tag{14}$$

$$\begin{aligned}e_3&=\frac{\frac{G_{24}-G_{23}G_{LV3}G_{v3}G_{i3}}{1+G_{21}G_{L2}G_{i2}}}{\frac{sC_2}{sC_2R_{c2}+1}+\frac{G_{21}G_{LV2}G_{v2}G_{i2}}{1+G_{21}G_{L2}G_{i2}}};\\ g_3&=\frac{\frac{-G_{23}G_{L3}G_{i3}}{1+G_{21}G_{L2}G_{i2}}}{\frac{sC_2}{sC_2R_{c2}+1}+\frac{G_{21}G_{LV3}G_{v2}G_{i2}}{1+G_{21}G_{L2}G_{i2}}}.\end{aligned} \tag{15}$$

The uncoupled output impedance (Z_{3_out}) and coupled output impedance of Port3 ($Z_{3\_\text{out}\_c}$) can be obtained in the same way.

Fig. 4 shows the comparison of impedance frequency between analytical results and frequency sweeping results in PLECS when Port2 connects with a 20 Ω resistor and Port3 connects with a 40 Ω resistor. It can be seen that the analysis results align with frequency sweeping results, which validates the effectiveness of the derivation.

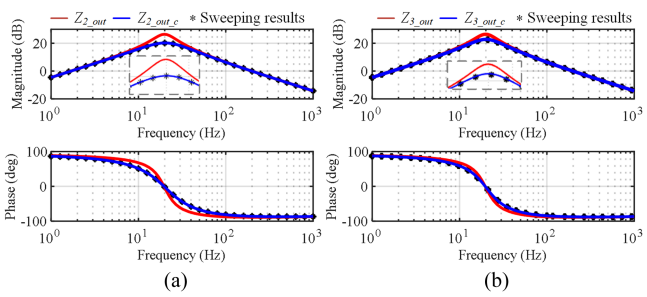

Fig. 4. Frequency characteristic of uncoupled and coupled output impedance of Port2 and Port3 when $Z_2 = 20\ \Omega$ and $Z_3 = 40\ \Omega$. (a) Port2. (b) Port3.

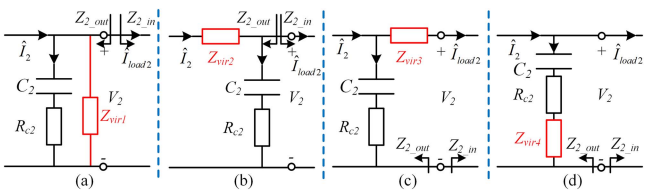

Fig. 5. Concept diagrams of the proposed four virtual impedance-based AD control. (a) Scheme 1. (b) Scheme 2. (c) Scheme 3. (d) Scheme 4.

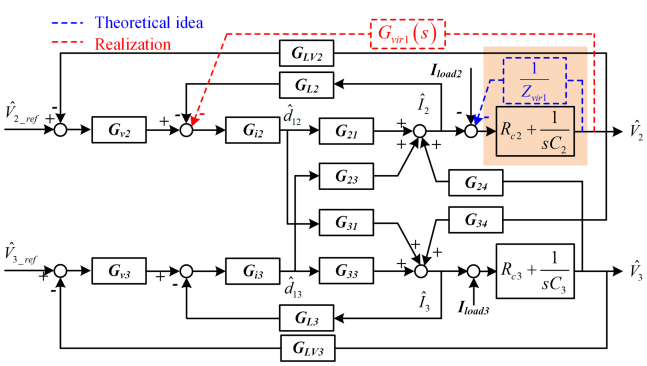

Fig. 6. Scheme one of AD control.

III. Proposed Virtual Impedance-Based AD Methods for the TAB Converter

In this section, a virtual impedance-based AD control is proposed to reshape the uncoupled output impedance of Port2 (Z_{2_out}). There are four different locations for the proposed AD methods, which are shown in Fig. 5. The AD control is derived based on the inherent output impedance H_r(s), where the impact of $Z_N{}^3$ and $Z_D{}^3$ is ignored.

A. Scheme One of AD Control

Fig. 6 shows scheme one of AD control. It can be seen that the virtual impedance Z_{vir1} increases the output current of Port2, which is illustrated by the blue dashed line. The transfer function in the capacitor branch can be modified as $(R_{c2}+1/sC_2)\|Z_{\mathrm{vir1}}(\mathrm{s})$. Thus, the inherent output impedance $H_r{}^1$(s) of scheme one can be represented as

$$H_r^1(s) = 1/\left[\frac{sC_2}{sC_2R_{c2}+1} + \frac{1}{Z_{\mathrm{vir1}}} - \frac{a_3}{1-b_3}\right]. \tag{16}$$

However, the theoretical idea cannot be implemented directly. Thus, in this work, a new transfer function G_{vir1}(s) is proposed to realize the theoretical idea of scheme one, which is illustrated as the red dashed line in Fig. 6.

As shown in Fig. 6, the phase shifting ratios d_{12} and d_{13} can be represented as

$$\begin{aligned}\hat{d}_{12} &= \left(\left(\hat{V}_{2\_\mathrm{ref}} - G_{LV2}\hat{V}_2\right)G_{v2} - G_{\mathrm{vir1}}\hat{V}_2 - G_{L2}\hat{I}_2\right)G_{i2}\\ \hat{d}_{13} &= \left(\left(\hat{V}_{3\_\mathrm{ref}} - G_{LV3}\hat{V}_3\right)G_{v3} - G_{L3}\hat{I}_3\right)G_{i3}.\end{aligned} \tag{17}$$

$H_r{}^1$(s) can be represented as

$$H_r^1(s) = 1/\left[\frac{sC_2}{sC_2R_{c2}+1} - \frac{a_3^1}{1-b_3^1}\right] \tag{18}$$

where the $a_3{}^1$ and $b_3{}^1$ are given as follows:

$$\begin{aligned}a_3^1 &= G_{24}a_1^1 - G_{21}\left(G_{vir1} + G_{LV2}G_{v2}\right)G_{i2}\\ &\quad - G_{23}G_{LV3}G_{v3}G_{i3}a_1^1 - G_{23}G_{L3}G_{i3}a_2^1\\ b_3^1 &= G_{24}b_1^1 - G_{21}G_{L2}G_{i2} - G_{23}G_{LV3}G_{v3}G_{i3}b_1^1\\ &\quad - G_{23}G_{L3}G_{i3}b_2^1\end{aligned} \tag{19}$$

$$a_2^1 = \frac{sC_3}{sC_3R_{c3}+1}a_1^1;\ b_2^1 = \frac{sC_3}{sC_3R_{c3}+1}b_2^1 \tag{20}$$

$$\begin{aligned}a_1^1 &= \frac{\frac{G_{34}-G_{31}(G_{vir1}+G_{LV2}G_{v2})G_{i2}}{1+G_{33}G_{L3}G_{i3}}}{\frac{sC_3}{sC_3R_{c3}+1} + \frac{G_{33}G_{LV3}G_{v3}G_{i3}}{1+G_{33}G_{L3}G_{i3}}};\\ b_1^1 &= \frac{\frac{-G_{31}G_{L2}G_{i2}}{1+G_{33}G_{L3}G_{i3}}}{\frac{sC_3}{sC_3R_{c3}+1} + \frac{G_{33}G_{LV3}G_{v3}G_{i3}}{1+G_{33}G_{L3}G_{i3}}}.\end{aligned} \tag{21}$$

Compared with the coefficients of H_r(s) in (7)–(9) and $H_r{}^1$(s) in (19)–(21), b_1–b_3 are equal to $b_1{}^1$–$b_3{}^1$. In addition, the denominator of $H_r{}^1$(s) in (16) and (18) should be identical. Hence, G_{vir1}(s) can be derived by

$$G_{\mathrm{vir1}}(s) = \frac{1-b_3^1}{Z_{\mathrm{vir1}}\left[\left(G_{24} - G_{23}G_{LV3}G_{v3}G_{i3} - \frac{sC_3G_{23}G_{L3}G_{i3}}{sC_3R_{c3}+1}\right)\Delta n_1 + G_{21}G_{i2}\right]} \tag{22}$$

where Δn_1 is equal to $(a_1$–$a_1{}^1)/G_{\mathrm{vir1}}$, which can be given as

$$\Delta n_1 = \frac{G_{31}G_{i2}}{1+G_{33}G_{L3}G_{i3}} \Big/ \left(\frac{sC_3}{sC_3R_{c3}+1} + \frac{G_{33}G_{LV3}G_{v3}G_{i3}}{1+G_{33}G_{L3}G_{i3}}\right). \tag{23}$$

B. Scheme Two of AD Control

Fig. 7 shows the concept of scheme two of AD control. Z_{vir2} may increase the output voltage of Port2 (V_2), which is illustrated

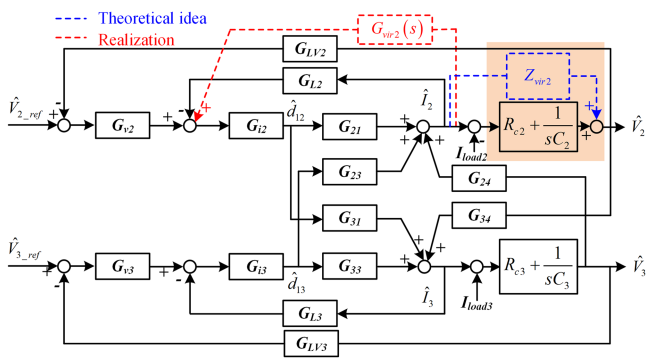

Fig. 7. Scheme two of AD control.

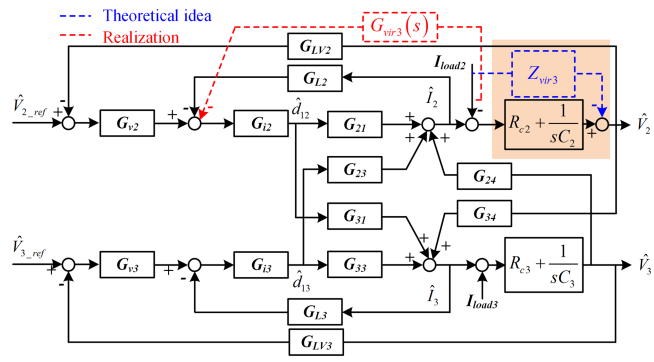

Fig. 8. Scheme three of AD control.

with a blue dashed line. The inherent output impedance $H_r{}^2(s)$ of scheme two can be represented as

$$H_r^2(s) = 1/\left[\frac{sC_2}{sC_2R_{c2}+1} - \frac{a_3}{1-b_3}\left(1+\frac{sC_2Z_{\text{vir2}}}{sC_2R_{c2}+1}\right)\right]. \tag{24}$$

Then, a new transfer function $G_{\text{vir2}}(s)$ is proposed to realize the theoretical idea, which is illustrated as the red dashed line. $H_r{}^2(s)$ with the AD control can be represented as

$$H_r^2(s) = 1/\left[\frac{sC_2}{sC_2R_{c2}+1} - \frac{a_3^2}{1-b_3^2}\right]. \tag{25}$$

where $a_3{}^2$ and $b_3{}^2$ are given as follows:

$$\begin{aligned} a_3^2 &= G_{24}a_1^2 - G_{23}G_{LV3}G_{v3}G_{i3}a_1^2 - G_{23}G_{L3}G_{i3}a_2^2 \\ &\quad - G_{21}G_{LV2}G_{v2}G_{i2} \\ b_3^2 &= G_{24}b_1^2 - G_{23}G_{LV3}G_{v3}G_{i3}b_1^2 - G_{23}G_{L3}G_{i3}b_2^2 \\ &\quad - G_{21}(G_{L2}-G_{vir2})G_{i2} \end{aligned} \tag{26}$$

$$a_2^2 = \frac{sC_3}{sC_3R_{c3}+1}a_1^2;\ b_2^2 = \frac{sC_3}{sC_3R_{c3}+1}b_1^2 \tag{27}$$

$$\begin{aligned} a_1^2 &= \frac{\frac{G_{34}-G_{31}G_{LV2}G_{v2}G_{i2}}{1+G_{33}G_{L3}G_{i3}}}{\frac{sC_3}{sC_3R_{c3}+1}+\frac{G_{33}G_{LV3}G_{v3}G_{i3}}{1+G_{33}G_{L3}G_{i3}}}; \\ b_1^2 &= \frac{\frac{-G_{31}(G_{L2}-G_{vir2})G_{i2}}{1+G_{33}G_{L3}G_{i3}}}{\frac{sC_3}{sC_3R_{c3}+1}+\frac{G_{33}G_{LV3}G_{v3}G_{i3}}{1+G_{33}G_{L3}G_{i3}}}. \end{aligned} \tag{28}$$

Compared with the coefficients of $H_r(s)$ in (7)–(9) and $H_r{}^2(s)$ in (26)–(28), a_1–a_3 are equal to $a_1{}^2$–$a_3{}^2$. Since the denominator of $H_r{}^2(s)$ in (24) and (25) should be equal, $G_{\text{vir2}}(s)$ can be derived as follows:

$$G_{\text{vir2}}(s) = (1-b_3)\cdot Z_{\text{vir2}}/\left[(Z_{\text{vir2}}+R_{c2}+1/sC_2)\cdot m_2\right] \tag{29}$$

$$\begin{aligned} m_2 = &\left(G_{24} - G_{23}G_{LV3}G_{v3}G_{i3} - G_{23}G_{L3}G_{i3}\frac{sC_2}{sC_2R_{c2}+1}\right) \\ &\times \Delta n_2 + G_{21}G_{i2} \end{aligned} \tag{30}$$

where Δn_2 is equal to $(b_1\text{-}b_1{}^2)/G_{\text{vir2}}$, which can be given as follows:

$$\Delta n_2 = \frac{-G_{31}G_{i2}}{1+G_{33}G_{L3}G_{i3}}/\left(\frac{sC_3}{sC_3R_{c3}+1}+\frac{G_{33}G_{\text{LV3}}G_{v3}G_{i3}}{1+G_{33}G_{L3}G_{i3}}\right). \tag{31}$$

C. Scheme Three of AD Control

Fig. 8 shows the concept of scheme three of AD control. Z_{vir3} would decrease the output voltage of Port2 (V_2), which is illustrated with a blue dashed line. Note that the value of virtual impedance in this scheme should be negative to reduce the impedance of Port2. The inherent output impedance $H_r{}^3(s)$ of scheme three can be represented as

$$H_r^3(s) = 1/\left[\frac{sC_2R_{c2}+1}{sC_2(R_{c2}-Z_{\text{vir3}})+1}\left(\frac{sC_2}{sC_2R_{c2}+1}-\frac{a_3}{1-b_3}\right)\right]. \tag{32}$$

Then, $G_{\text{vir3}}(s)$ is introduced to adjust the inner current loop, which is illustrated as the red dashed line. $H_r{}^3(s)$ can be represented as

$$H_r^3(s) = 1/\left[\frac{1-b_3^3}{1-b_3^3-c_3^3}\left(\frac{sC_2}{sC_2R_{c2}+1}-\frac{a_3^3}{1-b_3^3}\right)\right] \tag{33}$$

where $a_3{}^3$, $b_3{}^3$, and $c_3{}^3$ are given as follows:

$$\begin{cases} a_3^3 = G_{24}a_1^3 - G_{23}G_{LV3}G_{v3}G_{i3}a_1^3 - G_{23}G_{L3}G_{i3}a_2^3 \\ \quad -G_{21}G_{LV2}G_{v2}G_{i2} \\ b_3^3 = G_{24}b_1^3 - G_{23}G_{LV3}G_{v3}G_{i3}b_1^3 - G_{23}G_{L3}G_{i3}b_2^3 \\ \quad -G_{21}G_{L2}G_{i2} \\ c_3^3 = G_{24}c_1^3 - G_{23}G_{LV3}G_{v3}G_{i3}c_1^3 - G_{23}G_{L3}G_{i3}c_2^3 \\ \quad +G_{21}G_{vir3}G_{i2} \end{cases} \tag{34}$$

$$a_2^3 = \frac{sC_3}{sC_3R_{c3}+1}a_1^3;\ b_2^3 = \frac{sC_3}{sC_3R_{c3}+1}b_1^3;\ c_2^3 = \frac{sC_3}{sC_3R_{c3}+1}c_1^3 \tag{35}$$

$$\begin{aligned} a_1^3 = &\frac{G_{34}-G_{31}G_{LV2}G_{v2}G_{i2}}{1+G_{33}G_{L3}G_{i3}}/\left(\frac{sC_3}{sC_3R_{c3}+1}\right. \\ &\left.+\frac{G_{33}G_{LV3}G_{v3}G_{i3}}{1+G_{33}G_{L3}G_{i3}}\right) \end{aligned}$$

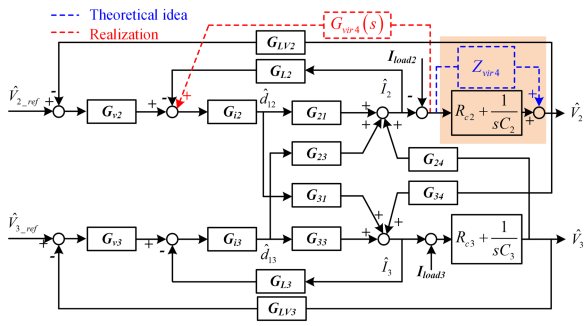

Fig. 9. Scheme four of AD control.

$$b_1^3=\frac{-G_{31}G_{L2}G_{i2}}{1+G_{33}G_{L3}G_{i3}}\Big/\left(\frac{sC_3}{sC_3R_{c3}+1}+\frac{G_{33}G_{LV3}G_{v3}G_{i3}}{1+G_{33}G_{L3}G_{i3}}\right)$$
$$c_1^3=\frac{G_{31}G_{\text{vir3}}G_{i2}}{1+G_{33}G_{L3}G_{i3}}\Big/\left(\frac{sC_3}{sC_3R_{c3}+1}+\frac{G_{33}G_{LV3}G_{v3}G_{i3}}{1+G_{33}G_{L3}G_{i3}}\right). \tag{36}$$

Compared with the coefficients of H_r(s) in (7)–(9) and $H_r{}^3$(s) in (34)–(36), a_1–a_3 are equal to $a_1{}^3$–$a_3{}^3$. b_1–b_3 are equal to $b_1{}^3$–$b_3{}^3$. Hence, G_{vir3}(s) can be derived as follows:

$$G_{\text{vir3}}(s)=(1-b_3)\cdot Z_{\text{vir3}}\cdot sC_2/\left[(sC_2R_{c2}+1)\,m_3\right]. \tag{37}$$

$$m_3=\left(G_{24}-G_{23}G_{LV3}G_{v3}G_{i3}-G_{23}G_{L3}G_{i3}\frac{sC_2}{sC_2R_{c2}+1}\right)\times\Delta n_3+G_{21}G_{i2} \tag{38}$$

where Δn_3 is equal to $c_1{}^3/G_{\text{vir3}}$.

D. Scheme Four of AD Control

Fig. 9 shows the concept of type four of AD control. The inherent output impedance $H_r{}^4$(s) with this theoretical idea can be represented as

$$H_r^4(s)=1\Big/\left(\frac{sC_2}{sC_2\left(R_{c2}+Z_{\text{vir4}}\right)+1}-\frac{a_3}{1-b_3}\right). \tag{39}$$

Then, G_{vir4}(s) is introduced to adjust the inner current loop to achieve the theoretical idea. $H_r{}^4$(s) with the virtual impedance-based AD control can be represented as

$$H_r^4(s)=1\Big/\left[\frac{1-b_3^4}{1-b_3^4-c_3^4}\left(\frac{sC_2}{sC_2R_{c2}+1}-\frac{a_3^4}{1-b_3^4}\right)\right] \tag{40}$$

where $a_3{}^4$, $b_3{}^4$, and $c_3{}^4$ are given as follows:

$$\begin{cases} a_3^4=\left(G_{24}-G_{23}G_{LV3}G_{v3}G_{i3}\right)a_1^4-G_{23}G_{L3}G_{i3}a_2^4 \\ \quad -G_{21}G_{LV2}G_{v2}G_{i2} \\ b_3^4=\left(G_{24}-G_{23}G_{LV3}G_{v3}G_{i3}\right)b_1^4-G_{23}G_{L3}G_{i3}b_2^4 \\ \quad -G_{21}\left(G_{L2}-G_{\text{vir4}}\right)G_{i2} \\ c_3^4=\left(G_{24}-G_{23}G_{LV3}G_{v3}G_{i3}\right)c_1^4-G_{23}G_{L3}G_{i3}c_2^4 \\ \quad -G_{21}G_{\text{vir4}}G_{i2} \end{cases} \tag{41}$$

TABLE II
G_{VIR}(S) OF DIFFERENT SCHEMES IN SIMULATION

	G_{vir}(s)
1	$G_{vir1}\big\|_{Z=100}=\frac{1.957e^{-4}s^2+58.26s+3.617e^4}{s^2+4127s+3.617e^6}$; $G_{vir1}\big\|_{Z=50}=\frac{3.915e^{-4}s^2+116.5s+7.235e^4}{s^2+4127s+3.617e^6}$
	$G_{vir1}\big\|_{Z=20}=\frac{9.787e^{-4}s^2+291.3s+1.809e^5}{s^2+4127s+3.617e^6}$; $G_{vir1}\big\|_{Z=10}=\frac{1.957e^{-3}s^2+582.6s+3.617e^5}{s^2+4127s+3.617e^6}$
2	$G_{vir2}\big\|_{Z=1}=\frac{0.05514s^2+5207s+3.001e^{-6}}{s^2+4016s+5.786e^6}$; $G_{vir2}\big\|_{Z=4}=\frac{-0.07888s^2+7182s+9.172e^{-9}}{s^2+5224s+2.336e^6}$
	$G_{vir2}\big\|_{Z=7}=\frac{-0.1668s^2+8581s+2.217e^{-7}}{s^2+6547s+1.664e^6}$; $G_{vir2}\big\|_{Z=9}=\frac{-0.2089s^2+9324s+2.306e^{-7}}{s^2+6943s+1.531e^6}$
3	$G_{vir3}\big\|_{Z=-1}=\frac{-23.17s^2-1.036e^6s+0.07368}{s^2+2.137e^5s+9.331e^8}$; $G_{vir3}\big\|_{Z=-5}=\frac{-115.8s^2-5.181e^6s+0.4805}{s^2+2.137e^5s+9.331e^8}$
	$G_{vir3}\big\|_{Z=-7}=\frac{-162.2s^2-7.254e^6s+0.6781}{s^2+2.137e^5s+9.331e^8}$; $G_{vir3}\big\|_{Z=-10}=\frac{-231.7s^2-1.036e^7s+0.9612}{s^2+2.137e^5s+9.331e^8}$
4	$G_{vir4}\big\|_{Z=1}=\frac{0.0552s^2+5207s+8.642e^{-6}}{s^2+4015s+5.786e^6}$; $G_{vir4}\big\|_{Z=3}=\frac{-0.04044s^2+6621s-5.768e^{-6}}{s^2+4756s+2.787e^6}$
	$G_{vir4}\big\|_{Z=5}=\frac{-0.1122s^2+7692s+5.946e^{-8}}{s^2+5684s+2.041e^6}$; $G_{vir4}\big\|_{Z=7}=\frac{-0.1668s^2+8582s-7.195e^{-8}}{s^2+6546s+1.664e^6}$

$$a_2^4=\frac{sC_3}{sC_3R_{c3}+1}a_1^4;\ b_2^4=\frac{sC_3}{sC_3R_{c3}+1}b_1^4;\ c_2^4=\frac{sC_3}{sC_3R_{c3}+1}c_1^4 \tag{42}$$

$$a_1^4=\frac{G_{34}-G_{31}G_{LV2}G_{v2}G_{i2}}{1+G_{33}G_{L3}G_{i3}}\Big/\left(\frac{sC_3}{sC_3R_{c3}+1}+\frac{G_{33}G_{LV3}G_{v3}G_{i3}}{1+G_{33}G_{L3}G_{i3}}\right)$$
$$b_1^4=\frac{-G_{31}\left(G_{L2}-G_{\text{vir4}}\right)G_{i2}}{1+G_{33}G_{L3}G_{i3}}\Big/\left(\frac{sC_3}{sC_3R_{c3}+1}+\frac{G_{33}G_{LV3}G_{v3}G_{i3}}{1+G_{33}G_{L3}G_{i3}}\right)$$
$$c_1^4=\frac{-G_{31}G_{\text{vir4}}G_{i2}}{1+G_{33}G_{L3}G_{i3}}\Big/\left(\frac{sC_3}{sC_3R_{c3}+1}+\frac{G_{33}G_{LV3}G_{v3}G_{i3}}{1+G_{33}G_{L3}G_{i3}}\right). \tag{43}$$

Compared with the coefficients of H_r(s) in (7)–(9) and $H_r{}^4$(s) in (41)–(43), a_1–a_3 are equal to $a_1{}^3$–$a_3{}^3$. G_{vir3}(s) can be derived by

$$G_{\text{vir4}}(s)=(1-b_3)\,sC_2Z_{\text{vir4}}/\left[(sC_2R_{c2}+sC_2Z_{\text{vir4}}+1)\,m_4\right] \tag{44}$$

$$m_4=\left(G_{24}-G_{23}G_{LV3}G_{v3}G_{i3}-G_{23}G_{L3}G_{i3}\frac{sC_2}{sC_2R_{c2}+1}\right)\times\Delta n_4+G_{21}G_{i2} \tag{45}$$

where Δn_4 can be expressed as

$$\Delta n_4=\frac{G_{31}G_{i2}}{1+G_{33}G_{L3}G_{i3}}\Big/\left(\frac{sC_3}{sC_3R_{c3}+1}+\frac{G_{33}G_{LV3}G_{v3}G_{i3}}{1+G_{33}G_{L3}G_{i3}}\right). \tag{46}$$

IV. SIMULATION VERIFICATION

In this section, simulation verification is performed to validate the proposed AD method. G_{vir} of each scheme is reduced to the second-order transfer function and given in Table II. The effect of each scheme on the output impedance of Port2 and dynamic characteristics is analyzed.

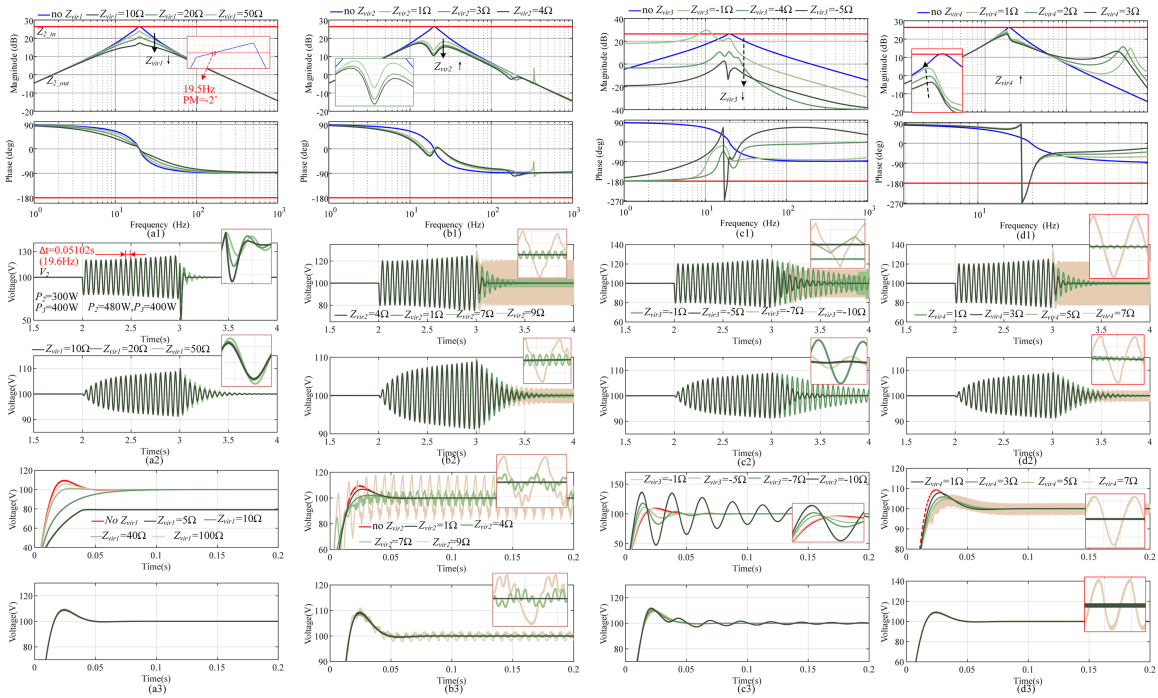

Fig. 10. Simulation results of AD control. (a1) Impedance characteristic of scheme one. (a2) Voltage waveform of scheme one. (a3) Step response of scheme one. (b1) Impedance characteristic of scheme two. (b2) Voltage waveform of scheme two. (b3) Step response of scheme two. (c1) Impedance characteristic of scheme three. (c2) Voltage waveform of scheme three. (c3) Step response of scheme three. (d1) Impedance characteristic of scheme four. (d2) Voltage waveform of scheme four. (d3) Step response of scheme four.

A. Scheme One of AD Control

Fig. 10(a1) and (a2) shows the impedance characteristic and voltage waveform under scheme one. It can be seen from Fig. 10(a1) that there are two intersection points between the output impedance Z_{2_out} and input impedance of CPL Z_{2_in} when P_2 is 480 W and P_3 is 400 W. The frequency and PM of the left intersection point is 19.5 Hz and -2°, which indicates the system is unstable. It can also be seen from Fig. 10(a1) that Z_{2_out} is decreased when scheme one of AD control is implemented, which indicates that the system can be stabilized. Fig. 10(a2) shows the voltage waveform when scheme one is implemented. It can be seen that there is an oscillation with 19.6 Hz at 2 s when P_2 is increased to 480 W, which agrees with the theoretical analysis in Fig. 10(a1). The oscillation disappears when scheme one is enabled at 3 s. It can be seen that the voltage recovery is faster when Z_{vir1} is 20 Ω.

Fig. 10(a3) shows the step response when Port2 and Port3 of the TAB converter connect with a 20 Ω resistor. It can be seen that the overshoot is improved as the virtual resistor Z_{vir1} decreases at Port2. But the voltage waveform at Port3 is not changed.

B. Scheme Two of AD Control

Fig. 10(b1) and (b2) shows the impedance characteristic and voltage waveform of Port2 under scheme two. It can be seen from Fig. 10(b1) that there will be no intersection points between Z_{2_out} and Z_{2_in} when the virtual resistor Z_{vir2} increases, which indicates that the system would be stable. For the voltage waveform shown in Fig. 10(b2), it can be seen that the voltage recovery is faster when Z_{vir2} is changed from 1 to 4 Ω. However, when Z_{vir2} is increased to 7 and 9 Ω, the oscillation happens again. It indicates that the system is not a minimum-phase system when Z_{vir2} is 7 and 9Ω. It can also be seen from Fig. 10(b3) that the step response causes oscillation when Z_{vir2} is 7 and 9 Ω.

C. Scheme Three of AD Control

Fig. 10(c1) and (c2) shows the impedance characteristic and voltage waveform of Port2 under scheme three. It can be seen from Fig. 10(c1) that the magnitude of Z_{2_out} is decreased and the system is stable when Z_{vir3} is decreased to -5 from -1 Ω. While Z_{vir3} is -7 Ω, it can be seen from Fig. 10(c2) that there is a large voltage ripple introduced by equivalent G_{vir3}. Meanwhile, it can be seen from Fig. 10(c3) that the response speed is increased when Z_{vir3} is changed from -1 to -10 Ω. The PM under scheme three is decreased, which thus leads to a large overshoot.

D. Scheme Four of AD Control

Fig. 10(d1) shows the impedance characteristic of Z_{2_out} with scheme four. It can be seen from Fig. 10(d1) that there are no intersection points between Z_{2_out} and Z_{2_in} when the virtual impedance Z_{vir4} is 1, 2, and 3 Ω, which indicates the system would be stable.

Fig. 10(d2) shows the voltage waveform under scheme four. It can be seen that the oscillation phenomenon disappears when Z_{vir4} is 1 and 3 Ω. When Z_{vir4} is increased to 5 Ω, the oscillation can be seen in the voltage waveform of Port2 and Port3. The

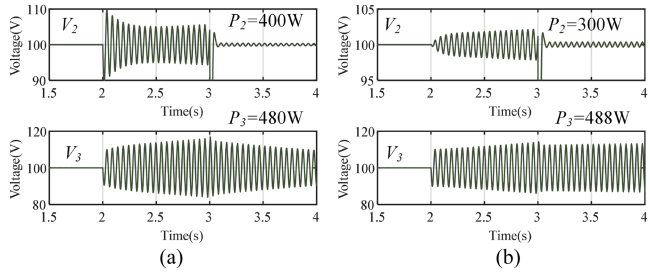

Fig. 11. Voltage waveform when oscillation occurs with different P_3. (a) $P_2 = 400$ W and $P_3 = 480$ W. (b) $P_2 = 300$ W and $P_3 = 488$ W.

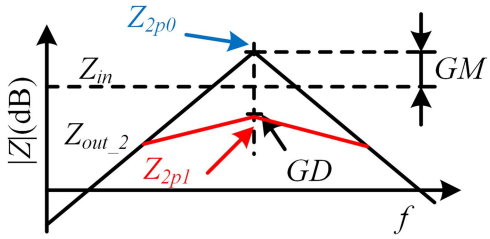

Fig. 12. Impedance characteristics at Port2 with scheme one of AD controls.

oscillation amplitude is higher when Z_{vir4} is 7 Ω. Meanwhile, it can be seen from Fig. 10(d3) that the overshoot is improved when Z_{vir4} is increased. However, the step response would be unstable if Z_{vir4} is continuously increased.

E. Operation Range of Proposed AD Control

It is revealed in [6] that the CPL at Port3 has an impact on the stable region of Port2. If the power of CPL of Port3 increases, the stable region of Port2 will be reduced. Fig. 11 shows the voltage waveform of Port2 and Port3 when CPL power at Port3 is increased to 480 and 488 W. However, as shown in Fig. 11, Port3 induces the oscillation phenomenon instead of Port2. Thus, the proposed AD control and the operation region analysis should be implemented on the port which supplies the largest CPL power. Thus, the operation region of the proposed AD control for the TAB converter resembles the two-port dc–dc converter in [18] and [20].

1) Scheme One of AD Controls (Parallel): Fig. 12 shows the curve of output impedance ($Z_{\mathrm{out\_2}}$) at Port2. Z_{2p0} represents the peak value of $Z_{\mathrm{out\_2}}$ without the implementation of scheme one of AD controls. Z_{2p1} represents the peak value of with scheme one. GD is the gain difference between Z_{2p0} and Z_{2p1}, measured in dB. It equals to gain margin (GM) when Z_{2p1} equals Z_{in}. Z_{2p1} can be expressed by Z_{2p} as

$$Z_{\mathrm{2p0}} = Z_{\mathrm{2p1}} 10^{\frac{\mathrm{GD}}{20}}. \tag{47}$$

Then, Z_{vir1} can be represented as

$$\frac{1}{Z_{\mathrm{vir1}}} = \frac{1}{Z_{\mathrm{2p1}}} - \frac{1}{Z_{\mathrm{2p0}}} \Rightarrow Z_{\mathrm{vir1}} = Z_{\mathrm{2p1}} / \left(1 - \frac{1}{10^{\frac{\mathrm{GD}}{20}}}\right). \tag{48}$$

Z_{in} represents the CPL impedance at Port2, which equals $-V_2{}^2/P_2$. $|Z_{\mathrm{2p}}|$ should smaller than $|Z_{\mathrm{in}}|$. Thus, (48) can be rewritten as

$$Z_{\mathrm{vir1}} < \left(\frac{V_2^2}{P_2}\right) / \left(1 - \frac{1}{10^{\frac{\mathrm{GM}}{20}}}\right). \tag{49}$$

Meanwhile, the current flowing through Z_{vir1} cannot be larger than the maximum power of Port2. Thus, the region of Z_{vir1} can be represented as

$$\frac{V_2^2}{P_{\mathrm{2m}}} < Z_{\mathrm{vir1}} < \left(\frac{V_2^2}{P_2}\right) / \left(1 - \frac{1}{10^{\frac{\mathrm{GM}}{20}}}\right) \tag{50}$$

where P_{2m} represents the maximum transferring power of Port2.

2) Scheme Three of AD Controls (Series): In this scheme, Z_{vir3} should satisfy the inequality, which is expressed as

$$Z_{\mathrm{2p0}} - |Z_{\mathrm{vir3}}| < |Z_{\mathrm{in}}|. \tag{51}$$

Z_{2p0} can be represented by Z_{in} as

$$Z_{\mathrm{2p0}} = |Z_{\mathrm{in}}| \, 10^{\frac{\mathrm{GM}}{20}}. \tag{52}$$

Thus, (50) can be rewritten as

$$|Z_{\mathrm{vir3}}| > \frac{V_2^2}{P_2}\left(10^{\frac{\mathrm{GM}}{20}} - 1\right). \tag{53}$$

Meanwhile, as shown in Fig. 5(c), the introduction of Z_{vir3} can reduce the voltage of capacitor C_2. Thus, the maximum value of $|Z_{\mathrm{vir3}}|$ cannot make capacitor voltage zero when the output current is maximum. Thus, the region of $|Z_{\mathrm{vir3}}|$ can be represented as

$$\frac{V_2^2}{P_{\mathrm{2m}}} > |Z_{\mathrm{vir3}}| > \frac{V_2^2}{P_2}\left(10^{\frac{\mathrm{GM}}{20}} - 1\right). \tag{54}$$

It is noted that the inequality is satisfied only when the left item is greater than the right item.

3) Schemes Two and Four of AD Controls: In schemes two and four of the proposed AD controls, the output current I_2 is feedback to the inner current loop through G_{vir2} and G_{vir4}. It can be combined with current LPF G_{L2} to G_{L2}–$G_{\mathrm{vir2,3}}$. It can be seen from Fig. 13 that the introduction of Z_{vir2} and Z_{vir4} can reduces the bandwidth of the inner current loop. For scheme two of AD controls, the bandwidth of the inner current loop is reduced to about 100 Hz when Z_{vir2} is 7 and 9 Ω. Also, the bandwidth of the inner current loop in scheme four is reduced to about 100 Hz when Z_{vir4} is 5 and 7 Ω. Thus, in this work, the maximum value of Z_{vir2} and Z_{vir4} is not allowed to reduce the bandwidth of the current loop to 100 Hz, which equals the cutoff frequency of outer voltage LPF $G_{\mathrm{LV2,3}}$ in Table I.

V. Experimental Verification

A scale-down experiment is implemented to validate the proposed AD control. Fig. 14(a) and (b) shows the experimental setup and equivalent circuit, where the controller is executed by PLECS RTbox. The CPL at Port2 and Port3 is emulated by a buck converter in which voltage control is applied to keep the output voltage at 40 V. The experimental parameters are given in Table III.

Fig. 15(a) and (b) shows the output voltage and current waveform of the TAB converter and two buck converters, respectively. The system operates stably when the buck converter at Port2 and Port3 are both connected with an 80 Ω resistor. While the

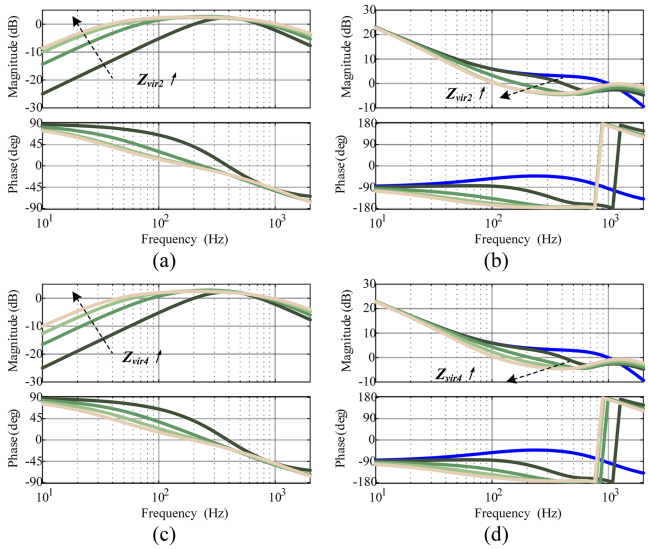

Fig. 13. Impedance characteristics with schemes two and four. (a) G_{vir2}. (b) Loop gain of the current loop with scheme two. (c) G_{vir4}. (d) Loop gain of the current loop with scheme four.

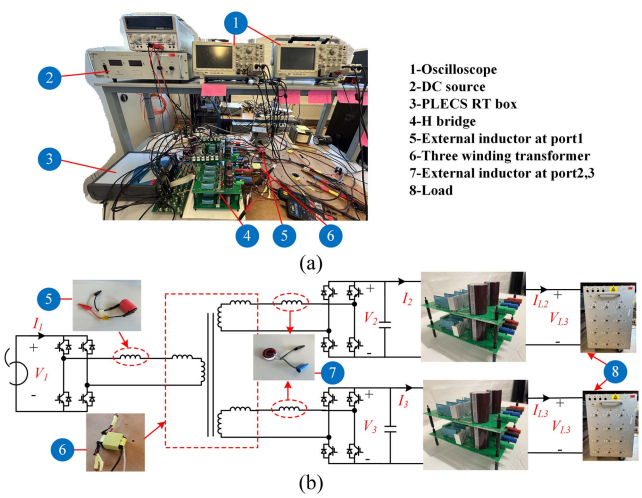

Fig. 14. Experimental setup. (a) Laboratory prototype. (b) Equivalent circuit.

TABLE III
MAIN PARAMETERS OF LABORATORY SETUP

Symbol	Quantity	Value
V_1	Nominal voltage of Port1 (V)	100
$V_{2,3}$	Nominal voltage of Port2 and Port3 (V)	50
L_{e1}	External inductor at Port1 (μH)	40
$L_{e2,3}$	External inductor at Port2 and Port3 (μH)	120
L_{12}	Leakage inductor	5.27
L_{13}	Leakage inductor	5.52
L_{23}	Leakage inductor	3.31
L_{buck}	Buck inductor (μH)	1000
C_{buck}	Buck capacitor (μF)	330
T_{step}	System discretization step size (s)	1e-5
$G_{v2,3}$	voltage controller of TAB	0.1+5.024/s
$G_{i2,3}$	current controller of TAB	0.01+0.314/s
G_{buck2}	voltage controller of buck converter at Port2	0.005+0.5652/s
G_{buck3}	voltage controller of buck converter at Port3	0.0005+0.05652/s

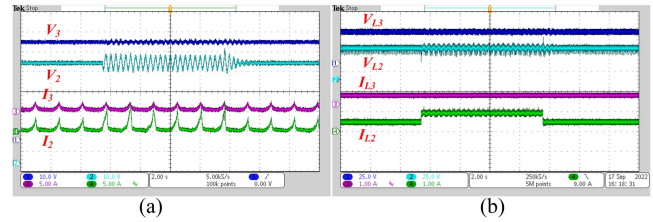

Fig. 15. Voltage and current waveform without AD method. (a) TAB converter. (b) Buck converter.

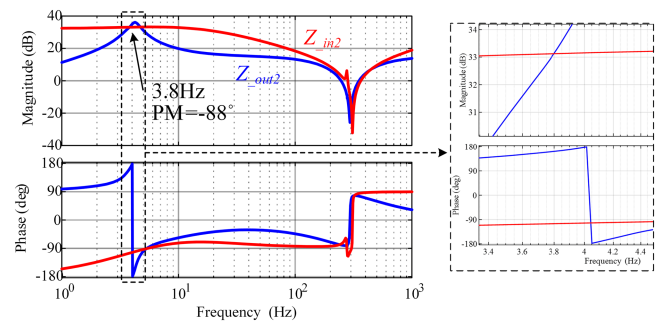

Fig. 16. Impedance characteristic of Port2 in the experiment.

TABLE IV
G_{VIR}(S) OF DIFFERENT SCHEMES IN EXPERIMENT

	G_{vir}(s)
1	$G_{vir1}\vert_{Z=66.7}=\dfrac{0.02089s^2+2.884s+67.34}{s^2+53.2s+4489}$; $G_{vir1}\vert_{Z=46.5}=\dfrac{0.02995s^2+5.566s+96.5}{s^2+53.2s+4489}$ $G_{vir1}\vert_{Z=40}=\dfrac{0.03483s^2+6.473s+112.2}{s^2+53.2s+4489}$
2	$G_{vir2}\vert_{Z=3}=\dfrac{1.05s^2+576.2s-4.239e^{-7}}{s^2+199.7s+3.644e^4}$; $G_{vir2}\vert_{Z=10}=\dfrac{1.39s^2+411.1s-1.796e^{-7}}{s^2+100.4s+1.138e^4}$ $G_{vir2}\vert_{Z=80}=\dfrac{0.8999s^2+530.3s-4.954e^{-8}}{s^2+121.8s+5541}$
3	$G_{vir3}\vert_{Z=-5}=\dfrac{-292.7s^2-8.462e^5s+0.0252}{s^2+5.387e^4s+2.647e^7}$; $G_{vir3}\vert_{Z=-20}=\dfrac{-1171s^2-3.385e^6s-0.1009}{s^2+5.387e^4s+2.647e^7}$ $G_{vir3}\vert_{Z=-60}=\dfrac{-3512s^2-1.015e^7s+0.2058}{s^2+5.387e^4s+2.647e^7}$;
4	$G_{vir4}\vert_{Z=3}=\dfrac{1.05s^2+576.2s-3.761e^{-8}}{s^2+199.7s+3.644e^4}$; $G_{vir4}\vert_{Z=10}=\dfrac{1.39s^2+411.1s+6.726e^{-7}}{s^2+100.4s+1.138e^4}$ $G_{vir4}\vert_{Z=100}=\dfrac{0.823s^2+557.7s-2.741e^{-7}}{s^2+129.9s+5483}$

resistor at Port2 is increased to 26.7 Ω, the system becomes unstable with 3 Hz oscillation. Substituting the experimental parameters into (4)–(15), the output impedance of Port2 and input impedance of the buck converter at Port2 are illustrated in Fig. 16. It can be seen that the frequency of the intersection point is 3.8 Hz and the PM is −88°. It indicates that the system has a 3.8 Hz oscillation, which is consistent with the experimental phenomenon in Fig. 15. Then, the oscillation disappears when the resistor is decreased to 80 Ω.

The proposed AD control is applied to eliminate the oscillation and the $G_{\mathrm{vir1\text{-}4}}$ of each scheme of AD control in the experiment is listed in Table IV.

Fig. 17(a1)–(a3) shows the experimental results when scheme one is enabled. It can be seen from Fig. 17(a1) that the oscillation issue disappears gradually when virtual resistor Z_{vir1} is 66.7 Ω. The oscillation issue disappears faster as shown in Fig. 17(a2) when Z_{vir1} is 46.5 Ω. While the Z_{vir1} is decreased to 40 Ω, the

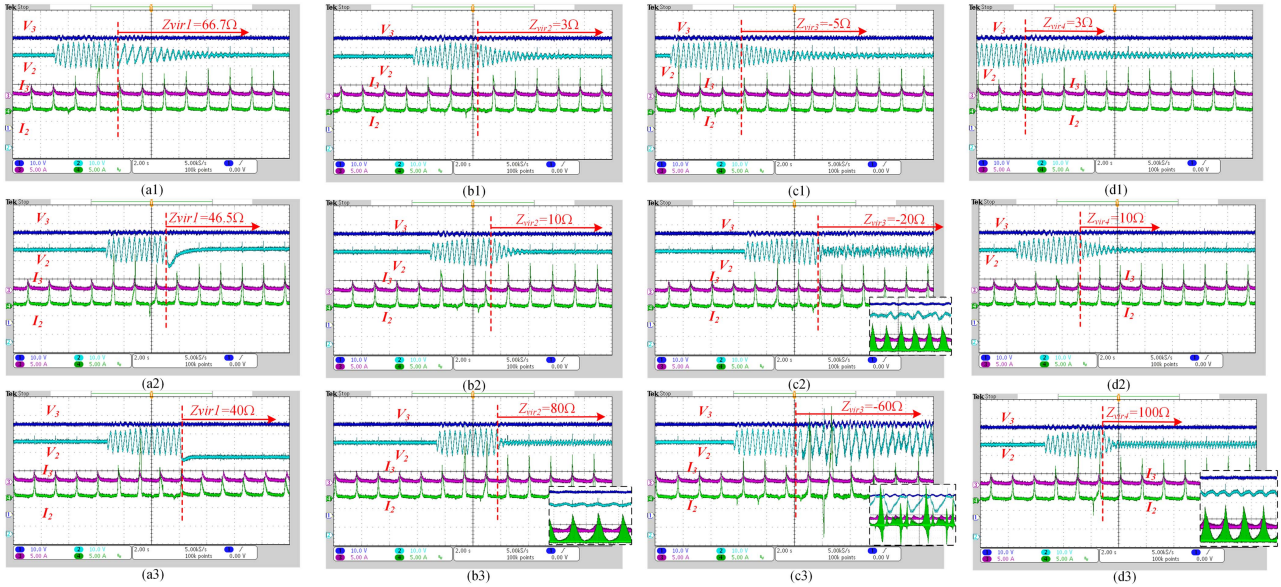

Fig. 17. Experimental results of AD control of schemes one–four. (a1) $Z_{\mathrm{vir1}} = 66.7\ \Omega$. (a2) $Z_{\mathrm{vir1}} = 46.5\ \Omega$. (a3) $Z_{\mathrm{vir1}} = 40\ \Omega$. (b1) $Z_{\mathrm{vir2}} = 3\ \Omega$. (b2) $Z_{\mathrm{vir2}} = 10\ \Omega$. (b3) $Z_{\mathrm{vir2}} = 80\ \Omega$. (c1) $Z_{\mathrm{vir3}} = -5\ \Omega$. (c2) $Z_{\mathrm{vir3}} = -20\ \Omega$. (c3) $Z_{\mathrm{vir3}} = -60\ \Omega$. (d1) $Z_{\mathrm{vir4}} = 3\ \Omega$. (d2) $Z_{\mathrm{vir4}} = 10\ \Omega$. (d3) $Z_{\mathrm{vir4}} = 100\ \Omega$.

oscillation phenomenon also disappears, but the bus voltage is decreased, which agrees with the analysis in Section IV-A.

Fig. 17(b1)–(b3) shows the experimental results when scheme two is enabled. It can be seen that the oscillation issue can be eliminated obviously when Z_{vir2} is 3 and 10 Ω. However, when Z_{vir2} is increased to 80 Ω, there exists a small fluctuation at Port2 voltage, which agrees with the analysis in Section IV-B.

Fig. 17(c1)–(c3) shows the experimental results when scheme three is enabled. It can be seen that the oscillation issue disappears when Z_{vir3} is $-5\ \Omega$. While the voltage oscillation happens when Z_{vir3} is decreased to $-20\ \Omega$. The oscillation becomes more serious when Z_{vir3} is decreased to $-80\ \Omega$, which agrees with the analysis in Section IV-C.

Fig. 17(d1)–(d3) shows the experimental results when scheme four is enabled. It can be seen that the oscillation issue can be eliminated obviously when Z_{vir4} is 3 and 10 Ω. However, when Z_{vir4} is increased to 100 Ω, there exists a small fluctuation at Port2 voltage, which agrees with the analysis in Section IV-D.

VI. Conclusion

This article developed a virtual impedance-based AD control to suppress the instability issue of the TAB converter with two CPLs. The proposed AD control consisted of four schemes which correspond to four different positions of virtual impedance at the output capacitor of Port2. The proposed AD control was achieved by adding virtual impedance to the inner current loop, where the equivalent transfer function of each scheme was obtained by comparing the output impedance with or without virtual impedance. The range of virtual impedance at different positions was specified.

Simulation and experimental results showed the effectiveness of the proposed AD methods for oscillation suppression. In scheme one, a high virtual impedance value could not maintain the terminal voltage. For schemes two, three, and four, a small fluctuation in bus voltage existed with high virtual impedance. The proposed AD method provided an effective solution to oscillation suppression for the application of multiport converters in industry.

Appendix

TABLE V
Coefficients of the Small Signal Model of TAB Converter

$$G_{11} = \frac{n_1\overline{V}_2}{2n_2 f_s L_{12}}\left(1-2\left|\overline{d}_{12}\right|\right), G_{12} = \frac{n_1\overline{d}_{12}}{2n_2 f_s L_{12}}\left(1-\left|\overline{d}_{12}\right|\right)$$

$$G_{13} = \frac{n_1\overline{V}_3}{2n_3 f_s L_{13}}\left(1-2\left|\overline{d}_{13}\right|\right), G_{14} = \frac{n_1\overline{d}_{13}}{2n_3 f_s L_{13}}\left(1-\left|\overline{d}_{13}\right|\right)$$

$$G_{22} = \frac{n_1\overline{d}_{12}}{2n_2 f_s L_{12}}\left(1-\left|\overline{d}_{12}\right|\right), G_{23} = -\frac{n_1^2\overline{V}_3}{2n_2 n_3 f_s L_{23}}\left(1-2\left|\overline{d}_{13}-\overline{d}_{12}\right|\right)$$

$$G_{24} = -\frac{n_1^2\left(\overline{d}_{13}-\overline{d}_{12}\right)}{2n_2 n_3 f_s L_{23}}\left(1-\left|\overline{d}_{13}-\overline{d}_{12}\right|\right), G_{31} = -\frac{n_1^2\overline{V}_1}{2n_2 n_3 f_s L_{23}}\left(1-2\left|\overline{d}_{13}-\overline{d}_{12}\right|\right)$$

$$G_{32} = \frac{n_1\overline{d}_{13}}{2n_3 f_s L_{13}}\left(1-\left|\overline{d}_{13}\right|\right), G_{34} = \frac{n_1^2\left(\overline{d}_{13}-\overline{d}_{12}\right)}{2n_2 n_3 f_s L_{23}}\left(1-\left|\overline{d}_{13}-\overline{d}_{12}\right|\right)$$

$$G_{21} = \frac{n_1\overline{V}_1}{2n_2 f_s L_{12}}\left(1-2\left|\overline{d}_{12}\right|\right) + \frac{n_1^2\overline{V}_3}{2n_2 n_3 f_s L_{23}}\left(1-2\left|\overline{d}_{13}-\overline{d}_{12}\right|\right)$$

$$G_{33} = \frac{n_1\overline{V}_1}{2n_3 f_s L_{13}}\left(1-2\left|\overline{d}_{13}\right|\right) + \frac{n_1^2\overline{V}_2}{2n_2 n_3 f_s L_{23}}\left(1-2\left|\overline{d}_{13}-\overline{d}_{12}\right|\right)$$

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Haoyuan Yu (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2016 and 2019, respectively, and the Ph.D. degree with AAU Energy, Aalborg University, Aalborg, Denmark, in 2024.

From October to December 2022, he was a visiting scholar with DC Systems, Energy Conversion, and Storage Group of the Department of Electrical Sustainable Energy, Delft University of Technology, Delft, The Netherlands. His research interests include power management, dc system stability, and multiport converter applications in dc traction power supply systems.

Hanwen Zhang (Graduate Student Member, IEEE) received the B.Eng. and M.Sc. degrees in electrical engineering from Northeast Electric Power University, Jilin, China, in 2017 and 2020, respectively. He is currently working toward the Ph.D. degree with AAU Energy, Aalborg University, Aalborg, Denmark.

In 2018, he was a visiting student with the School of Engineering, Cardiff University, Cardiff, U.K. Since 2021, he has been a Ph.D. student researcher with EUROfusion Consortium. In 2023, he was invited as a visiting Ph.D. student with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada. In 2024, he was a visiting Ph.D. student with the Department of Industrial Engineering, University of Rome "Tor Vergata," Rome, Italy. His research interests include dc grids, multiport dc converters, dc circuit breakers, FACTS, and nuclear fusion power plant protections.

Qi Zhang (Student Member, IEEE) received the B.Eng. and M.Sc. degrees in electrical engineering from China University of Mining and Technology-Beijing, Beijing, China, in 2015 and 2018, respectively.

He is currently a Research Assistant with Energy Technology from AAU Energy, Aalborg University, Aalborg, Denmark. His research interests include fault analysis of the power electronic-dominated power system, modeling and control of the power electronic-dominated power system, modeling and control of power electronic converters, selective harmonic elimination modulation, and protection of grid-connected converters and the power electronic-dominated grid.

Yanbo Wang (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the Department of Energy Technology, Aalborg University, Aalborg, Denmark, in 2017.

Since 2017, he has been a Postdoctoral Fellow, an Assistant Professor, and an Associate Professor with the Department of Energy Technology, Aalborg University. From June to October 2016, he was a visiting scholar with the Power System Research Group of the Department of Electrical and Computer Engineering, University of Manitoba. His research interests include distributed power generation systems, wind power systems, microgrids, and power electronic-dominated power systems.

Zian Qin (Senior Member, IEEE) received the B.Eng. degree from Beihang University, Beijing, China, in 2009, the M.Eng. degree from Beijing Institute of Technology, Beijing, China, in 2012, and the Ph.D. degree from Aalborg University, Aalborg, Denmark, in 2015, all in electrical engineering.

He is currently an Associate Professor with Delft University of Technology, Delft, The Netherlands. In 2014, he was a visiting Scientist with Aachen University, Aachen, Germany. His research interests include power quality and stability of power electronics-based grids and solid-state transformers. He authored or coauthored more than 100 journals/conference papers, 4 book chapters, and 2 international patents, and worked on several European and Dutch national projects in these areas.

Prof. Qin is an Associate Editor for IEEE Trans Industrial Electronics, and a Guest Associate Editor of IEEE Transaction Power Electronics, IEEE Journal of Emerging and Selected Topics, and IEEE Transaction Energy Conversion. He is a Distinguished Reviewer for IEEE Transactions of Industrial Electronics in 2020. He was the Technical Program Chair of IEEE-PEDG 2024, IEEE-PEDG 2023, IEEE-ISIE 2020, IEEE-COMPEL 2020, etc.

Zhe Chen (Fellow, IEEE) received the B.Eng. and M.Sc. degrees in electrical engineering from Northeast China Institute of Electric Power Engineering, Jilin City, China, in 1982 and 1986, respectively, the M.Phil. degree in power electronics from Staffordshire University, Stoke-on-Trent, U.K., 1993, and the Ph.D. degree in power and control from University of Durham, Durham, U.K., in 1997.

Since 2002, he has been a Full Professor with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. He is the leader of the Wind Power System Research program with the Department of Energy Technology, Aalborg University. His research interests include wind power, power electronics, power systems, and multienergy systems.

Dr. Chen is an Associate Editor for IEEE Transactions on Power Electronics, a member of editorial boards for many international journals, a Fellow of the Institution of Engineering and Technology (U.K.), and a Chartered Engineer in the U.K.

Pavol Bauer (Senior Member, IEEE) received the M.Sc. degree in electrical engineering from the Technical University of Kosice, Kosice, Slovakia, in 1985, and the Ph.D. degree in power electronics from the Delft University of Technology, Delft, The Netherlands, in 1995.

From 2002 to 2003, he was with KEMA (DNV GL), Arnhem, The Netherlands. He is currently a Full Professor with the Department of Electrical Sustainable Energy, Delft University of Technology, and the Head of DC Systems, Energy Conversion, and Storage Group. He is also a Professor with the Brno University of Technology, Brno, Czech Republic, and an Honorary Professor with the Politehnica University Timisoara, Timisoara, Romania. He authored or coauthored 8 books, more than 120 journal articles, and 500 conference papers. He holds seven international patents and organized several tutorials at international conferences. He worked on many projects for the industry concerning wind and wave energy and power electronic applications for power systems.