

Indium as a High-Cooling-Power Nuclear Refrigerant for Quantum Nanoelectronics

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The frontiers of quantum electronics have been linked to the discovery of new refrigeration methods since the discovery of superconductivity at a temperature of around 4 K, enabled by the liquefaction of helium. Since then, advances in cryogenics have led to discoveries such as the quantum Hall effect and new technologies such as superconducting and semiconductor quantum bits. Presently, nanoelectronic devices typically reach electron temperatures of around 10–100 mK by use of commercially available dilution refrigerators. However, cooling electrons via the encompassing lattice vibrations, or phonons, becomes inefficient at low temperatures. Further progress toward lower temperatures requires new cooling methods for electrons on the nanoscale, such as direct cooling with nuclear spins, which themselves can be brought to microkelvin temperatures by adiabatic demagnetization. Here we introduce indium as a nuclear refrigerant for nanoelectronics and demonstrate that solely on-chip cooling of electrons is possible down to 3.2 ± 0.1 mK, limited by the heat leak via the electrical connections of the device.

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Quantum electronics relies on the precise control of electronic states in nanostructures, which is possible if the energy-level separation is much higher than the thermal energy $k_B T$. Access to novel states of matter such as electron-nuclear ferromagnets [1–3], non-Abelian anyons in fractional quantum Hall states [4,5], topological insulators [6], or exotic superconductivity [7–9] requires further progress in the cooling of nanoelectronics, approaching the microkelvin regime.

Typical electron temperatures on the order of 10 mK are accessible in semiconductor and metallic nanostructures by mounting the chip containing the devices on an insulating substrate cooled by commercially available dilution refrigerators. The lowest-achievable electron temperature is limited by the heat transferred from the electrons at a temperature of T_e to phonons at a temperature of T_p . The heat flow between conduction electrons and phonons in a metallic volume V is $\dot{Q}_{ep} = \Sigma V (T_e^5 - T_p^5)$, where Σ is a material-dependent coupling constant on the order of 10^9 W K⁻⁵ m⁻³ [10,11]. A residual electronic heat leak \dot{Q}_{leak} of 10 aW to a well-shielded nanostructure [12] with $V = 1$ μm^3 then yields $T_e \approx 25$ mK even as T_p approaches zero. Increasing the coupling volume V by electrodeposition of thick metal films [13] and by improving thermalization by means of liquid-helium immersion cells led to steady-state

values of $T_e \approx 4$ mK [13–15] in specially built dilution refrigerators.

The key to reduce the electron temperature further thus involves coupling the electron system to a cold bath without the necessity of heat transport via phonons. This can be achieved by nuclear magnetic cooling [16,17]. In the limit of small Zeeman splitting compared with $k_B T_n$, the magnetization of the nuclear spin system is $M \propto B/T_n$ at a magnetic field of B and a temperature of T_n . T_n can be reduced by adiabatically lowering the magnetic field from B_i to B_f . In the absence of an external heat load, M stays constant, and consequently $T_{n,f} = T_{n,i} \times B_f/B_i$ [18–20]. This technique has become the workhorse of ultralow-temperature physics, with the lowest attainable temperature of $T_n \sim 100$ pK [21].

On-chip nuclear magnetic cooling utilizes the spin-lattice relaxation to cool conduction electrons close to the temperature of a cold nuclear spin system that is co-integrated with the electronic device. The heat flow \dot{Q}_{en} is determined by the spin-lattice relaxation time τ_1 [22,23]:

$$\dot{Q}_{en} = \tau_1^{-1} n C_n (T_n - T_n^2/T_e), \quad (1)$$

where C_n is the nuclear heat capacity and n is the molar amount of the nuclei. If the magnetization is weak, the Korringa law $\tau_1 T_e = \kappa$ applies, with the Korringa constant κ , and C_n can be approximated by the Schottky law $C_n = \alpha B^2/T_n^2$, where $\alpha = N_0 I(I+1) \mu_n^2 g_n^2 / 3k_B$, with I being the size of the nuclear spin, g_n the g factor, N_0 the

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Avogadro number, and μ_n the nuclear magneton. In this limit, Eq. (1) reads

$$\dot{Q}_{en} = \alpha n \kappa^{-1} B^2 (T_e/T_n - 1). \quad (2)$$

The choice of nuclear refrigerant for nanoelectronics is based on finding a material with a large C_n , while keeping κ small to have efficient coupling to the electrons. Equation (2) shows that the material-dependent figure of merit α/κ allows us to compare different materials. In addition, the experimental implementation should allow for a large n and $B_i^2/T_{n,i}^2$ ratio for efficient cooling and long cold time.

Thus far, copper (Cu) was the sole material used for the nuclear cooling of nanoelectronics [16,17,24]. Naturally occurring Cu nuclei have a spin of 3/2, yielding $\alpha_{\text{Cu}} = 3.22 \mu\text{J K T}^{-2} \text{mol}^{-1}$ [23]. Bulk-Cu nuclear demagnetization stages benefit from the low magnetic ordering temperature of less than 0.1 μK [25], which allows T_n values in the microkelvin regime [26]. However, the weak electron-nucleus coupling given by $\kappa = 1.2 \text{ K s}$ [22] is a limitation for electron cooling.

To overcome this limit, we use indium (In) as an on-chip nuclear refrigerant. In features a much shorter spin-lattice relaxation time, characterized by $\kappa_{\text{In}} = 0.086 \text{ K s}$ [27], and a large nuclear spin of 9/2, with $\alpha_{\text{In}} = 13.8 \mu\text{J K T}^{-2} \text{mol}^{-1}$ increasing the molar nuclear cooling power by a factor of $(\alpha_{\text{In}}/\kappa_{\text{In}})/(\alpha_{\text{Cu}}/\kappa_{\text{Cu}}) = 60$ compared with Cu. The lowest attainable T_n for In is limited by the tetragonal crystal-field splitting of 250 μK [28].

In addition, the external magnetic field has to be kept above $B_c = 28 \text{ mT}$ to avoid the thermal decoupling of electrons by the superconducting phase transition [29].

To demonstrate the applicability of In as a refrigerant for scalable nanoelectronics, we directly measure T_e in a nanoelectronic device while ramping B to perform the nuclear demagnetization. While primary electron thermometry in the millikelvin regime has been realized in several ways [10,30–32], we use Coulomb-blockade thermometry due to its lack of sensitivity to a change in the magnetic field [33]. Coulomb-blockade thermometers (CBTs) rely on the universal temperature dependence of single charge localization in mesoscopic metallic islands [34] and have been proposed to provide the reference scale for millikelvin-range thermometry [35].

We integrate a nanofabricated CBT with In cooling blocks to directly cool the electrons inside the device (Fig. 1). The geometrical and electrical parameters of the thermometer are shown in Fig. 1(a). The islands are formed within the stripe of $N = 36$ tunnel junctions, and each has a total capacitance $C_\Sigma = 2C + C_0$, which determines its effective charging energy $E_C = e^2/C_\Sigma \times (N - 1)/N$, where e is the elementary charge. The zero-bias conductance of the device, $G(V = 0)$ decreases by [34,36]:

$$\Delta G/G_t = u_N/6 - u_N^2/60 + u_N^3/630 - \dots, \quad (3)$$

where $u_N = E_C/k_B T_e$. Notably, the width of the conductance dip depends only on N and $k_B T_e$, $eV_{1/2}/k_B T = 5.44N$ enabling primary thermometry without prior cali-

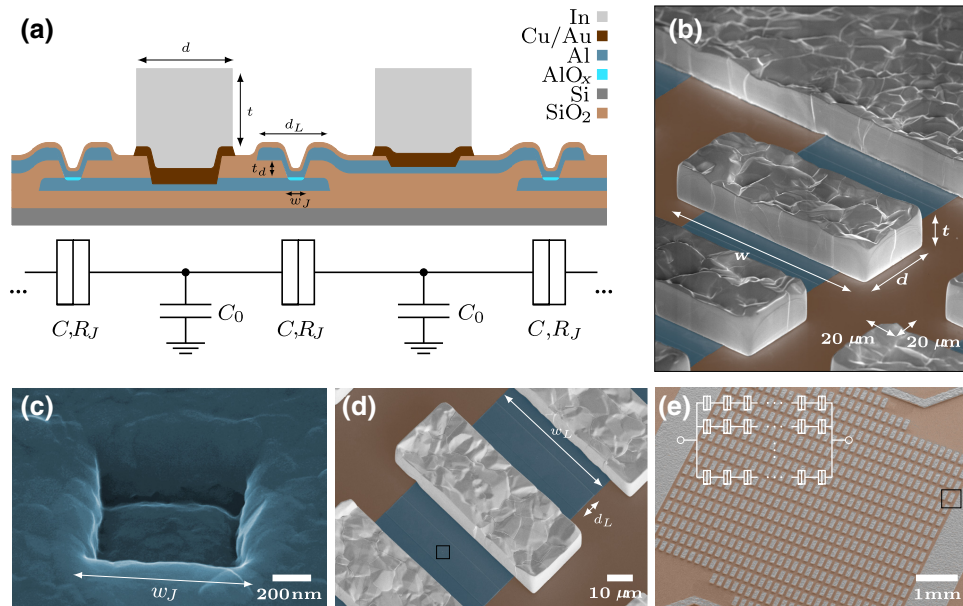


FIG. 1. (a) Cross section of the metallic islands and the Al-AIO_x-Al tunnel junctions with a resistance of R_J . The capacitance C is set by the overlap area $d_L \times w_L$, C_0 is the stray capacitance. The electrons are cooled by the electrodeposited In blocks. (b) False-color scanning electron micrograph of a single In fin. (c) A single tunnel junction between adjacent islands (d). The black square in (d) depicts the area in (c). (e) Overview of the full array with 35×15 islands. The black square depicts the area in (b).

bration [37]. We set E_C by the overlap area between adjacent islands, which is independent of the tunnel-junction area determining the junction resistance.

This flexibility in design is enabled by creating the Al-AIO_x-Al tunnel junctions *ex situ* in vias through the interlayer dielectric [Fig. 1(c)] [38]. The junction area is $w_j^2 = 0.55 \pm 0.1 \mu\text{m}^2$, with a tunnel resistivity of $12.8 \pm 0.8 \text{ k}\Omega \mu\text{m}^2$ at room temperature, close to previously reported values [38], yielding a total device resistance $1/G_t = 55.8 \text{ k}\Omega$ in an array of $N \times M = 36 \times 15$ junctions. The device resistance is temperature dependent and saturates at $89 \text{ k}\Omega$ below $T = 1 \text{ K}$ owing to the finite barrier height of the AIO_x insulating layer [39].

The CBT device used in this work is designed with an island overlap area of $w_L \times d_L = 18 \times 100 \mu\text{m}^2$ and a SiO₂ interlayer dielectric with thickness $t_d = 230 \text{ nm}$ [Fig. 1(d)]. A parallel-plate-capacitor model $C = \epsilon_0 \epsilon_r A/d$ using $\epsilon_r = 3.5\text{--}3.9$ for sputtered SiO₂ [40] gives an estimated capacitance in the range of $C_\Sigma = 485\text{--}540 \text{ fF}$, corresponding to the CBT working as a primary thermometer between approximately 1.5 and 250 mK. This range is limited by uneven charge distribution on the low side [36] and instrumental resolution on the high side.

The nuclear-magnetic-cooling functionality is integrated by electroplating an In block with a volume of $50 \times 140 \times 25.4(1) \mu\text{m}^3$ through a thick photoresist mask onto each island [Fig. 1(b)]. We achieve an In integration density of $1.6 \text{ pmol}/\mu\text{m}^2$. This figure determines the nuclear cooling power \dot{Q}_{en} [see Eq. (2)] per unit area. Electroplating with a constant current results in extensive crystallization and hydrogen formation, which decreases the density of the films and affects the patterning resolution. Therefore we apply forward-current and reverse-current pulses to the electrochemical cell to refine the grain structure and reach a patterning resolution of $1 \mu\text{m}$ [41].

The device is mounted on a Cu carrier block inside an rf-tight enclosure cooled by an unmodified commercial wet dilution refrigerator. The mixing-chamber temperature is measured by a calibrated cerium magnesium nitrate (CMN) thermometer, and the base temperature is found to be approximately 5 mK. The scheme of the measurement setup is shown in Fig. 2(b). The CBT is attached in a four-wire geometry, with the twisted pairs of the electrical wiring passing through a Cu powder [42] and a discrete-component third-order RC low-pass filter, which has a cutoff frequency of 50 kHz to reduce external noise. The differential conductance $G(V)$ of the CBT is measured by standard low-frequency (18.31 Hz) lock-in techniques as a function of the dc voltage bias, V .

First we determine E_C by simultaneously fitting a set of $G(V)$ curves against the full single-electron-tunneling model [34] at different T_{CMN} values set by heating the mixing chamber [Fig. 2(a)]. We find $C_\Sigma = 479 \pm 2 \text{ fF}$, close to the designed value, yielding $E_C = 330 \text{ neV}$. The measured electron temperature T_{CBT} agrees well with T_{CMN} for

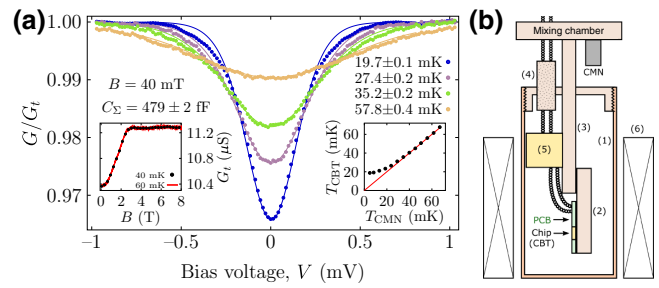


FIG. 2. (a) Normalized differential conductance G/G_t as a function of the voltage bias V at different temperatures, with the solid lines showing the best fit determining the measured electron temperature T_{CBT} and the island capacitance $C_\Sigma = 479 \pm 2 \text{ fF}$; see the text. Right inset: T_{CBT} as a function of the dilution refrigerator temperature T_{CMN} , showing a saturated $T_{\text{CBT}} \approx 20 \text{ mK}$. These measurements are taken with an applied magnetic field $B = 40 \text{ mT}$. Left inset: the change of G_t with magnetic field at two different temperatures. (b) The cryogenic setup used in the experiment. The CBT chip is mounted on a Cu plate (2) attached to the mixing chamber of the dilution refrigerator by a Cu coldfinger (3). The sample is well shielded from electromagnetic noise by an rf-tight enclosure (1), Cu-powder filters (4), and resistive low-pass filters (5). The magnetic field is applied by a superconducting solenoid (6).

temperatures above 30 mK, but decouples and saturates for lower values, demonstrating the inefficiency of phonon cooling via the device substrate [right inset in Fig. 2(a)]. The device exhibits a slightly- B -dependent G_t [left inset in Fig. 2(a)]. This magnetoresistance is, however, independent of the device temperature below 100 mK and therefore can be accounted for during the demagnetization cycles. The established calibration of the CBT enables its use in a secondary mode of operation, by measurement of the zero-bias conductance decrease and finding T_{CBT} on the basis of Eq. (3). This mode avoids additional Joule heating at finite bias voltages and allows real-time temperature sampling while the magnetic field is being ramped.

To perform the nuclear demagnetization experiment, we first set the initial field B_i and let the CBT thermalize while the heat released by nuclear spin magnetization is absorbed by the dilution refrigerator. We typically find $T_{\text{CBT}} \approx 20 \text{ mK}$ after 24 h and $T_{\text{CBT}} \approx 16 \text{ mK}$ after 72 h of precooling at $B_i = 12.8 \text{ T}$. Then we reduce the field to $B_f < B_i$ with a constant rate \dot{B} while measuring the zero-bias conductance $G(V = 0)$ of the CBT. We continuously track the conductance minimum in a dynamic bias window of $\approx 20 \mu\text{V}$ to compensate for voltage-bias drifts over the several hours' timescale of the experiment. The voltage-bias window is continuously updated following the zero-bias point, which is determined by the measurement software on the basis of the nonlinear $G(V)$ curve.

A typical experimental run starting from $B_i = 12.8 \text{ T}$ is shown in Fig. 3(a). We set a magnetic field ramp rate $\dot{B} = -0.4 \text{ mT/s}$ and a final field $B_f = 40 \text{ mT}$. The strong

electron-nucleus coupling results in a reduction of the electron temperature T_{CBT} from its initial value of 16 mK, while $T_{\text{CMN}} \approx 5$ mK remains essentially constant. During the demagnetization cycle, we measure the curvature of the Coulomb-blockade peak and find excellent agreement with the model calculations based on the already inferred E_C for each temperature data point with no additional fit parameters [Fig. 3(b)]. This analysis confirms the primary nature of our CBT throughout the entire temperature range of the experiment.

Here we find an electron temperature $T_e = 3.2 \pm 0.1$ mK after on-chip demagnetization, with previously reported values reaching $T_e = 4.7$ mK with Cu as the nuclear refrigerant [17]. We also demonstrate superior performance compared with phonon-cooled devices, where steady-state values above $T_e = 3.9$ mK were measured in a custom-built dilution refrigerator [13].

On reaching the lowest temperature at $B \approx 2$ T, the stage warms up quickly, and after the field ramp stops at $B_f = 40$ mT, it relaxes to the starting temperature. This behavior indicates that the nuclear heat capacity is depleted by parasitic heat leaks before the field ramp is finished.

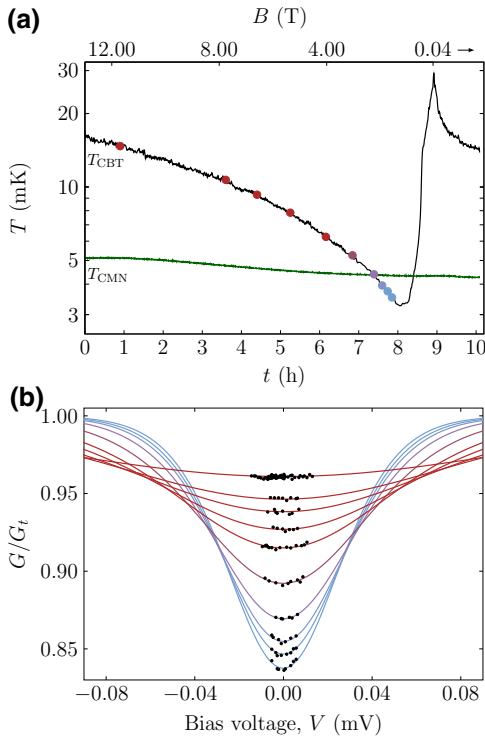


FIG. 3. (a) Electron temperature T_{CBT} and refrigerator temperature T_{CMN} as the field is reduced from 12.8 T (initial value 16 mK) to 40 mT at $\dot{B} = -0.4$ mT/s, including a 1-h thermal-relaxation period at the end. $T_{\text{CBT}} < T_{\text{CMN}}$ is clearly obtained. (b) The normalized conductance at small voltage biases (black dots) at different temperatures confirms the expected zero-bias curvature; see the text. The position of each curve is shown by a dot of the corresponding color in (a).

We analyze the cooling performance and heat leaks of our device by performing demagnetization runs at different \dot{B} between -0.3 and -6 mT/s [Fig. 4(a)]. All data exhibit a similar behavior with a minimum temperature well below $T_{\text{CMN}} \approx 5$ mK. To determine the heat input by parasitic heating, we numerically model the time evolution of T_n and T_e on a single island. We ignore the weak thermal coupling to phonons and assume that the heat flow between the electrons and nuclei is described by Eq. (1). We consider the Hamiltonian of the nuclear spin where the interaction of the nuclear quadrupole moment with the crystal-field gradient is included with $e^2qQ = -198$ neV in a direction Θ with respect to a large external magnetic field B [28]:

$$\mathbf{H} = -\gamma B \mathbf{I}_z + \frac{e^2qQ}{4I(2I-1)} \frac{3 \cos^2 \Theta - 1}{2} (3\mathbf{I}_z^2 - \mathbf{I}^2). \quad (4)$$

The set of eigenvalues ε_m are averaged over Θ and define the partition sum $Z = \sum \exp(-\varepsilon_m/k_B T_n)$, which yields the nuclear spin entropy $S_n = k_B \partial(T_n \log Z)/\partial T_n$ and the heat capacity $C_n = T_n(\partial S_n/\partial T_n)_B$. The time evolution of the temperatures then follows:

$$\begin{aligned} \frac{dT_n}{dt} &= \frac{T_e T_n - T_n^2}{\kappa} + \frac{\partial T_n}{\partial B} \dot{B}, \\ \frac{dT_e}{dt} &= -\frac{C_n}{C_e} \left(\frac{T_e T_n - T_n^2}{\kappa} \right) + \frac{\dot{Q}_{\text{leak}}}{nC_e}. \end{aligned} \quad (5)$$

The heat capacity of the electron system is assumed to follow the Sommerfeld rule, $C_e = \gamma T_e$, and we include a parasitic heat leak \dot{Q}_{leak} as a free parameter. Evaluating the experimental data in Fig. 4(a), we plot $\dot{Q}_{\text{leak}}(B)$ in the upper inset in Fig. 4(a) and find the same behavior independent of \dot{B} with a linear increase at high fields and a rapid upturn below 2 T. We evaluate the linear segment and find that the dissipation \dot{Q}_{leak} changes linearly with \dot{B} (lower inset in Fig. 4), $\dot{Q}_{\text{leak}} = a|\dot{B}| + \dot{Q}_0$, with $a = 18$ fW s/mT and $\dot{Q}_0 = 0.18$ fW per island. Notably, the largest measured heat leak per island is 108 fW, similar to earlier reported values in similar experiments [17], but much higher than figures for combined on-chip and off-chip refrigeration [16,44].

The linear $\dot{Q}_{\text{leak}}(\dot{B})$ is in striking contrast with observations on macroscopically large nuclear cooling stages, where eddy currents in the bulk refrigerant lead to $\dot{Q}_{\text{leak}} \propto \dot{B}^2$ [23]. It is also inconsistent with a dominating static heat leak yielding a constant \dot{Q}_{leak} , or with an environmental coupling of $\dot{Q}_{\text{leak}} \propto T_e^n - T_{\text{env}}^n$. This confirms that the metallic islands of the CBT are thermally well decoupled from the environment; however, the rate-independent \dot{Q}_{leak} suggests the presence of a well-coupled thermal mass consuming the In nuclear heat capacity over the timescale of the experiment.

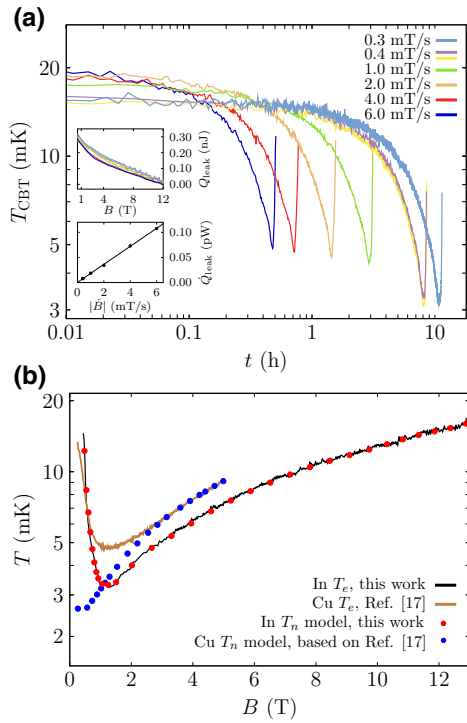


FIG. 4. (a) T_{CBT} as a function of time for various magnetic field ramp rates \dot{B} . Two distinct runs with $\dot{B} = -0.4$ mT/s are shown to demonstrate the reproducibility of the data. The lower inset shows the extracted heat leak \dot{Q}_{leak} per island (black dots) and a linear fit (solid line). The upper inset demonstrates that the total absorbed heat \dot{Q}_{leak} per island collapses onto a single curve for all runs; see the text. (b) Comparison between on-chip demagnetization performed in the work reported in Ref. [17] with Cu (raw data retrieved from Ref. [43]) and our experiment using In with $\dot{B} = -0.4$ mT/s. The T_e values (solid lines) are measured data, whereas T_n (dots) is calculated with Eq. (5).

We evaluate the performance of electroplated In as an on-chip electron refrigerant by considering the nuclear heat capacity integrated per unit area, $\alpha' = \alpha n/A$, and use α'/κ as a figure of merit. Our device features $\alpha'/\kappa_{\text{In}} = 250 \mu\text{W}/\text{m}^2 \text{K T}^2$, to be compared with $0.076 \mu\text{W}/\text{m}^2 \text{K T}^2$ [16] and $2.33 \mu\text{W}/\text{m}^2 \text{K T}^2$ [17] achieved with Cu.

We benchmark our implementation by comparing our data with the results reported in Ref. [17]. The measured T_e and the calculated T_n are plotted in Fig. 4(b). Our simulations based on Eq. (5) confirm that the In nuclei are strongly coupled to the electron system, resulting in $T_n = T_e$ throughout the entire experiment with $\dot{B} = -0.4$ mT/s, resulting in $\dot{Q}_{\text{leak}} = 7.85$ fW per island. In contrast, the weaker hyperfine coupling of Cu results in a deviation between T_n and T_e despite a similar heat leak $\dot{Q}_{\text{leak}} = 6.3$ fW per island [17], demonstrating the limitations of Cu as an on-chip refrigerant.

In conclusion, we demonstrate that electron temperatures of 3.2 ± 0.1 mK can be reached by nuclear magnetic

cooling on-chip with In as a nuclear refrigerant, a result that is the coldest measured electron temperature without additional off-chip nuclear demagnetization cooling. We therefore conclude that on-chip integrated nuclear refrigeration using In is a versatile means to decrease the electron temperature of nanoscale devices.

Raw datasets are available at the 4TU.Centre for Research Data repository [45].

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