Influence of the metal inter-layer on resistive random access memory forming voltage

by

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to obtain the degree of Master of Science at the Delft University of Technology

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Abstract

Neuromorphic computing, a novel computing configuration inspired by the brain, aims to perform calculations based on physical neurons and synapses, attracting significant attention in recent years. Resistive random access memory (RRAM) shows great potential in this field, demonstrating high operation speed, nanoscale scalability, long retention time, non-volatile performance, and a simple structure.

Despite the promising performance of RRAM, a high forming voltage potentially hinders the widespread application of the device. This thesis aims to diminish and eliminate the forming voltage. To achieve this, different metals were inserted between the insulator layer and the bottom electrode of the RRAM, serving as an interface metal layer. The interface metal was expected to introduce oxygen vacancies to the insulator, thereby decreasing the forming voltage. Advanced nanofabrication processes were employed in the cleanroom, and a related recipe was developed. The influence of layer thickness and device area was also studied to gain a comprehensive understanding. Among all the samples, Ru-based devices were observed to be forming-free.

Data analysis methods were applied to model the data, with the random forest method found to be the most suitable, achieving an accuracy of 82.4%. The model was verified by measurements of 10 nm Ru-based devices. Feature importance was then calculated to interpret the model. The four most important features determining the forming voltage are the thickness, standard electrode potential, area, and work function of the interface metal. This work adopts a new approach to eliminating the forming voltage, not only providing a forming-free device but also offering a guideline for future research on forming voltage.

Acknowledgements

I would like to express my deepest gratitude to all those who have supported and guided me throughout the completion of this thesis.

First and foremost, I wish to thank my supervisors, Prof. Dr. M.H.F. Sluiter and Prof. Dr. Ryoichi Ishihara, for their invaluable guidance and support throughout this thesis. Their feedback and instruction were instrumental in its successful completion. I also extend my thanks to my mentor, Mr. Erbing Hua, who significantly assisted me with the lab work and presentation preparation.

I am also grateful to the members of my thesis committee, Prof. Dr. S. (Sid) Kumar and Prof. Dr. ir. S. (Sten) Vollebregt, for their kind attendance at my defense. My sincere thanks go to Prof. Dr. S. (Sid) Kumar again for his excellent teaching and warm encouragement during my master's studies.

I would like to thank Hampus Hoffman for his insightful discussions and advice on my presentation and experiments. My sincere thanks also go to Saskia van der Meer, who assisted me with the graduation procedures, Drs. R.M. Huizenga, who helped me with the XRD measurements, and Haowei Jiang, who supported me during the SEM measurements.

I would like to thank my family and friends. Without their unwavering support, I could not have successfully completed my master's studies.

Finally, I want to thank everyone who has helped me during my Master's.

Jiaze Li

Delft, June 2024

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Nomenclature

Abbreviations

Abbreviation	Definition
AI	Artificial intelligence
ALU	Arithmetic logic unit
ANN	Artificial neural network
CBRAM	Conductive bridge random access memory
CF	Conductive filament
CIM	Computing in memory
CMOS	Complementary metal–oxide–semiconductor
CRS	Complementary resistive switching
DNN	Deep neural network
DRAM	Dynamic random access memory
eBRS	Electronic bipolar resistance switching
ECM	Electrochemical metallization
EDS	Energy-dispersive X-ray spectroscopy
FeFET	Ferroelectric field effect transistor
GPU	Graphics processing unit
HRS	High-resistance state
IMC	In memory computing
LRS	Low-resistance state
MAC	Multiply-accumulate

Abbreviation	Definition
MIM	Metal–insulator–metal
MRAM	Magnetic random access memory
MVM	Matrix-vector multiplication
NN	Neural network
NVM	Non-volatile memory
OxRAM	Oxide-based random access memory
PCA	Principal component analysis
PCM	Phase change memory
RF	Random forest
RNN	Recurrent neural network
RRAM or ReRAM	Resistive random access memory
SCLC	Space charge limited conduction
SEM	Scanning electron microscopy
SNN	Spiking neural network
SRAM	Static random access memory
TPU	Tensor processing unit
VCM	Valence change memory
XRD	X-ray diffraction

1

Introduction

1.1. Research motivation

Semiconductor materials, being among the most important functional materials in today's society, significantly shape our daily lives. The unexpected rapid growth of information technology, along with electrical and electronics engineering, has created a demanding need for advanced devices. The ever-evolving information technology system has revolutionized computers, smartphones, automobiles, and more, leading to numerous achievements. However, this system has also become incredibly complex, integrating hardware, software, data storage, and connectivity within products [1].

Conventional computers adopt the Von Neumann architecture, in which memory units and computing/processing units are physically separate, requiring data transfer between the processor and memory (Fig. 1.1). This architecture consumes energy and introduces latency to the system [1], [2], a phenomenon known as the "Von Neumann Bottleneck" [3], [4]. This bottleneck has become an

unignorable problem in the face of today's large data and high-speed tasks.

Facing the aforementioned problems, neuromorphic computing has been proposed. The concept is inspired by the human brain (Fig. 1.1), which improves energy efficiency and reduces latency while enhancing parallelism [5], [6].

It is important to note that although conventional Von Neumann computers may perform calculations faster and with higher accuracy, human brains are far superior in terms of energy efficiency. For example, AlphaGo, a Google-developed computer that defeated one of the best human players in the game of Go, consumes tens of thousands of times more energy than the human player to accomplish the task [5].

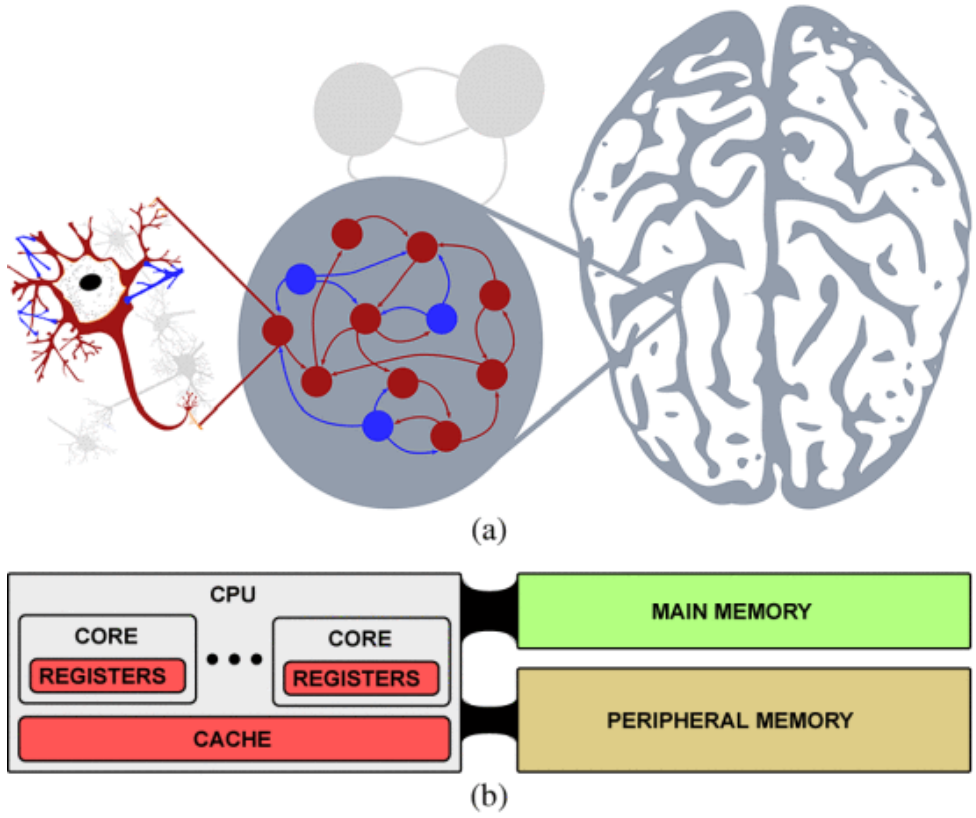


Figure 1.1: A Comparison between Human Brain and Computer [7]. (a) Human brain architecture. (b) Conventional computer architecture.

Considering all the discussed hardware architectures for neuromorphic computing, in-memory computing (IMC), also referred to as computing in memory (CIM), is one of the most promising candidates [8]. Its core principle is computing in situ, meaning computation tasks are performed within the memory unit [9]. By

integrating the functions of the memory and computing units, IMC reduces or even eliminates the energy consumption associated with data transfer. Furthermore, the diminished physical gap between the memory and processor, known as the memory wall [10], [11], significantly improves system performance in terms of latency [11], [12].

In spite of the strengths of the new architecture, IMC requires advanced memory devices that can store information and perform computing simultaneously. Memory is the heart of IMC. Unfortunately, the most well-developed complementary metal–oxide–semiconductor (CMOS) memory devices to date are not deemed suitable for neuromorphic computing applications. For instance, both static random access memory (SRAM) and dynamic random access memory (DRAM) are types of volatile memory, which fail to retain training data once power is discontinued. NOR flash memory exhibits relatively low density [13], while NAND flash memory features a highly condensed string structure that complicates its integration into neuromorphic computing [14]. An overview can be seen in the following Table 1.1.

Table 1.1: CMOS-based memory limitations in IMC

Type of Memory	Limitations
SRAM	Volatile and large cell size
DRAM	Volatile
NOR Flash	Low density
NAND Flash	Complicated to integrate

Based on this, an alternative form of memory has emerged beyond conventional charge-based memory, distinguished by its switchable resistance that encodes information. This type of memory represents information based on its resistance states and can be termed 'memristive devices' in accordance with the definition in memristive systems [15]. Some examples of memristive devices include phase change memory (PCM) [16], magnetic random-access memory (MRAM), and

ferroelectric field-effect transistors (FeFET) [17]. Among all memristive devices, resistive random access memory (RRAM or ReRAM), sometimes referred to as a memristor, is particularly attractive due to its simple structure, outstanding scalability, fast operation speed, long retention time, and high compatibility with the modern CMOS industry.

However, despite these advantages, there is still a considerable distance to traverse before RRAM can be applied on a mass scale. Among all the efforts to improve device stability, eliminating electroforming is an important approach. Typically, a high voltage is applied to the device initially to enable resistive switching ('2-forming' in Fig. 1.2) [18]. The presence of high voltage forming is unfavorable for circuit design, as it may damage the RRAM device and degrade its lifetime [19]. The high forming voltage is also incompatible with advanced CMOS technology nodes [20]. Therefore, developing a device that can operate without forming (referred to as forming-free) becomes essential [21], [22].

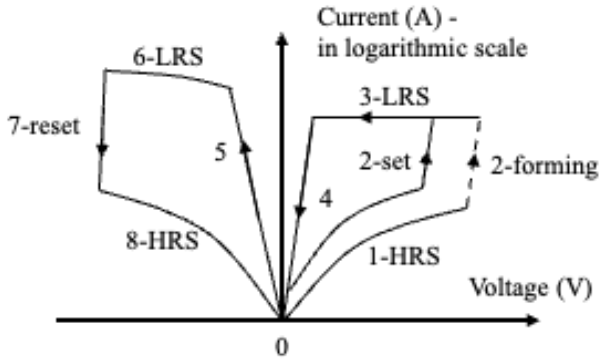


Figure 1.2: I-V curve for a typical RRAM device.

1.2. Problem to solve

The RRAM typically has a metal–insulator–metal (MIM) structure (Fig. 1.3), where the resistance of the insulator can be manipulated by the electric input to perform information storage. The two metal layers act as the top electrode and bottom electrode. Due to its vital role, much attention has been drawn to the insulator layer [23]. Various models [24]–[26] have been established to describe the RRAM

working process.

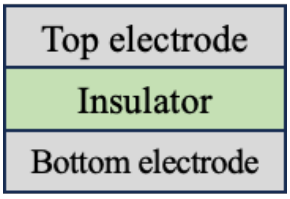


Figure 1.3: Metal-insulator-metal RRAM structure.

Among all the insulators, HfO_2 offers the advantages of a high dielectric constant, wide band gap, and compatibility with the modern CMOS industry [27], [28], making it one of the most researched materials for RRAM.

To achieve forming-free operation in HfO_2-based devices, one method is to prepare multi-layer devices. For instance, a tri-layer RRAM has been fabricated to achieve forming-free operation, with its mode of operation identified as bulk switching [20]. $HfO_x/TiO_x/HfO_x/TiO_x$ multi-layer devices have also been observed to be forming-free, where the titanium-rich layer may induce oxygen vacancies in the device, facilitating the formation of a conductive path in the material [29].

Another approach to lowering the forming voltage towards forming-free operation is decreasing the insulator thickness (Fig. 1.4). It has been confirmed that reducing the thickness of the insulator may lead to a lower forming voltage, with forming-free operation observed at 3 nm HfO_2 [30].

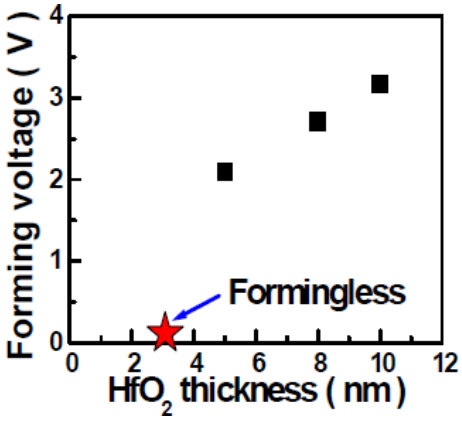


Figure 1.4: Forming voltage versus HfO_2 thickness for the $TiN/TiO_x/HfO_x/TiN$ device [30].

However, the multi-layer device is complicated to fabricate, and the tri-layer or even quad-layer structure also increases fabrication costs. On the other hand, RRAM devices with very thin insulators exhibit limited stability [31], while devices with higher HfO_2 thickness, such as 5 nm HfO_2, require a forming process at approximately 2V (Fig. 1.4) [30]. Fabricating an RRAM device with a simplified structure and higher HfO_2 thickness remains a challenge.

1.3. Project content

It is understood that the bottom electrode plays an important role in manipulating the forming voltage [32]. The bottom electrode may introduce oxygen vacancies, which facilitate the forming process. Additionally, the bottom electrode can determine the interface barrier. For example, tungsten has been confirmed to achieve forming-free operation by lowering the oxide-metal interface barrier [33].

Based on the aforementioned research, a special metal interlayer, termed the 'bottom metal' layer, is implanted beneath the insulator in this project. Specifically, a 5 nm HfO_2 layer is deposited as the insulator. Both the top and bottom electrodes are composed of 30 nm platinum, a widely reported electrode material used in RRAM applications [34]. Six different metals are used as the bottom metal: gold, ruthenium, nickel, niobium, tantalum, and titanium. The control group consists of devices without the bottom metal, where the 30 nm platinum bottom electrode directly contacts the insulator. Additionally, a 5 nm titanium layer is added on top of the insulator layer to introduce oxygen vacancies from the top. The device structure is illustrated in Fig. 1.5.

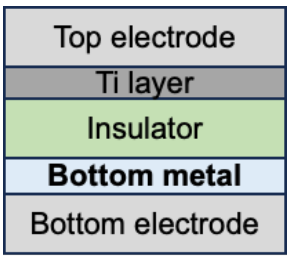


Figure 1.5: Implantation of an additional bottom metal layer.

The six experimental bottom metals can be roughly divided into two groups based on their standard electrode potential, which describes how easily the metal can be oxidized, thus evaluating the chemical activity of the metal. Gold and ruthenium are categorized as inert metals, while the other four metals are expected to have moderate to high chemical activity. It is expected that active metal interlayers under the HfO_2 may be oxidized and absorb the oxygen from HfO_2, introducing oxygen vacancies into the insulator. This will also modify the interface barrier. Thus, the inserted metal layer assists the forming process and lowers the forming voltage.

It is important to note that the chemical activity of metals can be assessed from various aspects, and the standard electrode potential is merely one method rather than the only method to interpret metal activity. Many factors together determine the properties of a metal. For example, although tantalum appears active based on its standard electrode potential, it is, in fact, inert and stable in reality because it forms a thin layer of tantalum pentoxide as a protective layer.

By varying the metal species, layer thicknesses, and device areas, multiple factors that may affect the device forming are investigated. The thickness of the bottom metal is expected to determine the amount of oxygen vacancies introduced into the insulator, while the metal's chemical activity indicates how easily the oxygen vacancies can be produced. A prediction of the possible understanding of the method by which the bottom metal determines the forming voltage is summarized in Table 1.2.

Table 1.2: Predicted parameters of the bottom metal that may affect the forming voltage

Factor	Influence
Chemical activity	Introduction of oxygen vacancies into the insulator
Work function	Modification of the interface barrier
Layer thickness	Amount of oxygen vacancies implanted
Device area	Number of spots for forming CF

All devices in this project are personally handmade and measured in the cleanroom. Machine learning is employed to uncover the intrinsic relationships between distinct factors.

1.4. Influence of interlayer on other aspects

It is worth mentioning that, apart from the forming voltage, interlayer metal insertion has been found to change device performance in many other aspects. Ismail et al. [35] added an aluminum layer in the middle of the CeO_2 insulator layer (Fig. 1.6a), improving the device's lifetime and operating voltage. TiN was inserted between the top electrode and the insulator (Fig. 1.6b), acting as a barrier layer to stabilize device operation and prevent failure [36]. Additionally, MoO_x was developed as an oxygen buffer layer (Fig. 1.6c) to improve device retention [37]. Furthermore, a titanium capping layer (Fig. 1.6d) was found to improve the device's linearity [38], [39]. Hence, the application of the 'bottom metal' interlayer may not only modify the forming voltage but also influence a wide range of other aspects.

Notably, many of the interlayers are inserted between the top electrode and the insulator (Fig. 1.6), while the study of the interlayer at the bottom electrode-insulator interface is much less common [32], [40]. Investigating the interlayer at the bottom electrode-insulator interface may not only enhance our understanding of how metal influences the RRAM forming voltage but also provide an approach to improve RRAM devices.

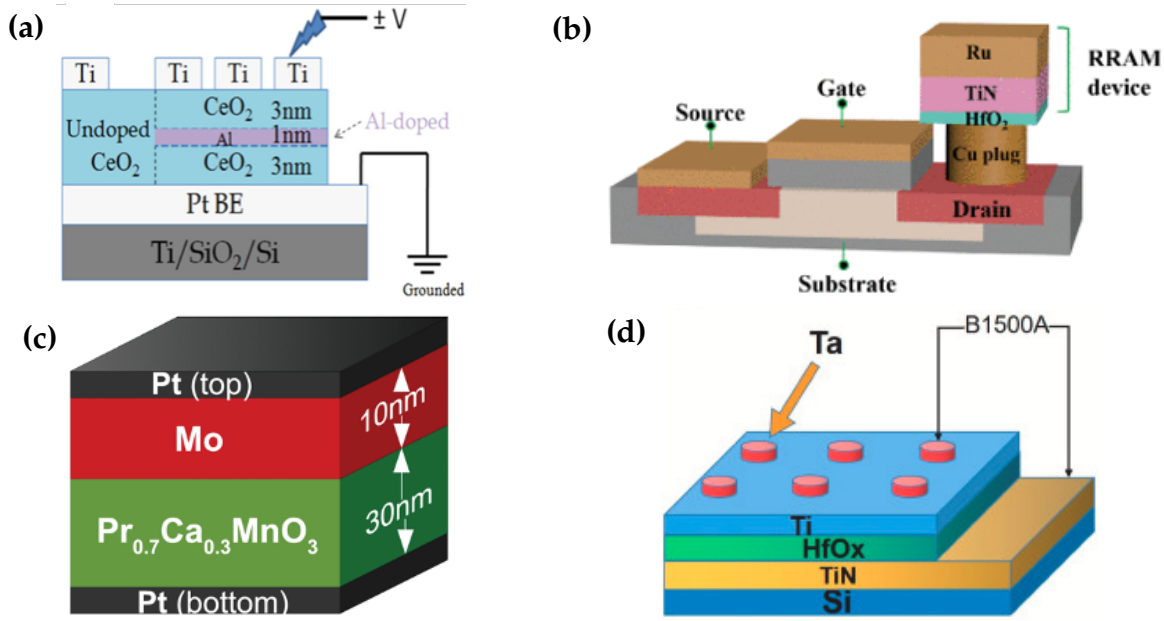


Figure 1.6: interlayer insertion in RRAM devices. (a) Al interlayer in the RRAM device [35]. (b) TiN interlayer in between the top electrode and insulator [36]. (c) MoO_x interlayer as barrier layer [37]. (d) Ti interlayer as capping layer [39].

1.5. Thesis structure

This thesis is structured as follows:

- Chapter 2 introduces the background of neuromorphic computing and RRAM devices.
- Chapter 3 details the fabrication steps undertaken to prepare RRAM devices in the cleanroom.
- Chapter 4 outlines the measurement process and offers a brief interpretation of the results.
- Chapter 5 discusses the application of machine learning analysis.
- Chapter 6 presents the conclusion and future outlook.

2

Background Study

This chapter introduces the background of neuromorphic computing and RRAM devices. The first part explains why we study RRAM, and the second section details what RRAM is.

2.1. Von Neumann architecture

The Von Neumann architecture is widely adopted for today's computing systems, where the memory units and processing units are physically separated (Fig. 2.1). This design endows modern computers with high versatility, making them useful in our daily lives for handling various kinds of tasks [41]. However, with the advent of the 'big data era,' the amount of information that computers need to process is increasing rapidly [42], making the latency induced by data transfer between the memory and processor a serious problem. Additionally, contemporary computers place significant emphasis on the processor, demonstrating a processor-centric nature, which can be at odds with the prevailing trend of a data-centric approach

[5], [12], [43]. A mismatch between the speed of the processor and the speed of the memory (mostly DRAM) is observed, known as the 'memory wall' [10], which limits the overall performance of computers. Energy consumption is another issue. A significant amount of energy is dissipated in moving data rather than in computation itself [11], [44], increasing the demand for cooling systems.

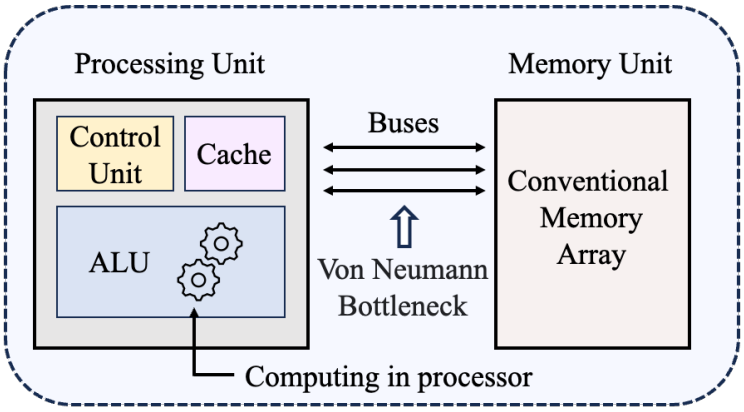


Figure 2.1: A conventional Von Neumann computing system structure, where 'ALU' stands for arithmetic logic unit.

Efforts have been made to solve the problem. The graphics processing unit (GPU), for instance, connects several cores with the memory, improving parallelism [45]. Units dedicated to specific computing tasks, such as the tensor processing unit (TPU) for accelerating multiply-accumulate (MAC) operations, have also been designed [46]. Nonetheless, re-engineering within the Von Neumann system is unlikely to thoroughly address the challenges.

2.2. In memory computing

Compared with modern computers, biological nervous systems may process information more energy-efficiently [7]. Unlike a Von Neumann computer with separate memory and processing units, biological systems perform data computation within the synapses and neurons, which are also the fundamental elements for information storage.

Inspired by the brain, a new approach called neuromorphic computing has been proposed. Instead of attempting to 'improve' conventional systems, neuromorphic

computers adopt a non-Von Neumann architecture. In-memory computing (IMC) is one of the widely accepted hardware structures for neuromorphic systems [47]–[49], where the basic components are essentially memory devices. Mimicking biological systems, IMC integrates processing and storage functions in one unit [11], [50], allowing computational tasks to be completed within memory arrays. Compared to another concept, near-memory computing, where processing is carried out close to the memory, IMC completes computational tasks within the memory unit without the need to read back the content [9]. An illustration of IMC is shown in Fig. 2.2.

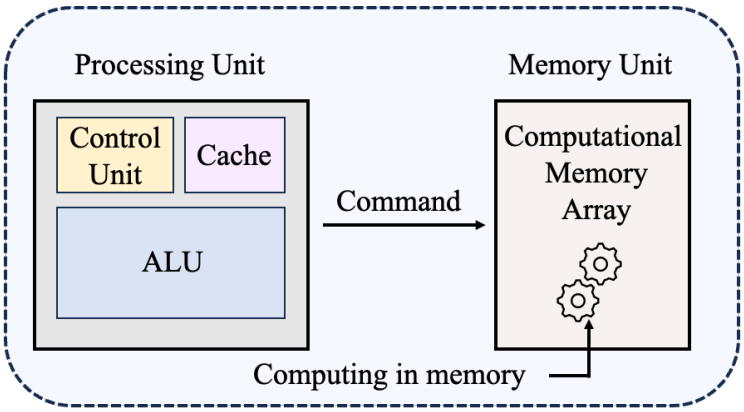


Figure 2.2: In-memory computing architecture. Note that computational tasks are completed within memory arrays.

IMC offers several advantages. By conducting calculations within memory, IMC eliminates the gap between the processor and memory, thereby reducing latency and energy consumption. Additionally, it significantly increases parallelism by performing calculations within the dense array of memory devices [2], [9], [12]. The unique design of IMC provides strengths in operations such as multiply-accumulate (MAC) and matrix-vector multiplication (MVM) [12], [51], [52], which enhances its application in artificial intelligence (AI), particularly in the area of machine learning [53], [54].

The key to "brain learning" is widely believed to be the updating of the connection strength between neurons, also referred to as the "weight" of the synapse. This feature is imitated by artificial systems and becomes the core of

machine learning [55]. To achieve this, non-volatile memory (NVM) devices are specially arranged to form crossbar arrays. In this architecture, input and output lines are arranged perpendicularly, connected by a memristor at each node, whose conductances are programmable. These memristors act as synaptic devices, with their resistance representing the "weight" concept in biological synapses. This architecture enables optimization on a hardware basis and offers a potential solution to accelerate machine learning (Fig. 2.3), though it comes at the cost of losing the generality provided by conventional computing systems.

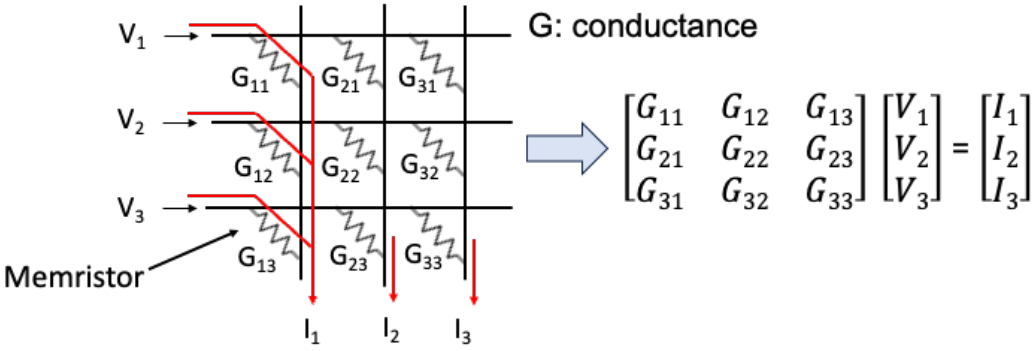


Figure 2.3: An illustration of crossbar performs MVM operation.

The property of changing the weight of the synapses to fit the learning task is known as synaptic plasticity [55]. This efficient MVM operation can be extremely attractive for offline machine learning. The use of NVMs ensures that once training is completed, the model can operate independently for the assigned task, while the specially designed crossbar arrays optimize the calculation from the very bottom hardware level.

As the heart of IMC, memories are expected to demonstrate fast operation speeds, low working voltages, low power consumption, high on/off ratios, and other characteristics. The RRAM device is one of the most promising candidates that fulfill these requirements and is thus selected as the research objective of this project. The device utilizes Ohm's law and Kirchhoff's law to execute calculations within IMC, greatly facilitating the training of neuromorphic models [56], offering a bright future.

2.3. RRAM design and operation

Resistive random access memory (RRAM), offering advantages such as a simple structure, high compatibility with CMOS manufacturing, outstanding scalability, long retention time, low power consumption, and fast operation speed [1], [34], [57], is now one of the most heavily studied non-volatile devices. These benefits make RRAM a strong candidate for neuromorphic computing, with relevant demonstrations seen in [58] and [59].

The structure of a typical RRAM device is metal-insulator-metal (MIM), where the insulator layer provides the switching function. A bird's-eye view of a single RRAM device can be seen in Fig. 2.4. The resistance of the RRAM can be manipulated by applying suitable electrical pulses, and the resistance state will be retained unless another signal is given, demonstrating the non-volatile characteristic of RRAM.

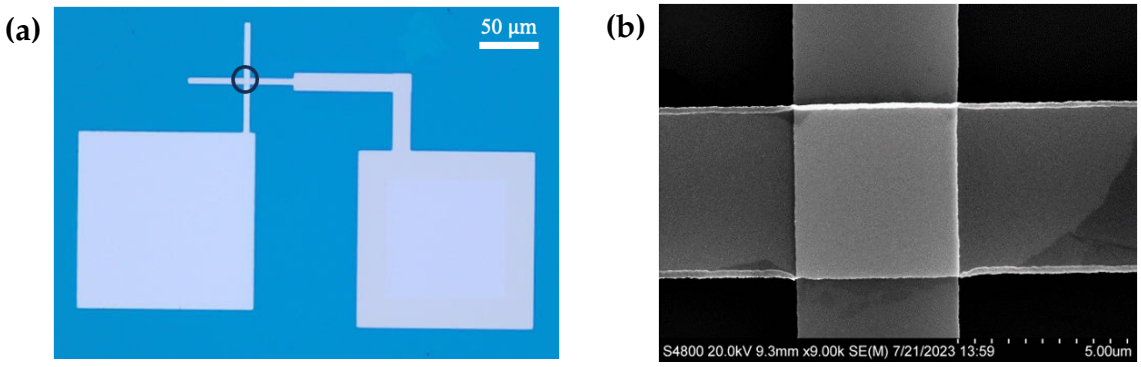


Figure 2.4: A bird's-eye view of a single RRAM device in (a) optical microscopy with MIM structure in the black circle; and (b) scanning electron microscopy.

The mechanism of RRAM resistive switching is not yet fully understood. It is generally accepted that the formation and rupture of a conductive filament (CF) present the resistive switching property [60], [61].

Typically, RRAM devices exhibit two states: a Low-Resistance State (LRS), corresponding to data '1', and a High-Resistance State (HRS), corresponding to data '0'. Consequently, the measurement of RRAM devices can be divided into two principal components: set and reset. Initially, the RRAM remains in its original

HRS state until the first electrical signal triggers the formation of the CF in the device, transitioning the RRAM into LRS; this voltage is referred to as the forming voltage. The process that turns RRAM back to HRS is called 'RESET,' with a RESET voltage (V_{reset}), while the process 'SET' describes the switching from HRS to LRS, applying a SET voltage (V_{set}). Current compliance is usually employed in the SET process to protect the RRAM from potential damage, such as thermal effects. Specifically, if it is the first time the device is set, this process is referred to as 'forming'.

2.4. RRAM switching mechanism

Two kinds of RRAM devices are introduced in this section: oxide-based random access memory (OxRAM) and conductive bridge random access memory (CBRAM).

Notably, apart from these two types of RRAM, there are many other kinds, such as RRAM based on phase transition-based CFs. Scientists have studied silicon oxide (SiO_x) devices and observed silicon enrichment during the electroforming process [62], [63]. The subsequent transition between amorphous silicon and semi-metallic silicon is believed to be the reason for the resistive switching. This filament switching is considered an intrinsic property of silicon oxide, as it occurs independently of the electrode [64].

Interfaces also play a significant role in determining the switching properties of RRAM devices [65].

2.4.1. Forming

An idealized I-V curve of the device cycle is shown in Fig. 2.5, with the forming process highlighted. The working sequence is illustrated in the graph from steps 1 to 8. Current compliance is added at the forming stage to prevent overshooting.

During the forming process, a conductive filament (CF) is formed in the device. According to the types of CF, RRAM devices can be divided into two main kinds: oxide-based random access memory (OxRAM, Fig. 2.6a) and conductive bridge

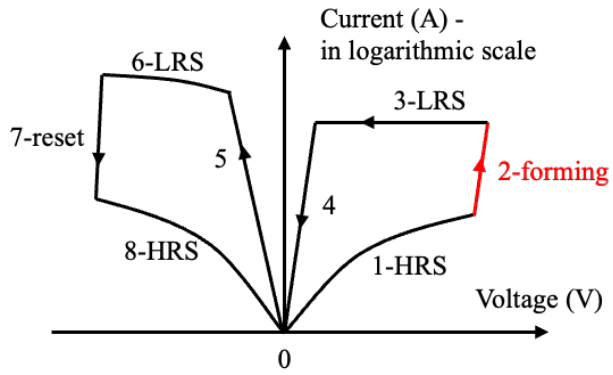


Figure 2.5: Idealized I-V curve with forming highlighted

random access memory (CBRAM, Fig. 2.6b).

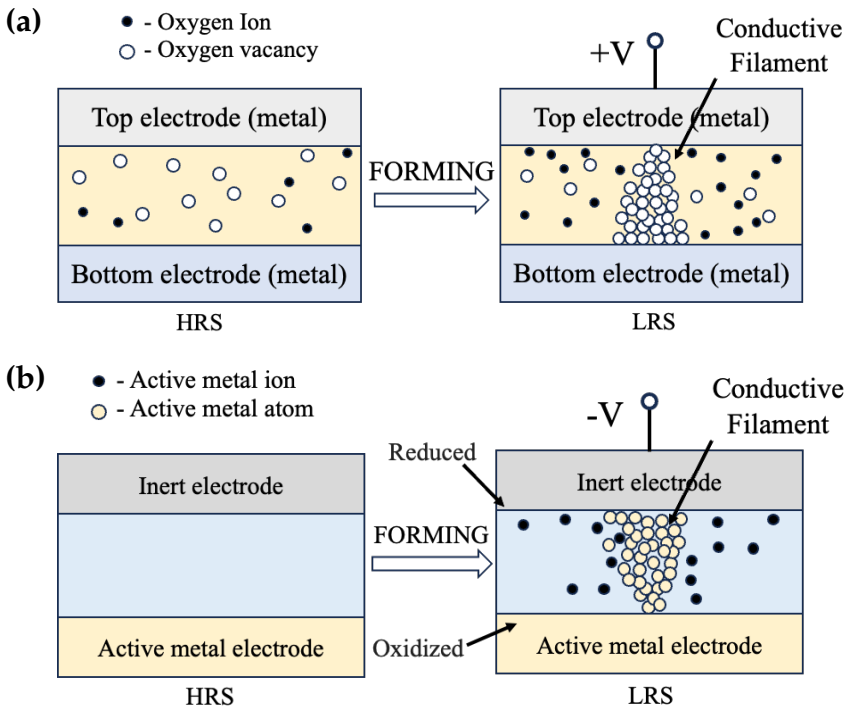


Figure 2.6: Schematic diagram of the internal structure of an RRAM forming process: (a) OxRAM forming process, where the yellow layer is the insulator. (b) CBRAM forming process, where the blue layer is the insulator.

In OxRAM, the insulator layer is usually an oxide. There are oxygen vacancies in the material (white circles in Fig. 2.6a). When a positive voltage is applied to the top electrode, the oxygen atoms may be displaced from their original positions, creating defects known as oxygen vacancies. Under a high electric field, oxygen

ions move toward the top electrode, and the resulting oxygen vacancies drift to form a CF [66]. The oxygen may be discharged at the top electrode or react with the electrode, so the electrode acts as an "oxygen reservoir" [67]. The formation of the CF significantly decreases the device's resistance, causing the transition from HRS to LRS (Fig. 2.5).

On the other hand, in the CBRAM device, the CF is composed of metal atoms (Fig. 2.6b). In this case, a negative voltage is applied to the top electrode (or a positive voltage applied to the bottom electrode). The active metal is oxidized at the bottom electrode, and the ions migrate along the electric field towards the cathode. The ions are reduced at the top electrode and deposited, growing the CF. The formation of the CF marks the presence of LRS.

2.4.2. Reset

In the reset process, a reverse voltage is applied to the bipolar RRAM devices, changing the device from LRS to HRS (Fig. 2.7).

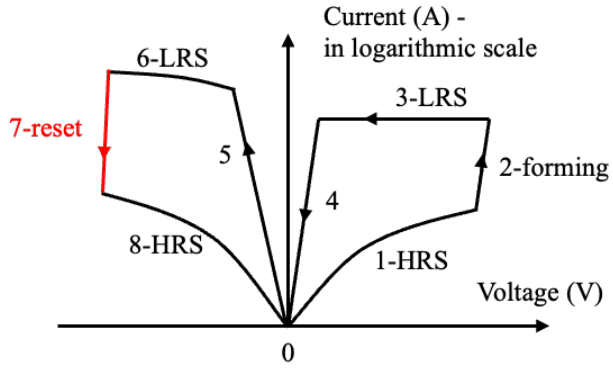


Figure 2.7: Idealized I-V curve with reset highlighted

In the reset process, a negative voltage is applied to the top electrode of the OxRAM. The reverse electric field drives the oxygen ions back into the bulk material from the interface, where they recombine with the vacancies. The loss of oxygen vacancies disrupts the CF, transitioning the device from LRS to HRS (Fig. 2.8a).

In CBRAM, a positive voltage applied to the top electrode oxidizes the metal atoms in the CF near the bottom electrode. The ions move in the opposite direction

due to the reverse electric field compared to the forming process. Consequently, the CF dissolves, and the loss of contact at the bottom electrode increases the device's resistance, turning the device into HRS (Fig. 2.8b).

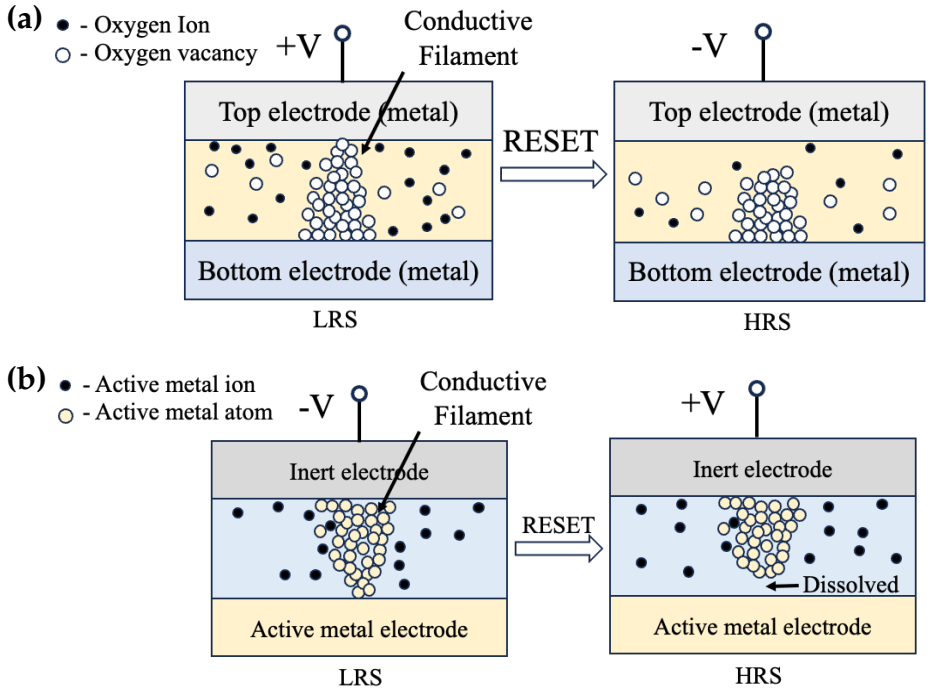


Figure 2.8: Schematic diagram of the internal structure of an RRAM reset process: (a) OxRAM reset process, where the yellow layer is the insulator. (b) CBRAM reset process, where the blue layer is the insulator.

2.4.3. Set

The set process is very similar to the forming process, during which the device changes from HRS to LRS. However, the set operation voltage is usually smaller than that of the forming process (Fig. 2.9). This is because, in a fresh device, the defects in the material are randomly arranged (as shown in the HRS images in Fig. 2.6a and Fig. 2.6b). A high forming voltage is required to build the filament and initiate the switching. After the device is formed, a base of the CF is constructed, and the reset process only disrupts part of the filament (as shown in the HRS images in Fig. 2.8a and Fig. 2.8b). Hence, a smaller voltage is needed in the set process compared to the forming process.

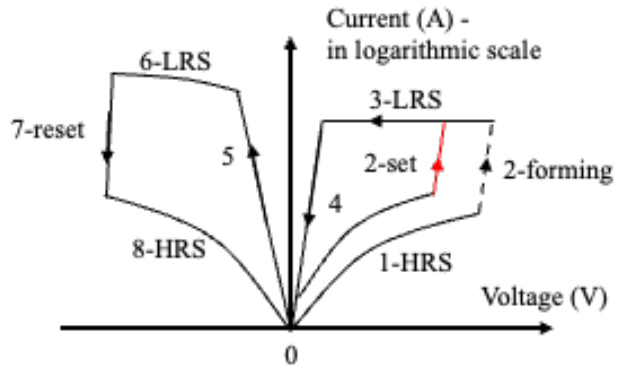


Figure 2.9: Idealized I-V curve with set highlighted

In both OxRAM and CBRAM, the CF is re-formed similarly to the forming process. The difference is that only a portion of the CF needs to be rebuilt at this time, rather than forming the entire filament. The schematic for the whole operation can be seen in Fig. 2.10. Note the difference between set and forming.

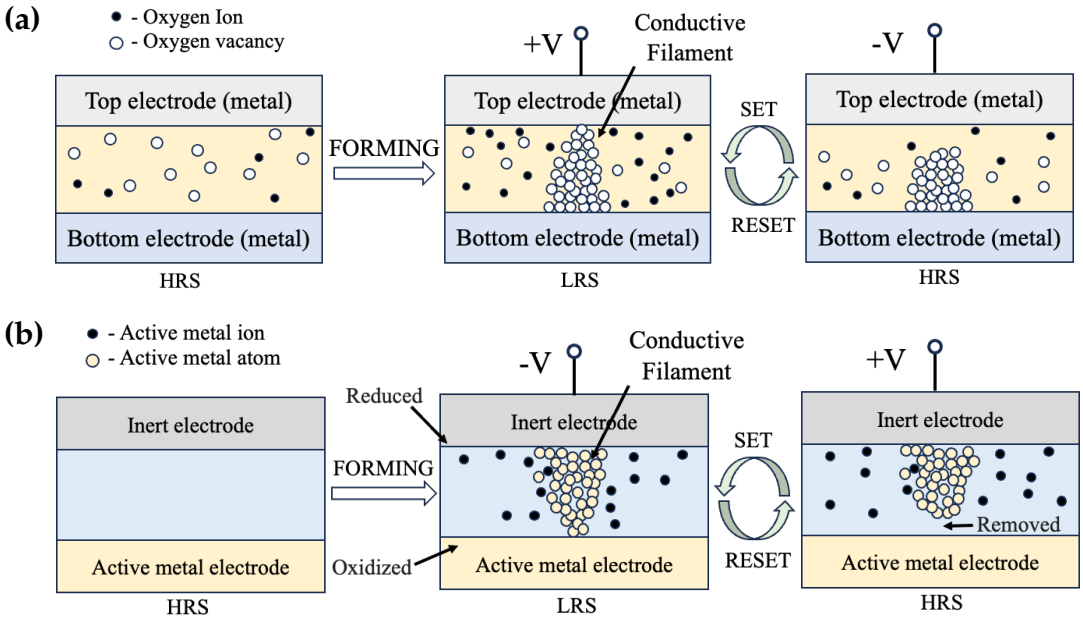


Figure 2.10: Schematic diagram of the internal structure of an RRAM during the operation: (a) OxRAM forming process, where the yellow layer is the insulator. (b) CBRAM forming process, where the blue layer is the insulator.

2.5. Challenges and outlook

Research on RRAM began early in the last century, and numerous devices exhibiting resistive switching have been demonstrated [68], [69]. Companies such as Samsung [70], Micron, and TSMC have all invested in RRAM [1]. Fig. 2.11 briefly shows the historical development of RRAM. Current studies of RRAM focus on 3D integration [71], [72], embedded memory [73], and chip-level integration [74].

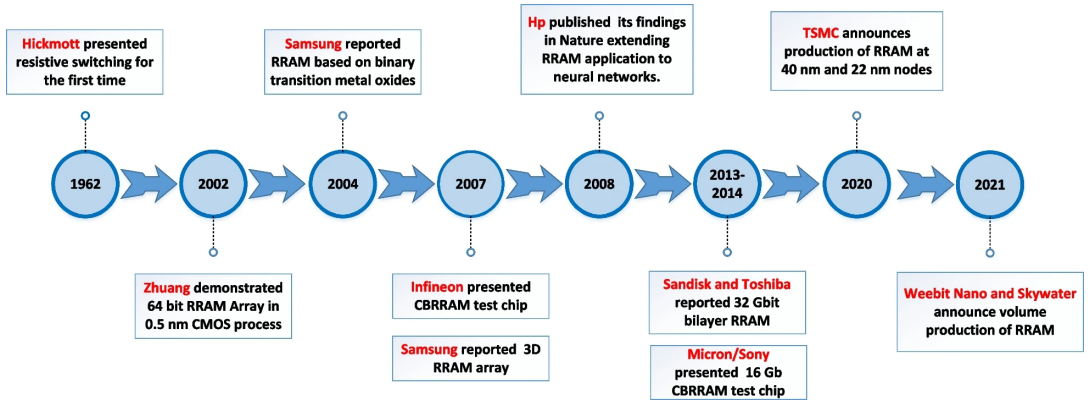


Figure 2.11: RRAM development in history [1]

RRAM has many advantages and is currently one of the hottest topics in the field of memory devices. However, there is still a long way to go before the mass application of RRAM. One of the biggest challenges for RRAM is the control of variability, both cycle-to-cycle and device-to-device [60], [75], [76]. It is also notable that, although some devices may show superiority in one or several aspects, a device that demonstrates comprehensive excellence has yet to be seen [34]. Despite many groups claiming that their devices exhibit outstanding endurance, the measuring methods may not be convincing enough [77], and device durability remains a significant concern for RRAM [60]. Additionally, a transistor/selector is commonly adapted for the crossbar array with RRAM to address the sneak current problem, limiting the device's 3D integration scalability [78]. Further study of the RRAM switching mechanism may also aid the development of RRAM, as the current understanding is still under debate, and applying certain repeatable and reliable methodologies is necessary [79].

To summarise, although this thesis attempts to address the forming issue, there is still a need for work in areas such as device reliability, endurance, and mechanism study.

3

Device Fabrication

From the previous chapter, we learned that the working mechanism of RRAM devices largely depends on the properties of the electrode. This discovery prompted my interest in studying how electrode properties affect device performance. In this chapter, the fabrication process for preparing RRAM devices is detailed. The devices are categorized into seven groups, each with a distinct electrode metal, resulting in the investigation of seven different electrode materials. Within each group, samples are fabricated with two different thicknesses and four different areas to examine additional influencing factors.

3.1. Facilities

The primary fabrication processes were conducted in the Kavli Nanolab cleanroom, located in the Faculty of Applied Sciences at TU Delft. The lab is equipped with facilities for lithography, dry etching, materials deposition, inspection, and more, providing the necessary environment for high-resolution fabrication.

3.2. Pattern design

An RRAM device typically has three layers. To investigate the influence of the device area, devices are designed with areas of 2 * 2 μm, 5 * 5 μm, 10 * 10 μm, and 20 * 20 μm. The first layer is defined as the bottom electrode, and a depiction of the first layer pattern can be seen in Fig. 3.1.

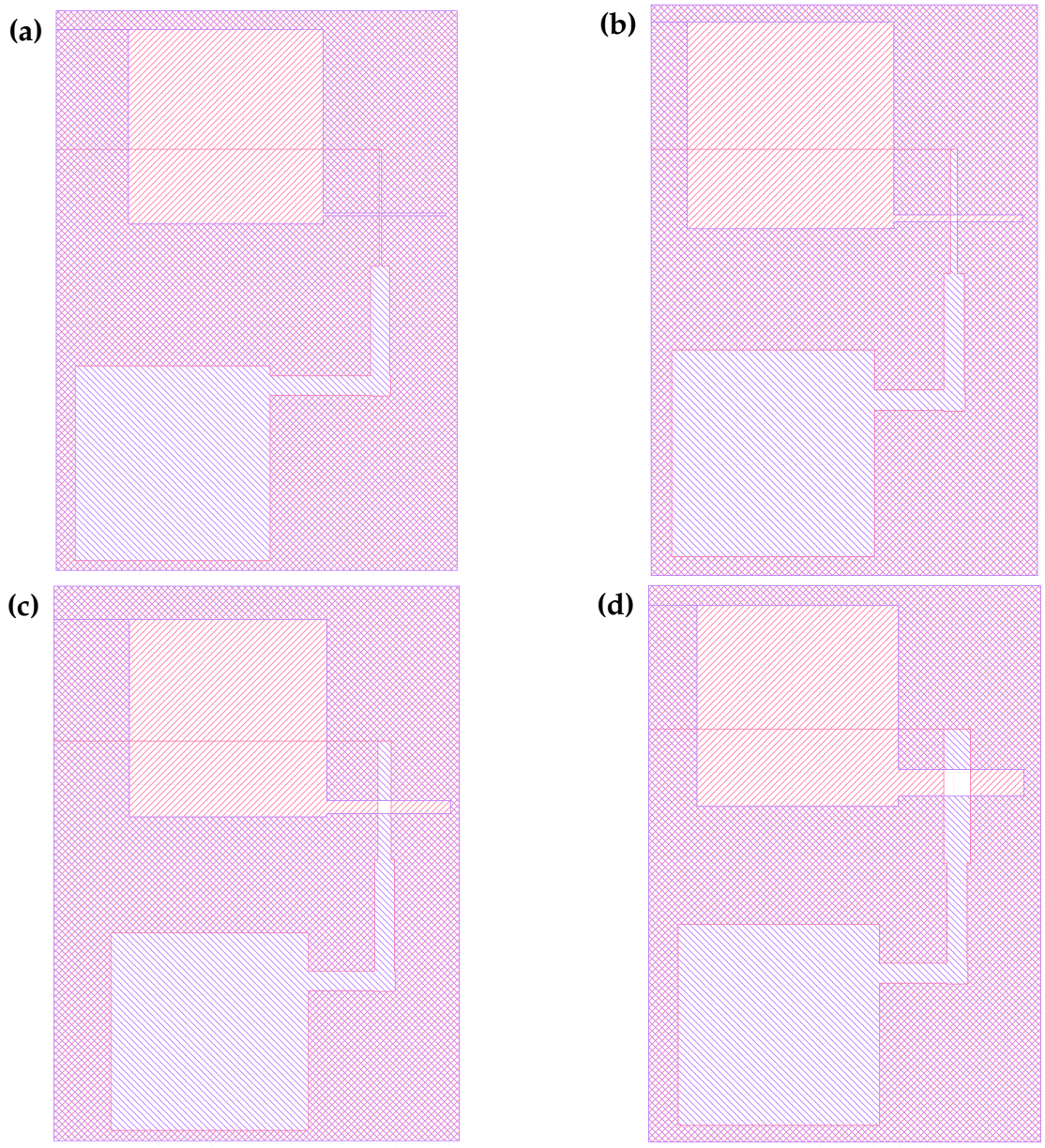


Figure 3.1: The pattern design for RRAM fabrication. The side lengths for the nodes in (a), (b), (c), and (d) are 2 μm, 5 μm, 10 μm, and 20 μm, respectively. The purple and orange colors correspond to the first and second layers.

In Fig. 3.1, the purple square, which is the lower unit in the illustration and represents the first layer, is designed as the bottom electrode. The orange square, representing the upper layer, is designated as the top electrode. The two large squares extend and eventually intersect, forming a small overlapping area that constitutes the desired device. Devices in four different areas are integrated on a single chip. These devices are formed by overlapping squares with side lengths of 2 μm, 5 μm, 10 μm, and 20 μm, respectively. For each area, the devices are arranged in twenty columns and two rows, forming a 20 by 2 array, resulting in a total of forty devices.

3.3. Wafer cleaning

The designed device is prepared on a silicon wafer. To ensure a clean surface and remove possible contamination, an acid cleaning process was performed as the first step, using fuming nitric acid (HNO_3) as the etchant. Photographs of me performing the acid cleaning process can be seen in Fig. 3.2.

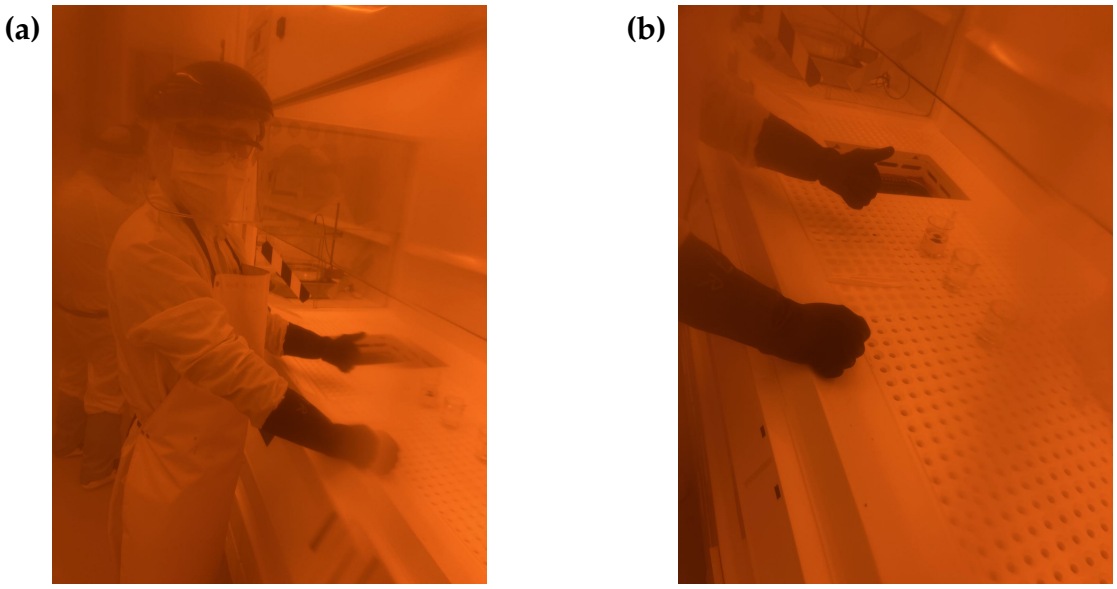


Figure 3.2: Photographs of the acid cleaning process in the cleanroom. (a) An overview picture. (b) A close-up image of the wet bench.

After the wafers were acid-cleaned, they were dried and collected in a wafer box (Fig. 3.3a). A properly cleaned wafer should appear shiny under light (Fig.

3.3b). The wafers were cleaned immediately before the experiment to prevent any dust contamination.

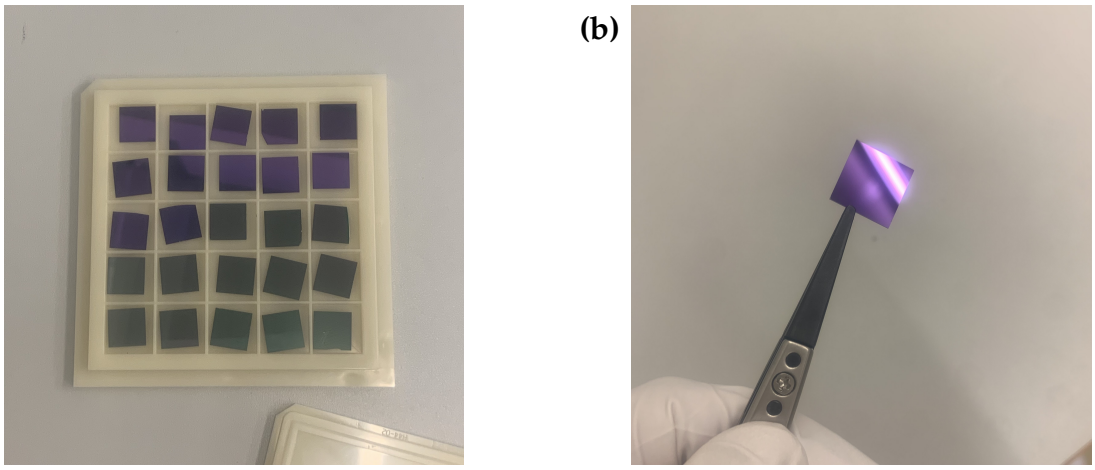


Figure 3.3: Wafers after cleaning: (a) Wafers in the wafer box. (b) A cleaned wafer under light.

3.4. First layer lithography

Lithography was performed after cleaning to create the pattern. A negative photoresist was applied to the bare wafer by spin-coating (Fig. 3.4a). The wafers were then baked to drive off solvents, solidifying the films (Fig. 3.4b). The work was carried out in the yellow light zone to protect the photoresist.

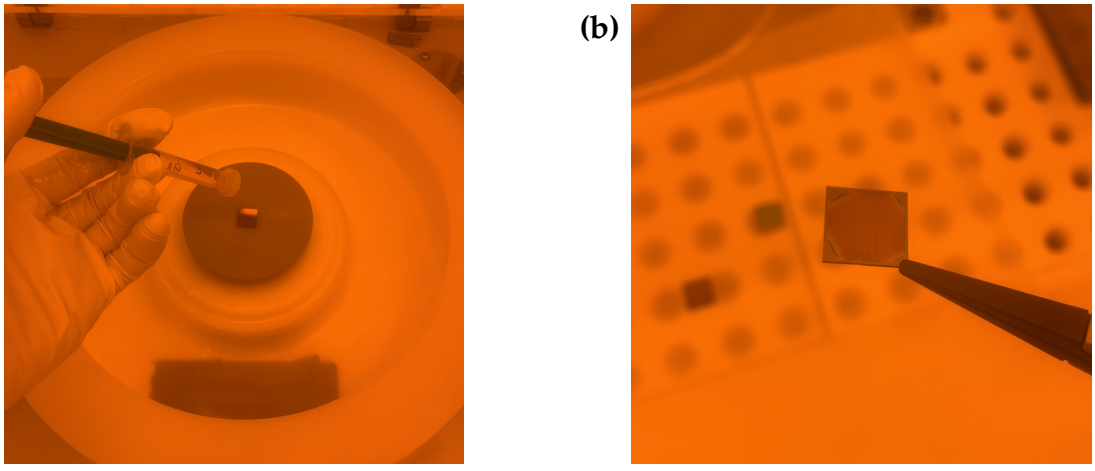


Figure 3.4: Spin coating: (a) Applying photoresist to the chip. (b) Chip after spin-coating.

The coated chips were then exposed under the laser writer (Fig. 3.5a). The laser operated at a wavelength of 365 nm. With the designed pattern uploaded to the laser writer, the graph was directly written onto the chip by the laser. The chip was then developed. The exposed portions of the negative photoresist became insoluble, while the unexposed parts dissolved in the photoresist developer (Fig. 3.5b).

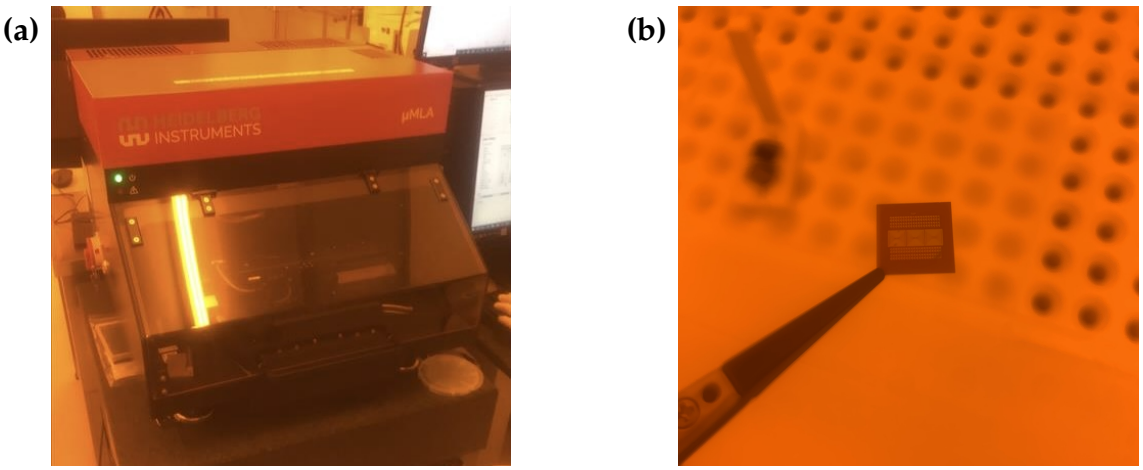


Figure 3.5: Laser-writer exposure: (a) An image of the laser writer. (b) Chip after lithography.

Residual photoresist was commonly seen after development (Fig. 3.6). Noting that photoresists are usually made of organic materials, gentle oxygen plasma was used as a photoresist descum to remove the leftovers.

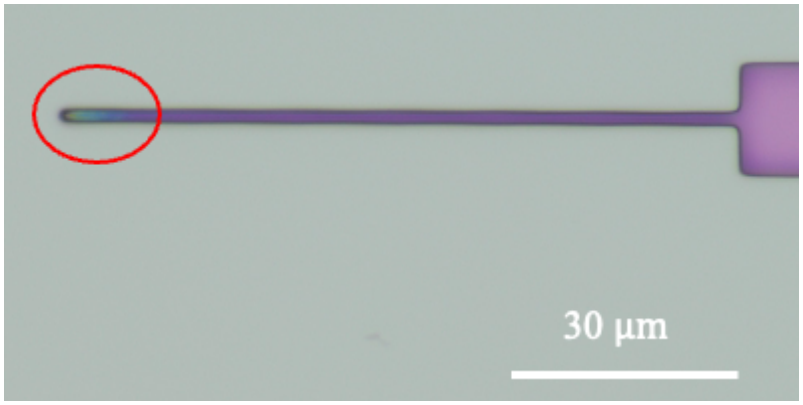


Figure 3.6: Residual photoresist after development.

The surface of the devices was clear after descumming. The optical microscopy inspection images can be seen in Fig. 3.7.

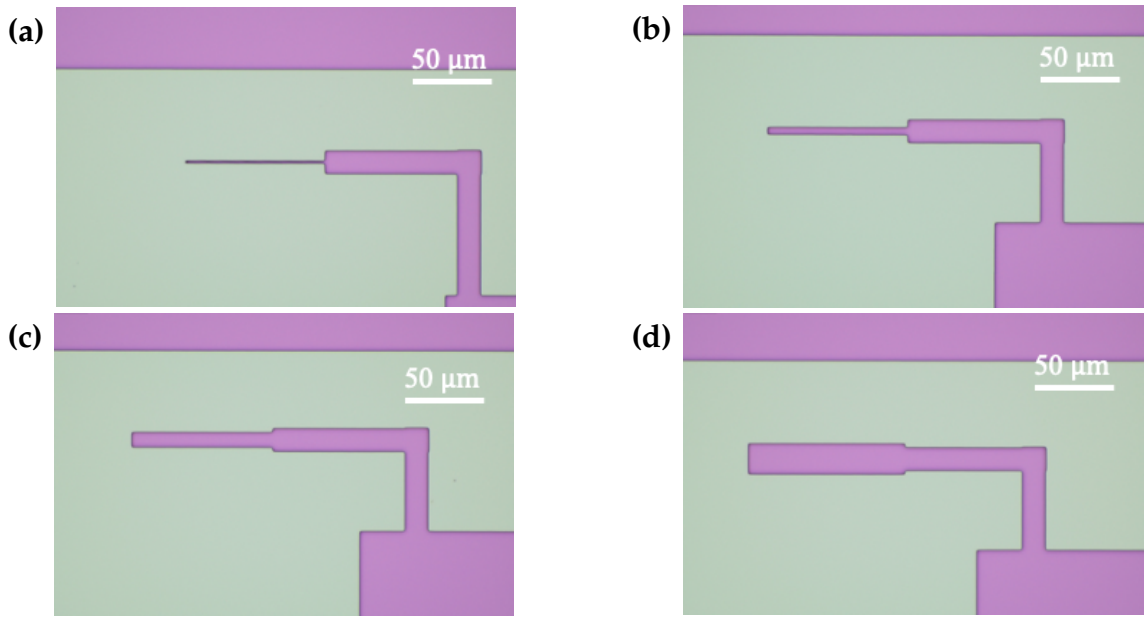


Figure 3.7: Optical microscopy inspection after first layer lithography: images (a), (b), (c), and (d) represent the devices with the cross-section side length of 2 μm, 5 μm, 10 μm, and 20 μm, respectively.

3.5. Bottom electrode deposition

After development, the chips were collected to perform the bottom electrode deposition. This was done using electron beam evaporation deposition. A high voltage was applied to the electron gun/filament to excite an emission current, which heated the target material to a very high temperature. The material was evaporated at such a high temperature, and the vapor was collected as a coating on the substrate (Fig. 3.8).

The deposition was performed with two distinct pieces of equipment. First, 5 nm of titanium was deposited as the connection/adhesion layer between the silicon-based semiconductor substrate and the subsequent metal electrode. Platinum, a common electrode material for RRAM that has been extensively reported in the literature, was then deposited to a thickness of 30 nm continuously after the titanium layer (Fig. 3.9a). Experimental bottom metals were then deposited (Fig. 3.9b). They were Au, Nb, Ni, Ru, Ta, and Ti. A control group without a bottom metal deposition was also fabricated.

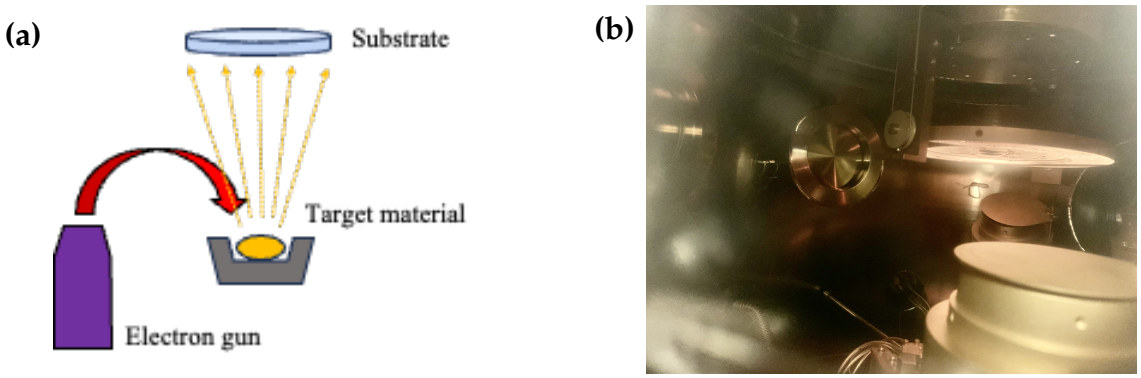


Figure 3.8: Electron beam evaporation: (a) A schematic diagram of the process. (b) A view looking into the chamber to see the substrate.

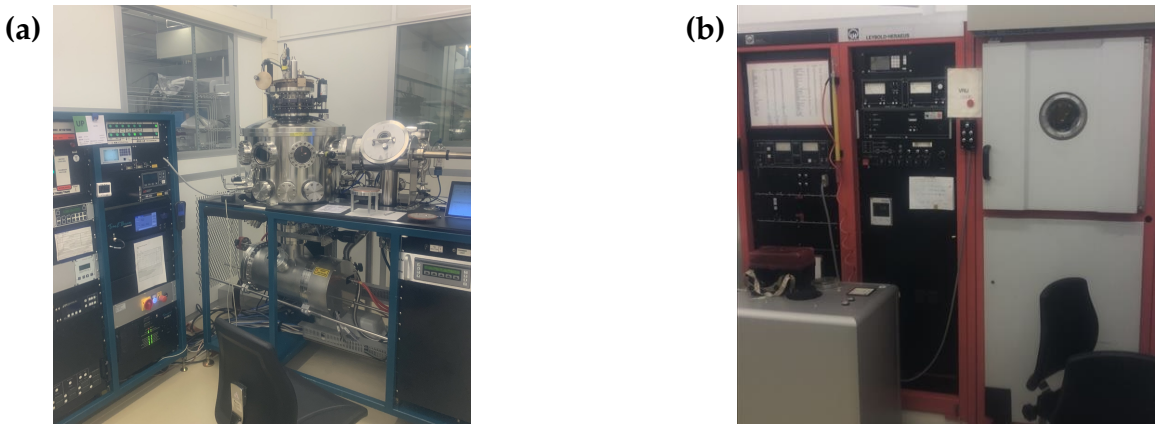


Figure 3.9: Metal deposition equipment: (a) Deposition equipment for Ti and Pt deposition. (b) Equipment for experimental deposition.

The experimental bottom metals were chosen based on the limited materials available in the lab. Ideally, a greater variety of metals would have been tested. To account for additional variables, the experimental metals were deposited in two thicknesses: 5 nm and 30 nm. An illustration of the bottom electrode deposition can be seen in Fig. 3.10.

After the bottom electrode deposition (Fig. 3.11), the chips underwent a liftoff process. During this step, the chips were soaked in a solvent, which dissolved the remaining photoresist and simultaneously removed the metal layer above it while preserving the metal on other parts of the chip. This process ensured that the desired pattern was achieved.

The result was then inspected under optical microscopy, revealing a clear and tidy liftoff. Fig. 3.12 shows the inspection results for the four different-sized

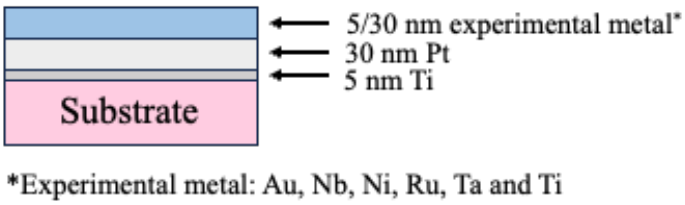


Figure 3.10: Schematic diagram of the deposition structure.

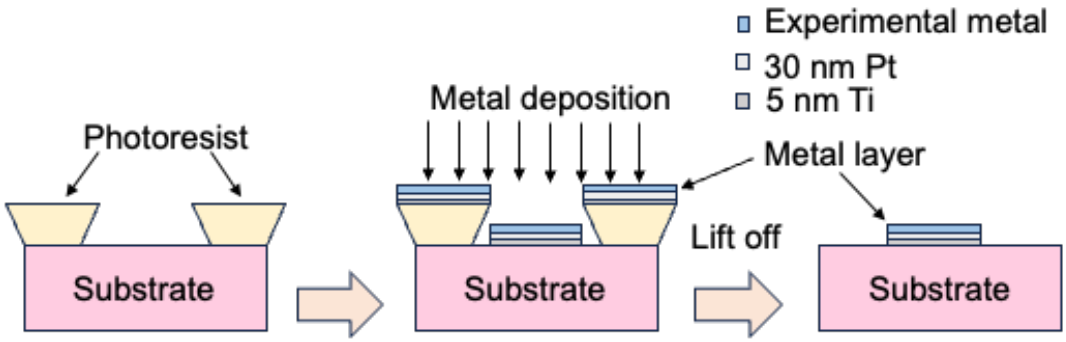


Figure 3.11: Schematic diagram of the liftoff process.

devices.

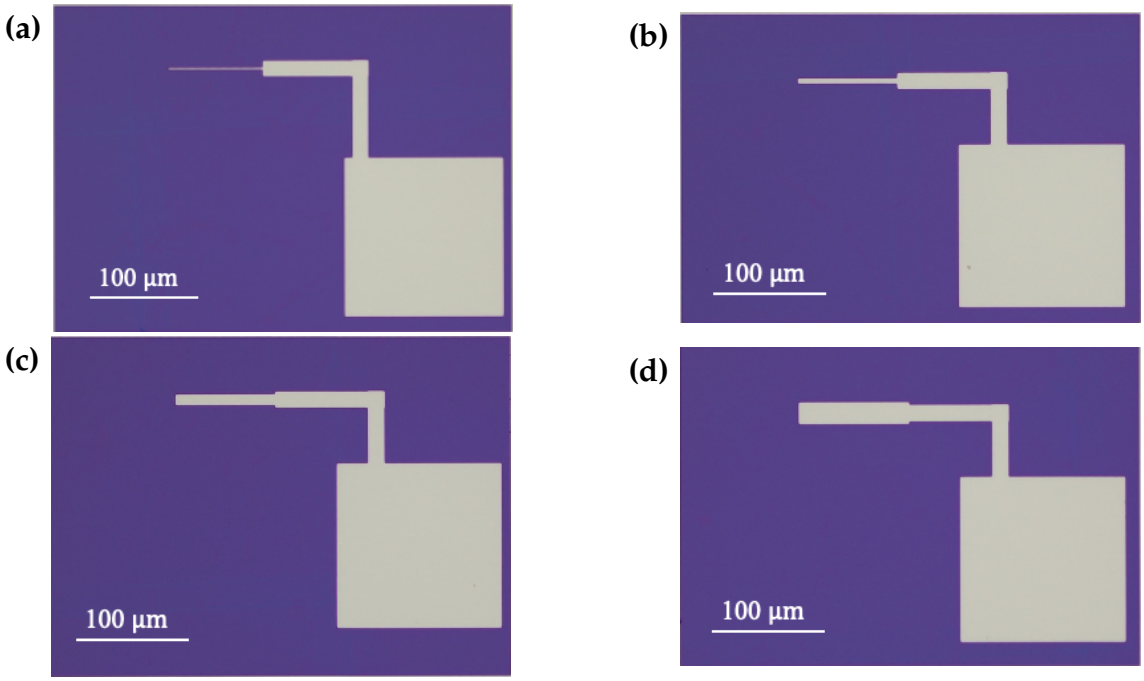


Figure 3.12: Optical microscopy inspection after bottom electrode liftoff: images (a), (b), (c), and (d) represent the devices with the cross-section side lengths of 2 μm, 5 μm, 10 μm, and 20 μm, respectively.

3.6. Dielectric sputtering

A layer of HfO_2 was then sputtered onto the bottom layer. HfO_2 is a commonly used dielectric material in RRAM applications. During sputtering, argon (Ar) gas was introduced into the chamber. Electromagnetic excitation was applied to ionize the argon, forming Ar^+ ions. This plasma was created, and the Ar^+ ions were accelerated to strike the target material, HfO_2. Each ion that struck the target transferred its momentum, dislodging target atoms. The dislodged atoms gained energy from the impact and traveled directly to the substrate surface, forming a thin film. A schematic diagram illustrating the principle of sputtering can be seen in Fig. 3.13.

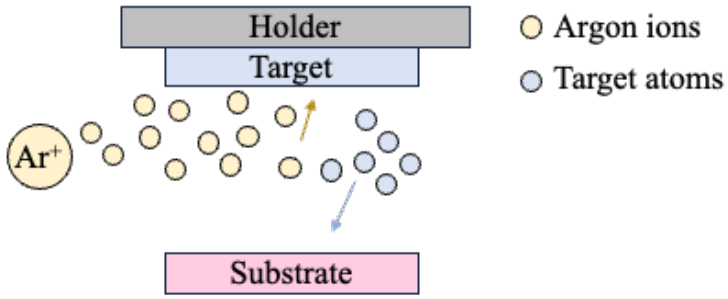


Figure 3.13: Schematic diagram of the sputtering process.

A 5 nm layer of HfO_2 was sputtered onto the chips. A comparison between the chips before and after sputtering can be seen in Fig. 3.14. Please note the color difference between the two states.

(a) **(b)**

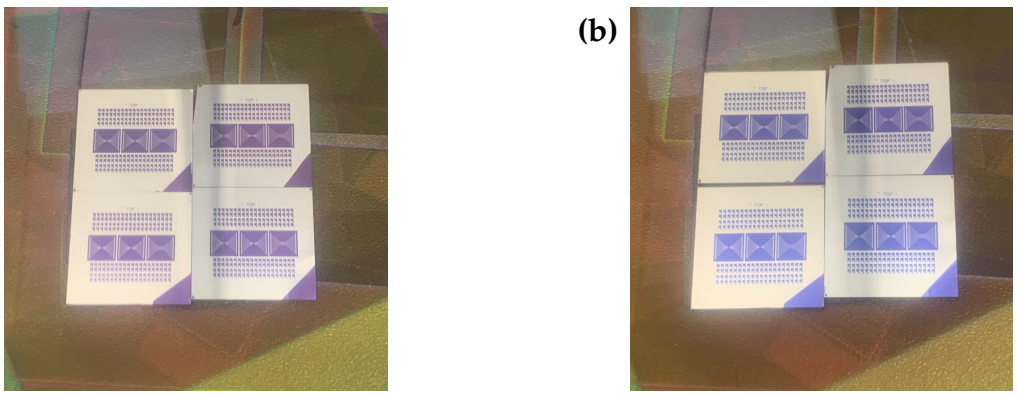


Figure 3.14: Dielectric sputtering: Chips (a) before and (b) after sputtering.

3.7. Top electrode lithography and deposition

The top electrode was introduced afterward, following a process similar to the bottom electrode fabrication. Lithography was performed (Fig. 3.15), followed by deposition.

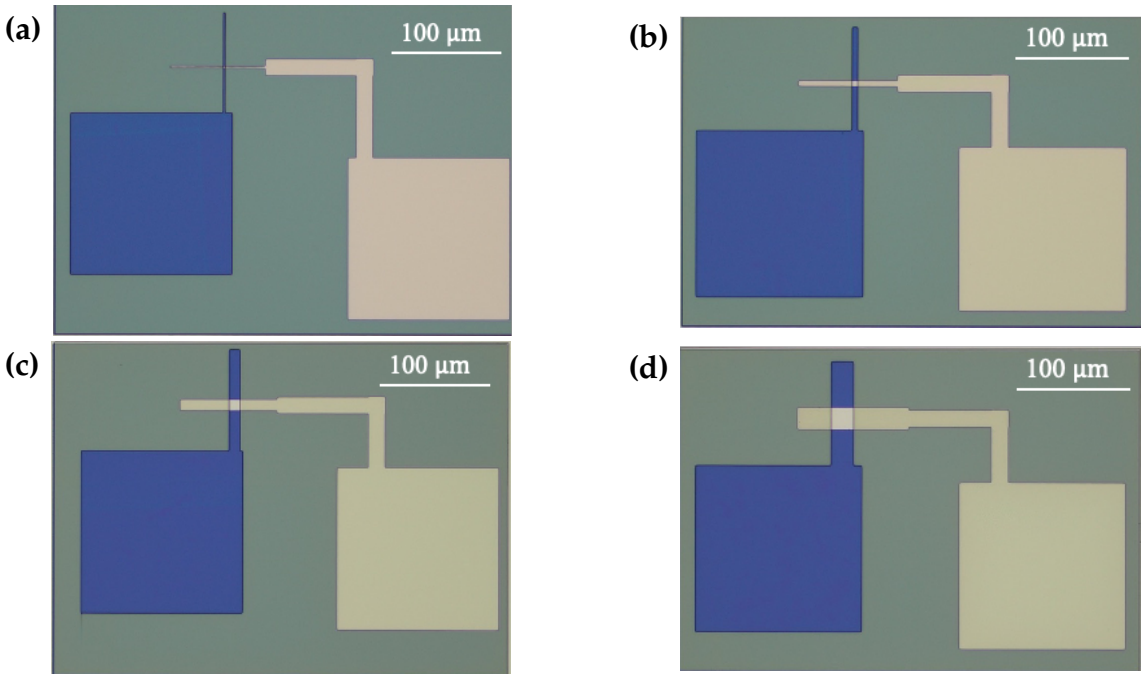


Figure 3.15: Optical microscopy inspection after top electrode lithography: images (a), (b), (c), and (d) represent the devices with cross-section side lengths of 2 μm, 5 μm, 10 μm, and 20 μm respectively.

The device was then deposited with 5 nm of titanium, which acted as a capping layer to introduce oxygen vacancies, and 30 nm of platinum, which is a conventional electrode metal (Fig. 3.16).

To examine the node, an optical microscopy inspection was performed, focusing on the cross-section. A clean cross was observed for each of the devices (Fig. 3.17), and the vertical structure corresponded exactly with that shown in Fig. 3.16.

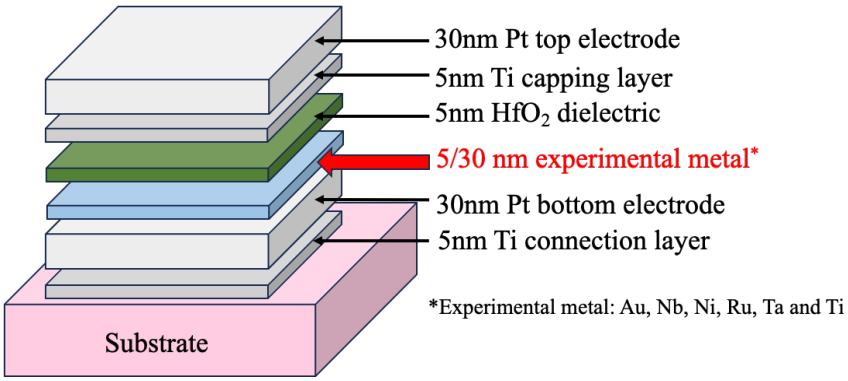


Figure 3.16: 3D schematic diagram of the device structure.

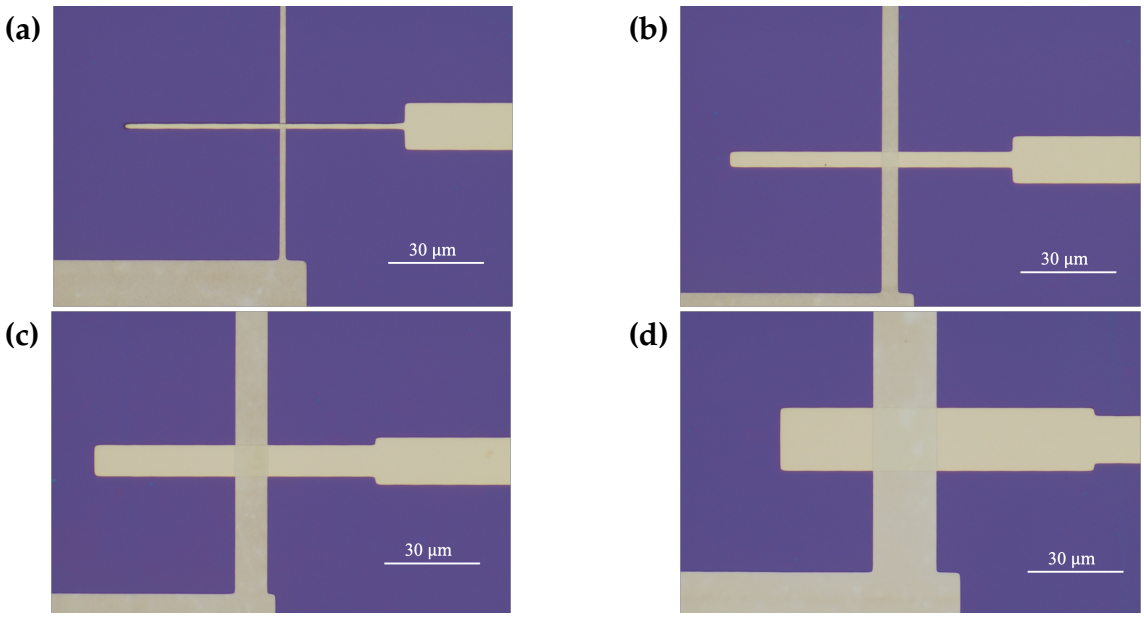


Figure 3.17: Optical microscopy inspection after top electrode deposition: images (a), (b), (c), and (d) represent the devices with cross-section side lengths of 2 μm, 5 μm, 10 μm, and 20 μm respectively.

3.8. Bottom electrode exposure etching

After the top layer deposition, a dielectric etching was performed. In this step, the dielectric on top of the bottom electrode was etched away to expose the bottom electrode for the subsequent measurement. The chips underwent a third-layer lithography process to create small windows on top of each bottom electrode. Subsequently, reactive-ion etching with a CHF_3/Ar gas mixture was used to remove the dielectric. During this process, the CHF_3 reacted with the HfO_2, and

the Ar etched the chip physically through bombardment. The etching rate had to be carefully controlled to etch away the covering dielectric while preserving the underlying metal structure. A three-dimensional schematic diagram showing the etching process can be seen in Fig. 3.18.

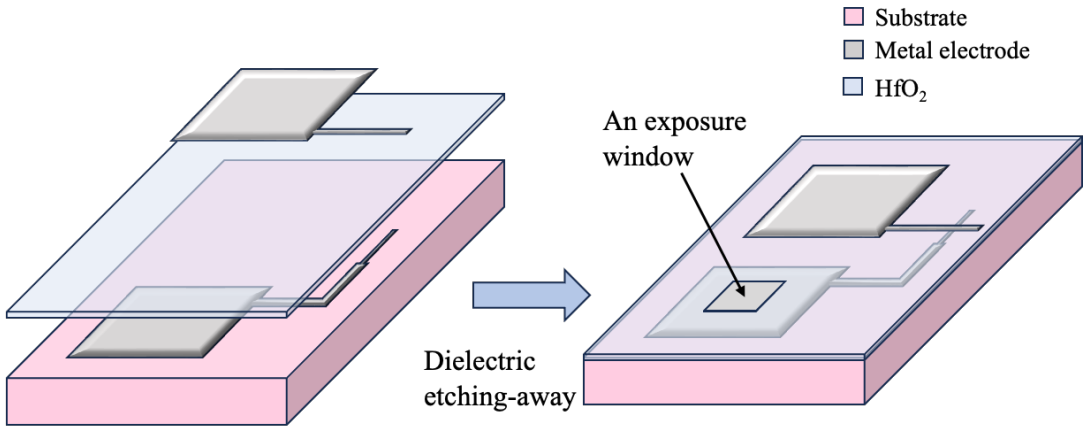


Figure 3.18: Schematic diagram of the dielectric etching process.

At this stage, the preparation process was essentially complete. A view of the finished chip can be seen in Fig. 3.19.

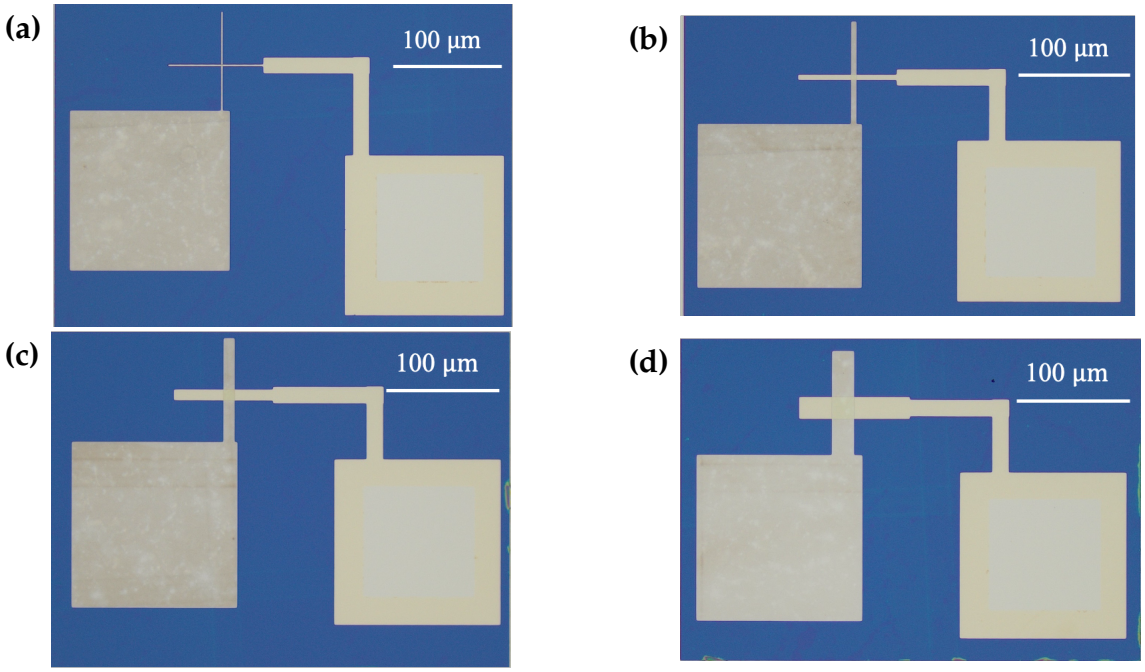


Figure 3.19: Optical microscopy inspection of the finished chip: images (a), (b), (c), and (d) represent the devices with cross-section side lengths of 2 μm, 5 μm, 10 μm, and 20 μm respectively.

Please note that the vertical structure of the cross-point, shown in Fig. 3.16, forms a metal-insulator-metal RRAM. Observe the small square in the center of the bottom electrode, visible as the shiny window in the center of the larger square on the right in each image. This window exposes the bottom electrode.

3.9. Final device structure

The final device structure is shown in Fig. 3.20. The main difference between the device I prepared and conventional RRAM devices is the addition of the bottom metal layer. This bottom metal is expected to modify the device's performance. Devices with bottom metal layers of 5 nm and 30 nm thickness were fabricated. Both the top electrode and bottom electrode consist of a 30 nm platinum layer (light grey in Fig. 3.20) and a 5 nm titanium layer (dark grey in Fig. 3.20). A control group without the bottom metal layer was also fabricated.

For each bottom metal at each thickness, two chips were fabricated simultaneously in case one failed during the preparation. Consequently, more than 25 chips were collected during the fabrication process.

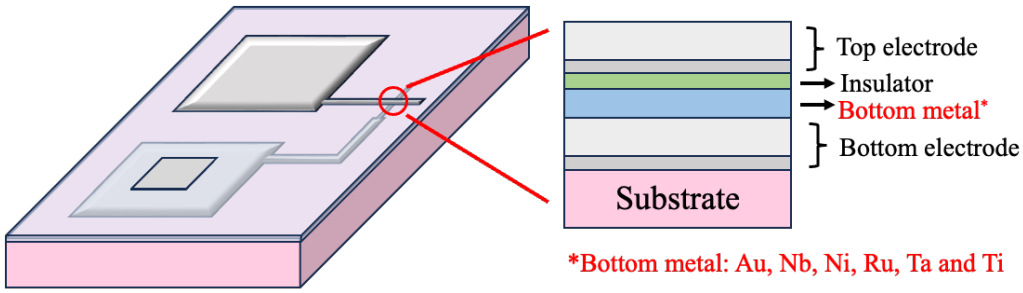


Figure 3.20: Three-dimensional image and cross-sectional image of the device. Light grey: 30 nm platinum layer. Dark grey: 5 nm titanium layer. Insulator layer: 5 nm HfO_2.

3.10. Device characterization

3.10.1. X-ray diffraction analysis

Devices were characterized after fabrication. They were first examined by X-ray diffraction (XRD) to gain phase information (Fig. 3.21, thanks to Mr. Richard Huizenga). Unfortunately, the phases of the two experimental metals and titanium layers were not detected due to their thin thickness. However, the presence of platinum and silicon was confirmed, verifying the successful deposition of the metal on the wafer.

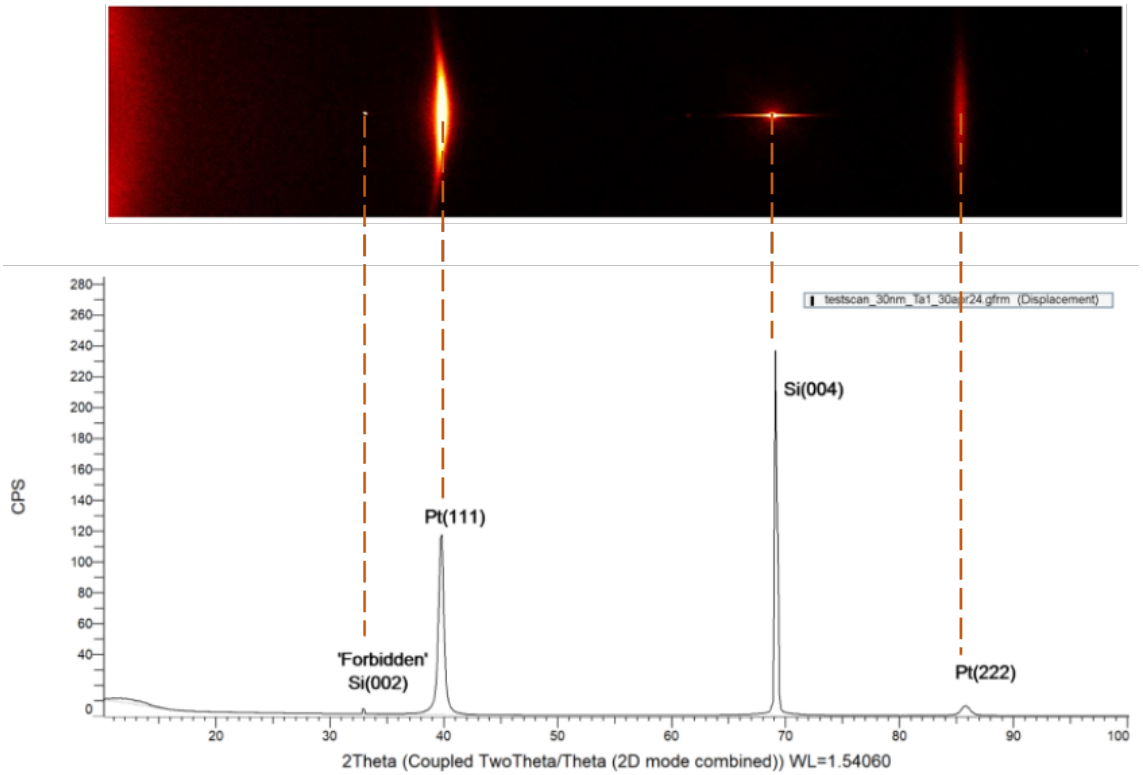


Figure 3.21: XRD measurement results. Platinum and silicon are detected.

3.10.2. Scanning electron microscopy inspection

Scanning electron microscopy (SEM) was used to inspect the devices. SEM is a technique that scans a sample with a focused electron beam. These electrons interact with the sample and carry information about the sample's topography. By

analyzing these electrons, an image of the sample can be acquired. Due to its very small wavelength, the electron beam can detect minute structures.

In this thesis, SEM was adopted to image the RRAM cross node (red circled area on the left of Fig. 3.20). Pictures were taken from a bird's-eye view, but the overlapping of the bottom electrode and top electrode can still be seen in the images.

The inspection of the RRAM node is shown in Fig. 3.22. The horizontal line in each image represents the bottom electrode, and the vertical line represents the top electrode. An HfO_2 dielectric layer is situated between the electrodes. The bottom metal layer sits between the bottom electrode and the HfO_2 layer. The device forms an MIM structure RRAM (right image Fig. 3.20).

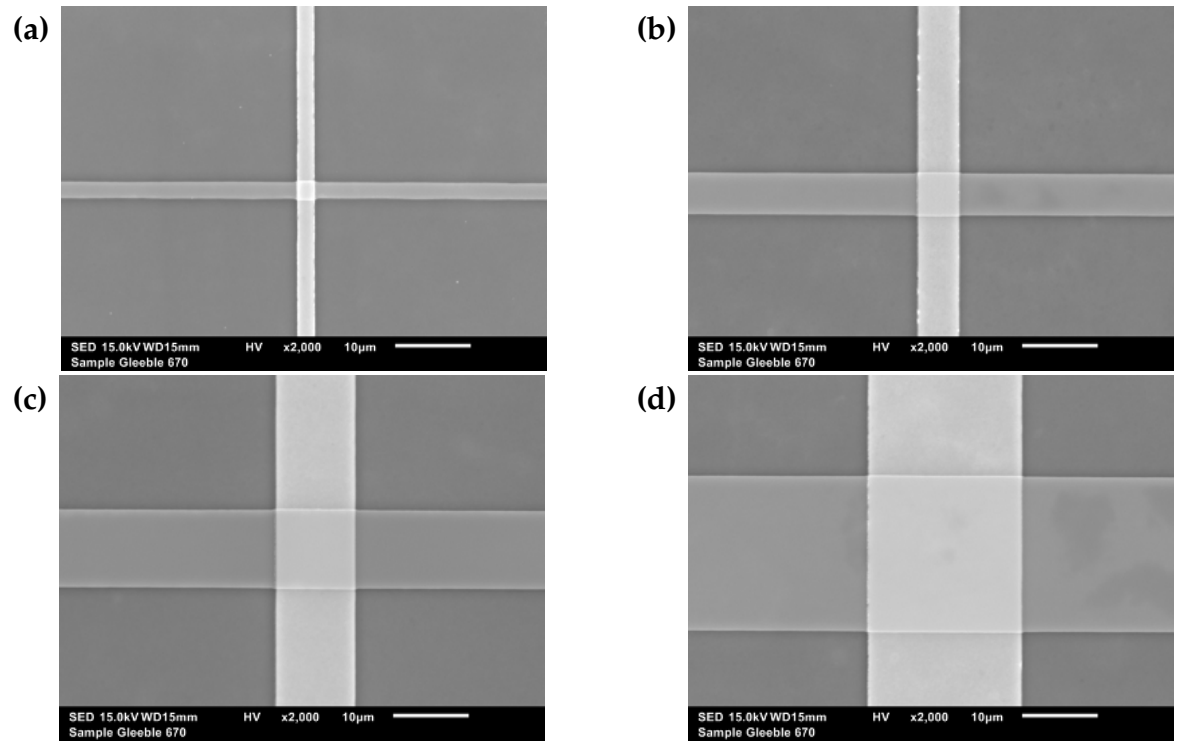


Figure 3.22: SEM inspection of the finished chip: images (a), (b), (c), and (d) represent the devices with cross-section side lengths of 2 μm, 5 μm, 10 μm, and 20 μm respectively.

3.10.3. Energy-dispersive X-ray spectroscopy analysis

Additionally, the electron beam can interact with atoms in the material, exciting inner electrons and creating inner electron holes. An outer electron may then jump into the hole, releasing the energy difference in the form of an X-ray. By analyzing these X-rays, we can determine the elemental composition of the sample. This technique is known as energy-dispersive X-ray spectroscopy (EDS).

To confirm the success of the metal deposition, EDS was used to analyze the device. Using the chip with tantalum as the bottom metal layer as an example, the results are shown in Fig. 3.23. The positive identification of titanium, tantalum, and platinum confirms the successful deposition of both the experimental metal and the electrode metal.

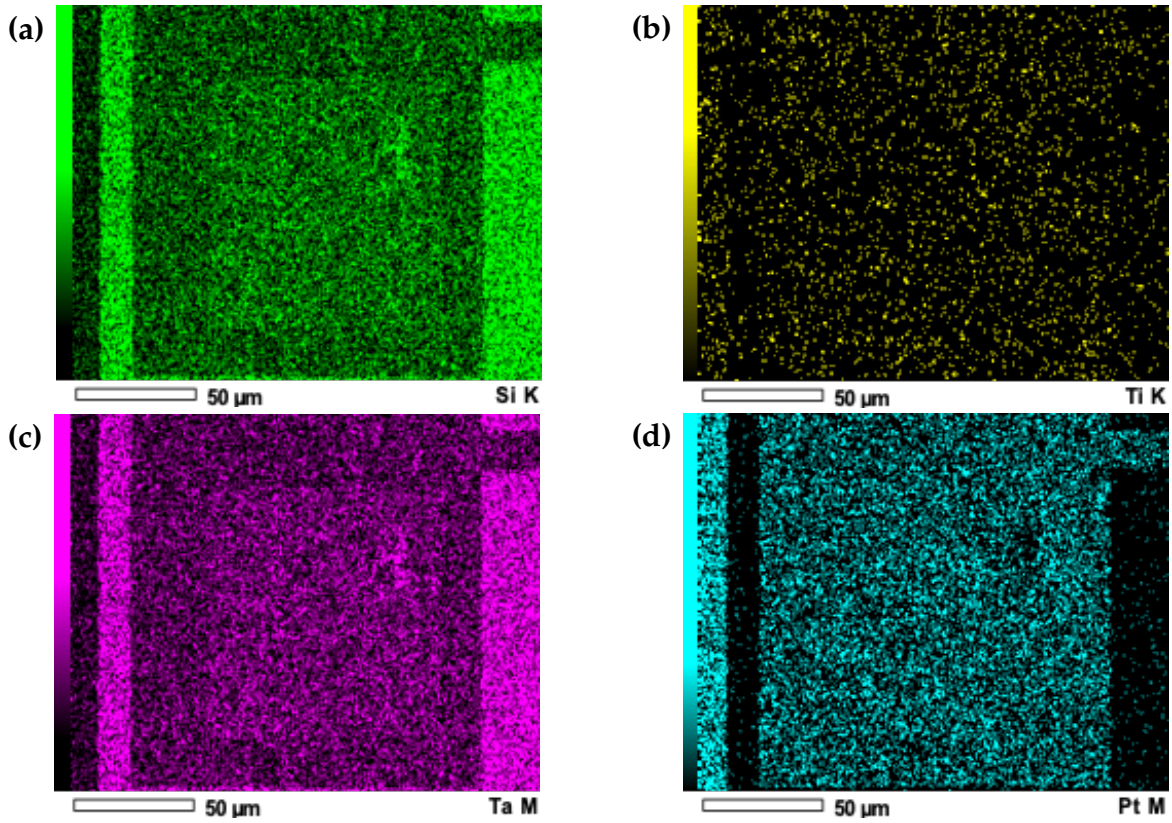


Figure 3.23: EDS inspection results: (a) Positive identification of silicon, the substrate material. (b) Positive identification of titanium, the connection layer between the substrate and electrode. (c) Positive identification of tantalum, the experimental metal of the chip. (d) Positive identification of platinum, the electrode material.

4

Device Measurement

Having completed the fabrication, the chips were collected for electrical measurement. A view of the prepared chip can be seen in Fig. 4.1 below.

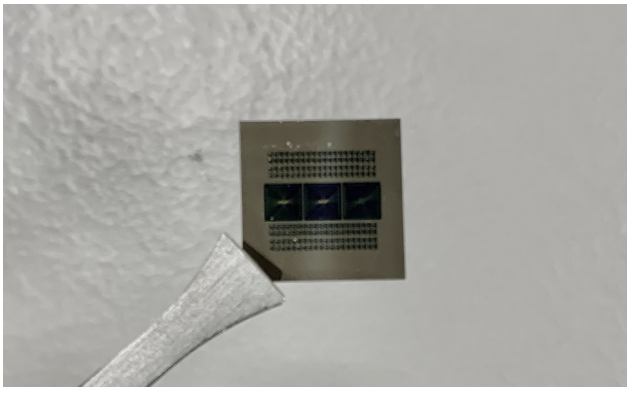


Figure 4.1: A view of the fabricated chip.

4.1. Facility and equipment

The measurement was conducted in the measurement room of the Else Kooi Laboratory at TU Delft. The equipment utilized for this process was the B1500A

Semiconductor Device Parameter Analyzer. Notably, the measurement was carried out in a regular atmosphere room, rather than in a cleanroom environment (Fig. 4.2).

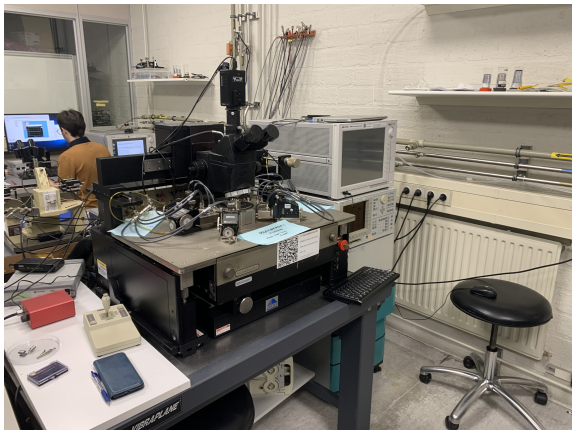


Figure 4.2: An image of B1500A in the measurement room.

4.2. Measurement process

During the measurement process, two metal probes were positioned on the bottom and top electrodes. The bottom electrode was grounded while a voltage signal was applied to the top electrode (Fig. 4.3a). Consequently, all the voltages discussed in this section refer to those applied to the top electrode. An image depicting the measurement process is shown in Fig. 4.3b.

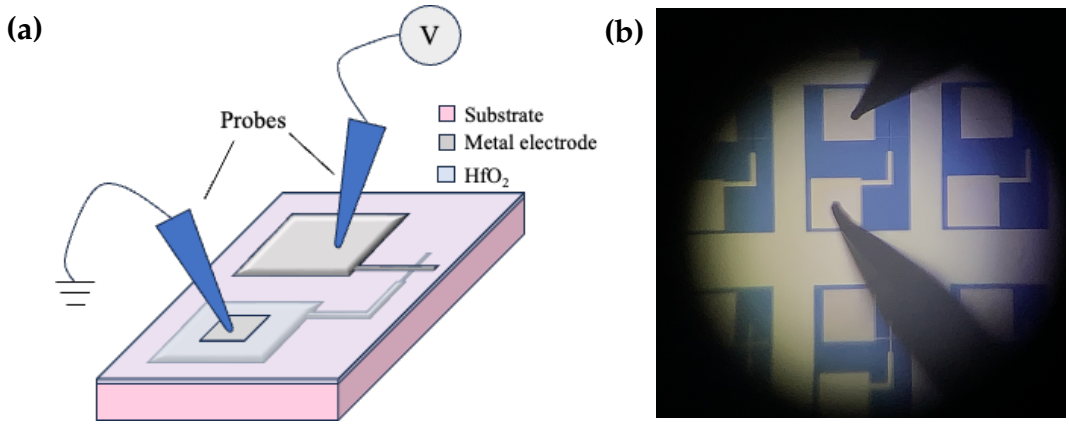


Figure 4.3: Illustration of the measurement process: (a) Schematic diagram of the measuring process. (b) A photograph of the measuring process.

Chips with different experimental bottom metals deposited in different thicknesses were fabricated. In the measurement step, more than 220 devices were tested, and 2000 cycles were run. The overall results are summarized to provide a brief overview. A table showing the fabricated samples is listed in the following Table 4.1.

Table 4.1: Number of chips that fabricated

Size / Metal	2 μm * 2 μm	5 μm * 5 μm	10 μm * 10 μm	20 μm * 20 μm
Au	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm
Nb	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm
Ni	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm
Ru	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm
Ta	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm
Ti	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm	2 * t=5 nm 2 * t=30 nm

* Note: "t" represents the thickness of the metal layer.

** Note: a control group without bottom metal deposited was prepared as well.

4.3. Measurement result

Devices were measured, and the device with a 30 nm bottom metal of Au serves as an example (Fig. 4.4). We can clearly observe the forming (red line), set (grey line), and reset (grey line) processes. The forming voltage is significantly higher than the set voltage. Specifically, it was observed that there are two forming cycles for the 2 µm x 2 µm device (Fig. 4.4a), likely due to the complete CF rupture after the

first reset. The forming voltage remains stable across devices of different sizes.

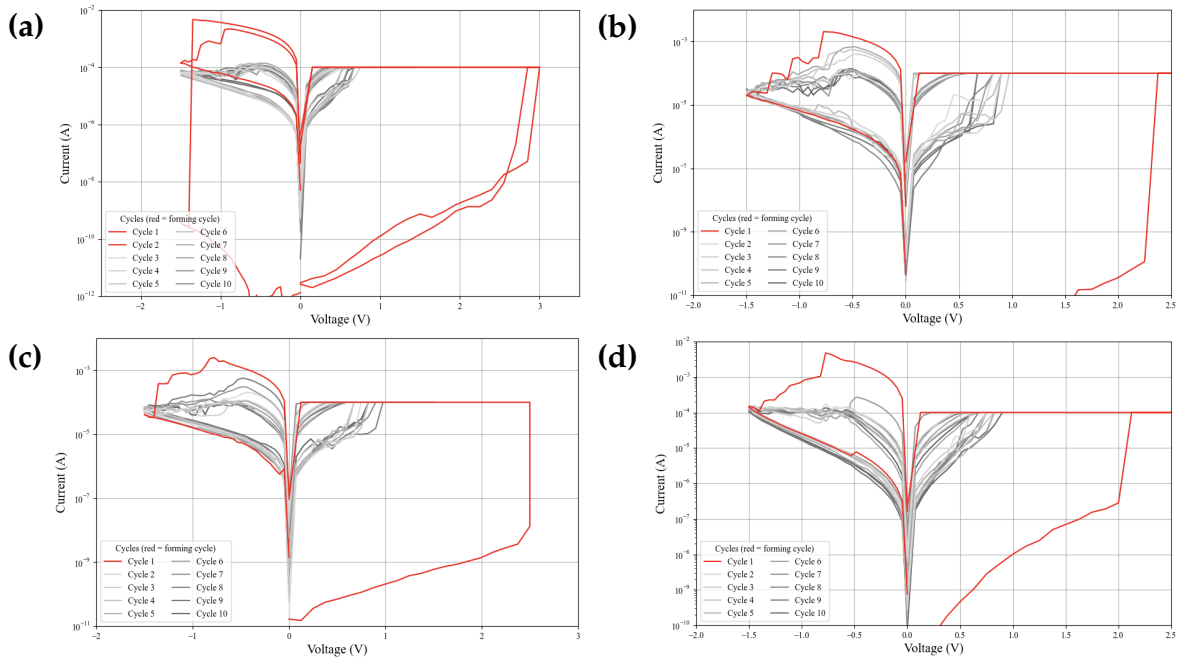


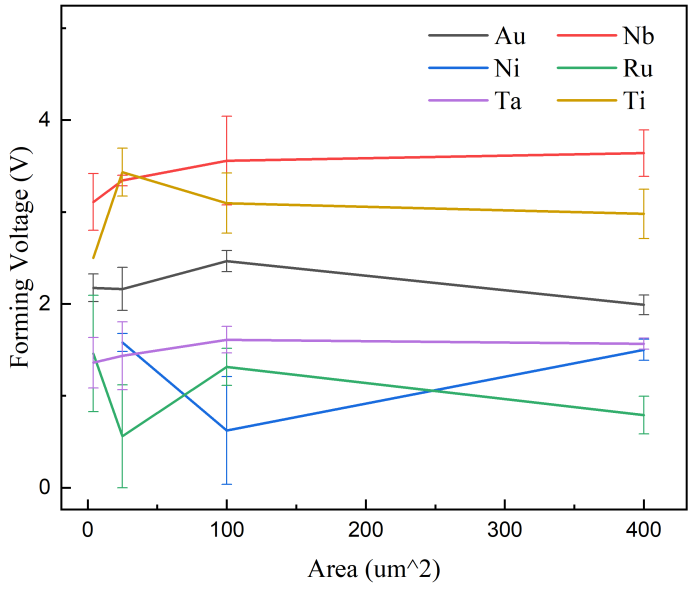
Figure 4.4: 30 nm Au bottom metal measurement results. Red lines: forming cycles; grey lines: regular set and reset cycles. (a) Device size: 2 μm x 2 μm. (b) Device size: 5 μm x 5 μm. (c) Device size: 10 μm x 10 μm. (d) Device size: 20 μm x 20 μm.

Multiple single devices were tested for each bottom metal at each device size. The average forming voltage was calculated and summarized in Fig. 4.5. The forming voltage is found to vary among different bottom metals.

The group labeled with Pt is the control group, where no additional bottom metal was deposited, so the 30 nm Pt electrode directly contacted the insulator. It is observed that RRAM devices are generally insensitive to the area, especially when the device size is relatively large, except for those with Nb and Ti bottom metals. The significant variation in Nb and Ti devices across different areas can be explained by the transformation of the switching mode. During the measurements, devices with Nb and Ti bottom metals were observed forming at both positive and negative voltages. This may be because Nb and Ti absorb oxygen from the insulator, acting as "oxygen reservoirs" and introducing oxygen vacancies from the bottom, which reverses the filament growth direction. The larger the device, the more dominant the role of the bottom metal. Therefore, these devices are more

likely to display a negative forming voltage.

(a)



(b)

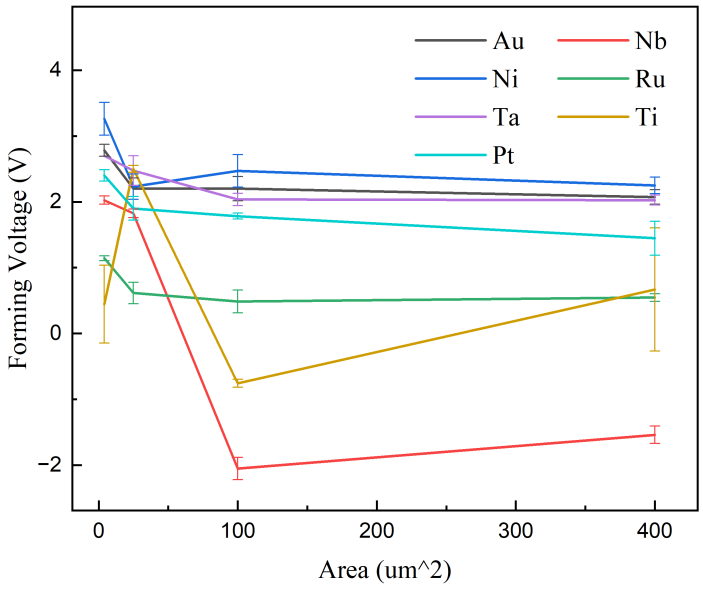


Figure 4.5: Measurement results with area variation. (a) Devices with bottom metal 5 nm thick. (b) Devices with bottom metal 30 nm thick.

4.4. Forming-free devices

During the measurements, forming-free devices were tested, most of which were Ru-based. An example is shown in Fig. 4.6, where the red line represents the first forming cycle. It is clearly seen that there is no forming voltage for the device.

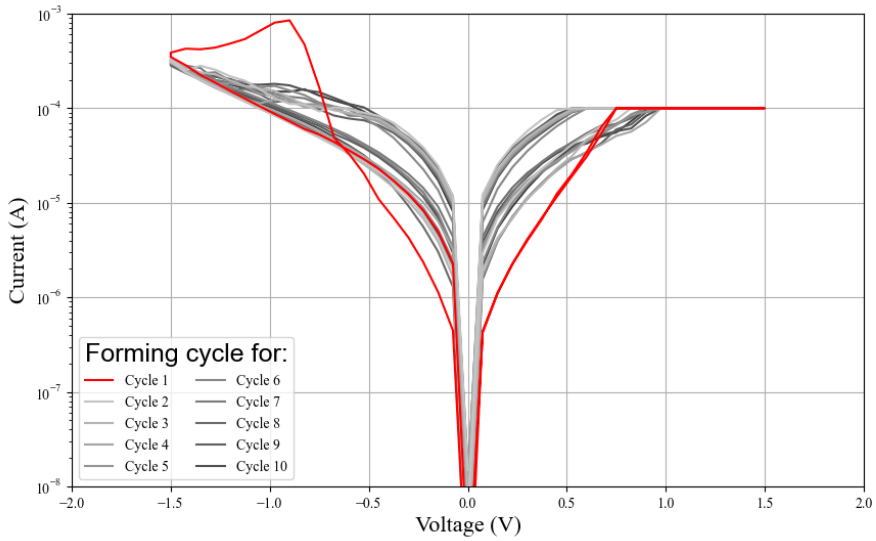


Figure 4.6: A forming-free Ru-based device.

Throughout the measurements, approximately 35% of Ru-based devices were observed to be forming-free. To explain this observation, the chemical activity of the bottom metal is suspected to play a key role (Fig. 4.7).

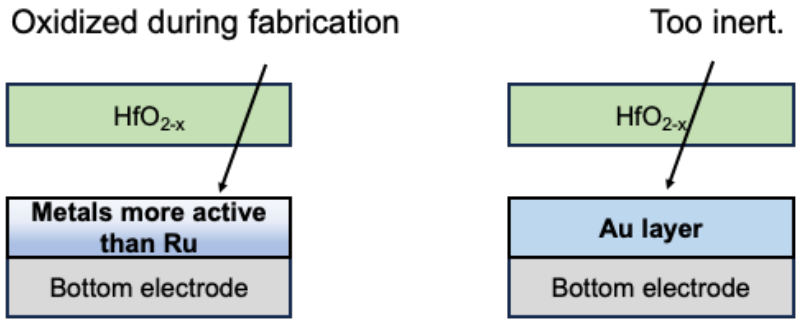


Figure 4.7: Explanation of the forming-free devices.

It is important to note that the bottom metal was expected to be oxidized by the insulator, causing oxygen vacancies to be implanted into HfO_2 to facilitate

the forming process. The hypothesis suggests that metals more active than Ru could have already been oxidized in the atmosphere during the fabrication process [80], resulting in no oxygen being absorbed from the HfO_2 after compaction. Conversely, gold might be too inert to attract any oxygen from the insulator, so the forming voltage was not affected.

Ru likely serves as the optimal point regarding chemical activity, being neither too active to be oxidized in the atmosphere nor too inert to remain uninfluenced by the devices. However, it is crucial to remember that the results are multifactorial rather than solely determined by chemical activity, as will be revealed in the following chapter.

5

Data Analysis

Having collected the data, it is crucial to understand how various factors determine the forming voltage. Computational methods were developed to elucidate these influences. The coding was accomplished with the assistance of ChatGPT [81].

5.1. Dataset

First, materials data were collected from The Materials Project [82]. The Materials Project is a "multi-institution, multi-national effort" designed to assist materials science researchers in reducing uncertainties through theoretical calculations to enhance research efficiency. The website hosts a vast repository of materials science information, including but not limited to material density, crystal structure, spatial arrangement, and band structure. These data provide foundational support for the machine learning computations in this project.

To obtain material data, it is essential to first register on The Materials Project website, obtain an API key, and configure the website interface. In this thesis,

material information for the elements Au, Nb, Ni, Ru, Ta, and Ti was collected. The downloaded data were then imported into Excel to create a foundational database. An overview of the output data is presented in Table 5.1. It should be noted that the collected information extends beyond the parameters listed in the table. Additional factors include work function, energy above the hull, and formation energy, to name but a few.

Table 5.1: Sample Table of Material Data

Formula	Density	Volume	...	Fermi Energy	Total Magnetization
Au	18.03	18.14	...	5.85	0
Ni	9.22	21.14	...	7.99	1.51
Nb	8.45	18.26	...	5.21	4.00E-06
...	...	...	...	...	...
Ru	12.38	27.10	...	8.37	7.00E-07

Some elements may have multiple allotropes. Among all the possible element configurations, only those that have been experimentally observed were selected. Configurations that are feasible only in calculations but have not been experimentally observed were excluded from the dataset for this thesis.

The element properties were then combined with the experimental results, which were the average forming voltages for each experimental group, concluded from more than 220 device tests (Fig. 5.1).

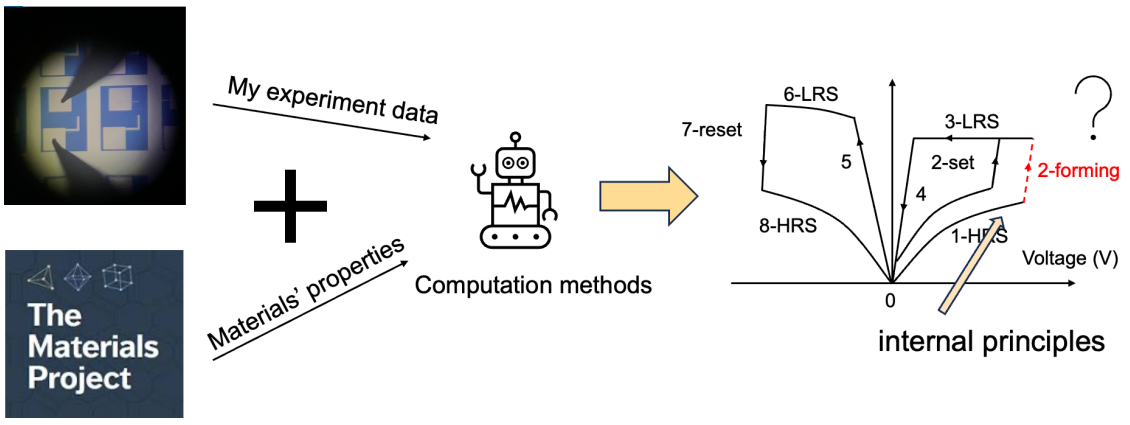


Figure 5.1: An illustration of the analysis workflow.

5.2. Principal component analysis

Principal component analysis (PCA) is a widely used data analysis method where the original variables are linearly combined to form new orthogonal variables, called principal components. These principal components represent the directions of greatest variance [83]. The inter-relationships of the variables are calculated, and by analyzing the principal components, we can extract the most relevant information and simplify complex datasets [84]. An illustration of the PCA method can be seen in Fig. 5.2.

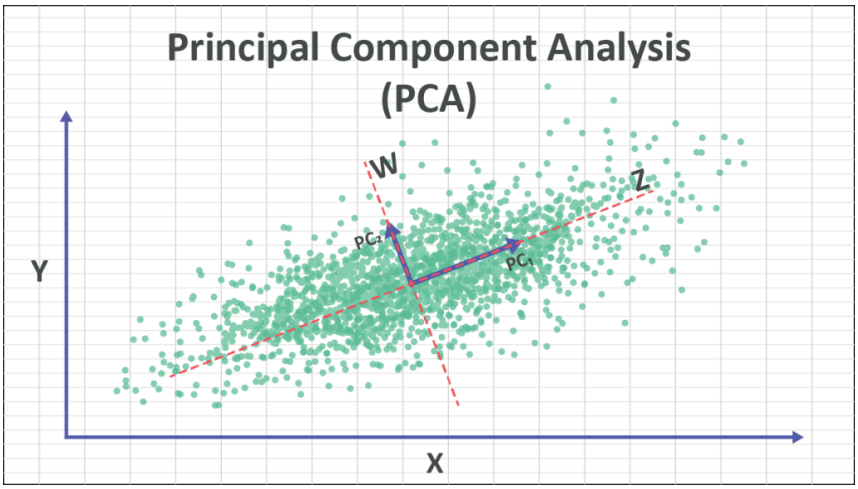


Figure 5.2: An illustration of principal component analysis [85].

In this project, PCA was initially applied to identify feature importances. However, the fitting result was quite unsatisfactory. The mean squared error reached 1.56, and the prediction accuracy was only about 20% with a tolerance of 30%. This poor result might be due to the small dataset. Although 220 data sets seem sufficient for an experiment, they are far from adequate for a statistical model.

5.3. Neural network

The neural network (NN) is inspired by the human brain and is widely applied in artificial intelligence (AI). Neural networks consist of interconnected layers of

nodes, also known as neurons. The neurons in a neural network are connected by weights, which determine the strength and direction of the signals passed between them. Typically, there is an input layer, several hidden layers, and an output layer. When there is more than one hidden layer, the model is referred to as deep learning.

In this thesis, an NN model with two hidden layers, each containing 64 neurons, was built. The two hidden layers were fully connected. Each hidden layer was followed by a 20

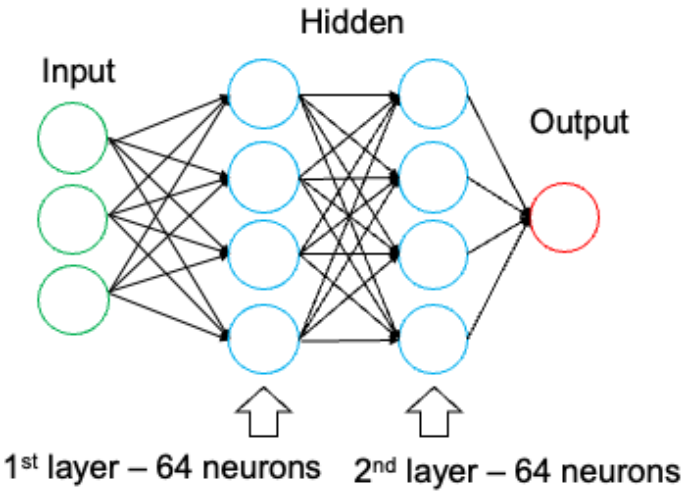


Figure 5.3: Neural network structure illustration.

The model was optimized over 120 epochs. The following Fig. 5.4 depicts the training process, where the loss is described by mean squared error. The training loss indicates the model's performance on the trained data, while the validation loss evaluates the model's performance on unseen data. The decreasing trend of both the training loss and validation loss indicates efficient training of the model.

It was found that using fewer or more epochs led to underfitting or overfitting, respectively. Despite this optimization, the model demonstrated relatively poor performance. The final mean squared error of the model was 1.32, and the accuracy was approximately 60% with a 30% tolerance. This result was better than that of the PCA, but still not satisfactory for the analysis.

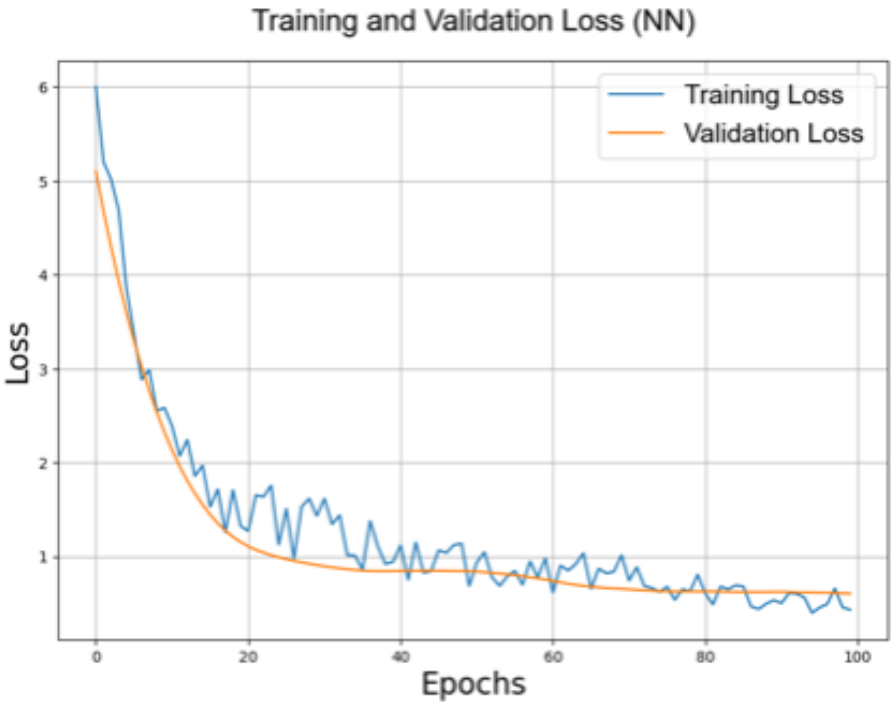


Figure 5.4: Neural network fitting result, where the loss is described by mean squared error.

5.4. Random forest regression

Finally, the random forest (RF), a powerful modeling algorithm, was applied. It was used for the regression task in this thesis with the aim of predicting numerical values.

A decision tree, named for its tree-like structure (Fig. 5.5a), is a widely adopted supervised learning algorithm in which the dataset is split into numerous subsets based on the input features [86]. At each node, a decision is made based on a selected feature, and each branch represents the outcome of that decision.

Random forest regression [87] is an ensemble learning method that operates by constructing many decision trees during training (Fig. 5.5b). Each tree is trained on a distinct subset of the data and makes its own independent prediction. The final prediction is obtained by averaging the predictions of all the decision trees, which increases the model's robustness and provides a more comprehensive estimation of feature importance.

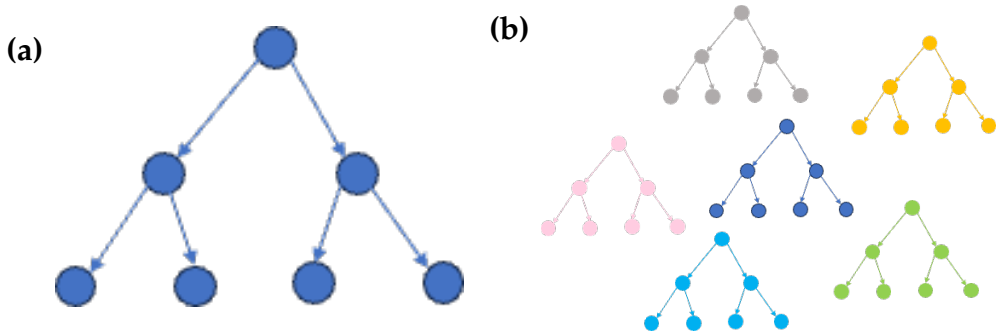


Figure 5.5: Illustration of (a) a decision tree, and (b) a random forest.

For the random forest (RF) regression training, 100 decision trees were utilized [88]. The results from these trees were averaged to produce the final output. Compared to PCA and NN, the RF method yielded significantly better results. The mean squared error for RF was only 0.401, while the accuracy reached 82.4% (with 30% tolerance). A comparison of the three methods is presented in Table 5.2.

Table 5.2: Comparison of results of PCA, NN, and RF methods

Method	Mean Squared Error	Accuracy (with 30% tolerance)
PCA	1.56	20%
NN	1.32	60%
RF	0.401	82.4%

To understand why RF produced the best results, several factors can be considered. First, RF is capable of analyzing non-numeric data, allowing for a more comprehensive input, which improves the output. Second, while neural networks perform well with large datasets, PCA is generally not favored for predictive modeling. Given the relatively small dataset used in this thesis, RF is likely the most suitable method.

5.5. Model interpretation

To understand the trained model, the importance of each feature was extracted. The seven most important features of the bottom metal that determine the forming

voltage are listed in Fig. 5.6.

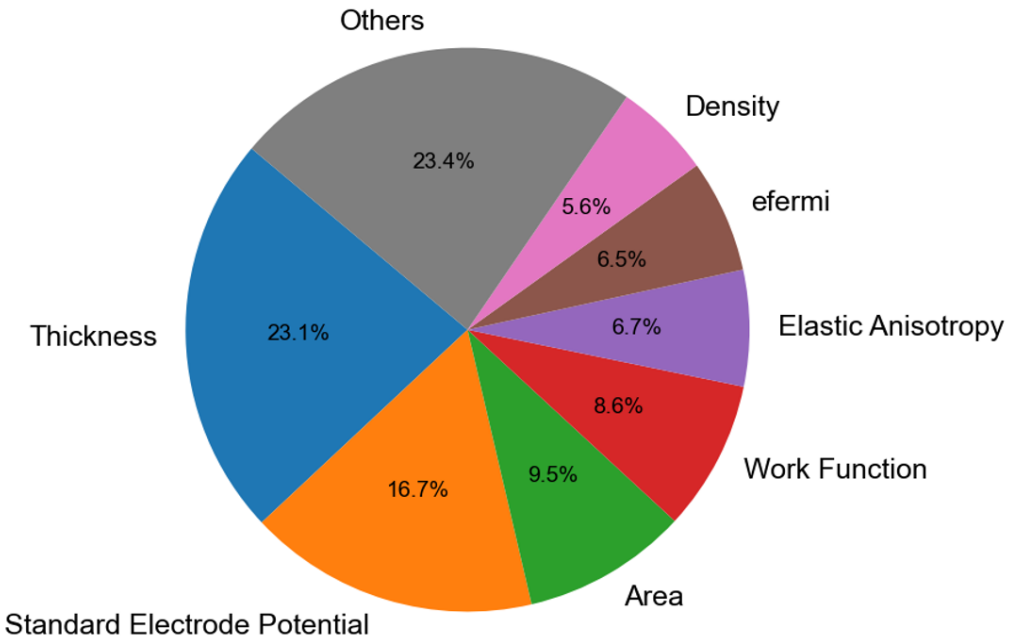


Figure 5.6: Top Seven Important Bottom Metal Features Identified by the RF Model.

The most relevant feature was determined to be the thickness of the bottom metal. This can be understood in terms of the amount of absorbed oxygen. Active bottom metals are expected to react with HfO_2 and introduce oxygen vacancies into the insulator. The bottom metal thickness indicates the amount of metal that may be oxidized by the HfO_2, thereby determining the forming voltage.

The second factor, standard electrode potential, is closely related to chemical activity. Typically, a more negative standard electrode potential indicates that the metal is easier to oxidize. Metals with very positive standard electrode potentials, such as gold, are almost impossible to oxidize. The standard electrode potential details the feasibility of the oxidation process between the insulator and the bottom metal.

Thirdly, the influence of the area can be confirmed by previous studies [89]–[91]. Forming voltage is observed to increase as the devices scale down, which is explained by the reduction of defects [91].

The work function is another important factor. It has been reported that the interface barrier between the insulator and the metal can affect the forming voltage [33]. By selecting an appropriate metal, the barrier can be lowered to minimize the forming voltage (Fig. 5.7), potentially leading to forming-free devices.

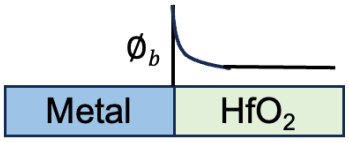


Figure 5.7: An illustration of the interface barrier

5.6. Model verification

To verify the model, 10 nm Ru-based devices were fabricated. These devices were produced using the same process as described in Chapter 3, but with a 10 nm thick Ru layer as the bottom metal. The device structure of the verification group is shown in Fig. 5.8.

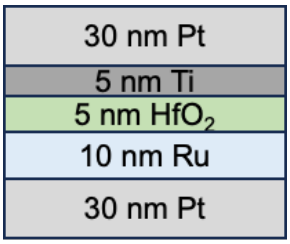


Figure 5.8: 10 nm Ru verification group

The model predicted a forming voltage of 1.2 V for the 5 × 5 μm devices and 1.14 V for the 10 × 10 μm devices, which matched the experimental results well. The measurement results are shown in Fig. 5.8.

The forming voltages for the 10 nm Ru 5 × 5 μm and 10 × 10 μm devices were very close to the predicted values of 1.2 V and 1.14 V, respectively. Hence, the trained model was verified by the experimental observations.

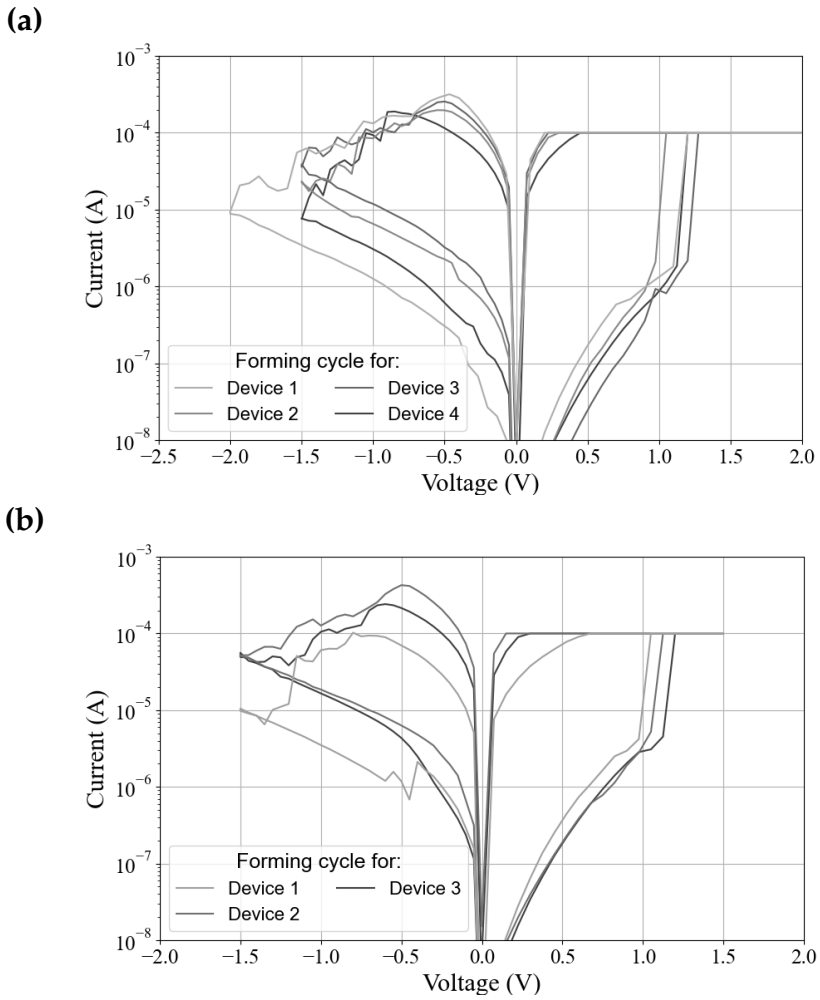


Figure 5.9: Forming voltage for 10 nm Ru devices in (a) 5 × 5 μm and (b) 10 × 10 μm.

6

Conclusion and Outlook

6.1. Conclusion

In this thesis, RRAM devices with different bottom metal layers were fabricated and evaluated. Over 220 devices were measured, revealing that the addition of an inter-layer significantly alters RRAM performance. Notably, forming-free devices were observed, with the rate of forming-free occurrence reaching up to 35% for Ru-based devices. It is understood that chip oxidation in the atmosphere during the fabrication process plays a crucial role.

To investigate the underlying principles and predict the forming voltage, principal component analysis, neural network, and random forest regression methods were employed. The first two methods demonstrated poor fitting results, with mean squared errors of 1.56 and 1.32, and accuracies within a 30% tolerance at 20% and 60%, respectively. The random forest algorithm exhibited the best performance, with a mean squared error of 0.401 and an accuracy of 82.4% within a 30% tolerance.

Feature importance analysis was conducted to interpret the random forest model. The top four important features of the bottom metal were identified as thickness, standard electrode potential, area, and work function. It was explained that thickness determines the amount of reacted oxygen, standard electrode potential indicates the feasibility of oxidation, area reveals possible defects underneath the electrode, and work function affects the interface barrier. It is important to emphasize that forming voltage is influenced by multiple factors, making it a complex parameter.

The model was ultimately verified using 10 nm Ru devices. Experimental data from both 5 × 5 µm and 10 × 10 µm 10 nm Ru devices matched the prediction results closely, demonstrating the model's effectiveness.

This work demonstrates the feasibility of combining experimental approaches with modeling predictions.

6.2. Outlook

However, this thesis has certain limitations. First, all devices were handmade, which introduces device-to-device variation due to the less stable and reliable nature of human operation compared to automated industrial processes. This variation is reflected in the error bars in Fig. 4.5a and Fig. 4.5b. Second, despite testing over two hundred devices, the dataset remains relatively small, reducing the reliability of the trained models. Third, it was observed that for some devices, the forming voltage could be either negative or positive, indicating that averaging the forming voltage does not perfectly reflect the RRAM's working mode or the forming operation. Lastly, machine learning methods, such as neural networks and random forests, are mathematical algorithms that lack physical meaning. Developing a physics-based model to analyze and understand the forming process can improve the model's reliability.

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