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Reduced Calibration Error Employing Parametrized EM models and DC Load Extraction

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***Abstract* — In this contribution we present an approach to reduce the error arising from the variations of the lumped load, due to process spread, in probe level calibrations. First, full-wave electromagnetic (EM) simulations are employed to generate the nominal standard responses, then a parametric EM simulation of the load structure is used to generate a parametrized model of the standard. The approach is tested using a Short-Open-Load-Reciprocal calibration algorithm and an impedance standard calibration substrates developed on a 150 mm Quartz wafer (400 µm thick). In this process the high fidelity of the lateral dimension of the fabricated structures, realized using IC Photolithography, allows to confine the variations of the load response to only the thin-film resistor thickness spread. The DC response of the load, measured during the calibration step, is used to identify the specific RF response of the probed load from the parametric model. A complete analysis using full-wave EM simulations accounting for process variation is presented together with a set of experimental data up to 67GHz.**

***Index Terms* — Vector Network Analyzer, calibration, on-wafer, probe-level, Short Open Load Reciprocal, SOLR, Quartz.**

I. Introduction

First-tier probe level calibrations using impedance standard substrates (ISS) are often used when pad level measurement of the device under test (DUT) are required, and the area penalty (cost) or the development time to integrate calibration structures in the same environment of the DUT, cannot be afforded.

The current development of commercial applications operating at frequencies above 30GHz, i.e., 5G mm-wave and 60GHz WAN, to name a few, and the need for accurate measurements in the range from RF to mm-wave, is pushing the accuracy requirements of broadband calibration approaches (i.e., SOLR, LRM, etc.). At these frequencies, the usage of classical ISS used in the RF bands (i.e., below 6GHz), are starting to show reduced accuracy due to unwanted substrate modes, as was shown in [1] and poor model definitions, discussed in [2]. The authors have already presented in [3] an accurate ISS realization employing a technology based on a CMOS process line, realized on Quartz wafers to reduce the effect of unwanted propagation modes, and in [4] a modelling strategy of the nominal calibration artifact via full-wave electromagnetic (EM) simulations. Nevertheless, the high accuracy of CMOS process lines, capable of providing high consistency in the lateral features of the manufactured structures, still suffers from the height variation of the layers, mostly in the extremely thin films (i.e., circa 100nm) required to realize the reference resistors (Fig1). This process spread leads to a considerable error in the calibration, when these variations are not accounted for in the loads models, or corrected for via trimming, as done in commercial ISS. In this contribution, we consider a parametrized EM model of the load response obtained by applying a varying thickness of the thin-film layer. During the calibration procedure (i.e., without requiring extra probe touchdowns), the short (acquired to remove the effect of the bias-tee and cable resistance) and the load DC resistances are used to acquire the specific DC value of the load being measured. This value is then used to identify the response, in the parametric model, of the specific load used in the calibration procedure.

The paper is organized as follows, first, the parametric EM model of the load and the procedure to realize the DC load compensation is described. Then an EM analysis of the calibration errors arising from process variations is introduced, and the proposed approach is benchmarked on synthetic data. After, the experimental setup and the Quartz based ISS substrate is presented and finally a set of measurement data employing the load compensation technique is presented.

II. Load parametric EM model

The EM simulations of all the calibration standards are carried out in Keysight ADS.

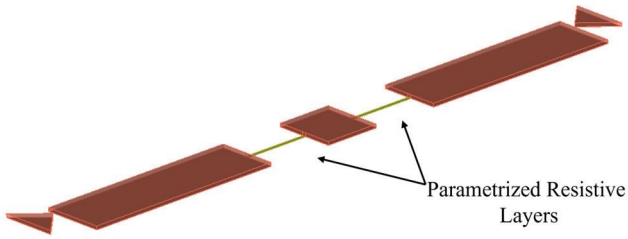

Fig. 1: EM model of 1-port Load standard in Advanced Design System (ADS) - Keysight® Momentum environment.

The gds file of the fabricated structure is imported (Fig. 1) in the EM simulation environment (2.5D simulation in Advanced Design System (ADS) - Keysight® Momentum), and the technology layer stack is included to provide the height and electrical parameters (nominal) of the various layers. Direct feed ports with the same spacing of the intended GSG probe are used to excite the structure. In Table 1 the parameters (nominal and variations) used for in the EM simulation are shown. The variation range was extracted using an optical microscope for

the lateral dimensions and using a Veeco Dektak 8 stylus profiler for the height. The effective permittivity is computed experimentally using a measurement on a thru and a line.

Table 1: Parameters used in modelling calibration structures.

	Nominal value	Mean measured value	Standard deviation
Top metal thickness	2800 nm	2878.2 nm	≈2%
Resistive layer thickness	100 nm	109.7 nm	±8%
Lateral dimensions	-	-	<1%

A parametric sweep of the thickness of the layers used to map the load standard is carried out to include the process spread of the technology (i.e., ±1% from nominal in thickness of the metal layer and ±8% on the resistive layer). The EM simulations are performed over the intended frequency range and parametric variation. The parametric load response is indexed by its DC overall response (i.e., parallel of the thin-film resistors in the GSG configuration of Fig. 1), see Fig. 2.

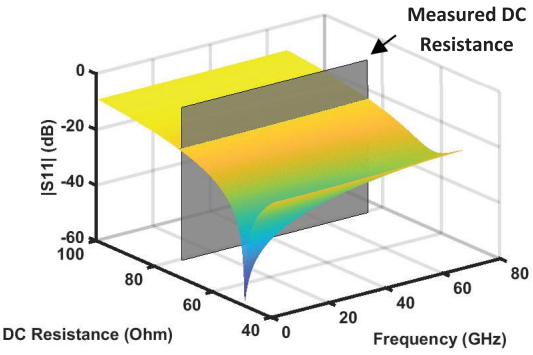

Fig. 2: Simulated reflection coefficient of Load standard versus frequency and thickness of thin film layer.

III. Load Compensation Approach – Synthetic Data

In order to study the viability of the load compensation approach, a simulation test bench, realized in ADS, employing a Montecarlo perturbation of the technology variation parameters, was considered, see Fig. 3. The simulation test bench includes all the standard devices used in the SOLR calibration and propagates the error in the response due to the height variation of the technology layers controlled by Gaussian distributed independent variables, see Fig. 4.

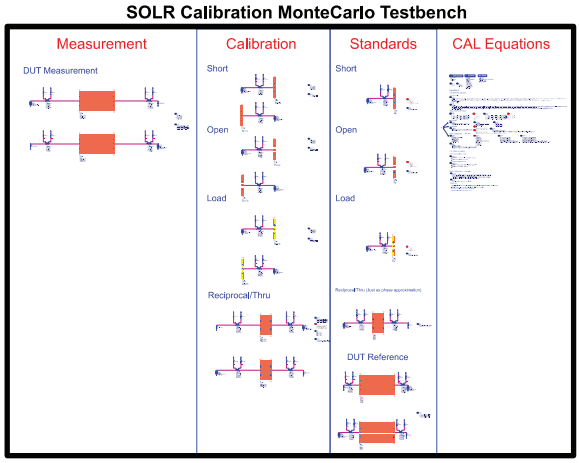

Fig. 3: SOLR Montecarlo testbench simulation in Keysight ADS.

An independent line is used as a reference device on which to apply the different calibration error sets derived from the 2250 perturbations. Note that on each structure a finite number of perturbations are applied, i.e., short (3 variations), open (3 variations) and load (250 variations) .

The calibration procedure, employs independent (stochastic) variables at each structures allowing to obtain a larger number of independent variations, i.e., 2250.

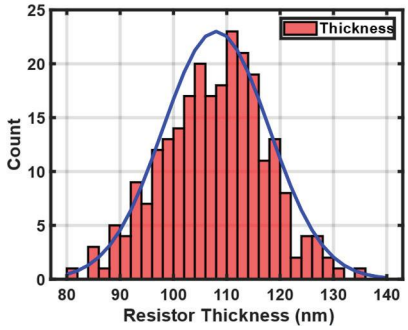

Fig. 4: Resistor height distribution of standards used in Montecarlo simulation

In order the quantify the performance of each of the calibration sets computed the worst case error bound (WCB) metric is used as presented in [5], and shown in eq. 1.

$$WCB = max\left|S'_{ij} - S_{ij}\right| \quad (1)$$

Where S' is the reference scattering matrix of the verification line (i.e., EM simulated), and S is the scattering matrix resulting from DUT after correction by each calibration sets and $i,j \in [1,2]$. The WCB when the load variation due to technology variation is not accounted in the standard model, is shown in Fig. 5.

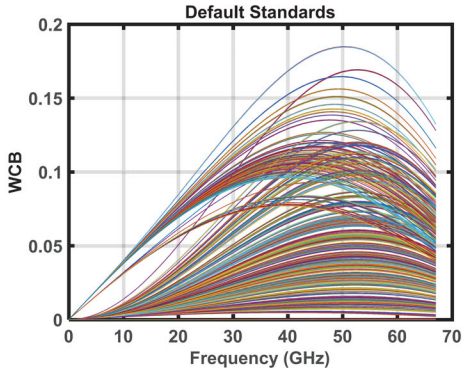

Fig. 5 Worse case error bound of independent line corrected using default standard definitions.

The plot shows a large variation of the calibration quality leading to a larger uncertainty in the calibration accuracy.

In the proposed load compensation method, in every load in the various calibration sets we first identify the load DC resistance value and then extract from the parametric response of Fig. 2, the corresponding frequency dependent response of that specific load. When performing this procedure and then applying the derived calibration sets to obtain the WCB metric we obtain the results shown in Fig. 6.

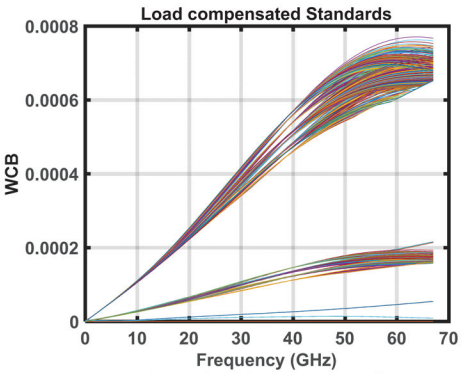

Fig. 6: Worse case error bound of independent line corrected using load compensated standard defenitions.

As can be seen in Fig. 6, the residual calibration error is greatly reduced and is now only derived from the other technology variation parameters, i.e., aluminum thickness variation.

IV. Experimental Setup and Quartz ISS

To experimentally validate the proposed approach, the measurement of a set of calibration devices (i.e., short, open and reciprocal) with a large number of loads across various dies and wafers (i.e., quartz wafer) was performed using 100 µm GSG Infinity probes from Formfactor® on a manual probe station. The measurement setup consists of a Keysight N5227A - PNA Network Analyzer and a E5270B parameter analyzer connected using the VNA internal Bias T (Fig 7). In the measurement procedure, after acquiring S-parameters on the load and short standards, also a DC measurement is performed to compute the Load standard's resistance.

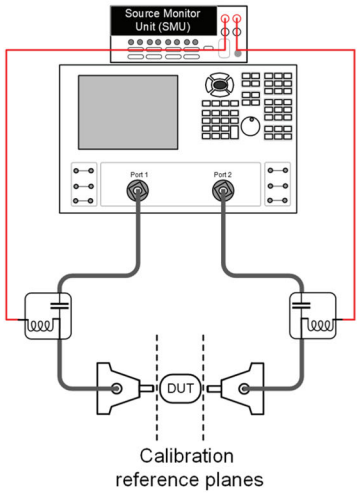

Fig. 7: Simplified schematic of the measurement setup including VNA, SMU, Bias Tee and Probes.

The calibration kits are integrated on a 400 µm Quartz wafer shown in Fig. 8.

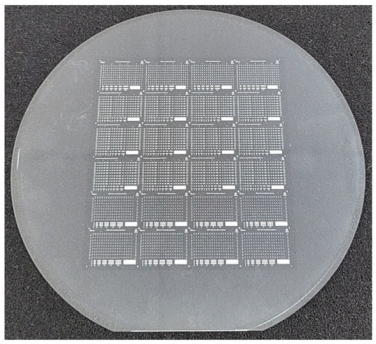
Fig. 8: Fabricated Quartz wafer.

V. Preliminary Experimental Results

Using the setup described in Section IV the data from one set of open, short and thru, combined with sixteen different loads was used (i.e., loads located on two wafer and four dies from each wafer). Selecting only one set of short, open and thru was done in order to minimize the impact of contact resistance variation and probe placement error and to highlight the impact of the load compensation technique. After, the analysis as described in Section III was performed, i.e., the different load artifacts are combined with the single set of short, open and thru to generate 16 sets of calibration error coefficients.

A 1320um line was employed as a verification device and the EM simulation of the line was used as the reference data to compute the WCB metric.

Fig. 9 and Fig. 10 present the WCB metric for the nominal standard definition case and the load compensated one, respectively.

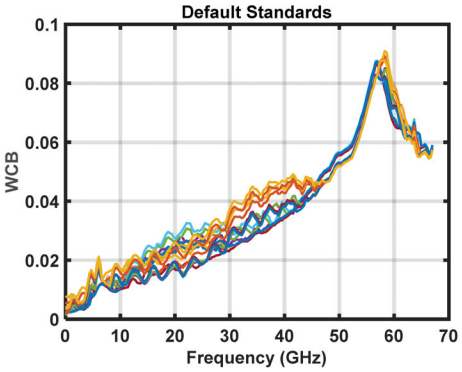

Fig. 9: Worse case error bound of independent line measurement corrected using default standard definitions.

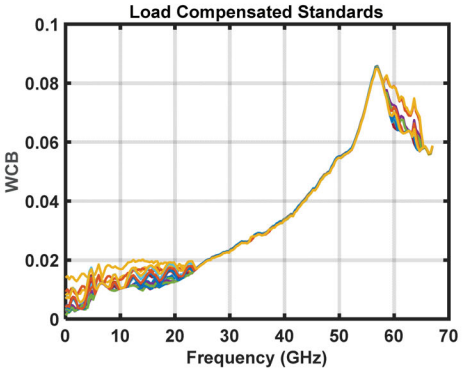

Fig. 10: Worse case error bound of independent line measurement corrected using load compensated standard definitions

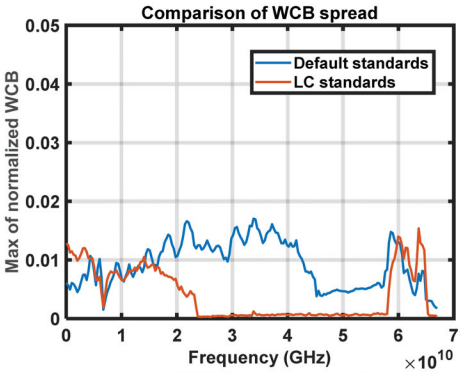

Fig. 11: Direct comparison of WCB spread for the nominal definition case (Fig. 9) and the load compensated one (Fig. 10).

Fig. 11 presents the reduced spread of the WCB metric when the load compensation approach is employed. The current limited dataset and reduced variation of the used load, keeps the improvement of the proposed technique limited. Moreover, the usage of a full manual probe station introduces a probe position error (compared to the EM port position definition) which linearly increases with frequency .

VI. Conclusion

In this paper the reduction in calibration accuracy due to (untrimmed) load variation due to process spread was addressed by using an EM parametric load model that can be indexed via the load DC resistance.

The method validity was supported by a Montecarlo simulation on EM devices where a perturbation comparable to process variation was applied.

Measurements shows a reduced spread in the WCB of resulting calibration when the proposed method is applied.

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