MASTER THESIS

AN IR-UWB PULSE GENERATOR BASED ON SWITCHED CAPACITORS RF-DAC

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Master of Science

in

Electrical Engineering

By

Xiao WANG

Supervisors:

Dr. Ir. Xin He (NXP)
Prof. dr. L. C. N de Vreeede (TU Delft)
Dr. Morteza Alavi (TU Delft)

Thesis Committee Members:

Dr. Ir. Xin He (NXP)
Prof. dr. Kofi A. A. Makinwa Vreeede (TU Delft)
Prof. dr. L. C. N de Vreeede (TU Delft)
Dr. Morteza Alavi (TU Delft)

This work is performed in NXP
High Tech Compus 46
5656 AE Eindhoven
Netherlands

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ABSTRACT

Since the release of the ultra-wideband (UWB) wireless indoor/outdoor standards by the U.S. Federal Communication Commission (FCC) in 2002 for the frequency range of 3.1-10.6 GHz, the impulse radio ultra-wideband (IR-UWB) wireless communication technique is rapidly developing in the last two decades. This technique dramatically increases the data rate and improves the location accuracy.

Due to a short duration of the UWB pulse, the precise location is obtained by measuring the delay of the transmitted signal, typically within the centimeter-level accuracy. A direct digital-to-radio-frequency IR-UWB pulse generator is a superior approach compared to the conventional analog-intensive configuration to reduce the system complexity, improve the functionality, frequency agility, and lower the cost.

This master thesis addresses the design and characterization of an IR-UWB pulse generator for car ranging applications. The generated UWB pulse has a 6.5 ns width with a 1GHz 30dB-bandwidth, which is compliant with the stringent spectral requirements of outdoor standards. The maximum pulse repetition frequency is 125 MHz. Moreover, the carrier frequency of the IR-UWB pulse covers both 6.5 and 8 GHz bands, which expands its regional commercial coverage. This IR-UWB pulse generator has been fabricated in a 40 nm Global Foundries LP CMOS process.

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1

INTRODUCTION

IMPULSE radio ultra-wideband (IR-UWB) technology is utilized worldwide for short-to-medium range wireless communications since the FCC permits the unlicensed operation within 3.1 GHz to 10.6 GHz [1-3]. This approach is based on the emission of short-duration pulses, which meet the ultra-wide spectrum masks that are regulated for commercial use. Accordingly, the high precision of the mutual distance is obtained by measuring the Time of Arrival (ToA) [4] of the pulse, due to which both outdoors and indoors localization systems can be realized on mobile terminals. Moreover, operating in a burst-like mode, the low duty-cycle makes the low power consumption an appealing character on power-constrained applications. By exploiting such advantages that IR-UWB technology can provide, IR-UWB has drawn much attention from the researchers as well as industries. Chosen by IEEE 802.15.4a task group, IR-UWB technique has now been a candidate for delivering communications and high-precision ranging [5]. Generally, a pulse generator is mandatory for IR-UWB systems to produce the short pulses that are compliant with spectrum masks. In this chapter, an overview of UWB definition and its application fields is presented in Section 1.1. Besides, mainstream architectures of IR-UWB pulse generators will be introduced in Section 1.2. Section 1.3 reveals the motivation and the targeted specifications of this project.

1

1.1. IMPULSE RADIO ULTRA-WIDE-BAND

1.1.1. UWB DEFINITION

As shown in Figure 1.1, UWB is a form of bitterly wide spread spectrum where RF energy is scattered over several octaves of the frequency spectrum, which also covers most narrow-band systems. Consequently, the emitted signal power generated by UWB transmitters is low enough to avoid interferences with others. Compared with conventional radio signals, UWB signals even can be regarded as imperceptible random noises. UWB

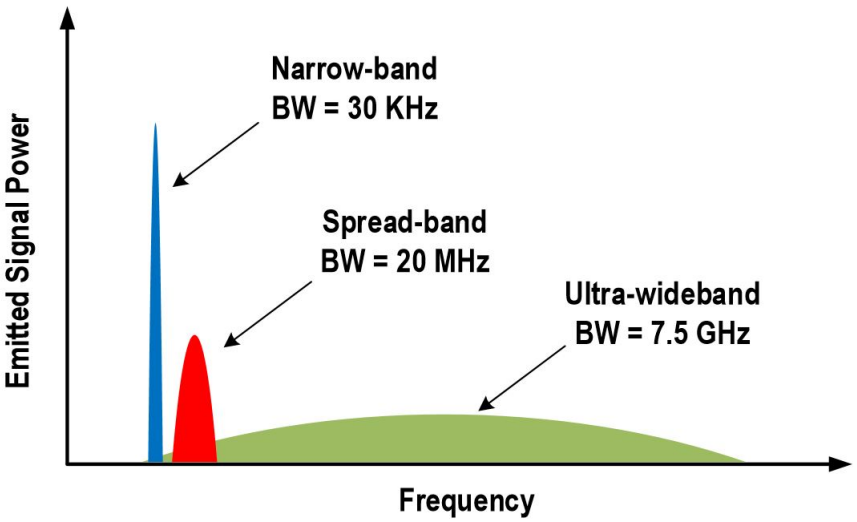

Figure 1.1: Bandwidth comparison of different types of wireless systems

is first defined by the FCC [6]. According to the FCC proposal, the communication system whose fractional bandwidth is equal to or greater than 20% of the frequency of the local oscillator, f_{LO}, or the emitted signal bandwidth occupies 500 MHz or more can be referred as the UWB system. The formula proposed by the FCC for calculating fractional bandwidth is as follows:

$$B_f = B/f_c = 2 \cdot \frac{f_h - f_l}{f_h + f_l} \tag{1.1}$$

where B_f is the fractional bandwidth, B is the emitted signal bandwidth, f_c is the center frequency, f_h is the upper frequency of -10 dB emission point and f_l is the lower frequency of -10 dB emission point. As shown in the equation 1.1, the fractional bandwidth is the ratio of signal bandwidth (-10dB) to the center frequency of transmission i.e., the average value of the upper frequency and the lower frequency. The reason why the FCC uses a -10 dB bandwidth rather than -20 dB bandwidth that is adopted in the defense advanced research projects agency (DARPA) is the very low power spectral density limit regulated by IEEE 802.15 standards [5], [7]. Ordinarily, it may not be possible for UWB systems operating so close to the noise floor to measure 20 dB bandwidth in most wireless communication cases.

1.1.2. UWB APPLICATIONS

IR-UWB characteristics make it an attractive and appropriate approach for imaging systems (like medical imaging, ground penetrating radars), communication systems (indoor monitoring systems and outdoor security ranging systems), and vehicular radar systems [8]. The IR-UWB characteristics are summarized as follows:

- Low power, low cost, and high data rate.
- Co-existence capability of multi-path.
- High precision based on the nanosecond order resolution.

Briefly, what UWB targets to evolve are those two main realms of wireless communication systems:

- High data rate and short range communication: The high date rate capability of UWB makes it an alternative to bluetooth technology. Built on this, wireless personal area network (WPAN) combined with surrounding entertainment devices can be established. Besides, wireless sensor/Ad-hoc networks can also be served by IR-UWB.
- Low data rate and medium range communication: Larger range and low date rate applications can also benefit from UWB technology, such as habitat monitoring wireless sensor networks and tactical communications like intrusion radars [8].

1.2. IR-UWB PULSE GENERATION APPROACHES

In an IR-UWB system, the UWB pulse generation, including the pulse-shaping and the subsequent RF modulation, is extremely challenging. The primary issue in the UWB pulse generation is related to a trade-off between circuit complexity and the stringent spectrum-regulated requirements imposed by both the FCC and ETSI [6] [9]. In recent decades, there have been numerous efforts exploring low-power, low-cost, less complicated UWB pulse generators [10-15]. Currently, three main categories dominate the IR-UWB pulse generator designs that are presented as follows:

1.2.1. CONVENTIONAL, ANALOG-INTENSIVE APPROACH

Similar to conventional narrow-band transmitters, the first approach is to initially generate a digital baseband UWB pulse, convert it to an analog signal using a digital-to-analog converter (DAC)/pulse modulator. This analog baseband UWB pulse is eventually up-converted into the designated UWB-RF frequency band using a local oscillator (LO) clock as depicted in Figure 1.2. Although doing so, the digital baseband UWB pulse can be easily replicated as RF as expected, the UWB system due to the need for an extra DAC and up-conversion mixer is not energy efficient. It is typical of UWB systems to work at several gigahertz frequency range, hence, those intermediate stages working at such high frequency further exacerbate the energy burden especially for battery-powered applications. Besides, the related LO signal is generated using a phase-locked loop (PLL) which increase the complexity of the UWB system. As stated earlier, the UWB pulse entails a broad bandwidth (experiences sharp transition). The start and stop time

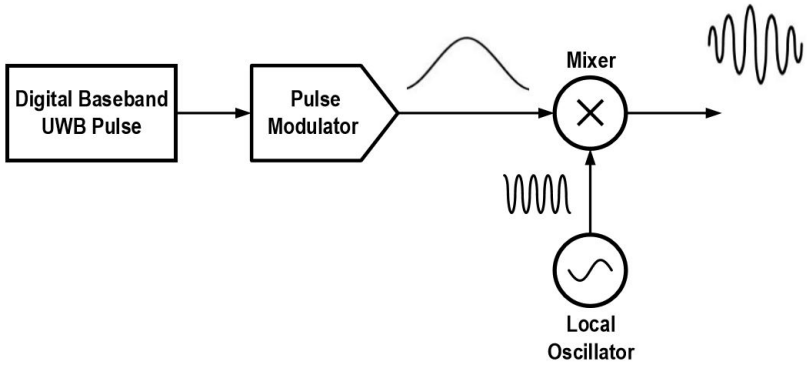

Figure 1.2: A conventional analog-intensive UWB pulse generation approach

of the PLL, however, limits the pulse width of the UWB signal causing spectral regrowth [10], [16]. In general, the drawbacks of this conventional architecture mentioned above drive the need for an advanced energy-efficient pulse generation technique.

1.2.2. PULSE-SHAPING-BASED APPROACH

The second UWB pulse generation approach is based on pulse shaping which is realized in two phases. In the first place, a relatively coarse UWB pulse, typically not satisfying the spectral requirements, is presented by a short pulse generator. Afterwards, a passive pulse-shaping filter is applied to obtain a spectrum-desired UWB pulse [17-18]. The benefit of this architecture is the simplicity of the structure compared with the conventional UWB pulse generator, only a passive band-pass filter is applied after the short pulse generator. However, integrating on-chip passive components such as inductors and transmission lines, due to their large occupied chip area, is expensive and should be avoided. On the other hand, the low quality factor of these passive components would result in significant linearity and efficiency degradation, which are crucial for a UWB-pulse generation. In consequence, all the issues mentioned above lead to the

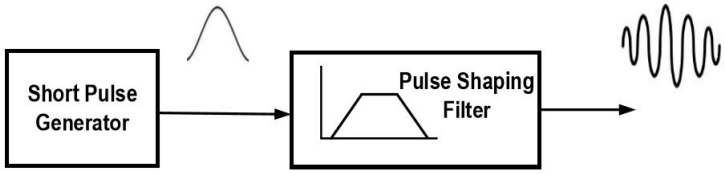

Figure 1.3: A pulse-shaping-based UWB pulse generation approach

implementation of off-chip filters that are adopted by most pulse-shaping UWB pulse generators. Once fabricated, the filter is fixed so that only one particular UWB pulse will be generated, which is taken as an immense obstacle for tuning capability. Usually, reconfigurable pulse shapes are desired for different application scenarios. Recently, to obtain flexible UWB pulses, passive filters are replaced by active FIR filters [18-19], which increase the power consumption significantly.

1.2.3. DIGITAL-INTENSIVE APPROACH

From the previous analysis, a fully reconfigurable pulse generator with low complexity is desired. Ideally, a high-speed DAC with high resolution could be a promising option to synthesize arbitrary waveforms [21]. Naturally, a radio frequency DAC (RF-DAC) is suit-

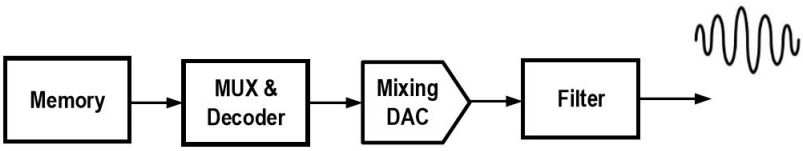

Figure 1.4: A digital-intensive UWB pulse generation approach

able candidate for this role [22], acting as a core part of the third UWB pulse generation approach. Moreover, a memory is needed for defining and storing the reconfigurable digital baseband pulse information. Consequently, a direct baseband-to-RF conversion is achieved, in which it eliminates the intermediate stages in the conventional analog-intensive RF transmitter (TX) chain. Direct-RF synthesis dramatically simplifies the TX architecture. Those two advantages over previously mentioned pulse generator schemes make RF-DAC-based architecture a preferred choice. However, RF DACs demand a quite high sampling rate, which not only complicate the DAC design but also digital logics. As a consequence of adopting higher sampling clock, the system efficiency of the RF-DAC-based UWB pulse generator architecture is degraded. Moreover, due to rigorous spectral requirement imposed by the FCC, it is preferable to employ linear RF-DAC architecture.

1.2.4. MOTIVATION AND TARGET SPECIFICATION

According to the aforementioned design challenges of the three types of UWB pulse generators in Section 1.2, an advanced UWB pulse generator needs to be directed towards possessing the characteristics as follows:

- Low structure complexity that is energy-efficient.
- Reconfigurable capability for different types of UWB pulses.
- Spectral-requirement compliance imposed by FCC.

1

In this thesis, a digital-intensive UWB pulse generator based on a switch-capacitor RF-DAC is proposed. The generated UWB pulses are well-compliant with the stringent out-of-band spectral requirements and have high peak amplitudes. Moreover, the proposed UWB pulse generator is applicable to multi-mode configuration which can cover both 6.5 and 8 GHz frequency bands. The contribution of this master project is adopting a first-order hold (FOH) interpolation filter as part of our research, which will be introduced in Chapter 3. The targeted specifications of this thesis project are listed as below:

Table 1.1: Targeted Specifications

Parameter	Specifications	Unit
Peak Output Power	>15	dBm
Carrier Frequency Range	6.5 - 8	GHz
Bandwidth	1	GHz
Out-of-band Supression	30	dBc

2

Radio Frequency Digital to Analog Converter

A radio-frequency digital-to-analog converter (RF-DAC) is a device that directly converts the digital code input into an analog output signal at radio frequency [22]. The direct baseband-to-RF conversion greatly outperforms traditional RF transmitters as discussed in Section 1.2. Apart from this, high-speed and high-resolution conversion provided by RF-DACs paves the way for the precise amplitude modulation. A mixing-DAC is the core part of the proposed pulse generator, the basics of DACs are introduced in Section 2.1 while the mainstream high-speed DACs are described in Section 2.2.

2.1. General Considerations of DACs

The theoretical ideal transfer function for a DAC is a series of discrete points that can be connected together to form a straight line, of which the start position is typically the origin point in the coordinate system. Roughly, the DAC can be regarded as a digitally controlled potentiometer whose output is part of the full voltage scale, decided by the input code. However, practical conversion accuracy of the DAC is affected by static errors caused by non-ideal circuit elements in the actual implementation, as well as dynamic errors. Generally, those static errors are summarized as follows: offset error, gain error, integral nonlinearity (INL) and differential nonlinearity (DNL). Besides, dynamic performances of a DAC are evaluated by widely-used specifications such as spurious free dynamic range (SFDR) and the third inter-modulation distortion (IMD3) , which indicate the system linearity that is crucial in RF communication [8], [23].

2.1.1. Offset and Gain Error

As shown in the Figure 2.1 (a), the definition of the offset error is the measured difference between the nominal offset point and the actual one where the offset point is the step value of the analog output when applying zero digital input signal to the DAC. Assuming that only the offset error is counted in conversion, the actual transfer function can be

considered as the mutated ideal transfer function after a translation in y-axis. From this perspective, the offset error shifts all points at the output from what would be the ideal transfer function by the same amount, which can either be positive and negative.

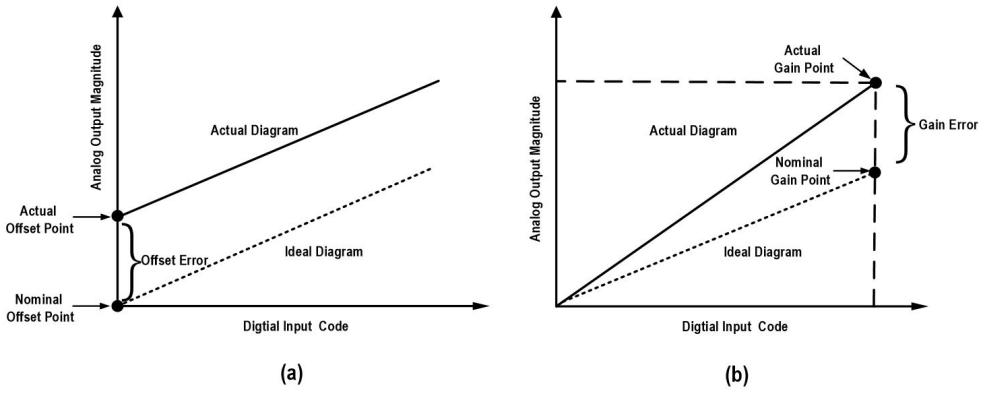

Figure 2.1: (a) Offset error; (b) Gain error.

The actual diagram in Figure 2.1 (a) can be expressed in the form of simple formula as:

$$y = k \cdot x + b \tag{2.1}$$

where the x is the discrete digital input code and the y is the discrete analog output. Obviously, the b represents the offset error. Covering the linear operating region of the DAC with a consistent value, offset error will be compensated in general by trimming, which is adding (or subtracting) the same value to the DAC's input.

Compared with offset error which is an extra "b" interference, the gain error is related to the additional deviation of k, the slope of ideal transfer function. The gain error, as shown in Figure 2.1 (b) is defined as the difference between the nominal gain point and actual gain point on the transfer function assuming the offset error has been calibrated to zero. In a similar way, the gain point is the step value when the digital input is full scale. Also, gain error can be calibrated out both in hardware and software.

$$LSB = \frac{FSR}{2^N - 1} \tag{2.2}$$

Typically, the amount of gain error is measured in least significant bits (LSBs) or as percent full-scale range (FSR) of the DAC. So does offset error. The LSB is defined in the equation 2.2, where N it the maximum bit number of a DAC.

2.1.2. DNL AND INL ERRORS

The differential nonlinearity (DNL), as shown in Figure 2.2(a), is the deviation of an actual analog output step height from the ideal value of 1 LSB. Usually, DNL is expressed in fractions of LSB, as shown in the equation 2.3.

$$DNL = \frac{segment - LSB}{LSB} \tag{2.3}$$

where the segment is defined in the equation 2.4, which is the n^{th} output step size.

$$segment[n] = V[n] - V[n-1] \tag{2.4}$$

Ideally, DNL error would be zero if the step height is exactly 1 LSB. In reality, however, each output step between a pair of adjacent input codes has a corresponding DNL error. Particularly, a special attention is paid to a case that any DNL is more negative than -l LSB will result in a nonmonotonic transfer function, which means that the analog output becomes smaller when increasing the input code. For the amplitude modulation used in a pulse generating, this is undesired.

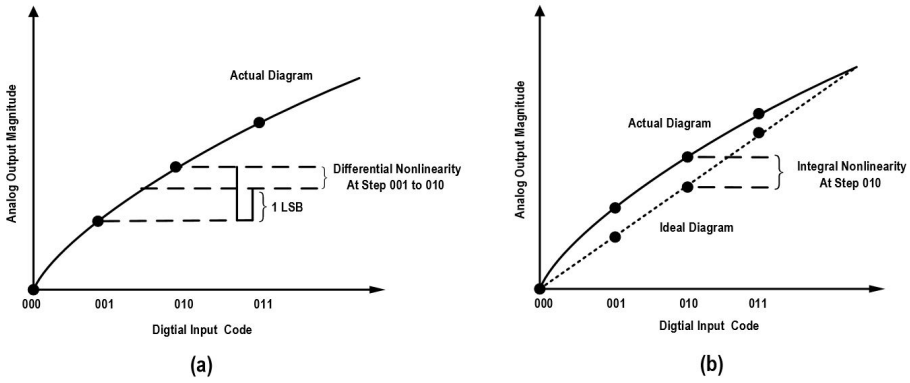

Figure 2.2: (a) DNL error; (b) INL error.

The INL error shown in Figure 2.2 (b) is the deviation of the values on the actual transfer function from a straight line, which is normally the line drawn between two ending points of the transfer function with nullified gain and offset error. In an alternative way, this line can be defined as a straight line which is drawn so as to minimize these deviations. Nevertheless, the first definition is widely-adopted because it can be verified directly.

$$INL[n] = \sum_{i=1}^{n} DNL[i] \tag{2.5}$$

In conclusion, INL error is the summation (integration) of all DNL errors of each step between start point and the calculating point as shown in the equation 2.5.

2.2. STATE-OF-THE-ART OF CIRCUITS USED IN RF-DACS

For sampled data systems such as DACs, in order to have inherently linear conversion, the discrete-time information which is derived from the digital code needs to be hold in one specific analog signal. Whether the analog signal is in the form of voltage or in the form of current, the circuits are divided into voltage-mode or current-mode circuits. In high-speed applications, the switched-current (SI) technique is always utilized for current-mode circuits while the switched-capacitor (SC) technique is applied for voltage-mode circuits [23].

2.2.1. SWITCHED-CURRENT BASED RF-DAC

A basic architecture of a binary weighted switched-current RF-DAC, or equivalently defined as a current-steering DAC is shown in Figure 2.3. By controlling the input bits which determine the on or off state of the switches, the amount of final output current depends on the number of turned on switched-current sources. These current sources can be implemented as either of a binary-weighted configuration using current mirror technique or as a thermometer structure employing unary current sources. Figure 2.3

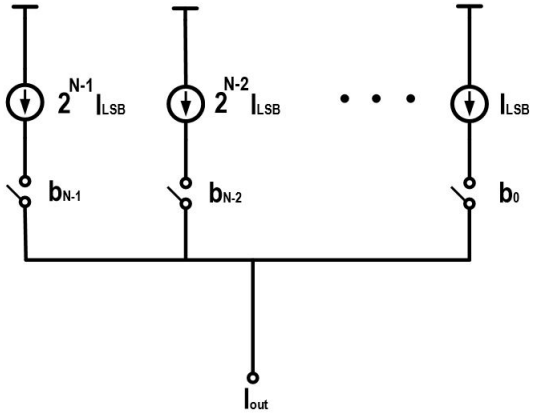

Figure 2.3: Current Steering RF-DAC

depicts the binary-weighted switched-current RF-DAC with N bit resolution. The key advantages of current steering circuit are the high speed due to the current-mode operation and its superior spectral purity due to inherently linear digital-to-analog conversion. While migrating to the lower CMOS technology nodes due to diminishing voltage headroom and smaller intrinsic device output resistance, the current source performance significantly degrades. This signifies that the switched-current RF-DAC configuration is extremely sensitive to the device mismatches which entail glitches and inferior spectral purity of switched-current RF-DAC. Note that this situation will further intensify when a high resolution (larger dynamic range) is postulated. Besides, a high-resolution/high-speed switched-current RF-DAC can even be nonmonotonic. Moreover, the output impedance of the current-steering DAC is input-code-dependent, caused by the limited unit current source output impedance [22-24].

2.2.2. SWITCHED CAPACITOR BASED RF-DAC

To some degree, the general idea of binary-weighted switched-capacitor RF-DAC shown in Figure 2.4 is similar to switched-current one as mentioned above. Briefly, the amplitude of the voltage source is digital controlled by input binary codes, which is based on a precise-ratio capacitors array. Actually, the switched-capacitor RF-DAC combines a class-D PA with a capacitor array working as a voltage divider, achieving a highly-efficient and spectrally-clean direct-to-RF conversion. Those capacitors in the array share a common top plate while each bottom plate can be switched between supply voltage and

ground purposely. Applying Thévenin equivalent, the voltage source amplitude seen from output direction is a fraction of supply voltage, which is proportional to the ratio of the switching capacitance over the total capacitance. Determining the number of switching transistors, the input digital code can further control the output voltage amplitude, which achieves the digital-to-analog conversion [25-26]. Note that in contrast to

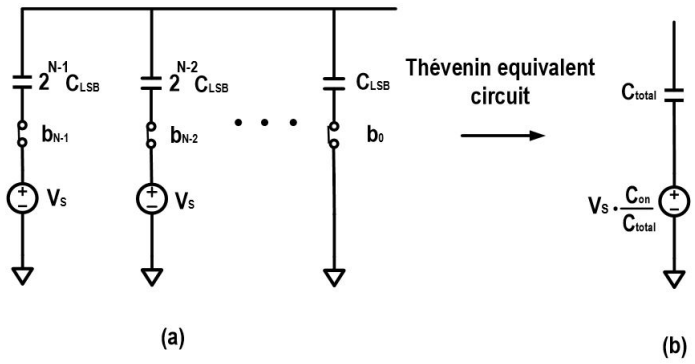

Figure 2.4: Binary-weighted Switched-Capacitor based RF-DAC

the current sources, the CMOS switches benefit from technology scaling. Thus, it is logical to adopt RF-DAC configuration that employs only CMOS switches and passive components such as capacitor that are digital friendly devices. In other words, this configuration has superior input-code-amplitude to output amplitude (AM-AM) performance compared to switched-current counterpart. More details will be described in Chapter 3.

3

A Switched Capacitor RF-DAC Design

Superior linearity and efficiency performance given by the switched-capacitor RF power amplifier proposed in reference [25] makes it competitive architecture for RF-DAC-based UWB pulse generators. Benefiting from scaled CMOS process, smaller parasitics enable faster switching operation, which facilitates operation at higher frequencies. However, the stringent spectral requirement imposed by the FCC standards is challenging. Besides, a proper solution is demanded to meet the peak power specification desired at both 6.5GHz and 8GHz carrier frequencies. Considering those two issues, a two-fold linear interpolation technique is adopted [27], meeting rigorous spectral purity imposed by communication standards in conjunction with utilizing a matching network incorporating a tuning capacitor to cover both the 6.5 and 8 GHz bands. There are two techniques will be introduced in this chapter. This chapter organizes as follows: the switched-capacitor power amplifier principle will be described in Section 3.1 which also includes the switch size optimization strategy. For addressing multi-carrier operation, various circuit configurations will be investigated in Section 3.2. Section 3.3 will introduce the matching network that is applied to meet the peak power requirement. Finally, interpolation methods are discussed in Section 3.4.

3.1. Switched Capacitor Power Amplifier Principle

As stated earlier, the switched-capacitor power amplifier (SCPA) utilizes an array of accurately-assigned capacitors that works as a voltage divider [25]. The number of the selected capacitors, of which the bottom plates are switched at an RF carrier frequency between the supply voltage and the ground, determines output (drain) amplitude that can be viewed as a voltage source. Moreover, the digital input code that contains both the envelop and phase information of the baseband data controls the CMOS switches. Consequently, a direct digital-to-RF conversion is achieved. As shown in the Figure 3.1 (a) and (b), in the capacitors array, all capacitors' top plates are connected. Moreover,

the Thévenin-equivalent impedance of the capacitors array is the total capacitance, including the turned-on and turned-off capacitors, which is code-independent. Due to the switching operation, a square wave is generated at the bottom plates of the selected capacitors. By adding an inductor in series with the top plate of the capacitors, at the

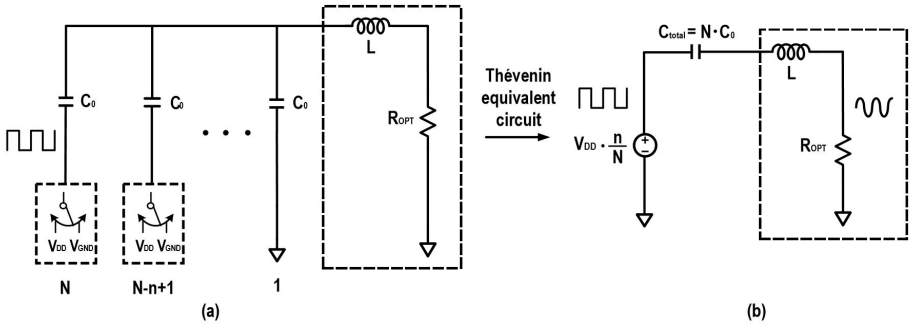

Figure 3.1: (a) Thermometer switched-capacitor array with the matching network; (b) Thévenin equivalent circuit.

output node, i.e., V_{out}, ideally, only the fundamental component at the RF carrier frequency is selected and the higher harmonics are suppressed. According to the Fourier series, the fundamental amplitude of the output signal is expressed as:

$$V_{out} = \frac{2}{\pi}(\frac{n}{N})V_{DD} \tag{3.1}$$

where the $\frac{2}{\pi}$ is the coefficient of the fundamental component, V_{DD} is the supply voltage connected to the CMOS switches, n is the number of turned-on capacitors, and N is the total number of the capacitors in the array. Accordingly, the output power is given as below:

$$P_{out} = \frac{2}{\pi^2}(\frac{n}{N})^2\frac{V_{DD}^2}{R_{OPT}} \tag{3.2}$$

As mentioned above, the square waveform, generated at the drain nodes, experiences sharp rise/fall times. In other words, the transition time from V_{GND} to V_{DD} is limited, during which the inductor behaves as a constant current source that is equivalent to an open circuit. As shown in Figure 3.2, there is a path from the switching terminal to the ground in the equivalent circuit, through which the dynamic power is consumed due to charging and discharging of the series capacitors. The dynamic power consumed by charge flow can be calculated as below:

$$P_{sc} = C_{in}V_{DD}^2 f \tag{3.3}$$

where f is RF carrier frequency and C_{in} is the series capacitance of switching capacitors and ground-connected capacitors:

$$C_{in} = \frac{n(N-n)}{N^2}C_{total} \tag{3.4}$$

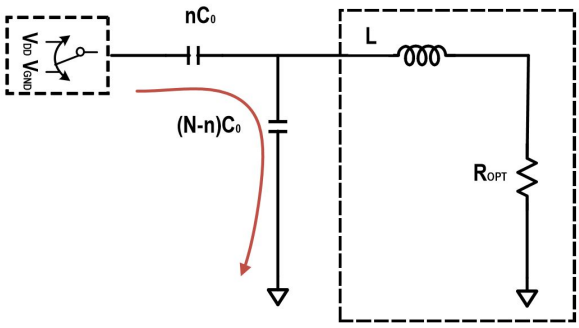

Figure 3.2: Equivalent circuit for dynamic consumption calculation

In the Figure 3.3, the simulated dynamic power consumption versus input code is shown.

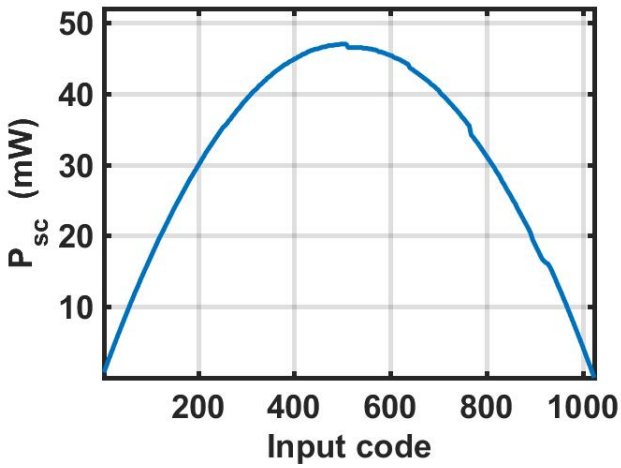

Figure 3.3: Dynamic consumption versus input digital code

As expected, P_{SC} is parabolic with a fixed RF carrier frequency according to the equation 3.3 and 3.4, from which C_{in} is maximum for n = N/2 and minimum for n = 0 and n = N. Given P_{SC} and P_{out}, ideal drain efficiency is defined as [25]

$$\eta = \frac{P_{out}}{P_{out} + P_{sc}} = \frac{4n^2}{4n^2 + \frac{\pi n(N-n)}{Q_{load}}} \tag{3.5}$$

where the Q_{load} is the loaded quality factor of the resonant network, which is given as:

$$Q_{load} = \frac{2\pi fL}{R_{opt}} = \frac{1}{2\pi fCR_{opt}} \tag{3.6}$$

3.2. SWITCH SIZE OPTIMIZATION STRATEGY

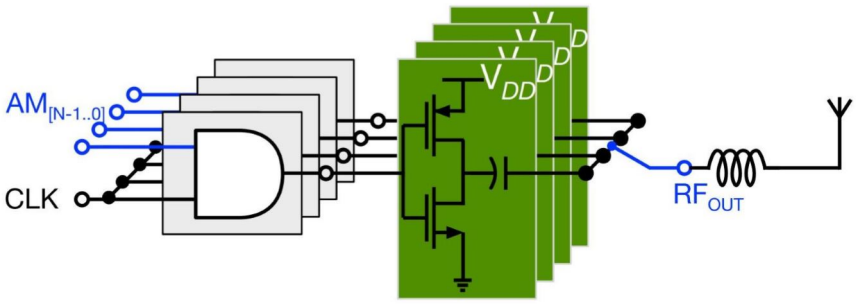

Figure 3.4: A single-ended switched-capacitor RF-DAC

A single-ended switched-capacitor RF-DAC is shown in Figure 3.4. Acting as a digital mixer, the AND logic up-converts the envelop information of the digital baseband UWB pulses into RF carrier frequency. Assuming that $A_{[N]}$ is "1", the output of the bitwise AND logic is a square wave, which drives the class-D digital CMOS switching PA at the RF carrier frequency. In the contrary, when $AM_{[N]}$ is "0", the output of the bitwise AND logic is zero, constant value, resulting in turning on/off the PMOS/NMOS respectively. Thus, either supply voltage or ground, which are both taken as the ac ground, is connected to the bottom plate of the capacitor. Combined with the series inductor, a resonator is established, leading to the selection of the fundamental frequency component and the suppression of higher harmonics. Finally, the up-converted UWB pulse is transmitted using an antenna. In this work, to achieve decent second harmonic suppression and obtain high output power, a push-pull (pseudo differential) digital power amplifier has been adopted as shown in Figure 3.5. As depicted in Figure 3.5, a transformer is employed to transforms 50 ohm antenna load into an optimum load for switched-capacitor DPA. In general, transformer performs the following tasks:

- It converts the differential signal, balanced, into a signal ended, unbalance, counterpart. It literally acts as a balanced-to-unbalanced (balun).
- It decouples the antenna output node from the switched-capacitor PA.
- In conjunction with input/output capacitors, it acts as a resonator to select the fundamental frequency component.
- It transforms 50 ohm antenna load into an optimum loading condition for the switching PA.

Compared with equation 3.2, the output power at the P_{out} is recalculated as:

$$P_{out} = \frac{8}{\pi^2}(\frac{n}{N})^2 \frac{V_{DD}^2}{R_{opt}} \tag{3.7}$$

Thus, the optimum differential loading impedance (R_{opt}) can straightforwardly be derived from equation 3.7 as: is given as:

$$R_{opt} = \frac{8V_{DD}^2}{\pi^2 P_{out}} \tag{3.8}$$

According to Table 1.1, the targeted RF peak power should be more than 15 dBm. Hence the corresponding value of the R_{OPT} is 37.6 Ω with V_{DD} = 1.2. Practically, however, due to matching network losses, the aimed RF peak cannot be achieved with R_{OPT} = 37.6Ω. Moreover, the extra losses, including the loss related to the on-resistance of the switches and dynamic transient switching loss (equation 3.3), relatively reduce the RF peak power. Thus, to determine the maximum output power, an $Spectre^{TM}$ circuit simulation at

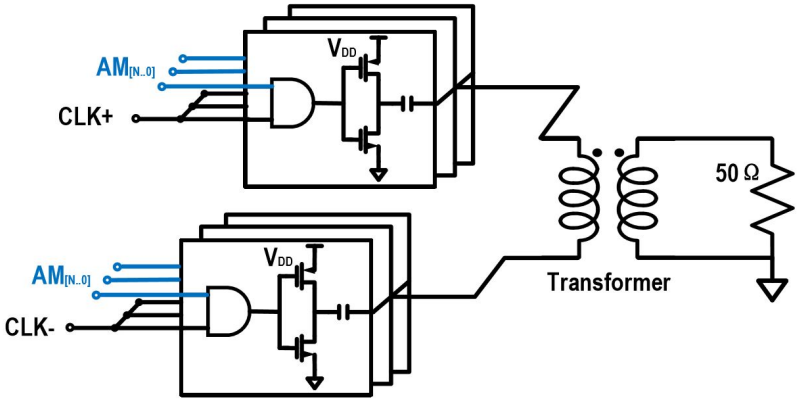

Figure 3.5: The proposed push-pull switched-capacitor RF-DAC

f_{LO} = 8GHz is done to optimize the CMOS device size and R_{opt} and the corresponding RF output power is depicted in Figure 3.6(a). Note that, in this simulation an ideal transformer with turn ratio of 1:1 along with proper tank capacitors are employed. The multiplication factor is the number of transistors in parallel constituting one switch, where the lengths of NMOS and PMOS are both 40 nm and the widths of NMOS and PMOS are 115 nm and 230 nm, respectively. The maximum output power, 20.84 dBm, is obtained when the terminal resistance is 4 Ω and the multiplication factor is 79. Moreover, Figure 3.6 (b) reflects the circuit simulation results of the drain efficiency versus R_{opt} and multiplication factor. The maximum drain efficiency is 87.45 %, and occurs when the terminal resistance is 4.6 Ω and the multiplication factor is 10. In this master project, achieving the targeted RF peak output power is superior to obtaining the highest drain efficiency.

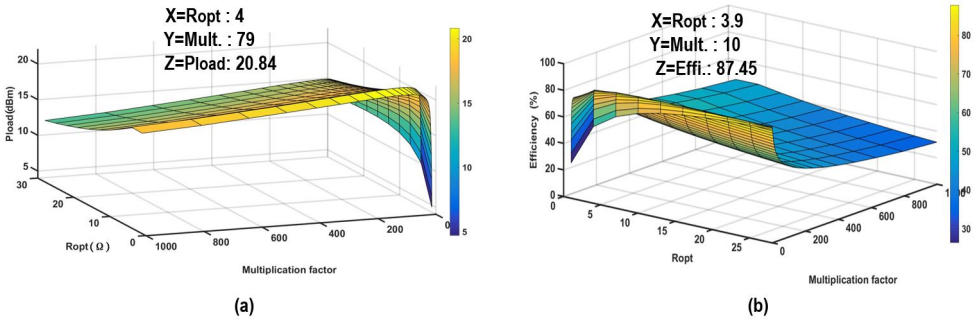

Figure 3.6: (a) Output power Optimization; (b) Drain efficiency Optimization.

As a result, our design strategy is based on meeting the aimed peak power while achieving an acceptable drain efficiency. As briefly discussed earlier, the on-resistance of the CMOS switch and its parasitic drain capacitance contribute to the drain efficiency degradation. Besides, the parasitic gate capacitance influences the driving capability of preceding chain of buffers affecting system efficiency of the digital-intensive transmitter. Thus, the variations of these three parameters with respect to CMOS multiplication factor are simulated and depicted in Figure 3.7 (a) and (b), respectively. Based on Figure.

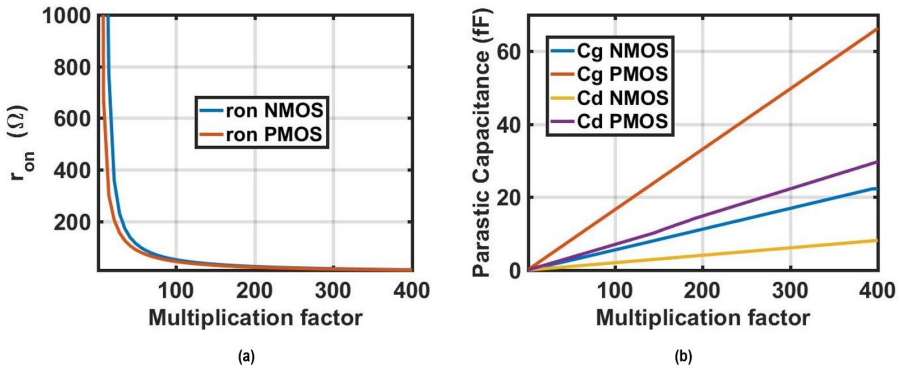

Figure 3.7: (a) On-resistance versus the multiplication factor; (b) Capacitive parasitics versus the multiplication factor.

3.7(a), with multiplication factor of 200, the r_{on} of both PMOS and NMOS are less than 20 Ω. Moreover, the total parasitic drain and gate capacitors for the multiplication factor of 200 are 18 fF, 44 fF, respectively. Note that this r_{on} and parasitic capacitances are done for only one unit cell of CMOS switch. It is noteworthy to mention that, in this project, the antenna impedance is considered to be 50 Ω. Thus, as indicated in the task of an on-chip transformer, the transformer together with the matching network provides the optimum loading condition at the drain node of DPA. This transformation will further

be investigated in the following sections.

3.3. TOPOLOGIES TOWARDS MULTI-CARRIER APPLICATION

From commercial considerations, a frequency-agile UWB pulse generator is desired. Hence, the UWB pulse generator must operate in multi-mode/multi-band configurations that cover both 6.5 and 8 GHz frequency bands. In other words, to cover various frequency bands, the designated matching network must relatively have tuning capability. Based on the switched-capacitor RF-DAC architecture, several matching network topologies have been investigated that will be discussed as follows:

3.3.1. FIRST TOPOLOGY TOWARDS MULTI-CARRIER APPLICATION

In the first approach, as shown in Figure 3.8, instead of a single capacitor used earlier, a pair of capacitors is utilized, in which one of the capacitors is in series with an band-select switch. By turning off the band-select switch, only one capacitor is connected to the CMOS switch resulting in a smaller resonant capacitor. Consequently, with a fixed inductor, the resonant frequency becomes higher. In contrast, by turning on the band-select switch a lower resonant frequency is obtained. In this case, the pair of capacitors acts as a single unit capacitor. Note that here one extra signal is needed to control the state of the band-select switch. However, since this band-select switch is located in se-

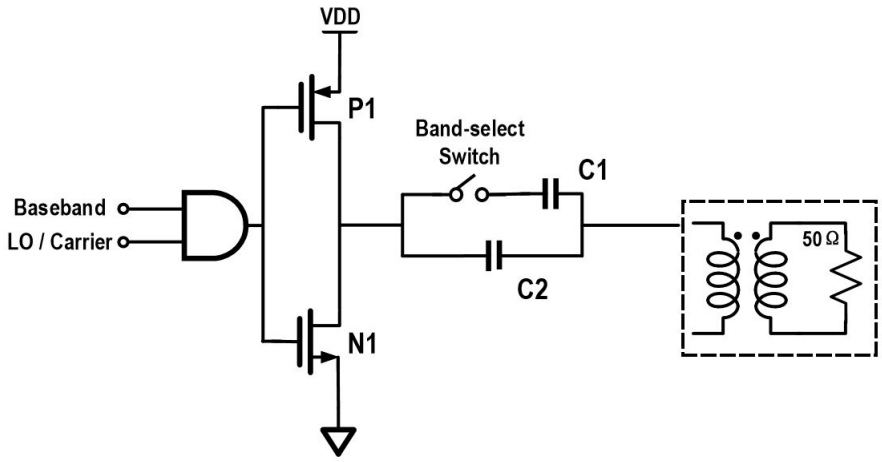

Figure 3.8: First topology towards multi-carrier application

ries with the primary capacitor of SCPA, the drain efficiency is dramatically degraded due to the on-resistance of the band-select switch. To attain a small on-resistance, the size (aspect ratio) of the band-select switch transistor must drastically be increased. Apart from that, the off-resistance of the switch also becomes smaller. Thus, the left plate of C1 capacitor in Figure 3.8, cannot be regarded as connected to an open circuit when the band-select switch is off. From this perspective, the idea of tuning the resonant capaci-

tor to select various band is unrealizable. Moreover, on-resistance slows down the transition time, making the signal less square-wave-like, which affects the linearity of SCPA. As stated in [25], the shape of square wave affects the AM-PM and AM-AM linearity performance of SCPA. It is noteworthy to mention that the proposed idea is applicable for lower frequency range. Nonetheless, for the targeted 6.5/8 GHz frequency bands, it is inappropriate.

3.3.2. SECOND TOPOLOGY TOWARDS MULTI-CARRIER APPLICATION

Similar to the first topology, the second one shown in Figure 3.9 (a), also tunes the resonant capacitor. Instead of using a capacitor together with a band-select switch, the CMOS switch of SCPA has two modes of operation. In the normal mode, it is acting as a typical CMOS switch while in the band-select mode is acting as a high-impedance circuit so that the connected bottom plate of the capacitor can be regarded as an open circuit. In this context, the capacitor is literally disregarded from the total resonant capacitor. Consequently, as discussed in the first approach, the desired frequency band is selected by merely engaging or dismissing the band-select circuit. To achieve the second state, a bitwise OR and a bitwise AND logics are employed by PMOS and NMOS, respectively. Besides, as depicted in Figure 3.9, the controlling signal is directly applied to the bitwise AND logic while a negated signal, generated by an extra CMOS inverter, is applied to bitwise OR logic. When a low frequency carrier, i.e., 6.5 GHz, is needed, all

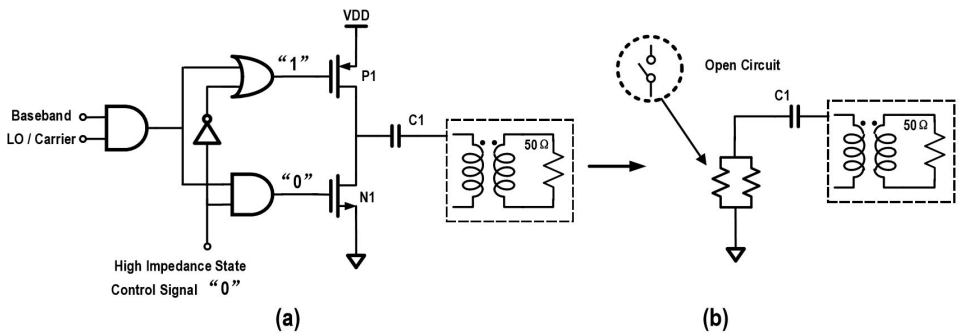

Figure 3.9: (a) Second topology towards multi-carrier application; (b) High-impedance equivalent circuit.

switched-capacitor units operate in the first mode. The outputs of both bitwise PMOS-connected OR and bitwise NMOS-connected AND are controlled by the output of the up-converted mixing AND whose inputs are the baseband and carrier signals. This is achieved when a band-select control signal is "1". In contrast, by setting this control signal to "0", the outputs of the PMOS-connected OR and NMOS-connected AND are fixed to "1","0", respectively. Therefore, both PMOS and NMOS are turned off, which represent a high-impedance circuit. As shown in the Figure 3.9 (b), the equivalent circuit is two parallel large resistors, which can ideally be regarded as an open circuit.

Compared with the first topology, due to avoiding to directly placing an explicit band-select switch in series with the primary capacitor of SCPA structure and reusing a CMOS switch of the SCPA as an implicit band-select switch, this topology is energy-efficient. However, as in the first approach, the off-state impedance significantly depends on the aspect ratio of the CMOS switch. As a result, there is a trade-off between the drain efficiency and off-state impedance of the switch. As stated in Section 3.2, to achieve the desired peak RF power and obtain a reasonable drain efficiency, the aspect ratio of the CMOS switch is reasonably selected large enough to simultaneously diminish the on-resistance of CMOS switch and generate a square-wave signal at the drain node of the CMOS switch. However, the "off" resistance is inversely proportional to the switch size. Moreover, an extra power loss is related to the additional control digital logic circuitries, including bitwise OR and AND, which operate up to 8 GHz. Consequently, like the first approach, the proposed technique is more applicable in the low Gigahertz frequency bands.

3.3.3. THIRD TOPOLOGY TOWARDS MULTI-CARRIER APPLICATION

The two band-select techniques that proposed earlier suffer from degradation of the RF peak power, drain efficiency, and signal purity. The third technique for the multi-mode/multi-band operation is quite straightforward, in which the tank resonant frequency is set to the middle of the two frequency bands. This is achieved using a capacitor that resonates with the tank equivalent inductor at 7.25 GHz which is in the middle of 6.5 and 8 GHz frequency bands. Compared with the previous methods, this topology does not suffer from the extra complicated circuitries and additional control signals needed for band-select modes of operation. This topology, however, slightly reduce the peak RF power, the drain efficiency, and the spectral purity since the tank circuit does not resonate at 6.5 and 8 GHz. In other words, higher harmonics reasonably present at the output node. Nevertheless, the system efficiency and the overall spectral purity of the former two approaches, due to the extra controlling circuitries, are inferior compared with the latter method. The primary advantage of this technique is its simplicity which is an essential feature operating at higher frequency bands.

3.4. MATCHING NETWORK TOWARDS PEAK OUTPUT POWER

As stated earlier, while covering two frequency bands of 6.5 and 8 GHz, the targeted peak RF output power of SCPA is 15 dBm. Thus, the 50 Ω antenna impedance must be transformed to an optimum impedance at the drain node of SCPA. Due to the presence of r_{on} and the parasitic capacitor, the optimum impedance of 4 Ω calculated in Section 3.1, should be revised. These parasitics are shown in Figure 3.10 (a). Moreover, the Thevenin equivalent of the SCPA with these parasitics is depicted in Figure 3.10 (b).

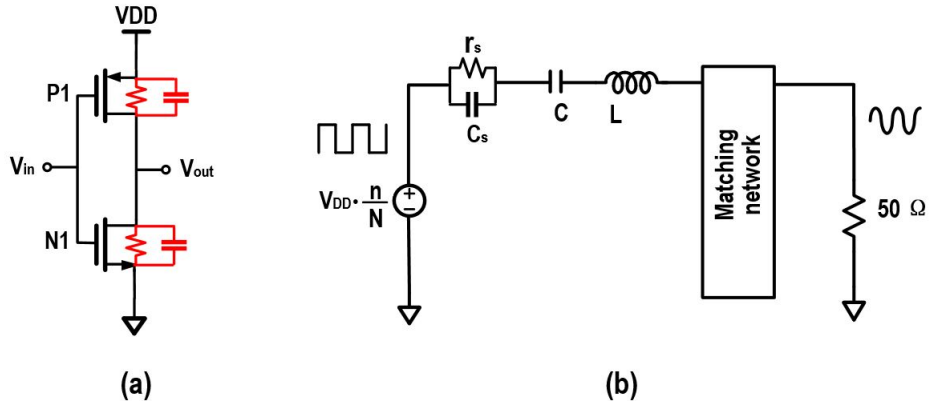

Figure 3.10: (a) Switch parasitics; (b) A Thévenin equivalent circuit where r_s and c_s are the effective resistance and capacitor, respectively

Thus, as in the case of conventional PA, a load-pull simulation is perform on the proposed SCPA to verify optimum loading at the drain node. As shown in the Figure 3.11 (a) and (b), the peak output power is simulated at both 6.5 and 8 GHz carrier frequencies where the Rho is the amplitude and Theta is the phase of a load reflection coefficient (Γ) of a 50 Ω load. Also, the corresponding system efficiencies at 6.5 and 8GHz frequencies

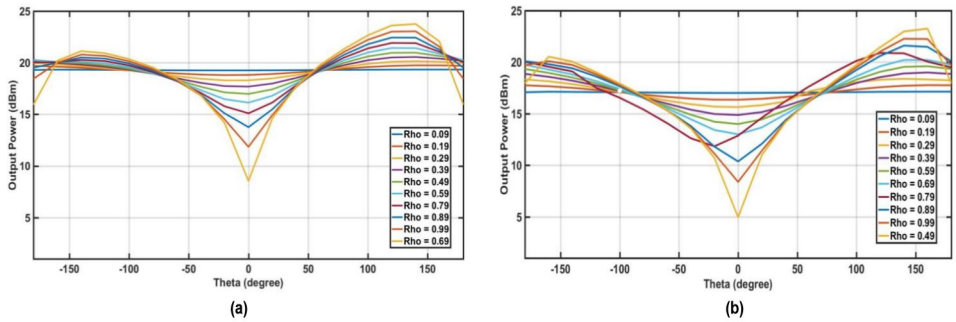

Figure 3.11: Peak output power loadpull at (a) 6.5 GHz carrier; (b) 8 GHz carrier.

are depicted in the Figure 3.12 (a) and (b), respectively. The maximum output power for 6.5 GHz carrier is obtained when Rho is 0.6 and Theta is 146 degree while these values for 8 GHz are 0.5 and 153 degree. Hence, two different matching networks are needed for transferring the 50 Ω into those optimal impedances, respectively.

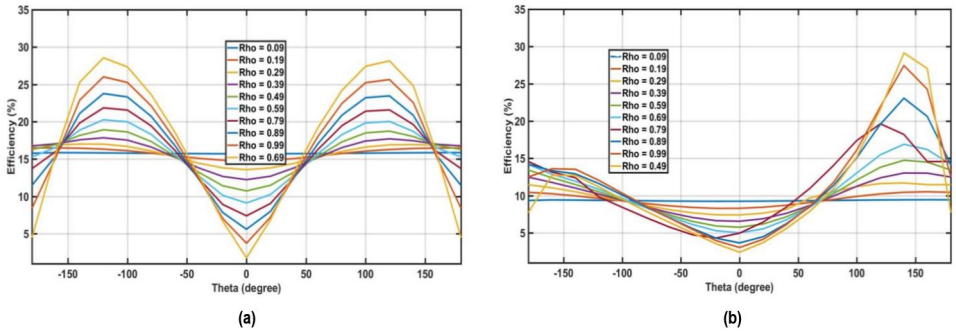

Figure 3.12: System efficiency loadpull at (a) 6.5 GHz carrier; (b) 8 GHz carrier.

However, the goal of this master project is to have only a unified matching network. To do so, Figure 3.13 demonstrates the proposed π matching network with two input/ output band-select capacitors which will be implemented off-chip. Using a control signal, this network transforms the 50 Ω load into two desired optimum loads at 6.5 and 8 GHz, respectively. A π-network is selected to have one fix inductor along with two band-select capacitors. To achieve the desired peak RF power at both frequency bands, first the inductor value is selected, and accordingly, the value of those capacitors are determined. In this context, 6.5 GHz band is selected when both of C2 and C3 are included in the π matching network. Correspondingly, by dismissing these capacitors, the circuit operates at 8 GHz frequency band.

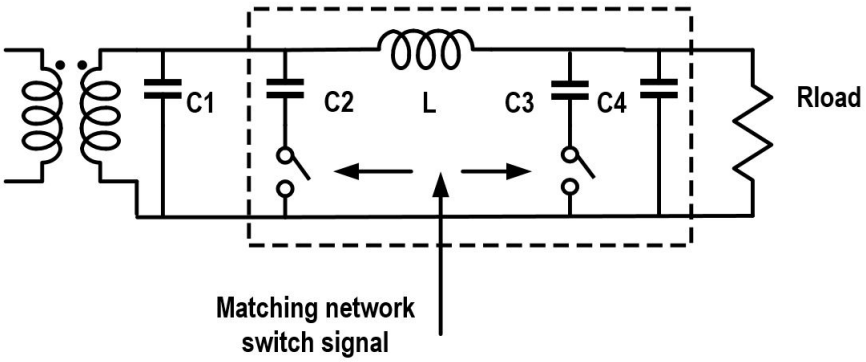

Figure 3.13: Matching network using band-select capacitors

3.5. SUPPRESSION OF SAMPLING SPECTRAL REPLICAS

In general, a DAC takes a sequence of discrete-time binary code input and generates a continuous-time output. Due to the sampling operation, according to the sampling theorem [28], the analog signal output of a DAC contains sampling spectral replicas. Moreover, since an input discrete sequence signal of a DAC, first converted into an impulse train, by employing a boxcar windowing filter, a continuous-time signal is reconstructed from its samples. The reconstruction filter is, indeed, a zero-order hold (ZOH) interpolation filter with a Sinc-function frequency response.

$$A = \frac{sin(\pi f / f_0)}{\pi f / f_0} \tag{3.9}$$

Thus, the sampling spectral replicas in the frequency domain are shaped by the Sinc-function roll-off factor, A. As a result of the sampling function, the sampling spectral replicas of the baseband signal occur at multiple integers of fc as shown in Figure 3.14. Thus, these replicas violate the out-of-band requirement imposed by FCC. More so, when a baseband signal with a larger bandwidth is employed the effect of sampling spectral replicas are more detrimental since the suppression level of a Sinc-function, as depicted in Figure 3.14, dramatically decreases. Typically, an anti-alias filter is needed and the requirement on this filter could be more rigorous the sampling frequency, fc, is selected at the Nyquist frequency, i.e., half of the highest sampling rate of the discrete-time system. To relax the requirement or even avoid using an anti-alias filter, up-sampling and interpolation techniques are utilized in this work, which are introduced as follows:

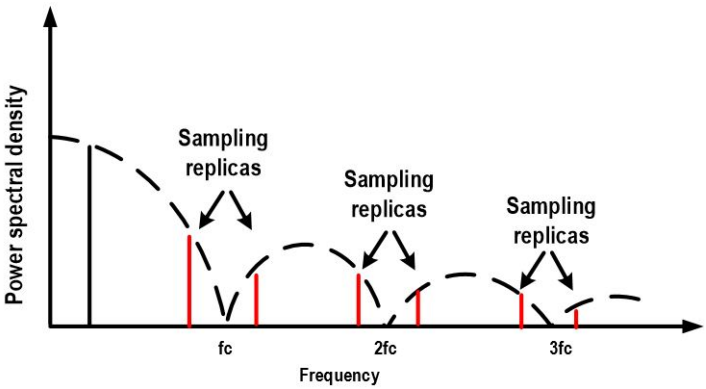

Figure 3.14: Unfiltered DAC output with images and sinc roll off.

3.5.1. UP-SAMPLING AND INTERPOLATING

The basic concept of the up-sampling and interpolating is to sample the digital baseband codes, in which some extra points are inserted, at a higher sampling rate. In other words, an up-sampler is a rate converter located in the middle of a discrete-time block and a

continuous-time counterpart. Literally, the up-sampling operation by "n" is achieved by inserting "n' zeros (zero-padding) between two consecutive samples. Nevertheless, an interpolation operation is a combination of an up-sampling and the following filtering operation. For example, a ZOH is an interpolation filter with a Sinc-function characteristic. Consequently, the sampling replicas are translated to higher frequencies far away from the baseband signal. In a low sampling clock case, as shown in the Figure 3.15 (a), the transition region of the anti-alias filter's frequency response required is quite sharp, which represents a high-order filter that is challenging and expensive. In the Figure 3.15 (b), utilizing an interpolation by K, which is an integer greater than one, the anti-alias filter requirements are significantly relaxed. On top of that, the dynamic range (signal-to-noise (SNR) ratio) of the designated mixing-DAC improves due to spreading the quantization noise of the DAC over a wider frequency range. In fact, the dynamic range increases by 3 dB by doubling the sampling rate. The predefined digital baseband

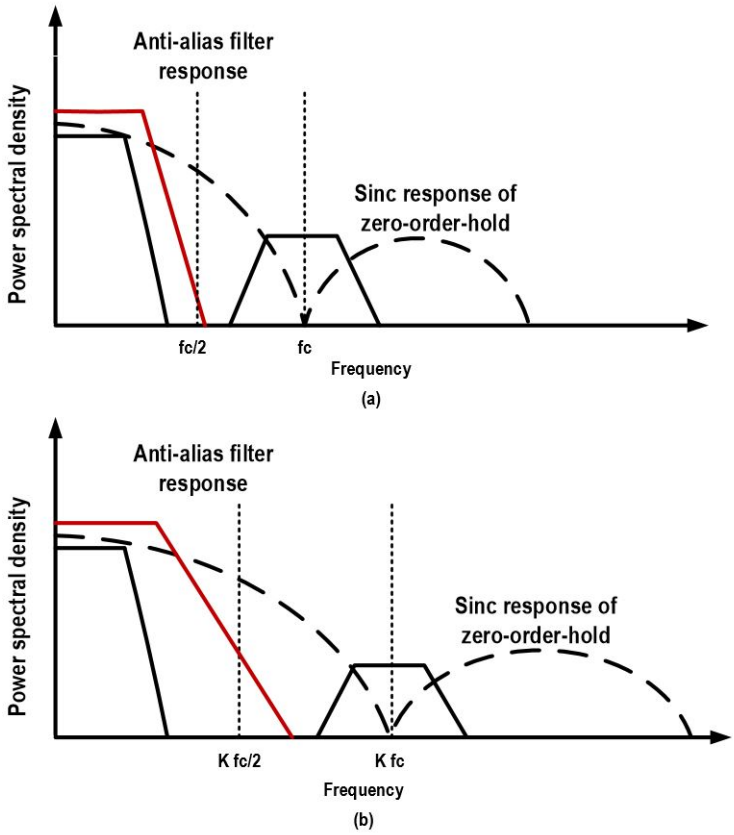

Figure 3.15: (a) Anti-alias filter requirements for a low sampling rate; (b) Anti-alias filter requirements for a high sampling rate

UWB pulses that are used for 1, 2, and 4 GS/s are depicted in Figure 3.16. The pulses'

lengths are all 6 ns. Comparing with the first UWB signal of 1 GS/s, twice and quadruple samples utilized in the 2 and 4 GS/s UWB pulses, respectively. The value of the additional inserted point is calculated by averaging the two original neighbor points. The three corresponding spectrum are shown in the Figure 3.17. As expected, the yellow curve which is the corresponding spectrum of 4 GS/s signal has the maximum frequency distance between the baseband and the first sampling replica, which dramatically improves the out-of-band suppression. The costs for up-sampling and interpolating are need for a larger memory space for storing extra inserted points and a 4-to-1 MUX operating at a 4 GHz clock, which contributes to more power consumption. The additional chip area for the memory and MUX is negligible.

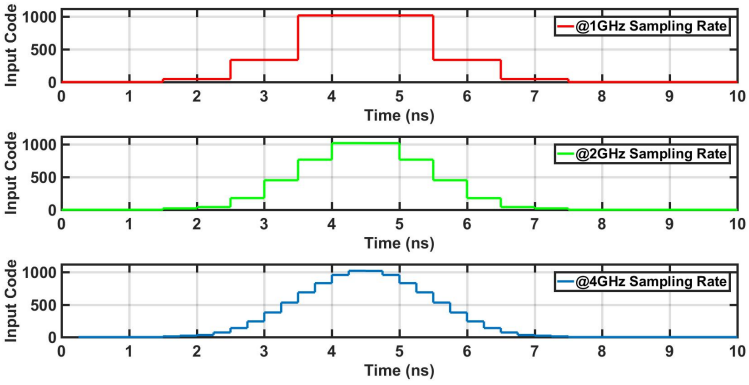

Figure 3.16: The digital baseband UWB pulses used for 1, 2, and 4 GHz GS/s.

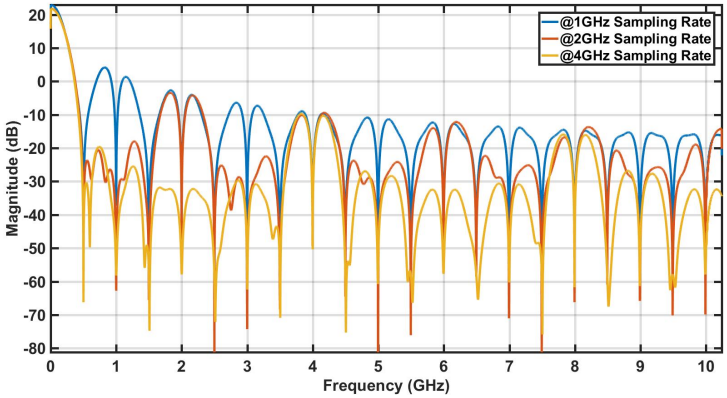

Figure 3.17: The spectrums of the digital baseband UWB pulses used for 1, 2, and 4 GHz sampling frequencies.

3.5.2. A TWO-FOLD, LINEAR INTERPOLATION SCHEME

Currently, most DACs operate in ZOH mode, holding a constant value during the sampling clock period. As stated earlier, the frequency response of the ZOH is Sinc function leading to suppression of the power of the spectral replicas by $sinc^2$ function. If the ZOH is replaced by the first-order-hold (FOH), the attenuation on the DAC's image components can be improved since the frequency response of the FOH, as illustrated in Figure 3.18, is the $sinc^2$ function. In other words, the higher-order interpolation sig-

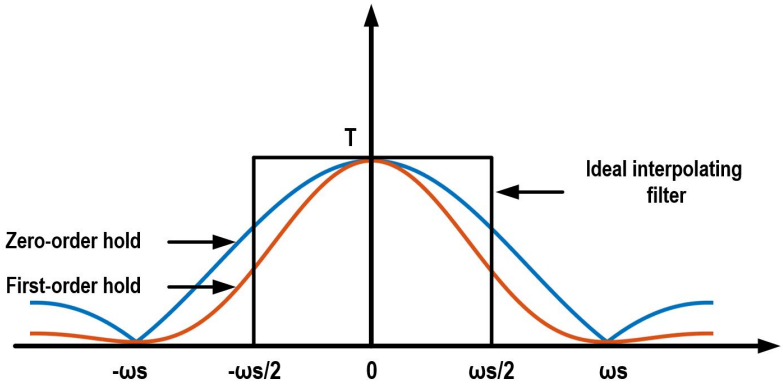

Figure 3.18: Zero-order-hold and First-order-hold frequency response

nificantly suppresses the out-of-band sampling spectral replicas. This further relaxes the requirements of the anti-alias filter in a case of a stand-alone DAC or disregards a band-pass filter (BPF) in an RF-DAC TX example. In practice, the realization of linear or

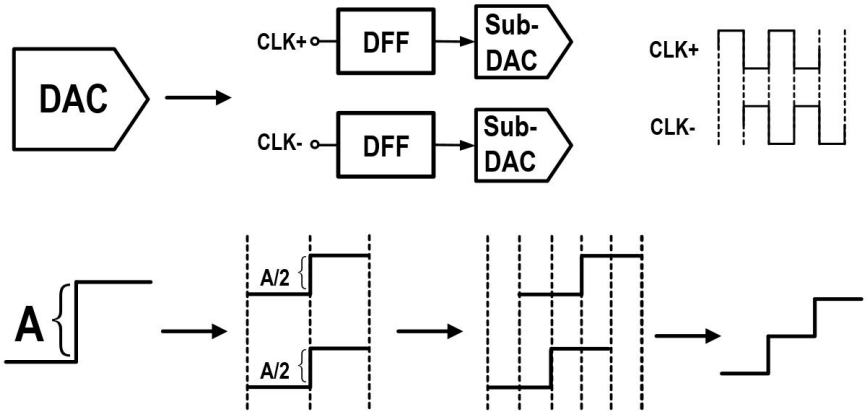

Figure 3.19: Interpolation by using complementary sampling clocks

even higher-order is rather complicated. Instead of a digital FOH linear interpolation, an N-fold linear interpolation is widely used to approximate a FOH linear interpolation to

suppress the sampling spectral replicas by a $sinc^2$ filter characteristic at multiples of the sampling clock. The two-fold linear interpolation [27] is adopted in the proposed SCPA by splitting it into two identical banks one of which drives by a complementary sampling clock generated by a simple inverter/phase aligner circuit. Illustrated in Figure 3.19, the switched-capacitor mixing-DAC comprises two smaller DAC whose capacitors and switch sizes are halved. Clocked by a pair of complementary sampling clocks, respectively, the DACs generate two smaller and identical up/down steps, between which there is a half-sampling-cycle shifting in time domain. These two steps are finally summed up by hard-wiring of all up-plates of switched capacitors. Note that the envelope signal of each mixing-DAC is also halved. Consequently, a two-fold interpolation is achieved, as shown in Figure 3.20. In this context, the number of switches is doubled while the total

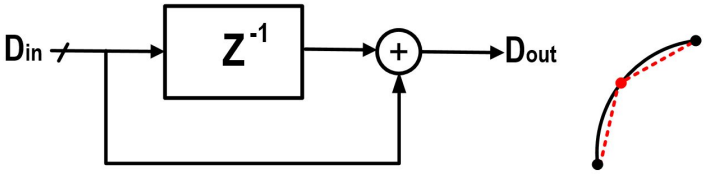

Figure 3.20: The two-fold interpolation system.

capacitance value is the same. In contrast to ZOH, in the FOH interpolation, the new samples are linearly added in the middle of the old ones.

Apparently, extra D-flip-flops (DFF) are needed when applying the complementary sampling clocks, leading to more power consumption. However, in practice, DFF is also necessary for time synchronization to compensate for different data/clock routings. Doing so, the sampling spectral replicas are significantly suppressed utilizing reasonably uncomplicated circuit design. Although the value of capacitors and switch sizes halved, due to the extra signal/clock routings and employing two identical banks, the chip area is almost doubled. A further improvement could be exploiting quadrature clocks to drive four DACs that are split from the original one. Certainly, the quadrature clocks needs to be provided by extra circuits.

4

AN IR-UWB PULSE GENERATOR

Based on the switched-capacitor RF-DAC unveiled in Chapter 3, a comprehensive impulsive radio (IR) UWB transmitter is proposed with an on-chip ROM memory storing a predefined digital UWB pulse. Briefly, the UWB pulse generator consists of two parts: a digital part managing digital control signals as well as a digital baseband UWB pulse; the switched-capacitor RF-DAC converts the digital baseband UWB pulse into an RF signal. The block diagram of the proposed IR-UWB pulse generator is introduced in Section 4.1. Section 4.2 describes the implementation of the switched-capacitor RF-DAC in detail, whereas the digital part is presented in Section 4.3.

4.1. PULSE GENERATOR TOP-LEVEL OVERVIEW

Consisting of the digital and RF-DAC parts as mentioned above, the block diagram of the IR-UWB pulse generator is shown in Figure 4.1. The digital part includes a address decoder, an read-only memory combined with a 4-to-1 multiplexer (Mux), and a binary-to-thermometer encoder. As thoroughly discussed in Chapter 3, due to adopting the push-pull SCPA in combination with the two-fold linear interpolation scheme, the switched-capacitor RF-DAC is composed of four identical sub mixing-DAC followed by a balun transformer converting a differential signal to a single-ended counterpart. Through an off-chip matching network, the up-converted the IR-UWB pulse finally is delivered to a 50 $|Omega$ transmitting antenna. In general, the IR-UWB pulse generator operates in two phases: In the first phase, the IR-UWB pulse is generated for the duration of 6.5ns (on-mode). The second phase is silent (off) mode. In the first phase, the pulse generation is initiated when the mode-control signal, D_{in}, becomes one. Hence, the IR-UWB pulse is generated at a fixed rate. In contrast, in the silence mode,D_{in} is zero and the resulting UWB pulse becomes zero. Note that the maximum pulse rate is 125 MS/s set by a limitation in ROM design which is discussed later.

First, D_{in} is decoded by the input-stage, an address decoder. Then, the 8 bits of the address decoder, $S_{[7..0]}$, drive the ROMs generating the desired IR-UWB pulse. The following Multiplexers, clocked at 4 GHz, facilitate the up-sampling operation. Subsequently, their binary output signals are converted into thermometer-coded bit streams

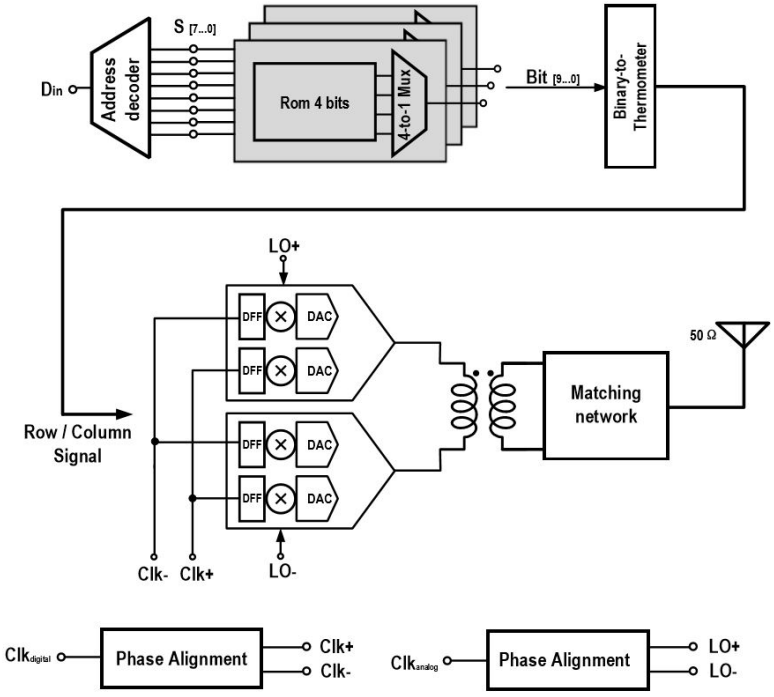

Figure 4.1: Block diagram of the proposed IR-UWB pulse generator

using a binary-to-thermometer encoder. As stated earlier, there are four identical mixing-DACs for the interpolation/ differential operations. As indicated in Figure 4.1, the complementary sampling clocks for linear interpolation and differential LO clocks for push-pull operation are realized using two phase-aligner circuitries. Moreover, DFFs are employed to synchronize these sampling clocks at mixing-DAC unary cells. At the end of the TX chain, there are balun transformer and matching network to provide the proper signal for transmitting antenna.

4.2. SWITCHED-CAPACITOR RF-DAC IMPLEMENTATION

4.2.1. SEGMENTED DAC STRUCTURE

In a high resolution DAC/mixing-DAC, a segmented approach is widely adopted [29-30], [40]. In the segmentation approach, the mixing-DAC is split into a combination of thermometer-coded unary and binary-weighted cells. Moreover, in the segmentation approach, there is a trade-off between unary cell matching and chip die area. Additionally, the circuit complexity, signal routing, and the power consumption are critical design parameters. On the one hand, the static and dynamic performances benefit from the better matching among thermometer-coded unary cells, which might slightly be degraded due to the gradient mismatch caused by the position of the unary cells and the

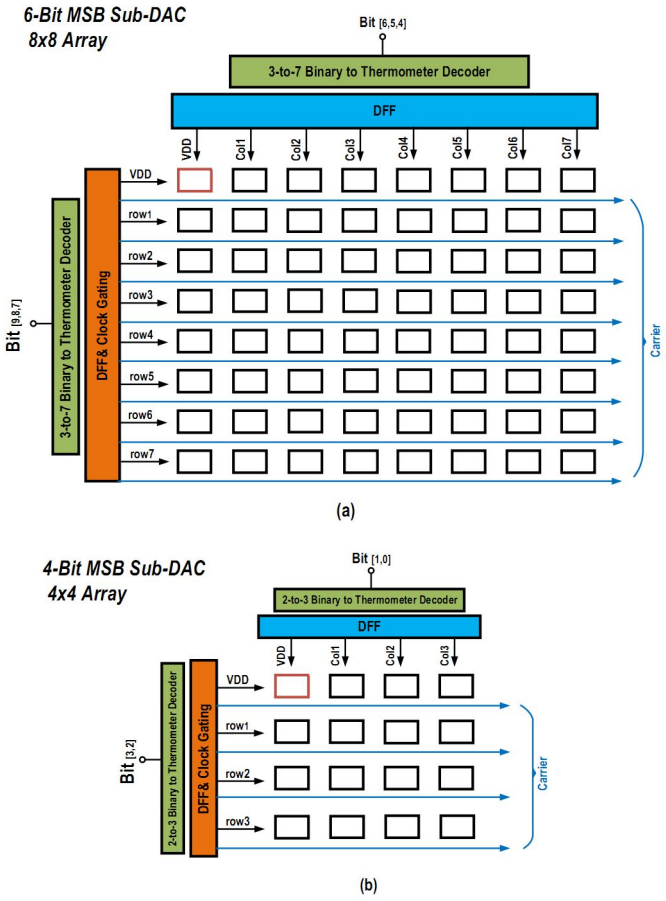

Figure 4.2: (a) 6-bit MSB thermometer-coded unary cells; (b) 4-bit LSB unary cells.

signal/clock routings. It worth mentioning that the number of unary cells grows exponentially when the thermometer-coded segment becomes larger, which dramatically increases the mixing-DAC's layout complexity. In this work, a 10-bit switched-capacitor RF-DAC is selected to meet both the spectral purity and RF power control requirements of the ranging application. In this context, 10-bit is split into 6 MSB and 4 LSB bits, respectively, to also guarantee the monotonicity of the proposed mixing-DAC. As mentioned before, the monotonic characteristic of the mixing-DAC is the premise of amplitude modulation for UWB pulse generation. The thermometer-coded MSB section comprises 63 unary cells while the LSB part consists of 15 unit cells. Note that ideally one MSB unary cell is equal to 16 LSB cells. In our implementation, both MSB and LSB unary matrices are surrounded by unary dummy cells to improve matching. Two 3-to-7 binary-to-thermometer encoders are respectively employed to generate column/row selecting signals for an 8x8, 6-bit MSB unary mixing-DAC matrix, whereas two 2-to-

3 binary-to-thermometer encoders are applied for exploited for a 4x4 4-bit LSB unary mixing-DAC matrix. In both sub-DACs, a clock-gating circuit is utilized to decrease the excess power consumption of LO clock while the selecting signal of a unary cell is off. Instead of simultaneously providing all units cells with the LO clock, the row selecting signals enable row-clock-gating circuit allowing the LO clock drives the unary cells in the designated row-line. Doing so, the LO feed-through, originated from the LO signal of mixing-DAC unary cell to the drain nodes, dramatically reduces. Besides, as stated earlier, the DFFs are employed to facilitates the adoption of the proposed up-sampling schemes. More importantly, the spectral purity of the proposed switched-capacitor RF-DAC improves using the synchronous operation of the row/column selecting signals. In fact, DFFs play a critical role in generating an undistorted envelope of the IR-UWB pulse by compensating the time-delay issue among the unary cells located at different places in the mixing-DAC matrix. Generally, the signal flow of the switched-capacitor RF-DAC is as followsUsing the binary-to-thermometer encoders, the input binary code is converted into the row/column selecting signals, which are then sampled by the DFFs with complementary sampling clocks. Finally, by sequentially turning on and off the CMOS switches according to the row/column selecting signals, the amplitude modulation is achieved.

4.2.2. SUB-DACS UNARY CELL

The unary unit schematic of 6-bit MSB and 4-bit LSB sub mixing-DAC is depicted in Figure 4.4, which contains three parts: The left part, in red dash box, is the row/column selecting circuit (row/column decoder); The inter-mediate part, in green dash box, is a bit-wise AND mixer for up-converting the baseband signal to the carrier frequency, whereas the right part, in blue dash box, is the CMOS switch followed by a capacitor.

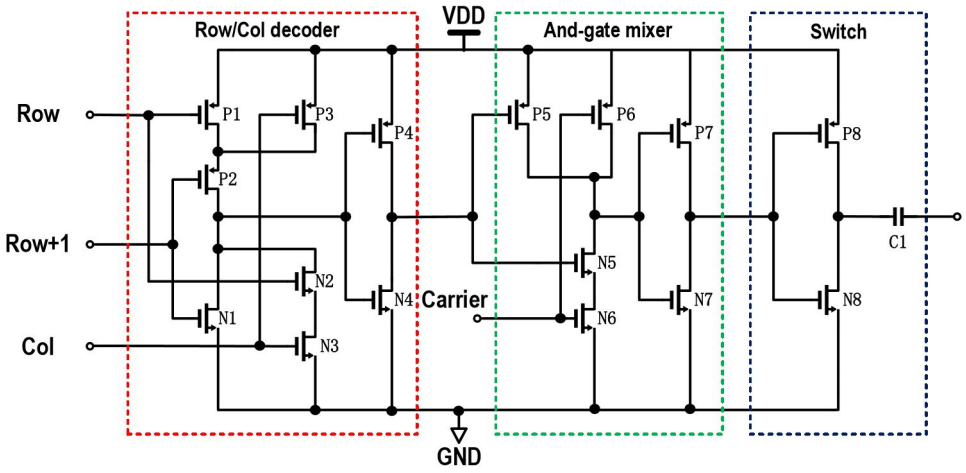

Figure 4.3: The unary unit schematic of 6-MSB and 4-LSB sub-DACs

Determined by three column/row selecting signals that originated from the binary-to-thermometer encoders, the output of the row/column decoder determines whether this specific unary cell turns on or off, which contributes to the output voltage. The mathematical relationship of the row/column decoder is expressed as follows:

$$Out = Row_{+1} + (Row \cdot Col). \tag{4.1}$$

The digital mixer is a two-input bitwise AND-gate circuit, which is driven by the output of the row/column decoder together with the LO clock. This carrier signal is a square-wave pulse controlled by the row-clock-gating circuitry. When the output of the row/column decoder is "1", the mixer generates a switching signal, which further drives the last CMOS switch that can be regarded as an inverter. By switching between supply voltage, V_{DD}, and the ground, a square wave is generated at the left plate of the connected capacitor while the right plate is connected to the followed balun transformer. The capacitance in MSB unit cell is 33.3 fF whereas the capacitance in LSB unit cell is 2.1 fF. The sizes of all transistors in 6-bit and 4-bit unary cells of sub mixing-DAC are given in the table 4.1 and 4.2.

Table 4.1: The 6-bit MSB transistor sizing.

PMOS	P1	P2	P3	P4	P5	P6	P7	P8
W/L (nm/nm) (MSB Unit)	600 /40	1200 /40	600 /40	600 /40	1200 /40	1500 /40	3600 /40	11200 /40
W/L (nm/nm) (LSB Unit)	240 /40	480 /40	240 /40	240 /40	120 /40	120 /40	225 /40	700 /40

Table 4.2: The 4-bit MSB transistor sizing.

NMOS	N1	N2	N3	N4	N5	N6	N7	N8
W/L (nm/nm) (MSB Unit)	300 /40	600 /40	600 /40	600 /40	1500 /40	1500 /40	1800 /40	5600 /40
W/L (nm/nm) (LSB Unit)	115 /40	230 /40	230 /40	115 /40	120 /40	120 /40	900 /40	3500 /40

It is noteworthy to mention that, instead of putting the designated capacitor in the unit cell, there is an alternative choice to put the capacitor outside and place them collectively as a consolidated capacitor. Nevertheless, as shown in Figure 4.4, the first approach, the chosen topology in this project, due to shorter routing lines, reduces the parasitic capacitance, C_{para}, at the common plate of the capacitors. According to the equation 3.1, the peak V_{out} at the load is recalculated as follows:

$$V_{out} = \frac{2}{\pi} \cdot \left(\frac{NC_0}{NC_0 + C_{para}}\right) \cdot V_{DD} \tag{4.2}$$

Theoretically, the drain efficiency drops 19 % from the original value assuming that the ratio, $\frac{NC_0}{NC_0+C_{para}}$, is 0.9, which is from layout perspective is extremely challenging. Thus,

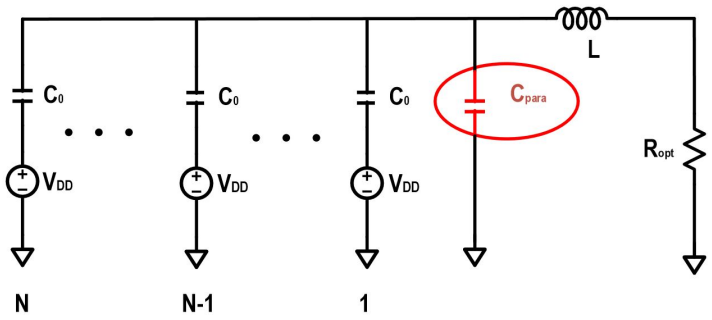

Figure 4.4: Routing parastic capacitance at the capacitors common plate

the lower C_{para} of this topology is desired and improves the peak RF power/drain efficiency performance. Additionally, in the second approach, the linearity is significantly degraded due to the inferior matching among the unary cells. Because the different positions of the unary cells lead to the huge difference among the routing lines that connect in the layout the CMOS switches and the capacitors together. In other words, the consolidated capacitor structure intensifies the unit divergence which induces more undesired AM-to-AM and AM-to-PM errors. Moreover, the irregular and asymmetric routings of the second approach is area-inefficient. Considering these two disadvantages, the capacitor-decentralization unary cell is finally adopted in this master project to obtain a superior matching and cost-efficient switched-capacitor RF-DAC.

4.2.3. DIGITAL LOGICS

The segmented mixing-DAC comprises several digital logic circuitries. The schematic details of the binary-to-thermometer encoder, the DFF, and the row-clock-gating circuit are introduced in following sections.

BINARY-TO-THERMOMETER DECODER

As stated earlier, the binary-to-thermometer encoders are needed for generating row/column selecting signals for the 6-bit/4-bit MSB thermometer-ceded sub mixing-DACs. For the 4-bit LSB sub-DAC, a 2-to-3 binary-to-thermometer encoder is utilized, which consists of a bitwise OR gate, a bitwise AND logic, and a buffer. By doing OR operation of the A_0 and A_1 inputs, BB_0 , the LSB of thermometer code, is generated whereas doing AND operation of those inputs yields BB_2, the MSB of the code. BB_1 is equal to A_1, hence only a buffer is used for synchronizing the outputs, $B_{[2..0]}$. The 3-to-7 binary-to-thermometer encoder is required for the 6-bit MSB sub-DAC. First, a 2-to-3 binary-to-thermometer encoder is utilized to generate the intermediate signals of $BB_{[2..0]}$. Then, the LSB output bits ,$B_{[2..0]}$ are generated by bit-wise OR operation of $BB_{[2..0]}$ and $A_{[2]}$ while the MSB output bits, $B_{[6..4]}$ are made by bit-wise AND operation of $BB_{[2..0]}$ and $A_{[2]}$. Since $B_{[3]}$ is equal to $A_{[2]}$, an additional buffer is incorporated to synchronize all output bits. In practice, extra buffers are applied in the 2-to-3 binary-to-thermometer encoder to reasonably synchronize all row/column signals both in the 4-/6-bit LSB/MSB sub mixing-DAC, respectively. In other words, they are employed due to the presence of more intermediate

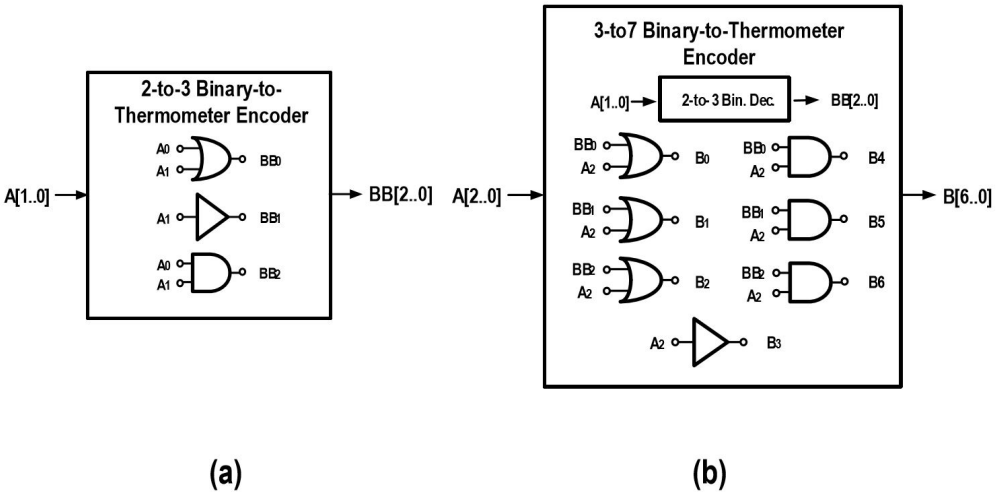

Figure 4.5: (a) The 2-to-3 binary-to-thermometer encoder (b) The 3-to-7 binary-to-thermometer encoder

stages in the 3-to-7 binary-to-thermometer encoder chain. It worth mentioning that all gates used above are set to minimum size to save the power consumption.

D FLIP-FLOP

DFFs are employed for two essential purposes: 1- For the complementary sampling clocks of the RF-DAC to implement the two-fold interpolation technique, 2- For synchronization of all row/column signals of 4-/6-bit LSB/MSB sub mixing-DAC, respectively. This synchronization is critical for seamless amplitude modulation. As shown in the Figure 4.6 (a), the DFF consists of two series latches that operate in a master-slave configuration. The circuit schematic of DFF latch is depicted in Figure 4.6(b). It operates as follows: When CLK is at low, a two-stage cascaded inverters composed of four outer transistors are transparent and the D input data is transferred to the output node, Q. Once CLK goes high, the top pass-gate logic, consisted of N4/P3, is activated leading to a cross-coupled latch configuration of the two inverters. In this phase, also called opaque mode, the bottom pass-gate logic, consisted of P4/N3, is off and the previous date input is stored/latched in the output node. The complementary clocks are required for this pass-gate-based latch. As discussed before, complementary clocks are used for the interpolation, which are generated by the phase alignment circuit from a single-ended digital clock signal.

ROW-CLOCK-GATING

As mentioned above, the clock-gating circuit is employed to save power consumption and reduce clock feedthrough to the RF-DAC output. In this project, the row-clock-gating is a combination of a bit-wise AND logic with the following buffer. When the row-select signal is high, the LO is applied to the unary cells of the designated row. One

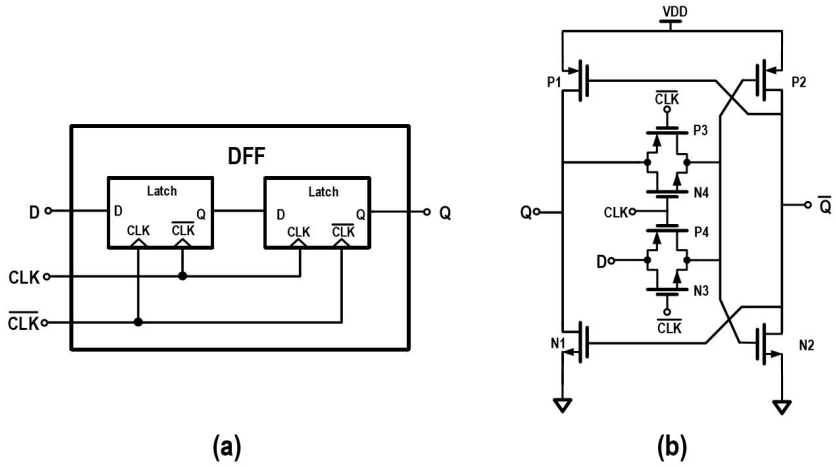

Figure 4.6: (a) The D flip-flop; (b) The latch schematic.

critical aspect of the row-selecting mechanism is related to the bit-wise AND mixing operation inside each unary cells. As stated earlier, its two inputs are the row/column decoder output and the LO clock. To accomplish an impeccable frequency up-conversion, the LO clock must arrive sooner than the data signal does. However, due to a time delay introduced by the row-clock-gating stage, the LO clock arrives later than the data signal resulting in incomplete digital mixing operation. To mitigate this issue, a bitwise logic is incorporated between the DFF that retimes row signal and the row-clock-gating as depicted in the Figure 4.7. Doing so, the gated LO clock is generated one sampling clock earlier than the row signal resulting in a seamless digital mixing operation.

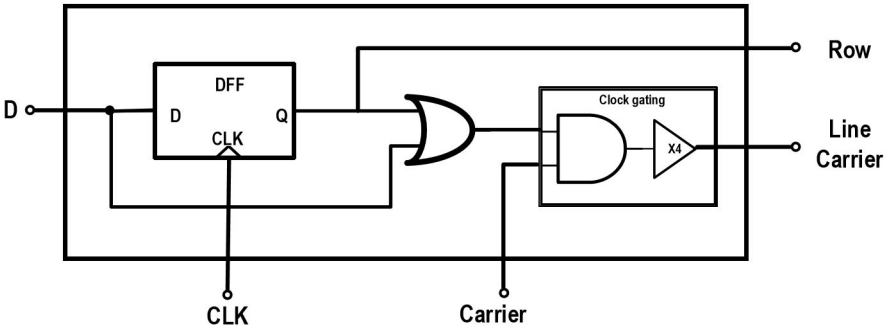

Figure 4.7: The DFF and row-clock-gating time synchronization.

4.3. MEMORY DESIGN AND IMPLEMENTATION

A memory is indispensable for storing an ultra-high-speed baseband IR-UWB pulses while an alternative approach is to generate this pulse off-chip. However, to apply these ultra-high-speed baseband data to the chip, high-speed I/O circuitries are required that are not available in this project. Thus, an on-chip self-made ROM is designed to store the predefined digital baseband IR-UWB pulse. As shown in the Figure 4.8, an address decoder is employed for generating address signals, $S_{[7..0]}$, that sequentially control the output of the ROM. The following stage is a 4-to-1 Mux which exploited for the interpolation. As discussed at the beginning of this chapter, when $D_{[in]}$ is high, the IR-UWB is in the pulse generating mode. In this phase, the corresponding address signals control the ROM, continuously providing the baseband IR-UWB pulse information. Nevertheless, when $D_{[in]}$ is low, the ROM stops generating the IR-UWB signal, and in fact, the circuit is in the silence mode. Figure 4.8 illustrates a single-bit-ROM, consists of four single-slice ROMs, which is exclusively designed for this master project.

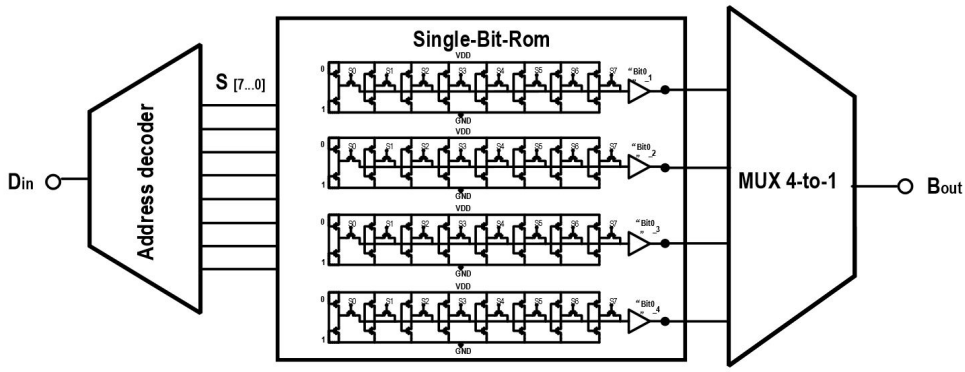

Figure 4.8: The single-bit-ROM combined with the address decoder and the 4-to1 Mux.

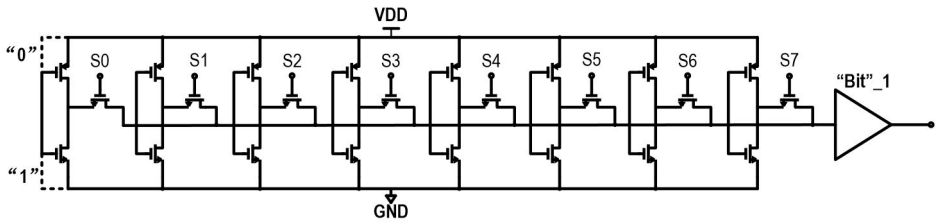

Figure 4.9: A single-slice ROM.

A single-slice-ROM is shown in Figure 4.9, which has 8 states that are controlled by $S_{[7..0]}$, respectively. When $S_{[0]}$ is high while the $S_{[6..0]}$ are low, the output of this single-slice-ROM is only determined by the first state which is either "1" (the ground-connected gate) or "0" (the supply-connected gate). The second state is delivered to the rom slice output when $S_{[1]}$ is high and the rest of address signals are low. The rest of 6 states are also operated similarly. Note that $S_{[6..1]}$ contain the IR-UWB pulse information while the two peripheral bits, i.e., $S_{[7]}$ and $S_{[0]}$, carry silence information. As shown in the Figure 4.8, there are four single-slice ROMs in a single-bit-ROM. Thus, the 10-bit resolution results in total 40 single-slice-ROMs that are controlled by $S_{[7..0]}$. The 10-bit ROMs that contain digital baseband IR-UWB pulse, $S_{[6..1]}$, and silence information are depicted in Table 4.3 and 4.4.

Table 4.3: The 10-bit ROM ($Bit_{[0..4]}$).

Bit "0"	S0	S1	S2	S3	S4	S5	S6	S7
Single-slice-ROM 1	0	0	1	0	1	0	0	0
Single-slice-ROM 2	0	1	1	0	0	0	1	0
Single-slice-ROM 3	0	1	0	0	0	1	1	0
Single-slice-ROM 4	0	0	0	1	0	1	0	0

Bit "1"	S0	S1	S2	S3	S4	S5	S6	S7
Single-slice-ROM 1	0	1	1	0	1	1	1	0
Single-slice-ROM 2	0	0	0	1	0	1	1	0
Single-slice-ROM 3	0	1	1	0	1	0	0	0
Single-slice-ROM 4	0	1	1	1	0	1	1	0

Bit "2"	S0	S1	S2	S3	S4	S5	S6	S7
Single-slice-ROM 1	0	0	0	0	0	0	1	0
Single-slice-ROM 2	0	1	0	1	1	0	1	0
Single-slice-ROM 3	0	1	0	1	1	0	1	0
Single-slice-ROM 4	0	1	0	0	0	0	0	0

Bit "3"	S0	S1	S2	S3	S4	S5	S6	S7
Single-slice-ROM 1	0	1	1	0	1	0	0	0
Single-slice-ROM 2	0	0	0	1	1	1	1	0
Single-slice-ROM 3	0	1	1	1	1	0	0	0
Single-slice-ROM 4	0	0	0	1	0	1	1	0

Bit "4"	S0	S1	S2	S3	S4	S5	S6	S7
Single-slice-ROM 1	0	0	0	1	1	1	0	0
Single-slice-ROM 2	0	1	1	1	1	1	1	0
Single-slice-ROM 3	0	1	1	1	1	1	1	0
Single-slice-ROM 4	0	0	1	1	1	0	0	0

Table 4.4: The 10-bit ROM ($Bit_{[5..9]}$).

Bit "5"	S0	S1	S2	S3	S4	S5	S6	S7
Single-slice-ROM 1	0	0	0	1	1	0	0	0
Single-slice-ROM 2	0	0	1	1	1	1	0	0
Single-slice-ROM 3	0	0	1	1	1	1	0	0
Single-slice-ROM 4	0	0	0	1	1	0	0	0

Bit "6"	S0	S1	S2	S3	S4	S5	S6	S7
Single-slice-ROM 1	0	0	0	0	1	0	1	0
Single-slice-ROM 2	0	0	1	0	0	1	0	0
Single-slice-ROM 3	0	0	1	0	0	1	0	0
Single-slice-ROM 4	0	1	0	1	0	0	0	0

Bit "7"	S0	S1	S2	S3	S4	S5	S6	S7
Single-slice-ROM 1	0	0	1	1	1	0	0	0
Single-slice-ROM 2	0	0	1	0	1	0	0	0
Single-slice-ROM 3	0	0	0	1	0	1	0	0
Single-slice-ROM 4	0	0	0	1	1	1	0	0

Bit "8"	S0	S1	S2	S3	S4	S5	S6	S7
Single-slice-ROM 1	0	0	0	0	1	0	0	0
Single-slice-ROM 2	0	0	0	1	1	1	0	0
Single-slice-ROM 3	0	0	1	1	1	0	0	0
Single-slice-ROM 4	0	0	0	1	0	0	0	0

Bit "9"	S0	S1	S2	S3	S4	S5	S6	S7
Single-slice-ROM 1	0	0	0	1	1	1	0	0
Single-slice-ROM 2	0	0	0	1	1	0	0	0
Single-slice-ROM 3	0	0	0	1	1	0	0	0
Single-slice-ROM 4	0	0	1	1	1	0	0	0

4.3.1. ADDRESS DECODER

The required address signals, $S_{[7..0]}$, for ROM are generated by an address decoder as shown in Figure 4.10. To produce $S_{[7..0]}$, the intermediate signals of $D_{[3..1]}$ are generated using three bit-wise AND gates while their inputs are C1/$D_{[in]}$, C2/$D_{[in]}$ and C3/$D_{[in]}$, respectively. Note that C1, C2, and C3 are 125, 250, and 500 MHz clocks, respectively. As depicted in Figure 4.10, the complementary signal of $D_{[3..1]}$ are generated employing three phase aligners. When Din is at high voltage, these three clocks are delivered to the phase alignment circuit that transfers a single signal to its differential counterparts. As shown in Figure 10, the resulted 6 intermediate signals, D1, D2, D3, $\overline{D1}, \overline{D2}, \overline{D3}$, have eight different combinations in one cycle of the 125MHz clock. By properly bit-wise ANDing these intermediate signals, the $S_{[7..0]}$ are generated. In this context, first S_0 is high and the rest is low. In the next half cycle of C3, S_1 will be high, and the rest of the bits will be low. In other words, in each half cycle, only one bit is high. Stated differently,

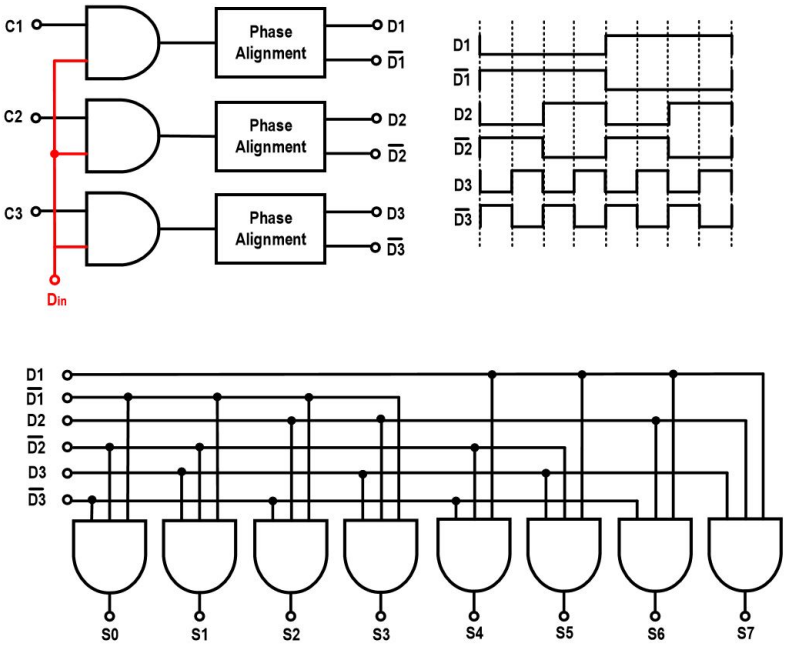

Figure 4.10: The address decoder.

the resultant controlling signals are eight 12.5% duty-cycle clocks operating at 125 MHz and a relative phase difference in multiples of 45 degrees. This operation will repeatedly be executed until D_{in} will be low. Then, the silence mode will be started. Note that in the silence mode S_7 is high and the rest is low. The schematic of the phase alignment circuit is depicted in Figure 4.11. Moreover, the required clocks, C1, C2, C3, They are generated

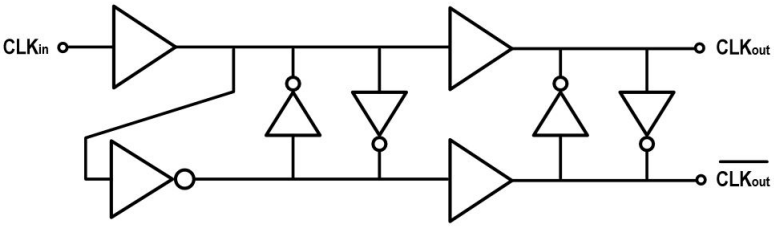

Figure 4.11: The phase alignment circuit.

by applying a 4 GHz off-chip clock to a cascade of 5 divide-by-2 circuitries. Depicted in Figure 4.12, a divide-by-2 circuit is implemented incorporating a DFF in a negative feedback loop. In this context, the complementary output node of $\overline{Q}$ is connected to the input D node.

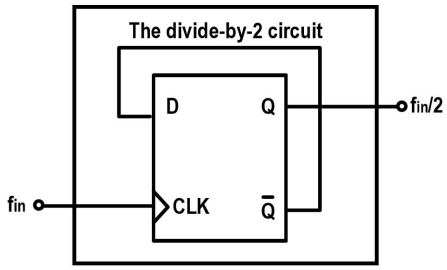

Figure 4.12: The divide-by-2 circuit

4.3.2. 4-TO-1 MUX

The 4-to-1 MUX is employed for the up-sampling operation and it is depicted in Figure 4.13. The inputs, B1, B2, B3, B4, are the outputs of the four single-slice ROMs in a single-bit-ROM, respectively. The 4-to-1 mux are controlled by two pairs of complementary clocks, A0 / $\overline{A0}$ and A1/$\overline{A1}$. A0 operates at 1 GHz while A1 runs at 2 GHz. Similar to

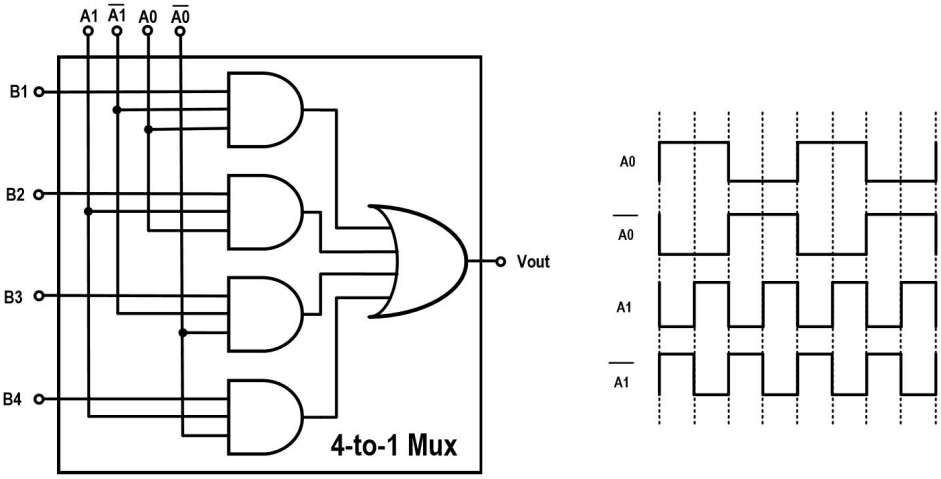

Figure 4.13: The 4-to-1 MUX.

the address decoder, the combination of the pair of two complementary clocks repeatedly generates four different states at the rate of 4 GS/s. In other words, the resultant controlling signals are four 25% duty-cycle sampling clocks operating at 1 GHz and a relative phase difference in multiples of 90 degrees. The first combination enables the connection of B1 to V_{out} while B2, B3, B4 disconnected from V_{out} due to the bit-wise AND operation of these signals with the corresponding control signals, A0/A1, generating "0" signal for the bit-wise OR logic. Sequentially, , V_{out} is connected to B2, B3, B4 respectively. Note that, the complementary clocks of A_0 and A_1 are produced by phase

alignment circuitries whose input clocks are generated using cascaded divided-by-two circuits.

4.4. TRANSFORMER

Figure 4.14 illustrates the layout of the employed balun, which is an octagonal transformer. The turns ratio is 1:1, where the inner/outer diameter is 100/130 um, respectively. The track width of the primary and the secondary sides are both 6 um, whereas the track spacing between primary and secondary coils is 3 um. The equivalent circuit of the transformer, based on fundamental concepts on a transformer [31], disregarding the overlap capacitors and substrate losses due to magnetic/electric fields, is shown in the Figure 4.15. Where the Km is the magnetic coupling factor between two coils, the

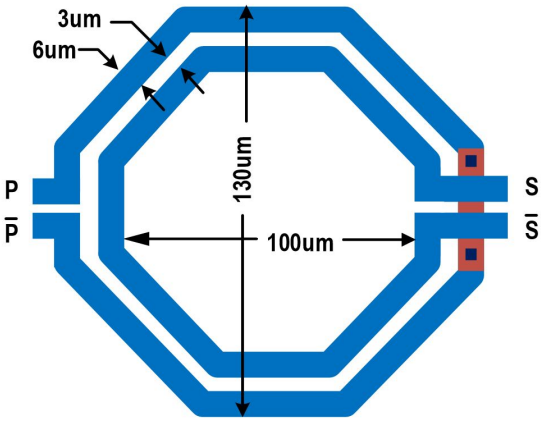

Figure 4.14: The layout of the transformer.

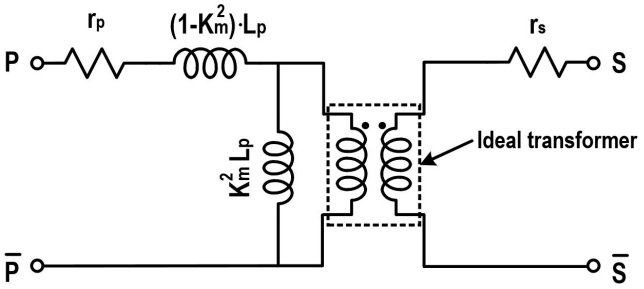

Figure 4.15: The equivalent circuit of the transformer.

Lp is the self-inductance seen from primary side, r_p and r_l are ohmic losses due to track traces in the primary and secondary coils, respectively.

4.5. TOP-LEVEL LAYOUT

The proposed switched-capacitor RF-DAC is implemented in 40-nm Global Foundaries LP CMOS process. The chip area is 1x0.85 mm^2. The top-level layout of the proposed IR-UWB pulse generator is shown in Figure 4.16.

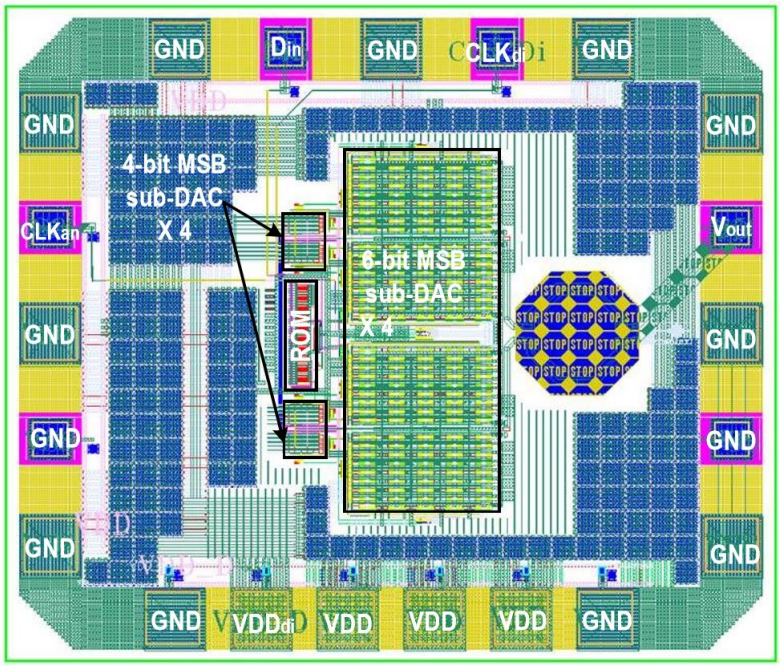

Figure 4.16: Top-level layout of the proposed pulse generator.

5

SIMULATION RESULTS

This chapter presents the simulation results of the whole system. Section 5.1 exhibits the static and dynamic performance of switched-capacitor RF-DAC at the schematic level. Section 5.2 illustrates the transient and the spectral post-layout simulation results of the proposed IR-UWB pulse generator. Moreover, the power consumption breakdown as well as the system efficiency are presented in Table 5.1. Finally, Table 5.2 compares the state-of-the-art with the proposed impulse-radio ultra-wideband pulse generator.

5.1. RF DAC SIMULATION RESULTS

5.1.1. OUTPUT POWER AND EFFICIENCY SIMULATION

Figure 5.1 (a) demonstrates the output power versus digital input code at two carrier frequencies of 6.5/8 GHz, respectively. As can be seen, due to the reasonably linear behavior of the output node voltage versus input code, the related output power follows a quadratic function of the digital input code. The peak RF output power at 6.5 and 8 GHz carrier frequencies are 59.4 mw (17.74 dBm) and 52 mw (17.1 dBm), respectively. They are both higher than the targeted specification, i.e., 15 dBm. Moreover, the drain efficiency and system efficiency are shown in Figure 5.1 (b) and (c), respectively. The peak drain efficiency at 6.5 GHz is 37.2 % while it is 33.4 % at 8 GHz. However, due to the large parasitic gate capacitance, C_g, of CMOS switches, the preceding data/clock driver circuitries consume significant power. Thus, the SC RF-DAC peak system efficiency degrades to 29.7% and 26.8% at both 6.5/8 GHz, respectively. Note that, the digital logics,

binary-to- thermometer encoders, and row-clock-gating circuit contribute to the degradation of the system efficiency. In the proposed IR-UWB pulse generator only 7.5/6.6% of the total power at 6.5/8 GHz, respectively, consumed by the drivers of CMOS switches and the remainder of the power consumed by the rest of digital circuitries. Nevertheless,

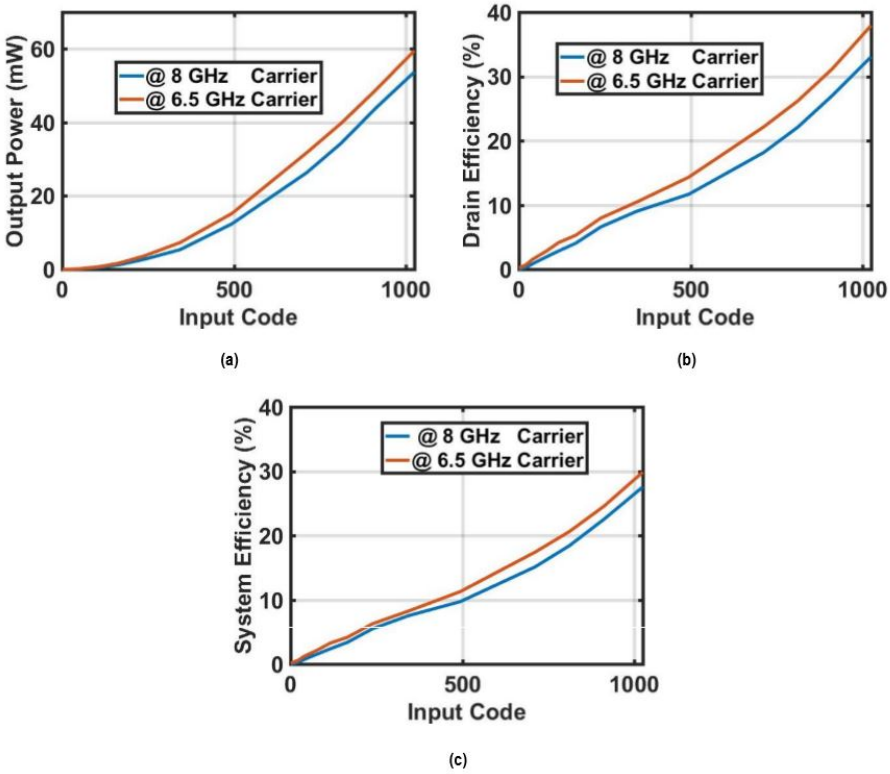

Figure 5.1: (a) Output power versus input code. (b) Drain efficiency versus input code. (c) System efficiency versus input code.

the post-layout simulation results of both the system efficiencies indicate dramatic degeneration as opposed to the schematic-level counterpart. The post-layout peak system efficiencies are 17.8% and 14.3% at 6.5/8 GHz, respectively. Moreover, the peak output power at both 6.5/8 GHz are 16/15 dBm, respectively. Thus, the performance of the proposed system strongly depends on the layout of the entire SC RF-DAC. In particular, the clock/data metal routings significantly affect the performance of the proposed pulse generator.

Thus, proper routing and layout design are desired. In other words, to decrease the associated parasitic capacitance of the metal routing, one can use the higher metal layers (metal six or seven) due to their larger distance with respect to the substrate. However, the minimum width of these metal layers is around 0.4 um. Thus, they cannot be

employed as the clock distribution metal routings of mixing-DAC matrices due to their minimum metal width leading to a significant growth in the area of the four mixing-DAC matrices. Therefore, the next best option is to utilize metal five which has a smaller minimum width, less metal area, along with a shorter distance to the substrate. It is worth mentioning again that, as discussed in Chapter 4, the RF output power dramatically degenerated by the parasitic capacitance of the top-plate capacitor of the CMOS switch.

5.1.2. AM-AM AND AM-PM SIMULATION

Figure 5.2 (a) and (b) exhibit the schematic-level AM-AM and AM-PM performance of the proposed IR-UWB pulse generator at 6/7.25/8 GHz, respectively. According to Figure 5.2(a), the AM-AM curves are quite linear with insignificant distortion, which confirms the linear behavior of switched-capacitor configuration. Since this performance

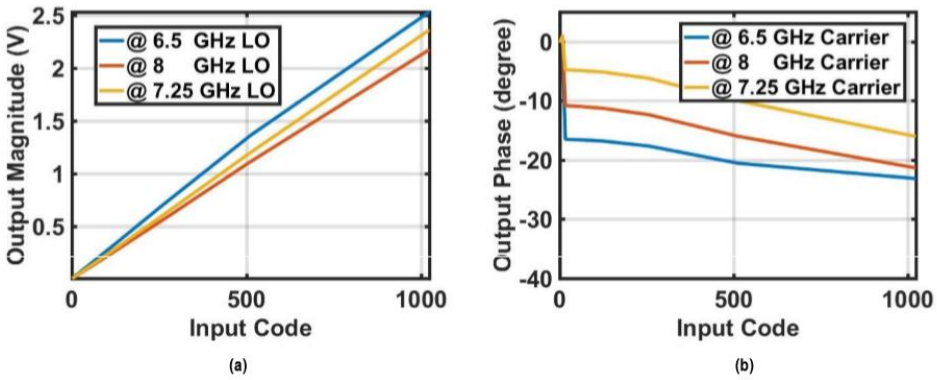

Figure 5.2: (a) AM-AM simultion at 6.5, 7.25, and 8 GHz; (b) AM-PM simultion t 6.5, 7.25, and 8 GHz.

is mostly related to the switches and capacitor voltage-division circuitries, this structure considerably benefits from technology scaling. In contrast, the AM-PM characteristic demonstrates considerable distortion. As a result, a significant contributor of spectral impurity originated from AM-PM distortion. The AM-PM nonlinear behavior of the switched-capacitor structure may be related to the code-dependent performance of the CMOS switch [41], [42]. Stated differently, as depicted in Figure 3.10, the CMOS switch parasitics, including r_{on} and C_{sw}, strongly depend on the NMOS/PMOS aspect ratio. In switched-capacitor RF-DAC, the switch parasitic depends on the input code word. At maximum input code, all CMOS switches are on leading to a minimum on-resistant. This indicates that the CMOS switch array's impedance is significantly low (r_{on}<1 Ω). However, at smaller input code word, due to a substantial on-resistance, the parasitic capacitance of the switch contributes significantly leading to a notable phase shift. In reality, due to dynamic variation of the input baseband code, the switch parasitics dynamically shift from the resistive parasitic to the capacitive counterpart [30].Note that at 7.25 GHz, the phase approximately varies 16 degrees while it shifts 23/21 degrees at 6.5/8 GHz, respectively. Since the tank of matching network, consisting of the C1 and

transformer in Figure 3.9, resonates at 7.25 GHz, the AM-PM profile of the proposed IR-UWB pulse generator is superior at its resonant frequency than at either of 6.5 and 8 GHz carrier frequencies.

Moreover, the AM-AM and AM-PM distortion profiles are simulated at three different loading conditions namely, 25,75 and 100 Ω, and depicted in Figure 5.3. As demonstrated in Figure 5.3 (a)-(b), the AM-AM profiles are still reasonably linear. However, due to shifting from their optimum loading conditions, the related peak output amplitude varies compared to the 50 Ω counterpart. Nevertheless, the AM-PM distortion profiles, depicted in Figure 5.3 (c)-(d) for both 6.5/8 GHz, insignificantly affected by the load variation.

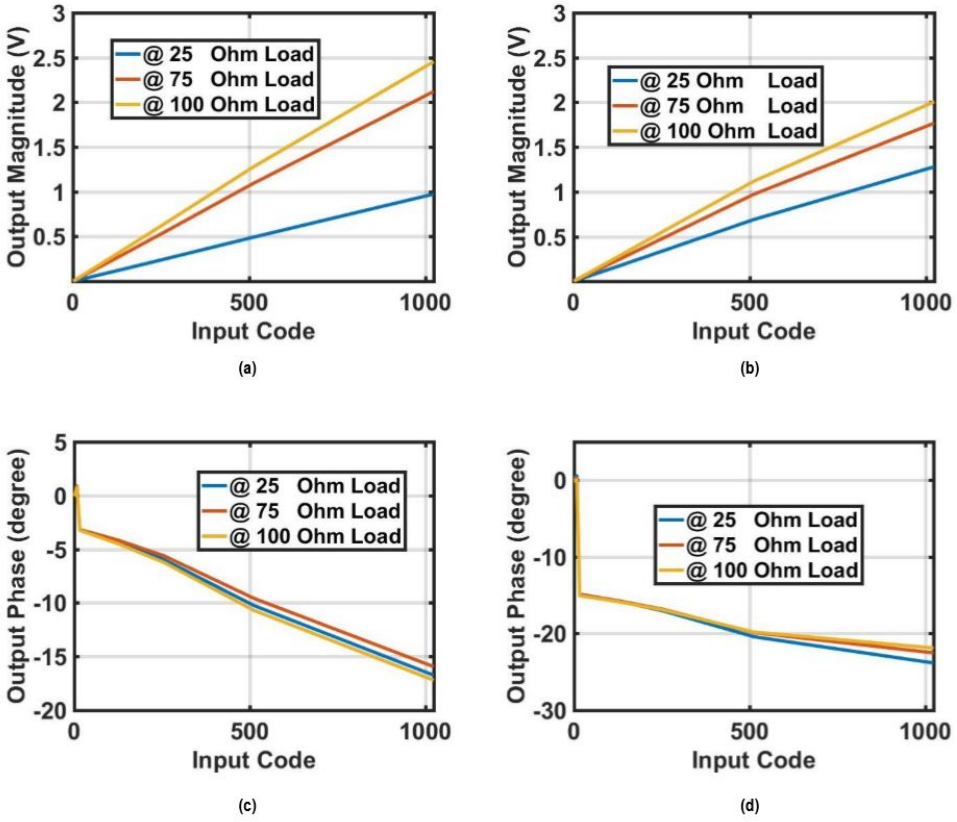

Figure 5.3: (a) AM-AM simulation with 25, 75, 100 Ohm loads at 8 GHz; (b) AM-AM simulation with 25, 75, 100 Ohm loads at 6.5 GH; (c) AM-PM simulation with 25, 75, 100 Ohm loads at 8 GHzr; (d) AM-PM simulation with 25, 75, 100 Ohm loads at 6.5 GHz.

5.1.3. TWO-TONE SIMULATION

A two-tone simulation verifies the spectral performance of the proposed switched-capacitor RF-DAC. The SC RF-DAC is a polar RF-DAC. Thus, the baseband complex data first converted into an envelope and a phase using a CORDIC [add the following reference]. The phase of a carrier signal is modulated using the baseband phase information. Eventually, the SCPA front-end combines the envelope and phase paths. In the case of two-tone test, the envelope signal acts as a full-wave rectifier waveform while, in every half cycle, its phase alters between 0 and π. The two-tone with a 1 GHz tone-spacing performed at both 6.5 and 8 GHz, respectively, and the related simulation results exhibited in Figure 5.4 (a) and (c), respectively. The two main tones and the related IM3 spurs at 6.5 GHz located at 6/7 and 5/8 GHz, respectively. Moreover, at 8 GHz, they are at 7.5/8.5 and 6.5/9.5, respectively.

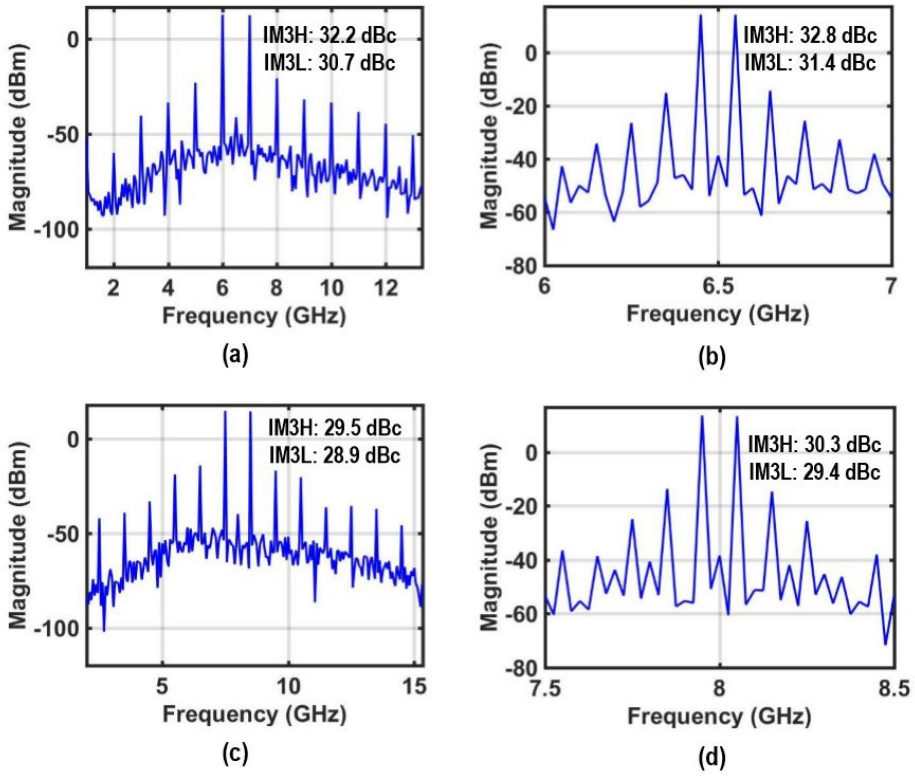

Figure 5.4: Two-tone simulations: (a) 6.5 GHz and 1 GHz tone-spacing; (b) 6.5 GHz and 100 MHz tone-spacing; (c) 8 GHz and 1 GHz tone-spacing; (d) 8 GHz and 100 MHz tone-spacing.

Based on these simulation results, the IM3-low/-high at 6.5 GHz are better than 30 dBc. At 8 GHz, however, the IM3-low/-high slightly deteriorated and they are better than 29 dBc. Moreover, the tone-spacing reduced to 100 MHz and the related simulation results depicted in Figure 5.4 (b) and (d). The resultant spectral purities are insignificantly

better than 1 GHz counterpart. This indicates that the RF-DAC performance is not much sensitive to the baseband bandwidth larger than 100 MHz. Unfortunately, smaller tone-spacings are not possible due to longer duration of simulations and multiple crashes of the workstation. As a result, the nonlinearity due to memory effect cannot be verified. The slight difference in the spectral purity of RF-DAC at 6 and 8.5 GHz arises from different AM-AM/AM-PM behaviors discussed in the previous section. Moreover, the impedance of CMOS switch array and the tank frequency response at 6.5 GHz are reasonably different respect to 8 GHz.

5.2. ULTRA-WIDE-BAND PULSE SIMULATION

This section demonstrates the post-layout simulation results. The goal of this master thesis is to implement an IR-UWB pulse generator. As stated earlier, utilizing a self-made on-chip ROM, the digital baseband UWB pulse stored in the memory. Then, this digital baseband signal continuously drives the SC RF-DAC. The transient post-layout simula-

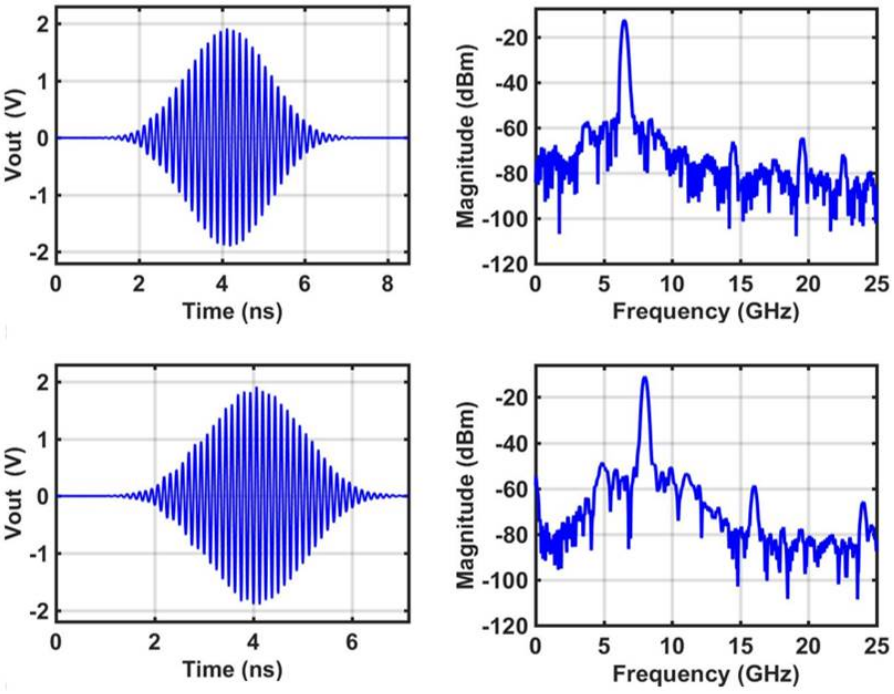

Figure 5.5: (a)UWB-IR pusle @ 6.5GHz carrier (b) Pulse spectrum at 6.5GHz carrier (c)UWB-IR pusle @ 8GHz (d) Pulse spectrum @8GHz carrier

tion results of the UWB pulse at both 6.5/8 GHz depicted in Figure 5.5 (a) and (c), respectively. The UWB pulse width is 6.5 ns which continues multiple LO clock cycles.The maximum peak-to-peak UWB pulse amplitudes at 6.5/8 GHz are 3.8/3.4 V, respectively. The related power spectral density of pulses at 6.5/8 GHz depicted in Figure 5.5 (b) and (d), respectively. As can be seen, the bandwidth of the main lob is 1 GHz. The out-of-

band spectral purity of the system at 500 MHz away from the carriers at 6.5/8 GHz are -34.9/-32.2 dBc, respectively. Therefore, the stringent spectral purity requirements imposed by FCC are met [5]. Table 5.1 exhibits the average output power of the generated pulse, the total power consumption breakdown, and the system efficiency at both 6.5/8 GHz, respectively. In contrast, when the pulse generator enters the silence mode, the average system efficiency dramatically improves due to the zero pulse generation. Let's consider a 10% duty cycle for the IR-UWB pulse generation. The average system efficiency can be expressed as follows:

$$Average \quad System \quad Effciency \quad = \quad 9.56\% \cdot 10\% + 100\% \cdot 90\% = 90.956\% \qquad (5.1)$$

Thus, the energy-efficiency of the system strongly depends on the duty cycle of an IR-UWB pulse that directly affects the battery lifetime. It is worth mentioning that one essential design parameter in IR-UWB pulse generation is pulse-repetitive frequency (PRF). As stated thoroughly in Section 4.3, due to designing a self-made ROM memory, the maximum PRF set to 125 MHz.

Table 5.1: Post-layout Level Power Performances of Proposed UWB-IR Pulse Generator

Carrier Freq.	Aver. Output Power	Core DAC Power	Digital Logic Power	Total Power	System Effi.
6.5 GHz	11 mW	86 mW	25 mW	112 mW	9.96%
8 GHz	8 mW	87 mW	29 mW	116 mW	7.16%

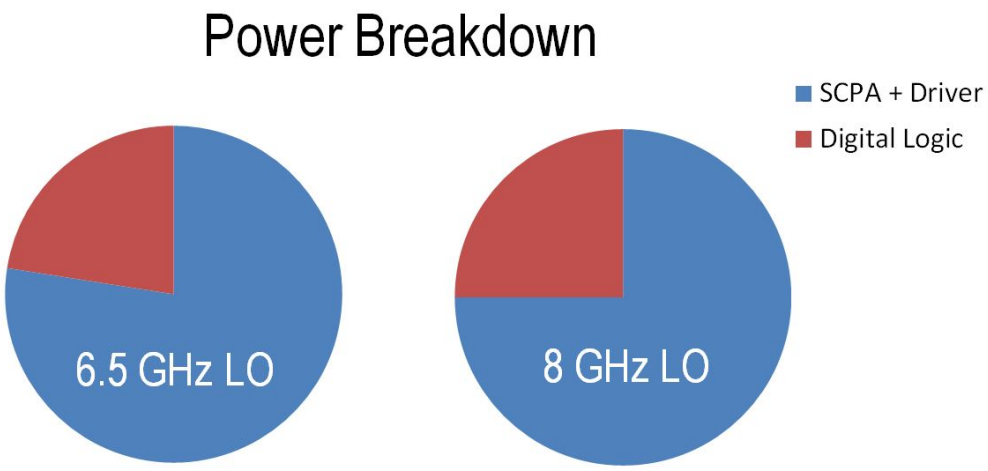

Figure 5.6: The power breakdown at 6.5/8 GHz

Besides, the spectrum comparisons of the generated UWB pulses with/without the up-sampling and two-fold techniques are shown in Figure 5.7 and 5.8, respectively. As can be seen, the spectral purity is improved by these two techniques.

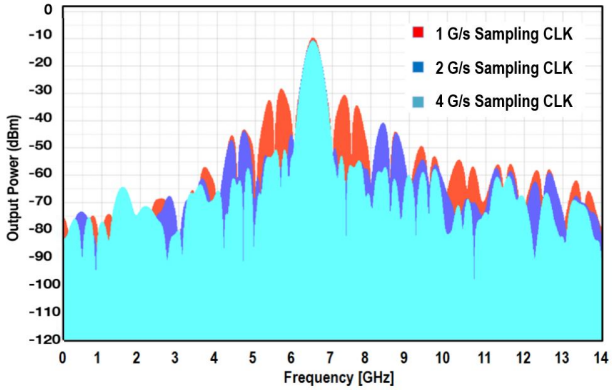

Figure 5.7: The UWB pulses' spectrum comparison with 1, 2, and 4 G/s sampling rates.

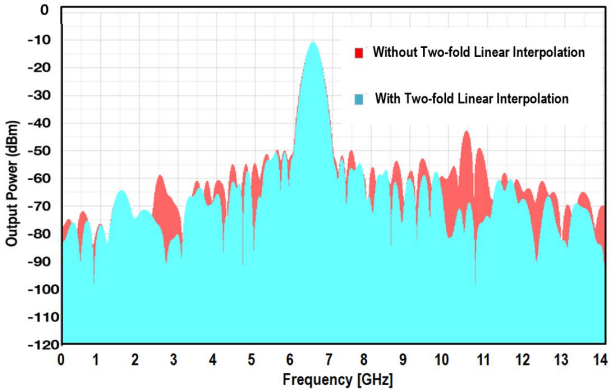

Figure 5.8: The UWB pulses' spectrum comparison with/without two-fold interpolation.

5.3. COMPARISON WITH STATE-OF-ART

Table 5.2 compares the performance of the UWB pulse generator with the state-of-the-art. Compared to the rest, the peak-to-peak amplitude is significantly larger than the other publication. Moreover, the spectral purity of the system, better than -30 dBc, is one of the considerable advantages of exploiting the proposed solution. Thus, spectral purity of the proposed RF-DAC meets the rigorous FCC outdoors standard requirements.

Table 5.2: Performances Comparison with Previously-Published Works

Ref.	CMOS Tech.	V_{DD}	Output Vpp	Pulse BW	Center Freq.	PRF	Area
[34]	65nm	1V	160mV	2.7GHz (10dB)	3.5 to 5.4GHz	333MHz	$4.5mm^2$ (die)
[32]	40nm	0.9V	583mV	1.7GHz (10dB)	7GHz	N/A	$0.012mm^2$ (core)
[37]	130nm	1.2V	1.72V	500MHz (10dB)	3.5 to 4.5GHz	10MHz	$2.88mm^2$ (die)
[38]	65nm	0.9V	126/91mV	1.4GHz (10dB)	3.1 to 5GHz	50MHz	$0.032mm^2$ (core)
This Work	40nm	1.2V	3.4/3.8V	1GHz (30dB)	6.5 to 8GHz	125MHz	$0.85mm^2$ (die)

6

CONCLUSION

6.1. THESIS SUMMARY

An impulse-radio ultra-wideband (IR-UWB) communication introduces an energy-efficient method for short-rang car application. In this thesis project, a switched-capac-itor RF-DAC based IR-UWB pulse generator is proposed and implemented in Global Froundries 40 nm CMOS process supporting three different frequency bands of 6.5, 7.25 and 8 GHz to primarily cover the European and Chinese market. The post-layout simulation results of Chapter 5 verify that the UWB pulses at both 6.5/8 GHz are compliant with the stringent spectral requirements imposed by FCC for outdoor applications. These simulation results reasonably predict the future measurement results. To meet the rigorous spectral purity of FCC and suppress the sampling spectral replicas, a switched capacitor RF-DAC along with a two-fold linear interpolation is implemented. Moreover, to enhance the regional coverage, two frequency bands of 6.5/8 GHz, a band-select matching network exploited. Doing so, the spectral purity of both 6.5/8 GHz bands are better than -30 dBc, facilitating the adoption of this architecture for outdoor applications. Moreover, by generating more than 3V peak-to-peak IR-UWB pulse amplitude, the detection range dramatically increases.

The up-sampling operation is realized employing a 4-to-1 multiplexer pushing sampling spectral replicas further away from the desired signal which mitigates the use of an explicit anti-alias filter at the expense of a higher sampling clock. Moreover, a two-fold linear interpolation adopted utilizing a pair of complementary clocks driving two identical sub mixing-DAC to suppress the sampling spectral replicas further. The two-fold interpolation adds an extra sampling point between a pair of consecutive samples which acts as a first-order hold interpolation at the second harmonic of the carrier frequency. The up-sampling by 4 in conjunction with the linear interpolation improve the out-of-band spectral purity and make the proposed IR-UWB pulse generator a strong candidate for outdoor applications. Another aspect of this master project is to achieve more than 15 dBm peak RF output power at both 6.5 and 8 GHz bands. Thus, the designated matching network must provide two optimum loads at both bands. Employing

an off-chip π matching network comprising two band-select capacitors with a fixed inductor, the desired optimum loads obtained at both bands. Additionally, this matching network further suppresses the sampling spectral replicas. It is noteworthy to mention that this matching network implemented off-chip due to the area constraint of the master project which implemented on-chip in the future development of the IR-UWB pulse generator. The details of design principles and methods to obtain the desired RF peak power along with techniques to improve the spectral purity of the proposed pulse generator thoroughly described in Chapter 3. The proposed solution is suitable for short-range applications while meeting the FCC rigorous spectral requirements of outdoor standards. The core area including the I/O pads is 0.23 mm^2 indicating a cost-effective solution together with a peak-to-peak RF pulse amplitude of more than 3V leading to a larger detection range. To further improve the performance of pulse generator, next section will recommend some techniques.

6.2. RECOMMENDATIONS FOR FUTURE WORK

One of the drawbacks of the current design is using a fixed baseband IR-UWB pulse. One can replace the ROM with multiple of interleaved SRAMs. Doing so, not only this system operates as a UWB pulse generator but also can perform as a generic TX supporting various wireless communication networks. Moreover, to further improve the performance, the addition of ultra-high-speed I/Os to enhance the baseband data rate are recommended.

To support multi-mode/multi-band standards, more innovations must be accomplished in the design of the matching network. One possible solution is to merge the balun transformer with the π matching network creating a wideband solution. Although, during the design phase, this approach was considered, due to time constraint and the scope of this master project further investigations deferred to the future development.

Finally, to include a power controlling mechanism to this chip, part of the bit resolution of the baseband data is designated for this purpose leading to an inferior dynamic range for the lower RF output power mode of operation. One suggestion is to decouple this controlling mechanism from the bit resolution using a bias controlled cascode PMOS/NMOS transistors on top of the main CMOS switch.

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