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Highly-Conformal Sputtered Through-Silicon Vias With Sharp Superconducting Transition

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***Abstract*— This paper describes the microfabrication and electrical characterization of aluminum-coated superconducting through-silicon vias (TSVs) with sharp superconducting transition above 1 K. The sharp superconducting transition was achieved by means of fully conformal and void-free DC-sputtering of the TSVs with Al, and is here demonstrated in up to 500 μm-deep vias. Full conformality of Al sputtering was made possible by shaping the vias with a tailored hourglass profile, which allowed a metallic layer as thick as 430 nm to be deposited in the center of the vias. Single-via electric resistance as low as 160 mΩ at room temperature and superconductivity at 1.27 K were measured by a three-dimensional (3D) cross-bridge Kelvin resistor structure. This work establishes a CMOS-compatible fabrication process suitable for arrays of superconducting TSVs and 3D integration of superconducting silicon-based devices. [2020-0354]**

***Index Terms*— Aluminum, cryogenic, interconnects, sputtering, superconducting, through-silicon vias.**

I. Introduction

SUPERCONDUCTING through-silicon vias (TSVs) are vertically interconnecting electric structures that have attracted the attention of both scientists and engineers interested in linking microelectronic integrated circuits (ICs) with quantum computing devices, THz-range electromagnetic sensors or microelectromechanical systems (MEMS) that operate in cryogenic regimes [1]. TSVs are generally used as means to connect devices that are on the top surface of a silicon wafer with devices that are on the bottom surface of the same wafer [2]. Alternatively, thin silicon layers featuring TSVs can be interposed between functional layers for the same purpose [3]. In line with such three-dimensional (3D) integration approach, interposers featuring superconducting TSVs represent a key element to pursue the fabrication and assembly of large, scalable and densely integrated superconducting systems. In-demand instances of the latter are *e.g* high-density quantum computing systems, where the layer implementing quantum bits (qubits) needs to be bridged to the microelectronic control layer [4] (Fig. 1). The latter typically requires CMOS-based circuitry compatible with cryogenic temperatures (*i.e.*, cryo-CMOS) [5] for the control and readout of the many physical qubits needed to implement error-tolerant logical qubits.

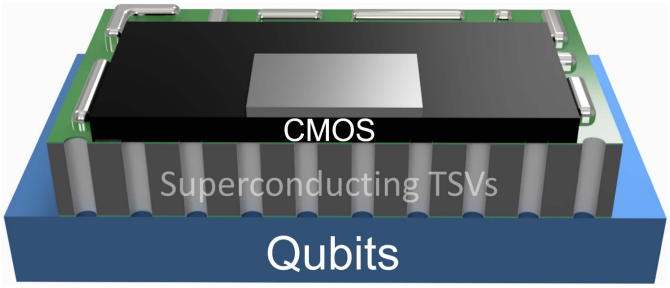

Fig. 1. Sketch of the proposed 3D integration concept for high-density silicon-based quantum computing systems, including a qubit-based layer, an interposer layer featuring TSV-based vertical superconducting interconnects, and a cryo-CMOS circuitry layer for the control and readout of the qubits.

Several works in literature have described a variety of approaches to deploy superconducting interposers [6]–[14], including our previous investigations [15], [16]. Foxen *et al.* [7] used indium bumps as electrical interconnects between two planar devices with aluminum wiring. They reported a superconducting transition at 1.1 K. Despite the advantage of low thermal budget for the process, the use of In, classified as contaminating metal in conventional CMOS technology, limits the possibility of integration with Si-based qubits and control electronics. Rosenberg *et al.* [14] developed 200 μm-deep blind vias in a 725 μm-thick silicon wafer. The vias were lined with TiN using chemical vapor deposition (CVD) and the wafers thinned down to 200 μm. The measured superconductivity at 2.5 to 3 K was not associated with a clear transition. Vahidpour *et al.* [8] demonstrated the fabrication of 250 μm-deep Al-coated TSVs with a superconducting transition below 1.2 K. The vias were etched on the backside of the Si wafer by inductively-coupled plasma

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and isotropic etching, obtaining a sloped-wall via geometry with diameter shrinking from about 200 μm on the bottom to 50 μm on the top side of the wafer. Taking advantage of the sloped profile, Al was deposited by electron-beam evaporation from the backside, and Parylene C was sputtered to fill the via from the same side. Subsequently, an etch-stop oxide layer was removed from the top via side, and the metallization step was repeated. In this interesting process for low aspect-ratio TSVs the size of the holes constrained the integration density of devices per wafer, whereas Parylene-C processing is not compatible with conventional CMOS technology. Grigoras *et al.* [11] fabricated arrays of 60 μm diameter TSVs coated with TiN by means of atomic layer deposition (ALD) in 495 μm-thick Si wafers, achieving a superconducting transition at around 1.6 K. ALD is a CMOS-compatible technique particularly advantageous to deposit few nm-thick metal layers with precise control. However, ALD is also a slow coating process, which would require numerous deposition cycles to achieve superconducting layer thicknesses in excess of *e.g.* the London penetration depth of at least 50 nm typically required to effectively shield the core of superconductors from magnetic fields [8], consequently reducing wafer processing throughput significantly.

It is worth noting that all approaches reviewed above produce functional superconducting TSVs. However, as noted they often involve fabrication methods that are slow or not compatible with conventional CMOS microfabrication or do not result in sharply defined TSV superconducting transitions.

We have previously demonstrated the fabrication of high aspect-ratio (HAR) superconducting TSVs using sputtered aluminum [15], [16]. Sputter deposition is a physical vapor deposition technique used for the deposition of thin films. Metallic layers are commonly deposited by means of this technique in IC and MEMS fabrication processes. Besides being compatible with CMOS processing, sputtering offers homogeneous and highly reproducible coatings with controlled deposition rates at different platen temperatures and gas concentrations. Additionally, it allows faster deposition of thick layers in comparison to other techniques such as ALD. This technology is also used in TSVs, mainly for the deposition of metallic seed layers required in *e.g.* copper electroplating [17]–[19]. Conformality of metal layers over structured substrates is extremely important to guarantee continuity and high electrical conductivity, particularly for extreme topographical structures such as vertical interconnects [2], [20]. The realization of TSVs with funnelled profile and sputtered Al enabled us to fabricate high-density superconducting interposer layers. We achieved a superconducting transition between 1.28 and 1.36 K, making the technology suitable for quantum applications or multi-tier stacking. The lowest electrical resistance measured at room temperatures was 80.4 mΩ, a value suitable for most MEMS applications, including notably the integration of MEMS and ICs. Nevertheless, we could not obtain a single, sharp superconducting transition in the cryogenic regime, as we instead measured a tight sequence of multiple superconducting transitions. We attributed this shortcoming to a non-uniform thickness of the metallic stack along the full

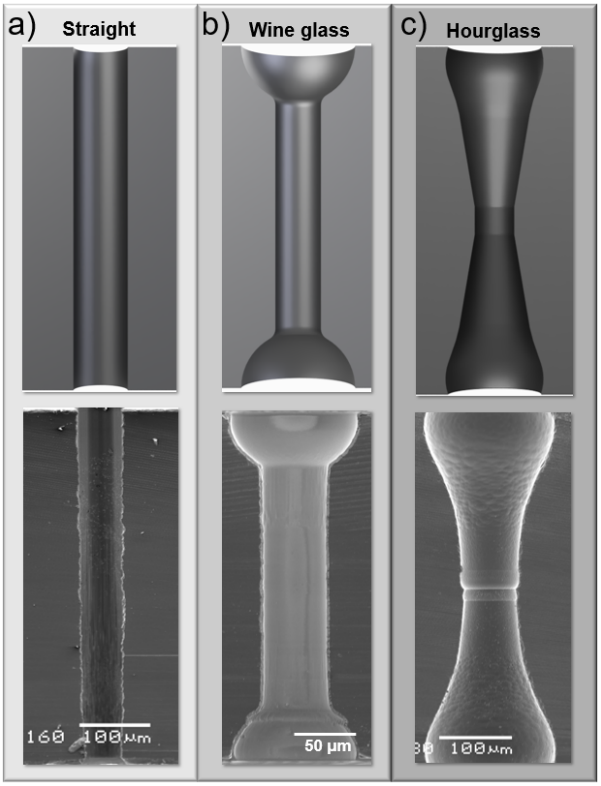

Fig. 2. Sketch (top) and corresponding scanning electron microscope (SEM) images (bottom) of the three types of fabricated and tested TSV geometries: (a) cylindrical, (b) wine glass-shaped, (c) hourglass-shaped.

interconnect path, moving from the flat wafer surface across the funnel to the inner TSV sidewall. This was obtained in spite of depositing a layer as thick as 4 μm of pure Al on the proximal section of the vias (*i.e.* the wafer surface). Depositing an even larger amount of Al expecting a thicker and more uniform layer in the inner section of the via is not recommended, as that would increase the stress on the wafer to levels susceptible to cause wafer warpage, besides adding inconvenient burden to the subsequent Al etching step. Therefore, to overcome the issue we looked for a more suitable design of the via geometry.

This paper presents a novel fabrication method that significantly improves the way metallic layers are sputtered inside deep and slender TSVs. We show that, by implementing an hourglass-shaped TSV profile and using the same amount of Al as in our previous work, it is possible to deposit thicker metal stacks in TSVs with improved coverage and conformality and with a more uniform control of the thickness across the entire via sidewall. The proposed fabrication method involves a carefully designed combination of different dry etching schemes to obtain a smoothly elongated and centro-symmetric TSV profile, with diameter shrinking from around 180 μm at both wafer surfaces to around 50 μm in the center of the TSVs. In combination with a low-pressure sputtering deposition of the Al/TiN stack, this results in a sharp superconducting transition above 1 K, which is demonstrated for even deeper Si vias (500 μm) than in our previous reports.

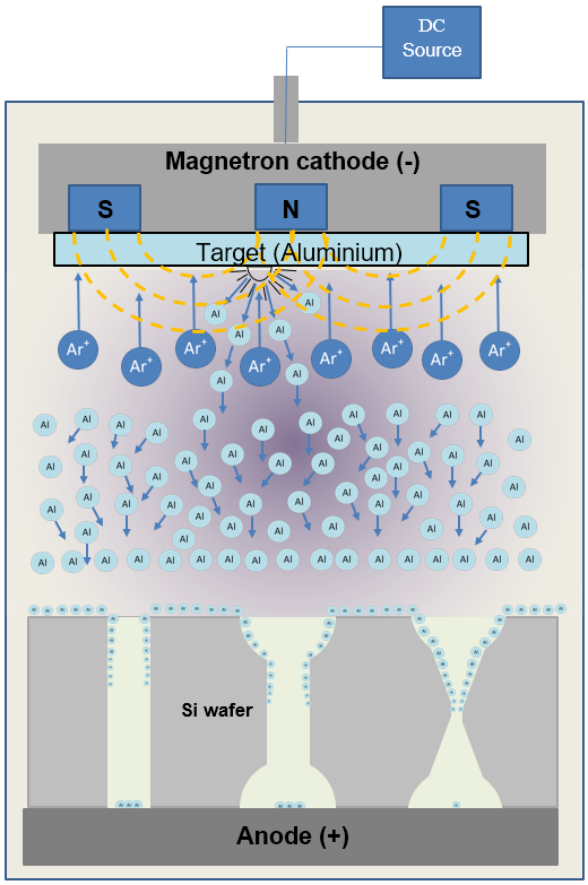

Fig. 3. Sketch of the result of single-side sputtering of aluminium over the three different TSVs designs of Fig. 2 (not to scale for illustration purposes). Note that complete TSV processing involves double-sided Al sputtering.

II. Hourglass Through-Silicon Vias

A. Design

The main aim of our research is to obtain HAR TSVs that optimize via coverage and conformality of the metal stack as well as superconducting performance while maintaining high reproducibility and compatibility with CMOS processing. A simple approach like sputtering TSVs with aluminum can fulfill these criteria only given a proper geometry of the TSVs, as illustrated by the progressive sequence of TSV designs that we implemented (Fig. 2) and we briefly review in the following.

Our TSV design work started with standard straight silicon vias (Fig. 2a). Perfectly cylindrical vias with diameter between 50 μm and 100 μm were fabricated by deep reactive ion etching (DRIE) on both 300 and 500 μm-thick 4-inch Si wafers. The lowest value of room temperature electrical resistivity we could measure upon Al sputtering was in the order of MΩ. This was attributed to the scarce amount of Al that could reach onto the sidewalls of the TSVs beyond the upper via section (*i.e.*, the section closer to the plasma in the sputtering chamber) during single-side via sputtering (see bottom left sketch in Fig. 3). Hence upon double-sided sputtering, the center (*i.e.*, middle section) of the vias was coated with a quantity of Al insufficient for a continuous let alone sufficiently thick layer.

To facilitate the penetration of the plasma within the TSVs during the sputtering process, a funneled TSV profile in the shape of a wine glass was introduced in 300 μm-thick Si wafers (Fig. 2b) [16]. This pseudo-hemispherical funnel was 50 μm deep and had a diameter of 120 μm at the wafer surface side. The central section of the TSV was cylindrical with a diameter of 50 μm and a length of about 200 μm. By means of this technology we could obtain superconductive Al-sputtered TSVs. The single-via average electrical resistance measured at room temperature was 355 mΩ. However, for the same vias we could not observe a single and sharp superconducting transition. Since the critical superconducting transition temperature for an Al film is inversely proportional to the film thickness [21], we attributed the smooth observed superconducting transition to the non-uniform thickness of the sputtered Al layer across the sidewalls of the vias. This determined the presence of via sections with differing metal thicknesses, associated with multiple differing transition temperatures. Specifically, the Al layers were systematically thicker at the junction of the planar and funnel sections than in the cylindrical section of the vias.

To reduce the unevenness of sputtered metal thickness between top and middle sections of the TSVs, we conceived of a novel TSV sidewall profile featuring 1) relatively wider access holes and 2) a smoother and elongated transition towards the center of the via. (see bottom right sketch in Fig. 3). Such profile would at once further facilitate plasma capturing and penetration, as well as allow superior sidewall conformality and thickness uniformity of the sputtered metal compared with wine glass-shaped TSVs (Fig. 3). Additionally, we wanted to prove the feasibility of our technology for thicker wafers than we previously reported. We hence implemented the second generation of funneled TSVs in the shape of hourglass (Fig. 2c).

B. Fabrication

Hourglass TSVs with diameter of access holes and of the central section measuring respectively 180 μm and 50 μm were fabricated on 500 μm-thick Si wafers. The larger access hole size relative to the 300 μm-deep wine glass vias was designed to accommodate for the correspondingly increased depth of the vias.

The fabrication process for the hourglass TSVs consists of the following three parts (Fig. 4): a) wafer-scale micromachining of the TSVs, b) electrical insulation of the TSVs for room temperature measurements, and c) conformal coating of the TSVs with Al as metallization and TiN as capping layer.

The fabrication started with thermal growth of a 300 nm-thick silicon dioxide layer on a 4-inch, double-side polished, 500 μm-thick Si wafer. A protective 5 μm-thick layer of silicon oxide was deposited by plasma-enhanced chemical vapour deposition (PECVD) on both sides of the wafer to be used as hard mask for the patterning of two-level cavities (Fig. 4a-b). These cavities were patterned by means of two sequences of photolithography and oxide etching steps, starting with the bottom wafer side (Fig. 4a). First, a 4 μm-thick layer of photoresist (AZ 3027) was spin-coated, and 100 μm diameter holes were patterned by exposing the resist

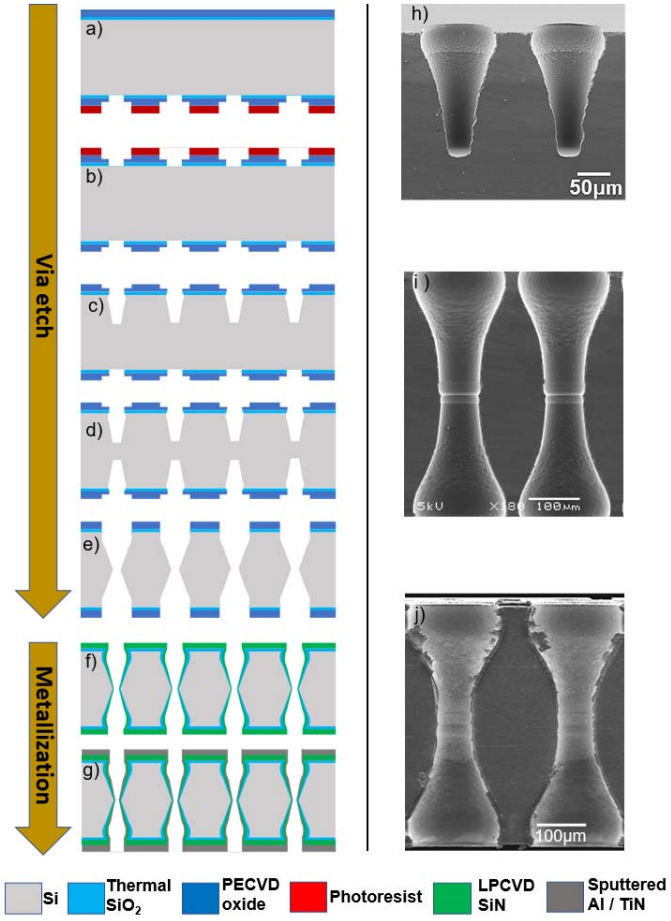

Fig. 4. Sketched cross-sections illustrating the fabrication process flow for hourglass TSVs: a) etching of bottom side two-level cavities; b) etching of top side two-level cavities; c) etching of top side funnels: anisotropic DRIE (Bosch process) followed by hemispherical isotropic etch; d) etching of bottom side funnels: anisotropic DRIE (Bosch process) followed by hemispherical isotropic etch; e) etching of top and bottom side funnels: anisotropic DRIE ("Pseudo KOH"); f) cleaning and thermal growth of insulating SiO_2 layer; g) double-sided sputtering and patterning of Al/TiN; h) SEM cross-sectional view of TSVs after step c) (the silicon oxide mask layer was removed by wet etching before dicing for imaging purposes); i) SEM cross-sectional view of TSVs after step e); j) SEM cross-sectional view of TSVs after step g).

to a dose of 500 mJ/cm^2 and subsequent development. Then the thick silicon oxide layer was etched by RIE for 6 min (see Table I for details) down to a thickness of about 2 μm. After this, a cleaning procedure was performed consisting of an oxygen plasma treatment (400 ml/min of O_2 at 1000 W) to remove the passivation layer, followed by immersion in HNO_3 (99 % concentration) at room temperature to remove organic contamination and then in HNO_3 (69% concentration) at 110 °C to remove any possible metallic particles. The backside of the wafer was then spin-coated with a 4.1 μm-thick layer of photoresist (AZ 3027), and 50 μm diameter holes were exposed with a dose of 650 mJ/cm^2, developed and etched by RIE for 7 minutes until the silicon oxide was totally removed. The same process to fabricate two-level oxide cavities was then performed on the top side of the wafer as shown in Fig. 4b.

The hourglass TSV sidewall profile was obtained using several configurations for DRIE varying in power, gas flow,

TABLE I
MAIN PARAMETERS USED FOR THE RIE ETCHING OF SILICON OXIDE

Etch type	RIE
Time [sec]	360
RF Power [W]	300
Pressure [mTorr]	180
Gas flow [sccm]	C_2F_6 = 36 CHF_3 = 144

etching time and temperature as summarized in Table II. The etching process started by anisotropic Bosch-type etching at 20 °C during 360 cycles (about 200 μm deep) on the front side of the wafer. Immediately afterwards, isotropic DRIE was conducted for 260 s at 20 °C. This particular type of etching used inductively-coupled SF_6 plasma generated near the coils in the upper part of the reactor chamber (Rapier Omega i2l). This step etched hemispherical cavities, which in this case ended up shaping the funnels in combination with the previous etch step (Fig. 4c). Fig. 4h shows a micrograph of the upper half of two neighboring TSVs as obtained after the above described etching steps. As for the two-level cavities, the wafer was then processed from the backside to obtain the funneled sidewalls using the same process steps as for the top side (Fig. 4d).

At this point, deep cleaning of the wafer was necessary to remove any possible residue of the octafluorocyclobutane (C_4F_8) passivation layer introduced during anisotropic DRIE. Firstly, a two-step oxygen plasma stripping was performed. The first step operated with a mixture of CF_4 (200 ml/min) and O_2 (35 ml/min) at 400 W for 3 minutes. The second step used pure O_2 (500 ml/min) at 1000 W for 10 minutes. A cleaning procedure with HNO_3 was performed next. Lastly, the wafer was immersed in a water solution of non-ionic surfactant (Triton) for 3 minutes and in buffered hydrofluoric acid (BHF, 7:1) for approximately 1 minute. The latter in addition worked as wet etch step to remove the bottom silicon oxide layer of the two-level cavities. This left only the outer, 100 μm-wide circular openings in the remaining oxide hard mask.

The final part of TSV shaping was performed by a so-called (dry) "pseudo-KOH" etching step, which mimics the effects produced by (wet) potassium hydroxide (KOH) etching by means of DRIE. The anisotropic plasma in this case was produced from a mixture of SF_6 and C_4F_8 gases. The plasma was generated in closer proximity of the substrate to obtain a larger impact on the edges of the partially etched funnels. As a result, these steps broadened the access holes, smoothed the TSV sidewalls and merged the upper half of the hourglass with the bottom part, completing the through-silicon etching. Pseudo-KOH etching was performed during 520 s on both sides of the wafer (Fig. 4e). However, because of the absence of a landing layer between the wafer and the chuck, during the backside etching a transport wafer had to be inserted instead, differently from the topside etching. This was necessary to prevent the backside helium pressure in the etching machine from dramatically increasing and consequently triggering arrest of the process. The use of a transport wafer added extra height to the process wafer, which slightly changed the etching performance. This is the reason for the

TABLE II
MAIN PARAMETERS FOR THE DRIE ETCHING STEPS IN HOURGLASS TSV FABRICATION

Etch type	Step 1: Bosch (anisotropic)	Step 2: isotropic	Step 3: anisotropic
Time [sec]	360 cycles: D1: 2 sec E1: 1.5 sec (Platen power: 80W) E2: 5.5 sec (Platen power: 30W)	260	520
Power [W]	Primary coil: 2200	Primary coil: 2500	Primary coil: 500 Secondary coil: 2000
Platen temperature [C]	20	20	50
Gas flow [sccm]	D1: C_4F_8 = 280 E1: SF_6 = 350 E2: SF_6 = 350	SF_6 = 500	SF_6 = 350 C_4F_8 = 210 O_2 = 210
Pressure [mTorr]	D1: 45 E1: 25 E2: 25	100	70

slight asymmetry and small mismatch between the etching on the front side and the etching on the back side of the wafer (Fig. 4i). The minor yet visible discontinuity in the sidewall of the middle TSV section was remedied by using smoothening steps in the finalization of the TSVs, as explained below. The wafer was then cleaned by oxygen plasma, a similar cleaning procedure with HNO_3 as described above, and by immersion in HF (40% w/w) for 17 minutes to remove the chemically-grown silicon oxide and any possible contamination that was not removed during the hot bath of HNO_3. Repeated sequential steps (three steps) of oxidation and oxide removal (two steps) were performed to smoothen the sidewalls. In each of these steps, a 2 μm-thick layer of thermal silicon oxide was grown on all Si surfaces and then removed by HF (40% w/w). Finally, a thermal SiO_2 layer and a 1 μm-thick layer of silicon nitride were respectively thermally grown and deposited by low-pressure chemical vapour deposition (LPCVD) on both sides of the wafer (Fig. 4f). These highly conformal dielectric layers served to electrically insulate the vias during their electrical characterization at room temperature and to ensure coverage of any remaining topography left after full TSV micromaching.

The metallization of the vias was performed by sequential sputter deposition of Al and TiN on both sides of the wafer (Fig. 4g and Fig. 4j) using a cryo-pumped Trikon Sigma 204 sputter-coater with a base pressure of 10^{-6} Pa. A 4.5 μm-thick layer of pure aluminum, as measured on the flat wafer surface, was first sputtered over the TSVs as superconducting layer. The deposition took 34 minutes and was performed with a substrate temperature of 25 °C, 20 sccm of argon gas flow and a DC power of 1.3 kW on the 16" Al target. The chamber pressure was set to 244 mPa, obtaining a deposition rate of approximately 2.25 nm/s. Subsequently, a 20 nm-thick layer of titanium nitride was sputtered over the aluminum, acting as a capping layer. TiN was deposited at 350 °C for 58.3 s. During the TiN deposition, the pressure was tuned to 569 mPa by using 20 sccm of argon and 70 sccm of nitrogen, and the power was set to 6 kW. Micrographs of the resulting vias after the metallization are shown in Fig. 5a-d.

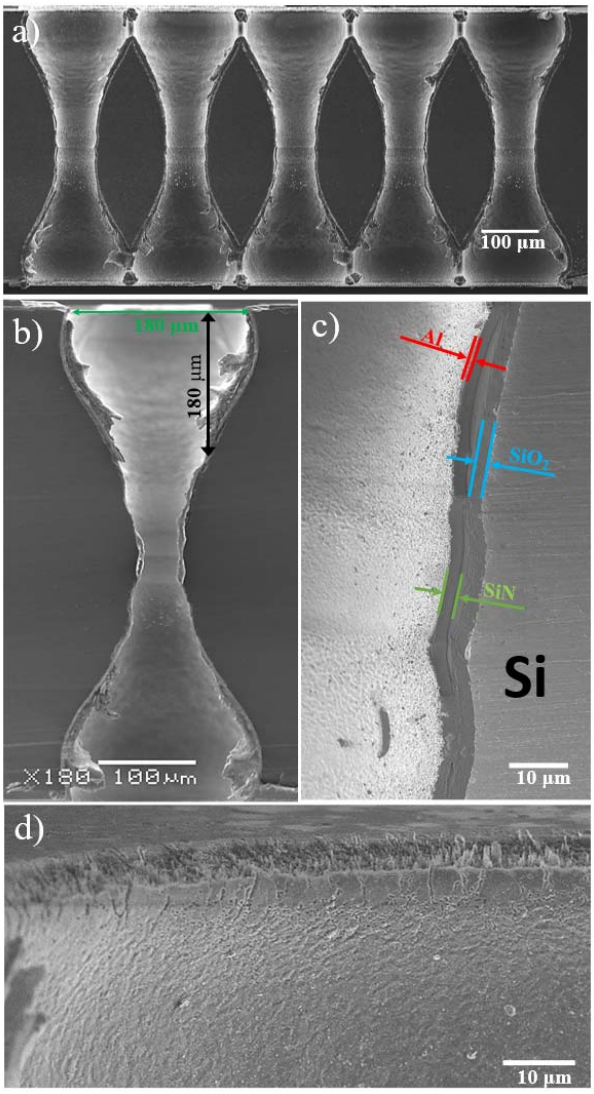

Fig. 5. SEM micrograph of the cross-section of 500 μm-deep TSVs after Al/TiN sputtering. (a) Array of TSVs. (b) Single via (hanging Al flakes due to saw dicing). (c) Central section of the via showing the layers stack (the TiN capping layer is not visible) (d) Edges of the vias at the intersection with the wafer surface.

The Al and TiN layers were finally patterned on both wafer sides by optical lithography and plasma etching (Fig. 6a-b). AZ 12xt-20PL photoresist was spin-coated to a thickness of 12 μm using an edge holder, soft baked at 110 °C for 240 s, exposed with 300 mJ/cm^2, post-exposure baked at 90 °C for 60 s and developed with AZ 300MIF developer per 60 s using a double puddle development process. The metallic layers were etched by inductively-coupled plasma at 25 °C using HBr (30 sccm) and Cl (20 sccm) as reaction gases and 500 W of RF power.

III. ELECTRICAL CHARACTERIZATION

Electrical measurements were performed at both room and cryogenic temperature to characterize the finalized Al/TiN-coated hourglass vias. TSV resistance was measured using a four-point probe method by means of a 3D cross-bridge

Kelvin resistor structure (Fig. 6c-d) [22]. A current was applied across one pair of diagonally opposite terminals (indicated by I and GND in Fig. 6d) and the resulting voltage drop across the central single via was measured across the other pair of terminals (V_1 and V_2). The value of the single-via resistance can be approximated using the following formula:

$$R = \frac{\pi}{\ln(2)} \frac{\Delta V}{I}$$

where $\frac{\pi}{\ln(2)}$ is used as geometric correction factor since the TSVs are coated with thin metallic layers and the probes are equidistant [22].

I-V measurements at room temperature were performed by means of a precision semiconductor parameter analyzer (Keysight 4156C) and a multi-probe station (Cascade Microtech). Cryogenic DC resistance through the vias was measured as a function of temperature with a standard 4-point probe method using a commercial adiabatic demagnetization refrigerator (ADR, Entropy GmbH). The sample was mounted on a copper block weakly coupled to the Gadolinium Gallium Garnet stage of the ADR. A thermometer and a resistive heater allowed to control the stage temperature down to 600 mK, well below the Al superconducting transition. During the measurements the current was kept constant at 30 μA, and the temperature was repeatedly changed in cycles of upward and downward sweeps between 1.1 K and 1.6 K. 5 measurement cycles and a final upward sweep were performed, for a total of 11 sweeps. The measurements were repeated over a period of 5 days to check for stability, and did not show signs of deterioration over time.

IV. Results

The fabrication process described above allowed the fabrication of high-density arrays of hourglass TSVs over a full 4-inch, 500 μm-thick Si wafer (Fig. 6a-b). The cross-sections shown in Fig. 5 evidence successful, fully conformal and void-free coating of the TSVs with sputtered Al/TiN. Although the transition in the edges of the vias at the intersection with the wafer surface is abrupt, the edges are sufficiently smooth to be properly and uniformly coated with Al. Minor damages to the coating of the edge were introduced during Al patterning. In particular, a metallic layer as thick as 430 nm could be deposited in the center of the TSV (Fig. 7). A metal thickness of 665 nm at 50 μm depth and of 1 μm at 170 μm depth was measured. (Fig. 8)

The wafer-scale yield for the fabrication of electrically conductive TSVs was close to 90 percent (Fig. 9). The single-via electrical resistance measured at room temperature was in the range of hundreds of mΩ for most of the TSVs (Fig. 10), with the lowest measured value of 160 mΩ. The measurements also evidenced the ohmic behavior of the TSVs, as show for a typical instance in Fig. 11.

A single, sharp and hysteresis-free Al superconducting transition was measured at 1.27 K (Fig. 12). We consider this result as conclusive proof of the quality and uniformity of the Al layer sputtered inside the hourglass TSVs. Since the ADR at our disposal could not measure I-V curves, we reserve to quantify the TSV's critical current in future work.

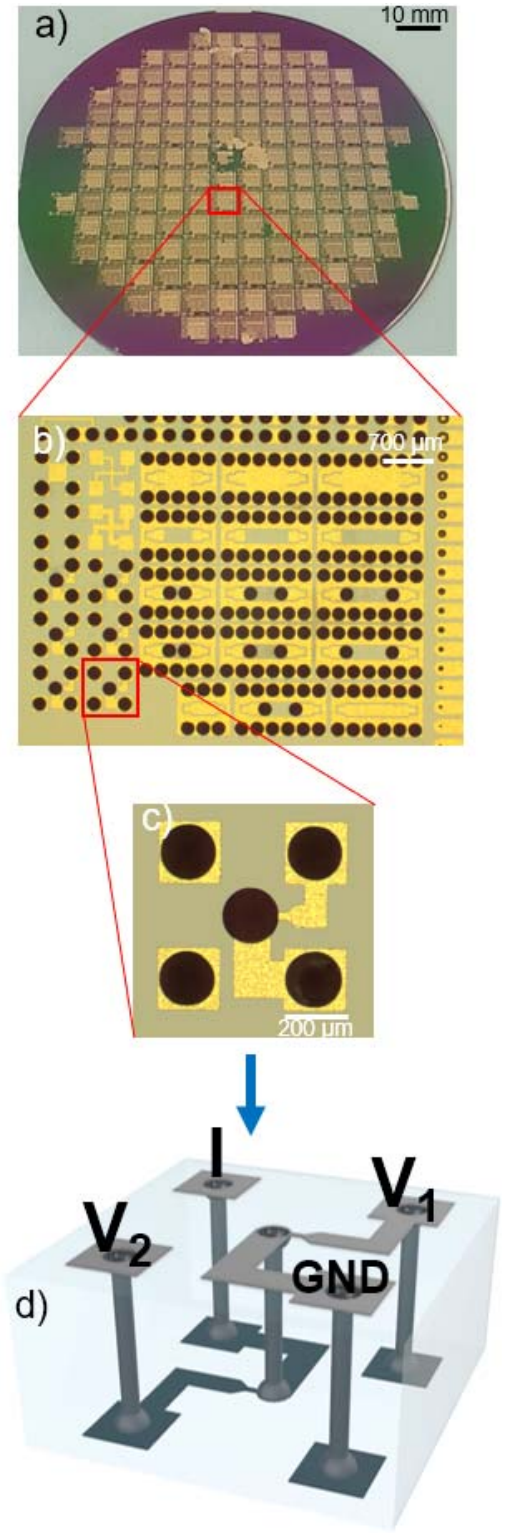

Fig. 6. a) Uniform Al/TiN patterning and interconnect definition over the full 4-inch Si wafer surface. b) Close-up of a die singled out from the wafer by saw dicing. c) Top view of a single cross-bridge Kelvin resistor structure used during the electrical characterization of the TSVs. d) Sketch of the 3D geometry of a single cross-bridge Kelvin resistor structure.

V. Discussion

In this work, we demonstrated a sharp superconducting transition in 500 μm-deep, electrically-insulated TSVs coated by sputtering a thick, conformal and TiN-capped layer of

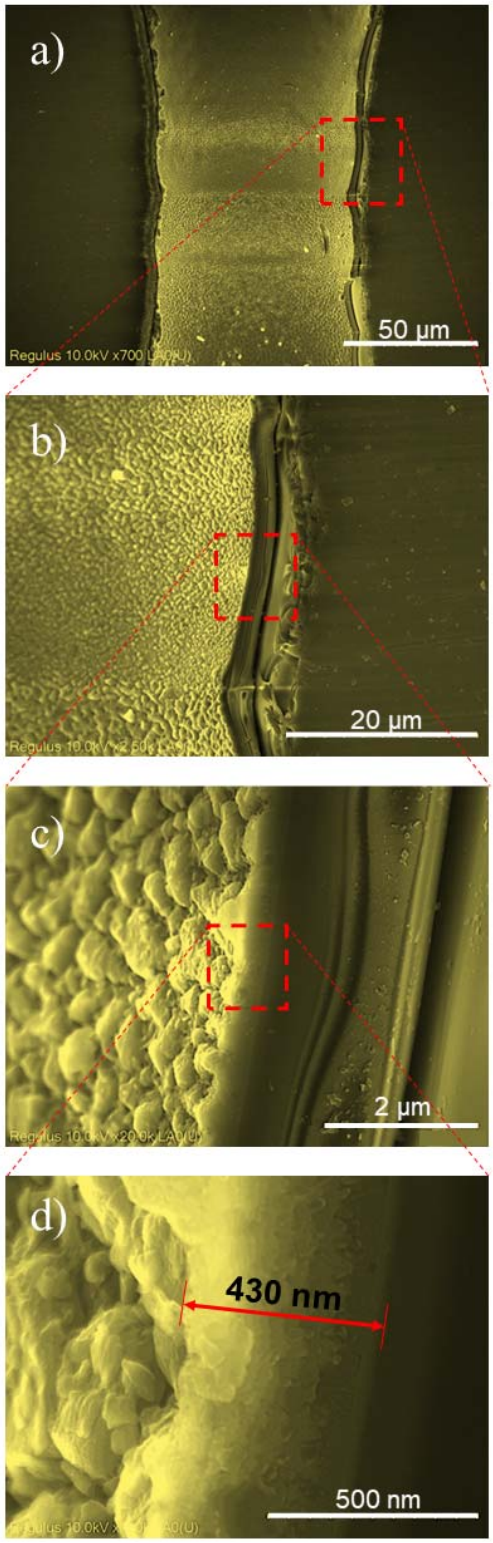

Fig. 7. SEM micrographs of the cross-section of the middle section of an hourglass TSV after metal sputtering and imaged at increasing magnifications. (a) 50 μm scale. (b) 20 μm scale. (c) 2 μm scale. (d) 500 nm scale, evidencing the measured thickness and the poly-crystalline microstructure of the Al layer (no TiN capping layer observed).

aluminum. Key to the conformal metal coverage of the sidewalls is the hourglass-shaped profile of the vias. The tailored profile has cylindrical symmetry with respect to the central

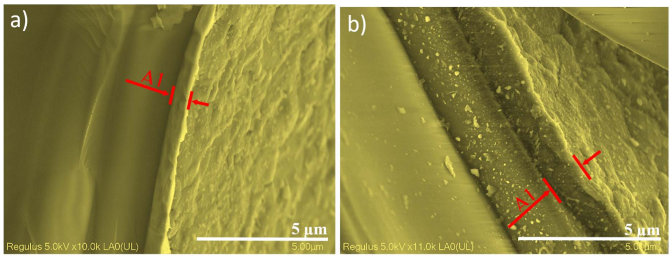

Fig. 8. SEM TSV cross section showing the metal thickness at a depth of a) 50 μm and b) 170 μm.

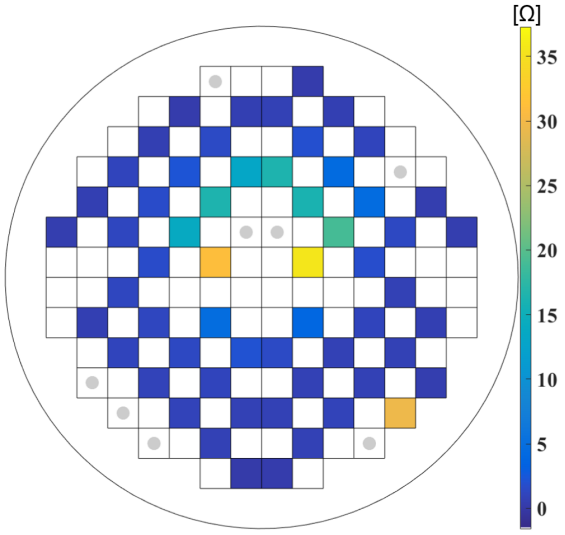

Fig. 9. Wafer map showing the fabrication yield and color-coded single-via sheet resistance for 4-inch wafer-level TSVs. Grey dots indicate the locations of electrically non-conductive TSVs.

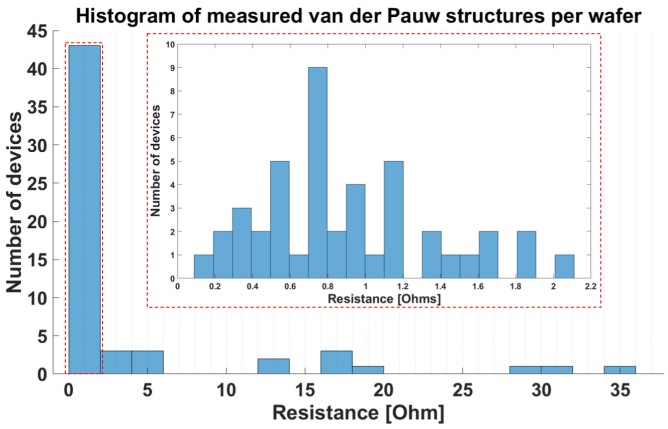

Fig. 10. Distribution of room temperature electrical resistance values measured for single hourglass TSVs using the 3D Van der Pauw structures. Includes a sub-plot of the distribution between 0 and 2 Ohm.

vertical axis, and nearly perfect vertical symmetry with respect to the center of that axis. Concerning the latter, we remark incidentally that the slight step in the TSV sidewall profile visible at the central junction of the opposite funnels (Fig. 2c), as well as the DRIE-induced sidewall scalloping (Fig. 7a-b), do not have any appreciable influence on the functionality of the TSVs, as confirmed by their measured electrical (super)conductivity.

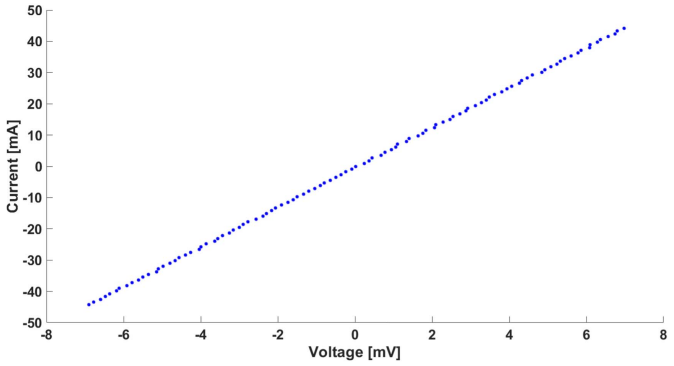

Fig. 11. Ohmic behavior of a single Al-coated hourglass TSV evidenced by I-V characterization at room temperature. The measured electrical resistance is 160 mΩ.

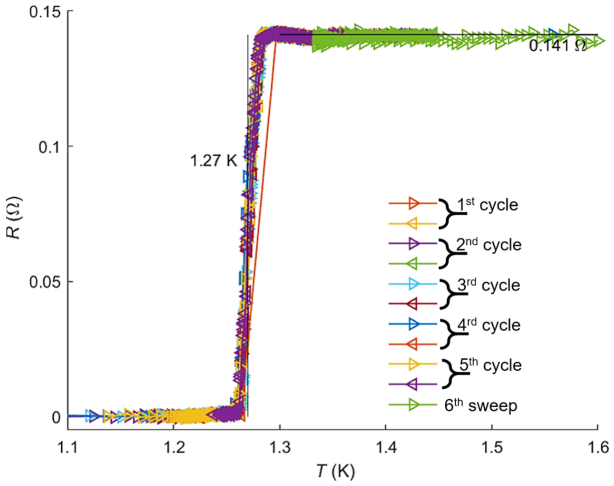

Fig. 12. Superconductive transition measured for a single cross-bridge Kelvin structure with 500 μm-deep Al/TiN-coated TSVs. The overlapping curves represent consecutive upward (→) and downward (←) temperature sweeps, and confirm the high repeatability of the measurements.

The hourglass TSV profile features relatively wide access holes (180 μm in this paper) to enhance plasma funneling into the core of the via, as well as a smooth tapering which exposes the entire length of top and bottom halves of the sidewall to the molecular flux incoming from the closest access hole. The progressive shrinking of the diameter of the via (down to 50 μm in its middle section) promotes lateral physical deposition of molecular species from the plasma to the sidewalls even in the center of the via, as it compensates for the decreased lateral mobility of the reactive molecules in that most remote via section. By virtue of these features and in combination with a suitable configuration of the Al sputtering process, the proposed via geometry overcomes the issues related to inconsistent, insufficiently thick or non-uniform metal coating that persisted in prior examples of superconducting TSVs.

Our versatile TSV technology allows to achieve a minimum inner diameter of 20 μm and a maximum diameter for the outer openings on top and bottom wafer surfaces of 250 μm for a wafer thickness of 500 μm. Thicker and thinner wafers are also compatible with our TSV fabrication process. Moreover, it is readily possible to sputter and pattern additional superconducting materials in hourglass vias, such as *e.g.* niobium, titanium and their alloys [23]. More generally, it is in principle possible to introduce any sputter material inside the proposed TSVs, including *e.g.* copper or gold, the limitations residing rather in the patterning of the metal layers.

The wafer-level fabrication yield is around 90 percent. The reason for the 10% failure rate is attributed to heat dissipation problems during the etching of the metallic layers. During the latter, the wafer with TSVs needs to be processed on top of a transport (Si) wafer, and it is thereby glued with a few drops of heat transfer fluid (PFPE, Galden). The heat transfer fluid improves the heat transfer from the wafers to the chuck; however glue dispensing is hardly perfect. During the etching of the metallic layer intense heat is produced, and in regions of the wafers where cooling from the chuck happens to be limited the photoresist may get burned and the metallic region severely attacked. This issue may be solved by performing metal etching in system with the capability of placing the wafer directly over the chuck. The fabrication process has good uniformity across the wafer and reproducibility from wafer to wafer. Only small variations (a few microns) in the etched vias for different wafers were observed. We have reproduced our process for the fabrication of superconducting Al-sputtered hourglass TSVs in 4 Si wafers. The fabrication yield per wafer of the TSVs turned out in all cases to be fairly similar to the typical case that we described in the text. As shown in Fig. 1, only small differences are noticed such as the shape and width of the funnel and the width at the central part of the TSVs.

The TSV technology here successfully demonstrated shows promise for application as vertical interconnection technology for physical qubit layers and superconducting MEMS devices. The sharp superconductive transition proves the high purity of the sputtered materials and the quality of the poly-crystalline layer formed during the deposition over the TSVs sidewalls. Without expectedly loosing signal quality or decreasing electrical performance, the TSVs can be densely packed, particularly when implemented in thin Si substrates. In this respect, we remark that the smallest pitch in closely-packed arrays of hourglass TSVs is bounded by the diameter of their access holes at the wafer surface; and that the latter is roughly proportional to the wafer thickness, as deeper TSVs require wider funnels to be properly coated by sputtering. As a result, the outer via diameter of hourglass TSVs can be downscaled to *e.g.* less than 100 μm for 300 μ-thick wafers. Dense arrays of superconducting TSVs are especially relevant in 3D integration to reduce signal latency, dissipate power more efficiently, and address dense arrays of coherent qubits.

We also believe that some minor modifications in TSV design and implementation, such as a relaxation of the geometrical transition from the wafer surface to the funnel and sputtering of other types of materials, could suffice to enable applications in support of *e.g.* photodetectors and other superconducting astronomical instruments exploiting the THz range of the electromagnetic spectrum [24], [25].

VI. Conclusion

Increasing demand of large-scale and high-density silicon-based quantum computing systems is pushing the development of 3D interconnect technologies to adapt to new and challenging requirements. We presented a microfabrication process for 500 μm-deep Al-based superconducting TSVs that is fully compatible with conventional CMOS fabrication processes and achieves single-via electrical resistance at room temperature as low as 160 mΩ. The high conformality and superior uniformity of the Al coating of the vias obtained by means of the tailored hourglass sidewall profile in combination with low-pressure DC-sputtering of Al was confirmed by a remarkably sharp superconducting transition measured at 1.27 K.

Future work will explore the full extent of the reach of the proposed 3D superconducting interconnect technology for multiple applications in silicon-based quantum computing, MEMS and THz sensing.

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