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Continuous rounds of quantum error correction (QEC) are essential to achieve fault-tolerant quantum computers (QCs). In each QEC cycle, thousands of ancilla quantum bits (qubits) must be read out faster than the qubits' decoherence time ($<<T_2^*$~120μs for spin qubits). To address this urgent need, several CMOS receivers operating at cryogenic temperatures (cryo-CMOS RXs) have recently been introduced for gate-based [1] and RF reflectometry [2] readout of spin qubits, as well as transmons' dispersive readout [3]. However, they have a few shortcomings. First, due to the temperature-independent shot noise of transistors in nanometer CMOS technology [4], their measured noise temperature (T_N) is limited to 40K, thus degrading qubit readout fidelity. Second, due to their large T_N, prior art showed either only the electrical performance of their chips by applying a relatively large (i.e., -85dBm [2]) modulated signal directly to the RX input [2,3] or offered limited qubit measurements by exploiting a HEMT amplifier prior to the RX [1]. Those issues hinder future monolithic integration between solid-state qubits and readout electronics. This work advances the prior art by (1) introducing a wideband passive amplification circuit at the RX front-end to minimize the shot noise contribution of the active devices, lowering prior art T_N by ~2.7x; (2) demonstrating the RX performance in an RF-reflectometry qubit readout scheme without using off-the-shelf LNA prior to the RX.

Figure 29.3.1 shows the principle of RF reflectometry readout in a double quantum dot (DQD) system. It uses a single electron transistor (SET) as a charge sensor, which is capacitively coupled to the right quantum dot (QD) via C_g. By sweeping the V_{RP} and V_{LP} plunger gates, individual electrons can be loaded in and out of the left and right QD, changing their occupation (N_L, N_R) in the charge stability diagram. The SET channel conductance is a function of its gate voltage ($V_{g,SET}$), N_L and N_R. At a fixed $V_{g,SET}$, the SET channel conductance curve shifts by ~e/C_g when an electron is added to the right QD. In the RF reflectometry system, the left QD is used as a data qubit, and the right QD is initialized to state $|0\rangle$ (spin down). During the readout, the data qubit state collapses to either $|0\rangle$ or $|1\rangle$. In case of spin up, the electron can tunnel to the right QD, modulating the SET conductance. Since the SET drain is coupled to an inductor to resonate with its parasitic capacitance, the SET state-dependent channel conductance can be measured by applying an RF tone at the tank resonance and monitoring the amplitude and phase of the reflected signal. The readout SNR (see the equation in Fig. 29.3.1) depends on its input equivalent noise power spectral density (N_{eq}), integration time (T_{int}), the power of the probe tone (P_{in}), and the separation between reflection coefficients (S_{11}) of the qubit states, reflecting the SET charge sensitivity. At first glance, to achieve the desired SNR, N_{eq} specification can be greatly relaxed by increasing P_{in}. However, a large voltage swing of the probe tone can force the DQD to operate across different charge regimes, disturbing readout operation. Hence, P_{in}<-100dBm is typically used, thus demanding extremely low T_N or large T_{int} to satisfy SNR>10dB to reach a minimum readout fidelity of 99.9% for QEC.

In deep sub-μm CMOS, the channel noise is not solely thermal but also includes shot-like noise due to the quasi-ballistic transport of the carriers (see $\overline{V_n^2}$ equation in Fig. 29.3.2). For a 40nm channel-length transistor, ~25% of the total noise is contributed by shot noise at room temperature (RT) [4]. By operating at 4K, the thermal portion of $\overline{V_n^2}$ becomes 75x smaller, but its shot noise portion reduces negligibly, since $(g_m/I_d)^2 \times I_d$ slightly increases in saturation. Hence, T_N merely reduces by ~4-5× in prior art cryo-CMOS RXs from RT to 4K [1-3]. To further reduce shot noise, one needs to significantly increase the transistor current (I_d), but this would greatly increase the power consumption and even degrades the thermal noise portion due to self-heating. Therefore, we propose to add a passive amplification network at the RX input and place active devices in the baseband (BB), where long-channel devices with low shot noise can be used. This greatly reduces the receiver's T_N, as the passive network only exhibits thermal noise, and its passive gain suppresses the active device shot noise.

Fig. 29.3.2-bottom shows the conceptual block diagram of the proposed RX. The input port of an off-chip quadrature-hybrid coupler (QHC) is connected to the qubit readout signal, while its isolation port is terminated by a 50Ω resistor (R_M) to provide wideband input matching. Two identical passive amplification and quadrature downconversion chains are connected to the QHC coupled (CPL) and through (THR) ports. Assuming the input impedance of the amplification/downconversion chain is much higher than 50Ω, the desired signal (V_s) is directed to the CPL and THR ports by √2x amplification but with 90° phase difference [5]. Combined with 4× voltage amplification realized by 1:2 step-up transformers and summing in-phase signals at the mixers' outputs, a total single-ended gain of ~15dB is obtained at the input to the BB amplifiers, thus significantly reducing their (shot) noise contribution to the RX noise temperature. With respect to the signal, the R_M noise appears with 90° phase shift at CPL/THR ports and eventually gets cancelled at the BB outputs due to the specific selection of LO phases used in the quadrature mixers.

Figure 29.3.3 shows the proposed RX schematic. Instead of using transformers that significantly increase chip area and limit the RX operating frequency range, the capacitive stacking technique in N-path filters is adopted to realize the required passive amplification [6]. In general, in an N-path filter, the in-band downconverted voltages across the mixing capacitors using out-of-phase non-overlapping clocks are additive inverse. Therefore, by properly stacking those capacitors, a BB voltage gain of 2 is realized at the bottom plate of the corresponding capacitor. In the first stage of our RX, the bottom-plate voltages of the mixing capacitors (C_1) are sequentially connected to an output node ($V_{o,RF}$), thus realizing a staircase approximation of the RF input signal with a gain of 2. The 2nd stage samples the resulting RF signal with the same method and realizes another 2× voltage gain in the BB capacitors (C_2). Finally, the corresponding BB signals of CPL and THR paths are combined to achieve R_M noise cancellation. Note that the voltage amplification occurs around the LO frequency, which can be tuned to achieve a wide operating frequency range.

For BB amplification, 31× programmable parallel self-biased inverters with long-channel transistors are used to minimize their shot noise. Since the transistor 1/f noise does not scale with temperature, the inverter's area should be large enough such that its 1/f noise at 4K does not limit the receiver's T_N at IF>5MHz. However, this increases the parasitic input capacitance of the BB amplifiers (C_{BB}), which transfers to the RX input by a factor of $(0.5\pi^2)\times(4\sqrt{2})^2$ due to the transparency and amplification of the passive network, thus limiting the RX channel bandwidth (BW). This results in a tradeoff between the RX noise and channel BW. Moreover, to have a negligible charge loading effect, $C_1>C_2>C_{BB}$, leading to another tradeoff between noise and area.

Fabricated in 40nm CMOS (Fig. 29.3.7), the RX chip with a core area of 0.26mm^2 consumes 10.8/12mW at 4K/RT at 1.1GHz. Fig. 29.3.4 shows the RX measured electrical performance. By tuning the LO frequency, the RX voltage gain remains larger than 40dB/35dB across the operating frequency of 0.1-2.5GHz at 4K/RT. Mainly determined by the off-chip QHC, the S_{11} remains <-10dB over the desired BW. Due to the limited driving capability of the output buffer, the BB channel BW is 9MHz at RT and increases to 23MHz at CT due to the increased transistor mobility. The RX noise is measured with the attenuated Y-Factor method in a helium dewar. The RX noise temperature does not improve when the number of active inverter cells is >15. At 4K, the RX noise temperature reaches 15±2.78K at IF=7-23MHz, showing a 15× reduction compared to RT, thanks to the passive amplification.

Figure 29.3.5 shows the DQD readout measurements in which the RX and DQD are placed at the 4K plate and on the mixing chamber of a dilution refrigerator, respectively, and the SET is coupled to a superconducting NbTiN inductor (Fig. 29.3.7). First, we measure the SET response by applying a -100dBm tone at the tank resonant frequency of 119MHz while sweeping $V_{g,SET}$. Regular Coulomb oscillations are observed (Fig. 29.3.5 top-left). Then, we fix $V_{g,SET}$ at a maximum oscillation slope (red dashed line), and monitor the reflected signal at the RX output while sweeping the V_{RP} and V_{LP} plunger gates. The resulting stability diagram shows clear distinctions when the number of electrons in the right QD changes (Fig. 29.3.5 top-right). To emulate qubit readout, 10000 readout shots at regions (1,3) and (1,4) of the stability diagram are executed. The resulting IQ constellation diagram from the RX downconverted signals reveals two distinct responses, showing an SNR of 9.8dB for an integration time of 10μs ($<<T_2^*$~120μs) for each single-shot readout, corresponding to a bit error rate of $<10^{-3}$ (Fig. 29.3.5 bottom).

Compared to prior art RXs (Fig. 23.3.6), this work achieves 2.7× lower noise while consuming the lowest power. As the RX front-end uses only switches and capacitors, its noise and BW are expected to further improve by technology scaling. Moreover, this work, for the first time, demonstrated 99.9% charge-state readout fidelity with a cryo-CMOS RX, thus paving a step towards integrating readout electronics in future scalable QC.

Acknowledgement:
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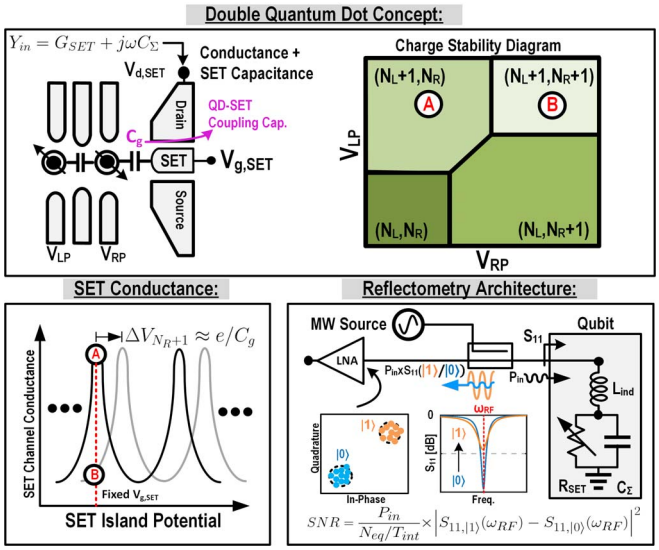

Figure 29.3.1: (Top-left) DQD structure with a SET; (Top-right) DQD's stability diagram; (Bottom-left) SET's conductance versus SET's potential; (Bottom-right) Block diagram of RF-reflectometry readout for semiconductor spin qubit.

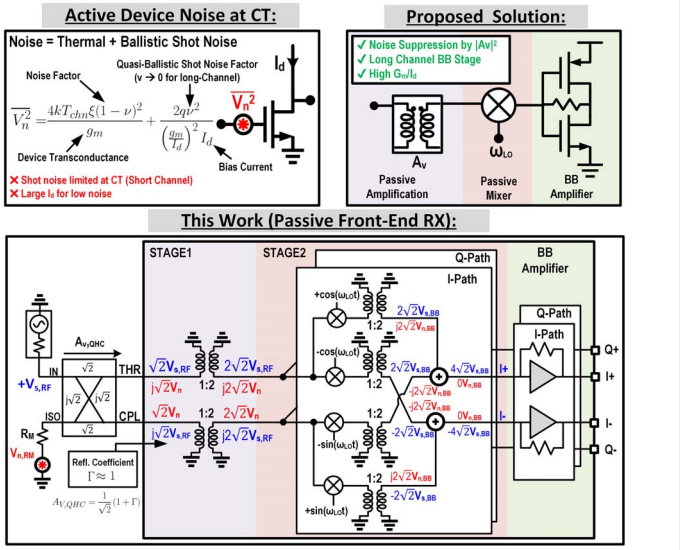

Figure 29.3.2: (Top-left) Input equivalent voltage noise of active devices, containing thermal and shot noise; (Top-right) Proposed solution to suppress shot noise at CT; (Bottom) Conceptual block diagram of proposed RX.

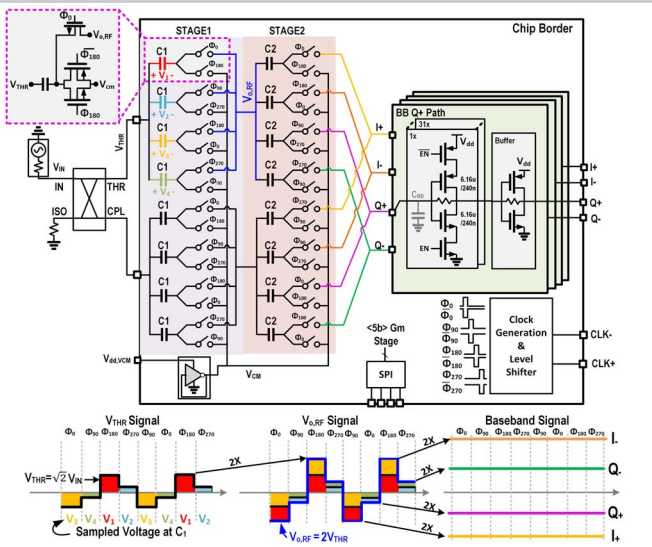

Figure 29.3.3: (Top) Proposed RX schematic, incorporating two stages of passive amplification/downconversion, and inverter-based baseband amplifiers; (Bottom) Conceptual waveforms of the intermediate nodes of the proposed RX.

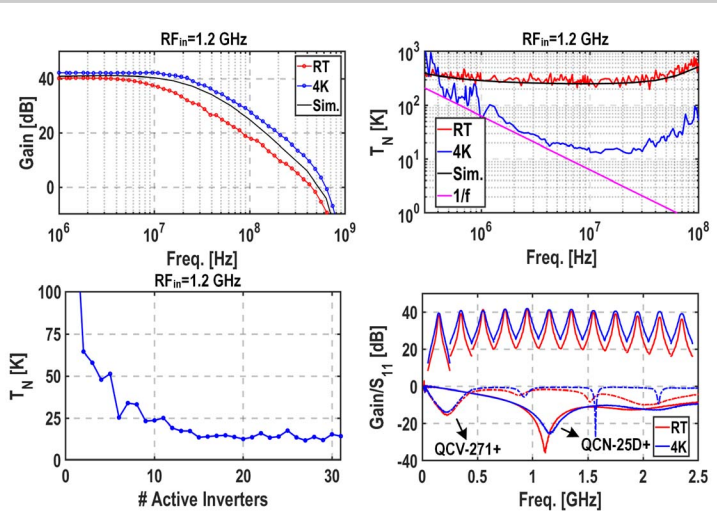

Figure 29.3.4: Electrical characterization of proposed RX at RT and 4K. (Top-Left) RX gain referred at BB frequencies; (Top-Right) T_N across BB frequencies; (Bottom-left) T_N versus number of active inverter cells; (Bottom-right) Gain and S_{11} of RX across 0.1-2.5 GHz measured with different QHC.

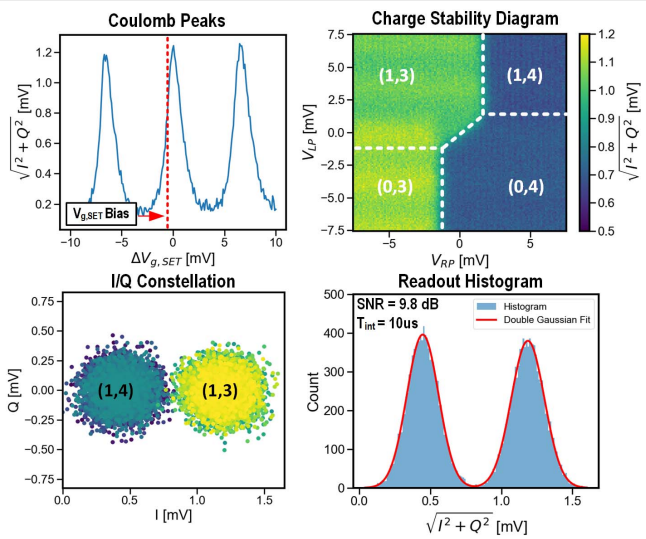

Figure 29.3.5: (Top-left) Coulomb oscillations; (Top-right) Stability diagram. (Bottom-left) I/Q diagram when measured at (1,3) and (1,4) regions; (Bottom-right) Histogram of 20k readout shots with T_{int}=10µs, achieving 9.8dB SNR.

	This Work	Prabowo ISSCC'21 [1]	Park ISSCC'21 [2]	Ruffino ISSCC'21 [7]	Kang ISSCC'22 [3]	Das IMS'22 [8]	Lin RFIC'22 [9]
Reported Architecture	RX	RX	RX	RX	RX	LNA	LNA
Front-End Topology	Passive Amplification	Inductive Degenerated LNA	Common-Gate LNA	Inductive Degenerated LNA	Inductive Degenerated LNA	Inductive Degenerated LNA	XMFR Feedback LNA
Operating Temp.	4.2 K	4.2 K	3 K	3.5 K	3.5 K	16 K	16 K
Operating Freq. [GHz]	0.1 – 2.2	6 - 8	0.2 - 0.6	5 - 6.5	4 - 7.25	3.6 – 5.3	4.2 – 9.2
RF Channel BW	46 MHz	2 GHz	200 MHz	1.4 GHz	2.25 GHz	1.7 GHz	5 GHz
Gain	42 dB	58 dB	90 dB	70 dB	47 dB	38 dB	35 dB
Noise Temp.† (NF)	15 K (0.21 dB)	44 K (0.6 dB)	44 K (0.6 dB)	40.5 K (0.55 dB)	86.5 K (1.1 dB)	10.6K^ (0.15 dB)	4.5 K (0.065 dB)
IB IIP3	-35.5 dBm	-50.8 dBm	-69 dBm	-72 dBm	-35 dBm	-	-
S_{11}	< -10 dB*	-	-	<-10dB	< -10 dB	<-10 dB	-8.9 dB
Power Dissipation	5.5mW + 4.8mW/GHz	66 mW	38 mW	108 mW	20 mW	23.1 mW^	21mW
Technology	40nm Bulk CMOS	40nm Bulk CMOS	22nm FinFet	40nm Bulk CMOS	40nm Bulk CMOS	65nm Bulk CMOS	22nm FDSOI

*Limited by the quadrature hybrid, † Referred at 300K, ^For best NF performance

	This Work	Prabowo ISSCC'21 [1]	Park ISSCC'21 [2]	Ruffino ISSCC'21 [7]	Kang ISSCC'22 [3]
Qubit Platform (Readout Technique)	Spin Qubit (Reflectometry)	Spin Qubit (Gate-Based)	Spin Qubit (Reflectometry)	Spin Qubit (Reflectometry)	Transmon (Dispersive)
Fridge Integration	Yes	Yes	Yes	No	Yes
Readout Characterization	Yes (CSD**, Single Shot Readout)	Yes (CSD**, SNR Characterization)	No	No	No
External Components	On PCB QHC + Isolator	HEMT LNA + Circulator	HEMT LNA + Circulator*	N.A	TWPA + Isolator*
T_{min} (SNR=1)	1.05 µs	1.96 µs	N.R	N.R	N.R

* Reported in the JSSC publication ** Charge Stability Diagram

Figure 29.3.6: Comparing (Top) electrical and (Bottom) qubit readout performance of the proposed RX with prior arts.

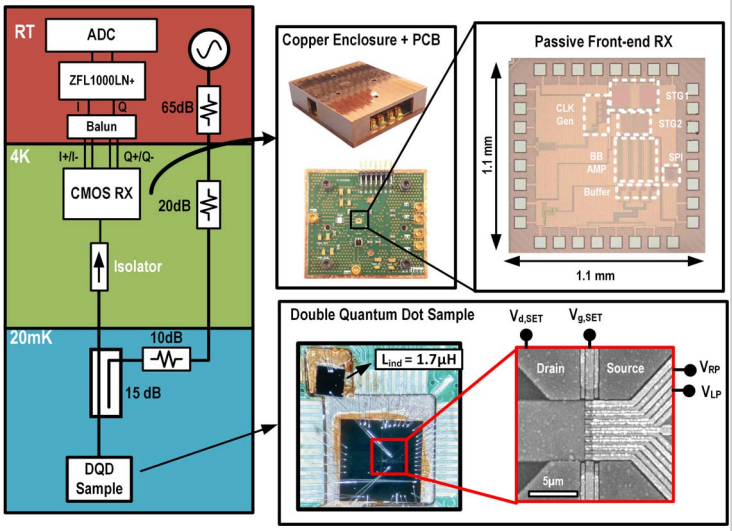

Figure 29.3.7: (Left) Block diagram of the measurement setup for qubit readout; (Right) Chip micrograph of the qubit sample and the proposed RX.

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