iTCM-Operated Three-Phase Three-Wire Voltage-Source Converter System Featuring Capacitor-Split Virtual Ground Connection

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iTCM-Operated Three-Phase Three-Wire Voltage-Source Converter System Featuring Capacitor-Split Virtual Ground Connection

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***Abstract*—High efficiency can be achieved in grid-connected converters by implementing a zero-voltage switching mechanism, such as the integrated triangular current mode (iTCM) modulation, which reduces the switching losses in the semiconductors. The iTCM can be readily adapted to a three-phase three-wire voltage-source converter (VSC) with the help of virtual ground (VG), which decouples the operation of three-phase switching cells. However, conventional methods of VG have all the zero-sequence currents flowing through the dc-link capacitors, resulting in an increase in the rms current, hence, extra loss for those passive components. This article, thus, introduces a capacitor-split VG topology that can relieve this issue by excluding the dc-link capacitors from the circulating path of the main zero-sequence currents, helping to reduce current stress for the dc-link capacitors. This topology is characterized by its filter capacitors being split into two halves and connected to the top and the bottom dc rails, respectively. Herein, the working principles of the proposed iTCM-operated three-phase three-wire VSC are comprehensively explained, and a detailed design guideline for the *LC* branch and *LCL* filter is offered. Analytical models for component stresses and the reverse current waveform have been developed and corroborated through PLECS simulations. A 3-kW, heatsink-less VSC system was constructed and tested, confirming both the system's effective functionality and the enhanced power efficiency of the proposed capacitor-split VG connection. Therein, the studied system demonstrated a significant efficiency improvement, ranging from 0.51% to 2% across the entire operating power spectrum, as compared to the conventional VG connection in iTCM-operated VSCs.**

***Index Terms*—Bidirectional rectifier, integrated triangular current mode (iTCM), power factor correction (PFC), voltage-source converter (VSC), zero-voltage switching (ZVS).**

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I. Introduction

THREE-PHASE ac–dc voltage-source converters (VSCs) are widely used in various industrial applications involving interaction with the public ac grid, such as renewable energy sources, battery chargers, static synchronous compensators, four-quadrant motor drives, data-centres, and more [1], [2], [3], [4], [5]. Three-phase three-wire two-level VSCs, exemplified in Fig. 1(a) and (b), primarily function as front-end conversion stages providing power factor correction (PFC) while connecting to the public grid via an ac filter to comply with the grid-current harmonic standards. These circuits provide a controllable dc voltage to either the load or the subsequent back-end circuit stage, e.g., a dc–dc or a dc–ac converter. High efficiency has been observed in the two-level VSC utilizing GaN or SiC MOSFET switches while operating at hard-switching pulsewidth modulation (PWM) with a fixed switching frequency set above the audible frequency range [2], [6]. However, thermal management and cost constraints limit the maximum switching frequency, impacting the maximal achievable power density of the system. Typically, commercial three-phase VSC systems achieve peak efficiencies below 98% and power densities below 3 kW/L, restricted by the need for large ac filters for harmonic compliance and substantial cooling systems to maintain semiconductor temperatures within safe limits.

Note that the circuits shown in Fig. 1(a) and (b) employ an *LCL*-based ac filter for supra-harmonics current attenuation with a virtual ground (VG) connected at the mid-point of the dc-link capacitors [cf. Fig. 1(a)] or VG connected at the top and the bottom dc rails [cf. Fig. 1(b)]. The VG concept was originally introduced in [7] to provide (from the grid point of view) high-frequency common-mode voltage (CMV) attenuation in three-phase three-wire VSCs, and has become a common solution in three-phase transformer-less solar inverters [3]. Interestingly, the VG creates a high-frequency CMV circulating path (through L_c and C_f) that can be used to provide a decoupling mechanism between the operation of the three phases of the VSC system. Therefore, by properly designing the cutoff frequency of the low-pass filter formed by L_c and C_f, the high-frequency components of the three-wire system can be seen as generated by three independent operated single-phase half-bridge converters because the zero-sequence current components (from the half-bridge operating switching-frequency band and above)

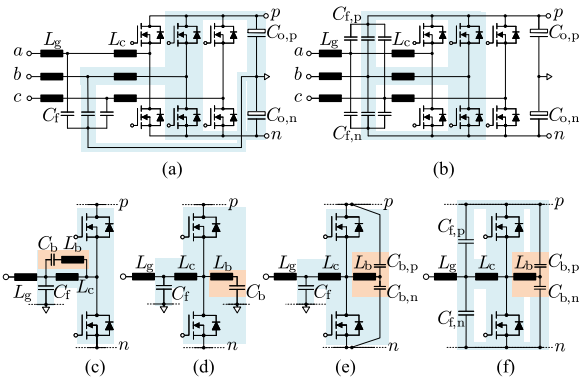


Fig. 1. Three-phase three-wire VSC: conventional circuit employing *LCL* harmonic filter using VG (a) at the mid-point of the dc-link capacitors; (b) at the top and the bottom dc rails. Illustrative single phase-leg featuring the iTCM configuration enabled by a passive *LC* branch highlighted in orange: (c) connected to the ac side (option 1); (d) connected to the mid-point of the dc-link capacitors (option 2); (e) connected at the top and the bottom dc rails (option 3); and (f) option 3 and *LCL* filter connected at the top and the bottom dc rails (option 4). Note that the necessary conductive EMI filter and protection devices at the ac and dc sides are not shown in this figure.

can circulate through L_c and C_f without much influence from the other half-bridge phases. The primary benefit of the VG connection at the top and the bottom dc rails [cf. Fig. 1(b)] lies in the reduction of current stress on the dc-link capacitor, because the path for the zero-sequence current components in each phase-bridges are confined within the top and the bottom dc rails without circulating through the typical electrolytic technology-based capacitors $C_{o,p}$ and $C_{o,n}$ as it typically occurs in Fig. 1(a).

A general strategy to improve the power density and specific power of the rectifier stage is to select a high switching frequency to reduce the size of the supraharmonics *LCL* ac filter. However, an increase in the switching frequency can escalate semiconductor switching losses and challenge both power efficiency and thermal management. Moreover, a higher switching frequency could also have an adverse impact on the high-frequency electromagnetic interference (EMI) filtering, which is specifically responsible for attenuating harmonics ranging from 150 kHz to 30 MHz. Therefore, a balanced tradeoff between efficiency and power density in designing grid-connected converters is necessary.

When operating at high frequencies, soft-switching turn-ON is of great relevance for efficiency improvement since the turn-ON loss can account for over 70% of the total loss even with wide-bandgap (WBG) semiconductors (e.g. SiC MOSFETs) [8], [9], [10]. Triangular current mode (TCM) modulation, known for its zero-voltage-switching (ZVS) turn-ON capability [8], [9], [10], [11], [12], [13], [14], [15], [16], has been a widely-used and promising technique to achieve extremely high efficiency and high power density for various applications, despite the fact that there are actually still minor residual ZVS losses left [11]. TCM operation has been extensively explored in single-phase rectifiers, featuring ZVS turn-ON [8], [9], [10], [11], [12], [13]. In TCM operation, in each switching period, the semiconductor current is manipulated to reach at least a minimal current (denoted as I_{zvs}) in the opposite direction (or reverse polarity) of the desired phase current before the switching-ON command. This entails that after the switching-OFF of the complementary switch, during the deadtime t_d, the voltage across the parasitic capacitance of the switch to be turned-ON drops to zero, allowing its body diode to conduct before the turn-ON command arrives. Subsequently, after the turn-ON command, the switch will start conducting when the polarity of the current reverses back to the desired polarity, so that full ZVS turn-ON is achieved. Detailed insights into ZVS in single-phase rectifiers can be found in [15] and [17].

The TCM operation presents two significant drawbacks that complicate the ac filter design as required for compliance with the grid standards: first, it induces large current ripple in the phase-leg, which needs to be confined within the converter; second, its variable frequency operation is dependent on several factors, including the circuit parameters, the instantaneous processed power, and the voltage levels of the grid and the dc link. To address the issue of large current ripples within the converter, the work in [10] proposed adding multiple parallel phase-legs, which are operated with symmetrical interleaved command within a switching period, effectively canceling out current harmonics and evenly distributing the total phase currents. This approach simplifies the design of the ac filter and helps distribute power losses among multiple circuit components. The latter enhances the thermal management of the system, but it requires a relatively complex control for PWM pulse synchronization, along with multiple high-bandwidth current measurement devices and gate drivers [8]. The works presented in [15], [18], and [19] introduce the use of an auxiliary *LC* branch in a single-phase inverter for splitting the TCM current flowing through the half-bridge semiconductors into ideally two parts, the low- and high-frequency current harmonics. The concept of employing the *LC* branch and TCM operation is termed integrated triangular current mode operation (iTCM) in [15], and the same nomenclature is kept in this study. Note that for an ac–dc converter the magnitude of the high-frequency components will be shared between the added *LC* branch and the converter-side inductor L_c of the typically employed *LCL* filter, while the grid will process the 50 Hz current component and the permissible remaining high-frequency component. Note that the *LCL* filter should be designed in such a way that the high-frequency component flowing into L_c will be confined into C_f and its 50 Hz component will flow into L_g [20].

The operation of iTCM in terms of achieving ZVS for semiconductors is similar to that of the conventional TCM strategy. In both TCM and iTCM methods, the required switching frequency operating range can be extremely (and prohibitively) wide. The wide-frequency range is particularly critical for the operation, which aims to minimize the circulating current in the circuit by restricting the ZVS switched current to a fixed (and maximum) value close to the minimal required current that guarantees ZVS, i.e., I_{zvs}, as illustrated in Fig. 3(b). To limit such a wide-frequency range, one common method is to increase the ripple current across the bridge-leg.

A soft-switching three-phase three-wire VSC system was proposed in [21]. However, due to the absence of a low impedance path for the zero-sequence current, the modulation implemented becomes relatively complex, requiring some phase currents to operate in discontinuous conduction mode. As discussed and

shown in Fig. 1(a) and (b), the usage of VG in the filter stage allows the high-frequency operational decoupling between the three half-bridge switching legs, thereby enabling conventional TCM operation. Herein, the two strategies discussed previously, namely, the parallel interleaved strategy (cf. [10]), or the iTCM strategy (cf. [18]), which are necessary for the ZVS operation to reduce the current ripple, can be applied.

The iTCM arrangement can be implemented in four ways as illustrated in Fig. 1(c)–(f). The implementations illustrated in Fig. 1(c) and (d) have been presented in [22]. To the best of the authors' knowledge in the literature today, the iTCM control methods presented in Fig. 1(e) and (f) represent novel contributions in this work. The iTCM method depicted in Fig. 1(c) will exhibit increased current stress on the filter capacitor $C_{\rm f}$, because it will process the whole high-frequency current components. The solutions shown in Fig. 1(d)–(f) provide an alternative parallel path that can be designed to split the low- and high-frequency current harmonics. For the methods depicted in Fig. 1(e) and (f), the filter capacitors, i.e., $C_{\rm f}$ and/or $C_{\rm b}$, are split into two halves that are connected to the top and the bottom dc rails, respectively. This capacitor-split topology is preferable in terms of current stress reduction in the dc-link capacitors because the high-frequency zero-sequence current components of the TCM operation will be confined in between the half-bridge switching cells and the top and the bottom dc rails. This characteristic is investigated in more detail in Section III-B. Finally, the circuit illustrated in Fig. 1(f) has the advantage that the high-frequency current component circulating through the *LCL* filter also stays confined to the top and the bottom dc rails. The main drawback of Fig. 1(f) is that the part count of the filter capacitors increases and that they will need to be able to block higher voltages because the dc rail connections will cause a voltage level shift of approximately $+\frac{V_{\rm dc}}{2}$ for those connected to the top dc rail and $-\frac{V_{\rm dc}}{2}$ for the ones connected to the bottom dc rail. This voltage level shift will be superimposed on the low-frequency voltage generated by the half-bridges.

All in all, this article contributes to the following points.

1) A new capacitor-split VG topology that facilitates iTCM operation is proposed to further improve the power conversion efficiency of the system.
2) Theoretical working principles of iTCM with the studied three-phase three-wire VSC system are thoroughly explained. The superiority of the proposed VG connection over the conventional one is analyzed in detail and validated through both simulations and experiments.
3) A mathematical model that accurately predicts the actual reverse current waveform is derived and verified by simulations.

The rest of this article is organized as follows. In Section II, the working principle of the proposed three-phase three-wire VSC operating with iTCM control as well as the design guideline for *LC* branch and *LCL* filters are detailed. In Section III, analytical models of the main components stress and the reverse current waveform are derived and validated by simulations in PLECS. Moreover, an analysis of the current ripples in the dc-link capacitors with different VG connections is given. In Section IV, the feasibility of the proposed converter system is verified with a 3-kW hardware demonstrator, and the performances of different VG solutions are benchmarked. Finally, Section V concludes this article.

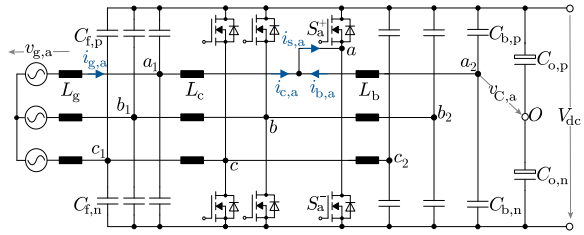


Fig. 2. Proposed three-phase three-wire VSC system featuring iTCM-control enabled by the capacitor-split VG connection of the *LCL* filter and the auxiliary *LC* branch. The switching node "a" is specifically extended to show the relationship between $i_{\rm s}$, $i_{\rm c}$, and $i_{\rm b}$.

II. Three-Phase VSC System With iTCM

A. Working Principle

The iTCM controlled three-phase three-wire ac–dc converter proposed in this work is shown in Fig. 2. Both the auxiliary *LC* branch and the *LCL* filter capacitors are split and connected to the dc-link top and bottom rails. The VG connection ensures the three half-bridge phases are decoupled from each other so that the zero-sequence voltage components generated at the switching nodes can be used to have a tight control of the half-bridge phase currents, and thus, the desired ZVS turn-ON is realized by the TCM operation.

In the proposed circuit, conventional modulation techniques such as the sinusoidal PWM (SPWM) method can be used and fairly easily extended to space vector PWM (SVPWM) or $\frac{1}{4}$ third harmonic injection PWM ($\frac{1}{4}$THIPWM) [23]. For a specific phase x ($x \in \{a, b, c\}$), these PWM modulators can be modeled by (1) and (2), where M is the modulation index, $V_{\rm dc}$ is the total dc-link voltage, $\hat{v}_{\rm g}$ is the magnitude of the symmetric three-phase grid line-to-neutral voltage $v_{\rm g,x}(t)$ given in (3), ω_0 is the grid angular frequency, $\varphi_{\rm x}$ is the phase shift (in radians $\varphi_{\rm x} = 0$, $-\frac{2\pi}{3}$, and $\frac{2\pi}{3}$ for phase a, b, and c, respectively), and the function $\mathrm{tri}(\omega_0 t)$ (for SVPWM) can be obtained as in (4), where $\mathrm{X_p}(\omega_0 t)$ and $\mathrm{X_n}(\omega_0 t)$ are given by (5) and (6), respectively

$$M = \frac{\hat{v}_{\rm g}}{V_{\rm dc}/2} \tag{1}$$

$$m_{\rm x}(t) = \begin{cases} \text{SPWM} \\ \quad M \cdot \sin(\omega_0 t + \varphi_{\rm x}) \\ \frac{1}{4}\text{THIPWM} \\ \quad M \cdot \left(\sin(\omega_0 t + \varphi_{\rm x}) + \underbrace{\frac{1}{4}\sin(3\omega_0 t + 3\varphi_{\rm x})}_{\text{zero seq. injection}} \right) \\ \text{SVPWM} \\ \quad M \cdot \left(\sin(\omega_0 t + \varphi_{\rm x}) + \underbrace{\frac{1}{4}\mathrm{tri}(\omega_0 t)}_{\text{zero seq. injection}} \right) \end{cases} \tag{2}$$

$$\begin{cases} v_{\mathrm{g,a}}(t) = \hat{v}_{\mathrm{g}} \sin\left(\omega_0 t \underbrace{+0}_{\varphi_{\mathrm{a}}}\right) \\ v_{\mathrm{g,b}}(t) = \hat{v}_{\mathrm{g}} \sin\left(\omega_0 t \underbrace{-\frac{2\pi}{3}}_{\varphi_{\mathrm{b}}}\right) \\ v_{\mathrm{g,c}}(t) = \hat{v}_{\mathrm{g}} \sin\left(\omega_0 t \underbrace{+\frac{2\pi}{3}}_{\varphi_{\mathrm{c}}}\right) \end{cases} \tag{3}$$

$$\mathrm{tri}(\omega_0 t) = -2(\mathrm{X_p}(\omega_0 t) + \mathrm{X_n}(\omega_0 t)) \tag{4}$$

$$\mathrm{X_p}(\omega_0 t) = \frac{1}{\hat{v}_{\mathrm{g}}} \cdot \max\{v_{\mathrm{g,a}}(t), v_{\mathrm{g,b}}(t), v_{\mathrm{g,c}}(t)\} \tag{5}$$

$$\mathrm{X_n}(\omega_0 t) = \frac{1}{\hat{v}_{\mathrm{g}}} \cdot \min\{v_{\mathrm{g,a}}(t), v_{\mathrm{g,b}}(t), v_{\mathrm{g,c}}(t)\}. \tag{6}$$

Assuming a negligible low-frequency voltage drop across L_{c} and L_{b}, the circuit in Fig. 2 will have a low-frequency voltage component $v_{\mathrm{C,x}}(t)$ at the terminals of capacitors $C_{\mathrm{f,p/n}}$ (terminal x_1, $x \in \{a, b, c\}$) or $C_{\mathrm{b,p/n}}$ (terminal x_2, $x \in \{a, b, c\}$) with respect to the dc-link mid-point (terminal O) as given in (7). Assuming symmetry between the upper and lower filter capacitors, i.e., $C_{\mathrm{f/b,p}} = C_{\mathrm{f/b,n}}$, for phase x the low-frequency current components drawn by the *LCL* filter capacitors and the auxiliary *LC* branch capacitors (denoted $i_{\mathrm{Cf,x}}$ and $i_{\mathrm{Cb,x}}$, respectively) can be determined as (8)

$$v_{\mathrm{C,x}}(t) = \frac{V_{\mathrm{dc}}}{2} \cdot m_{\mathrm{x}}(t) \tag{7}$$

$$i_{\mathrm{Cf/b,x}}(t) = 2C_{\mathrm{f,b,p/n}} \cdot \frac{\mathrm{d}}{\mathrm{d}t} v_{\mathrm{C,x}}(t). \tag{8}$$

For phase x, the current $i_{\mathrm{s,x}}$ flowing through the semiconductors is close to a triangle wave featuring a large peak-to-peak current ripple $\triangle i_{\mathrm{s,x}}$, as illustrated in Fig. 3(b). The upper and the lower current envelopes are denoted as $i^{+}_{\mathrm{sx,env}}$ and $i^{-}_{\mathrm{sx,env}}$, respectively. For high power factor operation each grid-side current is in phase with their respective phase-to-neutral grid voltage $v_{\mathrm{g,x}}(t) = \hat{v}_{\mathrm{g}} \sin(\omega_0 t + \varphi_{\mathrm{x}})$, so the grid-side current $i_{\mathrm{g,x}}$ can be expressed as $i_{\mathrm{g,x}}(t) = \hat{i}_{\mathrm{g}} \sin(\omega_0 t + \varphi_{\mathrm{x}}) = \frac{2}{3}\frac{P}{\hat{v}_{\mathrm{g}}} \sin(\omega_0 t + \varphi_{\mathrm{x}})$, where $\hat{v}_{\mathrm{g}}$ and $\hat{i}_{\mathrm{g}}$ are the grid-side peak values of the voltage and current, respectively, P is the three-phase input active power. For each switching period $i_{\mathrm{s,x}}$ goes to the reverse polarity at a certain value denoted as $|I_{\mathrm{zvs}}|$. Consequently, the body diode of MOSFET always conducts before the actual turn-ON of the switch so that the full ZVS turn-ON is achieved.

The key to achieve ZVS turn-ON is to charge the output capacitance C_{oss} of the switch to be turned-OFF from 0 V to V_{dc} and fully discharge C_{oss} of the one to be turned-ON from V_{dc} to 0 V. The equivalent total charge to be shifted from the upper and lower half-bridge's switches is due to two output capacitances $2C_{\mathrm{oss}}$. Based on the voltage-impedance current (V-Zi) method described in [17], the ZVS resonance interval for a three-phase system is shown in Fig. 4, and therefore, the minimum reverse conducting current $|I_{\mathrm{zvs}}|$ to ensure full ZVS could be expressed

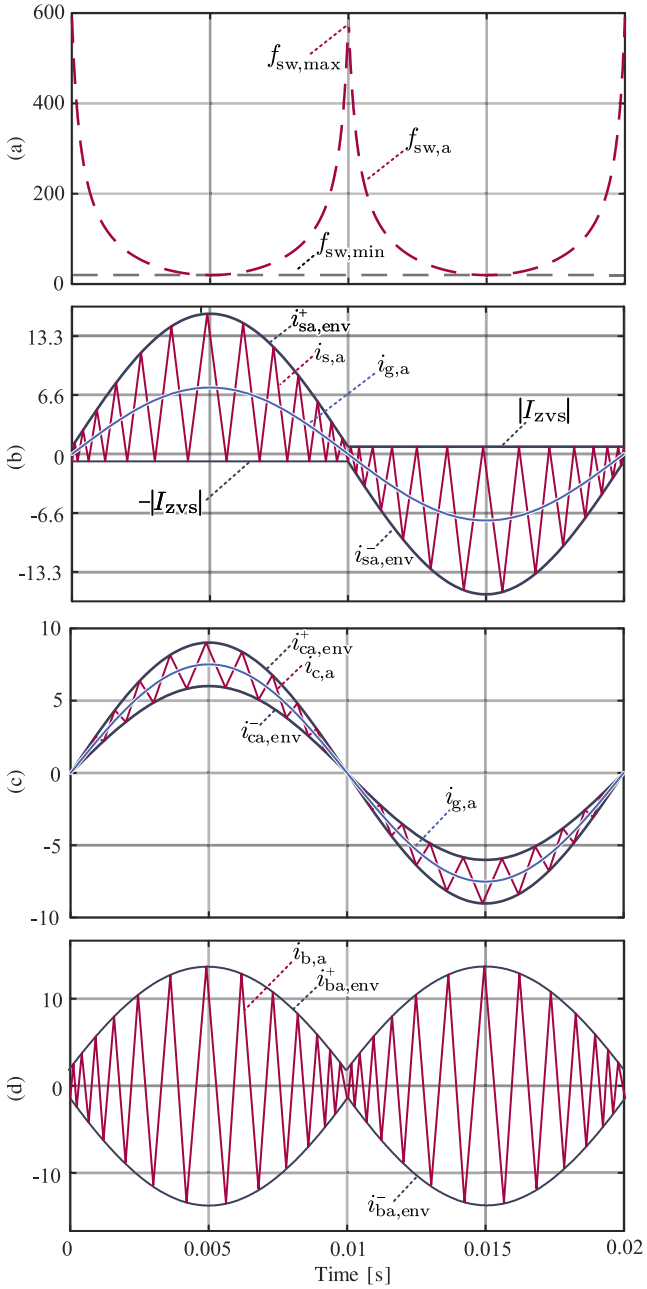


Fig. 3. Illustration of the main operational TCM or iTCM waveforms for the proposed converter (only phase $x = a$) in one grid period. (a) Instantaneous operating switching frequency ($f_{\mathrm{sw,a}}$). (b) Half-bridge semiconductor current $i_{\mathrm{s,a}}$ with constant reversal current I_{zvs}. (c) *LCL* filter converter-side current $i_{\mathrm{c,a}}$ (or current across L_{c}) with a relatively small ripple factor r. (d) *LC* branch current $i_{\mathrm{b,a}}$.

by the characteristic impedance Z of the *LC* circuit as in (9). Note that the C_{oss} of the MOSFET features a highly nonlinear nature and the charge-equivalent of the output capacitance $C_{\mathrm{oss,Q}}$ should be used in the calculation [11]

$$\begin{cases} |I_{\mathrm{zvs}}| = \sqrt{M} \cdot V_{\mathrm{dc}}/Z \\ Z = \sqrt{L/(2C_{\mathrm{oss,Q}})}. \end{cases} \tag{9}$$

In practice, however, the value L in (9) is usually much larger than of the C_{oss}, the charging/discharging current can reasonably

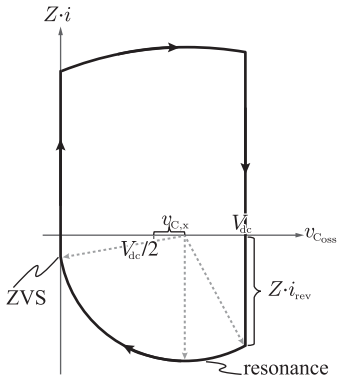


Fig. 4. V-Zi plot of the studied three-phase system in one switching cycle featuring ZVS turn-ON under rectifier mode.

be viewed as constant $|I_{\rm zvs}|$ during the resonance interval. This leads to a simpler alternative way of calculating $|I_{\rm zvs}|$ as given by (67) in Section IV.

The current envelopes $i^{+}_{\rm sx,env}$ and $i^{-}_{\rm sx,env}$ can be determined by (10) for $i_{\rm lf,x}(t) \geq 0$ and (11) for $i_{\rm lf,x}(t) < 0$, where $i_{\rm lf,x}(t)$ denotes the sum of all the low-frequency current components drawn by phase x as given in (12). The instantaneous peak-to-peak current ripple $\triangle i_{\rm s,x}$ of MOSFET is given in (13)

$$\begin{cases} i^{+}_{\rm sx,env} = |I_{\rm zvs}| + 2i_{\rm lf,x}(t) \\ i^{-}_{\rm sx,env} = -|I_{\rm zvs}| \end{cases} \tag{10}$$

$$\begin{cases} i^{+}_{\rm sx,env} = |I_{\rm zvs}| \\ i^{-}_{\rm sx,env} = -|I_{\rm zvs}| + 2i_{\rm lf,x}(t) \end{cases} \tag{11}$$

$$i_{\rm lf,x}(t) = \hat{i}_{\rm g}\sin(\omega_0 t + \varphi_{\rm x}) + i_{\rm Cf,x}(t) + i_{\rm Cb,x}(t) \tag{12}$$

$$\triangle i_{\rm s,x}(t) = i^{+}_{\rm sx,env} - i^{-}_{\rm sx,env} = 2|I_{\rm zvs}| + 2|i_{\rm lf,x}(t)|. \tag{13}$$

Usually the low-frequency components of $i_{\rm Cf/b,x}(t)$ are very small in magnitude as compared to $i_{\rm g,x}(t)$, and thus, the terms related to capacitor currents in (12) can be reasonably neglected. Therefore, it is hereafter assumed that $i_{\rm lf,x}(t) = \hat{i}_{\rm g}\sin(\omega_0 t + \varphi_{\rm x})$ for the rest of this article unless specified otherwise. Based on this assumption (10), (11), and (13) can be simplified into (14), (15), and (16), respectively

$$\begin{cases} i^{+}_{\rm sx,env} = |I_{\rm zvs}| + 2\hat{i}_{\rm g}\sin(\omega_0 t + \varphi_{\rm x}) \\ i^{-}_{\rm sx,env} = -|I_{\rm zvs}| \end{cases} \tag{14}$$

$$\begin{cases} i^{+}_{\rm sx,env} = |I_{\rm zvs}| \\ i^{-}_{\rm sx,env} = -|I_{\rm zvs}| + 2\hat{i}_{\rm g}\sin(\omega_0 t + \varphi_{\rm x}) \end{cases} \tag{15}$$

$$\triangle i_{\rm s,x}(t) = 2|I_{\rm zvs}| + 2\hat{i}_{\rm g}|\sin(\omega_0 t + \varphi_{\rm x})|. \tag{16}$$

For phase x, the ON- and OFF-time for the high-side switch S^{+}_{x} (and vice versa for the complementary low-side switch S^{-}_{x}) can be determined as (17) and (18), respectively, where the equivalent inductance L is defined in (19)

$$t_{\rm on,x}(t) = \frac{\triangle i_{\rm s,x}(t)}{\frac{1}{2}V_{\rm dc} - v_{\rm C,x}(t)} \cdot L \tag{17}$$

$$t_{\rm off,x}(t) = \frac{\triangle i_{\rm s,x}(t)}{\frac{1}{2}V_{\rm dc} + v_{\rm C,x}(t)} \cdot L \tag{18}$$

$$L = \frac{L_{\rm c} \cdot L_{\rm b}}{L_{\rm c} + L_{\rm b}}. \tag{19}$$

The instantaneous switching frequency $f_{\rm sw,x}(t)$ shown in Fig. 3(a) varies with time to achieve a constant reverse current $|I_{\rm zvs}|$, which can be expressed as

$$f_{\rm sw,x}(t) = \frac{1}{t_{\rm on,x}(t) + t_{\rm off,x}(t)} = \frac{\frac{1}{4}V_{\rm dc}^2 - v_{\rm C,x}(t)^2}{L \cdot \triangle i_{\rm s,x}(t) \cdot V_{\rm dc}}. \tag{20}$$

For SPWM operation, the minimal and maximal switching frequencies can be calculated as in (21) and (22), respectively

$$f_{\rm sw,min} = \frac{1}{2(|I_{\rm zvs}| + \hat{i}_{\rm g}) \cdot L} \cdot \frac{\frac{1}{4}V_{\rm dc}^2 - \hat{v}_{\rm g}^2}{V_{\rm dc}} \tag{21}$$

$$f_{\rm sw,max} = \frac{V_{\rm dc}}{8L \cdot |I_{\rm zvs}|}. \tag{22}$$

The current envelopes of $L_{\rm c}$, i.e., $i^{+}_{\rm cx,env}$ and $i^{-}_{\rm cx,env}$, are determined by (23) and (24), where the instantaneous peak-to-peak current ripple $\triangle i_{\rm c,x}(t)$ is given in (25). The current envelopes of $L_{\rm b}$, i.e., $i^{+}_{\rm bx,env}$ and $i^{-}_{\rm bx,env}$, are determined by (26) and (27), where the instantaneous peak-to-peak current ripple $\triangle i_{\rm b,x}(t)$ can be calculated as in (28)

$$i^{+}_{\rm cx,env}(t) = \hat{i}_{\rm g}\sin(\omega_0 t + \varphi_{\rm x}) + \frac{1}{2}\triangle i_{\rm c,x}(t) \tag{23}$$

$$i^{-}_{\rm cx,env}(t) = \hat{i}_{\rm g}\sin(\omega_0 t + \varphi_{\rm x}) - \frac{1}{2}\triangle i_{\rm c,x}(t) \tag{24}$$

$$\triangle i_{\rm c,x}(t) = \frac{\frac{1}{2}V_{\rm dc} - v_{\rm C,x}(t)}{L_{\rm c}} \cdot t_{\rm on,x}(t) \tag{25}$$

$$i^{+}_{\rm bx,env}(t) = \frac{1}{2}\triangle i_{\rm b,x}(t) \tag{26}$$

$$i^{-}_{\rm bx,env}(t) = -\frac{1}{2}\triangle i_{\rm b,x}(t) \tag{27}$$

$$\triangle i_{\rm b,x}(t) = \frac{\frac{1}{2}V_{\rm dc} - v_{\rm C,x}(t)}{L_{\rm b}} \cdot t_{\rm on,x}(t). \tag{28}$$

B. Design Guideline for LC Branch and LCL Filters

The minimum operating switching frequency $f_{\rm sw,min}$ could be limited to avoid an operation in the range of audible noise. Therefore, $f_{\rm sw,min}$ could be used to define the maximum values of L [which depends on $L_{\rm c}$ and $L_{\rm b}$ as shown in (19)], while considering the rated power of the system. As can be seen in Fig. 3(c) and (d), the current $i_{\rm s,x}$ is split between the *LC* branch and the *LCL* filter. The current stress across the two circuit paths is strongly dependent on the values of L_c and L_b. Therefore, another design parameter r is introduced and defined as the ratio of the maximum peak-to-peak current ripple allowed for $i_{\rm c,x}$ ($\triangle i_{\rm cx,max}$) to the peak current on the grid side, i.e., $r = \triangle i_{\rm cx,max} \,/\, \hat{i}_{\rm g}$. The factor r becomes a user design choice that can be utilized to determine the inductance value of $L_{\rm c}$. For SPWM operation, the value of $L_{\rm c}$ is given by the following

equation:

$$L_{\mathrm{c}} = \frac{1}{\underbrace{(\hat{i}_{\mathrm{g}} \cdot r)}_{\triangle i_{\mathrm{cx,max}}} \cdot f_{\mathrm{sw,min}}} \cdot \frac{\frac{1}{4}V_{\mathrm{dc}}^2 - \hat{v}_{\mathrm{g}}^2}{V_{\mathrm{dc}}}. \tag{29}$$

Combining (19), (21), and (29), L_{b} can be derived as in (30)

$$L_{\mathrm{b}} = \frac{1}{f_{\mathrm{sw,min}} \cdot (2|I_{\mathrm{zvs}}| + 2\hat{i}_{\mathrm{g}} - \hat{i}_{\mathrm{g}} \cdot r)} \cdot \frac{\frac{1}{4}V_{\mathrm{dc}}^2 - \hat{v}_{\mathrm{g}}^2}{V_{\mathrm{dc}}}. \tag{30}$$

The coefficient r can be selected from 0% to 200%. When $r \approx 200\%$, the control scheme becomes equivalent to the TCM control, i.e., it will lead to $L_{\mathrm{b}} \gg L_{\mathrm{c}}$, and when $r \approx 0\%$ the value of $L_{\mathrm{c}} \gg L_{\mathrm{b}}$. The optimal value of r will depend on the target design metric being optimized.

The maximum switching frequency given in (22) can be unrealistically high, posing some challenges to the practical implementation as well as to the design of the EMI filter [24]. Therefore, the switching frequency could be limited to a maximum value. In this case, the ZVS turn-ON is still guaranteed but the reverse current is not constant at $|I_{\mathrm{zvs}}|$ anymore. This will cause a larger peak-to-peak current ripple around the current zero-crossing point, leading to a higher turn-OFF current compared to the case without switching frequency limitation. Since the turn-OFF loss feature of WBG semiconductors is relatively low in comparison to the turn-ON, and due to the fact the switched current is naturally smaller close to the zero-crossing of the phase current, this trade-OFF is considered acceptable.

The transfer function from the converter output phase voltage $v_{\mathrm{c}}(s)$ to the grid-side current $i_{\mathrm{g}}(s)$ is expressed as follows:

$$\frac{i_{\mathrm{g}}(s)}{v_{\mathrm{c}}(s)} = \frac{\omega_{\mathrm{res}}^2}{L_{\mathrm{T}} s(s^2 + \omega_{\mathrm{res}}^2)} \tag{31}$$

where ω_{res}, L_{T} and C_{f} are the resonance frequency, the total inductance, and the total capacitance of the *LCL* filter, respectively, and expressed as

$$\omega_{\mathrm{res}} = \sqrt{\frac{L_{\mathrm{c}} + L_{\mathrm{g}}}{L_{\mathrm{c}} L_{\mathrm{g}} C_{\mathrm{f}}}} \tag{32}$$

$$L_{\mathrm{T}} = L_{\mathrm{c}} + L_{\mathrm{g}} \tag{33}$$

$$C_{\mathrm{f}} = C_{\mathrm{fp}} + C_{\mathrm{fn}}. \tag{34}$$

Therefore, the attenuation function in the frequency domain can be represented as follows:

$$\mathrm{Att}(\omega) = \left|\left|\frac{i_{\mathrm{g}}(j\omega)}{v_{\mathrm{c}}(j\omega)}\right|\right| = \frac{1}{L_{\mathrm{T}}} \cdot \frac{\omega_{\mathrm{res}}^2}{\omega|\omega^2 - \omega_{\mathrm{res}}^2|}. \tag{35}$$

Usually, the resonance frequency is set to be larger than $\frac{1}{6}$ times the switching frequency to achieve the stability of grid-side current control with the inherent damping under the continuous PWM methods [25]. Hence, extra active damping methods can be avoided, which are usually needed and potentially complicates the controller [26], [27], [28].

Generally, the current harmonics should be attenuated below the emission limits set by relevant standards, e.g., IEEE-519 and IEC-61000. Specifically, IEEE-519 defines the minimum acceptable harmonic emission limit for the currents, namely 0.3% of the fundamental current [29], noted as I_{IEEE519} in this article. Hence, the required minimum attenuation can be derived as

$$\mathrm{Att}_{\mathrm{req}} = \frac{I_{\mathrm{IEEE519}}}{V_{\mathrm{crit}}}. \tag{36}$$

By combining (35) and (36), the minimum required total inductance of the *LCL* filter for satisfying the standard can be derived as

$$L_{\mathrm{T-req}} = \frac{\omega_{\mathrm{res}}^2 V_{\mathrm{crit}}}{\omega_{\mathrm{crit}}|\omega_{\mathrm{crit}}^2 - \omega_{\mathrm{res}}^2| I_{\mathrm{IEEE519}}}. \tag{37}$$

Since L_{c} is determined by the ZVS operation as in (29), L_{g} is solely determined by the current harmonics filtering process

$$L_{\mathrm{g}} \geqslant L_{\mathrm{T-req}} - L_{\mathrm{c}}. \tag{38}$$

As a constraint for the *LCL* filter design, the maximum ac filter capacitance (i.e., the sum of C_{f} and C_{b}) is limited by the maximum allowable reactive power consumed by the converter. Hence, the filter capacitance should satisfy

$$C_{\mathrm{f}} + C_{\mathrm{b}} < q \cdot \frac{S_{\mathrm{N}}}{3\omega_{\mathrm{o}} V_{\mathrm{ac}}^2} \tag{39}$$

where S_{N} is the rated power of the converter and q is reactive power ratio and selected to be 5% in this article. C_{f} can be calculated based on (32), and C_{b} can subsequently be obtained by (39).

Based on the abovementioned design guideline for the *LCL* filter and *LC* branch, key circuit parameters for both the simulations and the experiments in later sections are obtained as listed in Table I. The harmonic spectrum of the simulated grid current waveform acquired through FFT analysis is shown in Fig. 5, verifying that the filter design complies with IEEE-519.

TABLE I
SYSTEM SPECIFICATIONS AND KEY CIRCUIT PARAMETERS FOR BOTH SIMULATION AND HARDWARE EXPERIMENT

	Symbol	Value
AC phase voltage	v_{ac}	230 V rms
Mains frequency	f_0	50 Hz
DC voltage	V_{dc}	800 V
Modulation index	M	0.813
Nominal output power	P_{o}	3.174 kW
Reverse current reference	$\lvert I_{\mathrm{zvs}}\rvert$	1.5 A
Grid-side inductance	L_{g}	325.5 μH
Converter-side inductance	L_{c}	325.5 μH
LC branch inductance	L_{b}	325.5 μH
LCL filter capacitance	$C_{\mathrm{f,p/n}}$	0.7 μF
LC branch capacitance	$C_{\mathrm{b,p/n}}$	0.7 μF
Current sharing coefficient	r	1.24

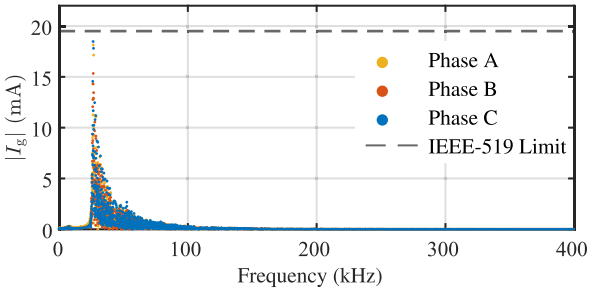


Fig. 5. Harmonic spectrum of the three-phase grid currents in compliance with IEEE-519.

III. Mathematical Modeling and Simulation Verification

A. Modeling of the Main Component Stresses

The maximum voltage stress across the semiconductors ($v_{\mathrm{S,max}}$) is defined by the maximum dc-link voltage ($V_{\mathrm{dc,max}}$)

$$v_{\mathrm{S,max}} = V_{\mathrm{dc,max}}. \tag{40}$$

For iTCM operation, the instantaneous rms current $i_{\mathrm{yx,rms}}(t)$ during each switching period flowing through several circuit components within the phase x can be calculated by (41), where the index y represents different circuit components, such as the half-bridge's ac terminal ($i_{\mathrm{sx,rms}}(t)$ with $y{=}s$), and the inductors L_{c} ($i_{\mathrm{cx,rms}}(t)$ with $y{=}c$) and L_{b} ($i_{\mathrm{bx,rms}}(t)$ with $y{=}b$)

$$i^2_{\mathrm{yx,rms}}(t) = \frac{1}{3}\left[i^+_{\mathrm{yx,env}}(t)^2 + i^+_{\mathrm{yx,env}}(t)\cdot i^-_{\mathrm{yx,env}}(t) + i^-_{\mathrm{yx,env}}(t)^2\right]. \tag{41}$$

Since the switching periods are negligibly small as compared to the grid period, (41) can reasonably be viewed as a continuous function and the total rms value of a certain components y for phase x over one grid cycle, which is denoted as $I_{\mathrm{y,rms}}$, can be calculated by taking the rms value of the integral of (41) over one grid cycle.

Based on (14), (15), and (41), the rms value of the semiconductor current $I_{\mathrm{s,rms}}$ can be derived as

$$I_{\mathrm{s,rms}} = \sqrt{\frac{1}{3}\left(2\,\hat{i}^2_{\mathrm{g}} + \frac{4}{\pi}\,\hat{i}_{\mathrm{g}}\,I_{\mathrm{zvs}} + I^2_{\mathrm{zvs}}\right)}. \tag{42}$$

Subsequently, the rms current of a single MOSFET switch $I_{\mathrm{sw,rms}}$ can be calculated as in (43) due to the symmetrical operation of the upper and lower phase legs over one grid cycle

$$I_{\mathrm{sw,rms}} = \frac{I_{\mathrm{s,rms}}}{\sqrt{2}}. \tag{43}$$

Defining a current-dividing coefficient k as in (44), which represents the proportion of $\triangle i_{\mathrm{s,x}}$ that flows through L_{c}, based on (16), (23), (24), (41), and (44), the rms current of L_{c} (denoted as $I_{\mathrm{c,rms}}$) can be derived as in (45)

$$k = \frac{L_{\mathrm{b}}}{L_{\mathrm{c}} + L_{\mathrm{b}}} = \frac{\triangle i_{\mathrm{c,x}}}{\triangle i_{\mathrm{s,x}}} = \frac{\triangle i_{\mathrm{s,x}} - \triangle i_{\mathrm{b,x}}}{\triangle i_{\mathrm{s,x}}} \tag{44}$$

$$I_{\mathrm{c,rms}} = \sqrt{\frac{1}{3}\left(\frac{3+k^2}{2}\,\hat{i}^2_{\mathrm{g}} + \frac{4\,k^2}{\pi}\,\hat{i}_{\mathrm{g}}\,I_{\mathrm{zvs}} + k^2\,I^2_{\mathrm{zvs}}\right)}. \tag{45}$$

TABLE II
Comparison of Analytical Current Stress Models and Simulation Results

Variable	Model-based calculation	Simulation	Deviation (%)
$I_{\mathrm{s,rms}}$	5.756 A	5.822 A	−1.13
$I_{\mathrm{sw,rms}}$	4.070 A	4.109 A	−0.949
$I_{\mathrm{c,rms}}$	4.914 A	4.932 A	−0.365
$I_{\mathrm{b,rms}}$	1.729 A	1.788 A	−3.30
$I_{\mathrm{cf,rms}}$	0.864 A	0.907 A	−4.74
$I_{\mathrm{cb,rms}}$	0.864 A	0.894 A	−3.36

Based on (16), (26), (27), (41), and (44), the rms current of L_{b} (denoted as $I_{\mathrm{b,rms}}$) can be derived as

$$I_{\mathrm{b,rms}} = \sqrt{\frac{(1-k)^2}{3}\left(\frac{1}{2}\,\hat{i}^2_{\mathrm{g}} + \frac{4}{\pi}\,\hat{i}_{\mathrm{g}}\,I_{\mathrm{zvs}} + I^2_{\mathrm{zvs}}\right)}. \tag{46}$$

The current ripple $\triangle i_{\mathrm{c,x}}$ is evenly shared by $C_{\mathrm{f,p}}$ and $C_{\mathrm{f,n}}$. Therefore, the current envelopes of $C_{\mathrm{f,p/n}}$, denoted as $i^+_{\mathrm{cfx,env}}$ and $i^-_{\mathrm{cfx,env}}$, are given as in (47). Based on (16), (41), (44), and (47), the rms current of the *LCL* filter capacitors $C_{\mathrm{f,p/n}}$, denoted as $I_{\mathrm{cf,rms}}$, can be derived as in (48). By a similar reasoning, the rms current of the *LC* branch capacitors $C_{\mathrm{b,p/n}}$, denoted as $I_{\mathrm{cb,rms}}$, can be derived as in (49)

$$\begin{cases} i^+_{\mathrm{cfx,env}} = \frac{1}{4}\triangle i_{\mathrm{c,x}}(t) \\ i^-_{\mathrm{cfx,env}} = -\frac{1}{4}\triangle i_{\mathrm{c,x}}(t) \end{cases} \tag{47}$$

$$I_{\mathrm{cf,rms}} = \sqrt{\frac{k^2}{12}\left(\frac{1}{2}\,\hat{i}^2_{\mathrm{g}} + \frac{4}{\pi}\,\hat{i}_{\mathrm{g}}\,I_{\mathrm{zvs}} + I^2_{\mathrm{zvs}}\right)} \tag{48}$$

$$I_{\mathrm{cb,rms}} = \sqrt{\frac{(1-k)^2}{12}\left(\frac{1}{2}\,\hat{i}^2_{\mathrm{g}} + \frac{4}{\pi}\,\hat{i}_{\mathrm{g}}\,I_{\mathrm{zvs}} + I^2_{\mathrm{zvs}}\right)}. \tag{49}$$

The precision of the abovementioned component stress model is verified by the simulation results obtained in PLECS. The simulation model operates in inverter mode and system specifications are listed in Table I. The calculated current stress based on the aforementioned model is compared with the simulation results in Table II, showing a good accuracy of the model.

B. Analysis on the Current Ripples in the DC-Link Capacitor

As mentioned previously, the capacitor-split VG connection circuit in Fig. 1(f) has an advantage over the one depicted in Fig. 1(d) due to its ability to reduce the rms current in the dc-link capacitor, which helps further improve the efficiency. In this section, a detailed description of the current components in the dc-link capacitor for the two circuit cases is provided and a comparison of the rms current is made.

The studied VSC system is built in such a way that the dc power supply outputs a constant dc current I_{DC}, which power is converted and consumed by the ac load whereas nearly all of the high-frequency current harmonics are handled by the passive filters placed in the dc and ac terminals of the converter. The circuits in Fig. 1(d) and (f) are redrawn in Fig. 6(a) and (b), respectively. Making the following notations as in Fig. 6: $i^+_{\mathrm{s,x}}$

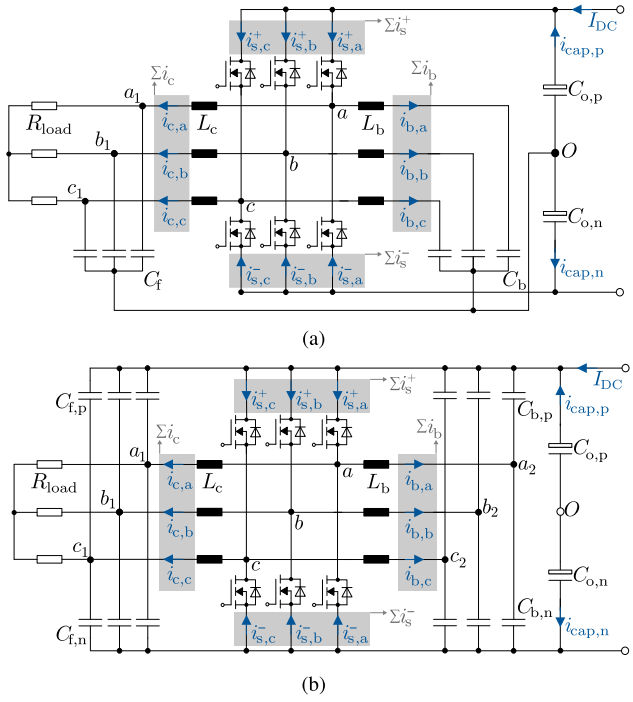


Fig. 6. Circuit diagrams for two different VG connections: (a) conventional VG connection; (b) capacitor-split VG connection.

and $i^-_{s,x}$ represent the instantaneous current of the upper and the lower switching legs for phase x, respectively; Σi^+_s, Σi^-_s, Σi_b, and Σi_c denote the sum of $i^+_{s,x}$, $i^-_{s,x}$, $i_{b,x}$, and $i_{c,x}$ for all three phases, respectively; $i_{cap,p/n}$ denotes the instantaneous current flowing through the upper/lower dc-link capacitor. Due to symmetry of the circuit, only $i_{cap,p}$ is discussed.

By Kirchhoff's current law (KCL), $i_{cap,p}$ for Fig. 6(a) is given as

$$i_{cap,p} = \Sigma i^+_s - I_{DC}$$

where I_{DC} is the constant dc current from the dc power supply. $i_{cap,p}$ for Fig. 6(b) can be deduced as

$$\begin{aligned} i_{cap,p} &= -\frac{\Sigma i_b}{2} - \frac{\Sigma i_c}{2} + \Sigma i^+_s - I_{DC} \\ &= -\frac{\Sigma i^+_s + \Sigma i^-_s}{2} + \Sigma i^+_s - I_{DC} \\ &= \frac{\Sigma i^+_s - \Sigma i^-_s}{2} - I_{DC}. \end{aligned}$$

The difference in $i_{cap,p}$ for these two cases, denoted as $\triangle i_{cap,p}$, can be calculated as

$$\triangle i_{cap,p} = \frac{\Sigma i^+_s + \Sigma i^-_s}{2} = \frac{\Sigma i_s}{2}.$$

Therefore, it is so far mathematically proven that for capacitor-split VG the current in the dc-link capacitor is free of the common-mode current components that exist for the conventional VG.

The rms value of the dc-link capacitor, denoted as $I_{cap,rms}$, is given as

$$I^2_{cap,rms} = \frac{1}{T}\int_{t_0}^{t_0+T} i^2_{cap,p}\,dt \tag{50}$$

where t_0 denotes an arbitrary start in time and T is the 50 Hz grid period. Take the difference in (50) for the two cases and denote the result as $\triangle I^2_{cap,rms}$, which is given by (51)

$$\begin{cases} \triangle I^2_{cap,rms} = \frac{1}{T}\int_{t_0}^{t_0+T}(i^2_{CM} + \underbrace{2i_{CM}\cdot(i_{DM} - I_{DC})}_{Q})\,dt \\ i_{CM} = \frac{1}{2}\left(\Sigma i^+_s + \Sigma i^-_s\right) \\ i_{DM} = \frac{1}{2}\left(\Sigma i^+_s - \Sigma i^-_s\right). \end{cases} \tag{51}$$

Note the second term in the above integral, i.e., Q, does not contribute to the final result since i_{CM} is orthogonal to both i_{DM} and I_{DC}

$$\begin{aligned} \int_{t_0}^{t_0+T}(i_{CM}\cdot i_{DM})\,dt &= \int_{t_0}^{t_0+T}\frac{\Sigma i^{+2}_s - \Sigma i^{-2}_s}{4}\,dt \\ &\equiv 0 \text{ (due to circuit symmetry)} \\ \int_{t_0}^{t_0+T}(i_{CM}\cdot I_{DC})\,dt &= I_{DC}\cdot\int_{t_0}^{t_0+T}\frac{\Sigma i^+_s - \Sigma i^-_s}{2}\,dt \\ &\equiv 0 \text{ (due to circuit symmetry).} \end{aligned}$$

Consequently, the integral in (51) can be reduced as

$$\triangle I^2_{cap,rms} = \frac{1}{T}\int_{t_0}^{t_0+T} i^2_{CM}\,dt > 0.$$

Therefore, it is so far mathematically proven that the rms current of the dc-link capacitor for the capacitor-split VG connection is definitely smaller than that for the conventional VG due to the absence of the common current components i_{CM}.

This conclusion is further verified by the simulation results in PLECS. For the conventional VG connection, the rms current value of the upper/lower dc-link capacitor is 5.17 A, whereas for the capacitor-split VG connection the value is 4.11 A. Considering a constant equivalent series resistance (ESR) value for the frequency range where most of these current harmonics lie, this would lead to over 35% reduction in losses on the dc-link capacitors.

C. Modeling of the Reverse Current Waveform

The reverse current ($i^-_{sx,env}$ during positive half mains cycle and $i^+_{sx,env}$ during negative half mains cycle) is achieved in a feed-forward manner by the time-varying switching frequency, which is calculated based on the reverse current reference $|I_{zvs}|$. With such an open-loop way of controlling, there are certain deviations in the actual reverse current waveform $i_{rev}(t)$ from the desired constant $|I_{zvs}|$. The major cause for such deviations is the fact that the effect of the flowing currents in the filter capacitor (C_f and C_b) voltages in (7), which for simplicity are usually neglected when calculating the switching frequency $f_{sw,x}(t)$. The following analysis takes this factor into consideration and a

model that accurately predicts the actual reverse current waveform is derived.

When calculating $f_{\mathrm{sw,x}}(t)$ according to (20) based on the simplified expression in (16), the actual $i_{\mathrm{rev}}(t)$ contains low-frequency components corresponding to the capacitor currents as in (52) for the positive half cycle and (53) for the negative half cycle

$$i_{\mathrm{rev}}(t) = -|I_{\mathrm{zvs}}| + i_{\mathrm{Cf,x}}(t) + i_{\mathrm{Cb,x}}(t) \tag{52}$$

$$i_{\mathrm{rev}}(t) = |I_{\mathrm{zvs}}| + i_{\mathrm{Cf,x}}(t) + i_{\mathrm{Cb,x}}(t). \tag{53}$$

Apart from the low-frequency voltage components $v_{\mathrm{C,x}}$ in (7), there are voltage ripples at switching frequency superimposed, causing the actual voltage appearing across $C_{\mathrm{f,p/n}}$ and $C_{\mathrm{b,p/n}}$ within one switching period to have a smaller average value than $v_{\mathrm{C,x}}$ during $t_{\mathrm{on,x}}$ in (17) and a larger average value during $t_{\mathrm{off,x}}$ in (18). With the other terms remaining the same in (17), an effectively smaller $v_{\mathrm{C,x}}$ would lead to a larger $\triangle i_{\mathrm{s,x}}$. Analysis on (18) would give the same conclusion, with $v_{\mathrm{C,x}}$ being effectively larger. A larger $\triangle i_{\mathrm{s,x}}$ in turn means a larger effective reverse current i_{rev}. During the positive half cycle, (17) can be rewritten into (54), where $\triangle i_{\mathrm{s,x}}[j]$ denotes the peak-to-peak current ripple at jth sampling point in time within one grid cycle, $t[j]$ denotes the start of the jth sampling point (beginning with the turn-ON moment of the upper switch), and $v_{\mathrm{cf}}(t)$ is the instantaneous voltage between the terminal x_1 and terminal O

$$\triangle i_{\mathrm{s,x}}[j] = \frac{1}{L} \cdot \left(\frac{1}{2} V_{\mathrm{dc}} \cdot t_{\mathrm{on}} - \int_{t[j]}^{t[j]+t_{\mathrm{on}}} v_{\mathrm{cf}}(\tau)\, \mathrm{d}\tau \right). \tag{54}$$

$v_{\mathrm{cf}}(t)$ is equal to the sum of the voltage ripple $\widetilde{v_{\mathrm{cf}}}(t)$ and the low-frequency voltage component $v_{\mathrm{C,x}}(t)$ defined in (7). Based on (54), the error in the peak-to-peak current ripple, denoted as $\triangle i_{\mathrm{e}}[j]$, is given by the following equation:

$$\triangle i_{\mathrm{e}}[j] = \frac{1}{L} \cdot \int_{t[j]}^{t[j]+t_{\mathrm{on}}} \widetilde{v_{\mathrm{cf}}}(\tau)\, \mathrm{d}\tau. \tag{55}$$

Considering $\widetilde{v_{\mathrm{cf}}}$ is caused by a symmetrical triangular-shaped current ripple in $C_{\mathrm{f,p/n}}$, $\triangle i_{\mathrm{e}}[j]$ can be derived as

$$\begin{cases} \triangle i_{\mathrm{e}}[j] = \frac{(A-B)\cdot \triangle i_{\mathrm{s,x}}[j]}{1-A+B} \\ A = \frac{2k\cdot t_{\mathrm{on}}}{L\cdot C_{\mathrm{f,p/n}}\cdot(t_{\mathrm{on}}+t_{\mathrm{off}})} \cdot \left(\frac{t_{\mathrm{on}}^2}{96} + \frac{t_{\mathrm{on}}\cdot t_{\mathrm{off}}}{32} + \frac{t_{\mathrm{off}}^2}{48} \right) \\ B = \frac{t_{\mathrm{on}}^2 \cdot k}{48 L \cdot C_{\mathrm{f,p/n}}}. \end{cases} \tag{56}$$

The accurate reverse current $i_{\mathrm{rev}}[j]$ during the positive half cycle is then given by (57), where $i_{\mathrm{Cf,x}}[j]$, $i_{\mathrm{Cb,x}}[j]$, and $i_{\mathrm{g,x}}[j]$ denote instantaneous currents at the jth sampling point for C_{f}, C_{b}, and grid side, respectively. The waveform during the negative half cycle is symmetrical to that during the positive half cycle

$$i_{\mathrm{rev}}[j] = -\frac{\triangle i_{\mathrm{s,x}}[j] + \triangle i_{\mathrm{e}}[j]}{2} + i_{\mathrm{Cf,x}}[j] + i_{\mathrm{Cb,x}}[j] + i_{\mathrm{g,x}}[j]. \tag{57}$$

Comparison between the model-based calculation and the simulated waveform during the positive half cycle in Fig. 7 shows a satisfactory accuracy of the model. The abovementioned derived model reveals the fact that the filter capacitors C_{f} and C_{b} have a significant impact on the actual reverse current waveform. A large capacitance value may reduce the reverse current at some times within one mains cycle, which could possibly cause a loss of ZVS at those points.

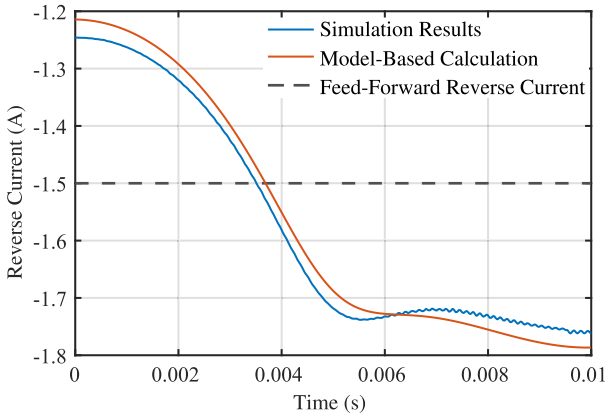


Fig. 7. Comparison of simulation results and model-based calculation for the average lower envelope of $i_{\mathrm{s,x}}$ during the positive half cycle, with simplified expressions used when calculating the switching frequency.

As mentioned before, a practical iTCM system necessitates inclusion of the switch commands deadtimes with certain length, which would have an influence on the reverse current waveform. A more accurate model should also take into account the resonance during the deadtimes [30]. Fig. 4 shows the V-Zi plot of the ZVS transition when the system works in rectifier mode. As it can be seen from the plot the correction related to the resonance is more pronounced around regions close to the zero crossing. Based on (57), the corrected waveform $i'_{\mathrm{rev}}[j]$ considering the resonance is given by (58), where $C_{\mathrm{oss,Q}}$ and C_{para} are the charge-equivalent output capacitance of the MOSFETs and the parasitic capacitance of the printed circuit board (PCB), respectively

$$\begin{cases} i'_{\mathrm{rev}}[j] = 1/Z \cdot \sqrt{(Z \cdot i_{\mathrm{rev}}[j])^2 + (\frac{1}{2} V_{\mathrm{dc}} - v_{\mathrm{C,x}}[j])^2} \\ Z = \sqrt{L/\left(2C_{\mathrm{oss,Q}} + 2C_{\mathrm{para}}\right)}. \end{cases} \tag{58}$$

D. Modeling of the System Losses

In this section, a loss breakdown between various components in the system is provided based on their theoretical loss models. Main components that are taken into account for loss generation include the main inductors (L_{g}, L_{c}, L_{b}), the active switches and the dc-link capacitors. The system specifications considered here are listed in Table I.

Two types of losses are incurred in the magnetic components: winding and core losses. Winding loss P_{wind} due to high-frequency current ripples is calculated using its equivalent ac resistance R_{AC}, where skin effect and proximity effect are taken into consideration. For the hardware setup described in Section IV, litz wire is used to build the magnetic components, which has an overall diameter d_{w} of 2.78 mm, a strand diameter d_{s} of 0.1 mm, and a strand number n_{s} of 600. The approximation for the $R_{\mathrm{AC}}(f)$ as a function of frequency is given by the

TABLE III
FITTED SWITCHING LOSS COEFFICIENTS FOR C3M0120090 J SIC MOSFET AT 600 V

Coefficient	Turn-ON loss $E_{\mathrm{SW,ON}}$	Turn-OFF loss $E_{\mathrm{SW,OFF}}$
a in μJ	23.71	23.58
b in μJ/A	8.75	−1.17
c in μJ/A^2	0.16	0.50

TABLE IV
DETAILED INDUCTOR DESIGNS

	$L_{\mathrm{g,c,b}}$
Inductance	325.5 μH
Core material	N87
Core dimension	"55/28/21"
Core shape	EE
Number of stacks	1
Number of turns N	28
Coil length l	2.2 m
Number of winding layers k	3
Window height h	33.4 mm
Airgap length l_{g}	1.27 mm
Core volume V_{c}	43900 mm^3
Coeff. α	1.7236
Coeff. β	2.7422
Coeff. k	0.07865

following equation:

$$R_{\mathrm{AC}}(f) = \frac{4l}{\sigma_{\mathrm{cu}} n_{\mathrm{s}} \pi d_{\mathrm{s}}^2}\cdot \left[2F_{\mathrm{R}}(f) + \frac{1}{\pi^2 d_{\mathrm{w}}^2} G_{\mathrm{R}}(f) n_{\mathrm{s}}^2 + 2G_{\mathrm{R}}(f) n_{\mathrm{s}}^2 \cdot \frac{N^2(4\,k^2-1)}{12\,h^2\,k^2}\right] \tag{59}$$

where σ_{cu} is the electrical conductivity of copper, l is the total length of the coil, k and h are maximum number of layers of winding in the inductor and the height of the core window, respectively, and $F_{\mathrm{R}}(f)$ and $G_{\mathrm{R}}(f)$ are frequency-related multiplying factors due to skin effect and proximity effect, respectively. l, k, and h for the hardware in this article can be found in Table IV. Detailed derivation of $F_{\mathrm{R}}(f)$ and $G_{\mathrm{R}}(f)$ can be found in [31]. Then, for a given current waveform that contains higher order harmonics, the winding loss of an inductor P_{wind} can be calculated as (60). Here, the rms value for each harmonic component in an inductor current $I_{\mathrm{RMS}}(nf_0)$ are acquired through simulation in PLECS, n representing the nth order harmonic of the grid frequency f_0

$$P_{\mathrm{wind}} = \sum_{n=1}^{\infty} R_{\mathrm{AC}}(nf_0)\cdot I_{\mathrm{RMS}}^2(nf_0). \tag{60}$$

Core losses P_{core} are modeled based on the improved generalized Steinmetz equation described in [32] and [33]. The equations used for calculation are given in (61), with the relevant parameters listed in Table IV

$$\begin{cases} P_{\mathrm{core}} = V_{\mathrm{c}} C_{\mathrm{i}} f_0 \int_0^{1/f_0} \left|\frac{\mathrm{d}B}{\mathrm{d}t}\right| (\triangle B)^{\beta-\alpha}\,\mathrm{d}t \\ C_{\mathrm{i}} = k/\left((2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha}\,\mathrm{d}\theta\right). \end{cases} \tag{61}$$

Power dissipation incurred in MOSFETs consists of switching loss that happens at every commutation and conduction loss that is caused by the on-state resistance $R_{\mathrm{ds,on}}$. Conduction losses P_{cond} are calculated according to (62), with the simulated rms current I_{RMS} in Table II

$$P_{\mathrm{cond}} = R_{\mathrm{ds,on}} \cdot I_{\mathrm{RMS}}^2. \tag{62}$$

The switching energy E_{sw} dissipated as a function of I_{sw} switched current in each commutation is given by (63) based on a fitting curve of the actual measurement. The parameters required for calculation are given in Table III [16]. Again, the numerical calculation is based on the simulated waveform in PLECS

$$E_{\mathrm{sw}}(I_{\mathrm{sw}}) = a + b|I_{\mathrm{sw}}| + c|I_{\mathrm{sw}}|^2. \tag{63}$$

For the studied iTCM system, only the turn-OFF transition contributes to the switching loss P_{sw} as in (64), whereas for traditional continuous current mode (CCM) systems both turn-ON and turn-OFF transitions incur losses as in (65), where j and k represent the jth and kth instant of switching OFF and ON, respectively

$$P_{\mathrm{sw}} = V_{\mathrm{dc}}/600 \cdot f_0 \sum_j E_{\mathrm{sw,off}}(I_{\mathrm{sw}}[j]) \tag{64}$$

$$P_{\mathrm{sw}} = V_{\mathrm{dc}}/600 \cdot f_0 \left(\sum_j E_{\mathrm{sw,off}}(I_{\mathrm{sw}}[j]) + \sum_k E_{\mathrm{sw,on}}(I_{\mathrm{sw}}[k])\right). \tag{65}$$

The loss dissipated in the dc-link capacitors P_{dc}, which is given by (66), consists of the conductive losses due to the equivalent series resistance of the selected capacitor ESR and the losses due to leakage current I_{lk}. The simulated I_{RMS} under rated load for the capacitor-split iTCM, the conventional iTCM and traditional CCM systems are 4.11 A, 5.17 A, and 3.11 A, respectively

$$P_{\mathrm{dc}} = \mathrm{ESR} \cdot I_{\mathrm{RMS}}^2 + V_{\mathrm{dc}} \cdot I_{\mathrm{lk}}. \tag{66}$$

In practice, in the aluminum electrolytic capacitor technology, the leakage current can account for a considerable proportion of the total losses, however, it is difficult to be incorporated in the loss model as its value is affected by multiple factors including temperature, storage condition, and status of degradation [34]. Therefore, in this section, only ESR losses are considered. The details of the selected aluminum electrolytic capacitor for building the hardware in Section IV as well as its parameters required for calculation are given in Table V. Note that the ESR value provided in the datasheet is measured at 120 Hz [35] and this could lead to an overestimation since the ESR of the electrolytic capacitor tends to approach its 60% to 40% at frequencies above 1 kHz [34]. This variance in ESR with frequency and the loss due to the leakage current together may

TABLE V
DETAILED CAPACITOR DESIGNS

$C_{\mathrm{f/b,p/n}}$	
Part number	B32642B0104K
Manufacture	TDK
Rated capacitance	100 nF × 7
Technology	MMKP film capacitor
ESR	7 mΩ
Quantity	7
$C_{\mathrm{o,p/n}}$	
Part number	EKXJ401ELL820MM25S
Manufacture	Chemi-Con
Rated capacitance	82 μF × 9
Technology	Aluminum electrolytic
Dissipation factor	0.24
Quantity	9

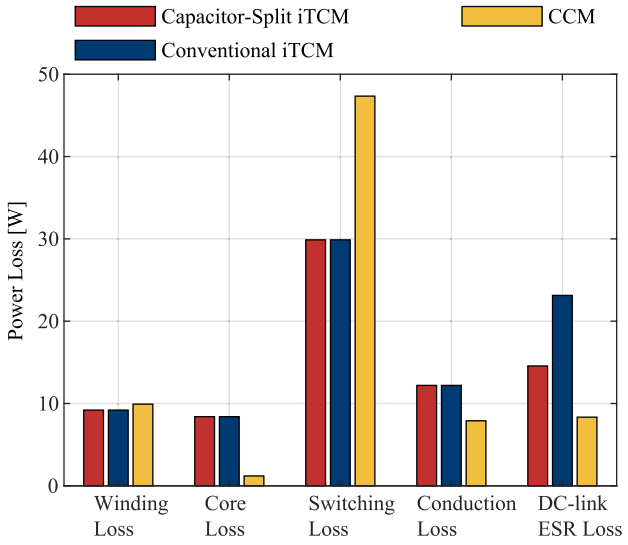


Fig. 8. Overall system loss breakdown for capacitor-split iTCM, conventional iTCM, and traditional CCM.

account for the discrepancy between the theoretical calculation and the experimental measurement.

Fig. 8 shows the overall system loss breakdown based on the abovementioned loss modeling methods. The CCM case study, as compared to the other two iTCM modulated systems, has less conduction loss in both, inductors and MOSFETs due to its smaller current ripples. However, its switching loss is much larger as compared to the other two cases since the SiC MOSFETs as used in this article feature mild turn-OFF energy but a relatively high turn-ON energy [36]. The capacitor-split iTCM and conventional iTCM have exactly the same losses in the main inductors and MOSFETs since the same current would flow through all the components in the system except for the dc-link capacitors. The difference in loss between these two systems lies only in the power dissipation in the dc-link capacitors, and an estimated difference of 9 W is given by the abovementioned analytical model.

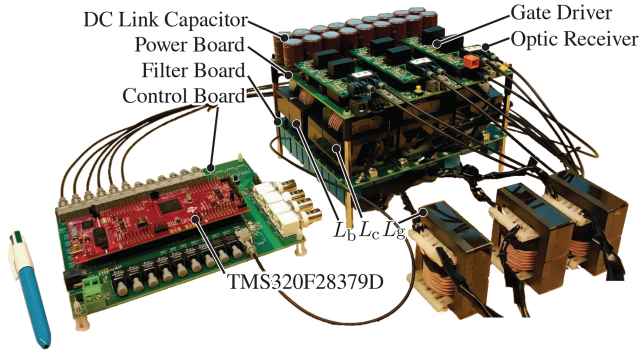


Fig. 9. Experimental setup.

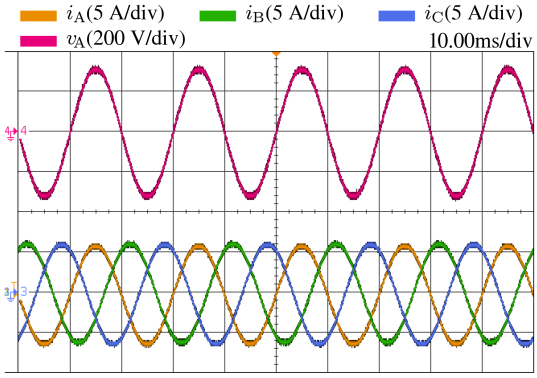
IV. EXPERIMENT VALIDATION

A 3-kW prototype as shown in Fig. 9 is built to validate the feasibility of the studied three-phase three-wire iTCM-operated VSC system and the superiority of the proposed capacitor-split VG connection shown in Fig. 2. During the experiments, the three-phase VSC is operated in inverter mode with the system specifications and key circuit parameters listed in Table I. Table IV lists the design details for the inductors. Table V lists the detailed information on the capacitors selected for constructing the filter capacitors $C_{\mathrm{f,p/n}}$ and $C_{\mathrm{b,p/n}}$, and the dc-link capacitors $C_{\mathrm{o,p/n}}$. Note that for comparison between the proposed capacitor-split and the conventional designs as in Fig. 6, $C_{\mathrm{f,p}}$ and $C_{\mathrm{f,n}}$ in Fig. 6(b) are connected in parallel to form C_{f} in Fig. 6(a) to ensure that the same amount of capacitance is employed for the two designs. This is the same case with $C_{\mathrm{b,p}}$, $C_{\mathrm{b,n}}$, and C_{b}. The voltage and current waveforms are captured by the KEYSIGHT InfiniiVision DSOX3024 A oscilloscope, and the efficiency of the converter system is measured by the YOKOGAWA WT5000 power analyzer.

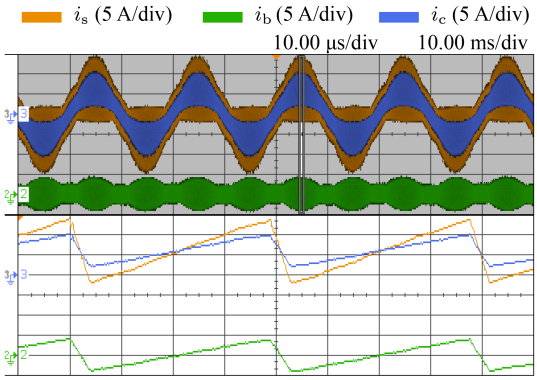
Note that the value of $|I_{\mathrm{zvs}}|$ needs to be commensurate with the deadtime so that (67) is satisfied, where t_{d} is the deadtime, C_{oss} is the output capacitance of the switch itself, which can be obtained from manufacturer's datasheet, and C_{para} is the parasitic capacitance between the drain and source in the PCB. C_{para} is especially prominent if a copper polygon is employed for the relevant nets when designing the PCB targeting the minimization of the parasitic inductance within the commutation loop. For the prototype tested in this article, t_{d} is set at 550 ns, C_{oss} is 48 pF (cf. [36]), and C_{para} is estimated at 290 pF. Therefore, $|I_{\mathrm{zvs}}|$ is chosen at 1.5 A

$$|I_{\mathrm{zvs}}| \cdot t_{\mathrm{d}} \geq 2\,(C_{\mathrm{oss}} + C_{\mathrm{para}}) \cdot V_{\mathrm{dc}}. \tag{67}$$

Fig. 10 shows the experimental results with circuit topology in Fig. 2 being used. Fig. 10(a) shows the output of three phase currents and phase-to-neutral voltage of phase A that have sinusoidal shapes. Fig. 10(b) shows the waveform of the semiconductor current i_{s}, the L_{c} current i_{c} and the *LC* branch current i_{b} for phase A. It is observed that i_{s} adopts a triangular shape and in each switching cycle reverses its polarity, where ZVS is achieved. Note that for practical reasons, the maximum switching frequency $f_{\mathrm{sw,max}}$ is clamped to 120 kHz. Therefore, it can be seen that the current envelopes of i_{s} is slightly enlarged



(a)



(b)

Fig. 10. Experimental results of the proposed three-phase three-wire VSC employing iTCM control and capacitor-split VG. (a) Three-phase output currents i_A, i_B, i_C, and phase-to-neutral voltage of phase A v_A. (b) Zoomed-in waveform of semiconductor current i_s, L_c current i_c, and LC branch current i_b for phase A.

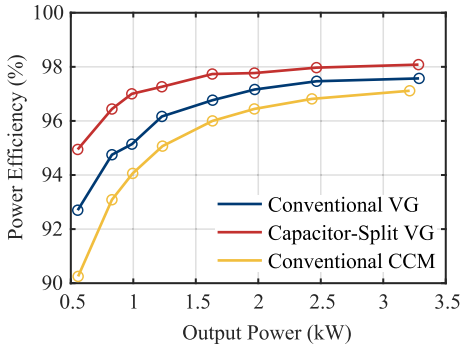


Fig. 11. Measured power conversion efficiency of the iTCM-operated three-phase three-wire VSC system at different output power with the conventional and the capacitor-split VG connections, as compared to that of the traditional CCM-operated system.

around the zero-crossing region. Moreover, it can be seen that L_c and L_b are well-designed so that the ripple in i_s is approximately equally shared by L_c and L_b.

Fig. 11 shows the comparison between the conventional VG connection [cf. Fig. 1(d)] and the capacitor-split VG connection [cf. Fig. 1(f)] on the measured power conversion efficiency of the studied system for a wide range of output power. For all the cases full-ZVS turn-ON is ensured. Moreover, in Fig. 11, the efficiency

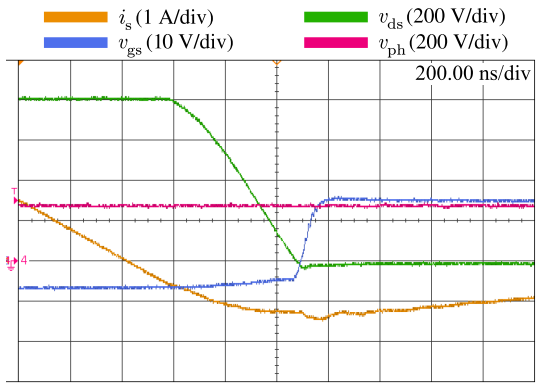
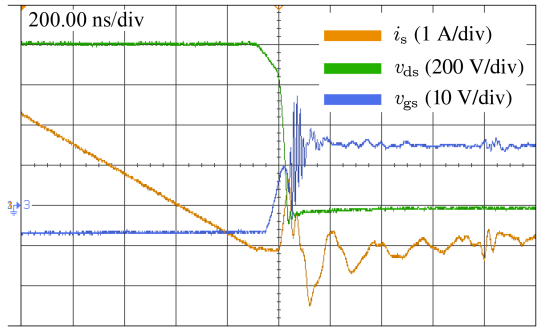
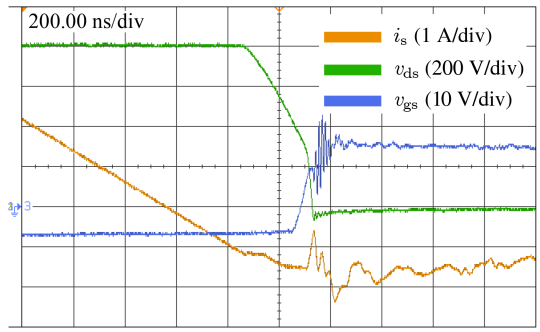


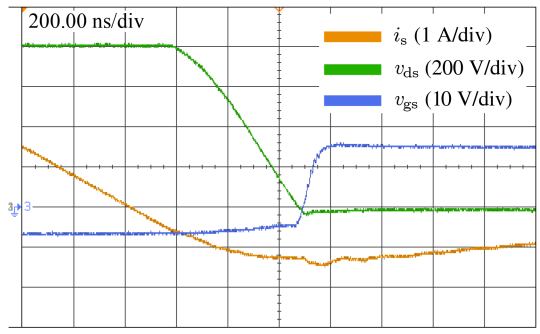
Fig. 12. Zoomed-in waveform of the gate-to-source voltage v_{gs}, the drain-to-source voltage v_{ds}, the semiconductor current i_s, and the phase voltage v_{ph} during the turn-ON process for the upper switching leg of phase A.



(a)

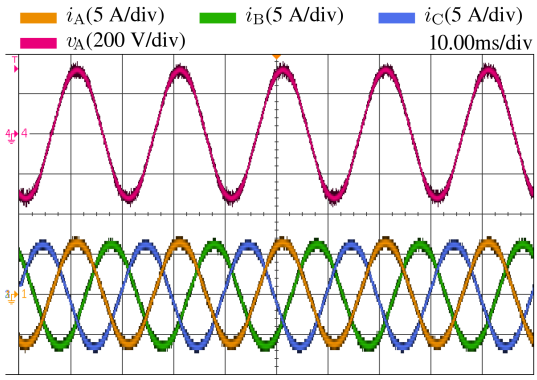


(b)

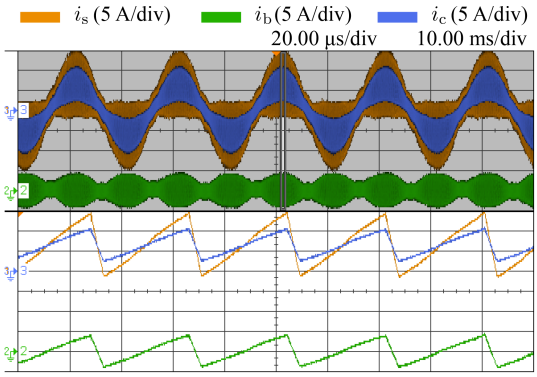


(c)

Fig. 13. Zoomed-in waveform of the gate-to-source voltage v_{gs}, the drain-to-source voltage v_{ds}, the semiconductor current i_s during the turn-ON process for the upper switching leg of phase A when different deadtimes are applied. (a) Deadtime 100 ns, hard switching. (b) Deadtime 250 ns, half-ZVS. (c) Deadtime 550 ns, full-ZVS.



(a)



(b)

Fig. 14. Experimental results of the proposed system modulated with THIPWM. (a) Three-phase output currents i_A, i_B, i_C, and phase-to-neutral voltage of phase A v_A. (b) Zoomed-in waveform of semiconductor current i_s, L_c current i_c, and *LC* branch current i_b for phase A.

of the iTCM operation is compared against the conventional CCM operation that has a fixed switching frequency equal to the average of that for the iTCM operation and does suffer hard-switching for a considerable operating range. As it can be seen, the measured efficiency for the iTCM operation with either of the two VG connections is higher than that for the CCM operation within the whole range of output power. Furthermore, a substantial improvement in the efficiency for the whole range of output power is observed with the capacitor-split VG connection as compared to the conventional VG. Specifically, the measured efficiencies at full-load are 98.082% and 97.572% for the capacitor-split one and the conventional one, respectively. The only difference between the two connections lies in the circulating path of the zero-sequence currents. The reason why the capacitor-split topology in Fig. 1(f) has an efficiency increase ranging from 0.51% to 2% is that the zero-sequence currents are confined only within the filter capacitors, switching legs and the dc rails, and therefore, the dc-link capacitor has less loss due to the resulting reduced rms current. Note that for a fairer comparison, film capacitors of lower voltage rating might be used to construct C_f and C_b for conventional iTCM system, which, due to its lower ESR, may slightly improve the efficiency for the conventional design. However, since the losses in the filter capacitors are only of several mW, in this article, this effect is neglected.

TABLE VI
SYSTEM SPECIFICATIONS FOR THIPWM MODULATION

	Symbol	Value
AC phase voltage	v_{ac}	230 V rms
Mains frequency	f_0	50 Hz
DC voltage	V_{dc}	650 V
Modulation index	M	1.0
Nominal output power	P_o	3.174 kW
Reverse current reference	$\lvert I_{zvs}\rvert$	1.5 A
Current sharing coefficient	r	1.24

Fig. 12 shows the detailed ZVS turn-ON process for the upper leg during the positive half mains cycle. It can be seen that the gate signal v_{gs} applies only after the drain-to-source voltage v_{ds} has fallen to zero, meaning the full-ZVS turn-ON is achieved. During ZVS turn-ON, i_s steadily discharges the output capacitor of the MOSFETs.

Fig. 13 shows the effect of the half-bridges deadtime in the ZVS turn-ON. Adequate deadtime is necessary to ensure full-ZVS and too short a deadtime leads to hard switching. For a deadtime of 100 ns as shown in Fig. 13(a), v_{gs} applies soon after v_{ds} just starts to fall, causing hard switching and significant ringing. For a deadtime of 250 ns in Fig. 13(b), v_{gs} applies in the middle of the output capacitor discharging, resulting in half-ZVS. For a deadtime of 550 ns in Fig. 13(c), the deadtime is long enough for v_{ds} to fall to zero and, thus, full-ZVS turn-ON is achieved.

As discussed in Section III-A, the system can also work with other modulation methods such as THIPWM and SVPWM if a higher modulation index M is desired. Fig. 14 shows the experiment results of the proposed system modulated with $\frac{1}{4}$THIPWM with the same hardware platform, the system specification listed in Table VI.

V. CONCLUSION

This work introduces a new iTCM-operated three-phase three-wire VSC with a capacitor-split VG connection. The proposed capacitor-split VG connection effectively reduces the current stress of the dc-link capacitors by confining the zero-sequence currents between the filter capacitors and the two dc rails. The iTCM facilitates zero-voltage turn-ON of the switches for the entire grid cycle, redirecting the high-frequency TCM currents to the internal *LC* branch circuits rather than the ac side. Detailed working principle of iTCM on the three-phase VSC, and the design guideline for the *LC* branch and *LCL* filters are explained in detail. The mathematical models for the main components stresses and the reverse current waveform are built to facilitate component selection. Finally, a 3-kW prototype is demonstrated and tested to verify the feasibility and efficiency advantages of the system studied. It is shown by the experimental results that the iTCM ensures ZVS in all three phases and the capacitor-split VG connection helps to reduce the rms current through the dc-link capacitors, achieving the highest efficiency between the benchmarked systems.

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