An Energy-Efficient High-Speed Full-Duplex IR-UWB Transceiver For Joint Raddar and Communication (RadCom)

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An Energy-Efficient High-Speed Full-Duplex IR-UWB Transceiver For Joint Radar and Communication (RadCom)

Master's Thesis

To fulfill the requirements for the degree of
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Abstract

In recent years, short-range reliable wireless system with high data rate and low power consumption has drawn sufficient attention and is in great demand in various applications. For biomedical implantable applications such as neural sensing and Brain-computer Interfaces (BCIs), due to the increasing number of sensing channels and elements, not only the precision of the biomedical analysis is increased, but also a wireless system with higher data rate is required. Besides the high data throughput, as an implanted device, settling within a human or animal body requires high reliability and low power consumption. Such a wireless system finds its position in smart wearable devices as well. With a higher data rate and small form factor, more functionalities can be adapted to those smart wearable devices. The energy-efficient characteristic also allows a longer working time and battery life. Similarly, the above-mentioned wireless system is a prime candidate for multi-media applications like virtual reality (VR). A higher data rate means more visual, audio, and sensing data can be transmitted simultaneously, which allows for more advanced functions and a better user experience. Furthermore, this high data rate, low-power wireless system can be also adopted at advanced control system.

Among all possible technologies, Impulse Radio Ultra-Wide-Band (IR-UWB) technology is a promising solution for this short-range wireless system. Within this master thesis project, a transceiver exploiting IR-UWB technology is proposed and implemented as a solution for the above-mentioned short-range, high data-rate, low-power reliable wireless system. The transmitter is from Yu Huang's hybrid modulation transmitter. A fifth-order wide-band low-power GM-C low-pass filter is implemented with novel closed-loop GM-C BiQuad architecture in the receiver. Besides, the adoption of Electrical Balanced Duplexer (EBD) and Digital Self-interference Cancellation (DSIC) promises strong isolation between transmitter and receiver. Thus, this transceiver is also full-duplex (FD) and achieves simultaneous radar and communication (RadCom). With RadCom, this transceiver accomplishes a higher integration level, higher spectral efficiency, and lower cost. Besides, it enables a new range of applications since it can serve as a radar and communication device simultaneously. With the ability of ranging, object detection, and tracking, this transceiver is also an excellent solution for automotive sensing and human sensing: social distancing, child presence detection, non-contact vital sign detection, etc.

Designed and fabricated in TSMC 28 nm CMOS process, this chip has a form factor of only 0.155 mm^2. The achieved maximum data rate is 1.66 Gbps, while the transceiver DC power is within 20 mW.

1 Introduction

Thanks to the fast development of electrical and electronic engineering, plenty of sensors with higher precision for various applications are implemented. Besides, finer data processors are designed and fabricated. These lead to the rapid growth of data throughput between devices in our daily routine. The data volume created, captured, copied, and consumed worldwide is increasing exponentially and will be over 175 zettabytes by 2025 [1].
High data volume brings challenges to data transmission, where a high data-rate communication link is the blood vessel for such a massive amount of data. Within a highly integrated system, numerous high-speed solutions are proposed, like cable-package attachment, which enables hundreds of Gbps chip wire-line communication [2], [3]. Wire-line communication between different systems is also promising owing to the satisfactory characteristic of communication wires such as fiber optics. However, wireless communication has always been preferred over the wire-line link since its birth. The conductor-less characteristic makes life easier for both designers and users. Wireless communication makes the whole data transmission link less lengthy and tidy and enables many new applications that are impossible for conventional wire-line counterparts. However, the most troublesome drawback of wireless communication is the limited data rate. Since the data is transmitted in the air, the attenuation is very significant, which limits the transmission range. Besides, various regulations are defined to suppress the power of signal emission, which limits the data rate as well. To enhance data rate, frequency duplex strategies like frequency hopping, orthogonal frequency-division multiplexing (OFDM) and parallel data transmission are proposed [4]. However, these solutions are complex and power hungry.
Compared with other solutions, the IR-UWB technology-based communication system is more attractive owing to its characteristics like high data rate, low power, short range communication in personal area network (PAN). It is proved to be a prime candidate for applications like BCIs, smart wearable devices, and VR [5], [6]. In this thesis, a transceiver using this technology with RadCom and full-duplex functions is proposed.
A detailed background of this technology is introduced in this chapter. In subsection 1.1 the basic principles of IR-UWB techniques are introduced, while in 1.2 the idea of RadCom is described. Subsection 1.3 presents the system objectives and specifications of this IR-UWB transceiver.

1.1 IR-UWB

1.1.1 Ultra-Wide-Band Technology

Ultra-Wide-Band (UWB) technology has recently drawn plenty of attention due to its reliable high data rate and fine-ranging resolution features. The definition of UWB signal from Defence Advanced Research Project Agency (DARPA) is one that has a fractional bandwidth BW_{frac} larger than 25%, where the fractional bandwidth is the ratio between signal -10 dB level bandwidth and center frequency as shown in Eq. 1:

$$BW_{frac} = \frac{BW_{-10dB}}{f_c} = \frac{2(f_H - f_L)}{f_H + f_L} \tag{1}$$

where f_c can be defined as:

$$f_c = \frac{(f_H + f_L)}{2} \tag{2}$$

While in communication perspective, the definition from Federal Communications Commission (FCC) is commonly adopted: UWB device uses a signal with a fractional bandwidth BW_{frac} larger than 20% or with an absolute bandwidth BW_{-10dB} larger than 500 MHz, as shown in Fig. 1.

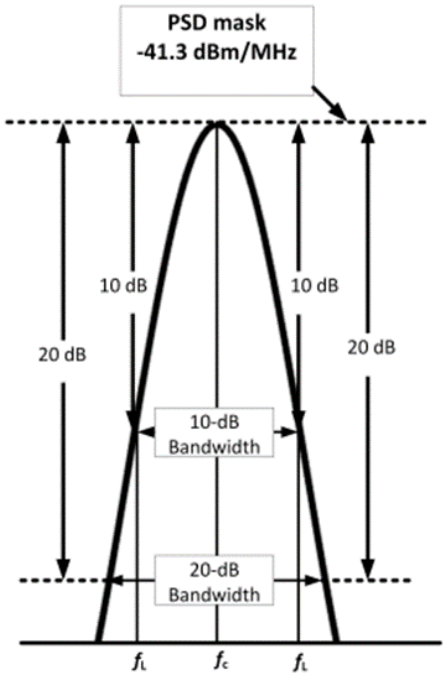


Figure 1: Definition of UWB signal [7]

According to Fig. 1, unlike a standard narrow-band signal, the bandwidth of the UWB signal is larger than 500 MHz, which results in an impulse in the time domain with a pulse duration of less than 2 ns. Furthermore, 500 MHz bandwidth is a relatively small value in the UWB scenario, which means that commonly the pulse duration would be sub-nanosecond level. The available frequency band for UWB application is very wide: 3.1-10.6 GHz. However, a wide bandwidth and spread available frequency band bring challenges to emission power control and interference control to other adjacent narrow-band signals. Few regulations are published to handle this problem. The maximum mean effective isotropic radiated power (EIRP) density of UWB signal is set to be -41.3 dBm/MHz by FCC in 2002 [8]. In Europe, the Electronic Communications Committee (ECC, a committee of the Conference of Postal and Telecommunications Administrations (CEPT) in Europe) stipulated the frequency band for unlicensed use of UWB communications and radar systems, which is even more strict than the one from FCC [9]. The power masks set by those two regulatory bodies are shown in Fig 2.
With those strict power density masks, the maximum transmitted power from the transmitter output antenna is limited, which will consequently limit the communication range. Thus, the link budget must be carefully calculated to obey this power mask and meanwhile maximize the possible communication distance.

1.1.2 Impulse Radio Ultra-Wide-Band

UWB technology consists of two main types: single-band UWB and multi-band UWB or multi-carrier UWB. For multi-band UWB (MB-UWB), the wide bandwidth is composed of several sub bands. One of the most famous multi-band scheme is combining frequency hopping and OFDM,

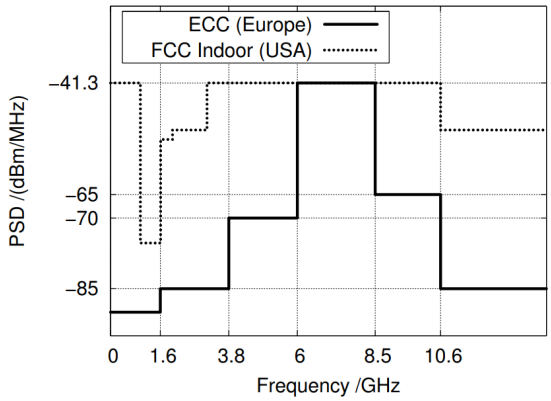


Figure 2: European UWB mask & FCC mask [8]

called multi-band OFDM (MB-OFDM), where adaptive frequency hopping is used to deduce the interference. Such MB-UWB technology can obtain a bandwidth of 528 MHz, and the maximum data rate can reach up to 480 Mbps [10]. However, adaptive frequency hopping and OFDM require a complex system and consume a lot of power. Thus, MB-UWB is not preferred in this thesis.
The main candidates for single-band UWB are impulse radio UWB (IR-UWB) and direct sequence UWB (DS-UWB). Unlike MB-UWB, the wide bandwidth of DS-UWB is obtained by exploiting high-rate consecutive chips. Compared with DS-UWB, IR-UWB technology has been proven to have superior performance in realistic systems [11]. Thus, it is adopted in this thesis project.
As stated in its name, a short-duration baseband pulse with a low duty cycle is used to generate the IR-UWB signal. The spectrum characteristic is determined solely by the pulse duration and shape. Thus, with an appropriate pulse shape and length set, the FCC or ECC mask can be fulfilled. To have a wide bandwidth, the pulse duration should be relatively small, which normally is in nanosecond or sub-nanosecond levels. No sinusoidal carrier is required to up-convert the signal because the pulses are already in the radio frequency spectrum [12]. This makes IR-UWB a good candidate for carrier-less transmission implementation. Besides the reduced complexity brought by its carrier-less characteristic, the pulse-based scheme also allows reliable high-speed communication. While one pulse can be usually considered as one symbol, the symbol rate can be very high since the pulse period is already minimal and the symbol period could be as small as the pulse period [5]. Furthermore, since the duty cycle is low, within one period, the inactive time is longer than the active time, which is usually few nanoseconds. The radiated signal hence obtains a high peak to average power ratio (PAPR) to obey the power mask. Also, the DC power level of the transmitter can be released. In conclusion, all those attributes of IR-UWB technology make it a promising solution for high data rate, low power, and low-cost short-range communication.

1.2 RadCom

Since FCC regulated the band and power mask of UWB signal in 2002 [8], plenty of business interest and research efforts have been put on this technology. However, UWB has already been a popular option for ranging and detection for decades due to its competitive characteristics. It is originally used for military ranging, object detection, and tracking implementation in radar. Such UWB radar uses the high bandwidth feature to achieve fine ranging and imaging [13]. Table 1 shows the frequency bands used in radar applications. To further exploit this advantage of UWB technology, the simultaneous radar and communication (RadCom) scheme is considered in this thesis.

Table 1: *Radar Frequency Bands*

Radar Band	Frequency (GHz)	Wavelength (cm)
Millimeter	400-100	0.75-0.30
Ka*	26.5-40	1.1-0.75
K	18-26.5	1.7-1.1
Ku*	12.5-18	2.4-1.7
X	8-12.5	3.75-2.4
C	4-8	7.5-3.75
S	2-4	15-7.5
L	1-2	30-15
UHF	0.3-1	100-30

*Subscriptions 'a' is for 'above' and 'u' is for 'under'.

The simultaneous radar and communication (RadCom), also called joint radar communication (JRC), aims to develop devices and algorithms that can achieve this dual functionality. The inherent tool for both radar and wireless communication is radio waves. Thus, despite the very different design considerations and parametrization, it is desired and feasible to merge them into one device where the hardware like baseband (BB) and analog front-end (AF) as well as antennas can be shared to reduce the cost and increase the integration level.

The motivations, as well as use cases of this RadCom system are mainly those two fields: Vehicle-to-Everything (V2X) and Internet of Things (IoT) applications [14].

V2X application is of vital importance in the smart or advanced automotive field. And the integration of communication and ranging has already been proposed in the last century [15]. Furthermore, with the development of microelectronics and power electronics, the automotive nowadays is more electrically intensive, and the driving has become more autonomous. To achieve more and more advanced and sophisticated functionalities, vehicles are equipped with an increasing number of sensors with high complexity, which will, in turn, generate a massive amount of data to be processed. It is predicted that the data generated per single trip of an automated driving vehicle could reach up to level of terabytes [14]. Thus, conventional V2X communication and sensing are not adequate anymore since a sufficiently low latency and very high reliability is a must for the smart automotive, which also brings about the need for this novel RadCom system. RadCom finds its position in many use cases, especially safe-related ones in V2X as shown in Fig . 3: forward collision warning, do not pass warning, blind intersection warning, vulnerable road user discovery, etc. [14].

With RadCom, both the frequency band as well as bandwidth are increased for finer sensing resolution and higher data rate in communication. Furthermore, collaborative radar imaging is enabled to increase the imaging accuracy besides the reduced cost and power consumption with the adoption of RadCom system [16]. However, since in V2X, low latency and high reliability are of top priority, and it requires middle-range communication, it is not the target application scenario of this project.

Besides V2X, RadCom occupies the core position in future IoT as well. The motivation for implementing such a dual functionality system in IoT is more natural and intuitive than the V2X application. Despite various use cases in IoT, they can be categorized into two generalized parts:

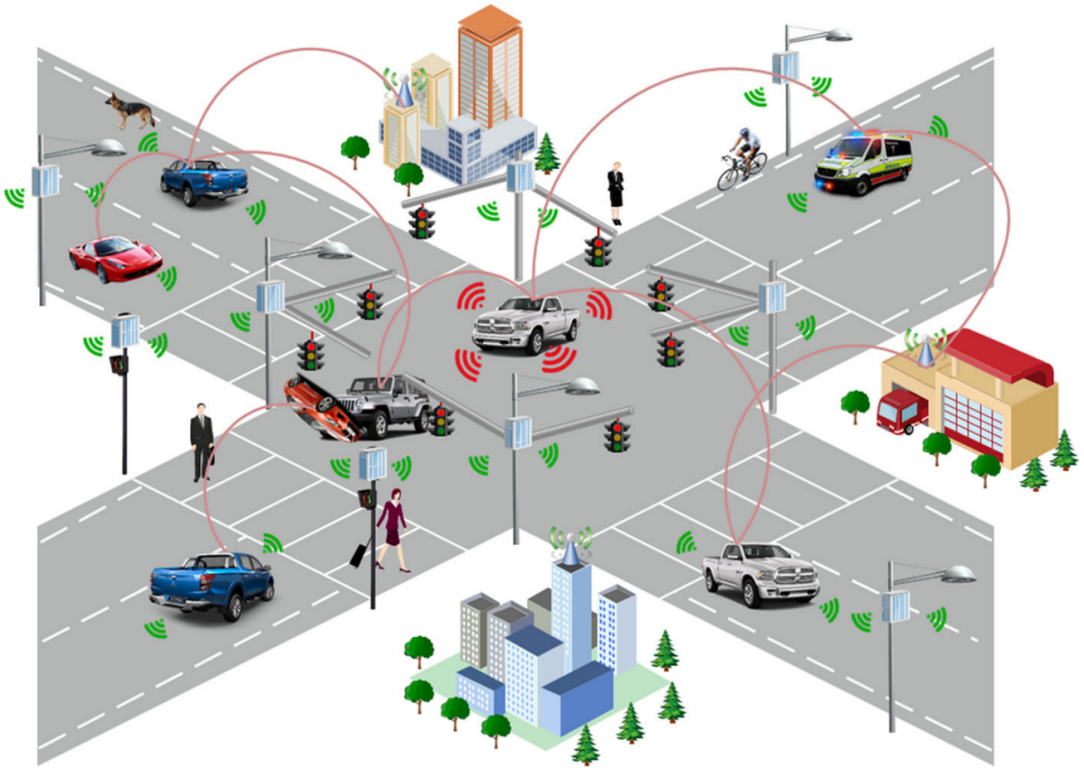


Figure 3: Use cases of RadCom in V2X application [14]

1. *Communication component*: Wired and wireless communication link

2. *Sensing component*: Sensors that collect data

Although the sensors used in IoT nowadays are very heterogeneous, a significant portion of them are radar-related and work based on the reflectometry principle [14]. Thus, it can be concluded that the modern IoT consists of two principle parts: communication components and radar components. Then, it is natural and intuitive to merge these two parts and implement a device with RadCom technology to reduce cost, power and increase integration level as well as spectrum efficiency. Furthermore, sharing hardware would generate less electronic garbage and is environmentally friendly. The energy-efficient full-duplex transceiver proposed in this paper with low-cost, high data rate, and RadCom functionality also found its possible application in IoT. However, since radar and wireless communication have been developed separately for decades, their design considerations, as well as their design process, are different. Thus, there are still challenges to implement a compatible RadCom system: miniaturization of radar system; radio wave shape/frequency flexibility etc. [14].
One of the commonly used technology to implement the RadCom system is OFDM. Several papers proposed RadCom system exploiting OFDM-based radar technology [17]. In comparison to a single carrier (SC) system, a multi-carrier counterpart obtains a wider bandwidth and more degree of freedom for waveform synthesis. With increased synthesized bandwidth, both the data rate and range resolution are improved with the flexibility to adapt the channel and bandwidth according to communication requirements. However, OFDM technology requires complex implementation and consumes high power. There are other implementations, but the problem still exists [18], [19]. Here in this thesis, the IR-UWB technology is used instead of OFDM. High bandwidth is achieved with a single

carrier system. Thus, the radar can still benefit from fine resolution, while the complex frequency multiplexing is eliminated, which increased the power efficiency dramatically.

1.3 System Objectives and Specifications

Within this master thesis project, a transceiver exploiting IR-UWB technology is proposed and implemented as a solution for the above-mentioned short-range, high data-rate, low-power reliable wireless system. With the adoption of EBD and DSIC, full-duplex and RadCom are also enabled in this transceiver. Since the maximum data rate of the transmitter in [5] is 1.66 Gbps, the receiver should be designed to be capable of resolving the transmitted data. So the targeted data rate would be 1.66 Gbps. The transceiver works in a higher UWB band: 6 to 8 GHz in compliance with the FCC power mask, and the total DC power of this transceiver shall not exceed 20 mW. The targeted communication range is sub-meter level (0.5 m in the air). All the above-mentioned specifications are concluded in table 2.

Table 2: *Design specifications for communication part*

Technology	**TSMC 28 nm**
Supply voltage (V)	**0.9**
Maximum Data Rate (Gbps)	**1.66**
DC Power Consumption (mW)	**20**
Frequency Range (GHz)	**6-8.5**
Communication Range (m)	**0.5**

Furthermore, when this transceiver works as a radar, the targeted specifications are show in the table 3.

Table 3: *Design specifications for radar part*

DSIC Isolation (dB)	**30**
Range Resolution (m)	**0.3**
Unambiguous Range (m)	**37.3**
Velocity Resolution (m/s)	**0.24**
Maximum Velocity (m/s)	**15.1**
Range Accuracy (cm)	**1**

In the receiver design, a fifth-order low-power wideband low-pass filter is implemented with a novel closed-loop GM-C BiQuad architecture. Besides, both passive and active self-interference cancellation methods are adopted in this transceiver to cope with the spillover signal and enable full-deplex and RadCom. The DSIC is redesigned and modified based on the all-digital spillover cancellation method proposed in Sander Hijmans' master thesis [20].

The content of this thesis paper is arranged as follows: Chapter 2 discusses the commonly used IR-UWB TRX and the novel structure is proposed. In Chapter 3, the detailed design of the above-mentioned low-pass filter is described. In Chapter 4, the design of DSIC is presented. Then the system-level implementation of this chip is introduced in Chapter 5. Finally, conclusions are drawn in Chapter 6.

2 IR-UWB Transceiver

Since FCC authorized the unlicensed use of UWB signal in the frequency band of 3.1 to 10.6 GHz in 2002 [8], it has drawn significant attention from both academia and industry. Plenty of wireless systems and devices based on UWB technology have been proposed for various applications in the past decades.
As introduced in Chapter 1, the most commonly used method for achieving such a system is IR-UWB, which is also adopted in this thesis. IR-UWB signal is a repetitive short pulse with a low duty cycle. In the frequency domain, the IR-UWB signal sits in a high-frequency band (3.1-10.6 GHz) with a very wide bandwidth in comparison with a narrowband signal. The signal frequency spectrum can be manipulated by adjusting the pulse duration as well as the pulse shape to fulfill the FCC mask and adapt to different applications.
Within this chapter, the high-level architecture of this transceiver is presented. In Section 2.1, the IR-UWB transmitter structure is described, while in Section 2.2, the receiver architecture is introduced. Finally, the self-interference cancellation (SIC) scheme is discussed in Section 2.3.

2.1 IR-UWB Transmitter

In many proposals of IR-UWB transceiver, typically the IR-UWB pulse is directly generated by a pulse generator (PG) [21]. Since this pulse is already in the radio frequency band, no further up-conversion is needed like a carrier-based system [22]. Instead of having a local oscillator, baseband data signal, and mixer, an IR-UWB transceiver copes with this issue simply with the pulse generator. Thus, the complexity, as well as power consumption, can be significantly decreased. Fig .4 compares a typical narrowband transceiver architecture and a commonly used IR-UWB transceiver architecture mentioned above.

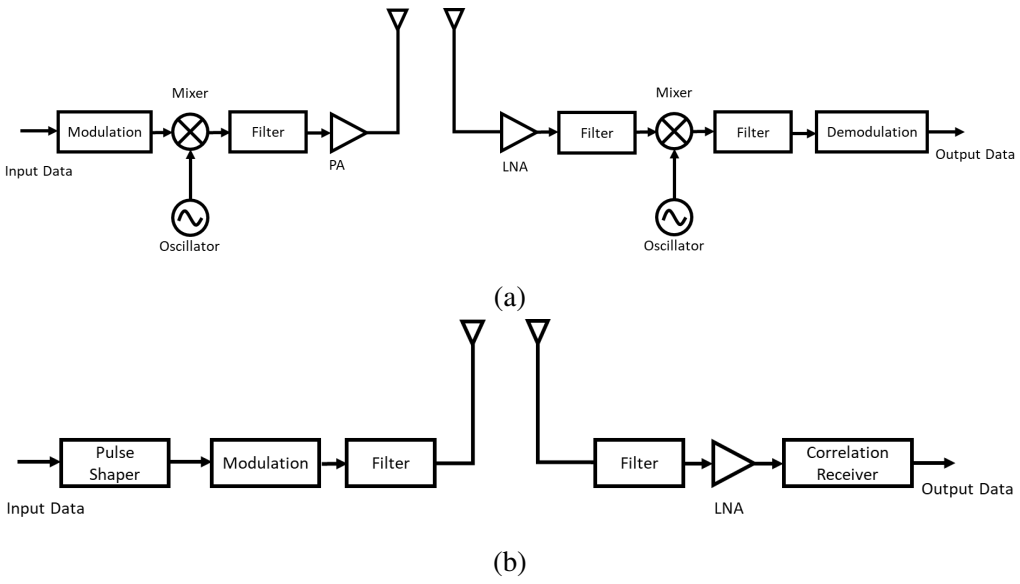


Figure 4: (a) Typical narrowband architecture; (b) Conventional IR-UWB architecture.

However, despite the benefits of its carrier-less characteristic, it also limits the modulation scheme available for this system. A plain UWB pulse contains no further information in communication. Further processing and modulation schemes must be carried out on the UWB pulse to transmit data. For a typical carrier-based signal, the phase, amplitude as well as the frequency of the carrier wave

can be used to encode the information. This arrangement is unfortunately not valid for IR-UWB pulse due to the carrier-less nature. Since the pulse is directly generated, it can be shaped on a time basis and shape basis. Thanks to its low duty cycle and short pulse duration, the long sleep time between pulses can be used to encode data. A unique modulation called pulse position modulation (PPM) is implemented and used in many papers [22], [23], [24]. Besides, the shape of the pulse can be modulated as well, depending on how the UWB pulse is exactly generated. Commonly used shape-based modulation schemes are pulse amplitude modulation (PAM), on-off keying (OOK), and binary phase-shift keying (BPSK) [5], [21], [22].

The data rate of the IR-UWB-based system can be relatively high since each short pulse is typically one symbol. Thus, the symbol rate is equal to the pulse repetition frequency (PRF), and the data rate is directly proportional to the PRF and the number of modulation bits [24]. To increase the data rate, either PRF or the modulation bits need to be increased. Unfortunately, PRF cannot be increased freely due to the average power mask of -41.3 dBm/MHz. To maintain low average power, a higher PRF means a lower pulse amplitude, leading to a sacrifice of communication range. A higher PRF will also increase the inter-symbol interference between pulses since the spacing between them is shrunk. Thus, to increase data rate, implementing an advanced modulation scheme is more viable. On the other hand, directly increasing PPM bits requires a very precise time detection. Some novel schemes are proposed to relax this hard requirement but the increment in data rate is still limited [23], [24]. Implementing an orthogonal frequency division modulation (OFDM) can raise the data rate but requires a much more complex architecture, which breaks the advantages of IR-UWB: low complexity and low power consumption. Thus, in [5], a novel transmitter architecture with hybrid modulation is designed and verified. This transmitter implemented by M.Song and Y.Huang is also used in the transceiver in this thesis project.

Besides the time-based and shape-based modulation mentioned above, this transmitter also adopts multiple phase-shift keying (MPSK). Finally, a hybrid modulation scheme featuring 4PAM, 4PPM, and 8PSK, is used to facilitate the data rate. With the PRF of 238 MHz, the maximum data rate can be calculated as follows:

$$Data\ rate = PRF \times Bits\ per\ symbol = 0.238 \times (2+2+3) = 1.66\ Gbps \tag{3}$$

Since the hybrid modulation scheme is used, the conventional edge-combining transmitter architecture introduced before, which uses the pulse generator, is not suited anymore. The generated pulse from PG must be set to the desired operational frequency directly. So it would be very difficult to do the PSK and PPM modulation simultaneously. Thus, a novel transmitter structure combining the ideas of conventional UWB transmitter and traditional up-conversion transmitter is proposed and shown in Fig. 5.

Instead of generating the pulse directly from PG, the IR-UWB signal is generated in several steps, and the idea of up-conversion is used in this transmitter. Firstly, a sinusoidal carrier signal with frequency at the center frequency of the IR-UWB spectrum is generated from the digitally controlled oscillator (DCO). This DCO can output carrier signal with 8 different phases to a multiplexer. Thus, the 8PSK modulation is directly accomplished by this DCO and multiplexer. Then, to convert this sinusoidal wave to an IR-UWB signal, an asynchronous pulse shaper (PS) and a digital power amplifier (DPA) are used. The PS and DPA utilize a staircase envelope on top of the carrier signal where the PAM determines the amplitude of the envelope, and the time-domain position of the envelope is decided by the PPM. Finally, the IR-UWB pulse is synthesized with 8PSK, PAM, and PPM information encoded. The PPM is achieved by a digital controlled delay generator while the PAM is realized by the DPA. This hybrid modulation contains in total 7 bits in one symbol, which is one UWB pulse. And the maximum data rate achieved by this transmitter can go up to 1.66 GHz, as calculated in equation 3.

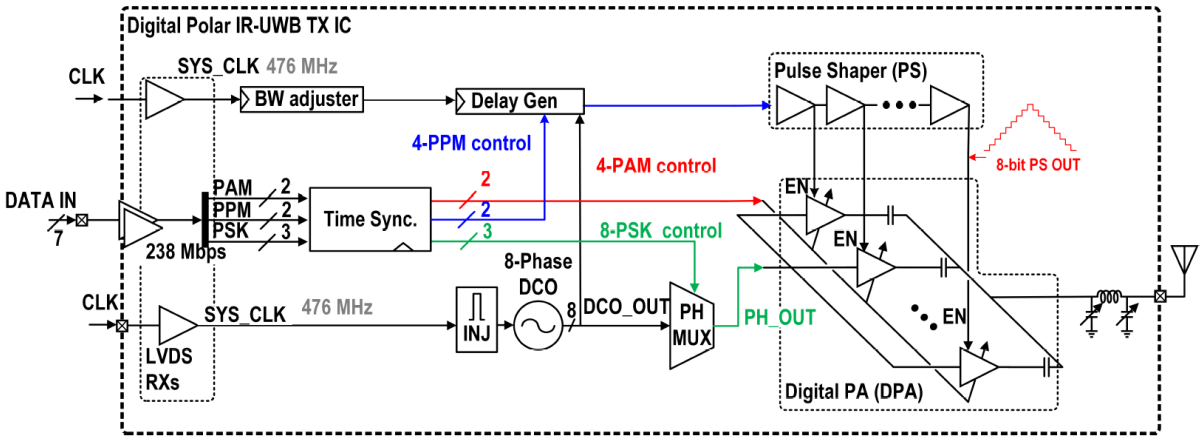


Figure 5: Transmitter architecture [5]

2.2 IR-UWB Receiver

Since the IR-UWB pulse is commonly generated directly with PG, it is a carrier-less communication system. And due to its carrier-less nature, conventional receiver architecture using a mixer to down-convert the RF signal and get the baseband data is not feasible here without a local carrier signal. As mentioned in the above chapter, the primary modulation methods are OOK, PAM, PPM, and BPSK. Thus, the IR-UWB receiver structure should be mixer-free and capable of demodulating the data encoded by the above-mentioned modulation schemes. Various UWB receiver architectures have been proposed during the past decades, and most of them can be categorized into two major types: coherent UWB receiver and non-coherent UWB receiver [25].

A coherent receiver structure requires synchronization between its transmitter and receiver, in which the receiver uses the synchronized signal from the transmitter to reconstruct the baseband data. Without a local oscillator, the synchronized transmitted signal is directly used in the coherent UWB receiver instead of a carrier signal. The RAKE receiver structure has been widely adopted as the coherent IR-UWB receiver. A RAKE receiver could effectively detect and combine the dispersed energy in multi-path components (MPCs) by assigning detecting fingers to each of them, where each finger is a matched filter, i.e. correlator. The general block diagram is shown in Fig. 6.

However, since the UWB pulse duration is very short, the amount of MPCs is much larger than other technology like CDMA [22]. Furthermore, a coherent RAKE receiver requires the exact information of each multipath channel. In other word, an accurate channel estimation, as well as fine synchronization are needed for each channel to extract multipath energy from MPCs. This configuration pushes the system complexity and power consumption to an unacceptable level. To cope with this issue and make coherent IR-UWB RAKE receiver viable, several advanced structures based on the conventional RAKE receiver are proposed like All RAKE (ARAKE), Selective RAKE (SRAKE) and Partial Combining RAKE (PRAKE) [25]. An ARAKE receiver combines all available multipath just like a basic RAKE receiver. PRAKE only combines the first M arriving multipath. SRAKE picks up the strongest few MPCs and combines them. Instead of combining all the MPCs, those structures select a limited amount of them and obtain a balance between collected energy and system complexity.

Despite reduced complexity, a coherent RAKE receiver is still a high-cost option. The complexity problem can be greatly mitigated by using a non-coherent receiver structure, where no channel estimation is needed. With a much-reduced complexity in comparison with a coherent one, a non-coherent

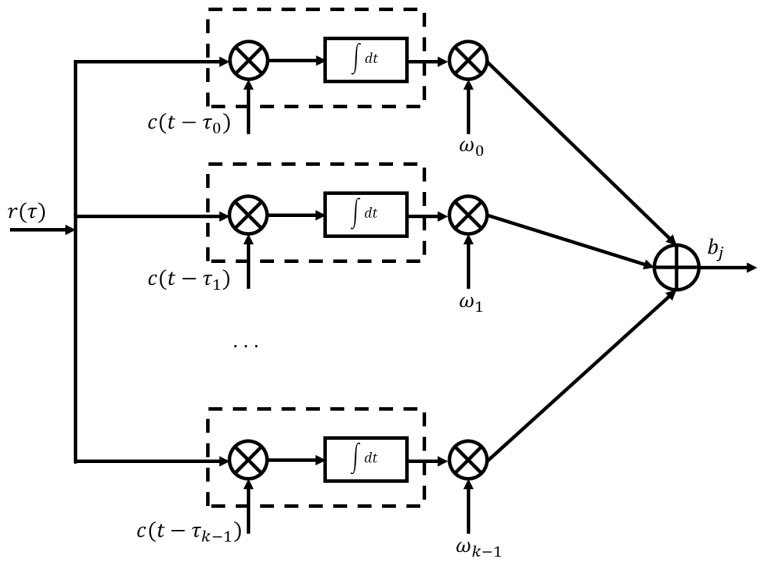


Figure 6: Coherent RAKE receiver architecture [25]

receiver has less cost and lower power consumption while still obtaining a good amount of energy with multi-path propagation. However, the price is higher noise level and poor Bit Error Rate (BER) performance. The commonly used non-coherent structures are auto-correlation (AC) receiver and energy detection (ED) receiver [25]. Instead of correlating with transmitted signal in RAKE receiver, an AC receiver correlates with a delayed version of itself. Then the correlation result is integrated and compared to obtain the baseband data. Some papers have already implemented IR-UWB receivers based on this idea [26]. Note that in the absence of a transmitted signal, the UWB signal itself should be a reference in the receiver. Thus, AC structure can be further classified as transmitted reference (TR) receiver, average transmitted reference (ATR), recursive transmitted reference (RTR) receiver, code-shifted reference (CSR) receiver, frequency-shifted reference (FSR) receiver, etc. [12], [25], [27]. An ED receiver consists of signal squaring, integration, and comparing. Due to its energy-detection characteristic, it is well suited for modulation scheme OOK, and there are also plenty of implementations of UWB receivers based on ED structure [28], [29].

Besides, some other special non-coherent UWB receivers are proposed for dedicated applications. In [24], a novel modulation scheme is implemented to facilitate a high data rate: digitalized multiple position modulation (D-MPPM). The modulation schematic looks similar to the TR receiver, where two pulses are used in one symbol. However, in the TR scheme, one symbol is used as a reference symbol and will be correlated with the second data pulse. In D-MPPM, the first pulse is used as a sync pulse, and the second pulse is the data pulse. The information is encoded in the time interval between those two pulses. Instead of correlation, the data is recovered by applying a time-to-digital converter (TDC) to measure this time interval. Thus, a dedicated receiver structure is implemented where the front-end is like an ED receiver. After obtaining the envelope of the received signal, an edge detector followed by 6-bit TDC is used to dissolve the PPM signal. Although the data rate is increased and the non-coherent structure is retained, the usage of a digital-to-time converter (DTC) in the transmitter and TDC in the receiver increased the system complexity as well. Furthermore, to have a high number of bits per symbol, the PPM time step is very small, which requires a very precise and fine DTC and TDC to obtain good BER performance. The clock used for DTC and TDC should also be very fast. Thus, it is not a preferred option for the general UWB signal.

In this thesis project, as introduced in section 2.1, the high-speed IR-UWB transmitter with a hybrid modulation scheme is adopted. To build up a UWB receiver capable of detecting and dissolving the signal from this transmitter, all the above-mentioned coherent RAKE structures and non-coherent structures are no longer feasible anymore. Besides the common PPM and PAM, the hybrid modulation scheme contains multi-phase modulation 8PSK. Unlike BPSK, which can be demodulated using correlation and integration, a multi-phase modulation requires a differential I/Q structure to decode the phase information. With above mentioned AC or ED non-coherent structure, the phase information will be ruined and buried. The inter-symbol interference (ISI) will become severe with increased PRF. The coherent RAKE structure is not available for this situation as well. Unlike conventional coherent structure, which mixes the received signal with the synchronized local carrier wave, the RAKE receiver directly correlate the received signal with (delayed) transmitted signal, which in principle is still an auto-correlation. This operation will annihilate the phase information as well. Thus, a novel high-speed IR-UWB receiver structure is proposed, as shown in Fig. 7.

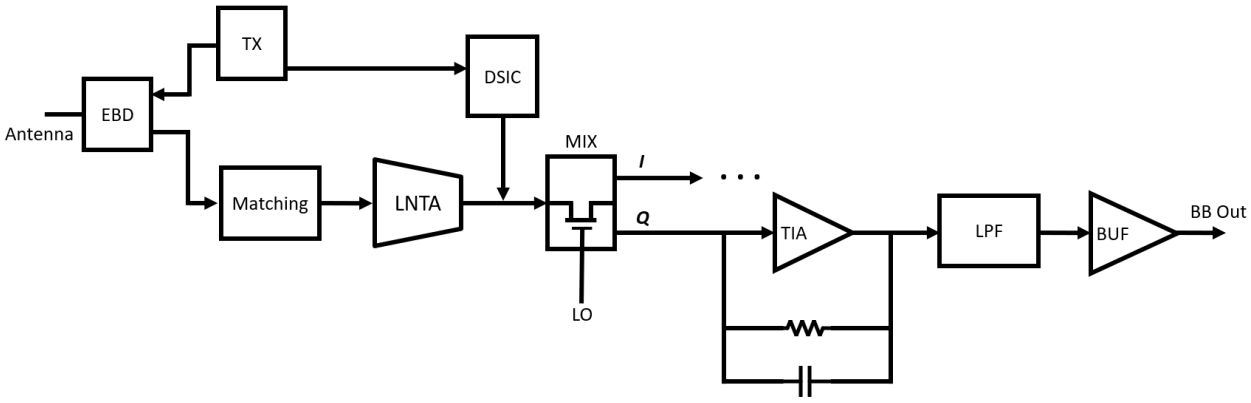


Figure 7: Proposed high-speed IR-UWB receiver

This structure is based on a conventional carrier-based receiver. After being detected by the antenna, the signal will firstly be amplified by a low-noise transconductance amplifier. The amplified output signal is in the current domain, allowing current-domain mixing and injection cancellation by DSIC. Then, the signal will be amplified again by a transimpedance amplifier (TIA), and the signal will become voltage again. After that, the signal will go through the low-pass filter to suppress undesired high-frequency components for anti-aliasing.

As a coherent receiver, the synchronized carrier UWB signal *LO* is needed for down-conversion. In this project, the *LO* signal is obtained from the buffered DCO in the transmitter. The receiver signal is mixed in the differential form to get the in-phase (I) and quadrature (Q) components, where the phase information of the received signal can be obtained from these I/Q components. Furthermore, the power consumption and noise of each block should be designed as low as possible to comply with the IR-UWB technology characteristics. The linearity of this receiver should be given special attention since PPM/PAM modulation scheme is used in this transceiver. An unexpected linearity will distort the pulse shape severely and lower the BER performance, which will furthermore lower the sensitivity and dynamic range of this receiver.

Although the conventional mixer-based receiver architecture is used, it is originally implemented for narrowband signals. When the UWB signal is applied, the biggest challenge is the increased bandwidth of the signal. This problem is mitigated in RF band devices like LNTA and mixer. Since

they are already operating in the RF band, they are wideband enough to be used in the UWB system. However, this is not true for the baseband device: low-pass filter (LPF). For a typical narrowband signal, the LPF bandwidth is only a few megahertz or even kilohertz. The LPF bandwidth required in this IR-UWB receiver can reach up to 500 MHz. Thus, LPF is the design bottleneck of this receiver. A novel LPF structure is implemented in this thesis to cope with the above-mentioned problem, and the details of the design are discussed in Chapter 3.

2.3 Self-interference Cancellation

The interference of the transmitter (TX) to the receiver (RX) is always a troublesome issue in a wireless system. With path loss, a signal would be attenuated dramatically during transmission. Thus, it is preferred to emit a signal with high power in TX to compensate for this path loss. While in RX, the received signal strength is so weak that an amplifier is needed right after the antenna. Thus, with a strong interferer and weak desired signal, this interference severely affect the transceiver. In the radar system, this interference is called TX to RX spillover. Since TX and RX must operate simultaneously, this spillover signal would always exist in RX and saturate the RX link chain. In the communication system, the isolation between TX and RX is also necessary to achieve antenna sharing and duplexing, which is required for multiband/multimode transceivers [30].
In this thesis project, the IR-UWB transceiver is targeted to achieve both RadCom and FD. Thus, self-interference cancellation (SIC) is required and implemented as well. At the early front-end, a duplexer is used to provide isolation and achieve antenna sharing. There are various types of duplex architecture like circulator, electrical balance, and quadrature balance [31], [32], [33]. The electrical balanced duplexer (EBD) is selected for this project due to its wide S11 bandwidth, moderate insertion loss, and low power consumption. At the late analog front-end, a dedicated digital self-interference cancellation (DSIC) module based on the all-digital spillover cancellation method is implemented [20]. The detailed design consideration and specifications are illustrated in Chapter 4.

3 The LPF Design

3.1 Background & Filter Type

As discussed in Chapter 2, the biggest challenge for this receiver is its ultra-wide modulation bandwidth, which dramatically increases the bandwidth that the receiver needs to handle compared to the narrowband system. Since the RF band blocks are already wide-band enough, the baseband part, which is the low-pass filter, becomes the bottleneck of this receiver. Nevertheless, another point that distinguishes it from typical LPF is the group delay. Group delay represents the time delay caused by a system for different frequency components, and it can be calculated as follow:

$$\tau(\omega) = \frac{-d\theta(\omega)}{d\omega} \tag{4}$$

This parameter is a vital criterion, especially for signals with complex waveform, or in other word, complex spectrum distribution. A constant or flat group delay asks for a constant change of phase with frequency. Non-flat group delay means that different frequency components going through the device or system would experience various time delays, which will cause severe distortion to the signal. Since PPM is adopted in this thesis and a time difference of nanosecond scale needs to be detected, the distortion caused by non-flat group delay will ruin the PPM information and lead to poor BER performance. Thus, besides wide bandwidth, the LPF must achieve a flat group delay as well. Furthermore, the power consumption, as well as noise, should be as low as possible. One last notable point is linearity, which will also cause distortion. Since the LPF is cascaded at the very last stage, the linearity should be optimal since the nonlinearity contribution of the later stage in a cascaded stage is larger than the preceding stages.

There exist multiple filter types in wireless systems: passive L(R)C filter, active RC filter, digital filter, and transconductance-capacitance (GM-C) filter. The ideas behind those filter structures are discussed and compared in the following paragraphs.

Passive L(R)C filter is a universal solution for filtering for centuries. It is simple, basic, and easy to be implemented. However, in an integrated circuit (IC), a passive inductor is too bulky and costly, which makes this direct passive implementation of filter suffers from area-inefficiency, large PVT variation, limited tunability, and parasitic. Thus, passive L(R)C filters are mainly used in off-chip low-frequency applications.

With the help of digital blocks, digital filters and switched-capacitor filters are also possible solutions. Nevertheless, in this thesis the receiver requires a high bandwidth filter, which will, in turn, need a very high clock frequency if the digital solution is adopted. This constraint limits the field of digital filters to relatively moderate or low frequency applications as well.

The Op-amp-based active filter has been developed and utilized for filtering out undesired frequency components for decades [34], [35], [36]. In contrast to conventional passive LC filters, the most significant advantage of an active filter is the absence of inductor L. This advantage is even more critical in the IC realm because implementing a passive inductor like a coil on a chip is very difficult and area-consuming with severe nonideality, as discussed above. While using a CMOS-based amplifier, this huge component can be replaced. Furthermore, the active device can also provide isolation between preceding and later stages thanks to its high-input/low-output impedances.

The architecture of active an RC filter is relatively simple. An active device, usually an Op-amp, provides a low-pass-shape transferring characteristic with specific performance parameters: gain bandwidth product (GBP), power consumption, etc. Combined with peripheral passive RC elements, a closed-loop feedback topology is formed, and the desired filtering characteristics can be obtained.

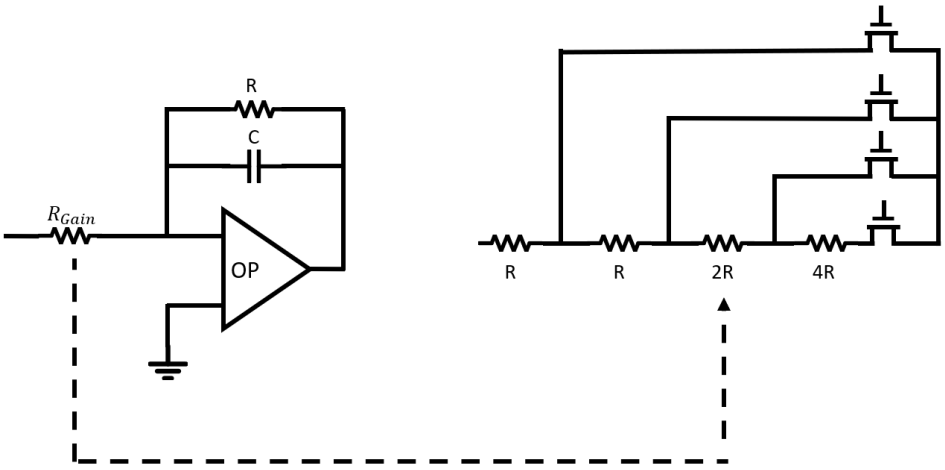


Figure 8: Active-RC filter with gain control [35]

Nowadays, active RC filters targeting high cut-off frequency are also proposed [34]. However, even with a specially designed amplifier, the power consumption, maximum bandwidth, stability, and form factor are still not optimized enough for the IR-UWB receiver in this work. Furthermore, there are trade-offs in the design of Op-amp on its GBW, phase margin (PM) and power consumption [36], which makes this architecture even more challenging to fit this application. For instance, for the desired mW-level low power consumption, the amplifier GBP is usually hundreds of MHz, and the closed-loop cut-off bandwidth is at a few MHz levels [35].

Transconductance-Capacitance (GM-C) structure is another principal approach for high-performance continuous-time analog filter. In contrast to active-RC filters using a closed-loop feedback topology, the GM-C filter provides an open-loop solution, which makes it a prime candidate for wide-bandwidth situation [37].

As stated in its name, the transconductor or operational transconductance amplifier (OTA) is the core element of this structure [37], [38], [39]. Furthermore, it is also an important part of many other continuous-time circuits like data converters, comparators, and oscillators [38]. The OTA can be considered as a black box that offers transconductance operation:

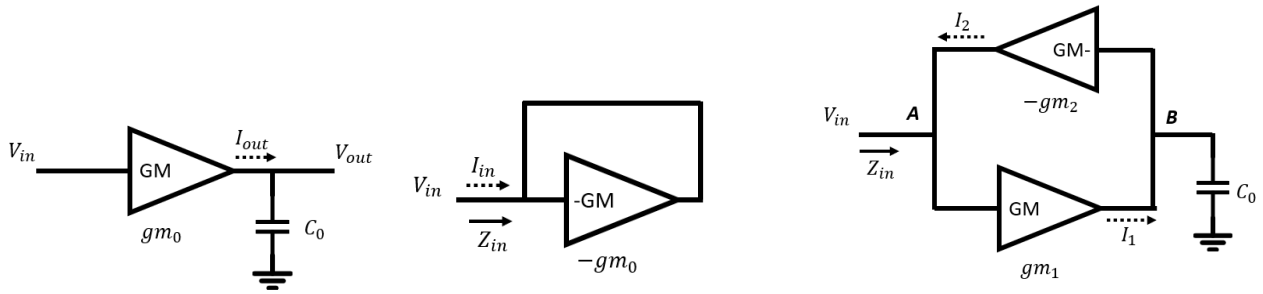
$$I_{out} = GM * V_{in} \tag{5}$$

where I_{out} is the output current, V_{in} is the input voltage, and GM is the transconductance. Based on different OTA designs, they would present different input and output impedance, power consumption, linearity, noise, and other properties.

By cascading the transconductor or OTA with a capacitor C, the GM-C integrator is formed as the basic building block of GM-C filter, which has excellent gain-bandwidth properties since it is an open-loop configuration [40]. Besides integrator, equivalent shunt resistor and inductor could also be implemented with merely OTA and capacitors, as shown in Fig. 9.

Note that a single gyrator can work as a shunt inductor. To implement a series inductor, two gyrators in series are needed. Compared with a conventional passive inductor, this active equivalent inductor is much more area-efficient and tolerant to variation.

Since the basic building blocks are presented, there are two common strategies to build-up the final GM-C architecture [41], [40]. The first approach is the cascade biquad method. Firstly, a second-order biquad is built up with GM-C integrator, resistor and inductor, which works like an equivalent



(a) Integrator (b) Resistor (c) Gyrator

Figure 9: Basic GM-C building blocks [41]

passive LRC second order filter. Then, few biquads are cascaded together to form a higher order filter. The number of biquads and their specifications are decided by the order and filtering type of the desired high-order filter that needs to be implemented. The second approach is the cascade pole method. In this method, a desired passive filter topology like leapfrog structure is firstly presented. Then, the passive elements are replaced with their corresponding GM-C equivalent elements [42], [39]. This conversation is usually implemented with the help of a general impedance converter (GIC) [37].

Compared with the GM-C filter, the analog-RC filter is more challenging and impractical in this scenario. The high-speed IR-UWB receiver in this thesis requires a filter bandwidth of hundreds of MHz to GHz level. Since the active-RC filter uses a closed-loop topology, to have good stability and enough gain, the unity-gain bandwidth or GBP of the Op-amp should be much larger than the filter cut-off frequency. In other word, if the active-RC filter is adopted in this receiver, an Op-amp with at least tens of GHz bandwidth needs to be implemented, which is impractical and violates the design targets of low power and low complexity.

The GM-C filter is a more promising solution for this receiver thanks to its open-loop operation property, in which a very broad bandwidth can be easily achieved. The drawback of this method is limited linearity. With an increased swing, the bias point would vary, which will cause a non-constant transconductance value. However, there are various solutions to tackle this issue like input attenuation (attenuate the swing), source degeneration, nonlinear term cancellation, and so on [37]. Thus, the GM-C filter is the most preferred architecture and is implemented for this IR-UWB receiver.

In this thesis project, a 2 Gs/s ADC is intended to be used at the baseband. Furthermore, the bandwidth of the UWB signal transmitted is 1 GHz in the RF band and 500 MHz in the baseband. To prevent aliasing of ADC, a 5th-order out-of-band filtering is needed. Since the TIA can provide a single pole, the LPF is implemented as a composition of two BiQuad sections, with each BiQuad consisting of two poles.

Besides the topology of the LPF, the filter shape must be selected carefully as well. As described at the beginning of this chapter, to have low pulse distortion, the group delay of the LPF should be flat, which gives a specific requirement to the filtering shape. There are various filter shapes with their dedicated transfer functions to fulfill specific requirements in different applications. For example, the Chebyshev filter has a small transition region at the expense of ripples in the passband. While a Butterworth filter compromises between attenuation and phase response. To achieve the no pulse distortion requirement, the most favorable option is a Bessel filter since it is optimized to obtain a good transient response due to a linear phase response (constant group delay) in the passband. How-

ever, the cost is poor frequency response: the out-of-band attenuation strength is compromised. If the Bessel filter shape is selected, the order of filtering must increase to compensate its poor frequency response of it. An increased filtering order means more BiQuads must be used, which will increase the system scale, and power consumption and degrade the noise and linearity performance. Thus, a transitional filter is adopted here as a compromise between a Gaussian filter, similar to a Bessel, and the Chebyshev filter. An ideal Gaussian filter does not exist in analog as a perfect balance between group delay and out-of-band filtering ability. Instead, two transitional filters implemented to approximate the Gaussian filter are commonly used: Gaussian-up-to-6dB and Gaussian-up-to-12dB.

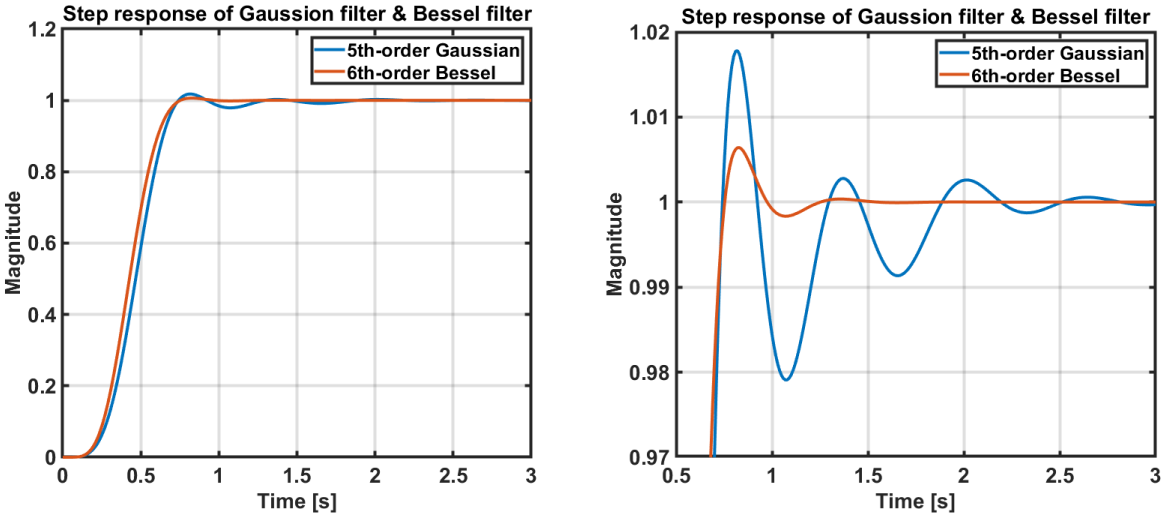


Figure 10: Transient response of Bessel and Gaussian-up-to-6dB filters

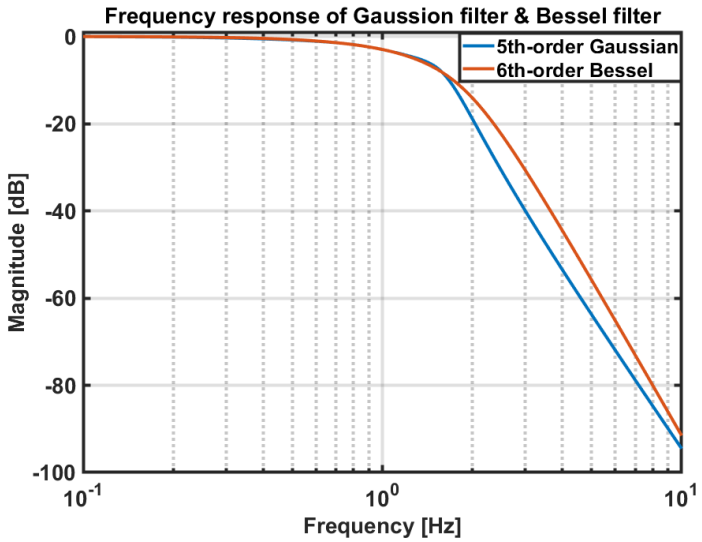


Figure 11: Frequency response of Bessel and Gaussian-up-to-6dB filters

As shown in Fig. 10, the Bessel filter indeed offers a quite good transient performance and thus very flat group delay, which will maximally preserve the shape of the signal. However, the out-of-band filtering is much poorer than the Gaussian type filter, according to Fig. 11. Even when the Bessel filtering is in sixth-order, the fifth-order Gaussian filter still provides a higher signal attenuation. The

group delay of the Gaussian filter is merely slightly worse than the Bessel one. Thus, Gaussian-up-to-6dB is the filter type implemented in this thesis project as a good compromise between attenuation and phase response. The design parameters of Gaussian-up-to-6dB filter sections are shown in table 4.

Table 4: *Gaussian-up-to-6-dB filter design parameters*

Section	f_0*	Quality factor	Comment
1	0.6650	-	1st order TIA
2	1.0317	0.8334	1st BiQuad
3	1.6087	2.2600	2nd BiQuad

*The frequencies are normalized to 1 Hz

The LPF output is directly buffered on-chip in this design. Besides, a current-based offset calibration is implemented within the LPF to trim away DC offset since the structure is pseudo-differential. Finally, the design specifications of this LPF is concluded in table 5.

Table 5: *Design specifications of LPF*

Supply voltage (V)	**0.9**
Filter shape	**Gaussian up to 6dB**
Filter architecture	**GM-C**
Order	**5 (with TIA)**
f_0 (TIA)	**332.50 MHz**
f_0&Q (1st BiQuad)	**515.85 MHz / 0.8334**
f_0&Q (2nd BiQuad)	**804.35 MHz / 2.2600**
Offset trimming	Yes
Total DC power consumption (mW)	2*

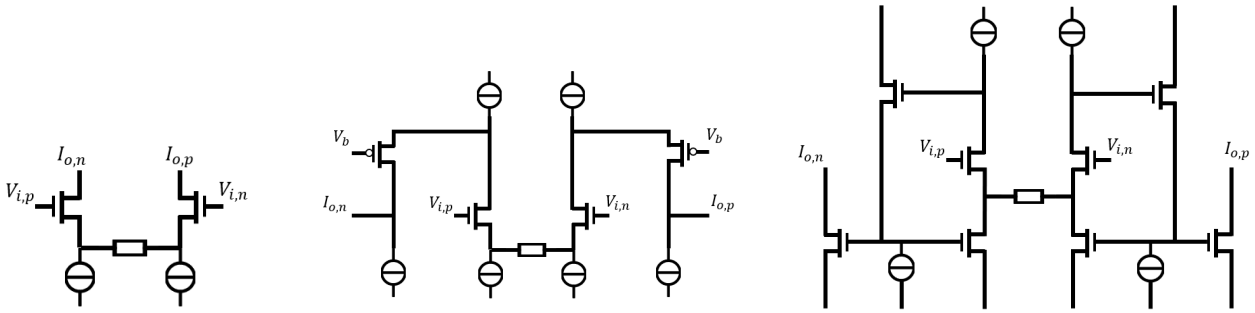
*TIA and offset trimming DAC included

The remaining content of this chapter is scheduled as follow. Section 3.2 introduces the design of the building block of the GM-C filter: the GM cell. In Section 3.3, a novel GM-C BiQuad is proposed and discussed. Then, the total 5th-order LPF including the single-pole TIA and two BiQuads are presented in Section 3.4. Finally, the layout design, as well as some post-layout simulations are discussed in Section 3.5.

3.2 GM Cell Design

As introduced in Section 3.1, transconductor is the core of a GM-C filter topology. Some papers have proposed complex OTA with fine characteristics [42]. However, in this thesis project, the target is

energy efficiency and low complexity. Thus, the transconductor is called GM cell in this thesis, which represents a basic block that provides the functionality of transconducting.
The following criteria are considered during the design of GM cell: bandwidth, power consumption, complexity, noise, and dynamic range. As an energy-efficient transceiver, the power consumption must be limited. Furthermore, since the signal is UWB, the bandwidth should also be wide enough to handle it, as stated before. A simple structure is preferred as well because high complexity will lead to a larger form factor and power. Finally, the power supply is set to be 0.9 V, which is already very low. The dynamic range should also get special attention to. Since the signal swing is limited, the noise should be limited as well to maximize the SNR at the baseband interface.
Besides sophisticated OTA structures, there are many existing topologies for low-complexity GM cells, as shown in Fig. 12. All of these structures are differential. To achieve transconductance operation, the basic idea behind them is to copy the differential input voltage on a resistive element and then sense the current flowing through it. The feedback loop topology is most suited for low-frequency applications, and many variants exist to improve its performance, like linearity and accuracy. The additional cascode stage maximizes the output impedance to make the output current node more like an ideal current source. However, all those tricks come with the cost of a limited input voltage range since all transistors should be set in the saturation region. To tackle this, a push-pull style is adopted where a complementary input stage is used.



(a) Single-stage (b) Folded cascode (c) Feedback loop

Figure 12: Popular GM topologies

Compared with other options, a single-stage GM cell structure outperforms other candidates in bandwidth, complexity, and noise. With the cascode stage or feedback loop, extra nodes are added, and the bandwidth will degrade. Those extra parts also give additional noise and require bias sources, which significantly increases the complexity. Thus, to realize a wide bandwidth while keeping the power consumption and complexity at a low level, the single-stage topology is preferred. In combination with push-pull configuration, a single-ended inverter structure is selected and implemented in this thesis project. As a simple inverter, the complexity is very low. Furthermore, since the current is reused, the energy efficiency is high. Without extra parts, no additional node is introduced and the gain-bandwidth performance is maximized. However, the drawback of an inverter is poor supply noise rejection. The variation of the supply significantly affects the bias current. Thus, a low-noise supply regulation is needed. Another downside of this structure is that the gm is not linear enough since the gm is set by the MOS transconductance, which is very nonlinear. To handle this issue, a degenerative resistor is added at the source of the MOS. Finally, two extra MOSs are inserted between the supply/ground and the inverter as digital enable switches. With this enable switch, the transconductance value is then configurable using several GM cells in parallel and enabling part of them to

obtain a specific desired GM value.

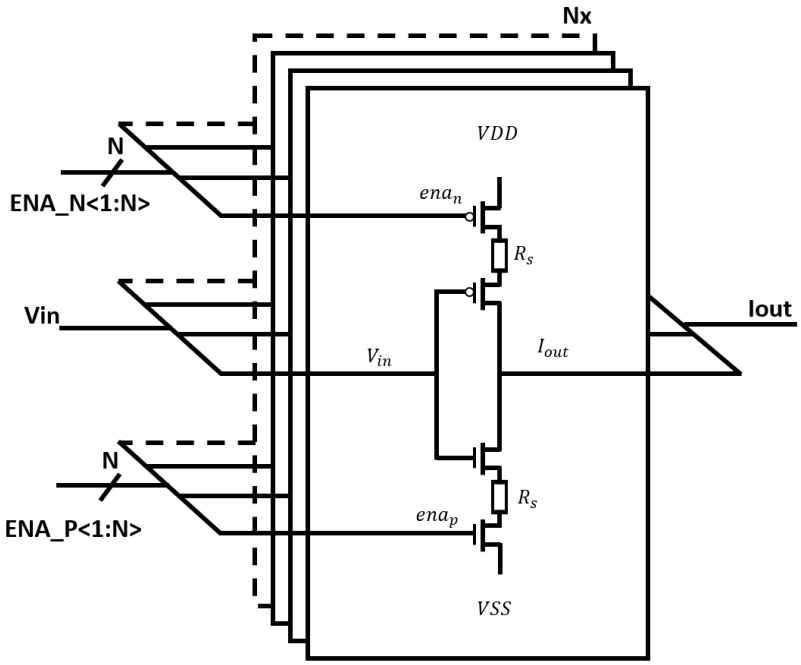


Figure 13: Proposed GM cell

The proposed GM cell is shown in Fig. 13. The GM cell is simple and only consists of an inverter, degeneration resistors, and two enable switches. The design target is that the trip-point is at half of the supply, where the GM value is linear and almost constant with input swings, while the output node is kept at half supply level as well. To form this GM cell, a low threshold voltage transistor structure of TSMC 28 nm technology is used since the supply voltage is low. To align the NMOS and PMOS and set the trip-point of the inverter at half of the supply, the width ratio of them is set to be:

$$WidthRatio = \frac{W_{NMOS}}{W_{PMOS}} = 1.27 \tag{6}$$

A low dropout regulator (LDO) is used here to control the supply variation. Under 0.9 V supply voltage, the LDO outputs a variance tolerant supply voltage of around 0.8 V. The width of NMOS is set to be 3.04 um while the width of PMOS is 2.4 um to optimize the GM cell performance. Both of them have two fingers. The NMOS length is set to be 90 nm, and the PMOS length is set to be 60 nm. The lengths of the two switches are set to be 40 nm while their widths are equal to the corresponding width of the inverter. With this configuration, the trip-point is set at half of the LDO output, which is 400 mV. By sweeping the R_s value from 1 kΩ to 5 kΩ and checking the simulated BW, DC gain, transconductance value and DC current, the optimal resistance value is selected to be around 2.7 kΩ such that the GM value is flat within 10% variation over the supply voltage range. The achieved performance of this GM cell is shown in table 6.

Table 6: *GM Cell Performance*

Structure	Inverter with resistive degeneration
Unity Bandwidth	2.2* GHz
DC Gain	22 V/V (26.8 dB)
Transconductance (GM)	188 uS (1/5300)
DC Current	6.5 uA
DC Power	5.85 uW

*Loaded with another unit GM cell

3.3 GM-C BiQuad

3.3.1 Basic GM-C Building Blocks

Typically, an OTA has a differential input and differential output. Both positive and negative transconductance can be achieved by playing with connection polarity. However, as introduced in Section 3.2, the GM cell used in this thesis project is a single-stage inverter, which is single-ended instead of differential. Furthermore, since it is inverter based, its current flows into the output node. In other word, the equivalent GM value is negative. To form a typical OTA, two GM cells are packaged together with inverted output pins, as shown in Fig. 14.

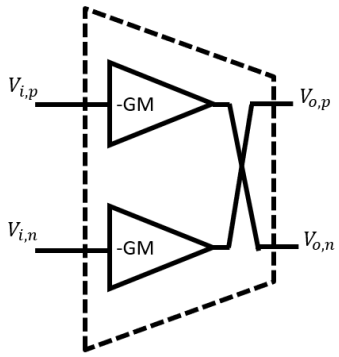


Figure 14: OTA formed by proposed GM cell

Similar to the one described in Fig. 9, basic GM-C building blocks built up with the GM cell proposed in Section 3.2 is discussed in this subsection. Firstly, the simple but important block is an integrator formed by a GM cell and a capacitor, as shown in Fig. 15.
The integration is achieved by applying the GM current on the shunt capacitor at the output node, as shown in equations 7 and 8. Note that the sign of the output voltage is inverted since an inverting-transconductance GM cell is used here.

$$I_o = V_{in} \times (-gm_0) \tag{7}$$

$$V_{out} = I_o \times \frac{1}{sC_o} = V_{in} \times \frac{-gm_0}{sC_o} \tag{8}$$

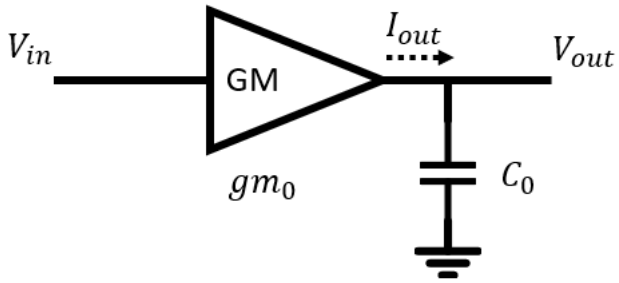


Figure 15: GM-C integrator

Another vital block is resistor. By shorting the input and output node of the GM cell, they would then have the same voltage level (diode connected GM cell). This structure can be considered as an equivalent shunt resistor. The calculation is shown in the following equations.

$$I_{in} = -I_o = -V_{in} \times (-gm_0) \tag{9}$$

$$Z_{in} = R_{eq} = \frac{V_{in}}{I_i} = gm_0 \tag{10}$$

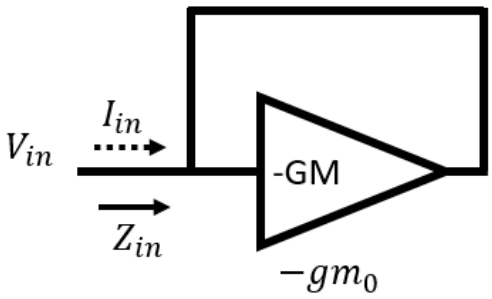


Figure 16: Equivalent shunt resistor formed by GM cell

Compared with normal passive resistor, this equivalent resistance value is more accurate. Also, the resistance value can be easily tuned digitally with a configurable GM value. Note that this shunt resistor is achieved with a negative GM cell. If a positive GM cell is applied, then it will become a negative resistor that feeds current back to the input node.

The most important and commonly used block is a gyrator. A GM-C gyrator is formed with two loop-connected GM cells with inverted signs. A capacitor is connected at one of the node. The block is shown in Fig. 17. Depending on the application, the output node could either be the same node with input or locate at another node.

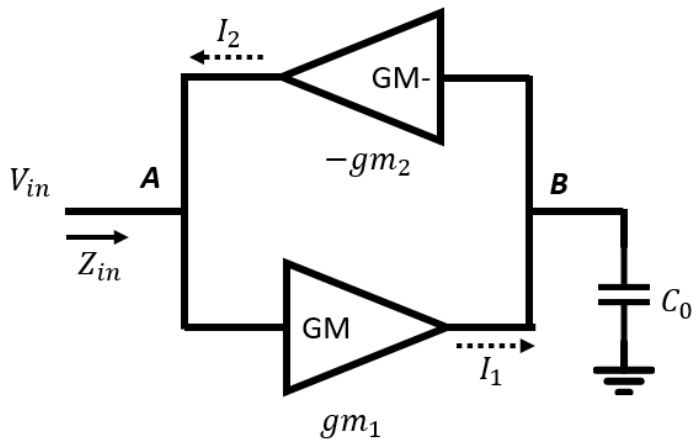


Figure 17: GM-C gyrator

As shown in Fig. 17, two GM cells are connected head to tail. In order to loop the current, they must have the opposite sign. Otherwise it would be an equivalent big GM cell with twice the transconductance value. There are two nodes. Node A is at the input of the positive GM cell, while node B is at the input of the negative or inverting GM cell. Usually, a capacitor is placed at node B since current flows out at node B and the voltage across the capacitor would then be positive. However, this is under the assumption that the voltage at node A is positive. Thus, the input port is commonly at node A, where a positive input impedance is seen from it since the upper GM cell is negative and current flows into node A. It is possible to set the input port at node B as well. Then the capacitor needs to be placed at node A, and the voltage at node A is negative. The theoretical calculations are shown as follows.

$$I_1 = V_{in} \times gm_1 \tag{11}$$

$$V_B = I_1 \cdot \frac{1}{sC_o} = \frac{V_{in} \cdot gm_1}{sC_o} \tag{12}$$

$$I_2 = V_B \times (-gm_2) = -\frac{V_{in} \cdot gm_1 \cdot gm_2}{sC_o} \tag{13}$$

$$Z_{in} = \frac{V_{in}}{-I_2} = \frac{sC_o}{gm_1 \cdot gm_2} = s \cdot L_{eq} \tag{14}$$

where

$$L_{eq} = \frac{C_o}{gm_1 \cdot gm_2} \tag{15}$$

$$H_{voltage} = \frac{V_B}{V_{in}} = \frac{gm_1}{sC_o} \tag{16}$$

According to equation 14, the input impedance is an equivalent inductor with an inductance value composed of GM values and the tunable capacitance. Thus, when the output port is at node A as well, the gyrator can be considered as a shunt inductor with configurable inductance value. Compared to

a passive inductor, this active equivalent one is tunable, area-efficient, and tolerant to PVT variance. Furthermore, if the output port is at node B, the lower branch is reused as an integrator with transfer function shown in equation 16. Then the gyrator can be considered as a shunt inductor cascaded with an integrator.

With all the above-introduced blocks, a GM-C BiQuad can be built. Since equivalent resistor, inductor and integrator are presented, a second-order filter can be easily achieved by first designing the passive LRC filter prototype and then replacing all the passive elements with their corresponding active equivalent counterpart. However, as discussed in Section 3.1, to realize this filter, the cascade pole method is commonly used, where a series inductor is always required. To achieve series inductor, two gyrators are used, as shown in Fig. 18. Instead of only one loop, two loops are used with four GM cells. Since it is an equivalent series inductor, the two nodes on the left and right sides are the two ports of the inductor. A capacitor is put at the middle node of the two loops to generate a frequency-dependent voltage. Note that the negative GM cell in the left loop and the positive GM cell in the right loop must have the same absolute transconductance value. Since it is a series device, its current must be consistent and continuous. Different absolute GM values of those two cells lead to different current values flowing in and out of this device. In practice, the GM value of all four GM cells are typically set to be the same for the sake of convenience and the series equivalent inductance can be calculated as follows:

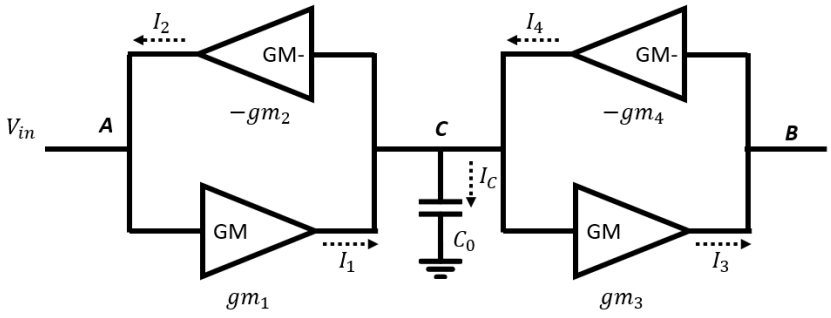


Figure 18: Equivalent series inductor with GM-C gyrator

Assume:

$$gm_1 = gm_2 = gm_3 = gm_4 \tag{17}$$

Then,

$$I_C = I_1 + I_4 = gm \cdot (V_A - V_B) \tag{18}$$

$$V_C = \frac{gm \cdot (V_A - V_B)}{sC_0} \tag{19}$$

$$I_{in} = -I_2 = -(-gm) \times \frac{gm \cdot (V_A - V_B)}{sC_0} \tag{20}$$

$$I_{out} = I_3 = gm \times \frac{gm \cdot (V_A - V_B)}{sC_0} \tag{21}$$

$$Z_{series} = \frac{V_{across}}{I_{through}} = \frac{V_A - V_B}{I_{in,out}} = \frac{sC_0}{gm^2} \tag{22}$$

3.3.2 Conventional Topology and Stability Issue

Last Section 3.3.1 presents the commonly used building blocks in GM-C filter design. With those blocks, the desired filter can be designed. There are two popular strategies to build up the GM-C filter architecture, as introduced in Section 3.1. The first strategy is by cascading the poles. The desired filter topology is firstly implemented with passive components, and then all the passive elements are replaced with the GM cell building blocks mentioned above. In [37], a fifth-order elliptic GM-C low pass filter is implemented. Firstly, the passive elliptic filter is presented as shown in Fig. 19.

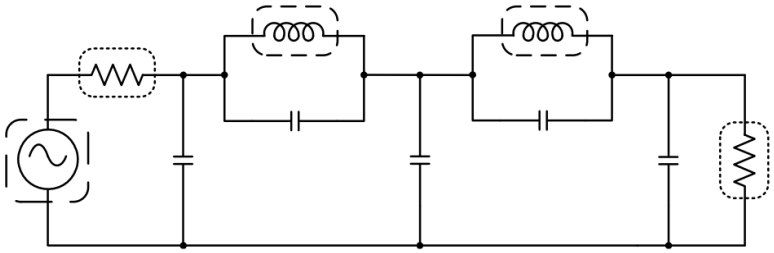


Figure 19: A passive 5th-order elliptic low-pass filter [37]

Then by replacing all the passive elements with their active equivalent blocks introduced in Section 3.3.1, the active GM-C filter is obtained, as shown in Fig. 20, which has the same filtering characteristics as the passive filter.

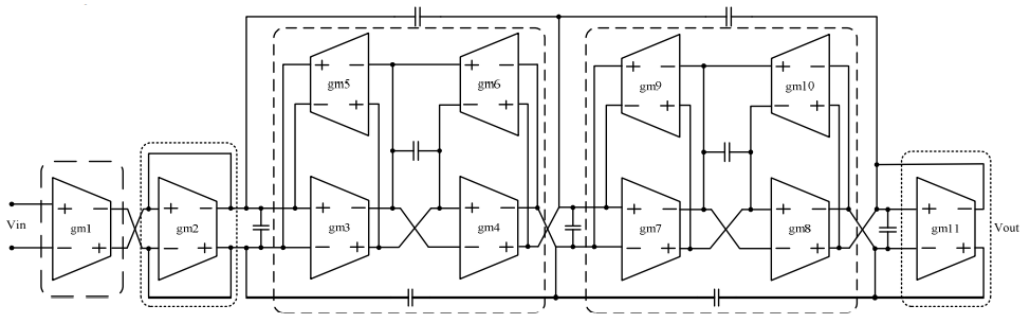


Figure 20: Active GM-C 5th-order elliptic low-pass filter [37]

Various GM-C filters have been implemented with this strategy. A 5th order GM-C filter with a leapfrog LC-ladder type is designed [42]. While in [39], a 5th order GM-C low pass filter with Chebyshev ladder characteristic is proposed.
However, another strategy of the cascade BiQuad method is adopted in this thesis project. Within this strategy, the GM-C filter is built up by cascading several GM-C BiQuad, which is a second order filter. The exact characteristics of each BiQuad depend on the desired filter type. In this project, since a fifth order Gaussian-up-to-6dB-filter-type is desired, and TIA can provide one single pole, the LPF is then composed of two BiQuads which provide a fourth-order of filtering.
Despite the different designs of OTA and GM cells, the implementation of GM-C BiQuad is achieved by a general topology. Similar to the cascade pole strategy, the design of second-order BiQuad starts with passive filter structure. Unlike high-order filters, the second-order filter utilizes a common LRC structure as shown in Fig. 21.
This filter can achieve band-pass filtering with a tunable bandwidth and quality factor Q. By replacing the resistor and inductor with the active GM-C equivalent block, the GM-C BiQuad is then obtained. To achieve low-pass filtering, the S-parameter in the numerator of the transfer function of this filter

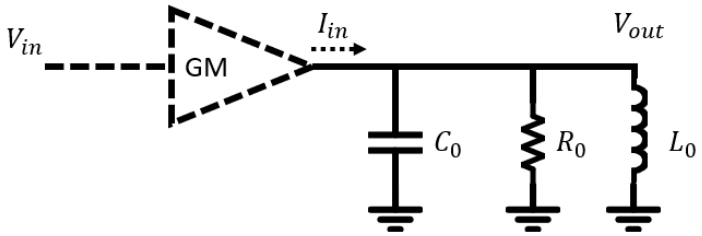


Figure 21: Passive LRC filter

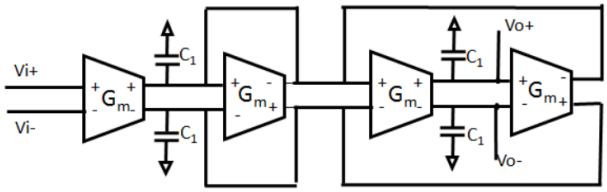
must be eliminated. Recall from Section 3.3.1 that the gyrator can be reused as a shunt inductor and a cascaded integrator. Thus, by switching the output port from node A to node B, the numerator S parameter can be canceled by the integrator, and the low-pass filtering can be easily achieved. This idea has been used as a common solution for low-pass GM-C BiQuad design. Thus, similar block diagrams can be found in Fig. 22 from different GM-C filter design papers.

For those BiQuads, a Gm cell is placed at the beginning to convert the input voltage to current. Then a capacitor, an equivalent shunt resistor, and an equivalent shunt inductor is connected after the first GM cell to absorb the injected current and translate it back to voltage. If the output node is directly the node right after the first GM cell, the BiQuad is then a band-pass filter. Thanks to the characteristic of GM-C gyrator, another integration is provided to the other node of the gyrator. By putting the output port at that node, the band-pass filtering becomes low-passing.

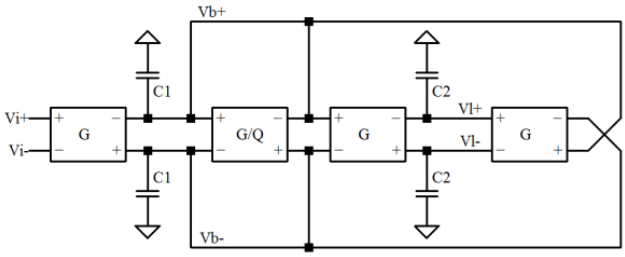
This BiQuad structure can be used in this thesis project as well. To suppress common mode variance, the baseband part of this receiver is differential. As discussed in Section 3.2, instead of a differential OTA, a single-ended inverter-based GM cell is implemented in this thesis. Thus, to form a differential filter, the pseudo-differential structure is used. One challenging point is the design of the GM-C gyrator since the GM cell used is single-ended and inverting. So it is not possible to directly achieve a single-ended gyrator, same as the one in Fig. 17. Thanks to the pseudo-differential architecture, one possible solution is to swap the input polarities between two GM cells on differential paths. The final diagram is shown in Fig. 23.

As shown in this diagram, there is a cross-coupling in the middle to create a pair of equivalent positive GM cells, which can, in turn, form a gyrator. Furthermore, two GM cells that are placed between differential paths together with the two self-connected GM cells form a Nauta Amplifier. These two GM cells can be considered as self-connected GM cells with a positive GM value, which is an equivalent negative resistor. The net shunt resistance at this node is then the sum of the positive equivalent resistor and negative equivalent resistor. However, this cross-coupling results in a positive loop gain for the common mode (CM) signal, which decides the biasing of the whole filter. Thus, a complex CM regulation circuit is needed between the two output points.

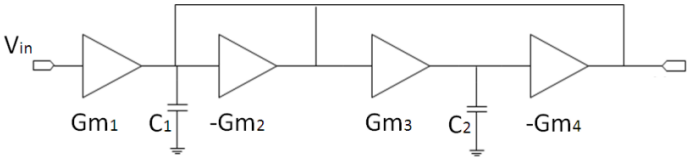
To avoid this issue, another solution is proposed, as shown in Fig. 24. Instead of swapping the input polarity, a GM-resistor pair is used to change the sign of GM cells. A GM-resistor pair is composed of a single GM cell in series with an equivalent resistor, which is a self-connected GM cell. It provides a voltage to voltage transformation, and the transfer function is calculated in equation 23.



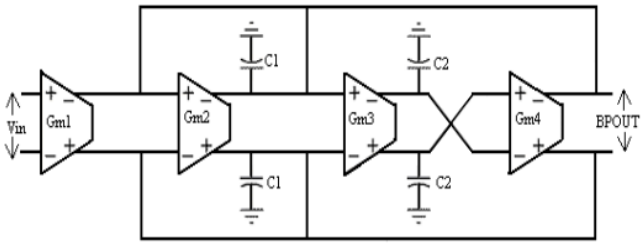
(a) A low-pass BiQuad [38]



(b) A low-pass and band-pass BiQuad [43]



(c) A single-ended low-pass BiQuad [44]



(d) A band-pass BiQuad [45]

Figure 22: Some GM-C BiQuads design

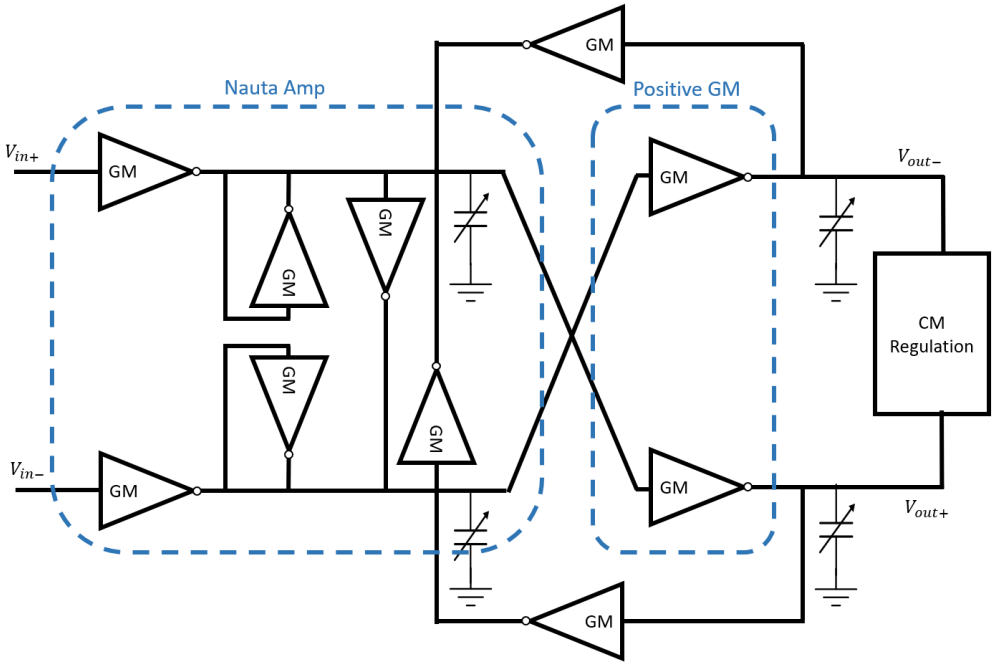


Figure 23: One solution with inverting scheme

$$H = \frac{V_{out}}{V_{in}} = \frac{I_{out} \cdot Z_{out}}{V_{in}} = -\frac{gm_1}{gm2} \tag{23}$$

If gm_1 is equal to gm_2, this pair can provide a unity-gain transformation with inverting sign. By cascading this pair with a normal inverting GM cell, a positive GM cell is then created. Furthermore, it can provide various gains by playing with the GM ratio of gm_1 and gm_2. This inverting pair is used in the block diagram in Fig. 24 to form a gyrator.

Unlike the previous solution, the BiQuad structure shown in 24 is symmetrical, and no cross-connection exists. Thus, the loop gain for both CM and differential mode (DM) signals is the same and negative. In other word, no extra complex CM regulation circuit is needed. In comparison with an active RC filter, this is a more open-loop solution, which means that the bandwidth, and Q can be relatively wide-range by configuring the equivalent resistance, inductance and capacitance value directly in the block diagram. The transfer function of this BiQuad is calculated as follows. Note that the signal is considered as single-ended one for the convenience of calculation.

As mentioned-above, the equivalent resistance and inductance are:

$$R_{eq} = \frac{1}{gm_1} \tag{24}$$

$$L_{eq} = \frac{sC_0}{gm_{positive} \cdot gm_{negative}} = \frac{sC_2}{gm_4 \frac{gm_2}{gm_3} \cdot gm_5} \tag{25}$$

Then,

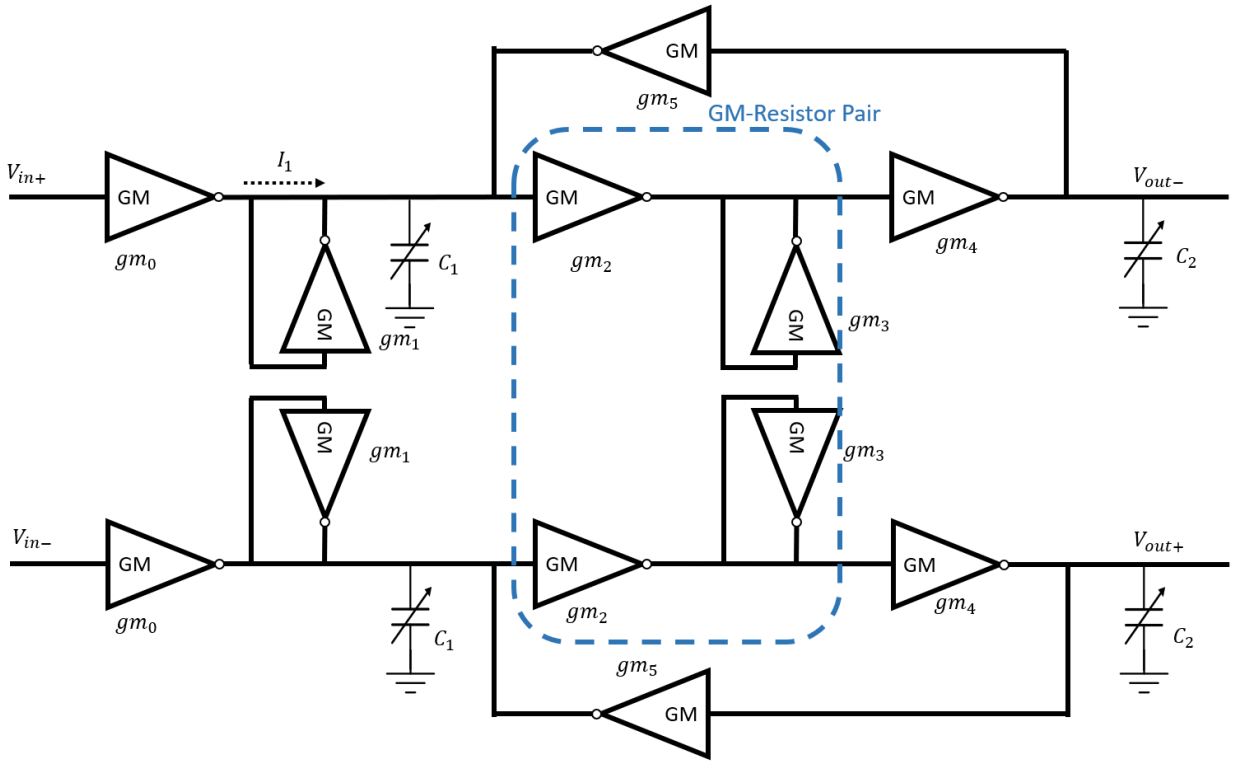


Figure 24: Second solution without inverting scheme

$$
\begin{aligned}
H(s) &= \frac{V_{out}}{V_{in}} \\
&= \frac{I_1 \cdot R_{eq}||L_{eq}||C_1}{V_{in}} \times H_{integrator} \\
&= \frac{I_1}{V_{in}} \times \frac{1}{1/R_{eq} + 1/L_{eq} + s \cdot C_1} \times \frac{gm_{positive}}{s \cdot C_2} \\
&= \frac{-V_{in} \cdot gm_0}{V_{in}} \times \frac{1}{gm_1 + \frac{gm_5 \cdot gm_4 \frac{gm_2}{gm_3}}{s \cdot C_2} + s \cdot C_1} \times \frac{gm_4 \frac{gm_2}{gm_3}}{s \cdot C_2} \\
&= -\frac{gm_0 \cdot gm_2 \cdot gm_4}{gm_3 C_1 C_2 \cdot s^2 + gm_1 gm_3 C_2 \cdot s + gm_2 gm_4 gm_5}
\end{aligned}
\tag{26}
$$

where the DC gain is:

$$
|H_{DC}| = \frac{gm_0}{gm_5} \tag{27}
$$

The resonance frequency as well as the quality factor can be obtained as well:

$$
\omega_o = \sqrt{\frac{gm_2 gm_4 gm_5}{gm_3 \cdot C_1 C_2}} = K \cdot \sqrt{\frac{1}{C_1 C_2}} \tag{28}
$$

$$
Q = \sqrt{\frac{gm_2 gm_4 gm_5 C_1^2}{gm_3 gm_1^2 C_1 C_2}} = K \cdot \sqrt{\frac{C_1}{C_2}} \cdot \frac{1}{gm_1} \tag{29}
$$

According to equations 28 and 29, the bandwidth is set by the ratio of those GM cell transconductance and the geometric mean of the two capacitors, while the quality factor Q depends on the transconductance values as well as the ratio of the two capacitors. Thus, there is no strong correlation or trade-off between those two parameters. In other word, the targeted filtering performance shown in table 5 could be achieved by playing with the transconductance value of all the GM cells and the value of the two capacitors.
However, even as an open-loop solution, the stability of this filter must be taken into account. Although the passive equivalent filter is simple and open-loop, the gyrator introduces one feedback loop. With this feedback loop, the system may become unstable. To illustrate this, the high-level block diagram of this BiQuad is drawn below in Fig. 25 to further analyze the stability.

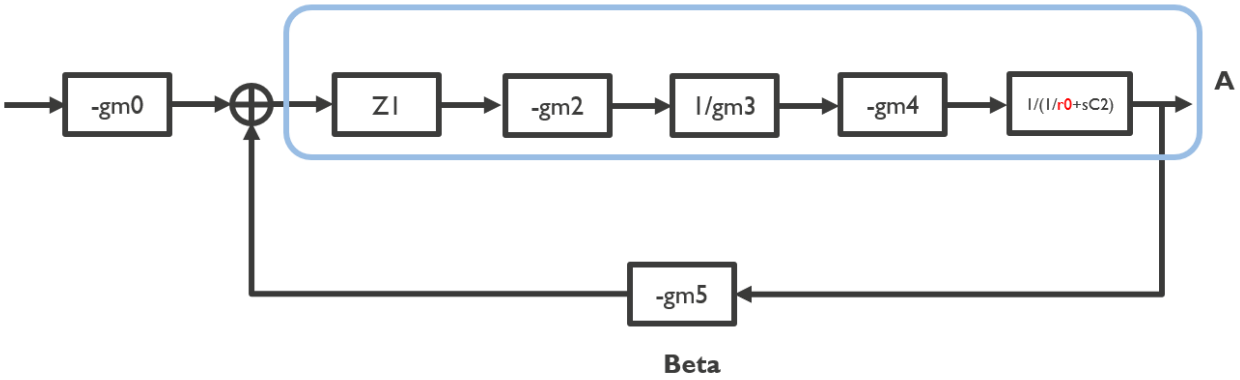


Figure 25: Block diagram of the BiQuad

As shown in Fig. 25, all the blocks inside the loop can be considered a single gain A. Then, this BiQuad becomes a very basic negative feedback loop structure. Unfortunately, this BiQuad structure fails to fulfill the requirement of this receiver LPF due to its strong relationship between quality factor Q and stability parameter phase margin (PM). While the bandwidth can be relatively easy to get pushed to a high value, the phase margin would decrease when Q is also pushed to a higher value regardless of the value of bandwidth. A theoretical analysis of this phenomenon is shown below.
The GM cell can be considered as a frequency-independent device within its bandwidth. The feedback signal is inserted through Kirchhoff Current Law (KCL) at the node right after the first GM cell. Thus, all the physical units can be extracted and a pure mathematical feedback model can be analyzed. There are two poles within the loop. One pole is from impedance Z_1, which is composed of the shunt equivalent resistor and capacitor C_1. The second pole is at the output node formed by GM cell output impedance and capacitor C_2. Both of those two poles are negative real poles, and they are within the large superimposed gain A. To generalize the situation, the transfer function of A is assumed to be:

$$A(s) = \frac{k_{DC}}{(\frac{s}{\omega_1}+1)\cdot(\frac{s}{\omega_2}+1)} = \frac{k_{DC}}{\frac{s^2}{\omega_1\omega 2}+s(\frac{1}{\omega_1}+\frac{1}{\omega_2})+1} \tag{30}$$

where the two negative real poles are ω_1 and ω_2. Then the closed-loop transfer function with negative feedback coefficient $-\beta$ is calculated below:

$$H(s) = \frac{A}{1-A\beta} = \frac{k_{DC}}{\frac{s^2}{\omega_1\omega 2}+s(\frac{1}{\omega_1}+\frac{1}{\omega_2})+1+k_{DC}\beta} \tag{31}$$

From this equation 31, the bandwidth, as well as the quality factor Q of this closed-loop system can be derived.

$$\omega_0 = \sqrt{k_{DC}\beta+1}\cdot\sqrt{\omega_1\cdot\omega_2} \tag{32}$$

$$Q = \sqrt{k_{DC}\beta+1}\cdot\frac{\sqrt{\omega_1\cdot\omega_2}}{\omega_1+\omega_2} \leq 0.5\cdot\sqrt{k_{DC}\beta+1} \tag{33}$$

As shown in equation 33, the second term $\frac{\sqrt{\omega_1\cdot\omega_2}}{\omega_1+\omega_2}$ reaches its maximum value of 0.5 when ω_1 and ω_2 are equal. Since the required Q value of the second BiQuad is as high as 2.26 as shown in table 5, the maximum Q situation is considered and it is assumed that the open loop poles ω_1 and ω_2 are the same and equal to ω_A. Then, the bandwidth and Q of the closed-loop system would become:

$$\omega_0 = \sqrt{k_{DC}\beta+1}\cdot\omega_A \tag{34}$$

$$Q = 0.5\cdot\sqrt{k_{DC}\beta+1} \tag{35}$$

$$PM = |\angle Loop\_Gain(\omega_{gcf})| \tag{36}$$

where,

$$Loop\_Gain(s) = A(s)\cdot\beta = \frac{k_{DC}\cdot\beta}{\frac{s^2}{\omega_1\omega 2}+s(\frac{1}{\omega_1}+\frac{1}{\omega_2})+1} \tag{37}$$

$$|Loop\_Gain(\omega_{gcf})| = 0\ dB \tag{38}$$

According to equation 35, to increase the quality factor Q, the only way is to increase the DC gain of the loop gain, which is $k_{DC}\beta$. However, increased DC gain would result in an increased gain crossover frequency. Even with constant ω_0, where ω_A needs to decrease to compensate for the increase of DC gain $k_{DC}\beta$, since the power of $k_{DC}\beta$ is 1/2 while the power of ω_A is 1 in equation 34, the increment of $k_{DC}\beta$ is always the square times of the decrease of ω_A. This arrangement would finally still cause the increment of gain crossover frequency, which further decreases the phase margin of the system since ω_0 is set to be constant. In other word, there is a trade-off between quality factor Q and stability parameter PM. To have a high Q, the PM will decrease regardless of the exact value of ω_0. This trade-off is illustrated clearly with the following simulation result Fig. 26 from MATLAB.
The closed-loop bandwidth ω_0 is set to be constant in this simulation, and the DC gain of the loop gain $k_{DC}\beta$ increases to boost the Q. As shown in this chart, the phase margin decreases rapidly with increased Q. To ensure the stability of this system, the phase margin should be larger than 45 degree. According to this chart, the maximum achieved Q would be around 1.4 to 1.5 if a PM of more than 45 is required. As shown in Fig. 27, the simulation result of a real circuit BiQuad implemented with the GM cell introduced in Section 3.2 also gives expected decreased stability performance with high Q value. The circuit simulation is carried out with Cadence.
According to the design specification in table 5, the required quality factor of the first BiQuad is 0.8334, which can still be achieved with this structure since the PM would be around 90 degrees with this Q value. However, the Q value of the second BiQuad is as high as 2.26, which would cause a catastrophic stability issue with this BiQuad architecture. As shown in Fig. 28, the required DC gain of the loop gain goes up to 19.5 V/V, which is 25.8 dB. Besides, the PM of the closed loop decreases to around 26 degrees, which is far less than the required safety value of 45 degrees. Thus, at least for the second BiQuad, the conventional "Open Loop" BiQuad solution is not valid anymore. To tackle this issue and break the trade-off between Q and PM, a novel closed-loop BiQuad structure is proposed and introduced in the following Section 3.3.3.

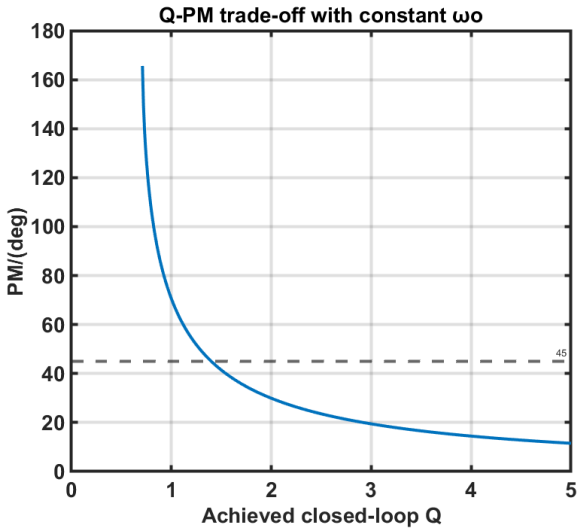
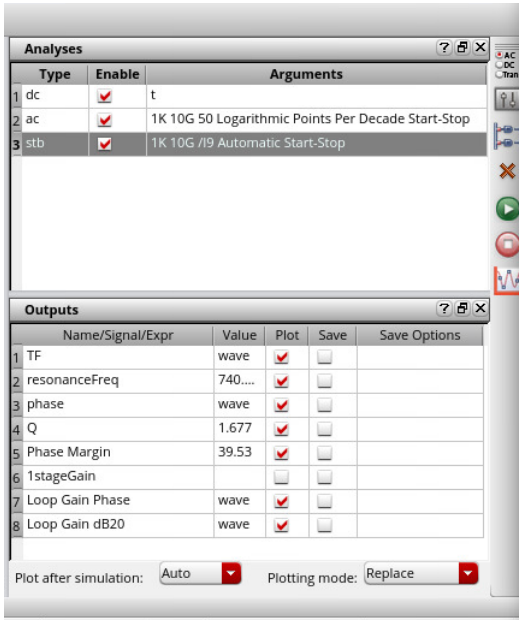
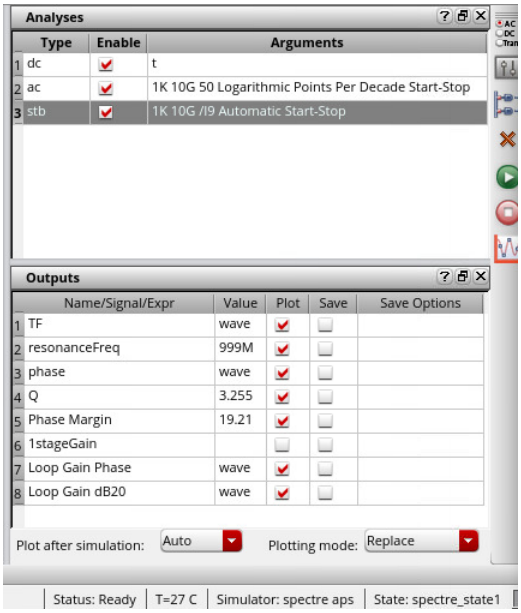


Figure 26: Trade-off between quality factor Q and stability PM

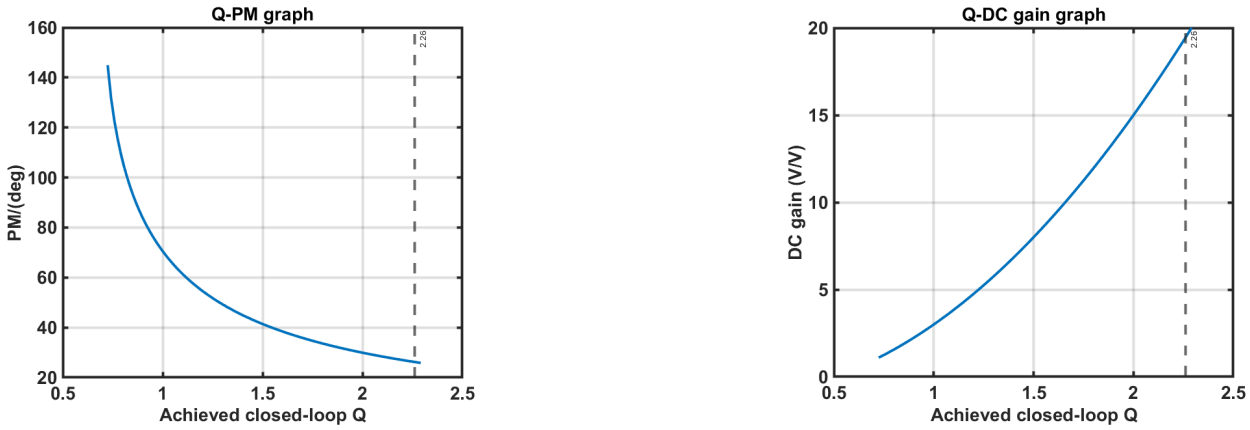


(a) Q-PM with Q of 1.677



(b) Q-PM with Q of 3.255

Figure 27: Circuit simulation of Q-PM trade-off



(a) Q-PM graph (b) Q-DC gain graph

Figure 28: Consequence of pushing Q to high value

3.3.3 Proposed Closed-loop BiQuad Topology

According to equation 30, the root cause of the above-mentioned Q-PM trade-off is that the open loop transfer function A has two negative pure real poles. This condition causes that the closed-loop Q is always smaller than $0.5 \cdot \sqrt{k_{DC}\beta + 1}$ as shown in equation 33. To find a way to break the trade-off, a more generalized open loop transfer function with complex poles is assumed below.

$$A = \frac{k_{DC} \cdot \omega_A^2}{s^2 + s\frac{Q_A}{\omega_A} + \omega_A^2} \tag{39}$$

Then, the closed-loop function becomes:

$$H(s) = \frac{A}{1 - A\beta} = \frac{k_{DC} \cdot \omega_A^2}{s^2 + s\frac{Q_A}{\omega_A} + \omega_A^2 + k_{DC} \cdot \omega_A^2 \cdot \beta} \tag{40}$$

The corresponding bandwidth and quality factor can be calculated as well.

$$\omega_0 = \sqrt{k_{DC}\beta + 1} \cdot \omega_A \tag{41}$$

$$Q = \sqrt{k_{DC}\beta + 1} \cdot Q_A \tag{42}$$

Unlike a pure real pole system where Q_A is limited to be maximally 0.5, a complex pole system can have any value of Q_A. Thus, instead of boosting the DC gain $k_{DC}\beta$ which degrades the stability performance, higher closed-loop Q can be obtained by increasing the Q of the open-loop transfer function A. Thus, the trade-off between Q and PM can be broken up.

However, to build up this system, the first step would be implementing an open-loop system with complex poles, which is quite difficult for the current BiQuad structure. According to the block diagram shown in Fig. 25, the open-loop system is composed of two real poles in cascading. The first pole is from impedance Z_1. Z_1 consists of an equivalent resistor and capacitor, and the pole created by them is definitely real. The second pole is at the position of C_2. In combination with the output impedance of the GM cell, the second real pole is created. Thus, it would be impossible to directly switch this open-loop system to the one with complex poles and higher Q since the poles are created by impedance and capacitance in a real circuit.

Nevertheless, switching to complex poles requires an open-loop quality factor Q_A value of more than 0.5. Although it is impossible to use the pole cascading structure, it is not compulsory to only use this one. Any system with a large Q value can be used as the open-loop system. Fortunately, the closed-loop system introduced above is a fair candidate. Even with Q and PM trade-off, Q can still be as high as about 1.5 with acceptable PM. Thus, a novel closed-loop or multi-loop BiQuad structure is proposed in this thesis project. The high-level block diagram of this idea is illustrated in Fig. 29 below.

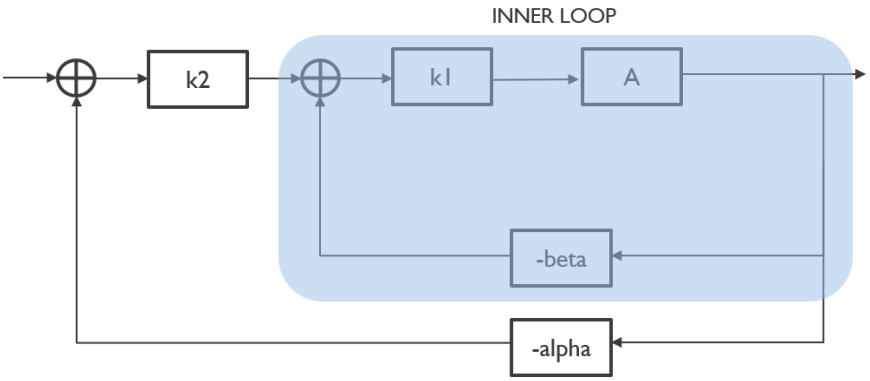


Figure 29: Block diagram of the multi-loop structure

As shown in this block diagram, two loops are presented. The inner loop is a basic feedback system. According to the analysis of the last part of Section 3.3.2, this inner loop system could achieve a transfer function of Q reach up to around 1.5 while maintain a good stability performance as shown in Fig. 26 and Fig. 27. Then, this inner loop can be considered as a black box with transfer function A. Together with another outer feedback loop, the previous analysis on a single loop feedback system can be repeated. With a higher open-loop system quality factor Q_A, the final quality factor of this closed-loop system can be boosted further without sacrificing the phase margin. Note that before checking the phase margin of the outer loop, the stability of the inner loop must get verified and fixed.

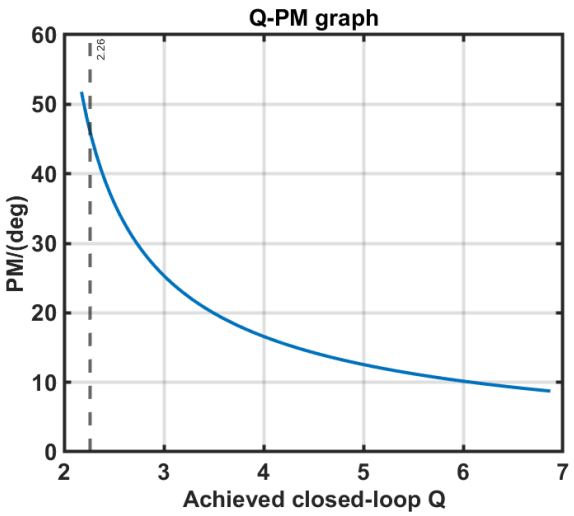


Figure 30: Simulated Q-PM graph of multi-loop system

The MATLAB simulation result of this multi-loop structure is shown in Fig. 30. Compared with the achieved Q-PM chart of a single-loop system, the closed-loop Q can easily reach up to 2.26, while

PM is still larger than 45. Thus, a feasible solution is proposed to break the trade-off between Q and PM.

A novel GM-C BiQuad structure based on the above-mentioned multi-loop idea is proposed and implemented in this thesis project. The detailed block diagram of this BiQuad structure is presented in Fig. 31.

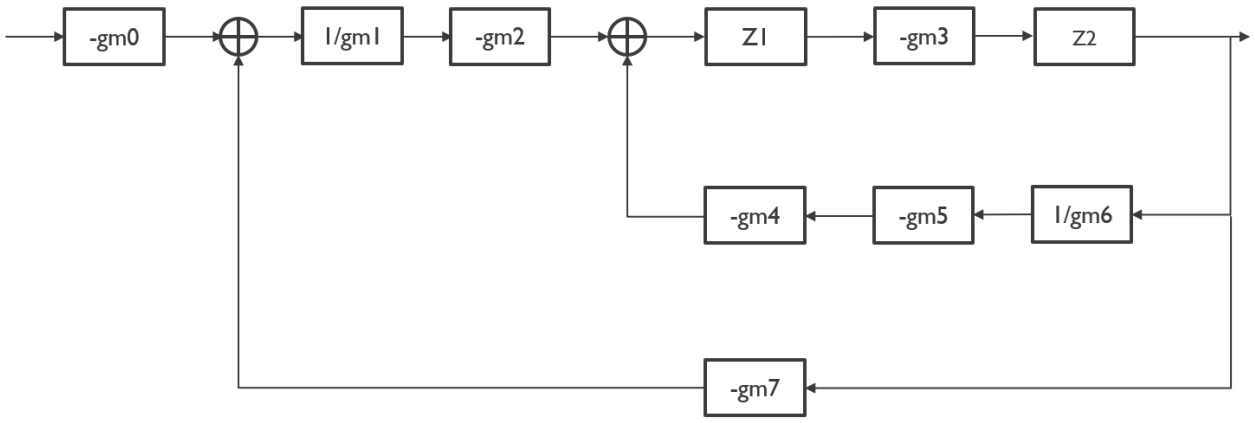


Figure 31: Block diagram of the proposed closed-loop BiQuad

This architecture is named "closed-loop BiQuad" because the conventional GM-C BiQuad is considered as a relatively "open-loop" option compared with an active-RC filter. With an intentionally added loop, this structure is then called a "closed-loop" BiQuad filter. The inner loop is not exactly the conventional GM-C BiQuad as shown in Fig. 25. Since the previous BiQuad structure is an inverting filter, with an inverting GM cell in the feedback path of the outer loop, the loop gain of the second loop would become positive and form a positive feedback system. To avoid this, one possible solution is to add a GM-resistor pair introduced previously to the GM cell in the feedback path of the outer loop. This arrangement will invert the sign of the outer loop and finally switch the second loop gain into negative. However, this will lead to increased complexity and power consumption. Another solution is by moving the GM-resistor pair in the open loop path to the inner feedback path, as shown in Fig. 31. Thus, the loop gain of the inner loop is still negative, while the closed-loop gain of the inner loop becomes positive. In combination with the negative outer loop feedback path, the loop gain of the outer loop becomes negative and a negative feedback is formed. The second solution is adopted for its better power efficiency since no extra GM cells are needed. The transfer function of this block diagram is calculated in steps. Firstly, the transfer function of the inner loop is calculated as follows.

$$A_{in} = Z_1 \cdot Z_2 \cdot (-gm_3) \tag{43}$$

$$\beta_{in} = \frac{gm_4 \cdot gm_5}{gm_6} \tag{44}$$

$$\begin{aligned} H_{in}(s) &= k_{in} \times \frac{A_{in}}{1 - A_{in}\beta_{in}} = -\frac{gm_2}{gm_1} \times \frac{-gm_3 \cdot Z_1 Z_2}{1 + \frac{gm_3 gm_4 gm_5 \cdot Z_1 Z_2}{gm_6}} \\ &= \frac{gm_2 gm_3 gm_6}{\frac{gm_1 gm_6}{Z_1 Z_2} + gm_1 gm_3 gm_4 gm_5} \end{aligned} \tag{45}$$

Then, for the second outer loop, the open-loop transfer function A_{out} is the closed-loop transfer function of the inner loop calculated in equation 45. The final transfer function of this system is calculated below.

$$A_{out} = H_{in} \tag{46}$$

$$\beta_{out} = -gm_7 \tag{47}$$

$$\begin{aligned} H_{out}(s) &= k_{out} \times \frac{A_{out}}{1 - A_{out}\beta_{out}} = -gm_0 \times \frac{gm_2 gm_3 gm_6}{\frac{gm_1 gm_6}{Z_1 Z_2} + gm_1 gm_3 gm_4 gm_5 + gm_2 gm_3 gm_6 gm_7} \\ &= -\frac{gm_0 gm_2 gm_3 gm_6}{\frac{gm_1 gm_6}{Z_1 Z_2} + gm_3 \cdot (gm_1 gm_4 gm_5 + gm_2 gm_6 gm_7)} \end{aligned} \tag{48}$$

The final BiQuad topology is illustrated in Fig. 32, where the GM blocks are represented with real GM cells, and the impedance Z_1 and Z_2 are replaced with real circuit elements. Note that Z_1 consists of a capacitor, an equivalent negative resistor, and real resistors to increase the tuning range. Z_2 is still a single capacitor.

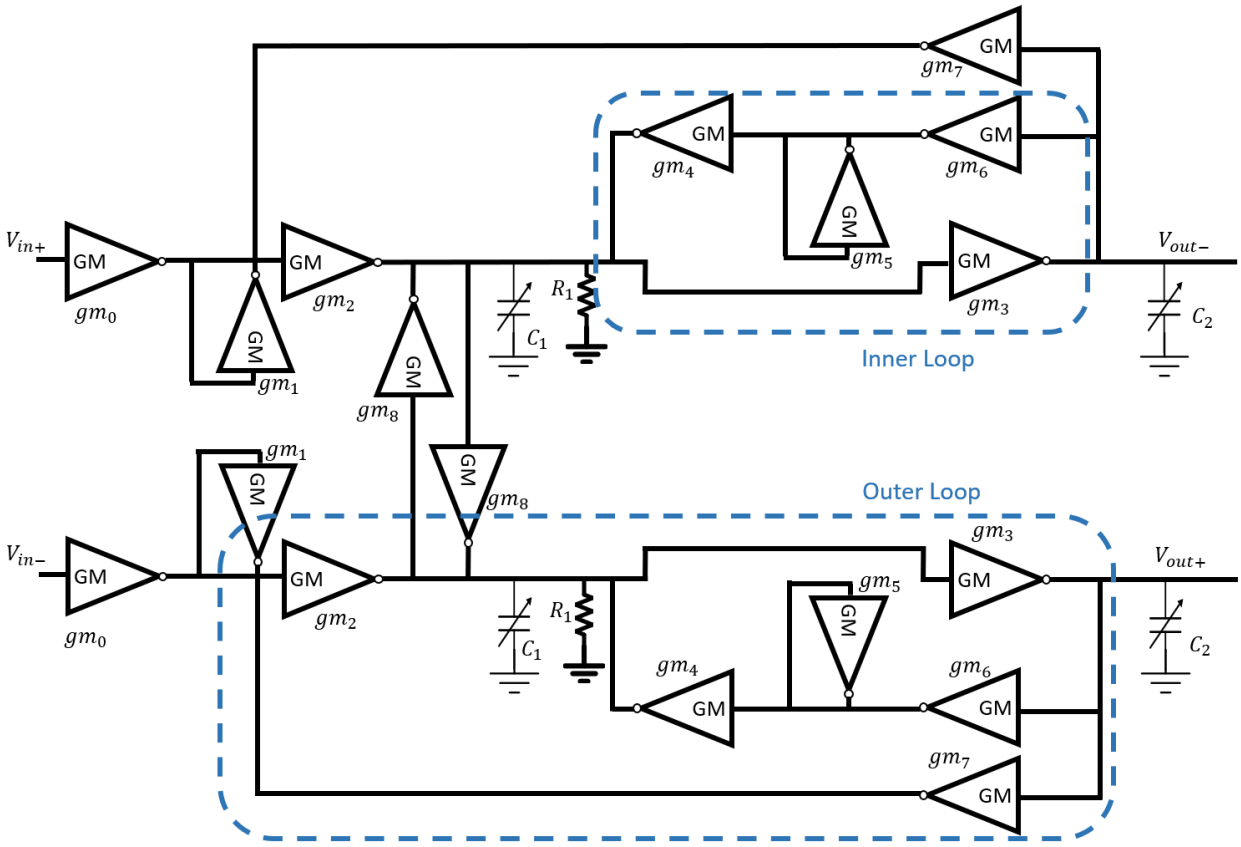


Figure 32: Proposed closed-loop BiQuad topology

By replacing Z_1 and Z_2 with circuit elements, the exact transfer function of this GM-C BiQuad can be obtained as calculated in equation 49.

$$H_{BQ}(s) = -\frac{gm_0gm_2gm_3gm_6}{\frac{gm_1gm_6}{\frac{1}{1/R_1-gm_8+sC_1}\cdot\frac{1}{sC_2}} + gm_3\cdot(gm_1gm_4gm_5+gm_2gm_6gm_7)}$$
$$= -\frac{gm_0gm_2gm_3gm_6}{gm_1gm_6C_1C_2\cdot s^2 + gm_1gm_6\cdot(\frac{1}{R_1}-gm_8)\cdot C_2\cdot s + gm_3\cdot(gm_1gm_4gm_5+gm_2gm_6gm_7)} \quad (49)$$

where the DC gain is:

$$|H_{DC}| = \frac{gm_0gm_2gm_6}{gm_1gm_4gm_5+gm_2gm_6gm_7} \quad (50)$$

The bandwidth as well as quality factor of this BiQuad are calculated below:

$$\omega_o = \sqrt{\frac{gm_3\cdot(gm_1gm_4gm_5+gm_2gm_6gm_7)}{gm_1gm_6\cdot C_1C_2}} = K\cdot\sqrt{\frac{1}{C_1C_2}} \quad (51)$$

$$Q = \sqrt{\frac{gm_3\cdot(gm_1gm_4gm_5+gm_2gm_6gm_7)\cdot C_1^2}{gm_1gm_6\cdot C_1C_2}}\cdot\frac{1}{\frac{1}{R_1}-gm_8} = K\cdot\sqrt{\frac{C_1}{C_2}}\cdot\frac{1}{\frac{1}{R_1}-gm_8} \quad (52)$$

The bandwidth and quality factor calculated above look similar to equations 28 and 29. However, this proposed BiQuad architecture has a multi-loop configuration and breaks the trade-off between Q and PM. With this BiQuad, Q can be easily boosted to the targeted 2.26 with PM still larger than 45 degree.

According to equations 51 and 52, the characteristics of the BiQuad are controlled by the capacitance C_1, C_2, the resistance R_1 and the transconductance values of all the GM cells. As discussed in Section 3.2, the structure has two extra transistors to switch on and off this GM cell. Thus, by putting several GM cells in parallel as one GM block and enabling part of them, the transconductance of this GM block can be then controlled digitally. The capacitors are digitally configurable as well. 16 capacitors are connected in parallel, corresponding to a 4-bit control word. Besides the capacitor, there is also a transistor on each parallel array to enable and disable this array. A similar idea is used to implement the configurable resistor R_1. The only difference is that the total capacitance would increase with more parallel cascading while the total resistance would decrease.

Although eight GM blocks, as well as capacitance and resistance are engaged in the control of BW and Q, making all of them digitally tunable would be redundant and power-wasting, increasing the system's complexity. The configuration of all those parameters are carefully designed such that the BiQuad can be tuned to the desired BW and Q (804.35 MHz and 2.2600) under different corners while keeping the complexity and power consumption minimum. The simulation results are presented in Section 3.5 where the layout of the LPF is implemented and simulation with all extracted parasitic has been carried out.

3.4 Fifth Order Gaussian Filter

As introduced in Section 3.1, the targeted filter shape is fifth order Gaussian-up-to-6dB filtering with 500 MHz bandwidth. This filtering is achieved by combining a single-pole TIA and two BiQuads. The second BiQuad is the bottleneck of this LPF since it requires the highest BW of 804.35 MHz and a high Q of 2.26. The requirement for the first BiQuad and TIA is more relaxed compared with the second BiQuad.

As a single-order filtering provider, there is no consideration of its quality factor needed during implementation. Furthermore, the targeted bandwidth, according to table 5, is as low as 332.5 MHz. Thus, the active-RC topology is used where the inverter-based amplifier only needs to achieve a gain bandwidth product of a few GHz. Unlike a conventional voltage-to-voltage active-RC filter, TIA is a current-to-voltage device since its name is transimpedance. Thus, the tunability of TIA is achieved by making the feedback impedance digitally configurable.
The closed-loop BiQuad topology proposed in Section 3.3.3 can be adopted as the first BiQuad as well. However, the whole transceiver's target performance is low complexity and high energy efficiency. Furthermore, the targeted Q value for the first BiQuad is 0.8334, which is relatively low. According to Fig. 26, with the conventional open-loop GM-C BiQuad structure shown in Fig. 25, the phase margin could still remain around 100 degrees with a Q value of 0.8334. Although this novel closed-loop breaks the Q-PM trade-off, the additional loop and GM cells increase the complexity and power consumption as well. Thus, to fit the target of energy efficiency, the conventional GM-C BiQuad structure, as shown in Fig. 24, is adopted as the topology of the first BiQuad in this LPF. The block diagram of the whole fifth-order LPF is shown in Fig. 33. The layout implementation, as well as simulation results, are illustrated in the next section.

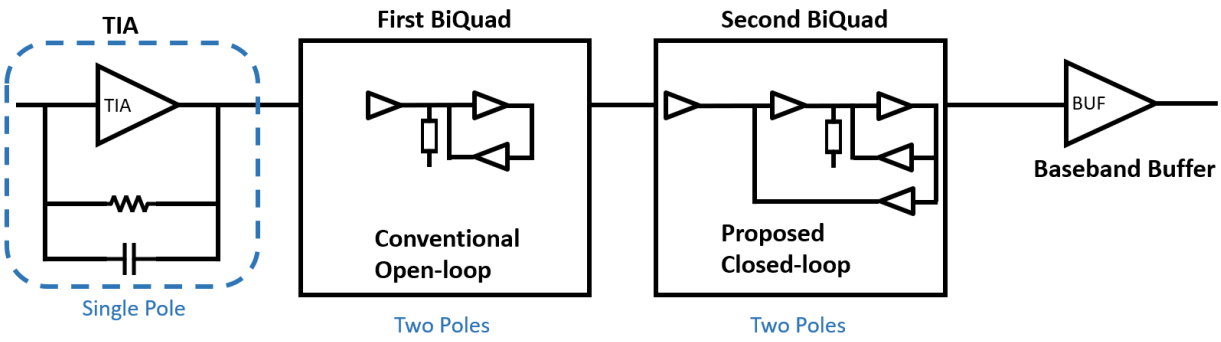


Figure 33: Topology of the fifth-order Gaussian-up-to-6dB filter

3.5 Layout Design

3.5.1 Low-parasitic Capacitor Array

As shown in equation 51, the scale of the BiQuad bandwidth is a few transconductance values of the GM cell times the geometrical mean of the two capacitors. While the GM cell transconductance value is 188 uS and the desired bandwidth is a few hundred MHz, their capacitor values for the second BiQuad would be around 100 fF. Since the capacitor is digitally tuned with 4 bits, the unit capacitance would be the whole capacitance divided by 2^4. Finally, the capacitance value of a unit capacitor or a single array capacitor is set to be 9 fF. It is a tough work to design such a small-value capacitor since normal parasitic is in fF level as well. In this project, the capacitor is achieved with multi-finger metal plates as shown in Fig. 34. The enable transistor is placed between one end of the capacitor and the ground to switch on and off this unit capacitor. However, even the ground is placed at merely the first and second metal layer, there are some parasitic capacitance between it and another end of the

capacitor, which will cause a non-zero switch-off capacitance and limited on-off ratio. By connecting 16 unit capacitors in parallel, the final capacitor for the second BiQuad is composed as shown in Fig. 36.

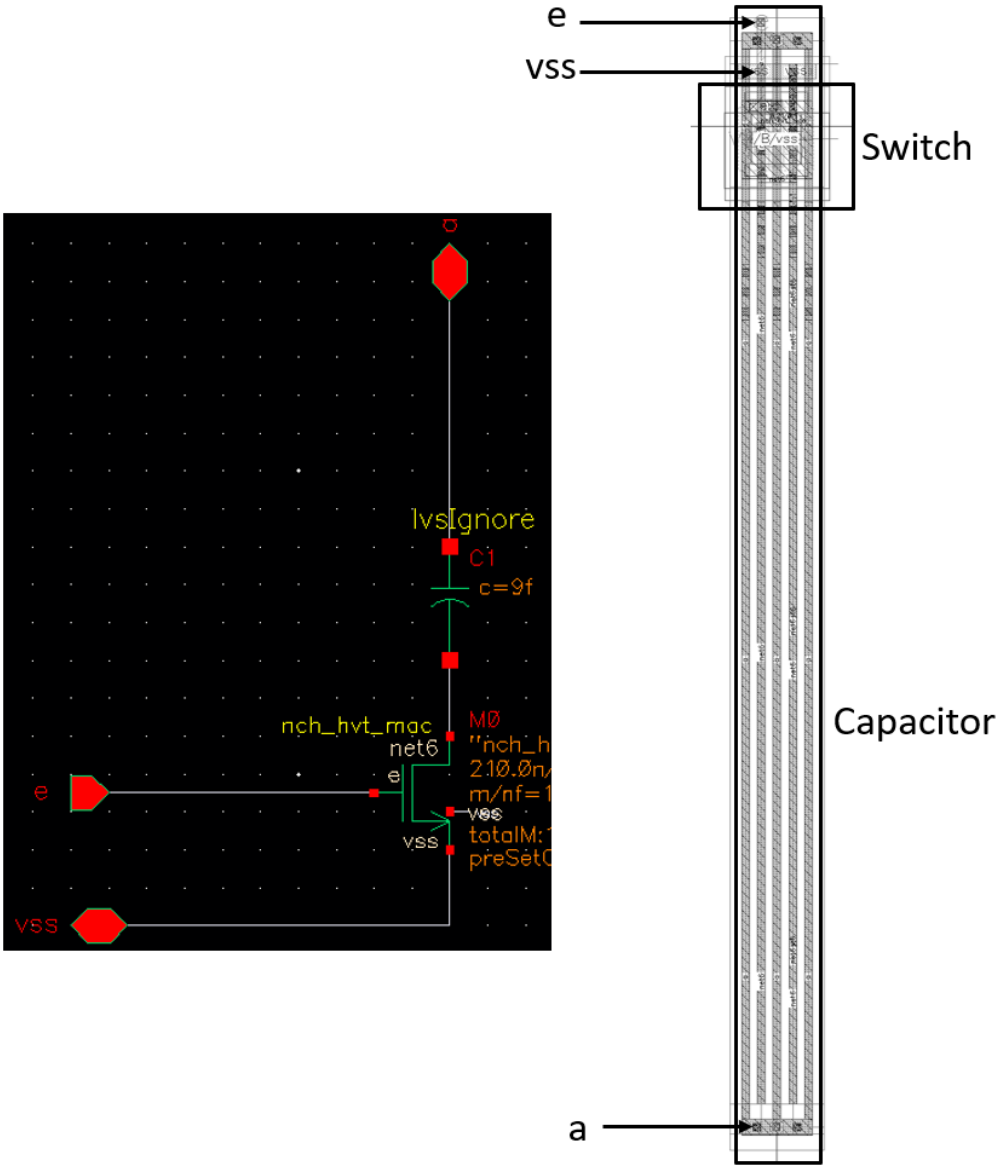


Figure 34: Unit capacitor for the second BiQuad

The situation is even worse for the first BiQuad. As introduced above, a conventional single-loop GM-C BiQuad structure is applied, which provides much less boosting to the open-loop bandwidth. Thus, the required capacitance for the first BiQuad capacitor is even smaller. In this thesis project, the unit capacitance for the first BiQuad is set to be 3.7 *fF*, which is smaller than the 9 *fF* used in the second BiQuad. Thus, the effect of parasitic capacitance is more severe. With the same layout design style, the off capacitance is simulated to be around 1.6 *fF*, which is larger than 1/3 of the on capacitance and results in a very limited on-off ratio of 2.32. Thus, a low-parasitic layout for first BiQuad unit capacitor is implemented as presented in Fig. 35. The ground plane is placed far away from the input node of the transistor to decrease the parasitic. The simulated off capacitance decreases to 0.56 *fF*. The whole capacitor array is illustrated in Fig. 36.

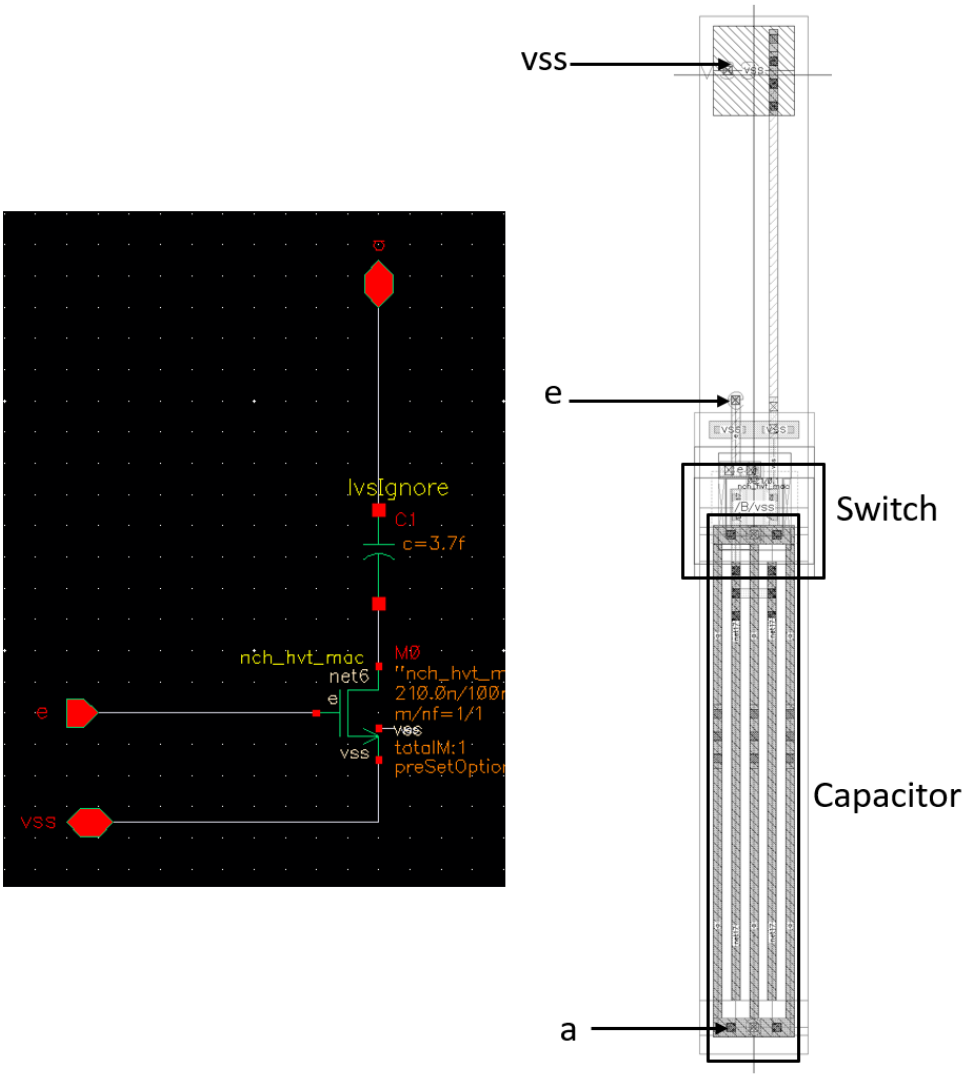
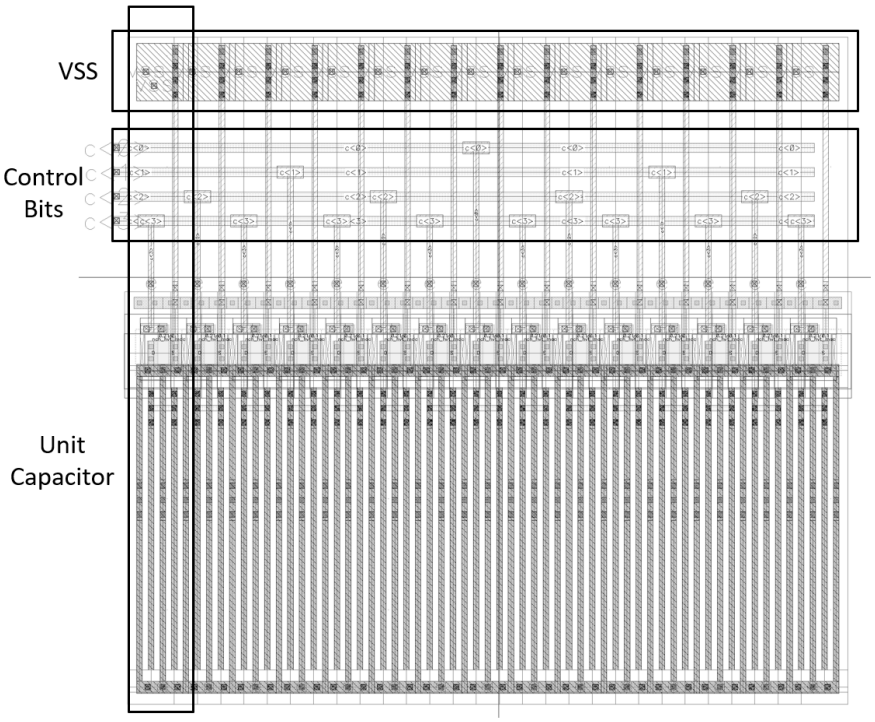
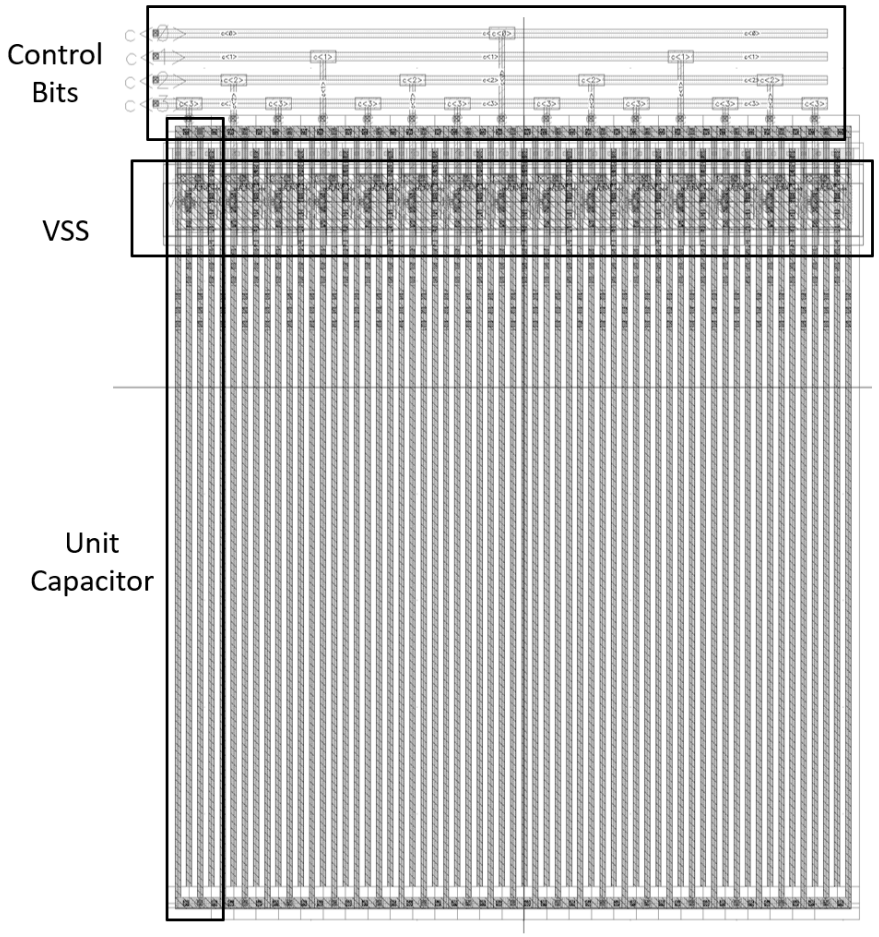


Figure 35: Unit capacitor for the first BiQuad



(a) BiQuad1 capacitor



(b) BiQuad2 capacitor

Figure 36: Full capacitor arrays for BiQuad 1 & 2

The simulation result of the capacitance value is illustrated in table 7 below. Ideally, the on-off ratio should be infinite, and the minimum capacitance of the capacitor array should be very close to zero. According to the simulation results in the table, the designed capacitors are far from ideal since their on-off ratio is limited to around 6.5 even with a low-parasitic design. However, this on-off ratio is large enough for this thesis project, with further optimization possible on this point in future work.

Table 7: *Simulation results of two BiQuad capacitors*

Section	BiQuad 1 unit capacitance*	BiQuad 2 unit capacitance*
Switch-on (fF)	3.6745	9.068
Switch-off (fF)	0.5630	1.381
On-off Ratio	6.5266	6.5662

*The capacitance are simulated with extracted parasitic from layout

3.5.2 Closed-loop BiQuad

With dedicated capacitors introduced in Section 3.5.1, the layout of the closed-loop BiQuad is implemented as shown in Fig. 37.

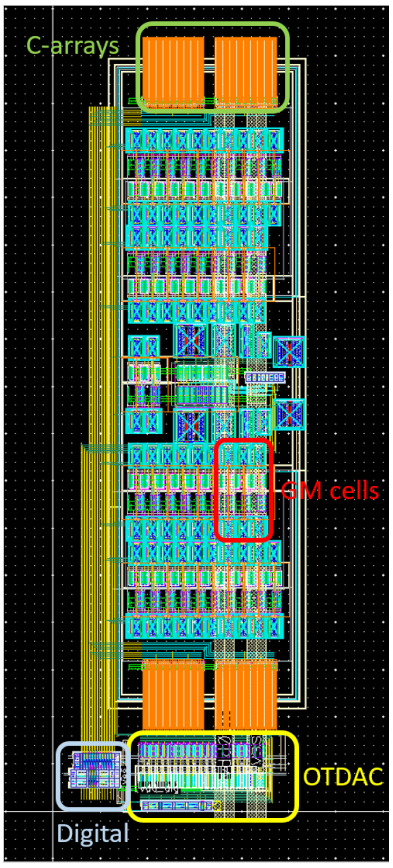


Figure 37: Closed-loop BiQuad layout design

As discussed in Section 3.3, this BiQuad is pseudo-differential. Thus, the layout is designed symmetrically along X-axis with all the GM cells densely placed. The capacitors are placed at the top and bottom of the cell for area efficiency. Finally, the offset-trimming DAC (OTDAC) and digital control block are placed for the performance tuning of the BiQuad, as shown in the layout figure.
The parasitic of this layout design is extracted, and then the performance of this layout is simulated. The target of this BiQuad design is to maintain the desired 800 MHz bandwidth and quality factor of 2.26 over all common corners. The simulation results are concluded in the following table.

Table 8: *Simulation result of proposed BiQuad under different corners*

Corner	**nominal/27°C**	**ss/-40°C**	**ss/120°C**	**ff/-40°C**	**ff/120°C**
Nbias code	8	8	8	11	12
LDO supply (mV)	819.2	898.3	866.8	785.2	785.5
Q	2.277	2.242	2.21	2.253	2.281
BW (MHz)	808.9	803.5	805.3	808.3	888.3
PM (deg)	72.48	92.25	75.37	79.38	60.33
C1 code	9	6	8	10	15
C2 code	13	4	10	10	15
Q code	2	7	2	1	1

According to the simulation results, the proposed closed-loop BiQuad has achieved the targeted performances and is tolerant to different corners. The only problem is that under fast-fast 120 °*C* corner, the BiQuad bandwidth would have an increment of around 10%.
While the tolerance to different corners is achieved by a wide tunability range, the BiQuad is tolerant to temperature and supply variance as well. The simulation results are shown in Fig. 38 and Fig. 39.

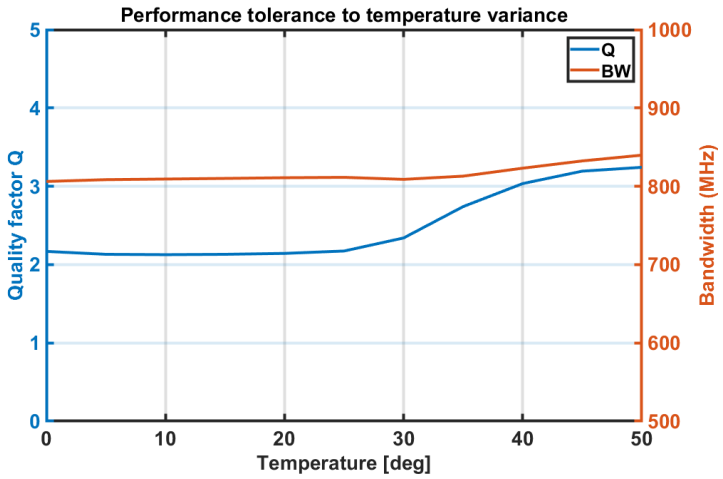


Figure 38: Performance tolerance to temperature variation

Instead of changing configuration bits to tune the performance back to the desired one, these simulations to temperature and supply voltage variations are carried out with the same bit setting. According

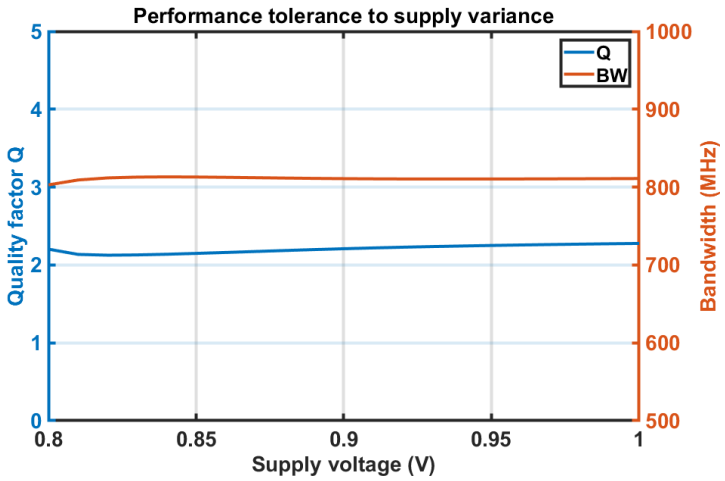


Figure 39: Performance tolerance to supply variation

to Fig. 38, the performance is almost constant when the temperature varies from 0 $^{\circ}C$ to 30 $^{\circ}C$. However, both Q and BW increase when the temperature rises above 30 $^{\circ}C$, and the amount of increment is acceptable. Fig. 39 shows the performance of the BiQuad with a 10 % variance in the supply voltage. Thanks to LDO, the supply level variance causes nearly no effect on the performance. Both Q and BW are almost constant over the supply variance.
The tunability range of Q and BW of this BiQuad is explored as well under the condition that the PM is larger than 45°. The simulation result shows that the available Q tuning range is from 0.856 to 3.22 while the BW range is from 441.3 MHz to 1.67 GHz. Thus, the Figure of Merit (FoM) of this BiQuad is calculated as follows.

$$FoM(BiQuad) = \frac{Power\ Consumption}{Number\ of\ Filtering \times Tuning\ Range} = \frac{0.385\ mW}{5 \times (1.67 - 0.44)\ GHz} = 115\ fW/pole/Hz \tag{53}$$

Based on the above-mentioned criteria, this BiQuad is compared with the state-of-the-art and the results are summarized in the following table 9.
Note that the quality factor of some papers shown in the performance table is filled with *NA*. This extraction is because those papers are not targeted to design a tunable Q LPF and the exact range of Q is not mentioned. However, since the conventional open-loop GM-C BiQuad structure is still used in those papers, the Q-PM trade-off discussed in Section 3.3 exists and limits the maximum Q to be around 1.4 in theory. The achieved normalized power or *FoM* is very low and is almost one-seventh of the lowest other work as far as the author could find. Besides, the high Q tuning range of this BiQuad provides the functionality to form complex filter types like Gaussian, Chebyshev, or Butterworth as well. All those characteristics mentioned above make it a prime candidate for low-power, high-BW complex filtering work.

3.5.3 Fifth-Order LPF

Similar to the closed-loop BiQuad presented in Section 3.5.2, the layout of the first BiQuad is designed in the same style as shown in Fig. 40.
Although this BiQuad is still in a conventional open-loop structure, the placement of OTDAC, digital part, capacitors, and GM cells are similar to the closed-loop BiQuad, while the connections between

Table 9: *Performance table of the proposed BiQuad*

Paper	BW (GHz)	Q	Power (mW)	Technology	Year	Type	*FoM**
This Work	0.44-1.67	0.86-3.22	0.385	28 nm	2022	GM-C	**115 f**
[38]	1.114	NA($\leq$ 1.4)	1.55	90 nm	2021	GM-C	0.7 p
[46]	0.015-0.095	NA($\leq$ 1.4)	14.2	500 nm	2009	GM-C	37.4 p
[47]	0.0022	2	0.3	40 nm	2019	GM-C	68.2 p
[40]	0.8-1.4	$\leq$ 1.258	24.2	180 nm	2006	GM-C	8.64 p
[48]	0.13-0.15	NA($\leq$ 1.4)	24	180 nm	2008	GM-C	10.67 p
[49]	1.5	NA($\leq$ 1.4)	11	65 nm	2015	GM-C	1.47 p
[50]	0.0002-0.04	NA	0.9	28 nm	2019	GM-C	7.5 p
[51]	0.24-0.5	NA($\leq$ 1.12)	4.1	180 nm	2010	Active-RC	1.36 p

*The unit is $W/pole/Hz$

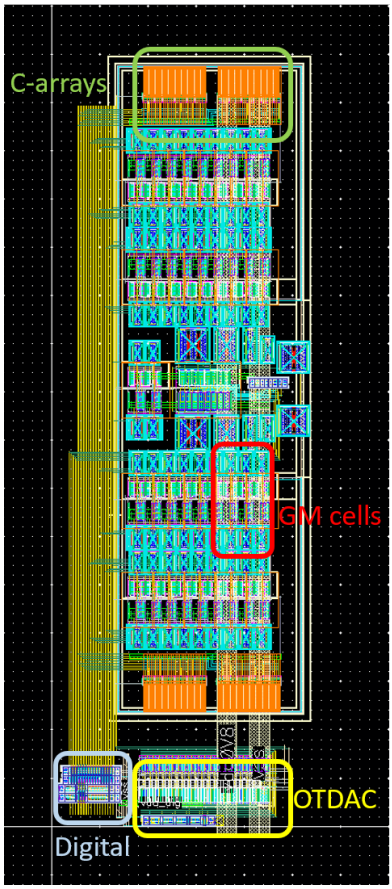


Figure 40: First BiQuad layout design

them are different. This feature is to promise the consistency of two BiQuads since they will be composed together to form the final LPF. The complete LPF layout is shown in Fig. 41. According to the topology shown in Fig. 33, the complete fifth-order filter consists of a differential TIA, which converts the input current into voltage while providing a single-order filtering. Then the differential signal will go through two BiQuads, with each of them consisting of second-order filtering. Since this filtering happens at the analog baseband, two identical but separate paths are needed for in-phase (I) and quadrature (Q) signals. Thus, in the layout shown in Fig. 41, four BiQuads are used in total. Besides BiQuads and TIA, the LDO, as well as many decoupling capacitors, are presented in the layout as well.

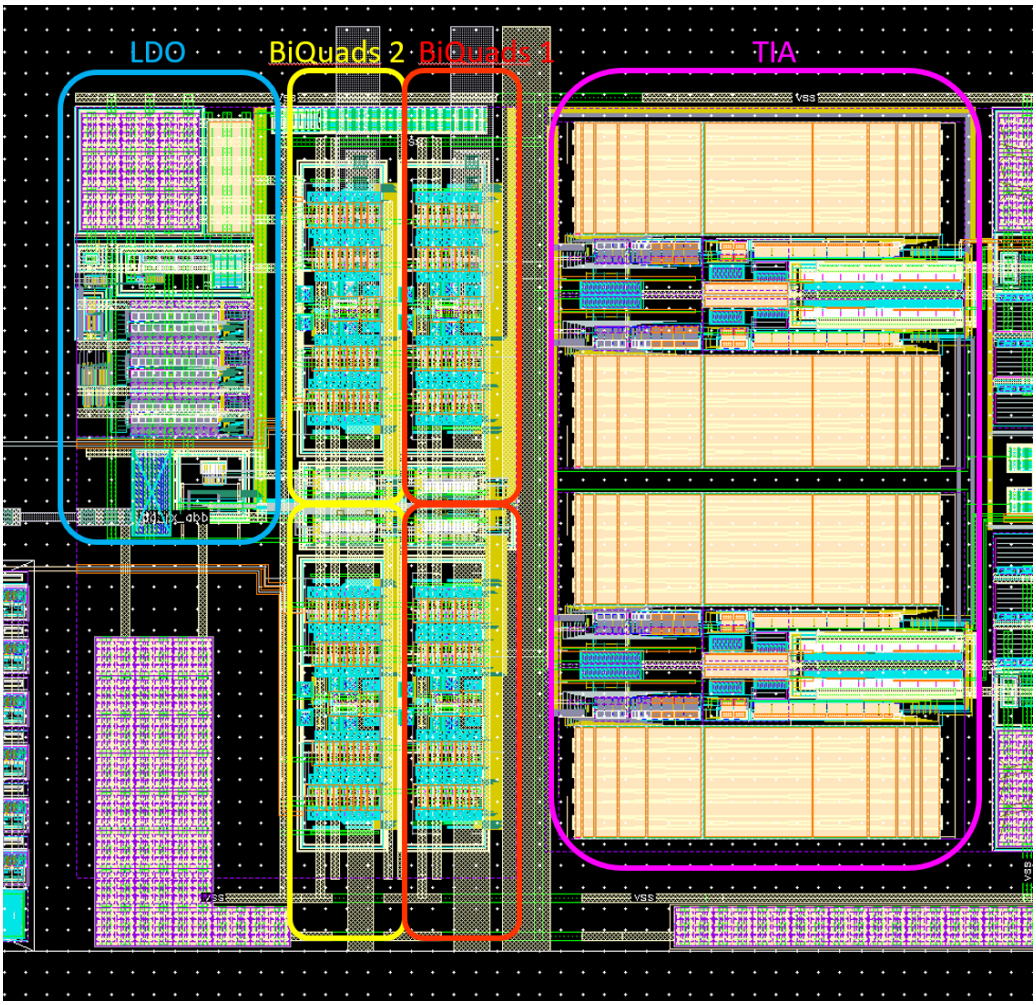


Figure 41: Layout design of the complete LPF

The simulation of this fifth-order filter has been carried out with the extracted parasitic of the above layout design. The simulated filtering shape is shown in Fig. 42, while the group delay is simulated and presented in Fig. 43. The simulated filtering shapes are compared with the idea Gaussian-up-to-6dB curve, illustrated in red in Fig. 42. According to the results, the curve with a high LPF gain setting is almost the same as the theoretical line. While the unity-gain setting curve shows some deviations at high frequencies up to 10 GHz. This phenomenon is due to the limited bandwidth of the GM cell, which degrades the performance of the first BiQuad. When the LPF gain is set to be at a high value, this degradation is mitigated, and thus the high-gain curve is much more ideal. However, the second BiQuad with proposed closed-loop architecture achieves good performance in

unity-gain and high-gain settings. Fig. 43 indicates the phase performance of this filter. Within the band of interest, the group delay is almost constant, and the variation is within ± 0.23 ns, which is well behaved as expected. The power consumption is 1.57 mW at the unity-gain setting and 2.23 mW at the highest-gain setting.

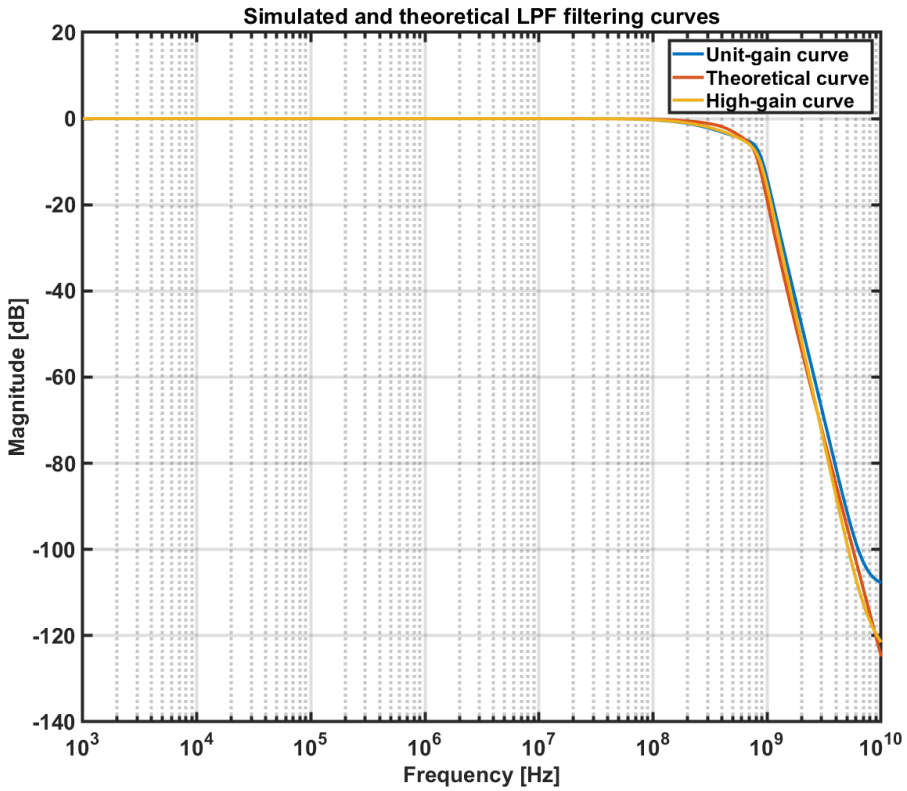


Figure 42: Simulated filtering curve of the fifth order LPF

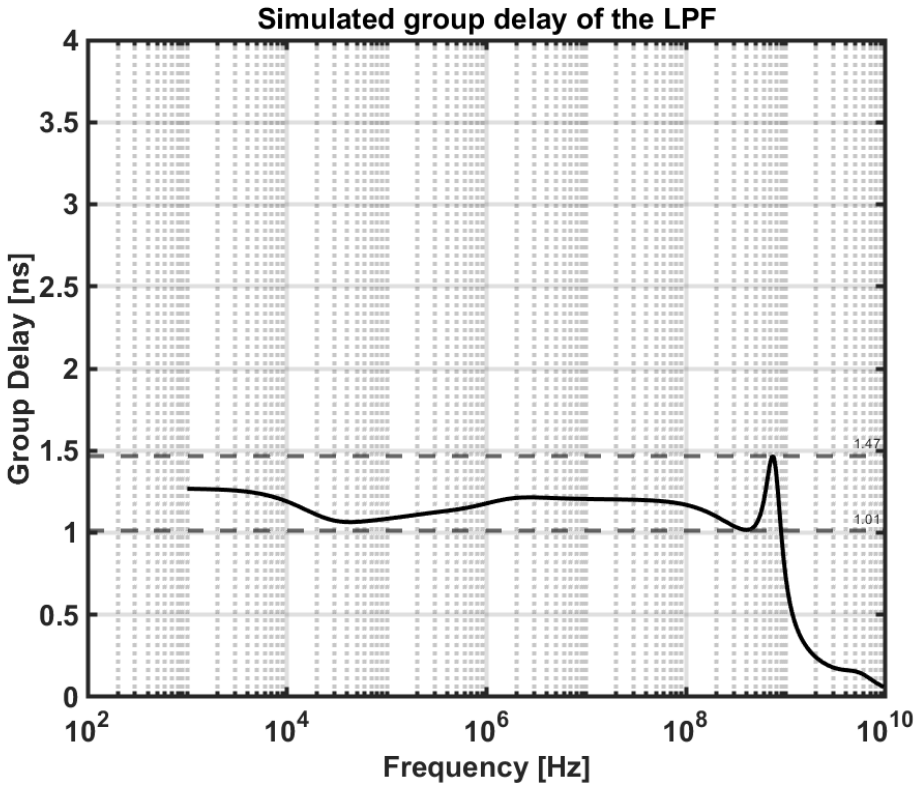


Figure 43: Simulated group delay of the fifth order LPF

4 The DSIC Design

As mentioned before, to achieve FD and RadCom, a strong and reliable self-interference cancellation is needed. Besides the passive EBD at the early front-end, a dedicated digital self-interference cancellation (DSIC) module is adopted as well. This module is implemented and modified based on the all-digital spillover cancellation method proposed in Sander Heijmans' master thesis project [20] and will be introduced in this chapter.
In the following Section 4.1, the idea of digital-controlled cancellation is discussed. In Section 4.2, the schematic-level implementation of DSIC is introduced. Finally, the DSIC layout design is presented in Section 49.

4.1 Digital-controlled Cancellation

It can be implemented both at the RF and BB parts as an active cancellation method. As stated in the thesis [20], the RX would saturate after the LNA without cancellation. Thus, the active RF cancellation is implemented.
Both analog feedback loop and digital-controlled method are possible options for the active RF cancellation scheme. Due to generated exact amplitude, the analog feedback loop outperforms its counterpart in spillover cancellation. However, it would be very challenging to implement the delay with this method. Furthermore, the high power consumption, as well as complexity, are not preferred in this project. Finally, the second option is considered more promising. The following figure Fig. 44 shows the block diagram of the DSIC method in [20].

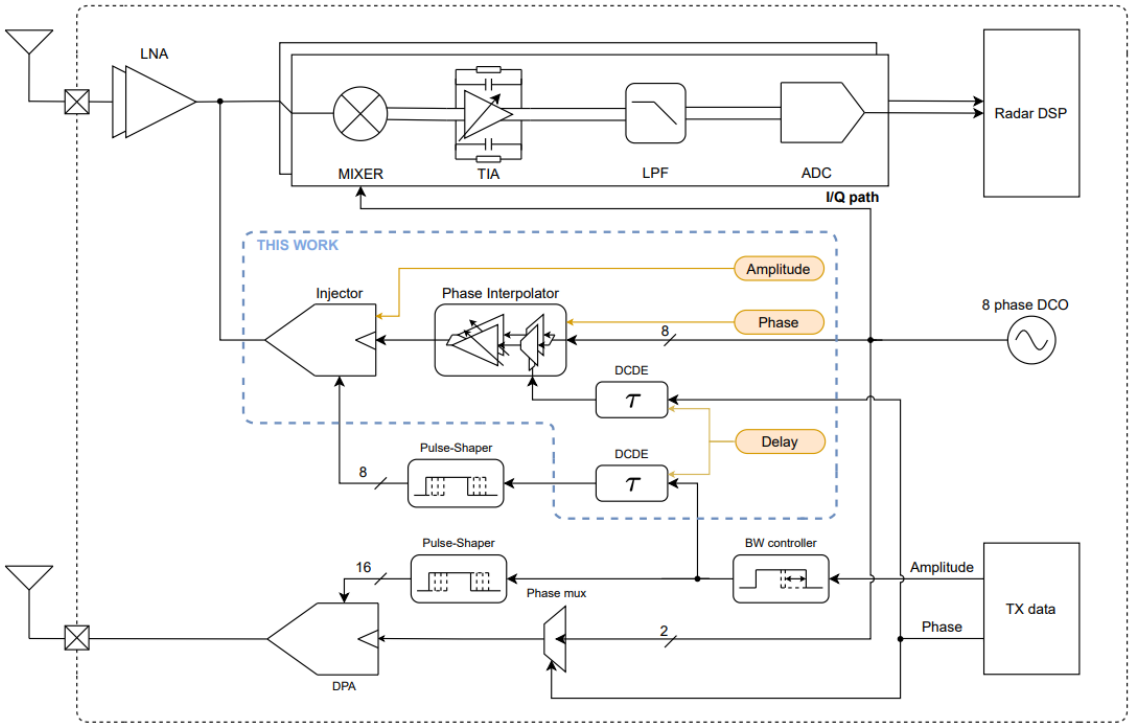


Figure 44: Proposed DSIC architecture in [20]

In this DSIC method, the same hybrid-modulation polar transmitter is considered. The main idea is to create a delayed phase-opposite cancellation signal with respect to the spillover signal to cancel it. Unlike the signal generation on the TX side, the cancellation signal is delayed and converted to a

current signal in order to be injected into the LNTA output to eliminate the spillover signal. Not only the time delay, but also the phase and amplitude of the cancellation signal can be controlled digitally to achieve the best cancellation performance. However, this DSIC module is not compatible with this thesis project. Further implementation, as well as redesign, are necessary to get it adopted in this transceiver.
According to simulations, the largest spillover signal is through the TX's power amplifier (PA), and the path is on-chip. Thus, it would be redundant to use multiple delay cells. Furthermore, the phase control in the thesis [20] is dedicated to BPSK, where 8-PSK is actually used in this TRX. Thus, the redesign of the phase selector is required. Besides, the digital interpolation blocks on the phase and amplitude of the cancellation signal are implemented to further optimize the cancellation performance.

4.2 Top Schematic

The redesigned DSIC block diagram is shown in Fig. 45 below, where the TX part is in brown, the RX part is in grey, and DSIC blocks are in red. Note that the digital interpolation blocks for phase and amplitude are in black. The basic idea of this DSIC module is still the same as the one in [20], which is to generate a delayed and phase-opposite signal for cancellation. However, the detailed implementation has been redesigned and modified.

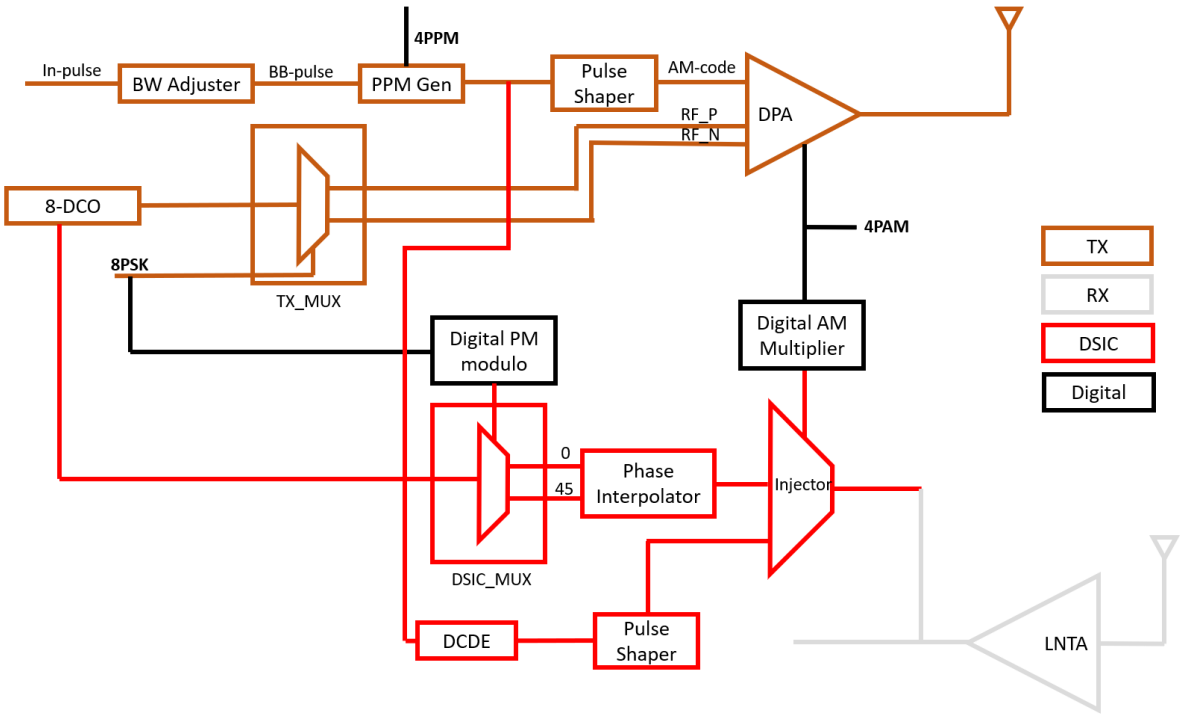


Figure 45: Proposed DSIC block diagram

Unlike the DSIC shown in Fig. 44, the 8-PSK signal, as well as 4PAM signal, are fetched from TX but not directly injected into the DSIC. A digital PM modulo is used to manipulate this PM signal such that the output PM signal could result in the correct phase information for the cancellation signal. Similarly, a digital AM modulo or multiplier is implemented to set the correct AM code for the cancellation signal. With the digitally corrected PM signal, a multiplexer DSIC_MUX is used to

select the signal with the corresponding phase from the 8-phase signal from 8-DCO. Furthermore, this multiplexer also outputs another signal with a plus 45° phase difference. The two signals with phase differences are inserted into the phase interpolator, where it can output a signal with a phase between the phases of the two input signals. The phase interpolator is tuned with a 4-bit control word, thus, the phase interpolation resolution is 2.8°. Similar to TX, the same staircase envelope is generated by pulse shaper with a tunable delay provided by the digital-controlled delay element (DCDE). However, the input AM code is taken from the node after the PPM generator where the TX PPM data is already encoded. Finally, the injector produces the cancellation signal where the RF signal is the output of the phase interpolator, the corrected PAM signal controls the amplitude strength, and the envelope is generated by the pulse shaper mentioned above. Unlike a digital PA (DPA) used in TX, the injector output is in the current domain and can be directly injected into the LNTA output to eliminate the spillover signal.

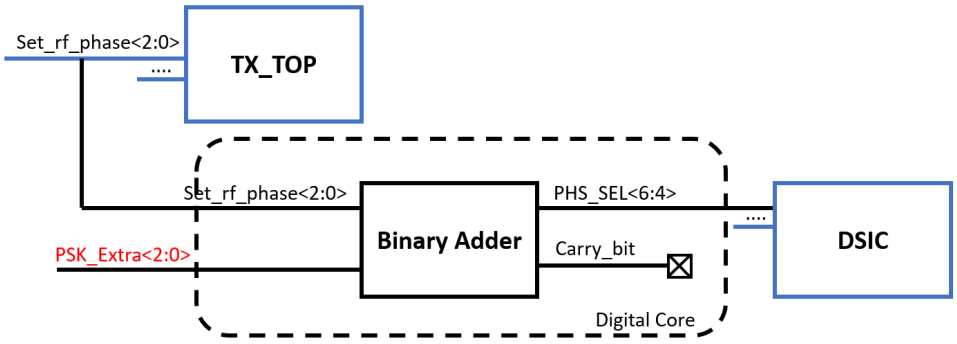


Figure 46: Digital PM modulo logic

The operation logic behind the digital PM modulo is shown in Fig. 46, and the basic idea is simple. As shown in this figure, the 8-PSK code, i.e., $Set\_rf\_phase< 2:0 >$, from TX is added with an extra control bits, i.e., $PSK\_Extra< 2:0 >$. The extra bit is used to control the amount of shift between the input TX 8-PSK code and output 8-PSK code used in DSIC. Ideally, if the spillover is in phase with the TX signal, the shift should be 4, resulting in an exact 180° phase difference between the two 8-PSK codes. Various extra bits values could be applied under different application cases.

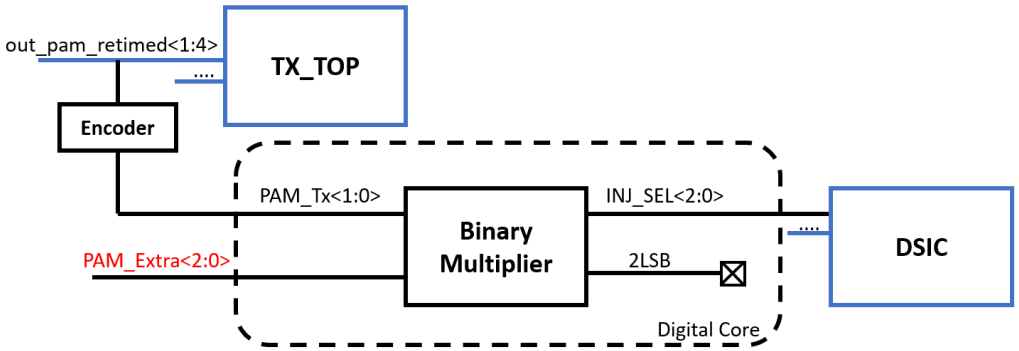


Figure 47: Digital AM modulo logic

Similarly, the AM code is interpolated by another extra bits, i.e., $PAM\_Extra< 2:0 >$, as well. However, the logic behind this AM modulo is scaling instead of linear shifting used in PM mod-

ulo. The PAM code from TX, $PAM\_TX<1:0>$, is linearly related with the PAM code for DSIC $INJ\_SEL<2:0>$. Although the spillover from TX to RX is more like a stochastic process in the time domain, the spillover amplitude is more deterministic. In other word, the actual spillover arrived at the RX may have some unknown phase different from the TX signal, which is handled by the digital PM modulo, the spillover signal amplitude is closely related to the amplitude of the TX signal. Once the TX PAM code is increased twice, not only the TX signal amplitude but also the spillover amplitude will increase twice. Thus, the DSIC PAM code is a kind of scaled number of the TX PAM code with specific scaling factor. This scaling is achieved with a binary multiplier, as shown in Fig. 47. Since the DSIC PAM code is also 3 bits, the 2 LSB of the multiplication result are discarded. Note that the TX PAM code is already decoded into thermo-code, i.e., $out\_pam\_retimed<1:4>$. Thus, an encoder is required to convert it back to binary and do further multiplication.
The two modulo, as mentioned above, are implemented in the digital core of this chip.

4.3 Layout Design

The layout of this DSIC is implemented and shown in the Fig. 49 below. Note that the phase selector contains the multiplexer DSIC_MUX and the phase interpolator shown in the DSIC block diagram in Fig. 45. All blocks are densely placed to reduce the total area of DSIC since it will be placed between TX and RX. The simulation result of this design shows that approximately a 30 dB cancellation can be provided with 3.7 mW power consumption. The Radar functionality of this DSIC module is simulated with Simulink, as shown in Fig. 48. With this DSIC, the ghost target caused by the TX-to-RX spillover is eliminated and the RadCom function can be achieved then.

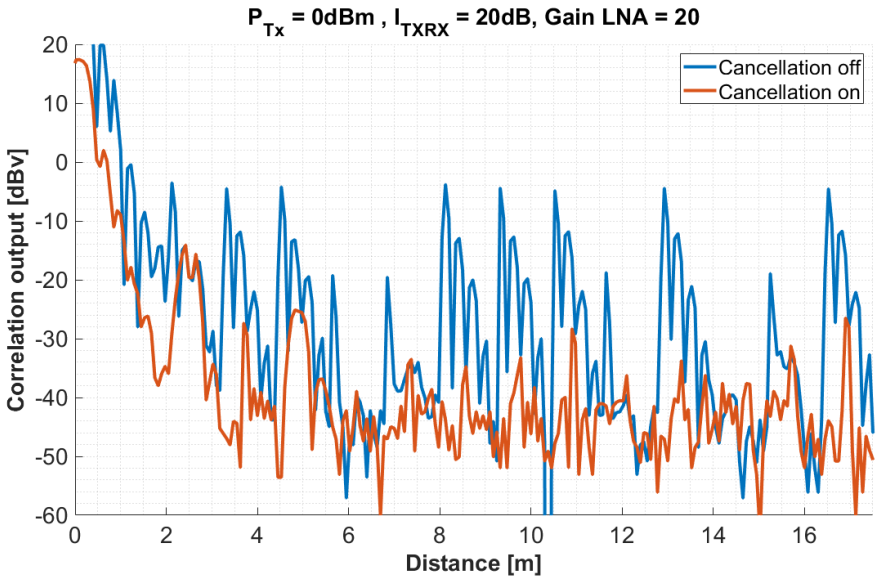


Figure 48: Simulation result of DSIC

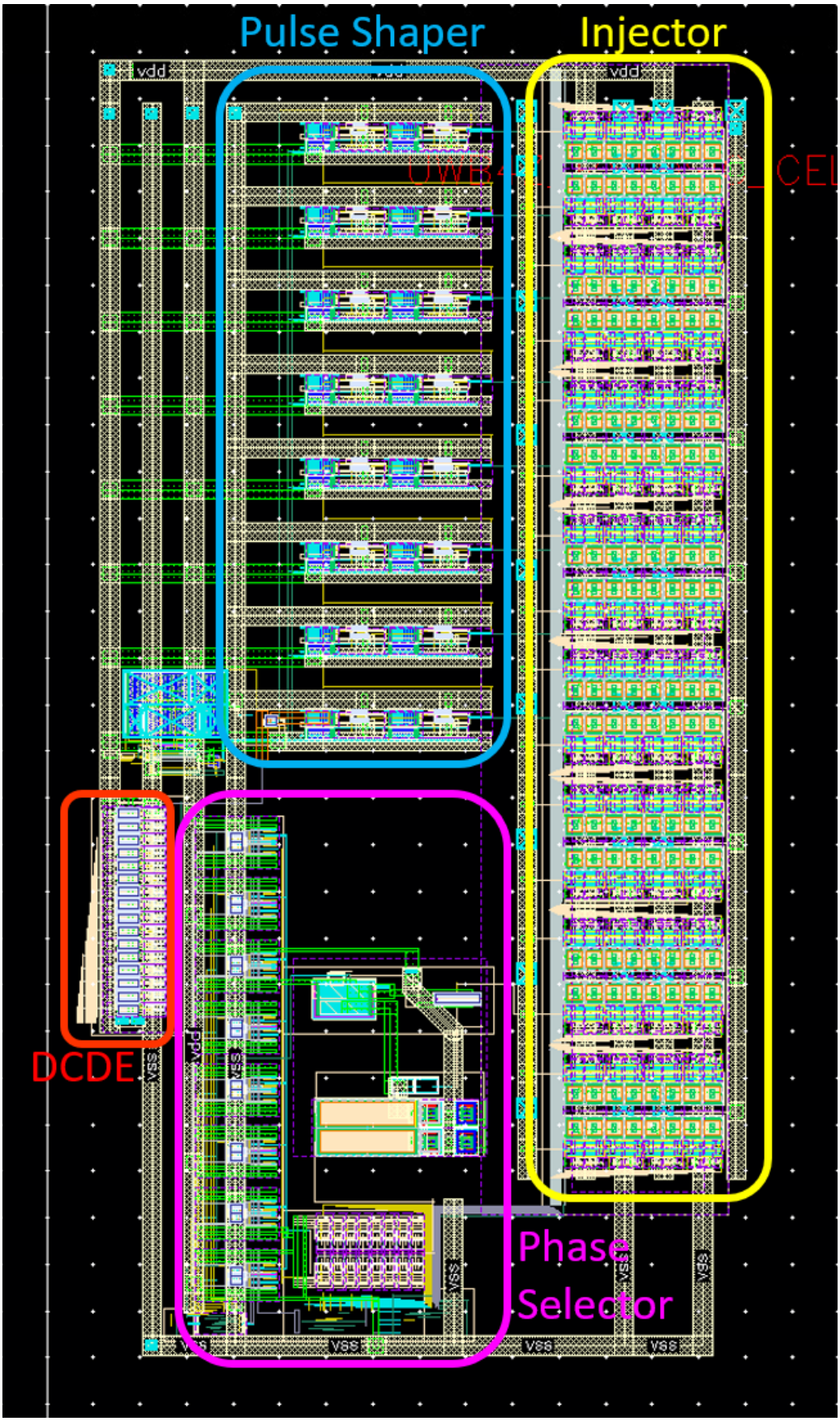


Figure 49: Layout design of proposed DSIC

5 System-level Design

5.1 Receiver Design

The final receiver consists of an LNTA, a mixer, LPF discussed in Chapter 3, and a baseband buffer. A common-gate LNTA is used with an inverter stage to provide higher gain. The mixer is a simple single-balanced passive 25% duty cycle non-overlapping IQ mixer. The baseband buffer provides sufficient output current and is impedance matched so that its output can directly connect to external devices like an oscilloscope. The layout implementation of this receiver is shown in Fig. 50 below.

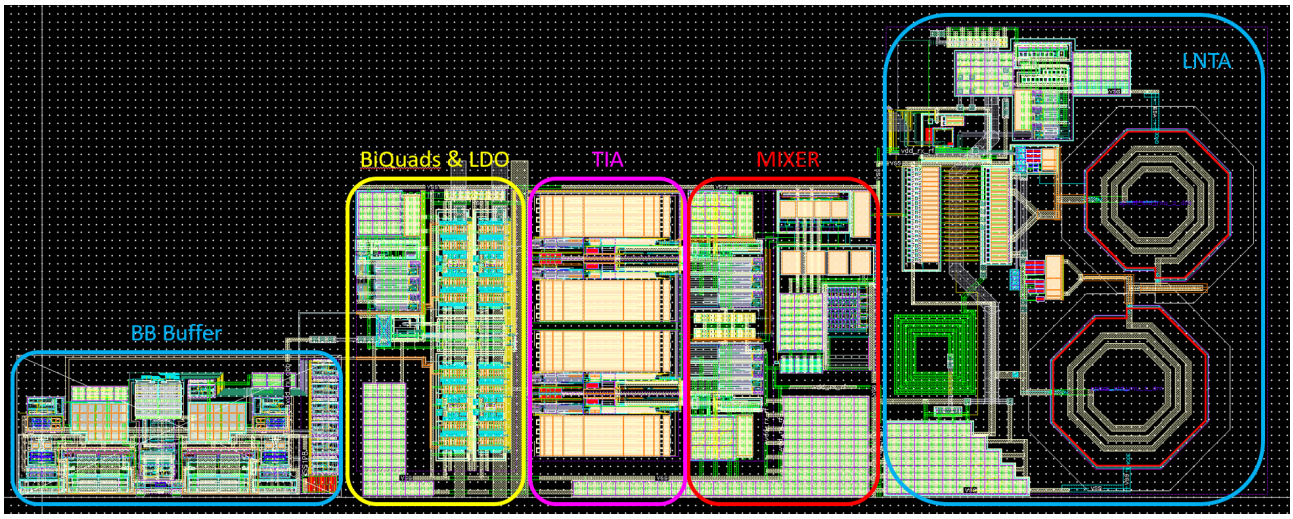


Figure 50: Layout design of proposed receiver

With this layout design, not only the filtering characteristic, other performances are simulated and concluded in the table 10.

Table 10: *RX Performance Table*

Corner	nominal/27°C
Noise Figure* (dB)	5.499
Supply Voltage (V)	0.9
RF Part Power (mW)	8.276
Baseband Part Power (mW)	1.624
S_{11} (dB)	-14.15
$P1dB_{output}$ (dBm)	0.353
Sensitivity (dBm)	-59.3

*Double side band NF integrated from 1 to 500 MHz

5.2 Transceiver Design

This IR-UWB transceiver consists of the transmitter presented in Chapter 2, the receiver introduced in Section 5.1 above, an electrical balanced duplexer (EBD), and DSIC implemented in Chapter 4. The block diagram is shown in the following Fig. 51.

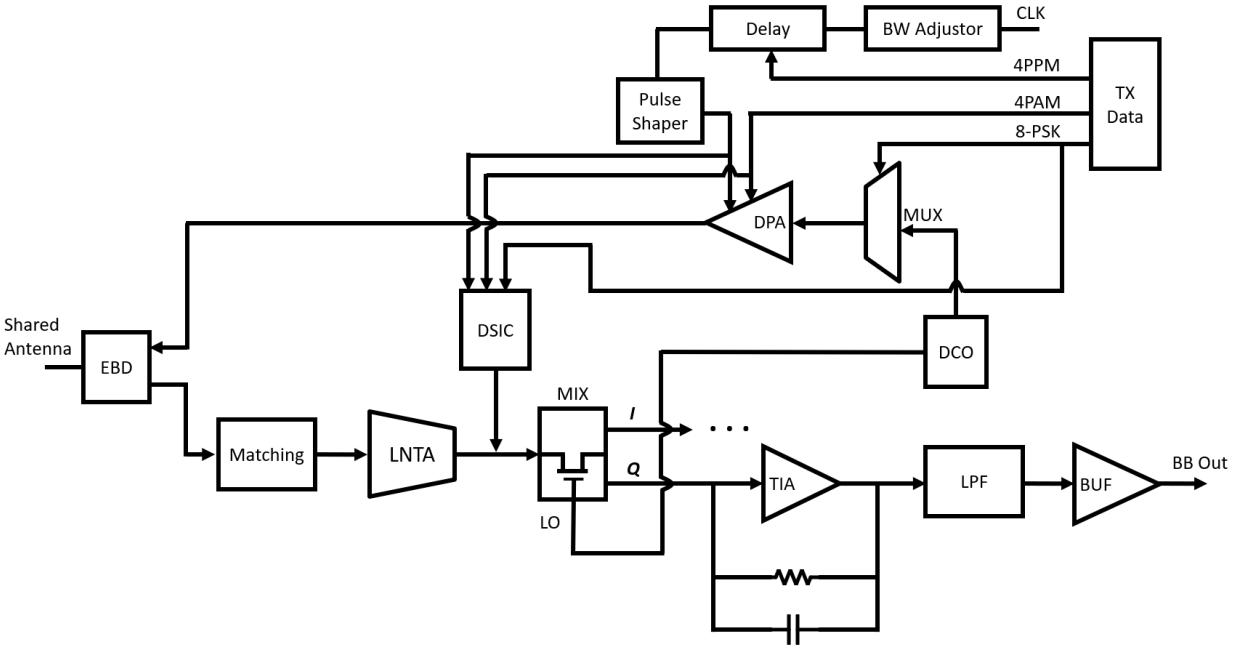
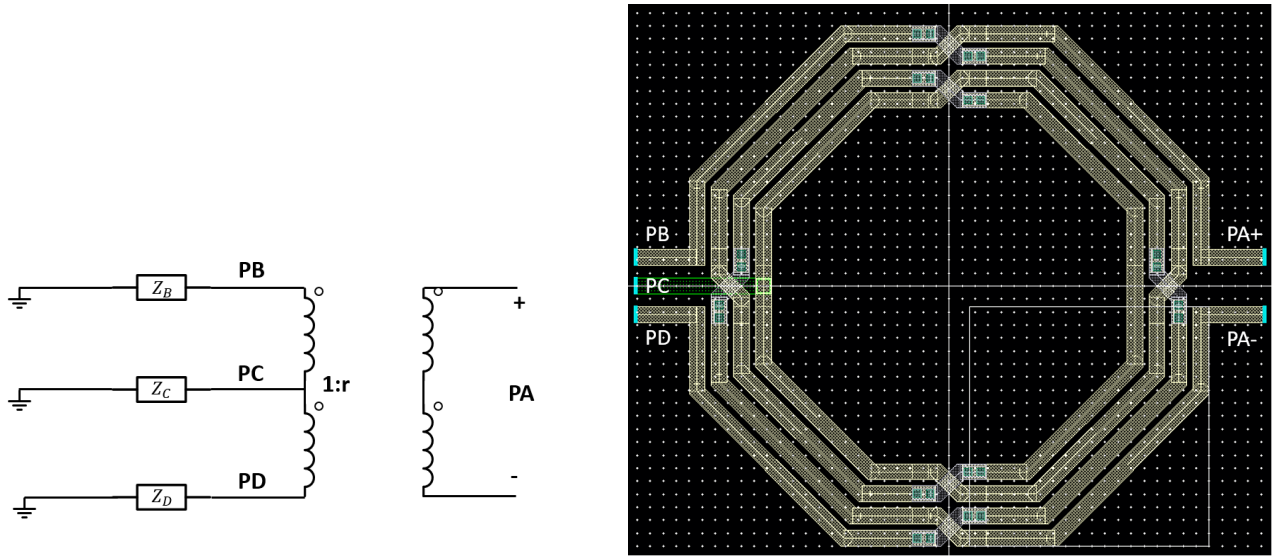


Figure 51: Proposed IR-UWB transceiver block diagram

The EBD used in this TRX is a hybrid transformer. Its equivalent schematic and layout design are shown in Fig. 52 below. There are four ports in EBD: one differential port P_A and three other single-ended ports. Its differential port is connected to the differential output of PA in TX. P_B is connected to the antenna shared by TX and RX. P_C is attached to the LNTA input while P_D is loaded with a balanced impedance Z. This EBD provides decent isolation between P_A and P_C, while a 3 dB insertion loss is presented. Simulation result shows a TX to RX isolation of -60 dB with 50 Ω impedance and -19.07 dB with a commercial dual patch antenna. This simulation is carried out at 8 GHz.
Finally, the layout of this complete IR-UWB transceiver is implemented and illustrated in Fig. 53. As presented in the layout, the balanced impedance connected to P_D of EBD is implemented with a configurable load. This load consists of an inductor as shown on top of the EBD. DSIC is placed between TX and RX to facilitate the spillover cancellation function. At the left lower corner, a standalone BiQuad block is implemented to check the BiQuad performance individually. This block consists of the proposed novel BiQuad and a baseband buffer. Finally, the performance of this transceiver is simulated and included in the following table 11.
As shown in this table, this transceiver achieves a high data rate of 1.66 Gbps while the total power consumption is limited to 19.59 mW. Thus, the energy efficiency is quite high. Furthermore, the adoption of EBD and DSIC facilitates the full duplex and RadCom functions as well. Thus, the targeted performance as an energy-efficient high-speed full-duplex IR-UWB transceiver with RadCom has been achieved. Further system-level implementation includes pad-ring design, floor plan, sealing, and dummy-filling. Those processes are briefly introduced in the appendix at the end of this thesis.



(a) EBD schematic (b) EBD layout

Figure 52: Equivalent schematic and layout implementation of EBD

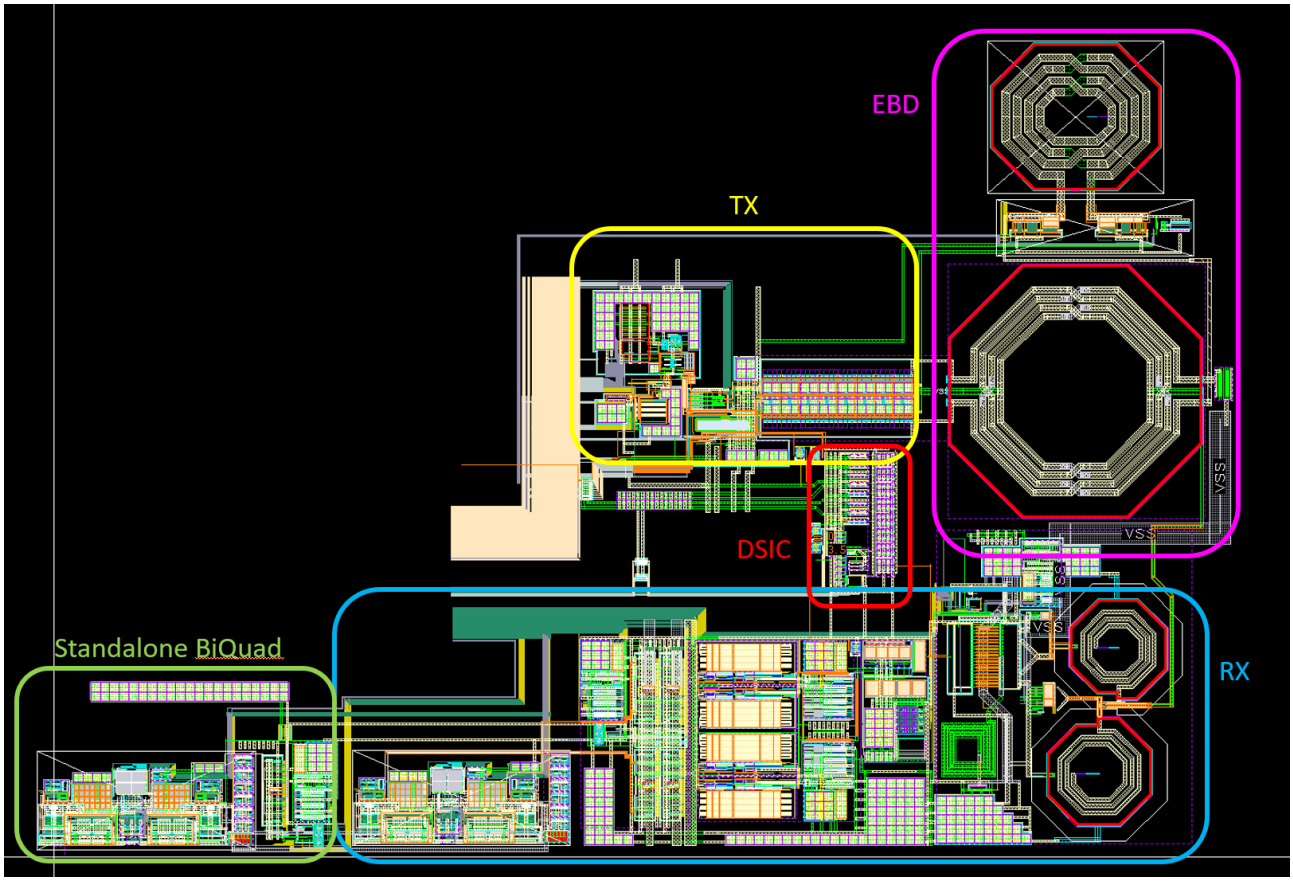


Figure 53: Layout implementation of the proposed IR-UWB transceiver

Table 11: *IR-UWB TRX Performance Table*

	This Work	**ISSCC 21**	**JSSCC 16**	**JSSCC 16**	**TCAS-I 19**
Technology (nm)	28	65	65	180	130
Frequency Band (GHz)	6-9	3.5-6	6.25-8.5	3-5, 7-9	3.5-4.5
Modulation	**Hybrid**	E-PPM	QPSK	BPSK	OOK
Duplex	**Yes (FD)**	No	No	No	No
Data rate (Gbps)	**1.66**	1.125	1	1	1
Sensitivity (dBm)	-59.3	-68	-69	-74	-38
SIC Isolation (dB)	**30**	-	-	-	-
Power Consumption (mW)	19.59*	28	432	72.9	120
Max Distance (m)	0.75	2	2	1	0.2
Energy Efficiency (pJ/bit/m)	**15.7**	24.9	432	102.2	120
BER	$\leq 1^{-4}$	$\leq 1^{-3}$	$\leq 1^{-3}$	$\leq 1^{-3}$	$\leq 1^{-3}$
RadCom	**Yes**	No	No	No	No
Reference	-	[52]	[53]	[54]	[55]

*Baseband buffer power is excluded

6 Conclusion

6.1 Master Thesis Conclusion

In this master thesis project, a transceiver utilizing IR-UWB technology is designed for short-range, high data-rate, and low power applications. A hybrid modulation scheme facilitates the data rate and communication range. Besides, active and passive self-interference cancellation methods are implemented in this transceiver to eliminate transmitter-to-receiver spillover, which enables full-duplex and simultaneous radar and communication.
As the hybrid modulation scheme is used, the digital polar architecture is implemented for the transmitter, and a differential I/Q coherent receiver architecture is designed. With a high data rate, the signal bandwidth is as large as 1 GHz, which makes wideband LPF the bottleneck of this receiver. A novel closed-loop GM-C BiQuad is proposed and implemented to form the desired fifth-order LPF. With the closed-loop architecture, the trade-off between stability and high-quality-factor has been broken up, which is an inevitable drawback for conventional open-loop GM-C BiQuad. With this new BiQuad, a fifth-order Gaussian-up-to-6dB filter is implemented and simulated, where the filtering shape is very close to the ideal curve and variation of group delay is within ± 0.23 ns. The achieved power consumption of this complete LPF is as low as 1.57 mW.
The implementation of DSIC provides isolation of around 30 dB between TX and RX. As an active cancellation module, it eliminates the spillover at the early RF part. Digital PM and AM modulo are implemented to interpolate the 8-PSK and PAM codes from TX and output correct codes for cancellation. With the corrected codes, DSIC produces a cancellation signal with the same amplitude and opposite phase of spillover and injects it into the LNTA output of the RX.
This transceiver is designed and fabricated in TSMC 28 nm CMOS process. The chip has a small form factor with an area of 0.155 mm^2. Due to the fixed tape-out plan of IMEC, the measurement of this chip will not be conducted within this thesis project period. The simulation results show that this transceiver achieves a high data rate of 1.66 Gbps while the total DC power consumption is limited to be 19.59 mW. With the adoption of EBD and DSIC, this transceiver is proved to be an excellent solution for short-range, high-speed low-power applications with FD and RadCom functions available.

6.2 Future Work

As mentioned above, measurement of the real chip needs to be carried out to further verify the performance of this transceiver.
In Section 3.5.3, the simulation result of the complete LPF shows some deviations from ideal curve at high frequency. This discrepancy is more evident in low-gain setting situations. This feature is due to the limited bandwidth of the GM cell used in the LPF. Although the GM cell bandwidth is designed to be 2.2 GHz and is larger than the interested frequency band of 500 MHz, it will still cause this deviation at a higher frequency. To further optimize the BiQuad performance, the GM cell needs to be redesigned to have higher bandwidth.
Instead of an ADC buffer, a baseband buffer is cascaded after LPF. The baseband buffer provides sufficient current for the external measurement device. However, it limits the linearity performance. Even with increased linearity performance of the proposed closed-loop BiQuad, the final linearity of the whole RX is not as good as desired. A linear baseband buffer or on-chip ADC buffer is expected in future work.

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Appendices

A Pad-Ring and Floor Plan

As a high-speed transceiver with hybrid modulation, real-time communication is expected. Thus, external high-speed data pins are required. In this thesis project, this is achieved with low-voltage differential signaling (LVDS). LVDS is a high-speed, long-distance digital interface for serial communication. Two wires are used for one signal with a 180° phase shift with each other, thus, they are differential signals. This configuration is capable of keeping high data rate while limiting the noise emission in a considerable low level.

However, since LVDS is differential and the hybrid modulation scheme consists of 7 bits, 14 pins are needed to cover all input bits. To compromise the chip area and number of possible input pins, 5 bits are provided in this chip design instead of 7. Besides, the baseband output pins are required as well. Since both I and Q outputs are differentials, 4 output pins are needed. A pair of differential inputs and outputs are included for the standalone BiQuad test. Then 5 SPI pins are reserved for the digital core. Finally, other pins are occupied with supplies and grounds. To reduce the interference between supplies of different blocks, separate supplies are provided. The pin list is shown in Fig. 55 below. According to this list, the pad ring is implemented.

The floor plan is presented in the following Fig. 54. The TRX is placed at the bottom right corner since the bottom pins are reserved as baseband output, and the RX outputs can be directly connected to corresponding pins at a short distance. The bottom left corner pins are dedicated ones for the input and output of standalone BiQuad. Finally, the complete chip layout is implemented following this floor plan, as shown in Fig. 56.

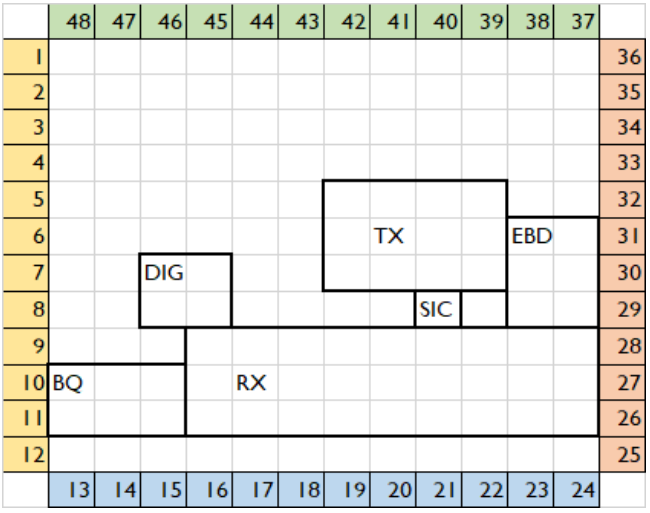

Figure 54: Floor plan

	hsuwbtrx					
	Number	**Pin Name**	**Type**	**Direction**	**Description**	Left
	1	LVDS_IN_P<3>	VAC	Input	LVDS data input (250 Mbps)	Bottom
	2	LVDS_IN_N<3>	VAC	Input	LVDS data input (250 Mbps)	Right
	3	LVDS_IN_P<2>	VAC	Input	LVDS data input (250 Mbps)	Top
	4	LVDS_IN_N<2>	VAC	Input	LVDS data input (250 Mbps)	
	5	VDD_IO	VDC	Input	VDD for IO	
	6	VSS_IO	VDC	Input	VSS for IO	
	7	LVDS_IN_P<1>	VAC	Input	LVDS data input (250 Mbps)	
	8	LVDS_IN_N<1>	VAC	Input	LVDS data input (250 Mbps)	
	9	LVDS_IN_P<0>	VAC	Input	LVDS data input (250 Mbps)	
	10	LVDS_IN_N<0>	VAC	Input	LVDS data input (250 Mbps)	
PRCUT	11	BQ2_IP	VAC	Output	BQ standalone test input	
	12	BQ2_IN	VAC	Output	BQ standalone test input	
	13	BQ2_OP	VAC	Output	BQ standalone test output	
	14	BQ2_ON	VAC	Output	BQ standalone test output	
	15	RX_OUT_IP	VAC	Output	RX baseband output	
	16	RX_OUT_IN	VAC	Output	RX baseband output	
	17	RX_OUT_QP	VAC	Output	RX baseband output	
	18	RX_OUT_QN	VAC	Output	RX baseband output	
	19	I_VCMOUT	VDC	Input	VCMOUT	
	20	VDD1P8	VDC	Input	1.8V VDD for output buffer	
	21	VSS1P8	VDC	Input	VSS for output buffer	
PRCUT	22	VSS	VDC	Input	Common VSS	
	23	VDD_BB	VDC	Input	VDD for analog baseband	
PRCUT	24	VSS	VDC	Input	Common VSS	
	25	VSS	VDC	Input	Common VSS	
	26	VDD_RX_RF	VDC	Input	VDD for RX_RF	
	27	VSS	VDC	Input	Common VSS	
	28	VSS	VDC	Input	Common VSS	
	29	RF_IN_OUT	VAC	Output	EBD output	
	30	VSS	VDC	Input	Common VSS	
PRCUT	31	VSS_PA	VDC	Input	VSS for PA	
	32	VDD_PA	VDC	Input	VDD for PA	
PRCUT	33	VDD_HS	VDC	Input	VDD for High-Speed Baseband	
	34	VSS	VDC	Input	Common VSS	
PRCUT	35	VDD_DIG	VDC	Input	VDD for digital	
	36	VSS	VDC	Input	Common VSS	
	37	CSN	VDC	Input	SPI	
	38	MOSI	VAC	Input	SPI	
	39	MISO	VAC	Input	SPI	
	40	SCK	VAC	Input	SPI	
	41	RSTN	VDC	Input	SPI	
PRCUT	42	VSS	VDC	Input	Common VSS	
	43	VDD_DCO	VDC	Input	VDD for DCO	
PRCUT	44	LVDS_CK_P	VAC	Input	LVDS clock (500 MHz)	
	45	LVDS_CK_N	VAC	Input	LVDS clock (500 MHz)	
	46	EXT_CK	VAC	Input	External clock (500 MHz)	
	47	LVDS_IN_P<4>	VAC	Input	LVDS data input (250 Mbps)	
	48	LVDS_IN_N<4>	VAC	Input	LVDS data input (250 Mbps)	

Figure 55: Pin list

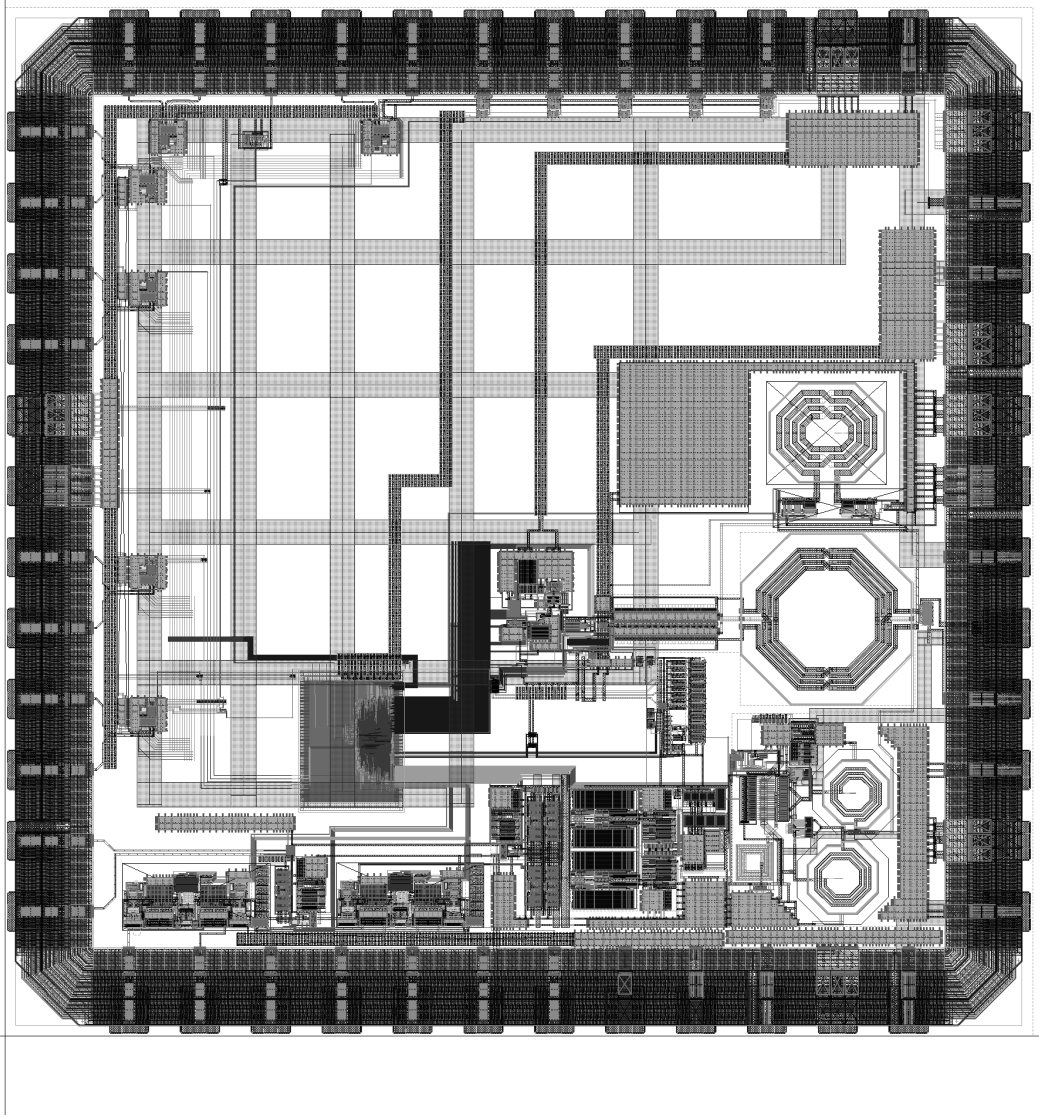

Figure 56: HSUWBTRX chip layout

B Chip Sealing and Dummy Filling

Before sending the GDS for fabrication, the final chip sealing and dummy filling have been carried out to avoid density errors. The sealed chip with dummies is shown in the figure below.

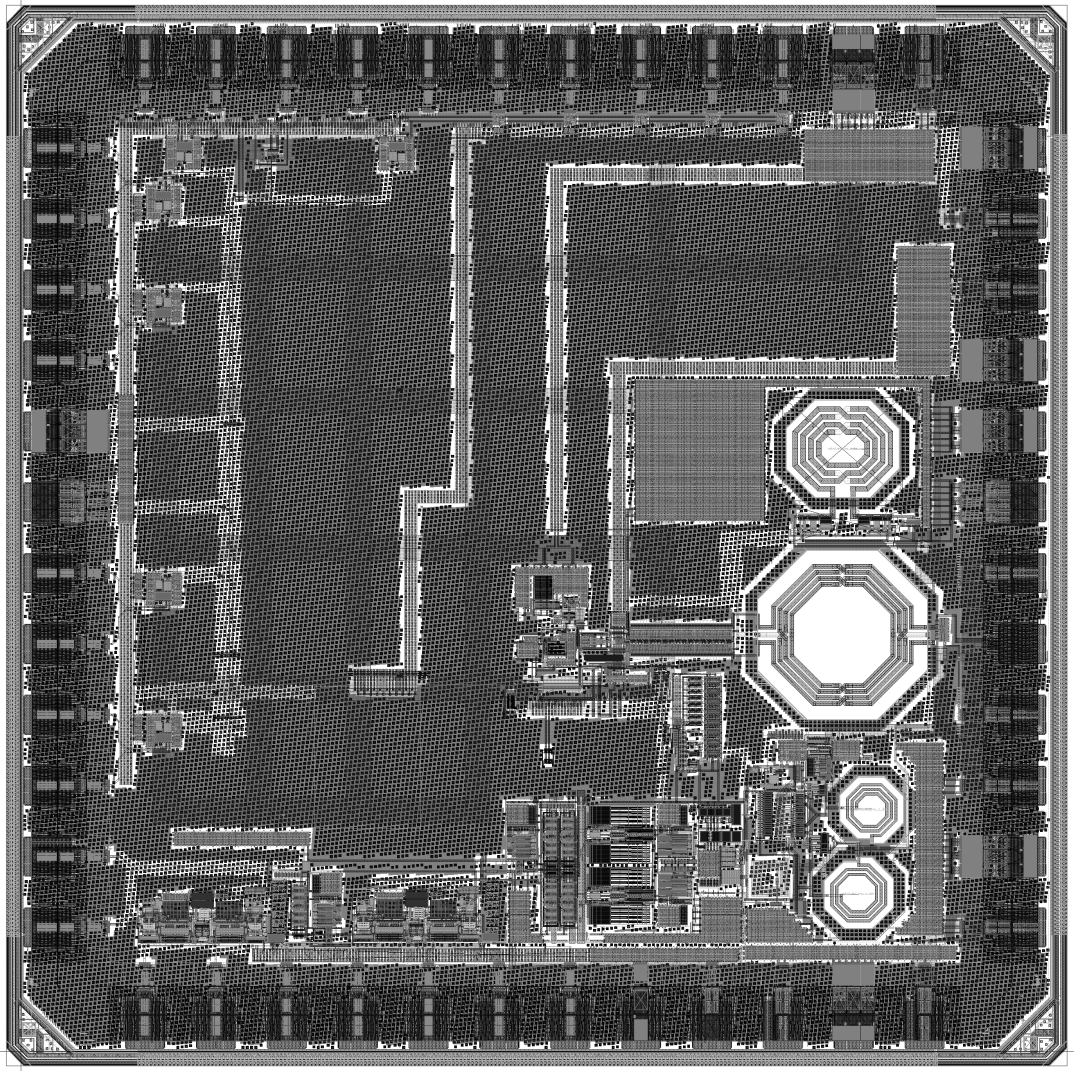

Figure 57: Chip layout with sealing and dummy filling