# Wideband and Energy Efficient Digital Transmitter

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Challenge the future

# Wideband and Energy Efficient Digital Transmitter

by

**Q. Bruinsma**

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|---|---|---|
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*This thesis is confidential and cannot be made public until December 31, 2021.*



TU Delft AMPLEON

# Summary

The ever increasing demand for faster data rates combined with the need for higher levels of integration, while keeping the production and operation cost to a minimum leads to the requirement of an efficient high bandwidth digital transmitter architecture. With the shortcomings of both polar and cartesian architectures, a new architecture is introduced, Multi-Phase cartesian, which bridges the gap of between the two conventional architectures. Multi-phase cartesian is implemented using two parallel connected RF-DACs, to allow for integration. Even though the switching behaviour of the DACs would suggest the use of switch-mode type matching networks, the choice is made to go for a Class-B type matching network, to enable a high bandwidth and minimise the need for predistortion. Two technologies are used for the design of the transmitter, LDMOS and GaN. The design of the desired output matching network is discussed together with the results of the simulations. Some initials measurements are performed and their results are showcased in this document. The achieved peak efficiency is 59 % with a 1 dB frequency of 200 MHz.

# Acknowledgements

First and foremost I want to thank my supervisors S.C. Pires and L.C.N. de Vreede. Thank you S.C. Pires for all the help, supervision and most of all by providing a different view on my work, which made me look at problems differently. My utmost gratitude goes out to L.C.N. de Vreede for all supervision, time and effort he has put in helping me with any questions I had. He makes designing RF circuits seem easy, while it most definitely is not.

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# 1 Introduction

Wireless communication and detection is everywhere. From smartphones to WiFi and Television to Radar, the demand for wireless systems is high. The biggest wireless network is the cellular phone network. For these networks large data streaming, e.g. high resolution video, is becoming more and more popular, and the rise of the internet of things (IoT) multiplies the amount of users, as a consequence the demand for faster data throughput is increasing. With the current fourth generation (4G) telecommunication network technology, a bandwidth is possible up to 100 MHz and the upcoming fifth generation (5G) technology will offer at a bandwidth of up to 400 MHz for sub 6 GHz operation and the possible bandwidth of 1 GHz in the mm-wave range. As a result, the bandwidth requirements of the transmitter (TX) hardware are increasing. Table 1.1 shows the data-rate and bandwidth requirements of present and future technologies.

Table 1.1: Telecommunication technology specifications [1][2].

| Technology | Peak download data-rate | required bandwidth |
|---|---|---|
| 4G | 100 Mbit $s^{-1}$ | 20 MHz |
| 4G+ | 1000 Mbit $s^{-1}$ | 20 MHz to 100 MHz |
| 5G | 20 Gbit $s^{-1}$ | 100 MHz to 1000 MHz |

With smartphones being extremely popular and almost taking up to role of a personal portable computer, their functionality grows with every iteration. An increase in functions leads to an increase in hardware, which consequently results in a higher cost. To keep the consumer price constant, the smartphone provider needs to lower the hardware costs. One area where this is possible is the communications part of the handheld device. Similar conditions apply to the network provider side. Due to the increased demand for higher data-rate there is more demand for the integration of the hardware. Digitising the hardware greatly decreases the size which leads to a reduced cost. Switching to digital has more

benefits, as it allows for more flexibility of the hardware [3]. Analogue systems are designed for a specific frequency and often require many changes when going to a different frequency, whereas a digital system can be easily standardised by handling changing conditions in the software domain[4].

Add to this, that the power consumption of the current cellular network is similar to that of the air traffic industry, which equates to about 5% of the world's carbon footprint [5], [6]. The pursuit of ever faster data speeds is only leading to an increase of the energy needed for this network. Not only is the power consumption of the network huge, but mobile devices are powered by batteries, so also here the power consumption of electronics is of great importance. There are multiple ways to reduce the carbon emission of wireless communication, one of these ways is to design better energy efficient hardware [7]. In wireless links the power amplifier is the most power hungry device [8], [9], with an average efficiency for modern 5G signals is in the range of 5% to 20% [10].

The afore mentioned problems show the need for wideband and efficient digital TX systems. The TX system architectures currently used are often not the most efficient ones. Therefore this thesis focusses on the implementation of a new system architecture that allows for a more energy efficient and wideband operation. From these problems a set of design specifications was created which are summarised in Table 1.2.

Table 1.2: System design specifications.

| Parameter | specification |
|---|---|
| Peak drain efficiency | 70% |
| Peak output power | 40 dBm |
| 1 dB bandwidth | 400 MHz |

This Thesis discusses the concept of Multi-phase cartesian transmitters. First a general introduction to PAs is given in Chapter 2, which is needed to better understand the operation of the multi-phase transmitter concept. After which, an introduction to load modulation as an efficiency enhancement technique is presented in Chapter 3. Chapter 4 introduces the multi-phase concept and compares it to the standard architectures that are currently used in wireless communication. By then the reader should be comfortable with the theory. Next we discuss the design procedure and the implementation in Chapter 5. For the actual TX implementation, previously designed radio frequency (RF) power digital to analog converter (DAC) hardware is used, which allows to test the principles, but at the same time also imposes some design constrains. chapter 6 and Chapter 7 discuss the results and indicate future steps that could be taken to reach even better results.

# I

# Pre-Study

# 2

# PA Basics

The PA is the most power-hungry component in a conventional transmitter chain, it takes as input a low power RF signal, that needs to be amplified before being transferred over the air. Due to its high power operation, high efficiency is desired, this to ensure as little power dissipation as possible.

This chapter starts with discussing the metrics that characterise the operation of a PA and continue with the various PA operating classes.

## 2.1. Performance Metrics

The PA is characterised by certain specifications, which describe the overall operation of the amplifier. These specifications are often set by two basic metrics of the PA, which are power and gain. A conventional PA has one RF input and one RF output terminal for the RF signal of interest. Furthermore, it has a direct current (DC) feed and ground connection, as shown in Figure 2.1.

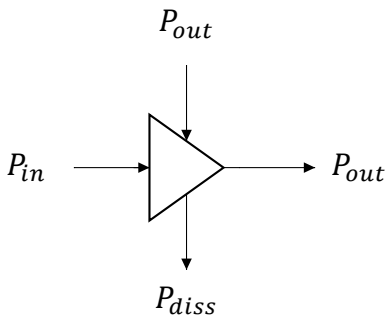



Figure 2.1: Power inputs (signal in and DC supply) and outputs (signal out and dissipated power) of an amplifier.

The instantaneous signal input power of the device is given by

$$P_{in}(t) = v_{in}(t) \cdot i_{in}(t), \tag{2.1}$$

where $V_{in}(t)$ and $i_{in}(t)$ represent the time-domain input voltage and current waveforms.

The desired signal output power is the Root Mean Square (RMS) power delivered to the load at the fundamental frequency $f_0$. The output power of a sinusoidal voltage and current is given in Equation 2.2.

$$P_{out} = \frac{V_{out}}{\sqrt{2}} \cdot \frac{I_{out}}{\sqrt{2}} \tag{2.2}$$

In RF applications, one often speaks of power gain, because power is the metric that is amplified and transmitted. The gain in terms of power is expressed as

$$A_P = 10 \log\left(\frac{P_{out}}{P_{in}}\right). \tag{2.3}$$

When both the input and output impedance are normalised to the same impedance, the voltage gain is depicted as

$$A_v = 10 \log\left(\frac{\frac{{V_{out}}^2}{Z_0}}{\frac{{V_{in}}^2}{Z_0}}\right) = 20 \log\left(\frac{V_{out}}{V_{in}}\right), \tag{2.4}$$

where $Z_0$ is the normalised impedance.

### 2.1.1. Efficiency

In the ideal case, the sum of the input and DC power together are equal to the power that is delivered to the load. Unfortunately real devices are not ideal and dissipate power as well. Efficiency is the metric used to express the power delivered to the load with respect to the power provided to the amplifier. There are multiple ways to define efficiency.

**Drain efficiency** is the ratio between the useful in-band RF output power and the DC power delivered to the drain of the active device. It is described using Equation 2.5. This efficiency metric is often used when discussing PA classes.

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.5}$$

**Power added efficiency** is another measure of efficiency. The difference with drain efficiency is that it takes the input signal power into account which leads to Equation 2.6.

$$\text{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}}{P_{DC}} \cdot \left(1 - \frac{1}{10^{A_p/10}}\right) \tag{2.6}$$

### 2.1.2. Linearity

Apart from efficiency there is linearity, which is used to describe the integrity of the signal.

**Error vector magnitude (EVM)** is commonly used to assess the quality of modulated signals. Amplified or transmitted signals are never exactly the same as the intended signal. This is due to non-idealities, which result from non-linearity and memory effects in the transmitter chain. These all lead to distortion of the signal. The difference between the ideal and distorted output of the transmitter is demonstrated in Figure 2.2, where the red dots represent the ideal symbols for a 16-QAM signal and the black dots the actual symbol values.

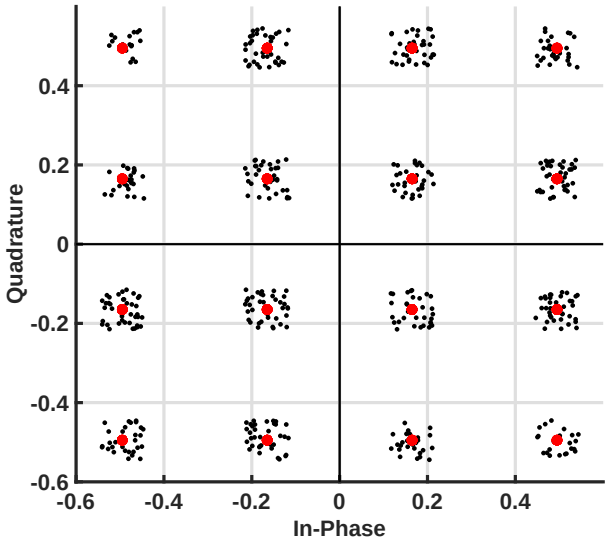



Figure 2.2: Visualisation of the erroneous transmitted signal and ideal constellation symbols.

When the error gets too large, the received signal may be erroneously detected and interpreted as a different symbol with respect to what was originally transmitted. This problem gets bigger the higher the modulation order is used. The EVM expresses the error between the theoretical value of the demodulated symbol and the value of the sent symbol. This is best visualised in Figure 2.3. It is used to measure the in-band signal quality [11].

To have an efficient comparison between the EVM of different systems or modulation types, some normalisation is performed. Normalising may be done using the RMS [12] with respect to the maximum constellation power or the average power of all constellation points. For a fair comparison between different systems it is important to know which one is used, such that the same method may be applied to both systems. Determining the EVM based on the RMS power is the most suitable for comparing different modulation schemes [11]. Here, the EVM is explained using the RMS power, but the procedure using the maximum power is similar.

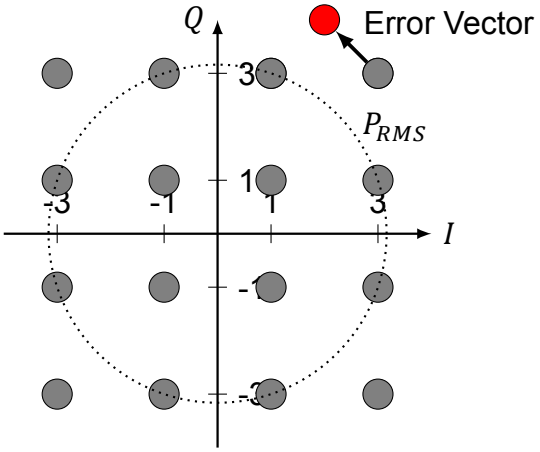



Figure 2.3: Representation of the error vector in a 16-QAM modulation.

The number of points along the In-phase or Quadrature axis in a quadrature modulation scheme is

$$n = \sqrt{M},$$

where $M$ is the modulation order. For 16-QAM, the modulation order is $M$ = 16. Thus for the modulation used in Figure 2.3, $n$ = 4, meaning there are 4 constellation points along the in-phase and quadrature axis. Describing each constellation point as a complex number, with an integer value along either two of the axis, leads to

$$C_{ideal,pq} = C_{I,ideal,pq} + jC_{Q,ideal,pq} = (2p - 1 - n) + j(2q - 1 - n), \tag{2.7}$$

where $p$ and $q$ satisfy $1 \leq p \leq n$ and $1 \leq q \leq n$, respectively. $p$ represents the $i$th value of the symbol along the I axis in Figure 2.3 and $q$ along the Q axis. The normalisation is performed by first setting the RMS value of the ideal constellation diagram to one [12]. In Equation 2.8, $P_{ideal}$ does not represent the power in the constellation, but is used to better visualise the correspondence with the measured case.

$$\begin{aligned} P_{ideal} &= \sum_{p=1}^{n} \left[ \sum_{q=1}^{n} \left( C_{I,ideal,pq}^2 + C_{Q,ideal,pq}^2 \right) \right] \\ &= \sum_{p=1}^{n} \left[ \sum_{q=1}^{n} \left( (2p - 1 - n)^2 + (2q - 1 - n)^2 \right) \right]. \end{aligned} \tag{2.8}$$

This leads to the normalisation factor

$$A_{ideal} = \sqrt{\frac{1}{P_{ideal}/M}}. \tag{2.9}$$

The same procedure is performed to get the normalisation of the measured samples. Similar to the procedure for the ideal constellation, but now for the measured powers, the RMS value is set to one. The total power in the measured constellation, with $T$ samples, is

$$P_{meas} = \sum_{r=1}^{T} \left[ V_{I,meas,r}^2 + V_{Q,meas,r}^2 \right], \tag{2.10}$$

where $V_{I,meas,r}$ and $V_{Q,meas,r}$ are the measured voltage amplitude of the $r^{th}$ symbol. $T$ must be large enough so that it encompasses all possible symbol transitions. The total power is now used to calculate the measured normalisation factor, which is

$$A_{meas} = \sqrt{\frac{1}{P_{meas}/T}}. \tag{2.11}$$

Using these normalisation factors the EVM is calculated as follows

$$EVM_{RMS} = \sqrt{\frac{\frac{1}{T}\sum_{r=1}^{T}\left[|S_{I,r}|^2 + |S_{Q,r}|^2\right]}{P_{S,avg}}}. \tag{2.12}$$

where $P_{S,avg}$ is the normalised power of the constellation symbols and

$$S_{I,r} = V_{I,meas,r} \cdot A_{meas} - C_{I,ideal,pq} \cdot A_{ideal},$$
$$S_{Q,r} = V_{Q,meas,r} \cdot A_{meas} - C_{Q,ideal,pq} \cdot A_{ideal}.$$

**Adjacent channel power ratio (ACPR)** is the ratio between the in-band power and the out-of-band power of one of the adjacent frequency bands.

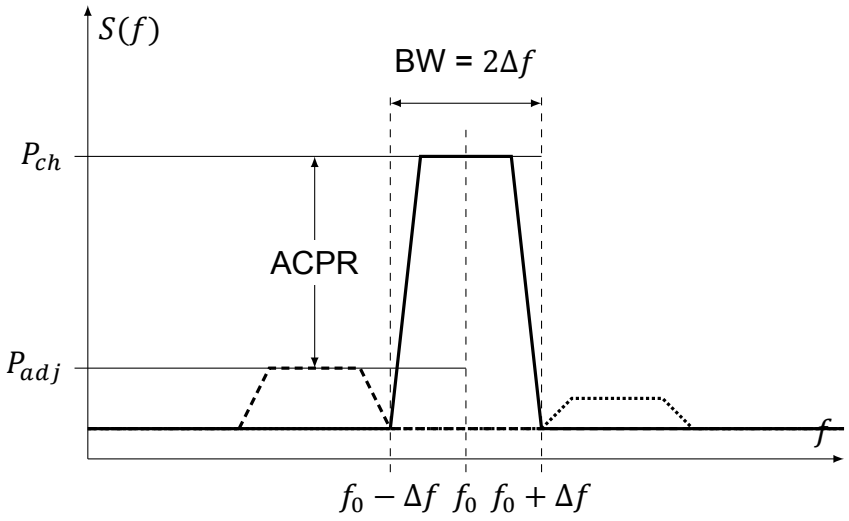



Figure 2.4: Transmitted in-band power and adjacent frequency bands.

$$ACPR_{dBc}=10 \cdot \log\left(\frac{P_{adj}}{P_{ch}}\right) \tag{2.13}$$

**AM-AM and AM-PM** or amplitude-modulation to amplitude-modulation and amplitude-modulation to phase-modulation, respectively, are measures that indicate the effect of the non-linearity of the active device on the output signal. With a linear device, the the output is a linear scaled version of the input signal, perhaps with a constant phase shift, as in

$$y(t) = f[x(t)] = G_T \cdot A(t)\cos(\omega t + \theta(t) + \psi), \tag{2.14}$$

where $G_T$ and $\psi$ are the gain and constant phase shift, respectively.

The non-linearity of the amplifier causes the amplitude of the to be amplified signal affects the gain and phase transfer of the output signal as

$$y(t) = f[x(t)] = g[A(t)]\cos(\omega t + \theta(t) + \Psi[A(t)]) \tag{2.15}$$

where $g[A(t)]$ and $\Psi[A(t)]$ are the AM-AM and AM-PM distortions, respectively.

## 2.2. Transconductance Classes

Normally, when maximum power possible needs to be transferred to the load, the maximum power transfer theorem is used. This theorem states that in order to maximize the power transfer, the load impedance must be equal to the complex conjugate of the source impedance. This is shown in Figure 2.5. However, this leads to a maximum efficiency of 50%, because half of the generated power remains in the active device. Thus to increase the efficiency, a different strategy than the conjugate match has to be used [13]. This means there is a trade off between output power, gain, linearity and efficiency. With this in mind, the performance of the various amplifier classes will now be discussed.

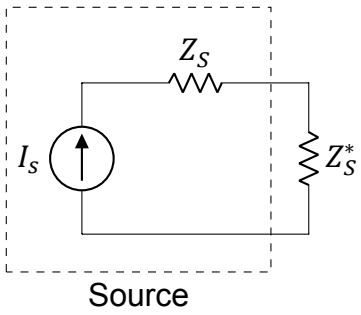



Figure 2.5: Maximum power theorem in a circuit diagram.

The main premise of a transistor is that when a voltage is presented at the gate (or base), a current starts to flow through its drain (or collector), respectively.

The voltage to current transformation is known as transconductance. The standard power amplifier classes use this transistor characteristic and are therefore referred to as transconductance amplifiers. Different amplifier operation modes in electronics are indicated by classes and a letter , e.g., Class-A, B or C. A transistor input characteristic curve is displayed in Figure 2.7.

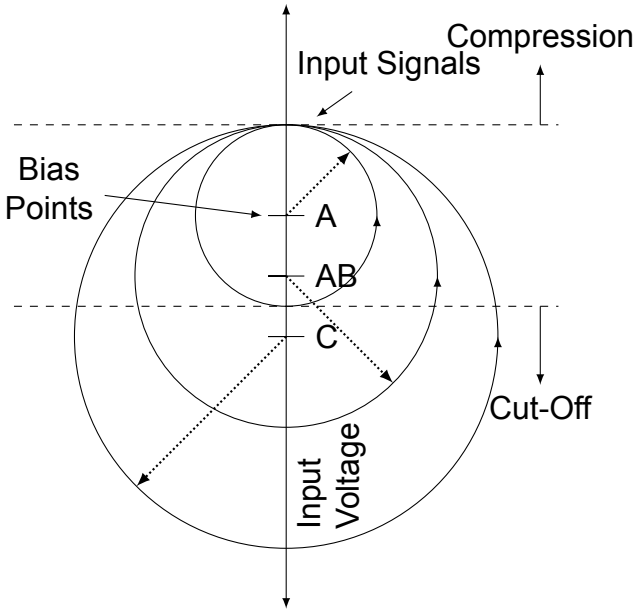



Figure 2.6: Visual representation of the bias points of different amplifier classes. Indicating that the input drive voltage (radii of the circles) needs to increase as the input bias voltage drops to put the PA towards class-C operation [14].

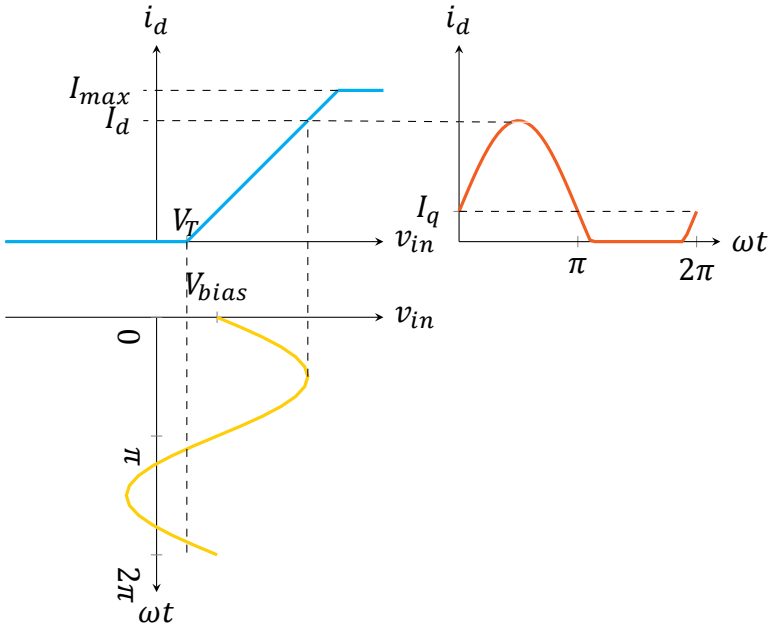



Figure 2.7: Input characteristic (blue) with the corresponding input (yellow) and output (red) waveforms of a Class-AB amplifier.

### 2.2.1. Class-A to C

The first class of PAs is the most basic small-signal amplifier where high linearity is preserved by operating the transistor in the active region for bipolar and saturation region for Field Effect Transistors (FETs), for the entire signal swing.

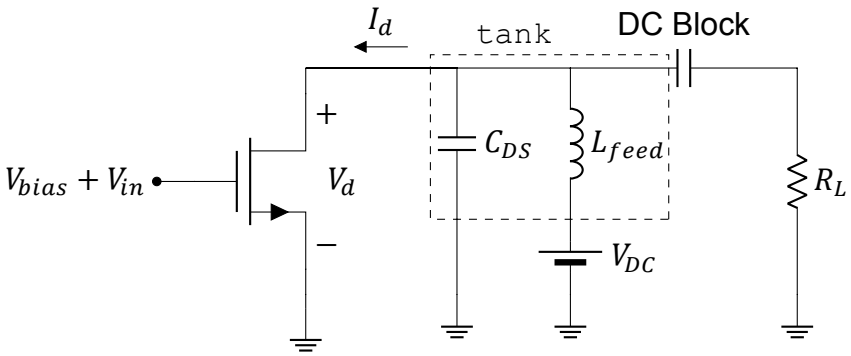



Figure 2.8: Circuit diagram used in the discussion of the standard classes. Each amplifier class has a different bias ($V_{bias}$) and input voltage ($V_{in}$). Both the drain current ($I_d$) and the drain voltage ($V_d$) are indicated and used throughout this section.

The class of operation as with respect to amount of signal swing in the saturation region is best visualised in Figure 2.6 from E.W. McCune [14]. Where the full signal swing of the drive voltage needs to increase when the input bias is lowered.

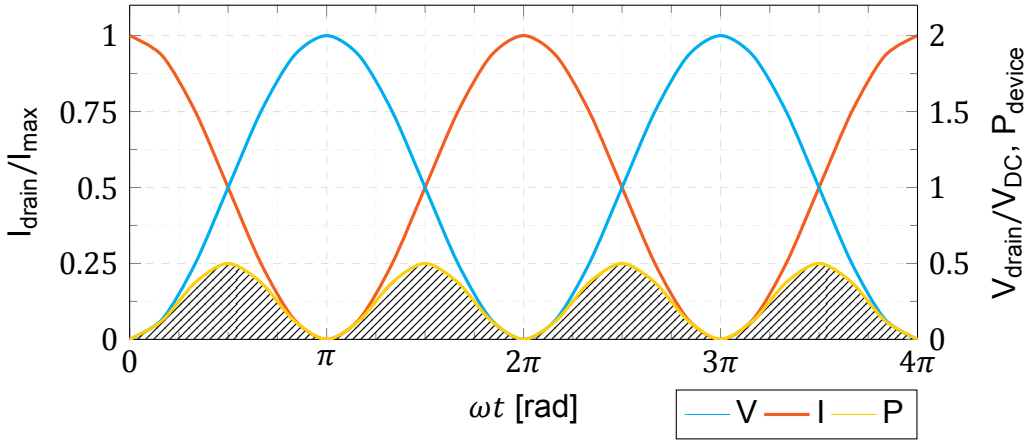



Figure 2.9: Normalised drain current and voltage waveforms of a Class-A Power Amplifier, with the shaded area indicating the power dissipated by the active device.

The best way to examine the behaviour of the different amplifier classes is by investigating the current and voltage waveforms at the drain of the transistor. Figure 2.7 presents a visual of the variables used in this section. The time-domain current signal is

$$i_d(t) = I_q + I_d \cos(\omega t), \tag{2.16}$$

where $I_q$ and $I_d$ are the amplitude quiescent and drain current, respectively. The

drain voltage waveform is

$$v_d(t) = V_{DC} - V_d \cos(\omega t), \tag{2.17}$$

where $V_{DC}$ and $V_d$ are the supply and drain voltage amplitudes, respectively. Comparing Equation 2.16 and Equation 2.17 shows that both waveforms are out of phase.

Taking the drain voltage swing to be equal to the supply voltage, also known as the zero saturation voltage condition $V_d/V_{DC} = 1$, and the drain current to be $I_q$=$I_d$, leads to maximum efficiency of only 50%. This case is known as class-A. These normalised waveforms are displayed in Figure 2.9. The ratio between the quiescent and drain current amplitude can be adjusted and thus the conduction angle [15]

$$\varphi = 2 \cdot \cos^{-1}\left(-\frac{I_q}{I_d}\right), \tag{2.18}$$

can be varied.

Now the drain current is expressed as function of the conduction angle as

$$i_d(t) = \begin{cases} I_q + I_d \cos(\omega t), & -\varphi/2 \leq \omega t < \varphi/2 \\ 0, & \varphi/2 \leq \omega t < 2\pi - \varphi/2 \end{cases} \tag{2.19}$$

For a Class-A amplifiers, the conduction angle is $2\pi$, because the full signal voltage swing at the input is translated to a corresponding current swing at the output of the active device. $I_d$ is now defined as

$$I_d = I_{max} - I_q,$$

which means the drain current now becomes

$$i_d(t) = \frac{I_{max}}{1 - \cos(\varphi/2)} \cdot [\cos(\omega t) - \cos(\varphi/2)]. \tag{2.20}$$

Using this equation for the drain current, both the DC and the fundamental components of the drain current are calculated by integrating over the conduction angle. Where the DC component becomes

$$I_{DC} = \frac{1}{2\pi} \int_{-\varphi/2}^{\varphi/2} \frac{I_{max}}{1 - \cos(\varphi/2)} \cdot [\cos(\omega t) - \cos(\varphi/2)] d\omega t. \tag{2.21}$$

By calculating the other Fourier coefficient, the fundamental component and higher harmonics are determined. The fundamental is given by

$$I_1 = \frac{1}{\pi} \int_{-\varphi/2}^{\varphi/2} \frac{I_{max}}{1 - \cos(\varphi/2)} \cdot [\cos(\omega t) - \cos(\varphi/2)] \cdot \cos(\omega t) d\omega t. \tag{2.22}$$

Rewriting yields

$$I_{DC} = \frac{I_{max}}{2\pi} \cdot \frac{2\sin(\varphi/2) - \varphi\cos(\varphi/2)}{1-\cos(\varphi/2)} \tag{2.23}$$

$$I_1 = \frac{I_{max}}{2\pi} \cdot \frac{\varphi - \sin(\varphi)}{1-\cos(\varphi/2)} \tag{2.24}$$

These expressions are used to plot the DC and fundamental components of the drain current as a function of the conduction angle. The plots are displayed in Figure 2.10. Using these voltages and currents to calculate the fundamental output power, the DC power and efficiency, leads to

$$P_{out} = \frac{1}{2} I_d V_d, \tag{2.25}$$

$$P_{DC} = I_{DC} V_{DC}, \tag{2.26}$$

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{1}{2}\frac{I_d}{I_{DC}}\frac{V_d}{V_{DC}}, \tag{2.27}$$

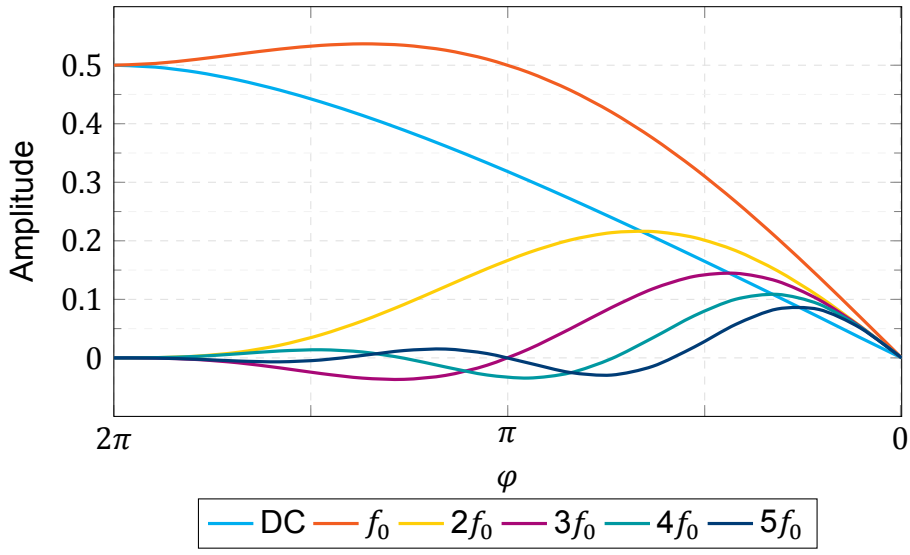



Figure 2.10: Normalised drain current amplitude of the DC, fundamental and up until the 5th harmonic [15].

As previously stated the transconductance classes are defined by their conduction angle. The class definitions are displayed in Table 2.1. Inspecting Figure 2.10 shows that the fundamental current amplitude for Class-A and B are equal, but the DC component is lower for class-B. Using Equations 2.23 and 2.24 with $\varphi = \pi$ leads to the following values for the DC and fundamental component

$$I_{DC} = \frac{I_{max}}{\pi},$$

$$I_1 = \frac{I_{max}}{2}.$$

Using these values to calculate the fundamental output power and efficiency. The output power of a class-B PA is equal to that of a Class-A amplifier, while its efficiency is 78.5%. The output power and efficiency are plotted in Figure 2.11 as a function of conduction angle. The figure indicates that if the conduction angle approaches zero the efficiency becomes 100%, this is because the DC power approaches zero, however, since also the output power goes to zero this is not a very practical solution. A visual example is shown in Figure 2.12, where the dissipated power is indicated by the shaded area, which is the product of the current and voltage that overlap. The smaller the conduction angle, the smaller this area becomes.

Table 2.1: class definitions as function of conduction angle.

| Class | Conduction angle ($\varphi$) |
|---|---|
| A | $\varphi = 2\pi$ |
| AB | $\pi < \varphi < 2\pi$ |
| B | $\varphi = \pi$ |
| C | $0 < \varphi < \pi$ |

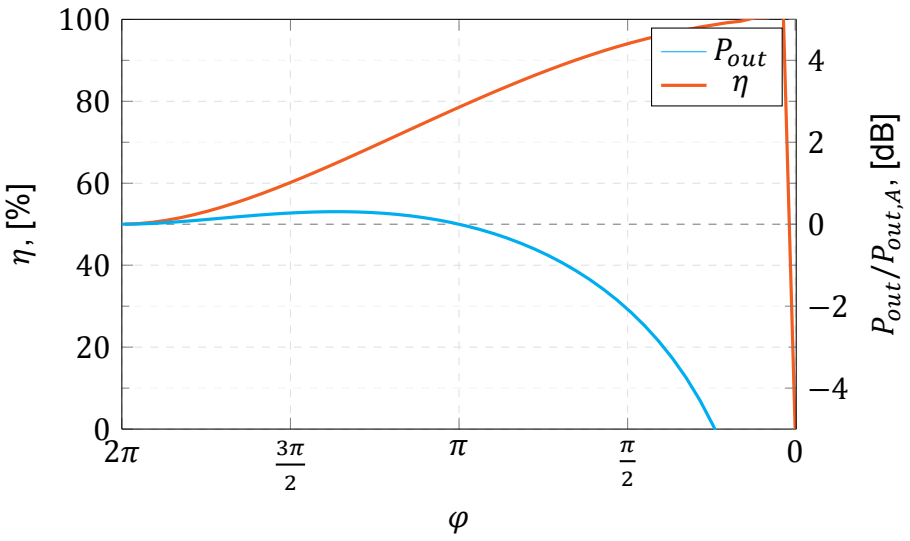
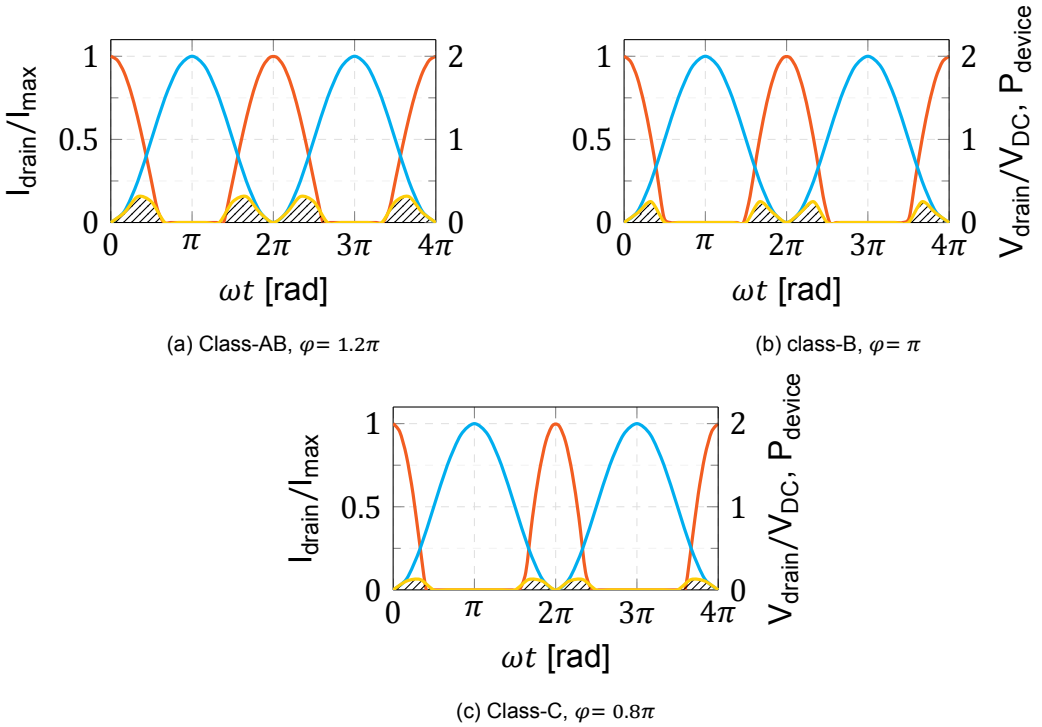



Figure 2.11: Output power and efficiency as function of the conduction angle [15].

The efficiency increase is also evident from using the loadlines of each individual amplifier class, which are plotted in Figure 2.13. Where the overlap of the voltage and current waveforms is somewhat more intuitive, as this is indicated by the area under the loadline, which decreases from class-A to class-C.

The transconductance classes provide a high level of linearity and output power




(a) Class-AB, $\varphi = 1.2\pi$

(b) class-B, $\varphi = \pi$

(c) Class-C, $\varphi = 0.8\pi$

Figure 2.12: Normalised drain current and voltage waveforms for different conduction angles, with the shaded area indicating the power dissipated by the active device.

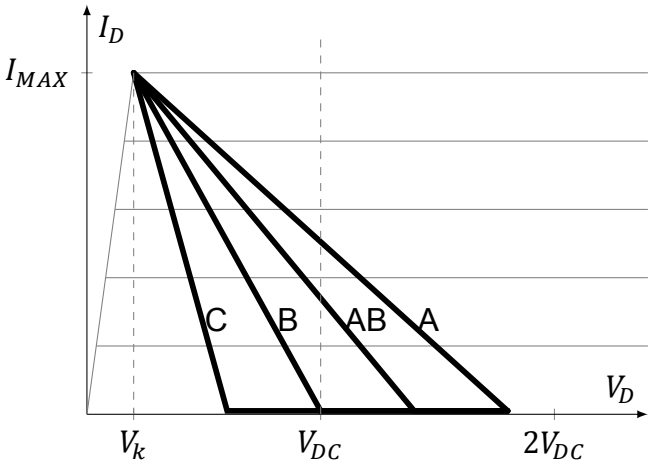


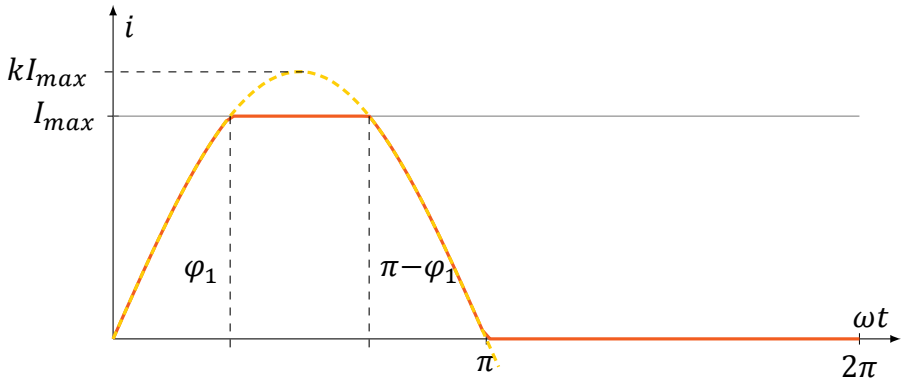

Figure 2.13: Different transconductance classes with their respective loadlines.

at moderate efficiency. However, output power and linearity can be traded off for higher efficiency, when moving to smaller conduction angles.

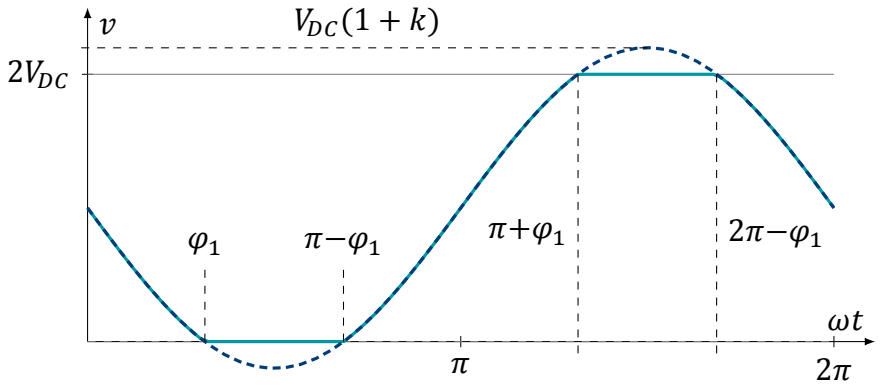
### 2.2.2. Overdriven class-B

The standard classes get their linearity from the signal amplitude being driven between cut-off and compression as depicted in Figure 2.6. However, what happens when the amplitude is increased further so that the active device is driven into compression? The first thing that will happen is that because of non-linearity,

extra harmonics are introduced. Since the device current is limited by the drain-source voltage, which cannot be less then zero. The current and thus the voltage will clip. Consequently, driving the device harder will square up the drain voltage. To best compare the overdriven case with the normal class-B, the drain current must also not exceed $I_{max}$. The ideal overdriven class-B waveforms are illustrated in Figure 2.14. An important note, as will be mathematically shown in this section; the amplifier requires certain impedance terminations for higher harmonics, for this reason the circuit shown in Figure 2.8 does not apply to the overdriven class-B amplifier. The clipping of the voltage waveform does not change its aver-




(a) Current




(b) Voltage

Figure 2.14: Ideal drain waveforms of an overdriven class-B PA.

age dc value, which means the DC component remains $V_{DC}$. The odd harmonic components introduced by the clipping are [16]

$$V_n = \frac{2V_{DC}}{\pi}\left[\frac{\sin(\varphi_1 - n\varphi_1)}{(1-n)\sin(\varphi_1)} - \frac{\sin(\varphi_1 + n\varphi_1)}{(1+n)\sin(\varphi_1)} + \frac{2\cos(n\varphi_1)}{n}\right] \tag{2.28}$$

with $n$ only taking the values 3,5,..., and $V_n$ = 0 for all even $n$. The fundamental voltage is

$$V_1 = \frac{2V_{DC}}{\pi}\left[\frac{\varphi_1}{\sin(\varphi_1)} + \cos(\varphi_1)\right]. \tag{2.29}$$

The DC current does increase, however, and now becomes

$$I_{DC} = \frac{I_{max}}{\pi}\left[\frac{\pi}{2} - \varphi_1 + \tan\left(\frac{\varphi_1}{2}\right)\right]. \tag{2.30}$$

The fundamental frequency component of the current is expressed as

$$I_1 = \frac{I_{max}}{\pi}\left[\frac{\varphi_1}{\sin(\varphi_1)} + \cos(\varphi_1)\right]. \tag{2.31}$$

and the odd harmonic components of the current are

$$I_n = \frac{I_{max}}{\pi}\left[\frac{\sin(\varphi_1 - n\varphi_1)}{(1-n)\sin(\varphi_1)} - \frac{\sin(\varphi_1 + n\varphi_1)}{(1+n)\sin(\varphi_1)} + \frac{2\cos(n\varphi_1)}{n}\right]. \tag{2.32}$$

Calculating the fundamental output power as function of $\varphi_1$ leads to

$$P_{out} = \frac{V_{DC} I_{max}}{\pi^2}\left[\frac{\varphi_1}{\sin(\varphi_1)} + \cos(\varphi_1)\right]^2, \tag{2.33}$$

and the DC supply power is

$$P_{DC} = \frac{V_{DC} I_{max}}{\pi}\left[\frac{\pi}{2} - \varphi_1 + \tan\left(\frac{\varphi_1}{2}\right)\right]. \tag{2.34}$$

The fundamental output power and DC power are used to calculate the efficiency as function of $\varphi_1$ and is [17]

$$\eta = \frac{1}{\pi}\frac{\left[\frac{\varphi_1}{\sin(\varphi_1)} + \cos(\varphi_1)\right]^2}{\frac{\pi}{2} - \varphi_1 + \tan\left(\frac{\varphi_1}{2}\right)}. \tag{2.35}$$

The fundamental output power relative to conventional class-B and efficiency as function of $\varphi_1$ are plotted in Figure 2.15. The plot indicates that if $\varphi_1$ approaches zero, meaning the voltage and current waveforms are a square wave, the efficiency is

$$\eta = 81\%.$$

The reason for this is to get the ideal overdriven class-B waveforms, the power dissipated in the load happens not only at the fundamental but also at the odd harmonics. This is proven by calculating the impedance at the odd harmonics using $I_n$ and $V_n$ from Equations 2.28 and 2.32, which leads to

$$Z_n = \frac{2V_{DC}}{I_{max}} = R_{opt}, \qquad \text{for odd } n \tag{2.36}$$

$$Z_n = 0, \qquad \text{for even } n \tag{2.37}$$

which shows that the conventional class-B load resistance is presented to the device at higher harmonics as well. This shows that controlling the impedance at higher harmonics leads to a further increase in fundamental output power and efficiency.

Figure 2.15 shows that the maximum achievable efficiency is 88.6%. The efficiency can even be further increased by presenting different impedances at higher harmonics. Doing this is known as a Class-F PA, which is often considered a switch mode amplifier.

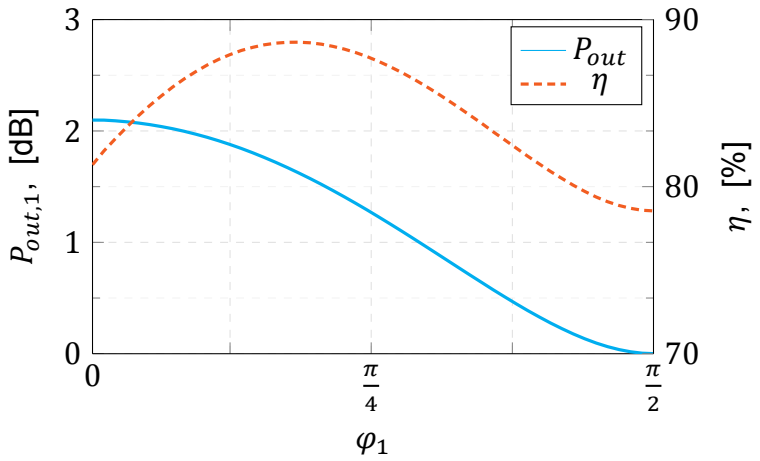



Figure 2.15: Efficiency and output power relative to class-B of an overdriven class-B PA as function of $\varphi_1$.

### 2.2.3. Class-F

A different way to increase efficiency is to use also open harmonic terminations to shape the drain voltage. This is done in the Class-F PA, where the voltage contains one or more odd harmonics and the current is still a rectified sine wave. The more open odd harmonics are introduced the more the voltage represents a square wave, whereas a half wave rectified sine wave results in only even harmonics beside the fundamental. The ideal waveforms are portrayed in Figure 2.16.

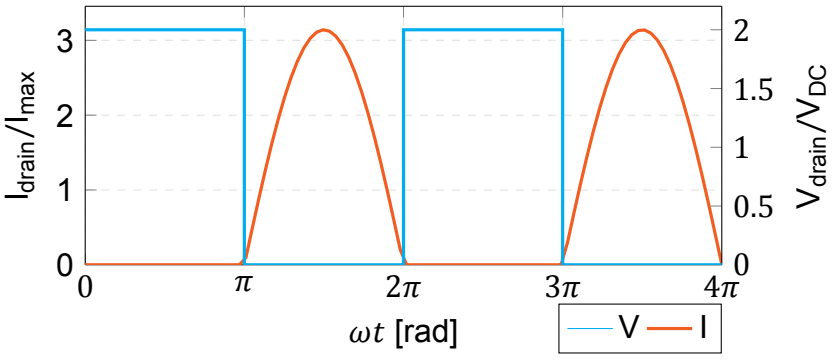



Figure 2.16: Ideal drain voltage and current waveforms of a Class-F PA.

The initial efficiency increase comes from a combination of less current and voltage overlap and the fact that the fundamental frequency amplitude is higher for a square wave than a sine wave with equal amplitude. This leads to a higher fundamental output power, while the DC power consumption stays the same.

To find the desired loads at higher harmonics the overdriven class-B is taken as basis for the analysis. To get the drain waveforms as depicted in Figure 2.16, $\varphi_1$ for the current in Equation 2.31 approaches $\pi/2$, leading to a fundamental current swing of

$$I_1 = \frac{I_{max}}{2}.$$

Whereas for the voltage the parameter $\varphi_1$ in Equation 2.29 approaches zero, thus resulting in

$$V_1 = \frac{4}{\pi} V_{DC}.$$

These values can now be used to calculate the output power at the fundamental frequency, which is

$$P_{out} = \frac{V_{DC} I_{max}}{\pi}. \tag{2.38}$$

Using the same value for $\varphi_1$ in Equation 2.30 causes the DC input power to be

$$P_{DC} = \frac{V_{DC} I_{max}}{\pi}, \tag{2.39}$$

where the equality of the DC input power and RF output power indicate a theoretical efficiency of 100%. Since the drain current waveform is a half wave rectified sine, the odd harmonics of the drain current are

$$I_n = 0, \tag{2.40}$$

for all $n = 3, 5, \ldots$. Now the required impedances at the fundamental, even and odd harmonics are calculated and result in

$$\begin{aligned} Z_1 &= \frac{V_1}{I_1} = \frac{8}{\pi}\frac{V_{DC}}{I_{max}} = R_L, \\ Z_n &= \frac{0}{I_n} = 0, && \text{for even } n \\ Z_n &= \frac{V_n}{0} = \infty. && \text{for odd } n \end{aligned} \tag{2.41}$$

The expressions in Equation 2.41 for the impedance indicate that the load at odd harmonics must be an open and the even harmonics must be short circuited. These harmonic terminations come in the form of resonators at the harmonic frequencies. An example of this is displayed in Figure 2.17. Where the series resonators block the odd harmonic voltages and the parallel resonator at the output passes all even harmonic currents.

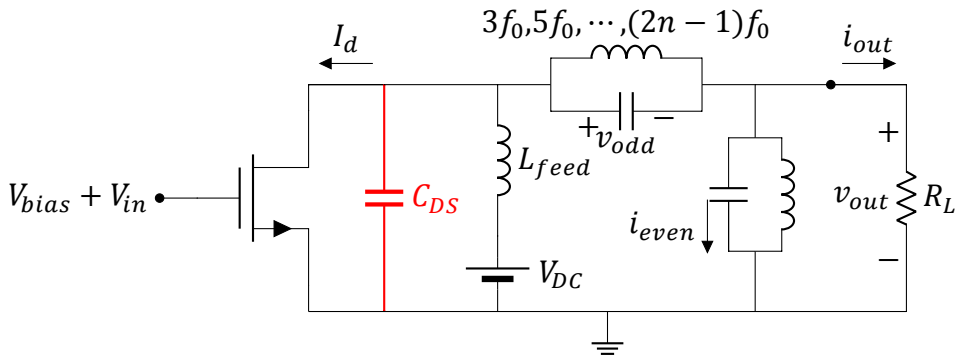



Figure 2.17: Circuit diagram used for waveform shaping with harmonic control termination.

The circuit diagram indicates that due to always present output capacitance it is impossible to create the ideal impedance conditions for all harmonics. However, creating the ideal condition for just a few harmonics already leads to a significant increase in efficiency. Figure 2.18 and Figure 2.19 illustrate the change in drain voltage and current with the introduction of more ideal harmonic conditions, respectively.

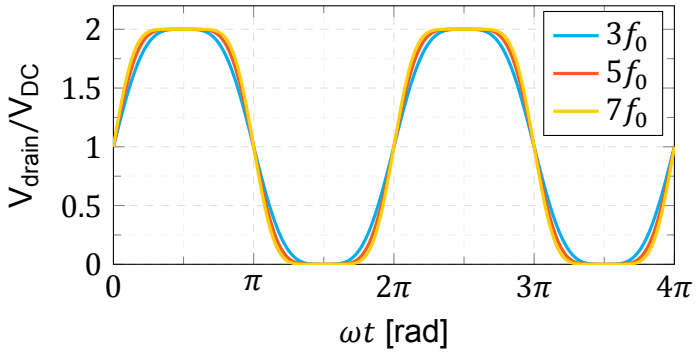



Figure 2.18: Normalised class-F drain voltage waveforms with different maximum odd harmonic opens.

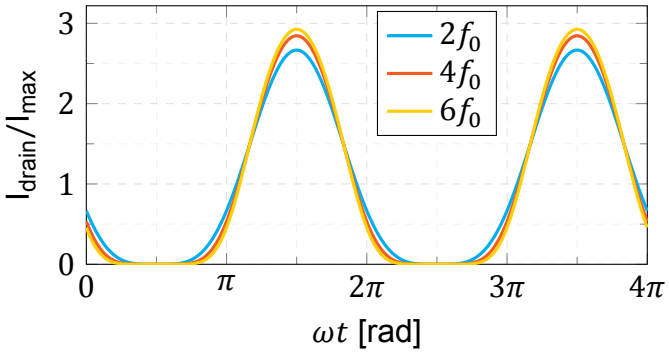



Figure 2.19: Normalised drain current waveforms with different maximum even harmonic shorts.

The increase in efficiency due to the increase in controlled harmonics is cal-

culated using [18]

$$\eta = \frac{\pi}{2(m+1)} \cdot \frac{1}{\tan\left(\frac{\pi}{2(m+1)}\right)}, \tag{2.42}$$

with $m$ being the maximum controlled odd harmonic and all even harmonics short circuited. The result of the expression is plotted in Figure 2.20, from which it is concluded that providing an open to 7 odd harmonics results in an efficiency of over 95%. A big problem with the Class-F PA is that the precise control of higher

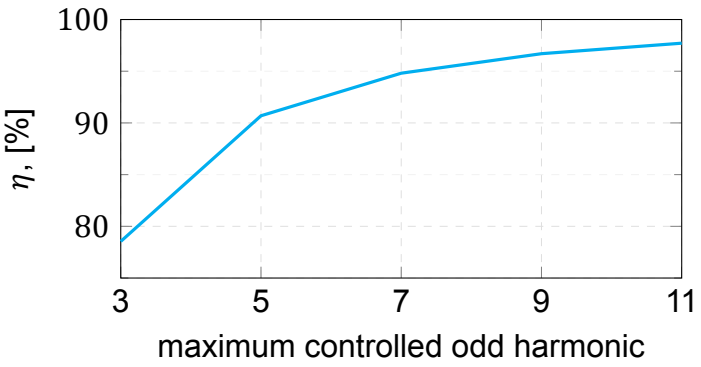



Figure 2.20: Efficiency with respect to the amount of controlled harmonics.

harmonics limits the bandwidth of the amplifier. The bandwidth of each harmonic is larger than that of the fundamental. To be precise the bandwidth is expressed as

$$BW_{@nf_0} = n \cdot BW_{@f_0}, \tag{2.43}$$

where $n$ is the controlled harmonic and $f_0$ is the fundamental frequency. Thus if a Class-F PA with a 7th harmonic open is designed for a bandwidth of 50 MHz at the fundamental, the bandwidth that must be controlled for the 7th harmonic is 350 MHz, which significantly increases the difficulty of design at high fundamental bandwidths.

## 2.3. Pure Switch-mode classes

Apart from the discussed transconductance amplifier classes, there are other type of classes that operate the device as a switch, rather than as a controlled current source. The idea behind this is that in the ideal case a switch does not dissipate power, because there is no voltage across it or no current through the switch at the same time. This means theoretically the maximum efficiency is 100%.

For switch mode PAs it is difficult to speak of input power, since the input impedance is predominantly capacitive, because the active devices are driven as switches, typically by a square wave. This means PAE needs to be redefined, to apply for switch mode amplifiers as well. Furthermore, for a switch-mode amplifier a driver is needed, so the best way to represent the PAE of a switch mode PA is

as follows

$$PAE_{dig} = \frac{P_{out} - P_{DC,driver}}{P_{DC,PA}}. \tag{2.44}$$

Just like with the transconductance amplifiers, the switch-mode ones are identified by letters as well, they will be discussed now.

### 2.3.1. class-D

The first of the switch mode PAs is the class-D, which uses a push-pull like structure depicted in Figure 2.21. Where the transformer at the input ensures a 180° phase difference between the two active device inputs. This causes $M1$ to be on while $M2$ is off and vice versa. This is best represented in Figure 2.22. To proof that the efficiency is 100% for a class-D amplifier, the output and DC power need to be calculated first.

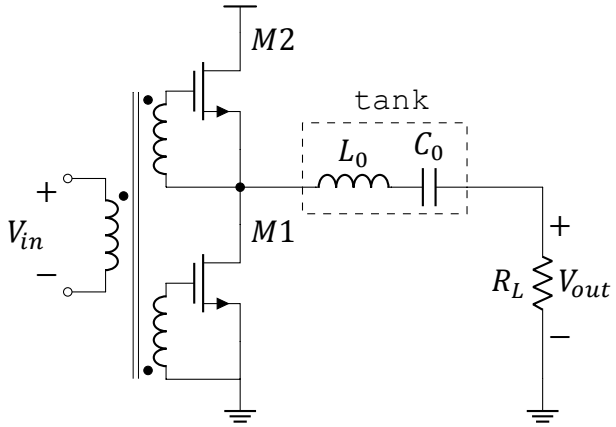



Figure 2.21: Circuit diagram for a push-pull class-D amplifier using nmos devices only.

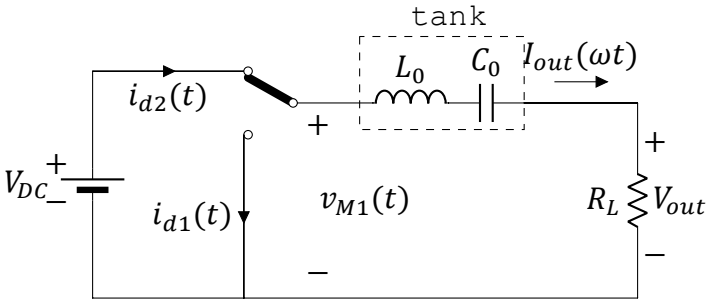



Figure 2.22: Equivalent circuit diagram for a class-D amplifier.

The tank at the output is tuned to the RF frequency to remove all the harmonics. This results in a sinusoidal output current and voltage. The voltage across M1 switches between the supply voltage $V_{DC}$ and ground. this voltage is expressed as

$$v_{M1}(\omega t) = V_{DC} \cdot p(\omega t),$$

where $p(\omega t)$ is a square wave function with values 0 and 1 and a duty cycle of 50%. Assuming the series tank has a high enough Q to allow only the fundamental frequency to pass to the load, the next step to find the output power is to calculate the Fourier series of $v_{M1}(t)$ which is

$$v_{M1}(t) = V_{DC} \cdot \left( \frac{1}{2} + \frac{2}{\pi} \sin(\omega t) + \frac{2}{3\pi} \sin(3\omega t) + \cdots \right), \tag{2.45}$$

so the output current is

$$i_{out}(\omega t) = \frac{2V_{DC}}{\pi R_L} \sin(\omega t). \tag{2.46}$$

The output current flows through the transistor that is on at that time. Thus the drain current of the devices are half wave rectified sine waves as depicted in Figure 2.23. From Equation 2.46 can concluded that the effective fundamental output voltage amplitude is

$$V_{out} = \frac{2V_{DC}}{\pi},$$

thus leading to an output power of

$$P_{out} = \frac{V_{out} \cdot I_{out}}{2} = \frac{2{V_{DC}}^2}{\pi^2 R_L}. \tag{2.47}$$

Since the device drain current waveforms are half rectified sine waves the DC current is the same as that of a class-B or

$$I_{DC} = \frac{I_{out}}{\pi} = \frac{2V_{DC}}{\pi^2 R_L}, \tag{2.48}$$

thus resulting in a DC power consumption of

$$P_{DC} = V_{DC} I_{DC} = \frac{2{V_{DC}}^2}{\pi^2 R_L}. \tag{2.49}$$

This means that the efficiency is

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{\left(\frac{2{V_{DC}}^2}{\pi^2 R_L}\right)}{\left(\frac{2{V_{DC}}^2}{\pi^2 R_L}\right)} = 100\%, \tag{2.50}$$

thus mathematically proving the 100% efficiency. Figure 2.23 shows that this is, because of the non overlapping voltage and current waveforms. It also shows that the two drain currents combined do indeed provide a sinusoidal wave.

A problem arises due to the use of two switches. Ideally the square wave that drives the input of the amplifier has zero transition time. In practice, however, there is a finite transition time ($\tau_{ts}$) which causes the devices to partially conduct

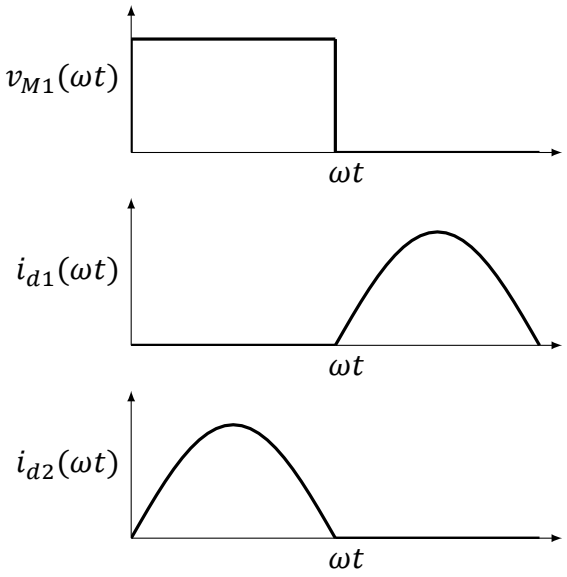



Figure 2.23: Class-D drain voltage and current waveforms.

current at the same time leading to a short from supply to ground for a fraction of the transition, which causes the efficiency to degrade. The derivation is long and unnecessary to repeat here [19]. There are many great resources for further reading, two are Krauss [20] and Grebennikov [21]. The end result of the efficiency as function of transition time is

$$\eta = \frac{\sin(\tau_{ts})}{\tau_{ts}}, \tag{2.51}$$

where the transition time is assumed to approximate a ramp function. A visual representation of the transition time is depicted in Figure 2.24. Equation 2.51 indicates that for $\tau_{ts}$ approaching zero, the efficiency approaches 100% as $\sin(\tau_{ts}) \approx \tau_{ts}$. However, practical implementations with real devices have output capaci-

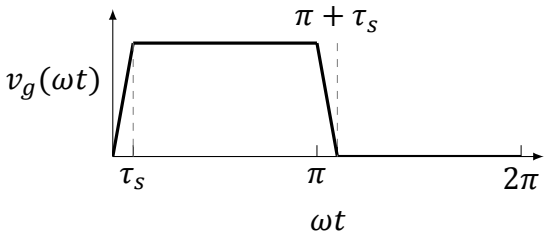



Figure 2.24: Transition time in the gate voltage waveform.

tances that need to be charged and discharged since one cannot resonate out this capacitance for all harmonics. Therefore, practical class-D circuits are less favourable at RF. When not implementing the class-D structure in a push-pull configuration, a p-type device is needed, which typically has poor RF performance.

### 2.3.2. Class-E

Considering the drawbacks of the class-D amplifier, the logical step would be to modify the circuit to use only one switch. This was first done in [22–24]. The second switch is often replaced with a large enough inductor to act as an RF choke. These first implementations use a single switch, but the output matching network is equivalent to that of a transconductance class amplifier. Thus, the optimum switch mode efficiency is not reached.

By changing the output network, a theoretical drain efficiency of 100% can be achieved. This amplifier is called the Class-E PA. The equivalent circuit diagram is displayed in Figure 2.25.

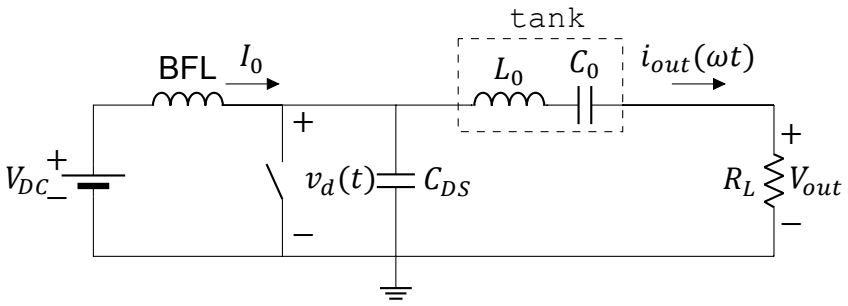



Figure 2.25: Circuit diagram of a Class-E PA.

To ensure optimum efficiency the voltage across the device when it is turned on must equal zero and the current through the device in the off state must be zero. The output impedance of the device is low in the on state and high in the off state. Since the inductor connected to the supply restricts fast change in the current flowing through it, the low impedance of the device in the on state provides a path to ground and the high impedance ensures the current flows through the load. The following conditions must be met

$$v_{DS}(t)\Big|_{t=T} = 0, \tag{2.52}$$

$$\frac{dv_{DS}(t)}{dt}\bigg|_{t=T} = 0. \tag{2.53}$$

Indicating that not only the voltage at the moment of switch turn on, must be zero, but also the change in voltage. This zero slope for the voltage allows for some component value mismatch in the matching network, as there is a time interval in which the switching can occur, for which the drain source voltage is still reasonably close to zero [25].

Time-domain analysis of the circuit leads to the expressions in Equations 2.54 and 2.55 [17]. These are used to plot the drain waveforms of the active device. The drain current during the period $0 \leq \omega t < \pi$ and voltage during period $\pi \leq$

$\omega t < 2\pi$ are illustrated in Figure 2.26.

$$\frac{v_{ds}(t)}{V_{DC}} = \pi\left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos(\omega t) - \sin(\omega t)\right), \tag{2.54}$$

$$\frac{i_d}{I_0}(t) = \left(\frac{\pi}{2}\sin(\omega t) - \cos(\omega t) + 1\right), \tag{2.55}$$

where the maximum value of the drain source voltage and drain current is found by taking the derivative of Equations 2.54 and 2.55. Which leads to the following values

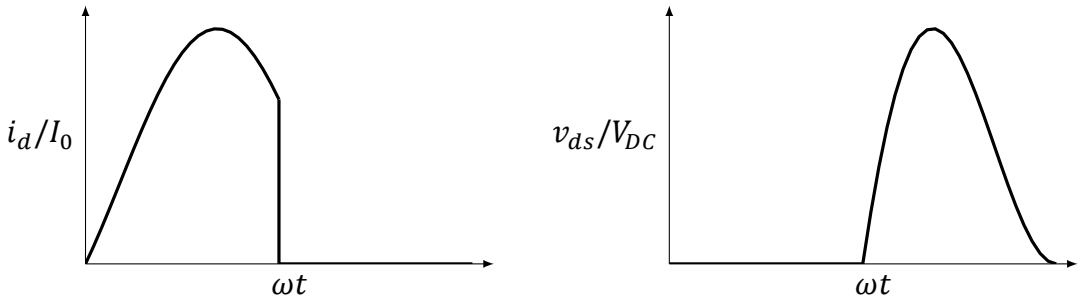
$$V_{max} = 3.562 V_{DC},$$

and

$$I_{max} = 2.8621 I_0,$$

where the steady state inductor current is found using

$$I_0 = 0.577 \frac{V_{DC}}{R_L}. \tag{2.56}$$




(a) Current (b) Voltage

Figure 2.26: Normalised drain waveforms for a Class-E PA.

Instead of assuming an inductor that acts as an RF choke, it is more reasonable to take a finite inductance, which does not only lead to a cheaper and more compact implementation, but also allows for the use of a higher load resistance which leads to a more efficient matching network [26–28].

Analytical analysis of the Class-E circuit is cumbersome and often avoided. For this reason either the analysis is simplified by taking the device on resistance zero or assuming an RF choke for the feed inductance. M. Acar, *et al.* [29] report the acquisition of a design set of equations that relate the system input to the circuit element values of the output matching circuit, where the feed inductance is finite and the device has a larger than zero on resistance. The design equations are displayed in Table 2.2.

Table 2.2: Set of design equations for a Class-E PA.

| design equations |
|---|
| $K_L(q,m) = \frac{\omega L_{feed}}{R_L}$ |
| $K_C(q,m) = \omega C_{DS} R_L$ |
| $K_P(q,m) = \frac{P_{out} R_L}{{V_{DC}}^2}$ |
| $K_X(q,m) = \frac{X_S}{R_L}$ |

Which are all a function of $q$ and $m$, which are defined as

$$q = \frac{1}{\omega\sqrt{L_{feed} C_{DS}}}, \tag{2.57}$$

$$m = \omega R_{on} C_{DS}. \tag{2.58}$$

The design equations are plotted in Figure 2.27 for different values of $q$ with $m = 0$. Each $q$ leads to a certain set of values for the design equations which can used to calculate circuit parameters as depicted in Table 2.2.

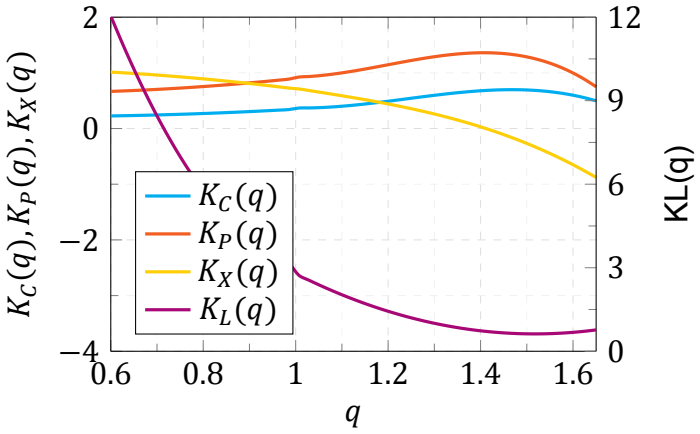



Figure 2.27: Design equations vs $q$ at $m = 0$.

## 2.4. Conclusion

Both transconductance and switch mode amplifiers have been discussed in this chapter. Transconductance PAs are the most linear, but suffer from lower efficiency. However, the linearity and output power can be exchanged for higher efficiency. Whereas the switch mode PAs, in theory, offer extremely high efficiencies at decent output powers. The drawback is that these amplifiers are highly non-linear and suffer from a lack of amplitude modulation. Moreover, comparing the bandwidth of both type of amplifiers indicates that the transconductance PAs allow for simpler design for wideband operation.

# 3

# Load Modulation

For a computer, data is expressed in ones and zeros, otherwise known as bits. To increase the speed at which data is transferred, different modulations are used that transfer symbols. Each symbol represents a combination of bits, an example for 16-QAM is depicted in Figure 3.1. As can be noted from this figure some modulation schemes like 16-QAM use symbols that are not located at peak power. 16-QAM is a quadrature amplitude-modulation technique with a modulation index higher than 4. For most modulation techniques the output power level is most of the time considerably lower than the peak power. For most PAs the highest efficiency is at the peak output power, thus the majority of the signal is transmitted with a lower efficiency. Fortunately, there are ways of increasing the efficiency of the TX PA also these lower output powers.

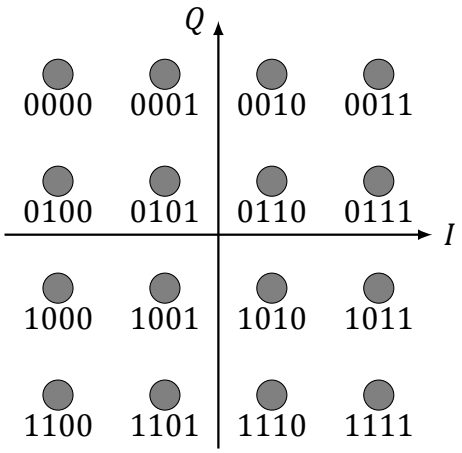



Figure 3.1: Symbol representation in 16-QAM.

One of the technique that is used to increase the efficiency in power back off is load modulation. With load modulation, as the name might suggest, the load that is offered to the PA output stages is dynamically varied, with varying output power.

A simple example on how load modulation would improve the efficiency of a Class B PA that is used in polar operation is given below. In subsection 2.2.1 the optimum load impedance for the device was shown to be

$$R_{opt} = 2 \cdot \frac{V_{DC}}{I_{max}} \tag{3.1}$$

The efficiency of the PA in power back-off is given by

$$\eta_{bo} = \eta_{max} \cdot \frac{I_1}{V_{dc}} R_L \tag{3.2}$$

For simplicity it assumed that the fundamental output current ($I_1$) has a linear relation with the input drive voltage. Equation 3.2 shows that with a lowering of the current the efficiency drops as well, if the supply voltage and load impedance are kept constant. However, it also means that the efficiency at power back-off can be increased by either changing the supply voltage or the load impedance.

The change in supply voltage is a technique used in both envelope tracking (ET) and envelope elimination and restoration (EER). ET modulates the supply in such a way that it leaves some headroom for the output signal swing. The linearity of the signal is still provided by the PA. Whereas, with EER the PA is kept in saturation to ensure the highest efficiency and the output level is fully determined by the supply.

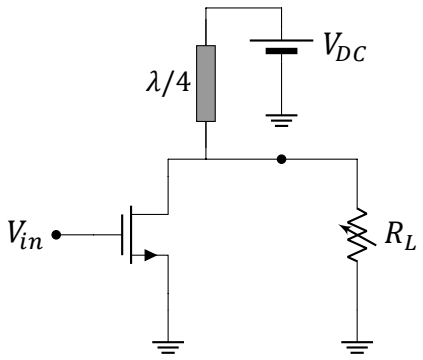



Figure 3.2: Simple load-modulating circuit diagram.

The variation in load impedance is what is referred to as load modulation. Where changing the load itself is called dynamic load modulation. Figure 3.2 shows a circuit with a variable impedance. An example of this is by using current controlled varactors to change the matching network at the output of the PA as in [30] and [31]. By changing the load the voltage swing remains the same at lower drain currents. This is demonstrated using the loadline of the amplifier in Figure 3.3. Where it shows that an increase in load impedance, contributes to an increase in drain current with the same drain voltage swing.

Another way is by having a constant load impedance, but changing the load that is perceived by the amplifier. This technique is called active load modulation,

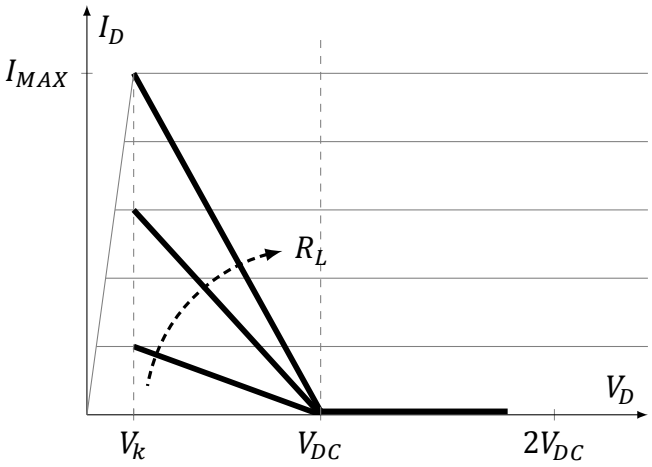



Figure 3.3: Change of the loadline with respect to the change in load impedance.

which uses current injection to change the perceived load. The two main ways of adjusting the ratio between the currents is by changing the amplitude (Doherty) or the phase between them (Outphasing). The remainder of the chapter will discuss the two main load modulation techniques to get a better insight in how it works and the effect on efficiency in power back-off.

## 3.1. Outphasing

Outphasing is an old modulation technique, as it was first introduced in [32] in 1935. Figure 3.4 depicts a simplified diagram of the outphasing system.

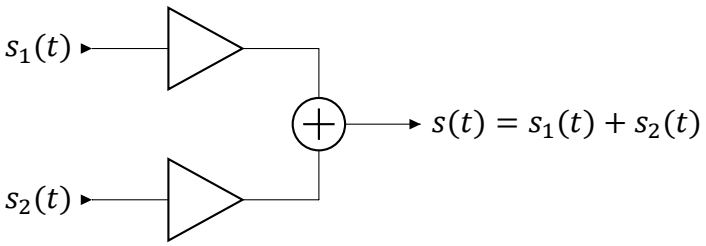



Figure 3.4: Outphasing system diagram.

In an out-phasing system two phase modulated signals are used to create a phase and amplitude modulated output. This is achieved by changing the phase between the two signals [33], as described in Equation 3.3. The addition of the two phase modulated signal can be performed in various ways. One way is to use isolating power combiners, like the wilkinson power combiner. The problem with using these kind of combiners is the isolating properties, which inhibit load modulation due to resistively dissipating the out of phase power. Thus only non isolating power combination is of interest in the scope of load modulation and thus

that will be the only type discussed in this section.

$$\begin{aligned} s_1(t) &= V \cdot \cos(\omega_c t + \theta + \phi) \\ s_2(t) &= V \cdot \cos(\omega_c t + \theta - \phi) \\ s(t) &= s_1(t) + s_2(t) \\ &= V \cdot \cos(\omega_c t + \theta + \phi) + V \cdot \cos(\omega_c t + \theta - \phi), \end{aligned} \tag{3.3}$$

where $\phi$ is the outphasing angle. Which shows the relation between output amplitude and the outphasing angle. Equation 3.3 indicates a major advantage of the outphasing system, which is that both $s_1(t)$ and $s_2(t)$ are constant envelope signals. This enables the usage of high efficiency switch mode power amplifiers. Whereas the combination of the two signals is both a phase and amplitude modulated signal. This illustrates that linear amplification can be performed using non-linear components, also known as LINC [33].

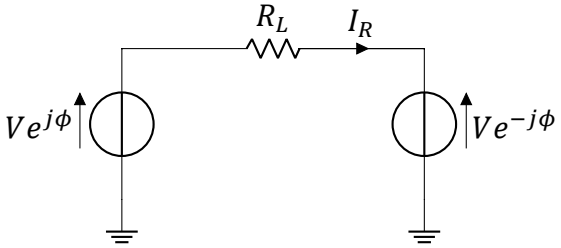



Figure 3.5: Simple outphasing circuit diagram.

To proof that outphasing is indeed a load modulation technique, the impedance seen by each source is calculated. For these calculations the simplified model in Figure 3.5 is used. Nodal analysis leads to the load current $I_R$ in Equation 3.4 [34], [35].

$$I_R = \frac{V}{R}(e^{j\phi} - e^{-j\phi}) \tag{3.4}$$

This load current is now used to determine the impedance seen by each source.

$$Z_1 = \frac{Ve^{j\phi}}{I_1} = \frac{R}{2}[1 - j\cot(\phi)] \tag{3.5}$$

$$Z_2 = \frac{Ve^{-j\phi}}{I_2} = \frac{R}{2}[1 + j\cot(\phi)] \tag{3.6}$$

Both Equation 3.5 and Equation 3.6 show that outphasing is indeed a load modulation technique, as the impedance seen by the active devices is dependent on the outphasing angle. In this case only the reactance changes meaning the loading is complex. This is undesirable, because this does not lead to an increase in efficiency. The loading of both sources is plotted in a smith chart in Figure 3.6.

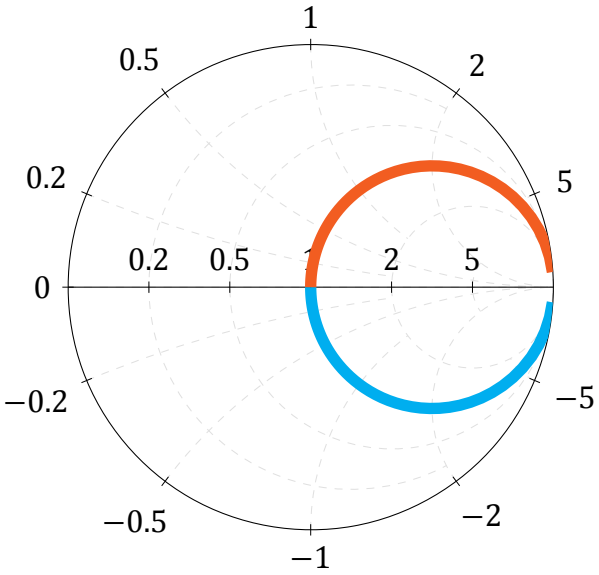



Figure 3.6: Loading conditions of the two amplifiers in an outphasing system.

Thus far there is no real advantage to using a outphasing system using class A, B and C PAs, as the system from Figure 3.5 has similar back-off efficiency behaviour as a transconductance PA. However, this changes when parallel impedances are introduced to each source. This results in the system as depicted in Figure 3.7.

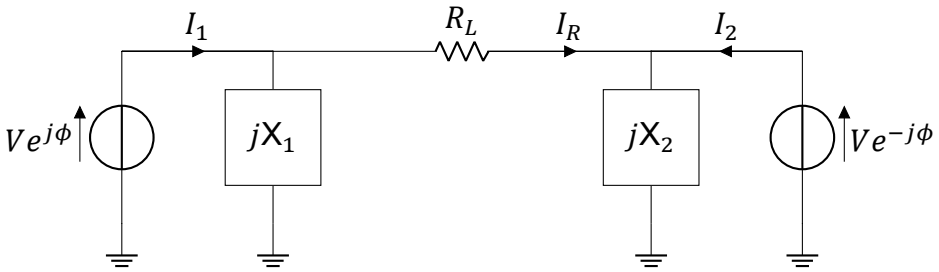



Figure 3.7: Outphasing circuit diagram with parallel impedance compensation.

Again nodal analysis is used to calculate the current supplied by each source.

$$I_1 = V \cdot \left( \frac{e^{j\phi} - e^{-j\phi}}{R_L} - j\frac{e^{j\phi}}{X_1} \right)$$
$$I_2 = V \cdot \left( \frac{e^{-j\phi} - e^{j\phi}}{R_L} - j\frac{e^{-j\phi}}{X_2} \right)$$

Since the impedances are parallel to the sources, it is easier to express them in admittances. The admittances are depicted in Equation 3.7 and Equation 3.8.

$$Y_1 = \frac{I_1}{Ve^{j\phi}} = \left(\frac{1-\cos(2\phi)}{R_L}\right) - j\left(\frac{1}{X_1} - \frac{\sin(2\phi)}{R_L}\right) \tag{3.7}$$

$$Y_2 = \frac{I_2}{Ve^{-j\phi}} = \left(\frac{1-\cos(2\phi)}{R_L}\right) - j\left(\frac{1}{X_2} + \frac{\sin(2\phi)}{R_L}\right) \tag{3.8}$$

The first major difference implied by these equations is that the reactive part is now also dependent on the outphasing angle. Something interesting happens when the admittance is set to $X = X_1 = -X_2$. This leads to the imaginary part of the admittance becoming equal at two points as defined in Equation 3.9.

$$\frac{1}{X} - \frac{\sin(2\phi)}{R_L} = -\frac{1}{X} + \frac{\sin(2\phi)}{R_L} = 0$$

which leads to

$$\sin 2\phi = \frac{R}{X} \tag{3.9}$$

This ratio leads to impedance curves in the smith chart similar to those in Figure 3.8. Where it can clearly be seen that the real axis of the smith chart is crossed twice which lead to peaks in efficiency.

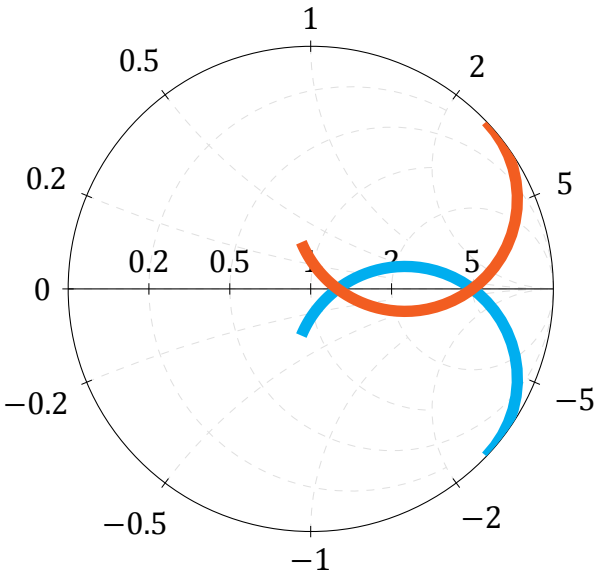



Figure 3.8: Loading conditions of the two amplifiers in an outphasing system with parallel impedance compensation.

To understand the effect of the ratio in Equation 3.9 on the efficiency, the fundamental output power and DC power need to be calculated. The output power is

$$P_{out} = \frac{|s(t)|^2}{2R}$$

where $s(t)$ is the signal from Equation 3.3. Which leads to

$$P_{out} = \frac{V^2}{2R}[1 + \cos(2\phi)]. \tag{3.10}$$

The DC power is dependent on the class of PA used. In this case a class B PA will be used as an example, which leads to a DC power of

$$P_{DC} = V\frac{2}{\pi}(|I_1| + |I_2|) \tag{3.11}$$

for which the currents are calculated as follows

$$I_1 = Ve^{j\phi}\left(\frac{1}{Z_1} - j\frac{1}{X}\right) \tag{3.12}$$

$$I_2 = Ve^{-j\phi}\left(\frac{1}{Z_2} + j\frac{1}{X}\right) \tag{3.13}$$

where

$$Z_1 = R\frac{e^{j\phi}}{\cos(\phi)}$$

$$Z_2 = R\frac{e^{-j\phi}}{\cos(\phi)}$$

Now Equations 3.10 and **??** can be used to calculate the efficiency, which leads to

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{\frac{V^2}{2R}[1 + \cos(2\phi)]}{V^2\frac{2}{\pi}\left(|\frac{1}{Z_1} - j\frac{1}{X}| + |\frac{1}{Z_2} + j\frac{1}{X}|\right)} = \frac{\pi}{4}\frac{1 + \cos(2\phi)}{|\frac{R}{Z_1} - j\frac{R}{X}| + |\frac{R}{Z_2} + j\frac{R}{X}|} \tag{3.14}$$

here the ratio between the resistance and reactance returns, which confirms the notion from before, that the ratio has effect on the efficiency curve. Figure 3.9 shows the exact effect. With decreasing ratio the efficiency peak is moved further into the back-off region.

One assumption that is made throughout this section is that the amplifier acts as a perfect voltage source. In general transistors act closer to a current source, however, it is possible to get relatively close to voltage source operation by using an overdriven class A, B or C [34], switch mode class D [20] or class E [36].

Another problem with outphasing is the fact that the input drive is kept constant. Only the phase difference between the two drive signals is adjusted. This means that at low output power the input power is still the same. This greatly reduces the power added efficiency at power back-off.

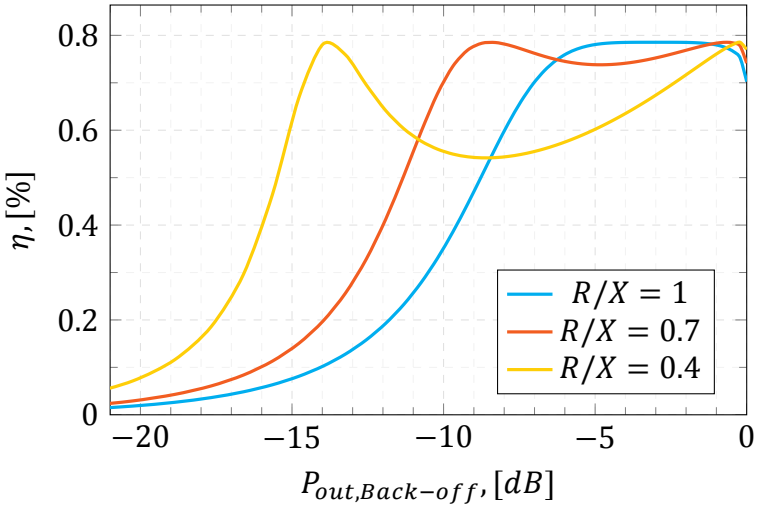



Figure 3.9: Efficiency at power back-off of a outphasing system.

## 3.2. Doherty

Doherty [37] is another technique to increase the efficiency at the power back-off operation of the PA. The general idea behind this technique is again that two amplifiers work together to provide the output power, however, instead the output is the sum of two currents.

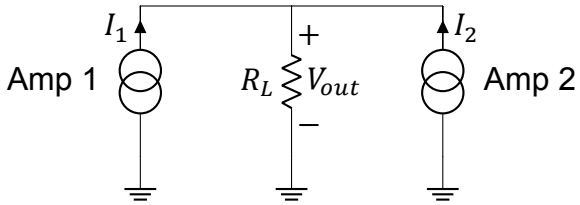



Figure 3.10: Simple load-modulating circuit diagram.

An example of a simple circuit in which the load is modulated is shown in Figure 3.10. The output voltage of the device is determined by both amplifier currents

$$V_{out} = R_L(I_1 + I_2).$$

Load seen by amplifier 1 is

$$Z_1 = R_L\left(1 + \frac{I_2}{I_1}\right), \tag{3.15}$$

thus showing that the load seen by the first amplifier can be increased by injecting a current using a second amplifier. This way the load can be kept at the ideal value at different back-off powers.

The idea is that at low output power levels only one amplifier is turned on, which is called the main amplifier. When a certain output power at input drive $V_{in} = \alpha$ is reached, the main amplifier voltage saturates and the second device,

called the peaking amplifier, turns on to provide the extra power. When the main device reaches saturation the second device starts to inject current in to the load. From Equation 3.15 it is concluded that the impedance seen by amplifier 1, which is taken to be the main amplifier in this example, increases. This increase in perceived load impedance leads to a increase in voltage swing at the drain of the main amplifier, which is undesired. Thus to keep the main device in saturation the two currents must be out of phase. This phase difference is achieved using a $\lambda/4$-transmission line. The basic circuit for a Doherty system is displayed in Figure 3.11. Where the shorted $\lambda/4$-transmission lines provide an open condition for the fundamental and even harmonic shorts. The $\lambda/4$-transmission line between the main amplifier and load is used to increase the effective load impedance seen by the main amplifier in power back-off where the peaking device is off or still not at maximum power. It is important to note that $I_m$ and $I_p$ represent the fundamental current amplitude. The ABCD matrix of the quarter wave transmission line in Figure 3.11 is the following

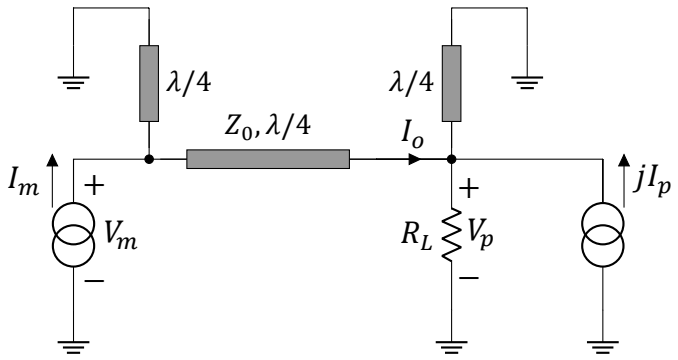



Figure 3.11: Doherty system diagram.

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & jZ_0 \\ j\frac{1}{Z_0} & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}, \tag{3.16}$$

where $Z_0$ is the characteristic impedance of the line. Applying Equation 3.16 to the output $I_o$ and $V_p$ leads to

$$I_o = j\frac{1}{Z_0}V_m \tag{3.17}$$

$$V_p = jZ_0 I_m \tag{3.18}$$

The only remaining relation is found using nodal analysis at the output. This leads to the relation in Equation 3.19.

$$I_o = \frac{V_p}{R} - jI_p \tag{3.19}$$

One thing that is evident from Equation 3.18 is that the voltage at the output of the peaking amplifier is independent on the current supplied by the peaking amplifier [35]. This means that ideally the linearity of the system is entirely defined by the linearity of the main amplifier as long as the voltage $V_m$ is kept below the clipping point. To keep the main amplifier from reaching this point, the relation between the peaking and main amplifier voltage must be found. This is achieved by substituting Equations 3.17 and 3.18 into Equation 3.19.

$$V_m = Z_0 \left[ \left( \frac{Z_0}{R_L} \right) I_m - I_p \right] \tag{3.20}$$

This relation clearly shows that the voltage at the output of the main amplifier is a function of the current delivered by the peaking amplifier. It also implies that if both amplifiers would be on during the full input drive, the ratio between the load resistance $R_L$ and the characteristic impedance $Z_0$ of the quarter wavelength line is of effect. So the real magic happens when the peak current is introduced at a later input drive. With a normalised input drive

$$0 < V_{in} < 1$$

the turn on point $\alpha$ is defined as

$$\alpha = \sqrt{\frac{1}{10^{P_{backoff}/10}}} \tag{3.21}$$

where $P_{backoff}$ is the power back-off point at which the main amplifier saturates and the peak turns on and

$$0 < \alpha < 1$$

leading to the following relations

$$\begin{aligned} I_m &= V_{in}(I_m)_{max} && 0 < V_{in} < 1 \\ I_p &= \frac{V_{in} - \alpha}{1 - \alpha}(I_p)_{max} && \alpha < V_{in} < 1 \\ &= 0 && V_{in} < \alpha \end{aligned}$$

Using these relations the impedance at two instances can be calculated, namely at back-off and at full drive. When the input drive is at the back-off point, the peak amplifier current is 0. Thus according to Equation 3.20 the main amplifier voltage becomes

$$(V_m)_\alpha = V_{DC} = \alpha \frac{Z_0^2}{R_L}(I_m)_{max} \tag{3.22}$$

For efficiency it is desired to keep the main amplifier at its voltage saturation point. Implying that the voltage at the output of the main amplifier is the same at the

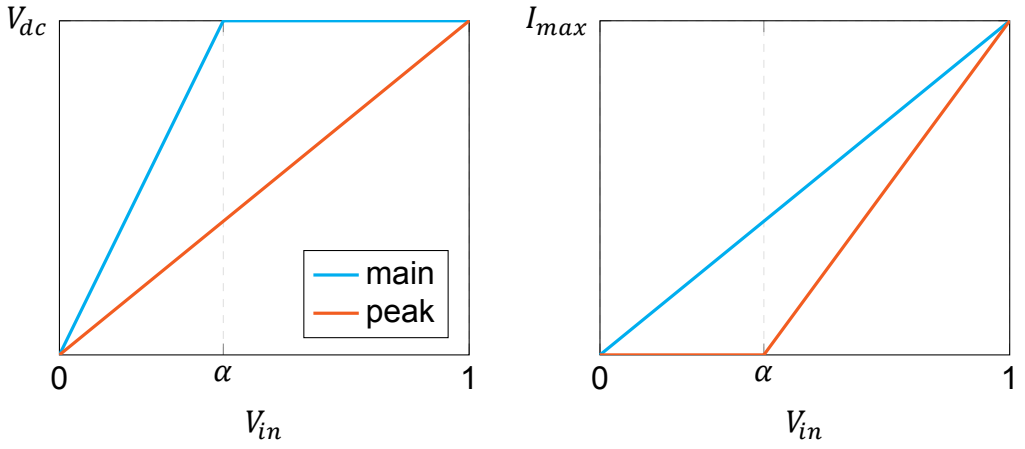
back-off point as at the full drive point. Leading to

$$V_m = V_{DC} = Z_0 \left[ \left( \frac{Z_0}{R_L} \right) (I_m)_{max} - (I_p)_{max} \right] \tag{3.23}$$

Where Equation 3.22 and Equation 3.23 can be solved to calculate the impedances needed, which results in

$$R_L = \alpha \frac{V_{DC}}{(I_m)_{max}}, \quad Z_0 = \frac{1}{\alpha} R_L$$

Figure 3.12 shows two plots of the main and peak amplifier voltage and current amplitudes as function of input voltage.




(a) output voltages (b) output currents

Figure 3.12: Doherty main and peaking amplifier output voltage and current amplitudes.

What is of interest is the effect of this load modulation on the efficiency. For this both the fundamental and DC power need to be calculated. For easy comparison the amplifiers used will be assumed class B as in the outphasing example. Therefore the fundamental output power is

$$P_{out} = \frac{(I_m)_{max} + (I_p)_{max}}{2} V_{DC} \cdot V_{in} \tag{3.24}$$

where $V_{in}$ is the normalised input voltage, which is dimensionless. Up to an input drive voltage of $\alpha$ the peaking amplifier does not contribute to the output power, thus for a class B amplifier the efficiency up to the back off point is

$$\eta_{back-off} = \frac{V_{in}}{\alpha} \cdot \frac{\pi}{4}, \quad 0 < V_{in} < \alpha. \tag{3.25}$$

The DC power of the main amplifier is

$$P_{DC,main} = V_{in} \cdot \left( \frac{(I_m)_{max}}{\pi} \right) V_{dc},$$

and that of the peaking amplifier

$$P_{DC,peak} = \frac{V_{in} - \alpha}{1 - \alpha} \cdot \left( \frac{(I_p)_{max}}{\pi} \right) V_{dc},$$

so the total DC power dissipated by the doherty amplifier is

$$P_{DC} = \frac{V_{DC}}{\pi} \left[ \left( (I_m)_{max} + \frac{(I_p)_{max}}{1 - \alpha} \right) V_{in} - \frac{\alpha (I_p)_{max}}{1 - \alpha} \right]. \tag{3.26}$$

Which can now be used to calculate the efficiency in the region where both the main and peaking amplifier are providing power for the output. This leads to the following efficiency

$$\eta = \frac{\pi}{2} \frac{[(I_m)_{max} + (I_p)_{max}] \cdot V_{in}}{\left[ \left( (I_m)_{max} + \frac{(I_p)_{max}}{1-\alpha} \right) V_{in} - \frac{\alpha (I_p)_{max}}{1-\alpha} \right]}. \tag{3.27}$$

This equation may seem daunting at first, but setting $(I_m)_{max} = (I_p)_{max}$, which is the case for a symmetrical doherty, leads to the following

$$\eta = \frac{\pi}{2} \cdot \frac{V_{in}^2}{3V_{in} - 1}, \quad 0.5 \leq V_{in} \leq 1 \tag{3.28}$$

which indicates that the efficiency of the system drops before it increases to the optimum class B value again. This is because the peaking amplifier has a lower efficiency than the optimum value, but when it first turn on, it contributes very little to the output power, thus the low efficiency has little effect. The further the power contribution of the peaking amplifier increases the lower the efficiency until the efficiency of the peaking amplifier is high enough that it increases the overall efficiency of the system. Figure 3.13 shows the efficiency curve of a symmetrical doherty.

## 3.3. Conclusion

Most modulations have a peak to average power ratio (PAPR) of larger than one, so it is desired to have a high efficiency in power back-off. Two active load modulation techniques were introduced in this chapter, outphasing and doherty. The former uses the phase difference between two signals to amplitude modulate the output signal. A huge advantage of outphasing is that it does not require linear devices for linear amplification, which allows for the use of high efficiency switch

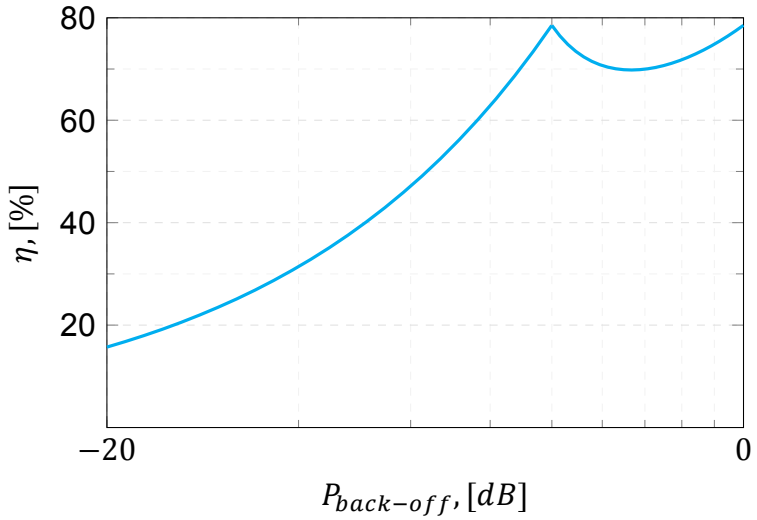



Figure 3.13: Efficiency in power back-off of a symmetrical doherty class B amplifier.

mode amplifiers. Unfortunately, the drawback of outhphasing is that the conversion from amplitude to phase is non linear and leads to an undesired increase in input signal bandwidth, while the RF bandwidth is small, which in turn limits the video bandwidth.

# 4

# Multi-Phase Theory

In wireless communication a modulated waveform of the form

$$s(t) = \boldsymbol{A}(t) \sin\left[2\pi \boldsymbol{f}(t) \cdot t + \boldsymbol{\theta}(t)\right] \tag{4.1}$$

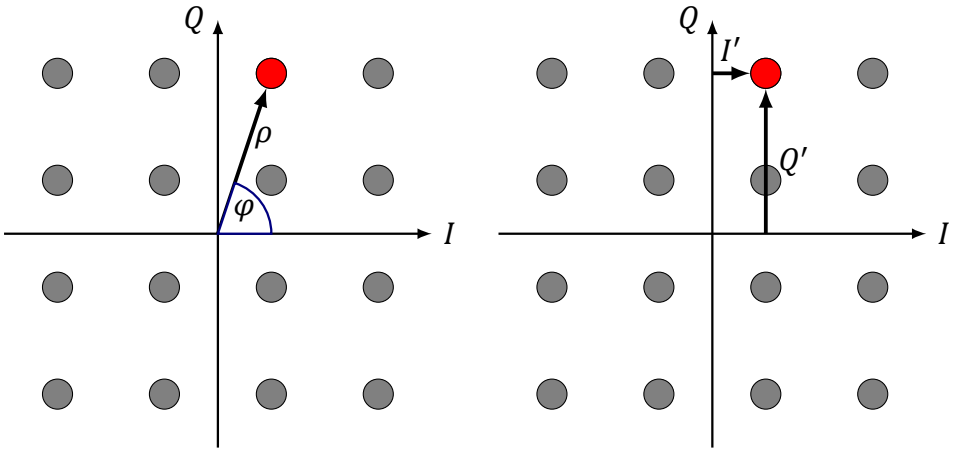
is used, where the bold parameters $\boldsymbol{A}(t), \boldsymbol{f}(t)$ and $\boldsymbol{\theta}(t)$ correspond to different variables that are changed when handling various modulation schemes. Of these parameters $\boldsymbol{A}(t)$ and $\boldsymbol{\theta}(t)$ are the most common to use for modulation. A few of the modulation schemes that use these two parameters include but are not limited to QAM, AM, PSK and MSK. There are two key architectures for representing these modulated signals that are discussed in this chapter. Both these architectures have their advantages and disadvantages, which need to be understood. To remedy these disadvantages a new architecture is introduced to bridge the gap. The main focus here is a digital system implementation, the discussed architectures can therefore be presumed digital unless stated otherwise.

## 4.1. Common architectures

Today there are two main transmitter architectures, polar and quadrature. The former represents the signal using the orthogonal phase and amplitude parameters. This is illustrated in Figure 4.1a and mathematically by:

$$p(t) = \boldsymbol{A}(t) \sin(\omega_0 t + \boldsymbol{\theta}(t))$$

This is an straightforward way of representing the information vector, however, combining the amplitude and phase information in a practical transmitter requires special attention on aligning the two. An example of such a transmitter is given displayed in Figure 4.3.




(a) Polar representation (b) IQ representation

Figure 4.1: 16-QAM constellation point representation.

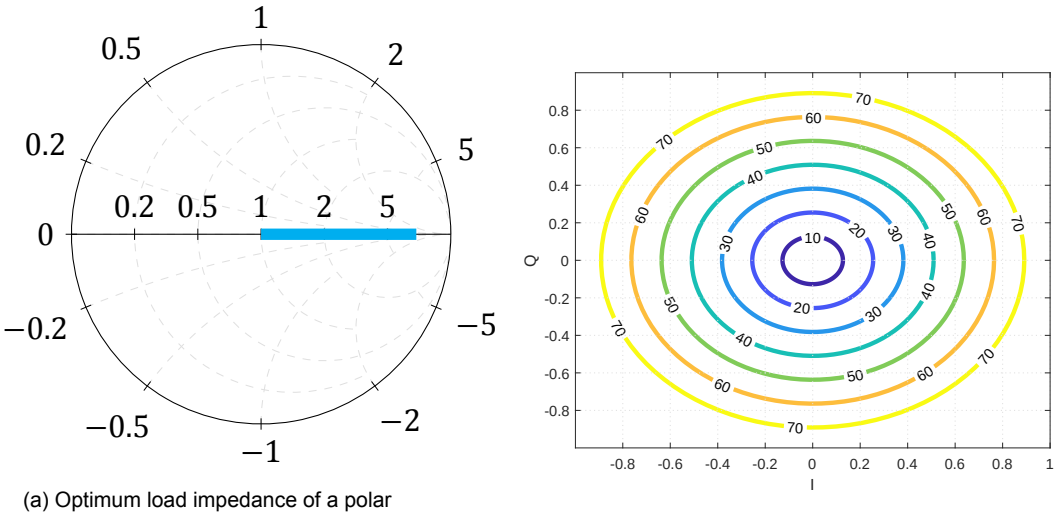
### 4.1.1. Polar

The majority of the fully digital architectures use a polar implementation [38], [39]. A major advantage of the polar architecture is its high efficiency and orthogonal phase and amplitude behaviour, which exhibit very low interaction in practical implementation. The PA in a polar transmitter using efficiency enhancement is often based on a form of supply voltage modulation. This could be envelope tracking (ET) or envelope elimination restoration (EER) [40]. Using Equation 3.2, which is repeated here

$$\eta = \eta_{max} \frac{I_1}{V_{DC}} R_L$$

shows that if the fundamental drain current, $I_1$, is lower than the maximum current, $I_{max}$, the efficiency drops linearly, since $I_1 \cdot R_L$ becomes less then $V_{DC}$. This assumes the use of a constant supply voltage and load resistance. Equation 3.2 indicates that the efficiency is only dependent on the drain current amplitude, which means the efficiency drop is equal at all phase angles. This is demonstrated in Figure 4.2, where the efficiency contours are circles. Increasing the load impedance in power back-off, e.g. by load modulation, increases the efficiency there as well. The other option is to keep the optimum load impedance equal to the presented one and modulate the supply voltage together with the drain current. The independence of the efficiency on the signal angle makes the polar architecture favourable for high PAPR signal modulations, commonly used in modern telecommunication standards.

Unfortunately there are a few problems that plague the use of a the polar architecture. One of which is a phenomenon known as bandwidth expansion. This is caused by non-linear operation when transforming the I and Q signal into a phase and amplitude modulated signal representation, which are essential to the polar system operation. Both I and Q vectors are amplitude modulated signals. The




(a) Optimum load impedance of a polar system

(b) Efficiency contour of a polar transmitter

Figure 4.2: The loading and the efficiency contours of a Cartesian transmitter.

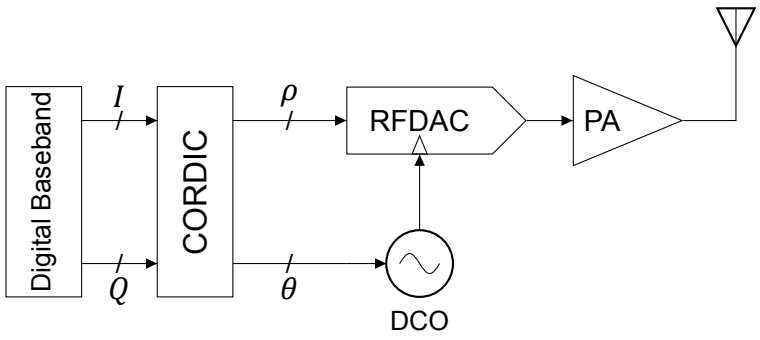



Figure 4.3: Digital polar architecture diagram [41].

amplitude and phase are calculated using the following formulae, respectively

$$\rho(t) = A(t) = \sqrt{Q(t)^2 + I(t)^2}, \tag{4.2}$$

$$\theta(t) = \tan^{-1}\left(\frac{Q(t)}{I(t)}\right). \tag{4.3}$$

Due to the large increase in bandwidth especially in the phase of the signal an extremely wideband phase modulator is needed, which typically limits the achievable maximum bandwidth of a polar system. Figure 4.4 shows the spectral power density of the Cartesian, amplitude [$\rho(t)$] and phase [$\theta(t)$] of a 64-QAM modulated signal. The figure clearly indicates that the bandwidth of the amplitude and phase signals are extremely large compared to the original Cartesian representation.

To better understand this expansion, consider a quick change in phase of the polar transmitter, e.g. when the signal crosses or gets in close proximity to the origin. This zero crossing requires only a small change in value for the I and Q vectors, but the related phase description basically needs to wrap around and so the related RF carrier signal needs a well controlled, but almost instantaneous

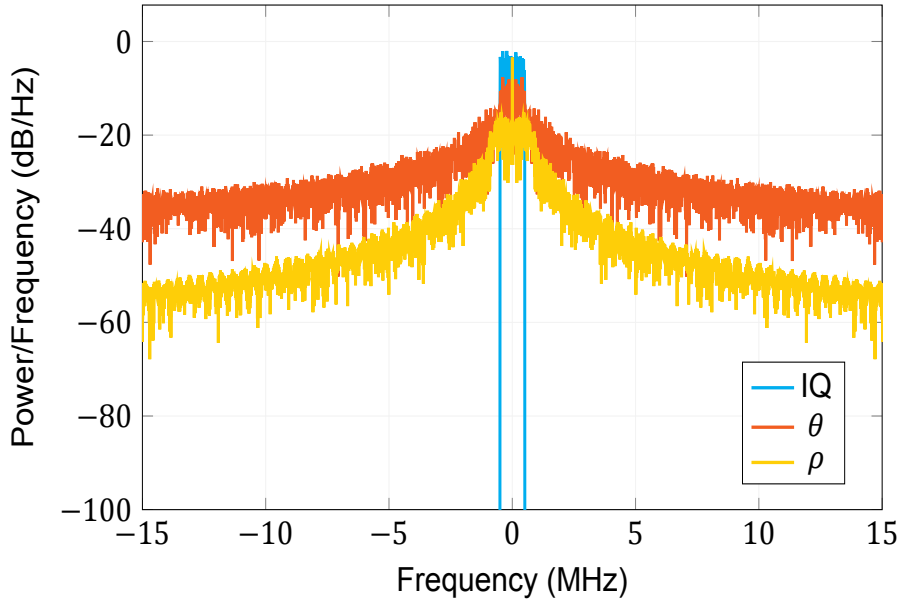



Figure 4.4: Spectrum of the branch signals in a polar and Cartesian transmitter. Displaying the bandwidth expansion of the amplitude and phase signals due to non-linear operations.

fast phase change [42]. To get the most accurate information on the phase, the sample frequency should be high. A high sampling frequency conveys the larger signal bandwidth needed to describe the phase.

The out-phasing amplifier, discussed in section 3.1, suffers even more from this problem as all the information is imposed on two phase modulated signals. When comparing linear IQ operation (e.g. class-AB) and the gradual transition to a pure out-phasing signal representation, for a 5 MHz bandwidth signal. One can observe a ten times larger bandwidth requirement to precisely represent the original TX signal. The amount of bandwidth expansion for this transition to out-phasing is depicted in Figure 4.5[43].

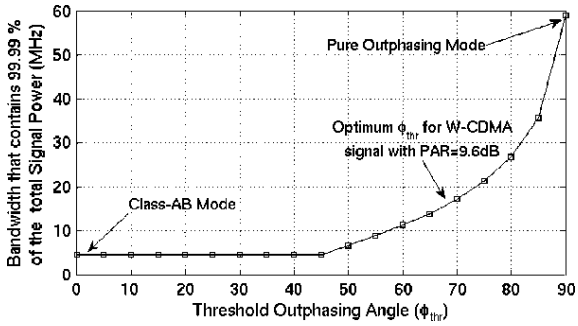



Figure 4.5: Amount of bandwidth expansion when transitioning from linear IQ to out-phasing for a 5 MHz bandwidth TX signal.

Another issue in the polar architecture is timing. As seen in Figure 4.3, the AM and PM paths are extremely different, which means they are likely to have different delays and requires careful (re)alignment, this is a common problem faced in polar transmitter design. This problem is further enhanced by the fact that the phase and

amplitude paths are operated on separate clock domains. Due to the asymmetric signal operation, also the clock tree implementations are different. So, even if the clock rates are the same, the clock tree delay variations between the two paths lead to mismatch in timing alignment. For WCDMA and 4G applications this alignment needs to be better than a nanosecond [44].

### 4.1.2. Cartesian

Apart form the polar architecture there is Cartesian or IQ signal representation. A Cartesian transmitter consists of two signal paths. The In-phase [$I(t)$] and Quadrature [$Q(t)$] path. These signals have a 90° phase difference. They typically directly represent the digital baseband data and therefore do not under go a non-linear operation. Depicted as follows

$$I(t) = A(t)\sin(\theta(t)) \tag{4.4}$$

$$Q(t) = A(t)\cos(\theta(t)) \tag{4.5}$$

To compose the TX signal, the I and Q vectors need only be added, which allows for a relaxed transmitter design with respect to bandwidth. A system diagram of the Cartesian architecture is displayed in Figure 4.6.

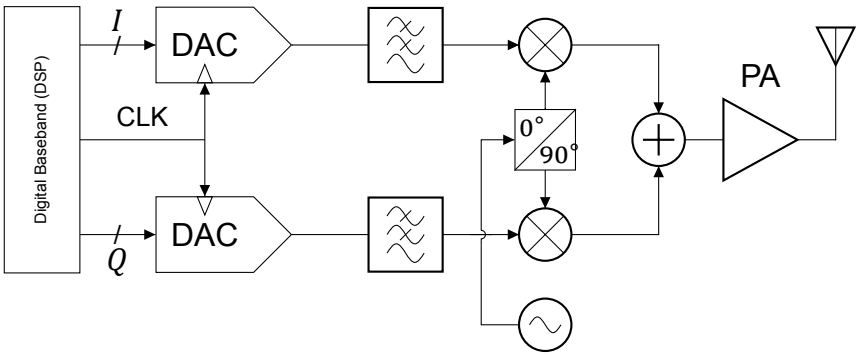



Figure 4.6: Conventional IQ architecture diagram [41].

In contrast with a polar system which has a single vector with a magnitude $\hat{\rho}(t)$ and a phase $\hat{\theta}(t)$. In a Cartesian system these are two to be summed vectors that are 90° out of phase. This phase difference between the vectors limits the achievable output power and efficiency with respect to a polar system.

Therefore, in the conventional analogue Cartesian system the I and Q signals are combined before the PA stage, as depicted in Figure 4.6. This leads to high linearity requirements of the PA meaning a linear class type needs to be used. This later requirement yields many challenges in their actual implementation with related design trade-offs. For this reason we focus in this thesis on TX architectures that are compatible with digital techniques. So our next step is implementing everything up to and including the PA in the digital domain. For such an all digital implementation, the output is delivered by a digital to RF amplitude converter

(DRAC). The digital implementation leads to a high integration and configurability. It also allows for the use of high efficiency switch mode PAs.

Within a Cartesian all digital RF transmitter concept the signals are now combined at the output of the high power components, the DRACs, as seen in Figure 4.7. As discussed in chapter 3, having two active devices that inject current into the same load, which leads to load modulation. Which is also the case in the all digital RF transmitter.

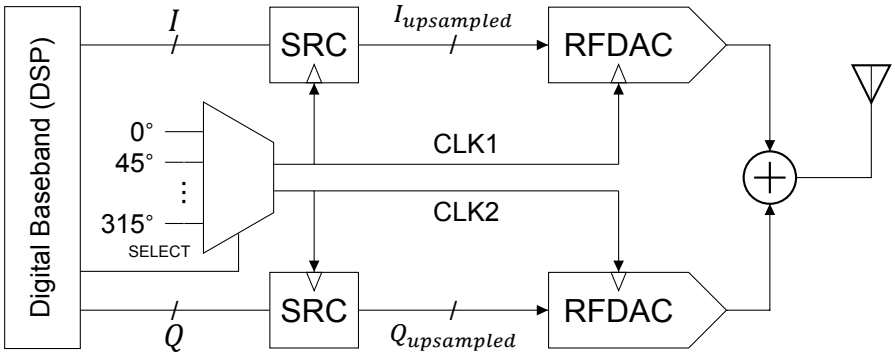



Figure 4.7: All-digital IQ architecture diagram [41].

When both In-phase and Quadrature signals have the same maximum magnitude the output signal of the transmitter is

$$V_{I,Q} = A(t) \cdot \cos(\vartheta/2) \tag{4.6}$$

where $A(t)$ is the amplitude of the resulting output signal and $\vartheta$ equals the phase between the two summed signals, which for a quadrature system is $\pi/2$. Comparing the output power to that of a polar transmitter leads to

$$P_{rel} = \frac{(A(t)\cos(\vartheta/2))^2}{A(t)^2} = 0.5. \tag{4.7}$$

Following these calculations the output power capability of a quadrature system is around half that of a polar system. The next step would be to calculate the ratio between polar and Cartesian transmitter with respect to the average power as a function of the signal angle [$\theta(t)$]. From [45] the relative output power of a Cartesian transmitter for an OFDM signal is

$$\overline{P_{rel}} = \frac{1}{2\pi}\int_0^{2\pi} \frac{1}{(\cos(\theta)+\sin(\theta))^2} d\theta = \frac{2}{\pi} \tag{4.8}$$

Thus the average output power of a Cartesian system for an OFDM signal is on average $2/\pi$ or approximately 2 dB lower.

The lower fundamental output power of signals with a phase of $0 < \theta(t) < \pi/2$ results in a lower efficiency in this region as well. The largest effect will again be at

the region where the in-phase and quadrature signals have the same magnitude. Simulating the output of a transmitter results in the efficiency distribution as shown in Figure 4.8.

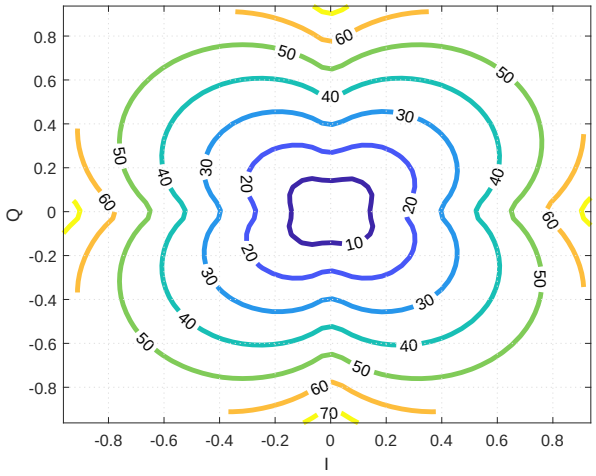



Figure 4.8: Constellation diagram efficiency contours of an IQ system

The lower output power and efficiency, in the areas where both I and Q have a comparable value, is because of the complex loading the two amplifiers cause on each other. This loading condition is displayed in Figure 4.9.

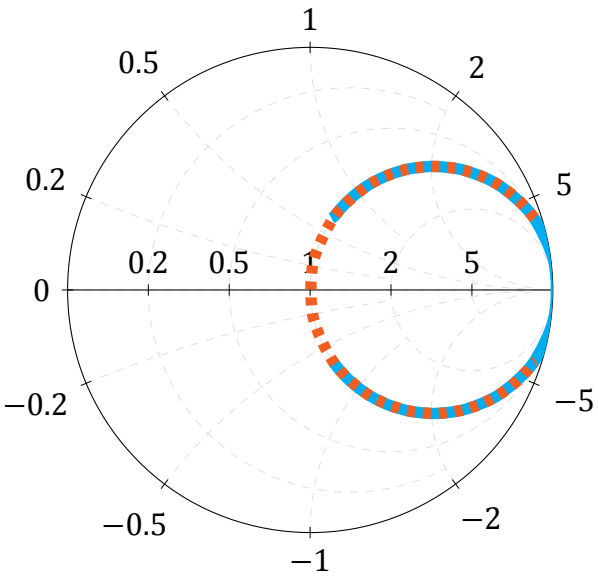



Figure 4.9: Loading conditions of the two amplifiers in an Cartesian system

The big advantage of the Cartesian system is the fact that no non-linear operations have to be performed on the generation of the signals. This retains the original bandwidth of the baseband signal. The spectrum of the IQ signal was already given in Figure 4.4 where it was compared to the bandwidth of the amplitude and phase signal of a polar architecture. The figure clearly shows the much

smaller bandwidth compared to polar. This relaxes the design of the Cartesian transmitter.

Another difference with respect to polar are the identical paths for the in-phase and quadrature signals. These identical paths makes delay difference less pronounced and allows retiming of the signals in the output stage. This solves the time alignment issue that is notorious for the polar architectures.

## 4.2. Multi-phase

Until now the advantages and disadvantages of polar and Cartesian transmitters have been discussed, an overview of the verdict is summarised in Table 4.1.

Table 4.1: Overview of advantages and disadvantages of Polar and Cartesian

| Metric | Polar | Cartesian |
|---|---|---|
| Bandwidth | multiple of BB-BW | equal to BB-BW |
| Average Relative Output Power | 0dB | -2dB |
| Ideal Max. Efficiency | 100% $\eta_{class}$ | 63.6% $\eta_{class}$ |
| Re-timing | issue | no issue |

The idea to combat the efficiency and output power problem is by using more phases than in the standard quadrature approach. This idea was first described in [46] and later implemented for a switched capacitor approach in [47]. The concept will be more deeply discussed in this chapter.

Instead of using the standard four phases of IQ (0,90,180,270) extra phases are introduced. The same as with a Cartesian system, two amplitude modulated signals are summed. Due to this similarity with Cartesian, the same TX architecture as in Figure 4.7 can be used. The only difference is the amount of clocks needed for the radio frequency digital to analog converter (RF-DAC), as these provide the phase difference between the vectors. A multiplexer is used for the different clocks. To ensure linearity the clock of an RF-DAC is only switched when the output of the RF-DAC is low. This leads to each of the RF-DACs being driven by only half of the total clocks; i.e. RF-DAC1 by the clock with phases $0°, 90°, 180°$ and $270°$, whereas RF-DAC2 is driven with the phases $45°, 135°, 225°$ and $315°$. The constellation point mapping is displayed in Figure 4.10 with eight phases, where the one RF-DAC only uses the blue phases and the other only the black ones. A data point will always be represented by two adjacent vector phases. Thus point A will only be represented using phases $I'$ and $Q'$.

This reduction in the angle between adjacent phases increases the efficiency. Meanwhile it keeps the linear process of adding two vectors, this means the use of similar architectures as used for the familiar Cartesian transmitter. There will be more points where peak power is reached by the output of the transmitter. This is best illustrated by Figure 4.11b.

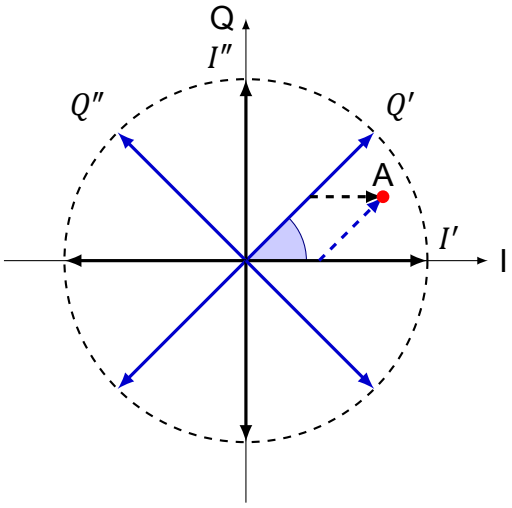
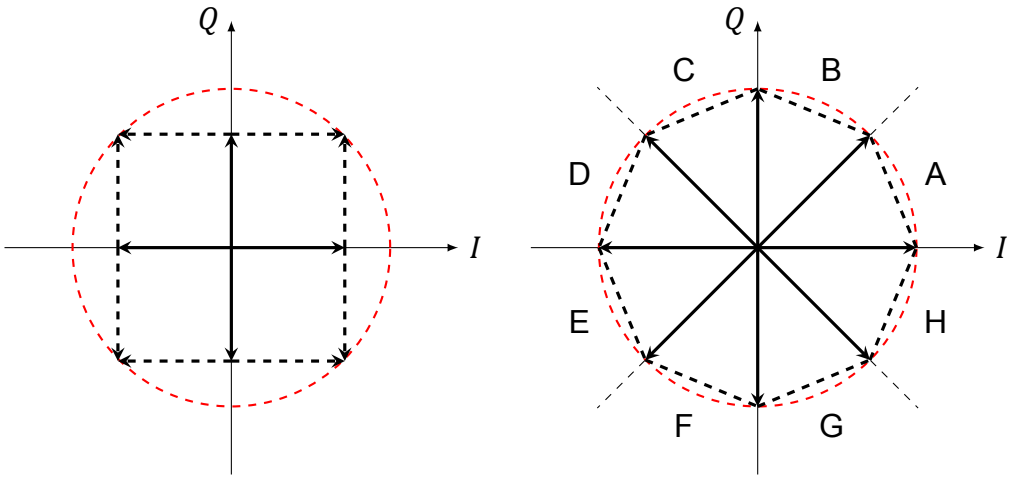



Figure 4.10: Phases and data representation in 8-Multi-Phase




(a) quadrature system (b) multiphase system

Figure 4.11: Peak output power of the combinations of the peak of adjacent phases

The power output is compared with that of a quadrature system, which is displayed in Figure 4.11, where the peak output power is represented by the red circle. The same as with the Cartesian transmitter, the output power of the of the system is lowest at the moment where the two adjacent phases are equal. Output power of the multiphase system can also be calculated using Equation 4.7, where in this case the angle $\vartheta$ is $\pi/8$. This leads to a lowest relative output power of $-0.69$ dB, which equates to an increase of 2.3 dB. If two times the phases are introduced again, this relative power can be decreased to $-0.17$ dB. Thus further increasing the amount of phases shows that the power output approaches that of a polar transmitter. This relative output power is displayed in Figure 4.12. The figure also indicates that introducing more than 32 phases has minimal increase (0.03 dB) in output power.

This increase in output power at the lowest points, signifies that the average

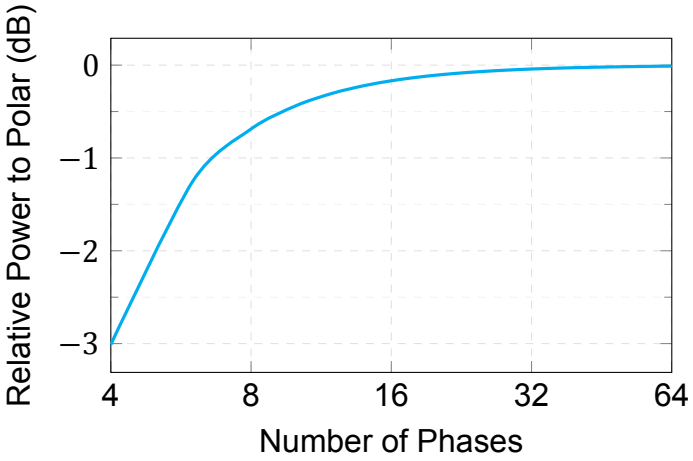



Figure 4.12: Output power relative to a polar transmitter with respect to the amount of phases used, where 4 is the standard Cartesian IQ transmitter.

output power also increases. To calculate this increase the mapping of a signal onto the multi-phase phases needs to be found. The general mapping is shown in Table 4.2. For the following calculation the equations from W. Yuan [45] will be used, where the amplitude of the two adjacent phases is as follows

$$I' = A(t)\cos(\pi/M) \cdot \frac{\sin(2\pi/M)}{\sin[2\pi/(M-\phi)]} \tag{4.9}$$

$$Q' = A(t)\cos(\pi/M) \cdot \frac{\sin(2\pi/M)}{\sin(\phi)} \tag{4.10}$$

$$\phi = \theta - \frac{2\pi}{M} \cdot m \tag{4.11}$$

where $M$ is the number of phases used, $m$ the segment and $\theta$ the angle of the combined signal. After some calculation, which need not be repeated here, W. Yuan found the output power relative to a polar transmitter to be the following

$$\begin{aligned} \overline{P_{rel}} &= \frac{1}{2\pi}\int_0^{2\pi} \frac{\sin^2[(M-2)/\pi/M]}{(|\sin(2\pi/M-\phi)|+|\sin(\phi)|)^2} \\ &= \frac{M\cdot\sin^2[(M-2)/\pi/M]}{2\pi[1-cos(2\pi/M)]}\cdot\tan(\pi/M) \end{aligned} \tag{4.12}$$

This equation calculates the relative output power for when the signal phase ($\theta$) is uniformly distributed between $0$ and $2\pi$. This results in the power curve of Figure 4.13. The figure shows that the initial doubling of the amount of phases already leads to an average relative power of $-0.46$ dB, which is an increase of 1.5 dB in relative average output power. Another doubling of the phases leads to an even further increase to $-0.11$ dB.

Not only does this smaller angle between adjacent phases lead to an increase in output power, but also an increase in efficiency.

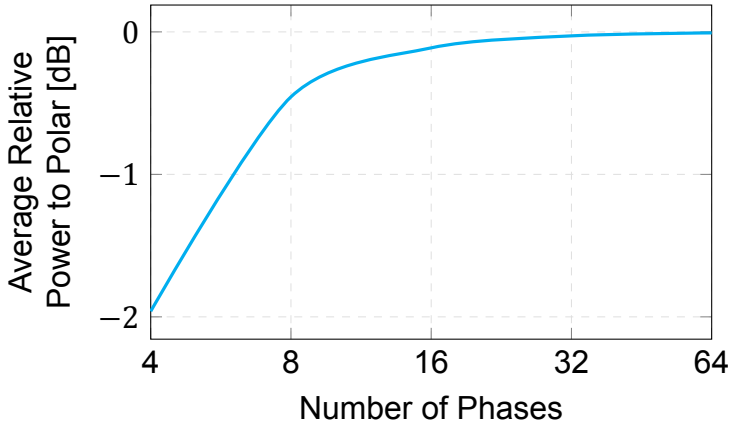
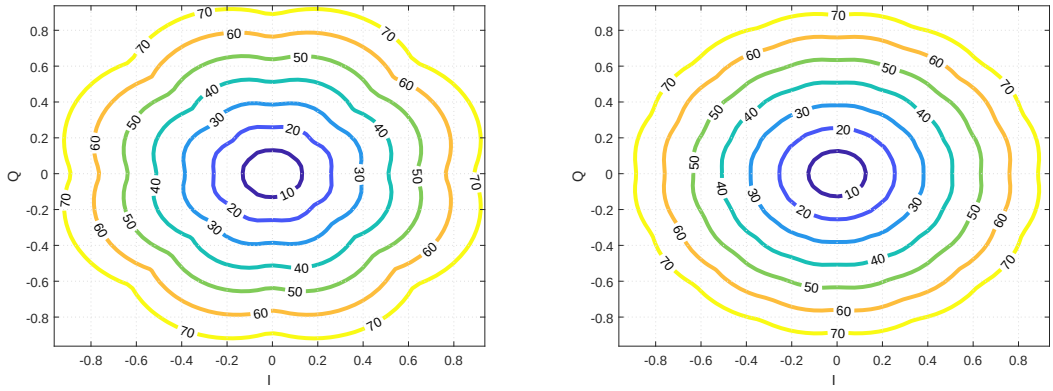



Figure 4.13: Average output power for a signal with uniformly distributed phase relative to a polar transmitter with respect to the amount of phases used, where 4 is the standard Cartesian IQ transmitter.

This increase in power and efficiency is because Multi-Phase (MP) reduces the undesired complex load modulation. However, it works a bit differently than the load modulation techniques related to efficiency enhancement discussed in chapter 3. Instead of increasing the power and efficiency in power back-off, it equalises the efficiency for possible signal angles in the IQ diagram, which is best shown using the efficiency contours in Figure 4.14. This equalisation leads to an increase in average efficiency as depicted in Figure 4.13.



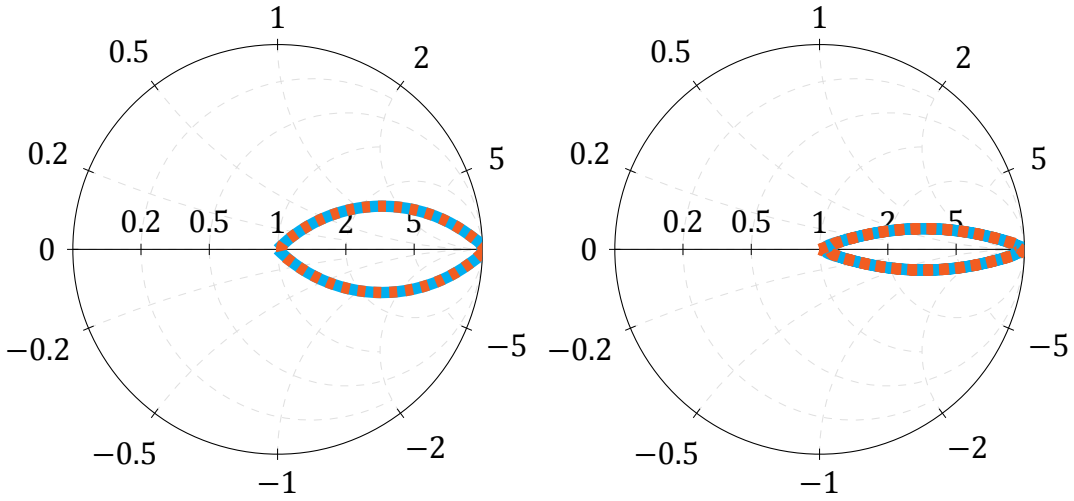

(a) 8 phases

(b) 16 phases

Figure 4.14: Constellation diagram efficiency distribution of Multi-Phase systems.

The plots in Figure 4.15 show that increasing the amount of phases leads to a loading condition closer to that of polar.

One implementation of the MP system has already been created and tested in [45]. In this implementation they use a switched capacitor amplifier. In a switched capacitor amplifier the digital code word is translated to an analogue amplitude by means of switching on all or some of the capacitors. A problem with capacitor arrays on chip is their size. Often these arrays consume a large area, which makes




(a) 8 phases (b) 16 phases

Figure 4.15: Loading condition of the two amplifiers in a Multi-Phase systems

them cost inefficient and less linear since the physical location of the switched element affects its electrical performance. By omitting the capacitors, the size and thus cost of the chip is reduced.

In [45] the transformation from Cartesian to MP was performed using trigonometric functions, which again are non-linear. Whereas, in this report the transformation is performed using simple subtraction and multiplication, which is linear. This linearity has a great advantage since it allows an easy implementation on chip. Meaning that no extensive signal processing is needed on the user side since the digital TX can be driven using the conventional Cartesian signals.

## 4.3. Practice

The theory shows that MP has a considerable efficiency increase with respect to Cartesian, without the bandwidth expansion experienced in a polar architecture. The next step would be to create a system that is able to implement signals using polar, cartesian and multi-phase. This implementation uses both Matlab™ and Keysight ADS™, where the former generates the signals and the latter runs the circuit implementation. For all the architectures a 1 MHz 64-QAM signal is used with a PAPR of $-6.6$ dB.

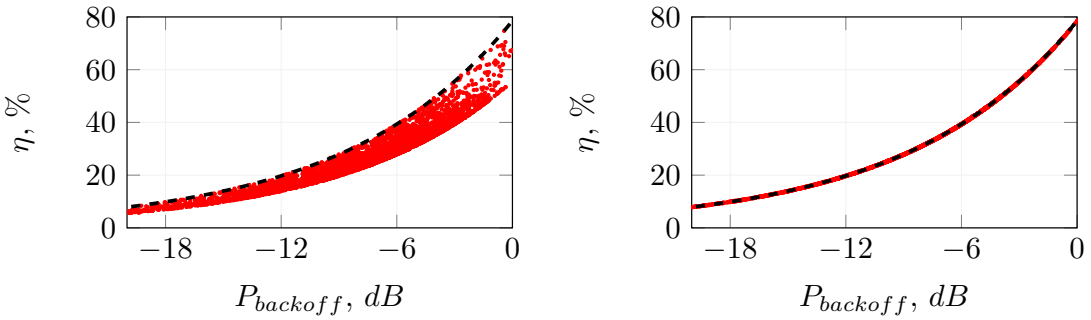
The best way to show the efficiency improvement is using Figures 4.16 and 4.17 where the transmitter architecture from Figure 4.7 is used for polar, Cartesian and MP. The same 64-QAM signal is transmitted using all architectures and the efficiency as function of power back-off is displayed. It is evident that the efficiency at the same output powers does not increase.

From a quick glance at Figure 4.16, a huge difference is immediately noticeable. Which is the large spread visible in the efficiency. Even at peak output power the efficiency for the cartesian architecture ranges from close to 56 % to the ideal

Table 4.2: vector description in the different architectures

| Segment | Polar | Cartesian | MP Cartesian |
|---|---|---|---|
| **A** | $\rho = \sqrt{I^2 + Q^2}$<br>$\varphi = \tan^{-1}\left(\frac{Q}{I}\right)$ | $I + jQ$ | I'=\|I\|-\|Q\|<br>Q'=$\sqrt{2}$Q |
| **B** | | | I"=\|Q\|-\|I\|<br>Q'=$\sqrt{2}$I |
| **C** | | | I"=\|Q\|-\|I\|<br>Q"=$\sqrt{2}$I |
| **D** | | | I'=\|I\|-\|Q\|<br>Q"=$\sqrt{2}$Q |
| **E** | | | I'=\|I\|-\|Q\|<br>Q'=$\sqrt{2}$Q |
| **F** | | | I"=\|Q\|-\|I\|<br>Q'=$\sqrt{2}$I |
| **G** | | | I"=\|Q\|-\|I\|<br>Q"=$\sqrt{2}$I |
| **H** | | | I'=\|I\|-\|Q\|<br>Q"=$\sqrt{2}$Q |

class-B 78.5 %. This is the efficiency drop caused by the complex loading on the active devices.




(a) Cartesian

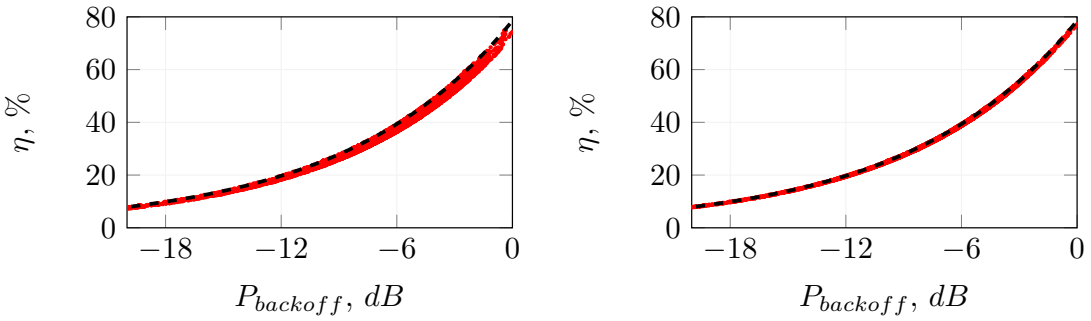
(b) Polar

Figure 4.16: Efficiency curve vs power back-off of a 64QAM signal using Cartesian and Polar compared to the ideal class B efficiency (dashed).

By introducing more phases, and thus less complex loading of the active device, the spread of the efficiency is decreased, which is evident from Figure 4.17.

Figures 4.18 and 4.19 show the efficiency per data point of a 16 times oversampled 64-QAM signal. Here the efficiency increase from cartesian to MP for a modulated signal becomes abundantly clear, from the absence of blue in the plot for cartesian. For each plot the average efficiency is calculated and summarised in Table 4.3, showing an increase of 6 % from cartesian to MP.

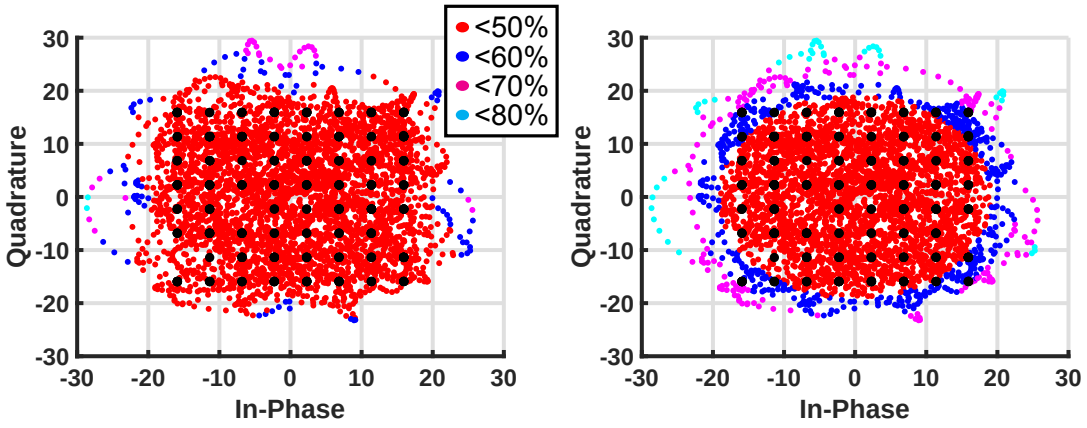
Using a symmetrical Doherty amplifier to increase the efficiency in power back-off, even further enhances the visual of the improvement on efficiency as is seen




(a) 8 phases (b) 16 phases

Figure 4.17: Efficiency curve vs power back-off of a 64QAM signal using Multi-phase

in Figures 4.20 and 4.21. The 16-MP architecture is nearly idenctical to that of polar, with the average efficiency just 0.6 % less. Thus clearly indicating that the efficiency of a polar system can be reached with a linear conversion from IQ.




(a) Cartesian (b) Polar

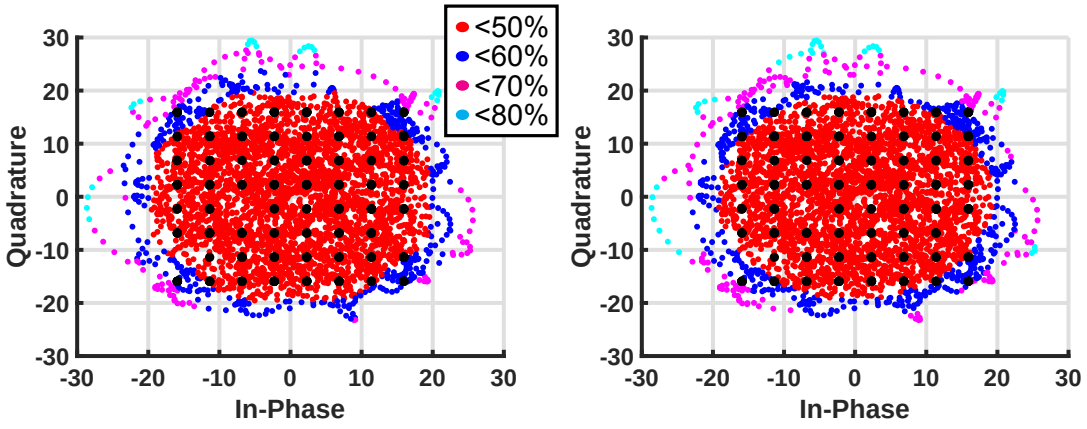
Figure 4.18: Efficiency per sample of a 16 times oversampled 64-QAM signal using a class-B PA for polar and cartesian.

Table 4.3: Average efficiency and linearity measures of the different architectures for a 64-QAM signal.

| Metric | Setup | Polar | Cartesian | 8 Multi-Phase | 16 Multi-Phase |
|---|---|---|---|---|---|
| Average | Conventional | 36.0% | 28.2% | 34.3% | 35.6% |
| Efficiency [%] | Doherty | 60.0% | 47.0% | 57.1% | 59.4% |

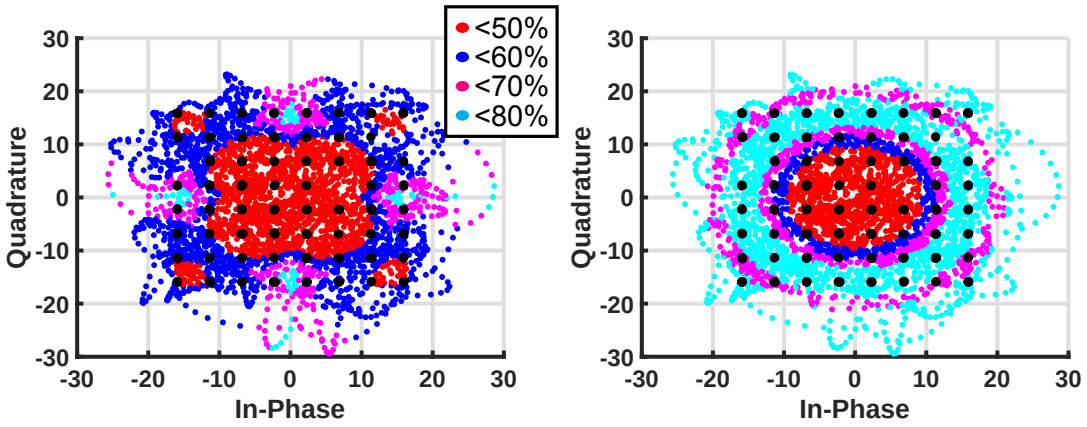
## 4.4. Conclusion

An overview of the advantages and disadvantages of MP are displayed in Table 4.4. The bandwidth is in principle equal to that of a Cartesian system, because the signal conversion is a linear process. Re-timing issues are also the same as result of using an identical system to Cartesian and can be solved in the hardware.



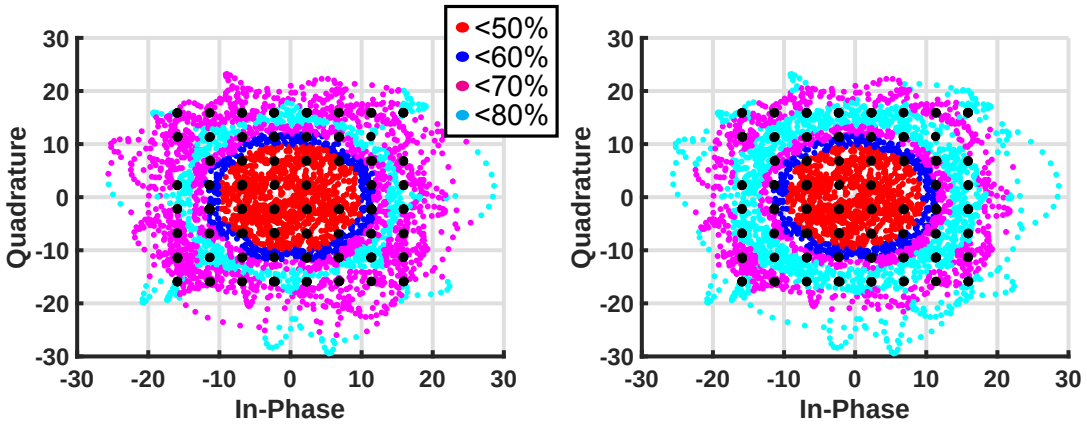

(a) 8 Multi-Phase (b) 16 Multi-Phase

Figure 4.19: Efficiency per sample of a 16 times oversampled 64-QAM signal using a class-B PA for MP and 16MP.




(a) Cartesian (b) Polar

Figure 4.20: Efficiency per sample of a 16 times oversampled 64-QAM signal using a Doherty class-B PA for polar and cartesian.




(a) 8 Multi-Phase (b) 16 Multi-Phase

Figure 4.21: Efficiency per sample of a 16 times oversampled 64-QAM signal using a Doherty class-B PA for MP and 16MP.

More work on this is currently performed within the Diplomat project. The output power and efficiency are higher than that of a Cartesian transmitter and even approach that of a polar architecture, for an increasing number of phases. Due to the linearity of the transformation from Cartesian to MP it is easily implemented on chip.

Table 4.4: Comparison of Multi-Phase with respect to Polar and Cartesian

| **Metric** | **Polar** | **Multi-Phase** | **Cartesian** |
|---|---|---|---|
| Bandwidth | multiple of BB-BW | equal to BB-BW | equal to BB-BW |
| Average Relative Output Power | 0dB | $-0.46$ dB | -2dB |
| Ideal Max. Efficiency | 100% $\eta_{class}$ | 90% $\eta_{class}$ | 63.6% $\eta_{class}$ |
| Re-timing | issue | possible | no issue |

# II

# Master Thesis

# 5

# Implementation

As previously discussed the all-digital transmitter allows for the use of high efficiency switch mode amplifiers. However, as discussed in chapter 2 the harmonic impedance matching network of the switch mode amplifiers often inhibit wideband operation. The idea behind the multi-phase architecture is to reach a higher average efficiency with respect to cartesian and a wider video bandwidth compared to polar. In this work these principles are of greatest concern. For this reason the termination network of a class-B type amplifier will be used, leading to the implementation of a digital class-B/class-C like transmitter. The digital case is somewhat different than the conventional one. The differences are discussed later in this chapter. First the transistors used are characterised, so that their values can be used during the comparison.

## 5.1. Characterisation

Before starting the design of the amplifier the transistors that are used must be characterised. This is essential for the design of the output match. The active device used will be an RF-DAC designed by R. Bootsman. A detailed characterisation is performed in [48], where both the input and output characteristics are determined of the GaN and LDMOS transistors, from Fraunhofer and Ampleon, respectively. These transistors are already part of the RF-DAC, meaning that the input characteristics are not of any importance, since these will be handled in the digital domain. The relevant parameters are displayed in Table 5.1.

For the design of the first polar RF-DAC a class-BE matching network was used, so it is still useful to look at the $I_{DS} - V_{DS}$ curve in Figure 5.1. The plot shows that at lower $v_{ds}$ the drain current peaks. This peak increases at higher drain currents, yielding non-linear effects.

Moreover, Figure 5.1 also demonstrates the knee voltage $v_k$, which is somewhere around 4 V. Using this together with the parameters from Table 5.1 leads

Table 5.1: Hardware parameters [48].

| Quantity | GaN25 | | LDMOS LM8 | |
|---|---|---|---|---|
| | min | max | min | max |
| TGW [mm] | | 4.8 | | 4.8 |
| $R_{on}$ [Ω mm] | | 2.17 | | 10.5 |
| $C_{DS}$ [pF mm$^{-1}$] | 0.58 | 0.65 | | 0.297 |
| $I_{max}$ [A mm$^{-1}$] | | 0.80 | | 0.25 |
| $V_T$ [V] | | −2.4 | 0.9 | 2.1 |
| $m/\omega_c$ [pF Ω] | 1.3 | 1.4 | | 3.12 |

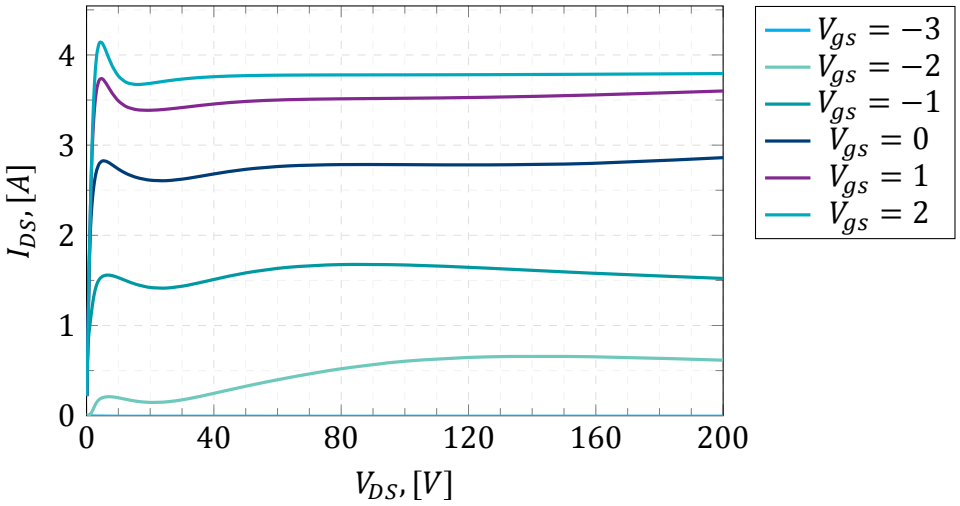



Figure 5.1: Fraunhofer GaN drain-source current as function of the drain-source voltage at various gate bias voltages.

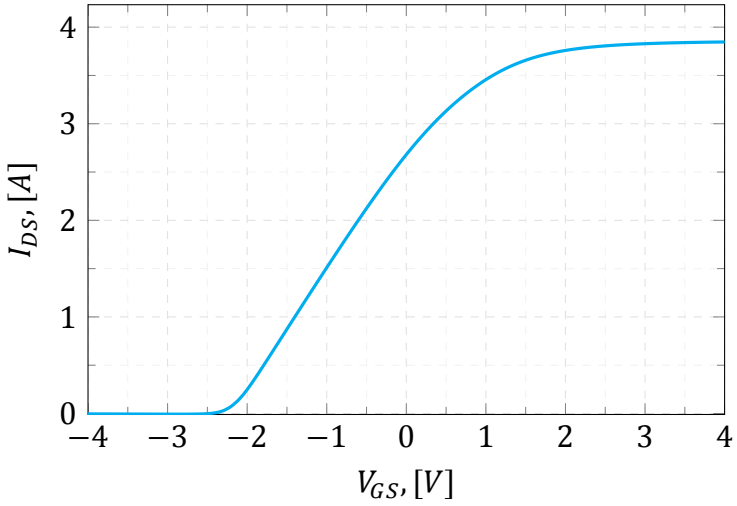



Figure 5.2: Fraunhofer GaN drain-source current as function of the gate-source voltage.

to a load resistance of

$$R_L = 2\frac{V_{DC} - V_k}{I_{max}} = 16\Omega. \tag{5.1}$$

Keep in mind that this is a starting point and is subject to change during the design phase. The two values in the table for the $V_T$ of the LDMOS are due to a $V_T$-shift lowering the threshold voltage from 2.1 V to 0.9 V

Now following the same procedure for the LDMOS device, the $I_{DS} - V_{DS}$ curve is plotted in Figure 5.3. From the plot it is evident that the knee voltage is higher than the GaN device and thus a lower load impedance is taken to start with.

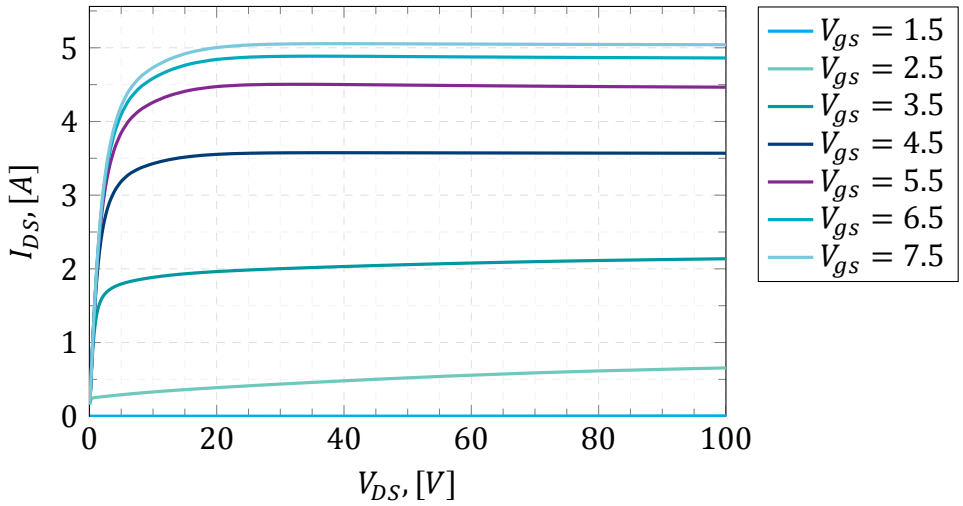



Figure 5.3: Ampleon LDMOS drain-source current as function of the drain-source voltage at various gate bias voltages.

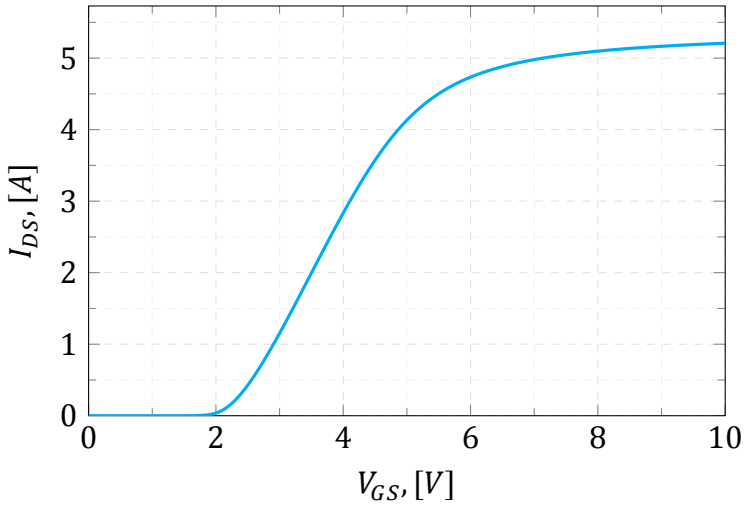



Figure 5.4: Ampleon LDMOS drain-source current as function of the gate-source voltage.

## 5.2. Digital class-B/Class-C

Chapter 2 explains that the class-B PA is a linear type of amplifier. Implementing this type of amplifier in the digital domain, changes the operation and brings some new challenges. The first change with respect to a conventional class-B amplifier

is the active device being square wave driven. This leads to the drain current turning into a square wave. Figure 5.5 shows the difference in drain voltage and current waveforms for a conventional and digital driven class-B. For a square wave of frequency $f_0$, the fundamental frequency component has an amplitude of $4/\pi$. For the best comparison with conventional class-B, the output power must be the same for both cases. The drain voltage still swings between zero and $2V_{DC}$, therefore the current must change. To make the fundamental drain current equal for both the conventional analogue and digital case the amplitude of the square wave needs to be scaled with $\pi/4$.

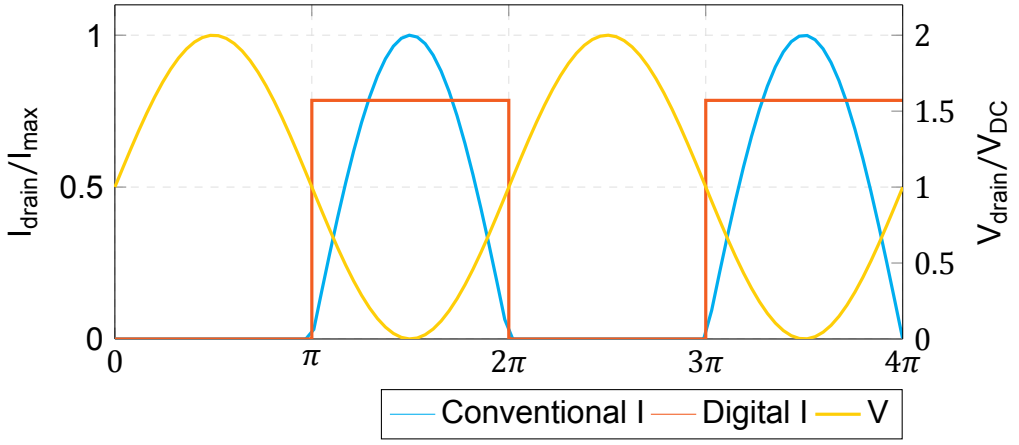



Figure 5.5: Conventional and digital class-B PA drain waveforms

In the digital case the drain current jumps to its peak value instantaneously which leads to a bigger overlap in current and voltage, as can be seen in Figure 5.5. This larger overlap results in a degradation of efficiency. The peak value of the square wave is now

$$I_{pk} = \frac{\pi}{4} \cdot I_{max}.$$

The voltage of the digital class-B case did not change. Since the fundamental component was kept the same as in the conventional class-B case, the fundamental output power remains equal as well. The DC current, however, becomes

$$I_{DC} = \frac{I_{pk}}{2} = \frac{\pi}{8} I_{max}. \tag{5.2}$$

Which leads to an efficiency of

$$\eta = \frac{\frac{V_{DC} I_{max}}{4}}{\frac{\pi}{8} V_{DC} I_{max}} = \frac{2}{\pi} \tag{5.3}$$

thus using a class-B output match for a switch mode amplifier leads to an efficiency of only 63.4% compared to the 78.5% of an analogue class-B amplifier. This clearly shows that some steps need to be taken in order to increase the efficiency.

## 5.3. Output Match

With the standard class-B output match, shown in Figure 5.6, the drain source capacitance is resonated out using a shunt inductor, the easiest way to implement this is using bondwires from the drain to the DC supply.

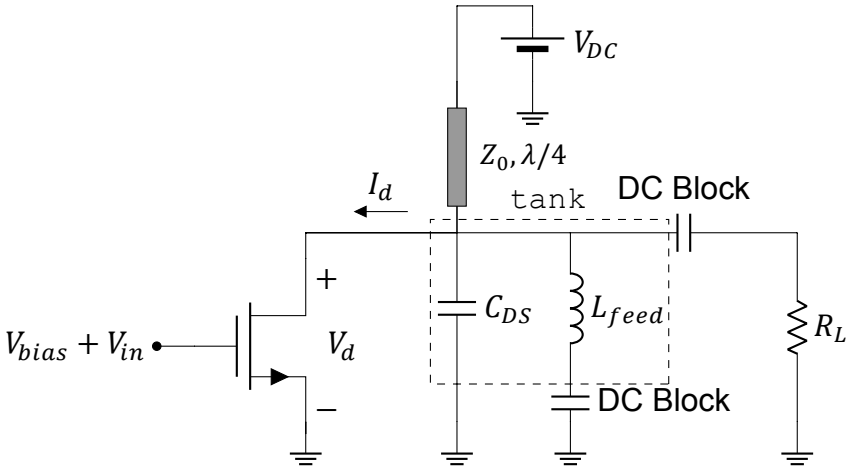



Figure 5.6: Class-B circuit diagram with resonant inductor $L_{feed}$.

Due to the hardware restrictions on the operating frequency, $f_c = 1\,\text{GHz}$, the resonance inductance is

$$L_{feed} = \frac{1}{(2\pi f_c)^2 \cdot C_{DS}}, \tag{5.4}$$

which for a single device with 3.84 pF output-capacitance operating at 1 GHz would lead to and inductance of $L_{feed} = 6.6\,\text{nH}$ and for two in parallel connected devices result in $L_{feed} = 3.3\,\text{nH}$. These values are too high to reliably implement using bondwires. Thus a substitute must be found.

The inductance needed to resonate out the capacitance can be approximated using a short circuited stub with a length less of than $\lambda/4$. This results in the circuit from Figure 5.7.

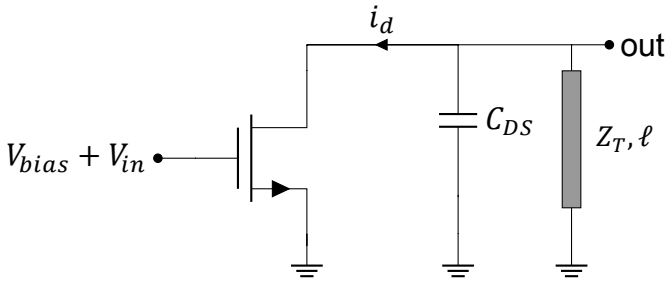



Figure 5.7: Inductance

The short circuited stub provides the correct inductance at the fundamental frequency, but does not terminate higher harmonics. To achieve this a second short circuited stub of length $\lambda/4$ is introduced in parallel to the other one. This

provides a short circuit to ground for all even harmonics. The resulting circuit is depicted in Figure 5.9.

The inductance needed to resonate out the capacitance is calculated using Equation 5.4. Resulting in a value of $L_{feed} = 3.3\,\text{nH}$ for the GaN device. With the use of the transmission line impedance equation from Equation 5.5 [49] both the length $\ell$ and the characteristic impedance $Z_T$ are calculated. Figure 5.8 provides a visual representation of a transmission line terminated with a load $Z_L$.

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan(\beta\ell)}{Z_0 + jZ_L \tan(\beta\ell)} \tag{5.5}$$

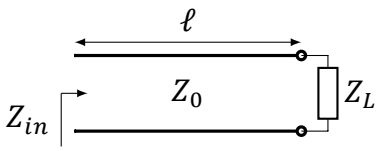



Figure 5.8: Visual representation of the input impedance of a transmission line terminated with a load $Z_L$.

The termination at RF is a short circuit, therefore $Z_L$ is 0. Simplifying Equation 5.5 to

$$Z_{in} = jZ_0 \tan(\beta\ell) \tag{5.6}$$

Equating the input impedance of the transmission line to the inductor impedance needed, leads to

$$Z_0 \tan(\beta\ell) = \omega L, \tag{5.7}$$

where $\beta = 2\pi/\lambda$ and indicating both the length $\ell$ and characteristic impedance $Z_0$ can be adjusted to get to the right value.

Starting by setting the characteristic impedance equal to the optimum load impedance of 16 Ω calculated earlier, leads to a line length of $0.191\lambda$.

The next step is to provide the correct real impedance to the drain of the active device. The external load is a 50 Ω resistance, while the optimum load impedance is around 16 Ω. For this conversion an impedance inverter is implemented using a $\lambda/4$ line which converts the impedance using

$$Z_{inv} = \sqrt{R_{opt} \cdot R_L}, \tag{5.8}$$

which leads to a characteristic impedance of the transmission line of 28.3 Ω. The implementation of the inverter is depicted in Figure 5.10.

To show the impedance offered to the drain as function of frequency, the circuit depicted in Figure 5.11 is used. Where the starting values based on the simple approximations are displayed in Table 5.2. After optimisation, the higher char-

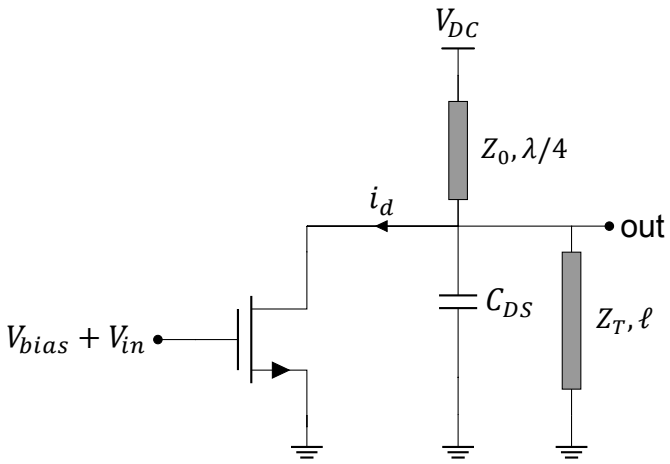



Figure 5.9: Parallel transmission line implementation

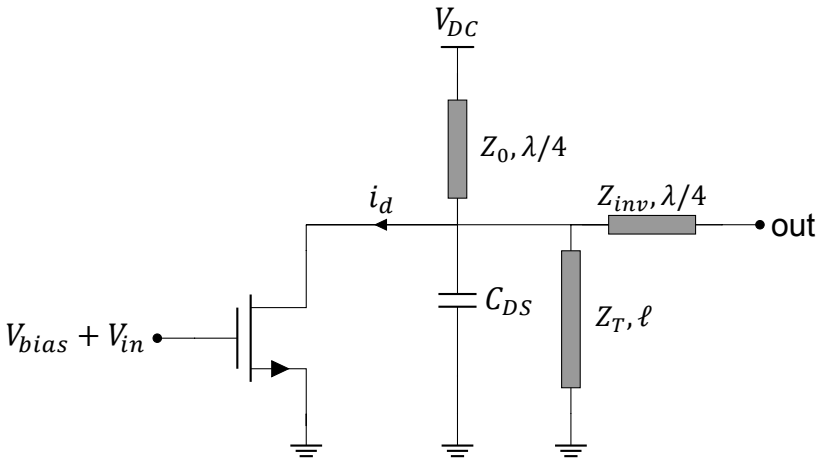



Figure 5.10: Parallel transmission line implementation

acteristic impedance of the transmission line results in a somewhat larger inductance, this is compensated for by the decrease in transmission line length. The increase in characteristic impedance also increases the bandwidth of the output matching network. The increased value for the impedance of the inverter line,

Table 5.2: Parallel stub circuit parameter values.

| Parameter | starting value | adjusted value |
|---|---|---|
| $Z_0$ | 16 Ω | 25 Ω |
| $Z_T$ | 16 Ω | 29.5 Ω |
| $\ell$ | $0.191\lambda$ | $0.139\lambda$ |
| $Z_{inv}$ | 28.3 Ω | 36 Ω |

## 5.4. Layout

Now that the output network architecture has been determined, the next step is to implement it on a printed circuit board (PCB).

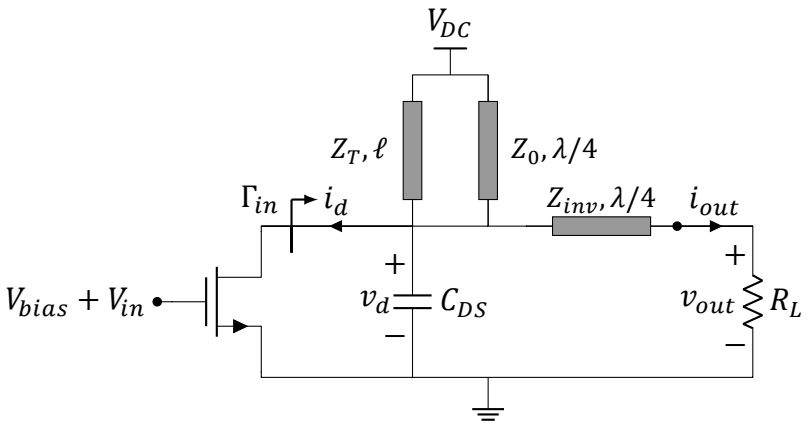



Figure 5.11: Parallel transmission line implementation

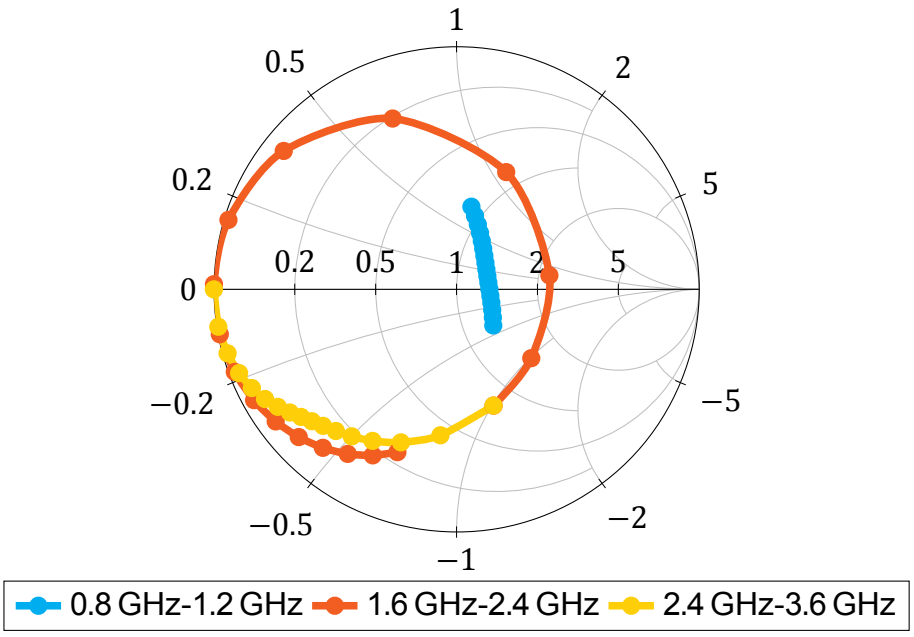


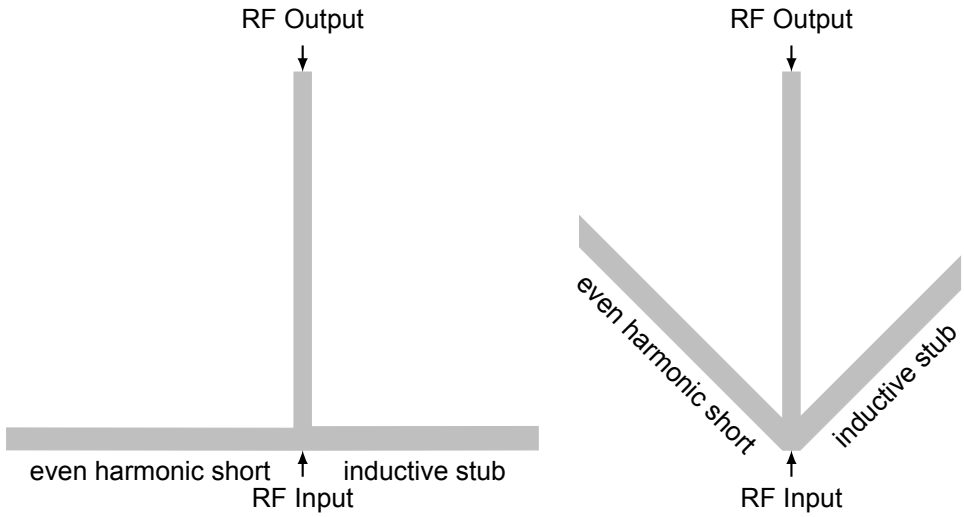

Figure 5.12: The input impedance $Z_{in}$ of the parallel stub network, as function of frequency.

In the conventional case, the stubs are placed perpendicular to the RF signal line as depicted in Figure 5.13a. However, due to the number and placement of the input traces, there are space limitations on the layout of the output match as shown in Figure 5.14. This restriction forced the stubs to be placed under a 45° angle. Fortunately, this angle does not diminish the performance of the output match.

### 5.4.1. GaN

With the general layout discussed, it is time to implement it with real devices and compare the results. The first implementation uses the Fraunhofer GaN25 device.

The output match for the GaN device shows promising results with respect to bandwidth. The 1 dB output power bandwidth achieves more than the required




(a) Conventional straight. (b) implemented bend.

Figure 5.13: Outputmatch layout.

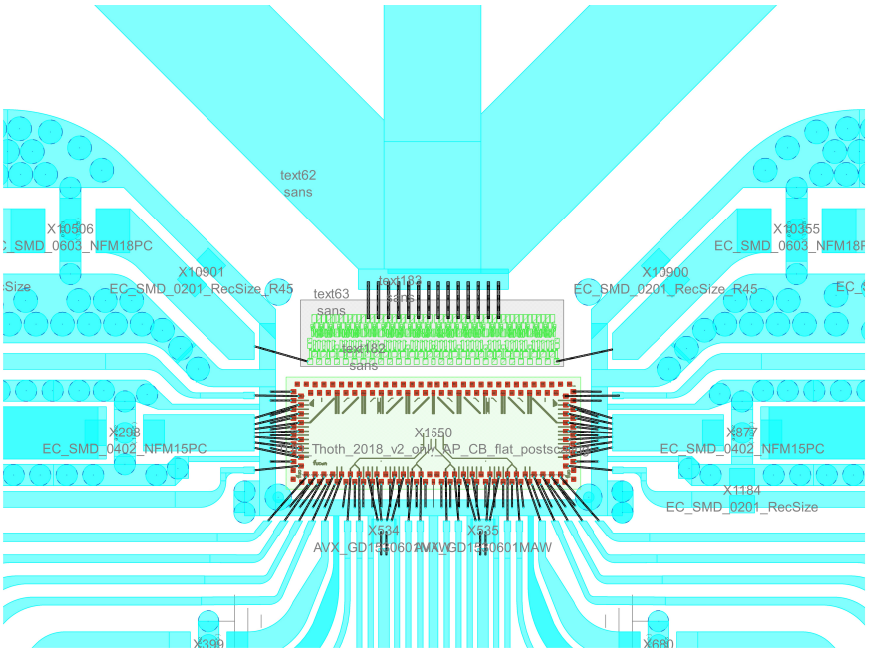
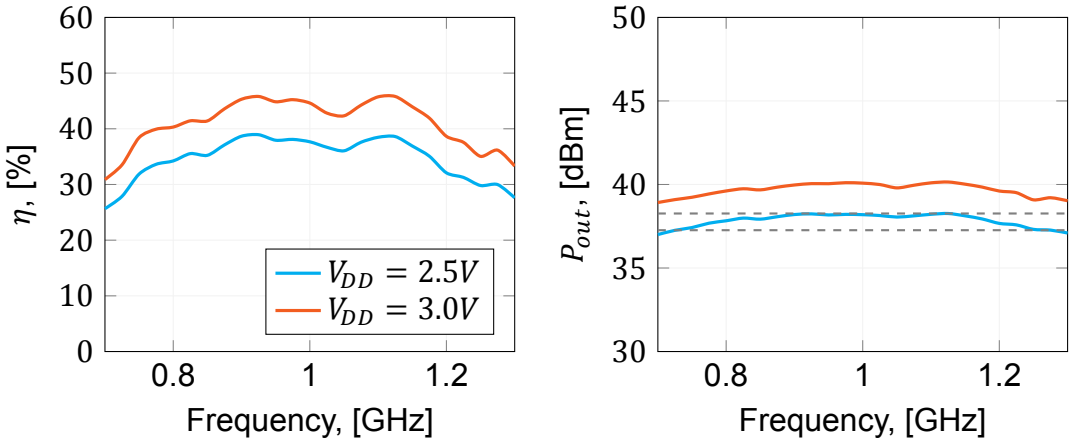



Figure 5.14: Limitations in space due to bias and input lines that exceed beyond the end of the chip, preventing the stubs from being placed perpendicular to the main RF signal line.

400 MHz.

Unfortunately, the device does not reach the desired peak drain efficiency. This is partly due to hardware limitations. The complementary metal–oxide–semiconductor (CMOS) driver is supplied with 2.5 V and between the driver and the GaN device, an all-pass filter is located at the input to ensure the integrity of the switched input signal. The all-pass filter creates a voltage divider, with a one to five ratio, at the input of the GaN device, resulting in a 0.5 V loss of the input drive voltage when $V_{DD}$ is set to 2.5 V. Comparing this 2 V swing at the input with Figure 5.2 shows




(a) drain efficiency (b) Output power

Figure 5.15: GaN output power and drain efficiency over frequency with an ideal transmission line output match.

that the device is not driven into saturation when the input is biased to allow for no quiescent current, thus maximum output power is not reached.

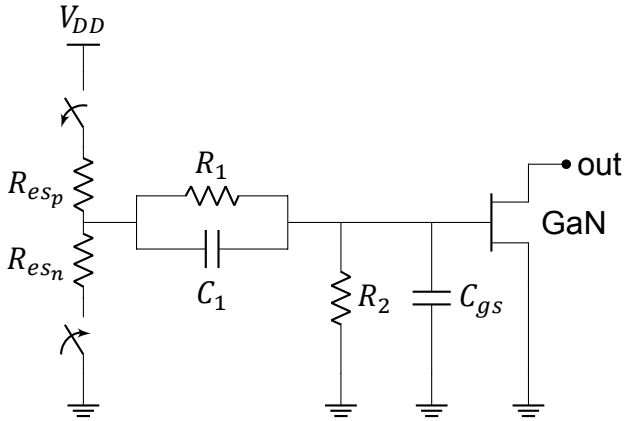
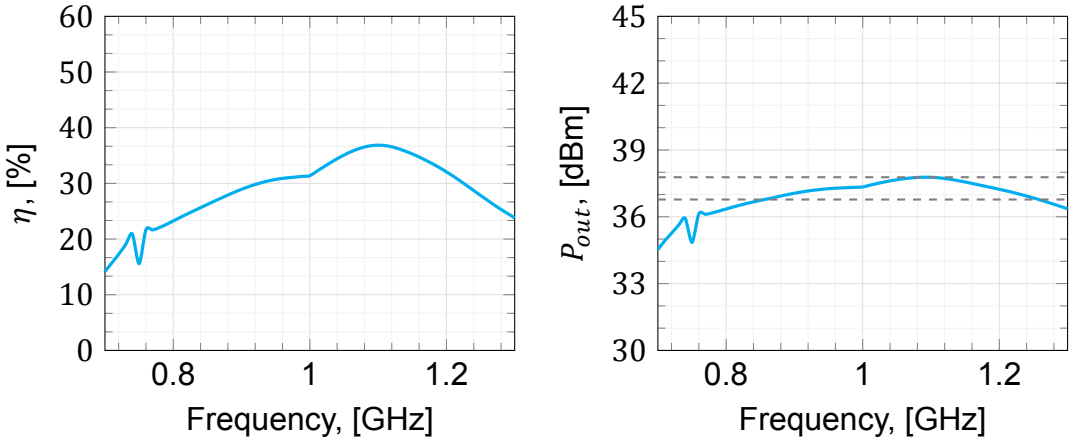



Figure 5.16: Input all-pass network of the GaN device.

The quiescent current should be low, to allow for higher efficiencies. Achieving this by biasing the input of the transistor below the threshold voltage means that the device is now operating in power back-off. Operation in this region leads to a lower efficiency. This can be counteracted by increasing the drain voltage swing. To do this, the load resistance must be increased.

The other option would be to increase the drive voltage by increasing $V_{DD}$ of the driver. This is a less reliable option, since the CMOS driver is subject to a breakdown voltage. The driver was designed with a $V_{DD}$ of 2.5 V in mind [48]. By increasing the $V_{DD}$ to 3 V, the efficiency and output power are increased by 7% and 1.8 dB, respectively. The increase is indicated by the orange line in Figure 5.15. Due to the unreliability, this will not be taken into account for the design, but might proof a beneficial tool during testing.

The last step before production is creating the layout of the output matching network on PCB. Using this layout a FEM simulation can be performed which takes into account the losses and effects in and around the PCB and provides the closest simulated result to the produced product. The result for the output power and efficiency using the FEM simulated output network is displayed in Figure 5.17. The plot shows that the lower frequencies experience the most degradation with the 1 dB output power point increasing from 750 MHz to 850 MHz, whereas the frequencies above 1 GHz remain mostly the same, with the peak output power decreasing with 0.05 dB. The efficiency has taken a bigger hit at the lower frequencies, with the largest deviation of 9 % inside the 1 dB bandwidth.




(a) drain efficiency (b) Output power

Figure 5.17: GaN output power and drain efficiency over frequency with the FEM simulated output matching network.

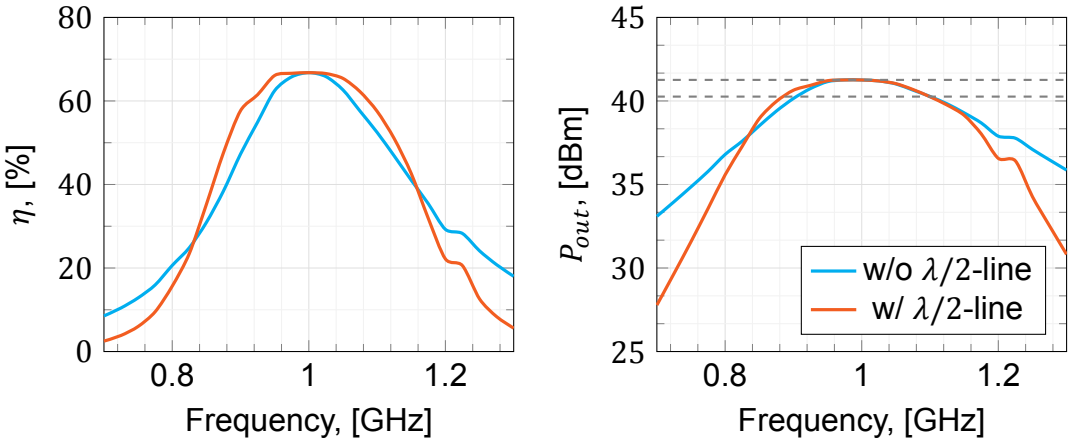
As the design to meet the bandwidth specification was cumbersome and time-consuming, it was decided that the results for now were acceptable. As increasing the operating frequency to around 1.05 GHz would still meet the bandwidth specification of 400 MHz. This allows for good comparison between polar, cartesian and MP, which is one of the goals of this thesis work.

### 5.4.2. LDMOS

The second implementation uses the Ampleon LDMOS LM8.

First a frequency sweep is performed to inspect the output power and efficiency as function over a wide range of frequencies. The results are plotted in Figure 5.18. The plots show that the efficiency of 66.7 % is an improvement over the GaN implementation, however, the bandwidth is much lower at 200 MHz.

A way to increase the bandwidth of the amplifier is by introducing a $\lambda/2$ transmission line open stub at the output of the circuit as depicted in Figure 5.19. This stub is an open at the fundamental frequency. However, at lower frequencies it provides an inductive impedance, whereas at higher frequencies a capacitive impedance is provided. In other words the $\lambda/2$ line mimics a parallel LC-tank.




(a) drain efficiency (b) Output power

Figure 5.18: LDMOS output power and drain efficiency over frequency.

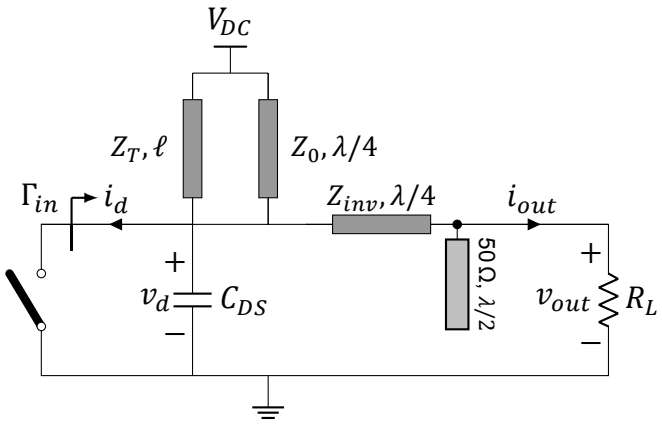



Figure 5.19: Circuit diagram with $\lambda/2$ transmission line stub.

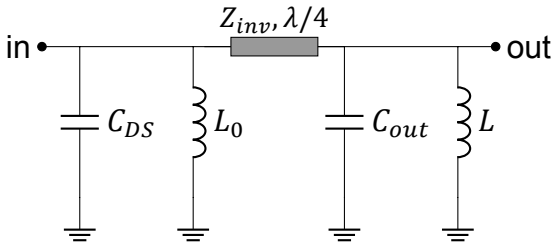



Figure 5.20: Equivalent circuit diagram for $\lambda/2$ transmission line stub as parallel resonator.

However, the LC-tank is preceded by a $\lambda/4$ transmission line. The line inverts the impedance of the parallel LC-tank, so that it can be approximated by a series LC-resonator as shown in Figure 5.21. The effect of the series resonator is the inverse reactance profile it has compared to the parallel LC-tank at the output of the LDMOS. This compensation increases the bandwidth of operation.

This is best illustrated using the impedances displayed in Figure 5.22. The blue line indicates the conventional case and the orange line the inclusion of the $\lambda/2$ stub. The smithchart shows that the $\lambda/2$ stub leads to the impedance close to

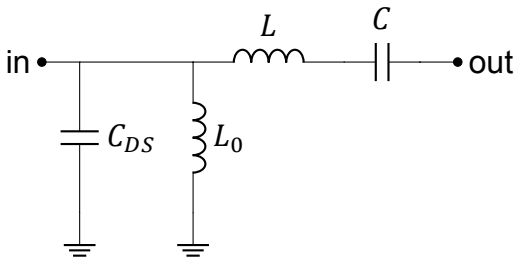



Figure 5.21: Equivalent circuit diagram for $\lambda/2$ transmission line stub as series resonator.

the fundamental frequency, closely following the constant resistance circle. The effect of this change in impedance is demonstrated in Figure 5.18 by the orange line. The power plot shows that there just a minor improvement of around 20 MHz, however, Figure 5.18a shows an efficiency increase within the 1 dB bandwidth. Where the maximum increase is a little over 10 %, leading to the conclusion that the inclusion of the $\lambda/2$ stub is beneficial.

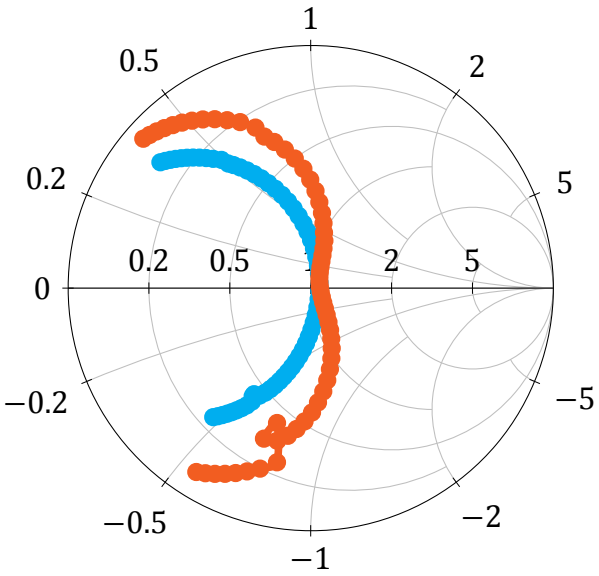
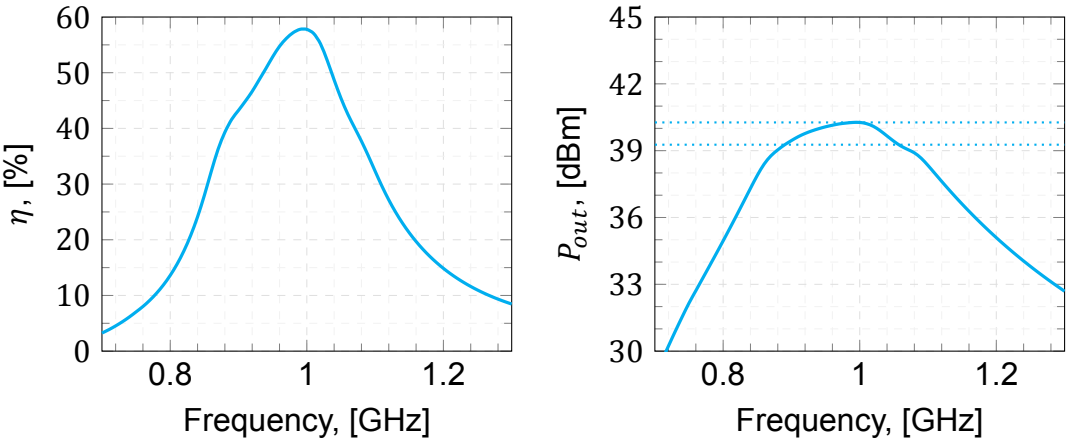



Figure 5.22: Impedance offered to the drain of the LDMOS device with and without the $\lambda/2$-line.

Since the $\lambda/2$ stub provides just marginally better performance, the choice is made to implement the line on the PCB, but disconnect it with a gap of 100 µm. This way it provides the option to do both measurements with and without the line, because it can simply be attached by means of a little solder.

Now that the design for the output matching network is chosen, it must be converted to a PCB layout. The results of the FEM simulations are depicted in Figure 5.23. The orange line shows the implementation with the $\lambda/2$ stub and unfortunately, the 1 dB bandwidth has been even further reduced to 120 MHz with a centre frequency of 970 MHz. The biggest impact, however, is on the efficiency, where it has dropped to a lowest value of 41.1 % within the 1 dB. Different from the afore mentioned ideal simulation results, the PCB implementation without the

$\lambda/2$ stub seems to lead to the best results, with a bandwidth nearly 200 MHz and a slightly higher efficiency of 57.8 %. The best explanation for this is that the losses of the $\lambda/2$ stub are two high counteracting the gain in bandwidth.




(a) drain efficiency

(b) Output power

Figure 5.23: LDMOS output power and drain efficiency over frequency with the FEM simulated output matching network.

## 5.5. Conclusion

Since the MP uses the same TX architecture as cartesian, two drain connected RF-DACs are used. An output match similar to that of a class-B PA is used to meet the bandwidth specification. However, since the active devices act as switches, the drain waveforms differ from that of a conventional class-B PA, which results in a somewhat lower drain efficiency. Implementing the class-B output match using a parallel transmission line implementation leads to the best result. Due to some hardware restrictions the drain efficiency is even further limited, but this does not pose a problem as the same system can be used for the comparison between cartesian and MP, still demonstrating the achieved improvement. Simulating the on PCB implemented output match leads to the results summarised in Table 5.3.

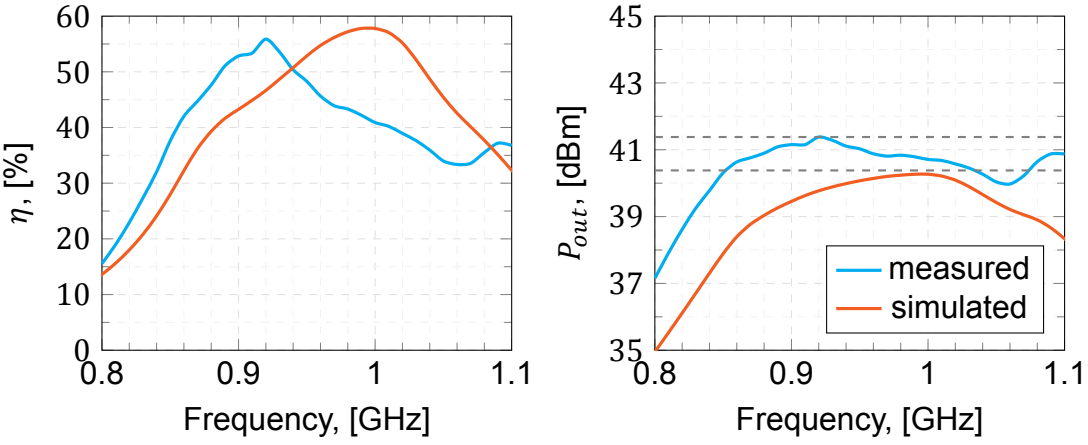
Table 5.3: Results and specifications of the digital driven class-B.

| specification | desired value | achieved value (GaN) | achieved value (LDMOS) |
|---|---|---|---|
| Peak drain efficiency | 70% | 30-40% | 57.7% |
| Peak output power | 40 dBm | 37.7 dBm | 40 dBm |
| 1 dB bandwidth | 400 MHz | 400 MHz | 200 MHz |

# 6

# Results

Now that the design has been completed, the hardware can be assembled for testing. The first step is to show that the hardware works correctly. This is done by performing a single tone frequency sweep. This provides the best comparison with the design simulations. The results of the measurements are depicted in Figure 6.1. The big difference that is immediately clear from the results is the shift in centre frequency, which has shifted from 1 GHz to 930 MHz. This is most likely due to the harmonics short not providing a perfect short at 1 GHz, which in the simulations showed the best performance at that frequency. However, in the simulations the short is provided at a frequency of 950 MHz.




(a) drain efficiency

(b) Output power

Figure 6.1: Measured LDMOS output power and drain efficiency over frequency.

In the coming months also the MP results for modulated signals will be collected. They will be added to the report when they become available.

Figure 6.2 clearly shows the linear region until the output reaches the triode region. The plot indicates the linear operation of the PA.

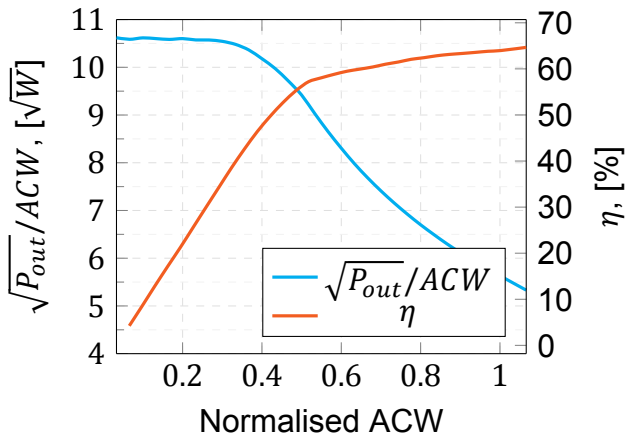



Figure 6.2: Measured LDMOS output power and drain efficiency over normalised ACW.

# 7

# Conclusion

Due to the introduction of 5G, there is a demand for higher data-rates has lead to a demand for an increase in modulation complexity and bandwidth. The former results in a larger PAPR for transmitted signals. Which in turn leads to a need for a higher efficiency in power back-off. The demand for high efficient TXs is even further increased by the huge power consumption of the telecommunication industry.

To support the increase in bandwidth, the transconductance amplifier is a logical choice, because of its high linearity. However, a disadvantage is that the maximum theoretical is considerably low. Whereas a switch-mode PA lacks the linearity and even amplitude modulation, but has an extremely high efficiency. More recently also duty-cycle reduced digital operation also referred to as digital class-C like operation proves to be an interesting option [50]. Both seem to be suitable options to implement in an RF-DAC.

The current architectures have certain drawbacks. Where polar lacks the wide bandwidth needed for higher data-rate demand, the cartesian architecture suffers from complex loading which causes the efficiency to drop. The orthogonality of the two polar signals means that the signal paths differ. This difference creates a different time delay in both paths, as well, leading to cumbersome alignment of the signal paths.

To combat these drawbacks a new architecture, the Multi-Phase cartesian architecture was introduced. Due to the linear nature of the cartesian to MP conversion, the bandwidth remains basically equal to that of the baseband bandwidth. By introducing more phases the complex loading that troubles cartesian is decreased. Because both signals in MP are amplitude modulated, the paths can be equal, thus allowing easy and straightforward re-timing.

The new architecture is implemented using two output connected RF-DACs. For the output matching network a class-B type is chosen to enable high bandwidths. However, due to the non optimised hardware of the DACs in combination

with the class-B output match, the efficiency is somewhat reduced.

The theoretical results show that the new architecture is extremely promising for high bandwidth operation and very useful for achieving higher average efficiencies in combination with well known efficiency enhancement techniques, like load modulation or supply modulation.

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# Acronyms

**4G** fourth generation. 1

**5G** fifth generation. 1, 2, 77

**ACPR** adjacent channel power ratio. 9, 10

**AM-AM** amplitude-modulation to amplitude-modulation. 10

**AM-PM** amplitude-modulation to phase-modulation. 10

**CMOS** complementary metal–oxide–semiconductor. 69, 70, 87

**DAC** digital to analog converter. 2, 77

**DC** direct current. 5, 6, 13–15, 17, 18, 20, 23, 24, 34, 35, 39, 40, 64, 65, 85, 87

**DRAC** digital to RF amplitude converter. 47, 48

**EER** envelope elimination and restoration. 30

**ET** envelope tracking. 30

**EVM** error vector magnitude. 7, 9

**FET** Field Effect Transistor. 12

**GaN** gallium nitride. VI, IX, 61–63, 66, 68–71, 74

**LDMOS** laterally-diffused metal-oxide semiconductor. VI, IX, 61, 63, 71–76

**LINC** linear amplification with non-linear components. 32

**MP** Multi-Phase. 53–58, 71, 74, 75, 77

**PA** power amplifier. V, VII, VIII, XI, 2, 5, 6, 8, 10–12, 14–20, 22–24, 26–30, 33, 35, 36, 44, 47, 48, 56, 57, 63, 64, 74, 75, 77, 85

**PAE** power added efficiency. 6

**PAPR** peak to average power ratio. 40, 44, 54, 77

**PCB** printed circuit board. 67, 71, 73, 74

**QAM** quadrature amplitude-modulation. 29, 54

**RF** radio frequency. 2, 5, 6, 20, 23, 25, 27, 41, 45, 47, 48, 66, 68, 69, 83, 85

**RF-DAC** radio frequency digital to analog converter. 50, 61, 74, 77

**RMS** Root Mean Square. 6, 7, 9

**TX** transmitter. 1, 2, 29, 46, 47, 50, 54, 61, 74, 77

# Glossary

**baseband** Frequency range of a modulated signal around DC. 47

**drain efficiency** Efficiency of an active device defined as the ratio between the DC supply power of the PA and the desired RF output power. 6, 74, 87

**loadline** Graphical representation of the current vs voltage at the drain of the device, indicating any restraints put on the device by the external circuit. 15

**Root Mean Square** The square root of the mean of the squared value, often used to describe the absolute average value of a time signal ($\sqrt{\langle \cdot^2 \rangle}$). 6, 7, 9

**transmitter** An electronic device which produces radio waves. 1, 2, 29, 46, 47, 50, 54, 74, 77

**zero saturation voltage condition** Limiting the maximum voltage swing at the drain to the supply voltage. 13

# Symbols

$\eta$ drain efficiency. 22

$i_d$ Time domain drain current. 12

$I_d$ Fundamental drain current amplitude. 12–14

$I_{max}$ Maximum achievable drain current. 13–15, 17, 18, 20, 27

$I_{out}$ Fundamental output current amplitude. 6, 23, 24

$I_{DC}$ DC supply current. 14

$I_q$ quiescent current, the current present at the drain of the transistor when no signal is provided to the input. 12, 13

$P_{out}$ DC supply power. 5

$\varphi$ conduction angle. 13–16

$\phi$ outphasing angle. 32

$\varphi_1$ overdrive angle. 17–20

$P_{in}$ Fundamental input power. 5, 6

$P_{out}$ Fundamental output power. 5, 6, 14, 18, 20, 23, 24, 28

$V_{DC}$ DC supply voltage. 13, 14, 17, 18, 20, 23, 24, 27, 28, *see* DC

$V_{DD}$ CMOS supply voltage. 69, 70, *see* DC

$V_d$ Fundamental drain voltage amplitude. 12–14

$V_{in}$ Input voltage amplitude. 6, 12, 23

$V_{out}$ Output voltage amplitude. 6, 23, 24

$Z_0$ Characteristic impedance. 66, 67