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Large Matrix Array Aperture for 3D Vascular Imaging Capture

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Large Matrix Array Aperture for 3D Vascular Imaging Capture

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Abstract

Three-dimensional ultrasound has initially been used to address volumetric imaging for diagnostic purposes and represents the leading-edge technological orientation in both transducer and IC (integrated circuit) architecture and design. However, new applications are coming up like biomarker measurements, preoperative navigation, real time surgery guidance or therapeutic procedures where 3D ultrasound modalities are key but their design objectives may need to be thought outside 3D echocardiography and radiology technological trade-offs. For those new applications, system architectures would need less complexity and imaging performances enabling easier hardware reconfigurability tailored to application-oriented imaging. This paper presents an ongoing development where a large matrix transducer has been assembled with multiple ASIC dies in a reconfigurable way. The transducer has a central frequency of 8MHz, a square pitch of 150µm × 150µm capable to fully image the upper carotid window thanks to a large aperture of 80x240 elements, resulting in a transducer active footprint of 12x36 square millimeters.

Keywords— *Matrix array, transducer, reconfigurable, 3D, ASIC integration*

I. INTRODUCTION

Matrix arrays are well known components in ultrasound imaging modalities since early 2000s. Matrix initial development were mostly driven by major players in ultrasound imaging which brought together key technological ingredients, as the matrix transducer, the microbeamforming IC technology and integration methods [1]. They have pushed these technologies up bringing unsurpassed imaging performances and frame rates to 3D imaging modalities in echocardiology and radiology. To reach that point, transducer and system manufacturers have managed difficult design trade-offs, leading to application-specific transducer and IC designs.

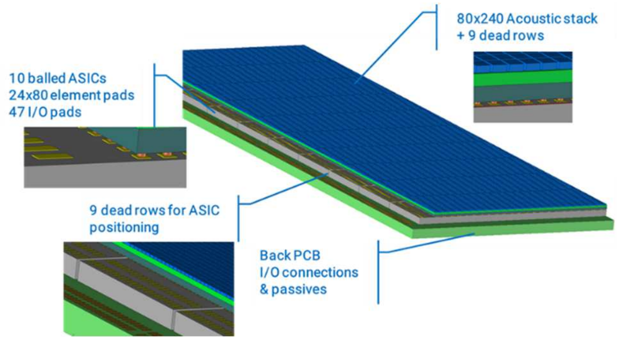

Figure 1 : Artist's impression of the overall transducer assembly.

This work targets the opposite direction by orienting the design to something flexible and versatile, capable to handle new application fields where the requirements are different and where ASIC integration is flexible enough to overcome the limitation of having to redesign the entire IC per application.

In context of the Dutch research program Ultra-X-treme [2], we target the design and the fabrication of a large (80x240 individual elements) and dense (150µm × 150µm pitch) high-frequency matrix transducer interconnected to multiple (10) ASIC chips [3] in a reconfigurable manner and along a semiconductor-like integration scheme.

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II. CHALLENGES

A. ASIC attachment process

The ASIC used in this work is based on the design reported in [3], which embeds multiple analog and digital functionalities with regard to the targeted ultrasound application. It allows to miniaturize the system and control its power consumption by controlling the functionality of the chip. In this case, the ASIC embeds individual channel functions with a rectangular pitch of 300 µm × 150 µm. To connect to the transducer array, the ASIC features a bond-pad array with a pitch of 150 µm × 150 µm, in which pairs of neighboring pads are shorted. As a result, and for the rest of the article, we will consider a square pitch of 150 µm × 150 µm with regard to the transducer-ASIC integration challenge, which is the main purpose of this paper.

As stated above, the ambition of this work is to define an integration path as close as possible from the semiconductor back-end standards. To interconnect the fully populated transducer to an ASIC, we have selected a reflow soldering process using solder balls rather than copper pillars for cost and process simplicity reasons. Thus, using both 8-inch dummy wafers with top-metal only, and functional 8-inch wafers, we start with the balling process. By subcontracting this operation, we first have:

- deposited the Under Ball Metallization. Our UBM is a 5µm thick NiAu layer,
- each wafer has been populated with 518 400 SAC305 solder balls of 70µm in diameter (60 µm height after reflow-soldering) through a Wafer Level Solder Sphere Placement process,
- each populated pad has a square shape of 53µm

Figure 2 shows the ball positioning and ball population arrangement.

Each silicon die measures 3.55 mm × 14 mm. For miniaturization optimization the chip is unpackaged (bare). It embeds front end ultrasound and digital functionalities for 80 × 12 individual elements where each element is connected with two pads resulting in an interconnexion scheme of 80 × 24 individual pads to be interconnected with a 150µm square pitch lattice. The photography presented in Figure 2 shows the die floorplan where we can see the 80x24 element pads lattice to align and interconnect with the transducer elements lattice and the 47 I/O pads that manage the power lines, the signal path, the synchronization clock and the digital commands.

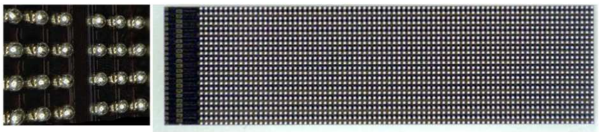

Figure 2 : Silicon die populated with solder balls and ASIC die floorplan with 80x24 element pads and 47 I/O pads.

SAC305 are standard solder-balls which exhibit a typical reflow profile (shown in Figure 3) above 240°C in less than 4-minutes temperature ramp-up. Such a temperature profile is a challenge with regards to piezoceramic-based transducer technologies. General piezo-based transducers are indeed layered with multiple organic materials that cannot sustain such a high temperature.

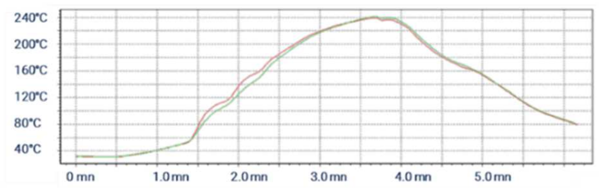

Figure 3 : Temperature profile for the reflow soldering process for silicon die attachment to the transducer.

The originality of this work lies in the total redefinition of the transducer architecture to manage the vertical assembly of bare dies by high temperature reflow soldering process with acceptable trade-offs on the transducer acoustical performances.

B. Transducer design and manufacturing flow

With regards to the transducer, multiple challenges have to be considered:

- The acoustic component size of 36x12 mm^2,
- The fine pitch of 150µm,
- The vertical integration scheme which involves having a silicon material underneath the acoustic component instead of a damping backing material,
- The reflow-soldering temperature process,
- Performances compliant with superficial imaging.

To address the above challenges, we moved from a regular transducer design to a "stacked composite" approach as illustrated in Figure 4 where the selected materials, including the organic ones, can sustain the temperature profile and where the diced-through composite allows thermal stress expression during the processes without warping the structure. We also have used a heavy rear material principle of operation [4] to limit the acoustic impact of the back silicon layer on the transducer performances and more particularly the ring down performance that would impact the axial resolution which is critical at this frequency (around 8MHz) for the target application of superficial imaging.

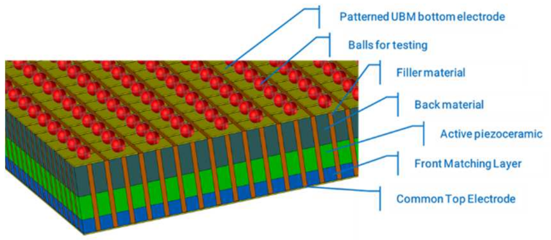

Figure 4 : Technical scheme of the transducer architecture.

To avoid periodic stationary waves due to the element pattern, we also have chosen a composite lattice of 75µm lateral pitch aligned with the metallization patterning. As a result, each element is composed of four individual pillars. Composite and element kerfs are about 20µm and the filler material is a high temperature epoxy material.

The vertical stack is simplified on purpose, the basic idea herein is to assemble acoustic compatible materials that are all compatible with temperature processes above 250°C (Curie Temperature and glass transition temperature) with a common thermal expansion coefficient (CTE) around 7ppm/°C. The filler kerf, since it is a polymer, exhibits a larger CTE parameter (about 20ppm/°C) but since the whole structure has been fully diced and filled with this epoxy material, we do not expect any warpage expression, but this remains to be experimentally confirmed.

For testing purposes, we optionally add some solder balls for further assembly on a test flex where it is possible to measure the intrinsic performances of such an acoustic stack with the limitation that there is no silicon die underneath and that it will be a partial verification.

C. *Transducer back-end Facilities*

ASIC bare dies have been singulated, flip-chipped on the transducer back side and then soldered in our dedicated pilot line in an ISO7 clean room environment shown in Figure 5.

Figure 5 : Vermon's ISO7 clean room dedicated to ASIC integration

III. RESULTS

A. *Transducer Assembly*

The transducer has been assembled and micromachined along the architecture schematic presented in Figure 4.

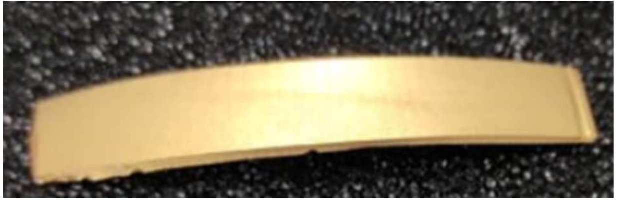

Figure 6 : Photography of the top of the 240x80 acoustic component.

From Figure 6 to Figure 8, different pictures of the assembled transducer are shown, where a slight warpage and a misalignment of the element pattern with the microstructure can be noticed.

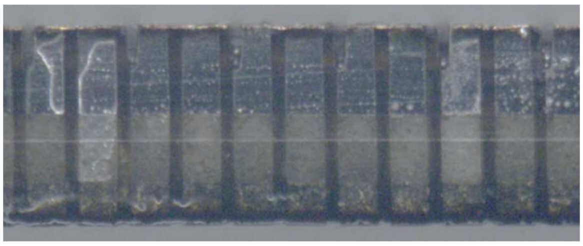

Figure 7 : Magnified photography of the cross section of the "stacked composite" acoustic component. The overall thickness is 280µm

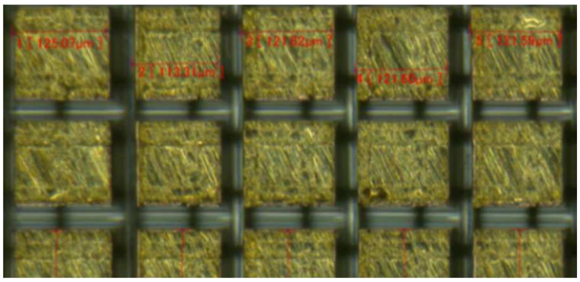

Figure 8 : Bottom pads (UBM) after element singulation. Singulation width is 25µm and element square pitch is 150µm.

For further tests, this transducer has been assembled on a test flexible printed circuit (FPCB) using a reflow soldering process where this time the solder balls are attached on the bottom face of the acoustic component and then interconnected to the FPCB, as shown in Figure 9.

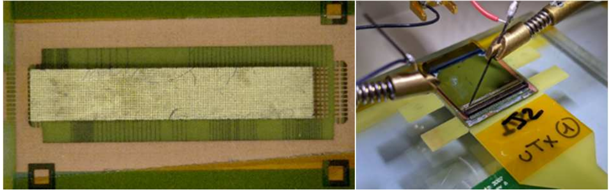

Figure 9 : Top view and experimental measurement of the acoustic component flip-chipped and interconnected on the FPCB.

To assess transducer performances, electrical, electroacoustical and acoustical measurements have been performed.

1) *Electrical impedance measurement*

Electrical impedance is a key property for matrix arrays since it gives information about the electrical adequacy between the transducer element and the transmit and receive analog front-end.

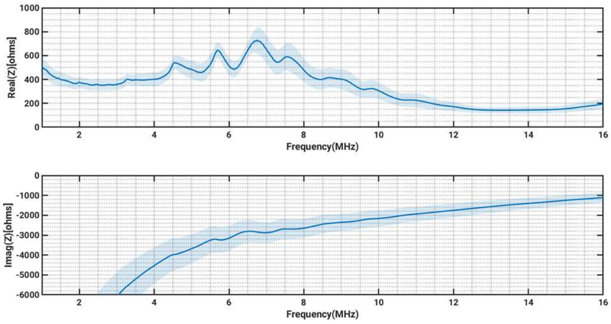

Figure 10 : Average and distribution of complex electrical impedance measured on 41 different elements. The transducer head is encapsulated in a silicone lens and the measurement is performed in air.

To assess this, we have measured the electrical impedance of 41 individual elements located over a smaller transducer aperture of 12x64 elements connected to the test flex by reflow soldering as illustrated in Figure 9. The measurements were performed using a probe tip positioned on the test FPCB termination pads using an Agilent Impedance Analyzer 4294A and a 42941A probe. The transducer has been encapsulated in its rubber silicone lens and the measurement is managed in air.

In Figure 10, averages and distribution of real and imaginary parts electrical impedance of 41 unitary elements are presented over the frequency. At 8MHz, one can measure an averaged value of about 440 – j2800 ohms for a static capacitance of 9 picofarad.

2) *Electroacoustic measurements*

Pulse-echo is a standard measurement for transducer characterization. It consists in the measurement of the transmit and receive response after the specular reflection on a flat target. We have used a Panametric pulser 5072PR generating a negative spike about 100V peak, connected to the transducer through a coaxial AWG42 cable bundle of 2.2m long with the following electrical properties: 60pF/m and 75 ohms of characteristic impedance. The flat steel target is located at 5mm from the transducer surface and the back propagated signal is measured through a Tektronix TDS3014B scope with a 16-averaging factor.

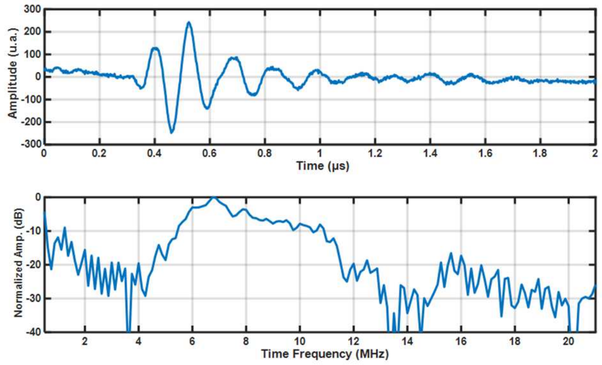

Figure 11: Pulse echo response of an individual matrix element.

Figure 11 shows the time and frequency response of a representative element pulse echo measurement. The response has to be considered by taking into account the impact of the coaxial cable and the experimental difficulties of measuring such a small acoustic aperture (130 µm square source). However, the measurement exhibits a central frequency around 8MHz and a ring-down that will need further transducer stack optimization.

3) *Acoustical measurement*

Acoustic measurement is another experimental tool to assess the transducer performances. Such measurements are performed by accurately positioning at different positions in front of the element aperture a 40µm diameter needle hydrophone (Precision Acoustics), when one unitary element is excited with the same negative spike (5072 PR Panametrics) and measured through the oscilloscope (Tektronix TDS3014B)

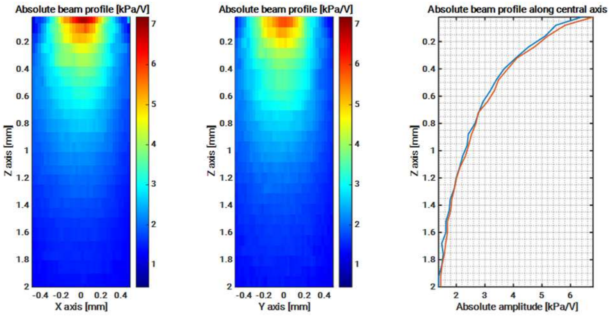

Figure 12 : Acoustic pressure measurements along the XZ and YZ planes and along the acoustical axis.

Transducer is lensed and its front face is immersed in water. In Figure 12 we can appreciate beam divergence in agreement with the source geometry and we can approximate the transducer element surface pressure as about 7kPa/Vp at the lens surface.

B. *Reconfigurable integration*

To assess the pitch-matched ASIC integration, we have used dummy silicon dies perfectly mimicking the interconnection interfaces and constraints, but without any electronic functionalities, and a dummy acoustic component where we have only used the rear material and its UBM surface finishing and patterning. The pitch-match vertical integration is managed through a flip-chip and pick & place initial processing using a DATACON EVO 2200, then the reflow soldering process is achieved by a PINK oven along the temperature profile presented in Figure 3. A polymer underfill is manually deposited using a needle.

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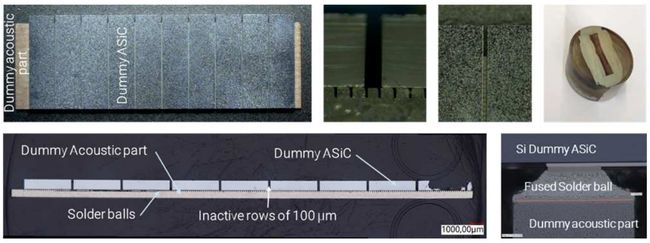

Figure 13 : Optical photography and SEM of 10 dummy ASICs assembled on a dummy acoustic component.

In Figure 13 the top photography presents the top and side views of the ASIC assemblies after the reflow soldering step, where a dead column of 0.1mm width has been successfully managed on the transducer backside patterning and on the accurate positioning of the 10 dummy ASICs. The bottom SEM shows the cross section of the whole assembly and an example of the fused solder ball. As a result, the demonstrated process, even if realized with dummy components is a first qualification stage of the multiple pitch-matched ASIC assembly.

IV. CONCLUSION

As a conclusion, a new transducer architecture allowing high-temperature ASIC pitch-matched integration has been defined and characterized. The whole assembly has been managed with dummy parts to successfully assess the capabilities of a reconfigurable ASIC integration over a large and dense transducer array. This demonstration has been managed within new dedicated matrix transducer assembly facility in a controlled environment. Next steps consist in doing the same process but with functional parts, finalizing the I/O pads wire bonding interconnection and final EMC and in addressing thermal encapsulation of the complete probes.

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