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Chaudhary, Aditya; Hoß, Jan; Lossen, Jan; Huster, Frank ; Kopecek, Radovan ; van Swaaij, René; Zeman, Miro

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Influence of Silicon Substrate Surface Finish on the Screen-Printed Silver Metallization of Polysilicon-Based Passivating Contacts

Aditya Chaudhary, Jan Hoß, Jan Lossen, Frank Huster, Radovan Kopecek, René van Swaaij, and Miro Zeman*

Passivated contact based on a thin interfacial oxide and a highly doped polysilicon layer has emerged as the next evolutionary step to increase the efficiencies of industrial silicon solar cells. To take maximum advantage from this layer stack, it is vital to limit the losses at the metal polysilicon interface, which can be quantified as metal polysilicon recombination current density (J_{0met}) and contact resistivity. In cell concepts, wherein a large variety of silicon substrate surface finish can be obtained, it is essential to know how the surface finish affects the J_{0met} and contact resistivity. Herein, commercially available fire through silver paste and the metal-polysilicon recombination current densities and contact resistivity are used for three different silicon substrate surface finishes, namely: planar or saw damage etched (SDE), chemically polished in acidic solution and alkaline pyramidal textured. Contact resistivity values below 3 mΩ cm^2 with J_{0met} in order of the recombination current density of the doped region (J_{0pass}) are obtained for samples with planar surface for both 150 and 200 nm n$^+$ polysilicon layer thicknesses. The results presented in this work show that the samples with flat substrate morphology outperform the samples with textured surfaces.

1. Introduction

Passivated contacts based on a stack of a thin interfacial oxide and doped polysilicon layer have demonstrated to be viable for application in silicon solar cells. A recently published cell efficiency of 24.58% on an industrial-sized solar cell by Trina Solar demonstrates the application of these passivated contacts.[1] This approach is based on the use of an ultrathin interfacial oxide layer (1–2 nm) grown on top of the crystalline silicon (c-Si) absorber and a highly doped polysilicon layer, which is deposited on top of the thin interfacial oxide. The thin interfacial oxide provides chemical passivation for the c-Si absorber surface in addition to acting as a diffusion barrier for the majority carriers from the polysilicon layer. The highly doped polysilicon layer, provides field-effect passivation and carrier selectivity.[2,3] In this way, losses from recombination are suppressed, and excellent recombination current density values below 5 and below 10 fA cm^{-2} can be achieved, with implied open-circuit voltage (iV_{oc}) values greater than 730 and 720 mV for the n- and *p*-type polysilicon, respectively.[4–9]

Excellent results have been obtained when thick polysilicon layers (≈200 nm) are utilized in the passivating stacks, with values of 1–2 mΩ cm^2 for the contact resistivity and 250–20 fA cm^{-2} for metal–polysilicon recombination current density.[8–13] However, excellent passivation and contact properties with thick polysilicon layers come at the expense of absorption losses incurring in the polysilicon layer. Passivation and contact properties for polysilicon/SiO_x layer stacks with textured silicon substrates were presented by Ciftpinar et al.[10] In that work, low-pressure chemical vapor deposition (LPCVD)-based polysilicon layers doped with $POCl_3$ diffusion (ex situ doping) were used with a thin thermal oxide. Two methods were used to compute the contact recombination in the work from Ciftpinar et al., one using modeling of photoluminescence (PL) maps and other by V_{oc} measurements for different metal coverages. Metal–polysilicon recombination current density of about 400 fA cm^{-2} for the sample with 200 nm-thick polysilicon is presented in that study; however, the influence of different substrate surface finishes was not analyzed. A study presented by Firat et al. shows recombination current density in the screen-printed-metallized region on the saw-damage-removed surface of 25.6 fA cm^{-2} with contact resistivity for fingers to polysilicon of 4.9 mΩ cm^2. While for the samples with a textured surface, the corresponding values were 56.7 and 1.8 mΩ cm^2 for a 200 nm-thick polysilicon layer with a 1.3 nm-thick thermal oxide.[14] Another study by Firat et al. shows a

A. Chaudhary, J. Hoß, J. Lossen, R. Kopecek
Advanced Cell Concept
International Solar Energy Research Center (ISC) Konstanz
Rudolf-Diesel-Str. 15, D-78467 Konstanz, Germany
E-mail: aditya.chaudhary@isc-konstanz.de

F. Huster
Department of Physics
University of Konstanz
D-78457 Konstanz, Germany

R. van Swaaij, M. Zeman
Photovoltaic Materials and Devices
Delft University of Technology
Mekelweg 4, 2628 CD Delft, Netherlands

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recombination current density in the screen-printed-metallized region and contact resistivity value for samples with a polished surface of 65.8 and 2 mΩ cm^2, respectively, for samples with a 150 nm-thick polysilicon layer and 1.5 nm thermal oxide. For the semitextured surface finish in the same experiment, they obtain values of around 150 fA cm^{-2} and 2.5 mΩ cm^2.[15] For increasing the utilization of polysilicon-based passivated contacts for front as well as rear surfaces of solar cells, it is useful to understand how the surface finish influences contact properties. This understanding will also allow a more accurate estimation of the potential gain from utilizing polysilicon-based passivated contacts in different cell structures and helps to compose lean production process sequences with maximum performance. Many process sequences use single-side etching (SSE), to eliminate unwanted residuals of quartz tube diffusion processes from one side of the wafer. This SSE process was performed for many years in HNO_3–HF solutions, but recently acidic–alkaline and purely alkaline-based processes became available.[16–18]

In this article, we present a study on the dependence of the contact properties of the polysilicon-based passivated layer stack on the substrate surface finish. We utilize two different polysilicon thicknesses and a wide range of fast-firing peak temperatures in this study to study the effect of thermal budget and the influence of the polysilicon thickness on the contact properties for substrates with different surface finishes. High-resolution scanning electron microscope (SEM) images are utilized to visualize the differences in contact formation between the samples at the microscopic level and explain the trends observed in macroscopic contact properties. Finally, the obtained results are used to present a model to explain the current flow between the metal and the polysilicon layer.

2. Experimental Section

We studied the properties of the contact of fire-through silver paste deposited by screen printing on samples as prepared in the subsection. Three different surface finishes were used in this work, namely, planar or saw damage etch, chemically polished, and alkaline textured. These surface finishes were passivated using two different polysilicon layer thicknesses (150 and 200 nm). In the firing-through process, the peak temperature set during fast firing was varied to study the influence of the temperature budget on the contact properties. The belt speed was kept constant at 3 m min^{-1} in this experiment.

2.1. Sample Preparation

We prepared symmetric samples with n^+ polysilicon layer on top of a wet chemically grown interfacial oxide layer. We used standard M2 n-type solar-grade Czochralski wafers (CZ) with an average thickness of 180 ± 10 µm and a base resistivity of 3.9 ± 0.1 Ω cm. The surface finish was obtained in the following way. The planar surface was obtained by 10 µm saw damage etching in 22% NaOH solution at 80 °C. For the chemically polished surface, a RENA InOxide inline tool was used and filled with HNO_3–HF solution, after the texturization step.

The random pyramidal texture was obtained by immersing the wafers in an alkaline solution of KOH and texturing additive MonoTexM (provided by RENA Technologies). After obtaining these surfaces, an ≈1.4 nm-thick interfacial oxide was grown at room temperature (25 °C) using nitric acid (NAOS). In situ phosphorous-doped polysilicon layers were deposited by LPCVD. To get different thicknesses for the polysilicon layers, we changed the deposition time during the LPCVD deposition step. These layers were annealed in a Centrotherm quartz tube furnace to form polysilicon layers by solid-phase crystallization at 825 °C for 30 min.

SiN_x layers were then deposited on both sides of the samples using a Centrotherm cPLASMA PECVD tube reactor. The silicon nitride deposition time was adjusted to have the same thickness for the three surface finishes. The depositions on both sides of the substrate were done subsequently in two separate depositions.

To give a quantitative estimate of the difference in the surface finish, Sdr (%) values were used. The Sdr (%) value was defined as the developed interfacial area ratio, that is, additional area contributed by the texture or other surface morphologies compared with the flat area.

$$\text{Sdr}\,(\%) = \left(\frac{A_{\text{surface}}}{A_{\text{flat}}} - 1\right) \times 100\% \tag{1}$$

where A_{surface} is the area of the surface and A_{flat} is the area of the corresponding flat surface. A higher Sdr (%) value corresponds to a larger increase in the total surface area of the sample.

The Sdr (%) values were calculated for 11–16 across samples with different surface finishes and are presented in **Figure 1**. These values were calculated from laser scanning microscope images using a routine in Mountain Map software, which is explained in the literature.[19] The images were recorded using Olympus OLS400 LEXT microscope.

The samples were screen printed using a specially designed fire-through silver paste for contacting polysilicon-based layer stacks. A high-temperature step was required for contact formation. This step was performed using a fast-firing belt furnace where the sample was passed through successively increasing temperature zones. We used a Centrotherm c.Fire fast-firing furnace for this purpose.

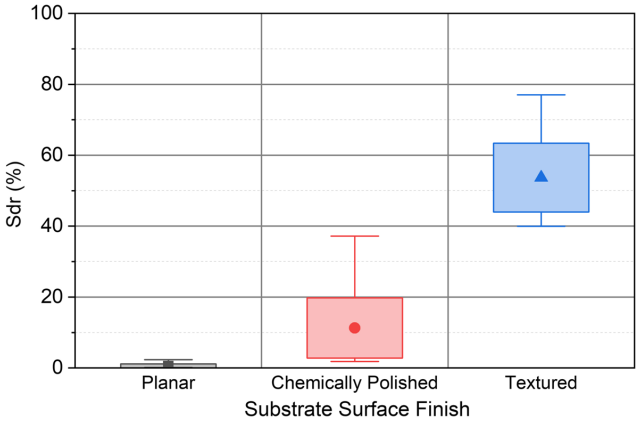

Figure 1. The Sdr (%) values for the three surface finishes: planar, chemically polished, and alkaline textured samples.

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In this experiment, we varied the set point for the highest temperature zone, hereafter referred to as the fast-firing peak temperature, from 760 to 820 °C, in steps of 15 °C. The motivation for choosing these temperatures came from our previous work, which showed J_{0met} values below 100 fA cm^{-2} with contact resistivity values below 3 mΩ cm^2 for samples with 150 nm-thick polysilicon-based contacts.[20]

2.2. Measurement Techniques

The implied open-circuit voltage (iV_{oc}) and recombination current density for the passivated region (J_{0pass}) for the symmetric samples were extracted by quasi-steady-state photoconductance (QSSPC) measurements with a Sinton WCT-120 lifetime tester.[21] iV_{oc} was measured once after silicon nitride deposition and once after printing and fast-firing steps, respectively. We use iV_{oc}-calibrated PL images to calculate the metal–semiconductor recombination current density, which we referred to as J_{0met}. It was calculated from the plot of recombination current density (J_0) as a function of metal fraction, as described in other studies.[20,22]

In addition to J_{0met}, we used contact resistivity to describe the metal semiconductor contact. To measure contact resistivity, we used the transmission line measurement (TLM) on equidistant finger lines of 10 mm. It is worthwhile to mention that we measured a lumped-contact resistivity, as we did not separate the contribution from the different components (resistance between metal and polysilicon and between polysilicon and wafer).

Our project partner, the University of Konstanz, conducted SEM images using Zeiss Neon 40 EsB thermal field-emission SEM apparatus. The samples were prepared by milling to view the interface. **Figure 2** shows an example of the cleaved cross-sectional image for samples with a 200 nm-thick polysilicon layer on a planar substrate. The measured thickness from the SEM image was close to the expected polysilicon thickness and in good accordance with spectroscopic ellipsometer measurements. In this figure, the silicon nitride layer was also marked. Additional images were also taken in top view to visualize the surface of the samples after removal of the bulk silver, glass layer, and the silver crystallites, in sequential etching steps with nitric acid and hydrofluoric acid.[20]

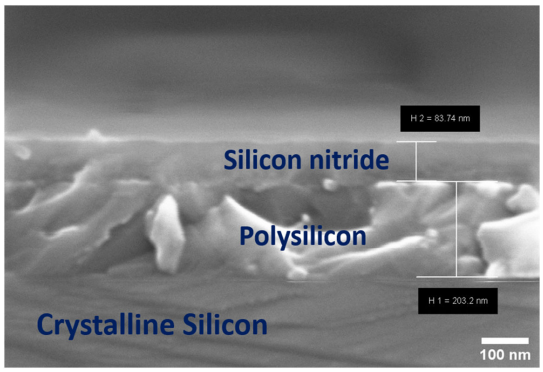

Figure 2. Sample with a 200 nm-thick polysilicon layer with a silicon nitride layer on top.

3. Results and Discussion

The implied open-circuit voltage (iV_{oc}) and recombination current density for the passivated region (J_{0pass}) for the different surface finishes and after SiN_x deposition are presented in **Figure 3**. Some samples were excluded from the metal–polysilicon contact analysis, as they showed a huge variation in passivation quality in comparison with the majority of the samples in the group. These variations might have crept in during the processing and handling steps.

The iV_{oc} of the planar samples is higher as compared with the chemically polished and textured samples. This could be attributed to the surface roughness of the different finish.[23,24] This trend in iV_{oc} is observed for both the 150 nm and 200 nm-thick polysilicon layers, for which we find mean values in the same range. The highest iV_{oc} of 743 mV is obtained for the planar sample with a 150 nm-thick polysilicon layer. The mean J_{0pass} values for the samples remain below 4 fA cm^{-2} for planar and chemically polished samples, while for textured, they are higher at almost 6 fA cm^{-2} before and after fast firing. These observations are in agreement with reports in the literature.[2,10,14]

Figure 3 also shows the iV_{oc} and J_{0pass} of the samples in the unmetallized center after printing of the silver paste and fast firing of the sample (fast-firing peak temperature, from 760 to 820 °C in steps of 15 °C). No significant change in the values of iV_{oc} and J_{0pass} of the samples was observed in the fast-firing peak temperature range we used; hence, all the measurements are grouped together in the plots in Figure 3. The fast-firing process increased the iV_{oc} further slightly, which can be explained by the hydrogenation of defects. After fast firing, the iV_{oc} of the planar samples is higher as compared with the other samples. This is similar to what is observed after silicon nitride deposition. From these results, we conclude that iV_{oc} and J_{0pass} is independent of the polysilicon layer thickness used in this experiment and from passing through the metallization process but is influenced by surface morphology.

3.1. Metallization

The contact resistivity as a function of the fast-firing peak temperatures is presented in **Figure 4**. It was measured on 5–7 TLM structures per sample. The mean contact resistivity values of samples with a 200 nm-thick polysilicon layer are slightly lower compared with the values for the 150 nm-thick polysilicon layer. Thus, utilizing thicker polysilicon layers leads to reduced contact resistivity. This has also been observed and explained in our previous work and in literature.[8,20] For samples having a planar surface, a higher mean contact resistivity value is observed, irrespective of the polysilicon thickness in comparison with other samples. Only at a fast-firing peak temperature of 760 °C, the textured samples show a mean value for contact resistivity slightly higher than that for planar samples. The lowest mean contact resistivity of 2.5 ± 0.1 mΩ cm^2 for the 150 nm-thick polysilicon layer is obtained for a textured sample fired at 820 °C. Similarly, for the textured sample with a 200 nm-thick polysilicon layer fired at 820 °C, the mean contact resistivity of 2.1 ± 0.1 mΩ cm^2 was obtained. A similar trend is also shown

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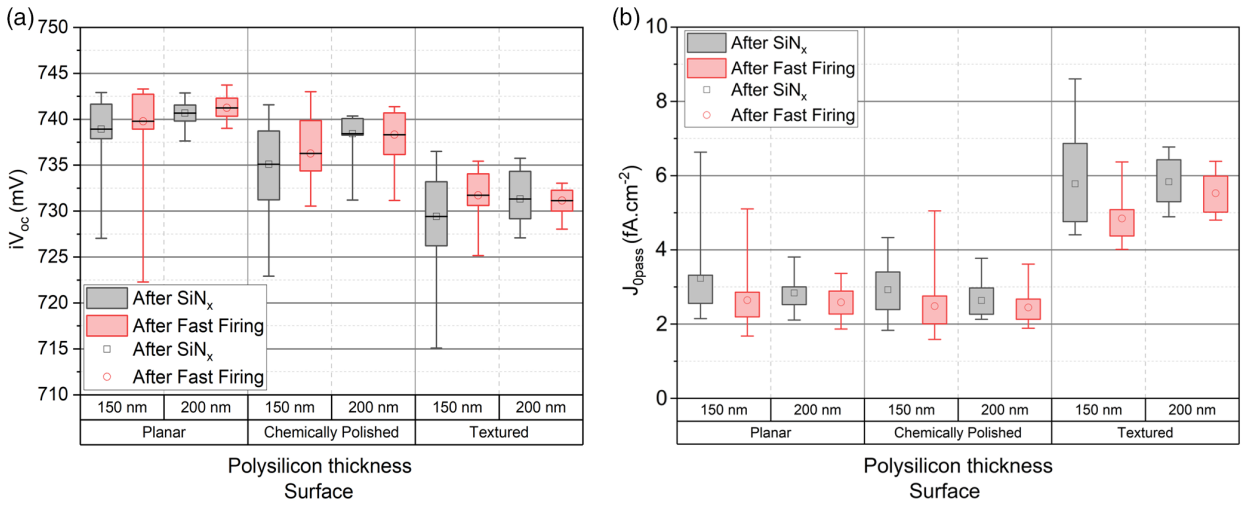

Figure 3. a) Implied open-circuit voltage, iV_{oc} (mV), and b) recombination current density for the passivated region, J_{0pass} (fA cm^{-2}), of unmetallized areas of symmetrical samples with different surface finishes.

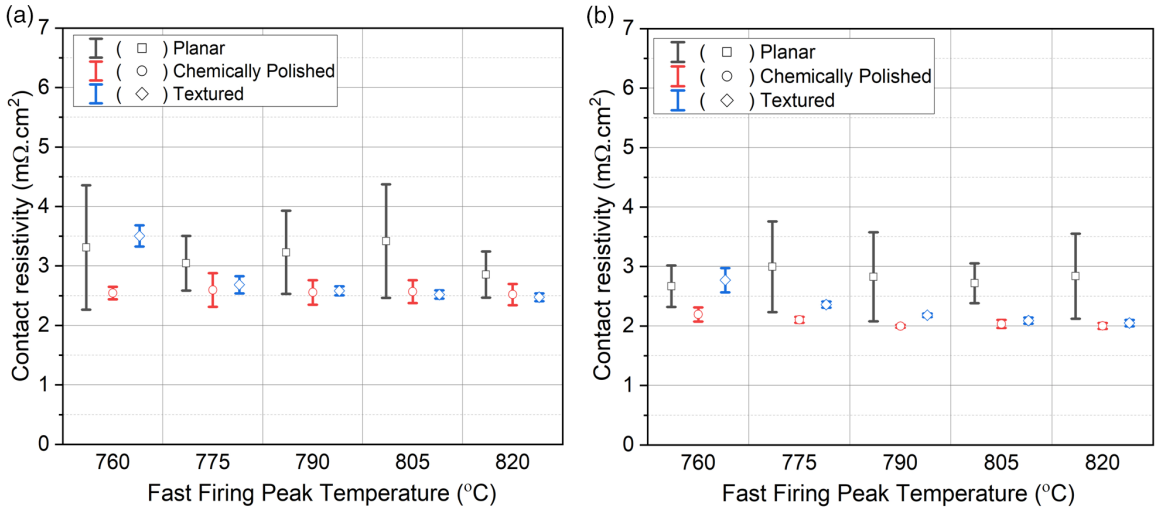

Figure 4. Contact resistivity for a) 150 nm and b) 200 nm polysilicon thickness with different surface finishes.

in the of Firat et al., wherein almost 63% drop in contact resistivity value occurs in a textured surface finish, as compared with the planar surface used for n^+ polysilicon/SiO_x-based contacts.[14]

Lower contact resistivity for the textured samples compared with flat surfaces has also been observed when phosphorus-diffused c-Si surfaces are used.[24,25] The possible reason for the samples with diffused surfaces has been explained by the increased surface area available for contacting as well as more pronounced glass etching due to increased surface roughness, leading to better contact for textured samples.[24,25]

Cross-sectional SEM images for samples with different surface finishes fired at a fast-firing peak temperature of 820 °C are presented in **Figure 5**. The bulk silver finger, glass layer, and silver crystallites embedded in the polysilicon layer have been marked in the images. In Figure 5a,b, we have marked the location of the interfacial oxide with a dashed line in accordance with the cleaved SEM and spectral ellipsometer measurements. The thickness of the polysilicon layer as marked in these images is in accordance with the nominal polysilicon layer thickness, as presented in Section 2.2. For the samples with a chemically polished substrate in Figure 5c,d, it is difficult to ascertain the exact thickness of the polysilicon layer, as the interface between the polysilicon layer and crystalline–silicon wafer cannot be differentiated clearly. For the planar surface and chemically polished samples, shown in Figure 5a-d, we see that the crystallites are present all across the interface. Figure 5e,f shows the samples with a textured surface. From Figure 5e,f, we conclude that most of the silver crystallites are present at the tips and the flanks of the pyramids. This feature has also been observed for silver metallization on textured surfaces with diffused layers.[25,26] We consider that current flow occurs from these silver crystallites to the bulk silver in places where they are in direct contact with it. Further, for metal

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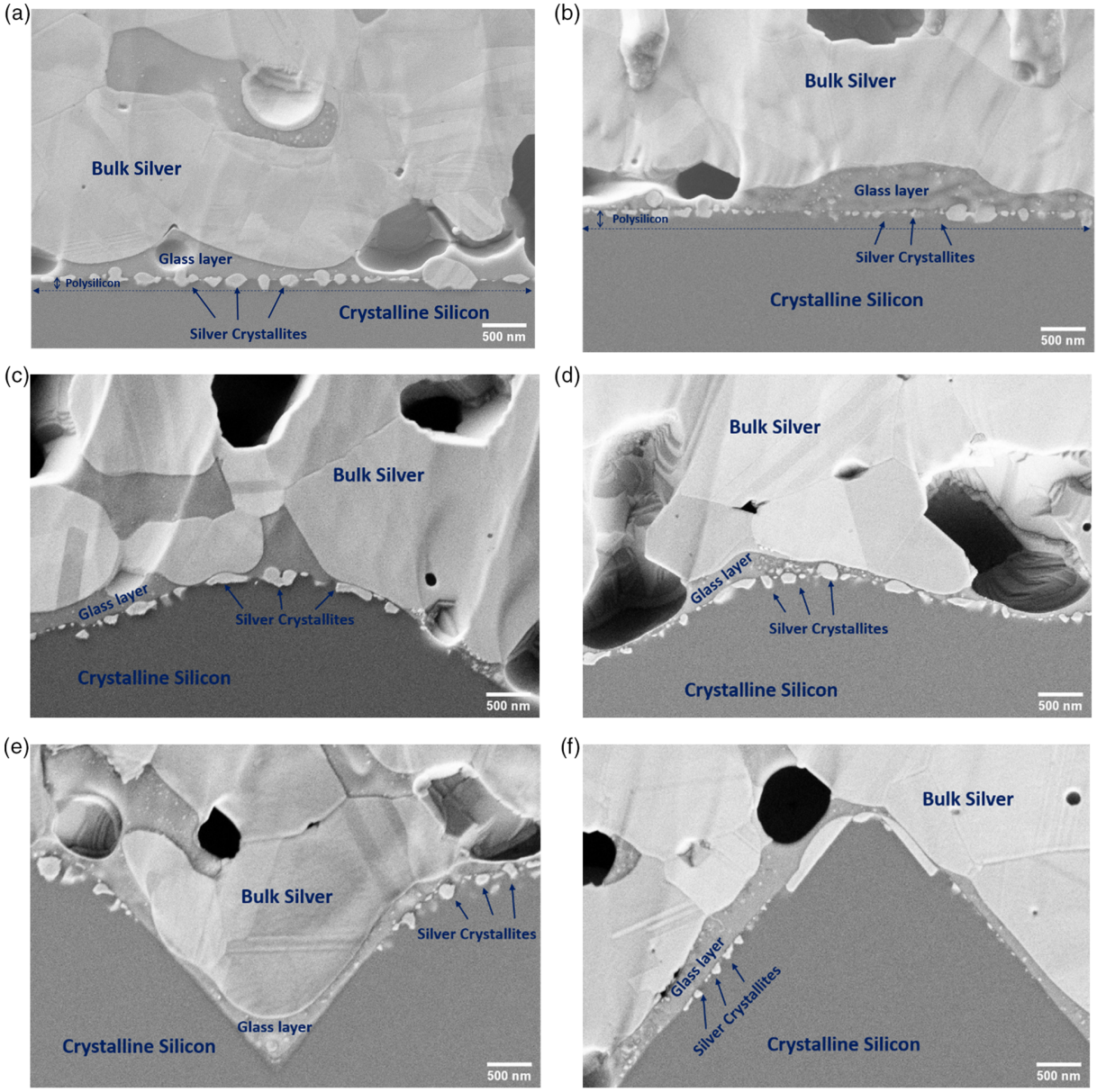

Figure 5. Cross-sectional SEM images for samples with the 150 nm-thick polysilicon layer (left) and 200 nm-thick polysilicon (right) fast fired at peak temperature of 820 °C: a,b) Samples with a planar surface, c,d) with a chemically polished surface, and e,f) with textured surfaces.

contacts to phosphorus-diffused crystalline silicon layers, it was presumed that current might also flow via the glass layer by multistep tunneling, if the glass layer is not too thick.[27,28] We assume that also for the silver–polysilicon interfaces, the silver crystallites and the glass layer determine the current flow through the interface similar to silver–phosphorus-diffused crystalline silicon interface. Compared with the samples with 150 nm-thick polysilicon layers, contact resistivity is lower for samples with the 200 nm thick polysilicon layer, even though there is no significant difference visible in the SEM images. At the fast-firing peak temperature of 760 °C, the density and size of these silver crystallites embedded through to the polysilicon layer are reduced, as shown in **Figure 6**. However, this has no significant impact on contact resistivity for chemically polished and planar samples. Only in the case of textured samples we see a rise in contact resistivity when we reduce the fast-firing peak temperature. In the SEM images of the textured samples, there are almost no silver crystallites embedded in the polysilicon and we think that the low density of these penetrating crystallites could be the reason for the rise in contact resistivity. In **Figure 7**, we show cross-sectional SEM images with higher magnification for the textured surface and we can see places where the glass layer is very thin. If tunneling through the glass layer has a contribution to contact resistance, the occurrence of such regions might be important. Also in these images, we can see silver particles embedded in the glass layer, also called precipitates. They are

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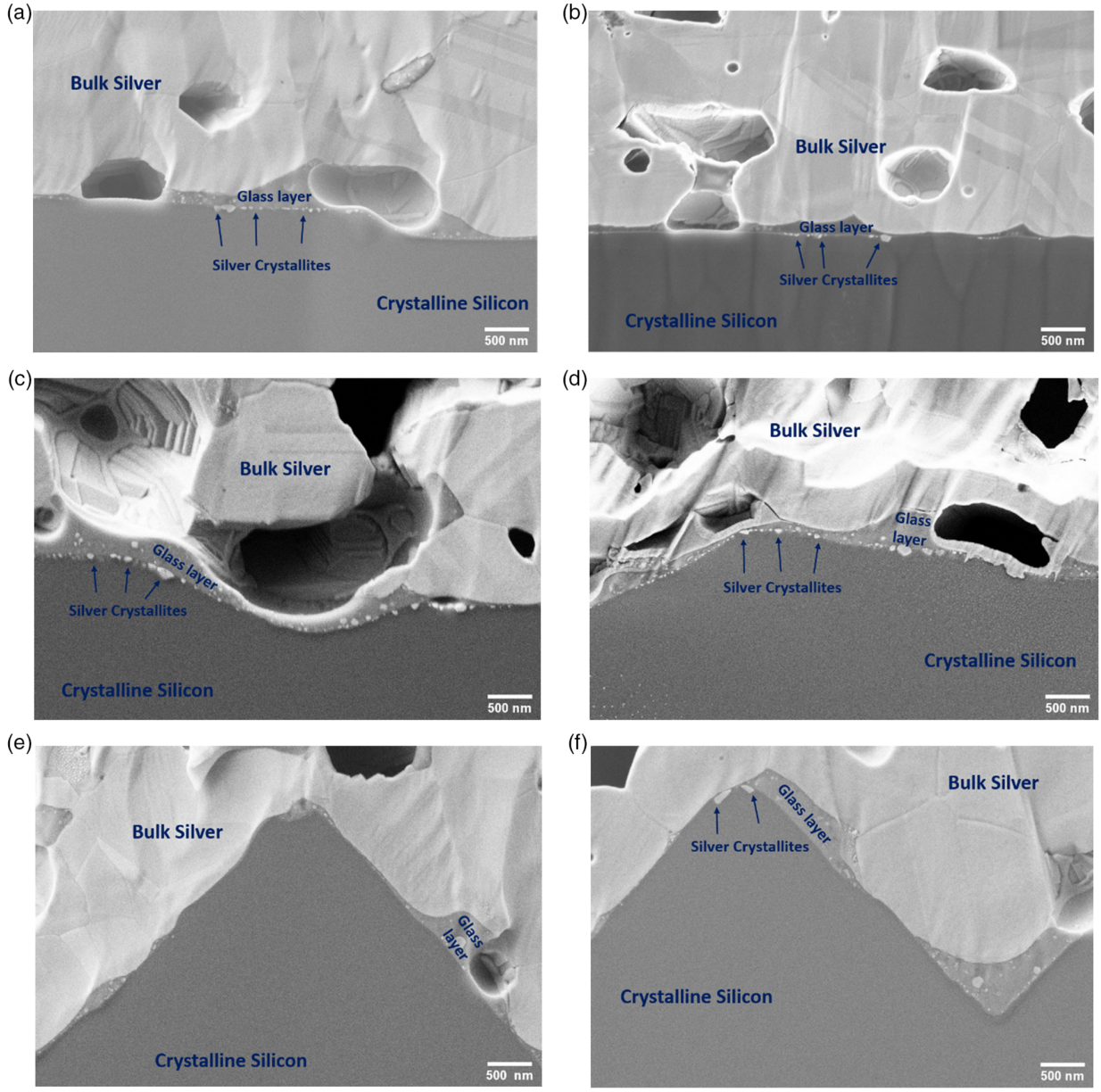

Figure 6. Cross-sectional SEM images for samples with the 150 nm-thick polysilicon layer (left) and 200 nm thick polysilicon (right) fast fired at peak temperature of 760 °C: a,b) Samples with a planar surface, c,d) with a chemically polished surface, and e,f) with textured surfaces.

also visible in Figure 6e,f (as well as in Figure 6c,d). The presence of the silver particles in the glass layer might further enhance the conduction through the glass. We conclude that at places where no silver crystallites penetrate the polysilicon layer, a thin glass layer with silver particles embedded in it could contribute to good electrical conductivity.

However, it would be speculation to judge which mechanism has which contribution from the microscope pictures, as they only show a minimal section of the cross section.

The J_{0met} values for the samples with different surface finishes as a function of the fast-firing peak temperature are presented in **Figure 8**. The error bars in the plots take into account the measurement uncertainty for all individual samples belonging to a group and the uncertainties arising from the process variations across the individual samples.[29]

For the planar samples fast fired at a peak temperature below 820 °C, J_{0met} is of the order of J_{0pass}. Thus, there is no additional recombination from the metallized areas. Similar low values are also observed for the chemically polished samples for the 200 nm-thick polylayer. The samples with a textured surface show higher values of J_{0met} in comparison with the planar and chemically polished samples. For textured samples with a 150 nm-thick polysilicon layer, J_{0met} is higher than the corresponding samples with a 200 nm-thick polysilicon layer. The dependence on fast-firing peak temperature is same for both the thicknesses: J_{0met} increases with higher temperature. Even

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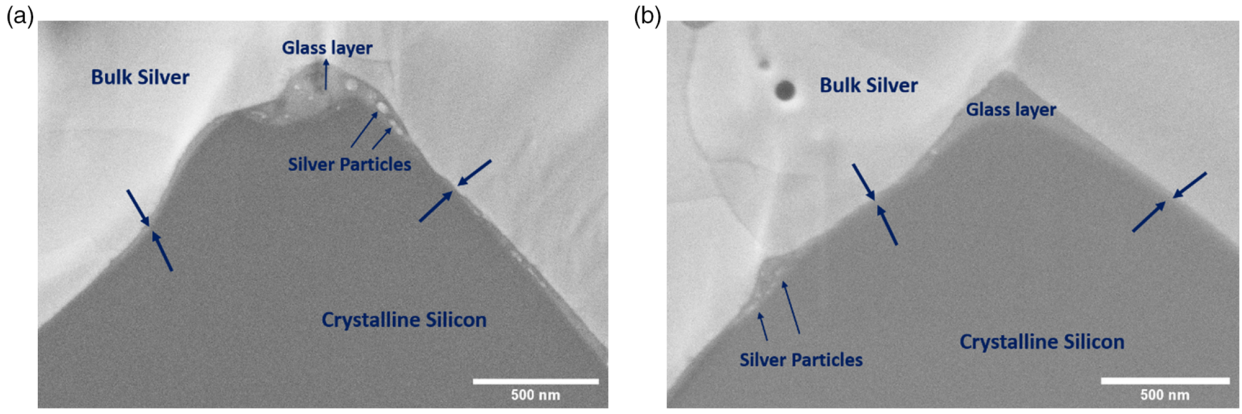

Figure 7. Cross-sectional SEM images for samples with a) 150 nm and b) 200 nm polysilicon layers with textured surfaces, fast fired at the peak temperature of 760 °C.

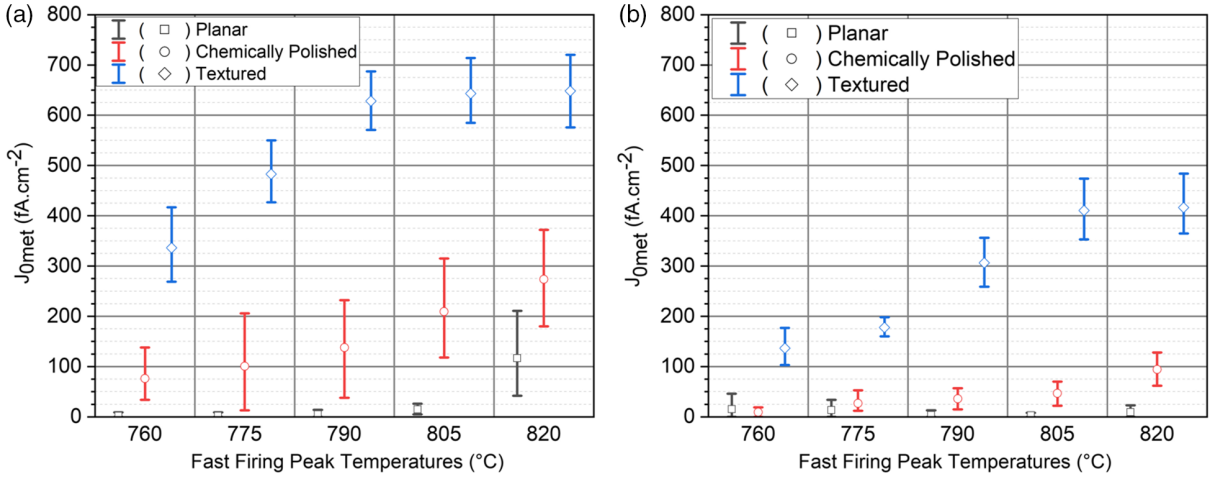

Figure 8. J_{0met} values for a) 150 nm and b) 200 nm polysilicon thicknesses with different surface finishes.

though in the cross-sectional SEM images for textured samples in Figure 7 we see almost no silver crystallites penetrating the polysilicon layer, the J_{0met} value is still high for these samples as compared with chemically polished or planar samples. A reason behind this could be the inhomogeneous thickness of the polysilicon/SiO_x stack. It has been observed that in textured surfaces, the thickness of the oxide and polysilicon can vary, leading to thinner layer stacks at the tips and flanks of the pyramids, as compared with the valleys and flat surfaces.[30,31] Based on this observation, we suggest that, due to the thinner passivating stack, the tips and flanks of the pyramids are more susceptible to damage caused by the metal paste constituents and hence lead to an overall higher metal polysilicon recombination current density.

To confirm the hypothesis of damage to the polysilicon/SiO_x layer at the tips and flanks, we took top-view SEM images of the textured samples fast fired at a peak temperature of 760 °C, as presented in **Figure 9**. These images were taken after the removal of bulk silver, glass layer, and silver crystallites, as mentioned in Section 2.2. In these images, we can see that the polysilicon layer has been consumed and the tips of the pyramids show deep cavities. As an example, we marked a cavity with a red outline. However, in the valleys, the damage to polysilicon is not observed. We suggest that this damage to the passivating layer and the tips of the pyramids is the reason behind high values of J_{0met}. In **Figure 10**, we present the top-view SEM image with higher magnification for the textured sample with a 150 nm-thick polysilicon fast fired at peak temperatures of 820 and 760 °C, respectively. For the sample fast fired at a peak temperature of 820 °C, the damage to the polysilicon layer at the flanks of the pyramids is also visible and more damage is observed as compared with the sample fast fired at a peak temperature of 760 °C. To guide the eye, we marked one of these regions with a red outline. This supports our hypothesis that the damage to the polysilicon/SiO_x stack is more pronounced at the tip and flank of the pyramids. In SEM images of planar and chemically polished samples fast fired at the same peak temperatures, cavities as seen at the tips of the pyramids were not observed. From Figure 9, we can also conclude that the damage to the pyramid tips is less for samples with the 200 nm-thick polysilicon layer as compared with the sample with a thinner polysilicon layer. This could be a reason for the lower J_{0met} for the textured samples with a 200 nm-thick polysilicon layer. Hence, increasing the polysilicon

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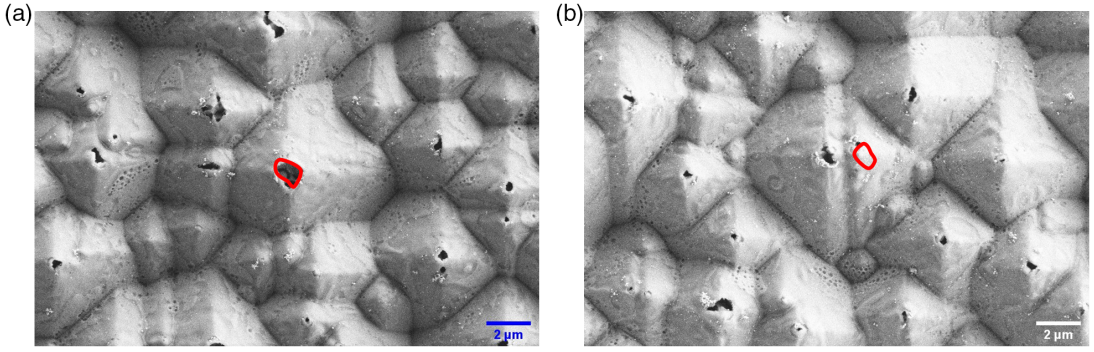

Figure 9. Top-view SEM images for samples with a) 150 nm- and b) 200 nm-thick polysilicon layer with a textured surface, fast fired at peak temperature of 760 °C.

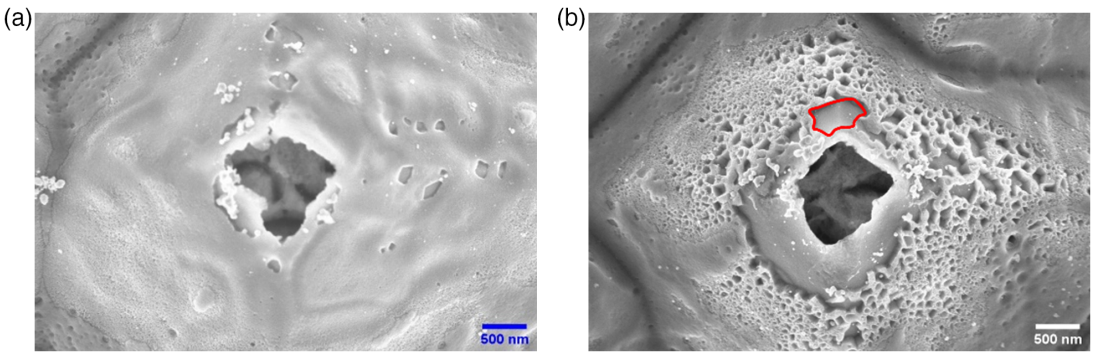

Figure 10. Top-view SEM images for samples with a 150 nm-thick polysilicon layer with a textured surface, fast fired at peak temperatures of a) 760 and b) 820 °C.

thickness can reduce the damage from metallization, although this comes at a price of higher parasitic absorption and longer deposition time.

4. Conclusion

Excellent level of passivation ($iV_{oc} \geq 730$ mV, $J_{0pass} \leq 6$ fA cm^{-2}) is obtained for samples passivated with n^+ polysilicon/SiO_x layers, for the 150 and 200 nm-thick polysilicon layer. The surface finish of the substrate has an effect on passivation. The planar surface outperforms the chemically polished and textured samples in terms of passivation quality as concluded from the higher iV_{oc} and lower J_{0pass} observed for these samples. Excellent values of contact resistivity (≤ 3 mΩ cm^2) and J_{0met} ($\approx J_{0pass}$) are obtained for the planar samples. Textured samples show higher J_{0met}, while the corresponding contact resistivity is comparably low as for chemically polished and planar samples. Excessive damage and the removal of the polysilicon layer at the tips and the flanks of the pyramids in textured samples are suggested to be the cause of their high J_{0met} values. For flat and polished surfaces, small crystallites are distributed more homogeneously over the whole surface.

These results show that the solar cell process flows, which result in a flat surface, either by alkaline etching of the saw damage, or from an acidic emitter etch back of a textured surface, are to be preferred to process flows, which result in a textured surface to be passivated by n+ polysilicon/SiOx-based passivating contact.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

cross-sectional scanning electron microscope, metallization, passivated contacts, polysilicon, screen printing, silicon substrate surface morphology

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