An RF-Powered DLL-Based 2.4-GHz Transmitter for Autonomous Wireless Sensor Nodes

Stoopman, Mark; Philips, Kathleen; Serdijn, Wouter A.

DOI
10.1109/TMTT.2017.2651817

Publication date
2017

Document Version
Accepted author manuscript

Published in
IEEE Transactions on Microwave Theory and Techniques

An RF-Powered DLL-Based 2.4-GHz Transmitter for Autonomous Wireless Sensor Nodes

Mark Stoopman, *Member, IEEE*, Kathleen Philips, *Member, IEEE*, and Wouter A. Serdijn, *Fellow, IEEE*

***Abstract*— This paper presents the system and circuit design of a compact radio frequency (RF)-powered 2.4-GHz CMOS transmitter (TX) to be used for autonomous wireless sensor nodes (WSNs). The proposed TX utilizes the received dedicated RF signal for both energy harvesting as well as frequency synthesis. A TX RF carrier is derived from the received RF signal by means of a delay locked loop and XOR-based frequency multiplier. The 50-Ω load is subsequently driven by a tuned switching RF power amplifier (PA) with 25% duty cycle input for high global efficiency. The design is fabricated in 40-nm CMOS technology and occupies a die area of 0.16 mm^2. Experimental results show a rectifier with 36.83% peak efficiency and power management circuit with 120-nA current consumption that enables a low start-up power of −18.4 dBm. The TX outputs a continuous 2.44-GHz RF signal at −2.57 dBm with 36.5% PA drain efficiency and 23.9% global efficiency from a 915-MHz RF input and supports ON–OFF keying modulation.**

***Index Terms*— Autonomous, power amplifier (PA), radio frequency (RF) energy harvesting, RF-powered, sensitivity, transmitter (TX), wireless sensor node (WSN).**

I. Introduction

THE Achilles' Heel of today's energy scavenged wireless sensor nodes (WSNs) is the unequal balance between the power *consumed* by the WSN and the power *generated* by the energy harvester. On one side of the scale, the power consumption of integrated circuits decreases over time with more advanced CMOS technologies. The energy harvester on the other side of the scale may also benefit from these improvements. It may thus be argued that today's unequal power balance can be solved with future technology improvements. This, however, might not be the case if the difference between the required power and the available power to the harvester simply is too big for a specific application. A second reason is that the scaling of CMOS devices is not necessarily beneficial for the performance of analog circuits [1]. Hence, innovations at both the energy harvester and the WSN are needed.

Radio frequency (RF)-powered WSNs have the distinct advantage over other energy harvesting systems that they are low cost and can operate wirelessly in a large variety of applications, even in cold, dark, and static environments [2]. Furthermore, a dedicated RF source can provide strong and reliable power and can even serve as a data and clock distribution hub such that the complexity and power consumption of the WSN can be greatly reduced [3]. Typical applications where these WSNs can be deployed are dynamic and fault tolerant self-organizing network used for industrial manufacturing, agriculture, and inventory control [4].

The absence of a stable reference frequency in low-cost WSNs makes it very challenging to implement a low-power wireless communication architecture. Passive RF identification (RFID) backscattering, therefore, has been a popular choice because of its simplicity and low power consumption [5]. The functionality and operating range, however, are limited and the system can suffer from reader self-jamming [6]. Other solutions have been proposed that utilize a local oscillator for RF carrier generation [7]. This not only requires significant power, but also is very challenging to realize with sufficient accuracy over process-voltage-temperature variations. In [8], a crystal-less RF-powered transceiver has been implemented that uses the received 915-MHz carrier frequency as phase-locked loop (PLL) reference frequency in order to realize a 2.4-GHz RF carrier to be used for wireless data transmission. A similar architecture has been proposed in [9], where the received signal is fed to an injection-locked frequency multiplier to generate a 402-MHz carrier.

Some fully integrated solutions have been proposed using on-chip antennas. An RFID tag harvesting at 5.8 GHz with a 3.1–10.6-GHz ultra-wideband transmitter (TX) has been proposed in [10]. Although the sensitivity of the tag itself is −14.22 dBm, the on-chip antennas greatly limit the wireless operating range to 7 cm.

In this paper, we demonstrate an RF-powered delay locked loop (DLL)-based 2.4-GHz TX in 40-nm CMOS technology. Frequency synthesis is realized using a dedicated RF signal that serves as input to a DLL and logic XOR-based frequency multiplier, which thereby eliminates the need for inductors and enables a low-complexity, low-power, and area efficient solution.

A nanowatt power management unit is proposed to enable excellent sensitivity and long wireless range RF-powering. A system level description and its key design considerations are given in Section II followed by the circuit design in Section III. Experimental results are discussed in Section IV and the conclusions are given in Section V.

II. System Level

A system level description of the proposed RF-powered TX is shown in Fig. 1. The required energy of the system is supplied wirelessly by an RF energy harvester that converts

Manuscript received February 19, 2016; revised July 12, 2016 and September 12, 2016; accepted January 6, 2017.

M. Stoopman and W. A. Serdijn are with the Section Bioelectronics, Delft University of Technology, 2628 Delft, The Netherlands (e-mail: m.stoopman@tudelft.nl; w.a.serdijn@tudelft.nl).

K. Philips is with the Holst Centre, IMEC-NL, 5605 Eindhoven, The Netherlands (e-mail: kathleen.philips@imec-nl.nl).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2017.2651817

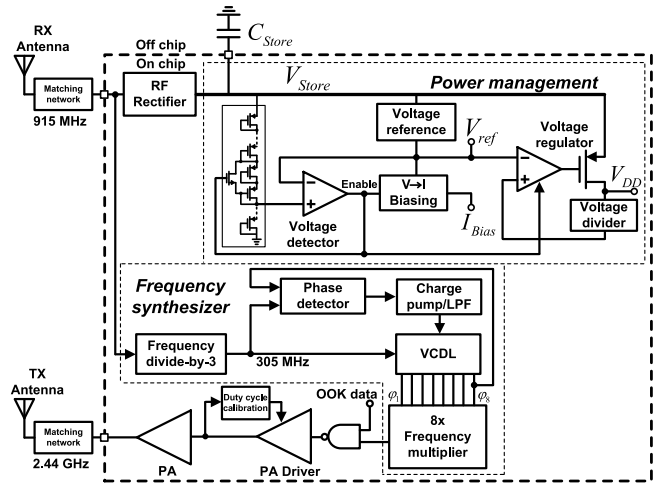


Fig. 1. Proposed RF-powered DLL-based TX.

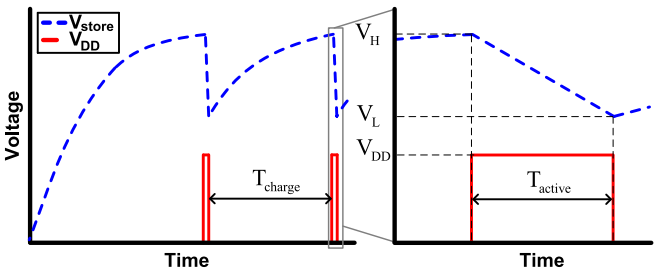


Fig. 2. Power management time-domain waveforms. Left: impression of the storage capacitor voltage. Right: zoomed-in-view illustrating the active period during wireless transmission.

the captured electromagnetic (EM) energy by the antenna into electrical dc (direct current) power. In this paper, a dedicated RF source is assumed within the vicinity of the WSN that provides strong and reliable power in the 902–928-MHz band. The effective isotropic radiated power in this unlicensed band is limited to 4 W by the Federal Communications Commission [11], therefore allowing for a long wireless range.

A. RF Energy Harvesting and Power Management

The harvested energy is first locally stored in a capacitor until enough energy is accumulated to initiate wireless data transmission. The voltage across the storage capacitor C_{store} and the supply voltage V_{DD} is sketched in Fig. 2 to illustrate the power management functionality. Here, V_L and V_H are defined as the low and high voltages that determine the amount of stored energy available to the system. When the system is in harvesting mode, the rectifier charges C_{store} to V_H while only the voltage reference and voltage detector are enabled. When $V_{\text{store}} \geq V_H$, the voltage detector enables the voltage regulator and voltage-to-current (V–I) converter, which provides a stable V_{DD} and bias current I_{bias} while C_{store} is discharged from V_H to V_L. The active time T_{active} is determined by C_{store}, V_H, V_L, V_{DD}, and the total current drawn by the system. Once $V_{\text{store}} \leq V_L$, the detector disables the voltage regulator and the system returns to harvesting mode. The charging time T_{charge} is determined by the available RF power at the antenna, the RF rectifier efficiency, the storage capacitor, and the power consumption of the voltage reference and detector. To determine the system design variables, we first consider the voltage regulator efficiency of this system.

The energy efficiency of an ideal linear voltage regulator (neglecting bias current) with a constant input and output voltage is simply given by $\eta = V_{DD}/V_H$. However, in this system, the input voltage of the voltage regulator decreases linearly with time when assuming a constant current sink I_{load} as load. The energy at the input of the voltage regulator for $V_{DD} \leq V_L \leq V_H$ is thus given by

$$E_{\text{in}} = \int_{t}^{t+T_{\text{active}}} I_{\text{load}} V_{\text{store}} dt = I_{\text{load}} T_{\text{Active}} \frac{V_H + V_L}{2}. \quad (1)$$

The energy delivered to the regulator load is given by $E_{\text{out}} = I_{\text{load}} V_{DD} T_{\text{active}}$. The voltage regulator energy efficiency $\eta_{\text{regulator}} = E_{\text{out}}/E_{\text{in}}$ then can be expressed as

$$\eta_{\text{regulator}} = \frac{V_{DD}}{V_H} \frac{2}{1 + \frac{V_L}{V_H}}. \quad (2)$$

The second term in (2) indicates the relative improvement in efficiency compared with a voltage regulator with constant input and output voltage. The required values for V_{DD} and V_L are determined by the circuit's minimum supply voltage and the voltage regulator implementation. The value of V_H on the other hand depends on the type of modulation and system parameters like power consumption, the amount of data that needs to be transmitted and the value of C_{store}.

The required energy for wireless transmission is found by relating the amount of data to be sent, *Data* [bit], and the *Bitrate* [bit/s] to $\eta_{\text{regulator}}$ and the TX power consumption

$$E_{\text{req}} = \frac{P_{\text{DC,Tx}}}{\eta_{\text{regulator}}} \frac{\text{Data}}{\text{Bitrate}}. \quad (3)$$

ON–OFF keying (OOK) modulation is realized by enabling and disabling the power amplifier (PA) with a NAND gate, the remaining TX core circuits are always on during modulation to minimize the start-up time. The average dc power consumed by the TX during transmission thus is written as $P_{\text{DC,Tx}} = m P_{\text{DC,PA}} + P_{\text{DC,core}}$, where m is the probability of transmitting a "0" and "1" data bit and $P_{\text{DC,PA}}$ and $P_{\text{DC,core}}$ are the dc power consumption of the PA and the remaining core circuits during transmission, respectively. Note that $P_{\text{DC,Tx}}$ is calculated with respect to V_{DD} and not V_H, since the power loss due to the regulator voltage drop is already included in $\eta_{\text{regulator}}$.

The energy available from the storage capacitor is given by

$$E_{\text{store}} = \frac{1}{2} C_{\text{store}} \left(V_H^2 - V_L^2\right). \quad (4)$$

To obtain a high efficiency, the difference between V_H, V_L, and V_{DD} needs to be as small as possible as indicated by (2) while V_{DD} sets the minimum voltage in order to meet the circuit supply specifications. Lowering V_H increases the required C_{store} as evident from (4), which in turn improves the system sensitivity (i.e., the minimum available power to reach V_H), since the rectifier now requires a lower minimum

power at the antenna to charge C_{store} to V_H. For a given value of C_{store}, the minimum V_H is found by substituting (2) into (3) and equating this with (4). Rewriting for V_H gives

$$V_H = \frac{m P_{\text{DC,PA}} + P_{\text{DC,core}}}{C_{\text{store}} V_{DD}} \frac{\text{Data}}{\text{Bitrate}} + V_L. \quad (5)$$

The active transmission time T_{active} is given by

$$T_{\text{active}} = \frac{C_{\text{store}} V_{DD}(V_H - V_L)}{m P_{\text{DC,PA}} + P_{\text{DC,core}}}. \quad (6)$$

As an example, a WSN containing 128 b of information with $C_{\text{store}} = 1$ μF, 500-kb/s data rate, $P_{\text{DC,PA}} = 1.5$ mW, $P_{\text{DC,core}} = 0.5$ mW, $m = 0.5$, $V_{DD} = 1$ V, and $V_L = 1.1$ V requires a minimum V_H of 1.42 V and allows for a transmission time of $T_{\text{active}} = 256$ μs. Using (2), a theoretical voltage regulator efficiency of 79.3% is found. Higher efficiencies can be achieved by increasing C_{store} such that V_H can be lowered. A practical upper limit for the capacitor selection is set by the leakage current. Large (super) capacitors tend to have a relatively high leakage current compared with the current output of the RF energy harvester and thus reduce the harvesting efficiency. In this paper, the storage capacitor is implemented off-chip with a low leakage 1-μF polyester film capacitor.

B. Frequency Synthesizer and Power Amplifier

Using the received dedicated RF signal as a reference frequency for frequency synthesis is a low cost and low complexity way of realizing an RF carrier for wireless data transmission when no other stable reference frequency (like a crystal resonator) is available to the WSN. By extracting the input frequency and applying a frequency multiplication of ratio 8/3, a TX carrier between 2.405–2.47 GHz can be realized that covers almost the entire unlicensed 2.4-GHz band [11]. The 8/3 architecture first has been proposed in [8] and has been implemented using a frequency divider and PLL. In the proposed RF-powered TX shown in Fig. 1, the RF input signal frequency is first divided by three and subsequently used as DLL reference signal. The DLL consists of a phase detector, charge pump (CP) with low-pass filter (LPF), and a voltage controlled delay line (VCDL) that produces eight evenly spaced signals that are fed to an eight-time frequency multiplier. For a 915-MHz input, the majority of the circuits thus operate at 305 MHz while only the PA operates at 2.44 GHz. Since the DLL mainly consists of logic gates and does not require any inductors, it allows for a compact and area efficient solution. The DLL also is a single-pole system and thus inherently stable.

The limited power budget and short-range application of a WSN usually require a small output power (<0 dBm). An RF PA with high global efficiency ($P_{\text{out}}/P_{\text{DC,total}}$), therefore, is required as the output power, which becomes comparable to the total power consumption of the WSN.

III. Circuit Design

A. RF Energy Harvesting and Power Management

The RF rectifier circuit design consists of a five-stage cross-connected differential rectifier, as shown in Fig. 3.

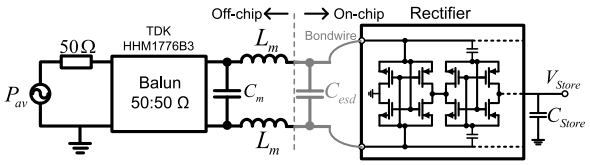


Fig. 3. RF rectifier with external matching network, RF balun, and 50-Ω signal generator.

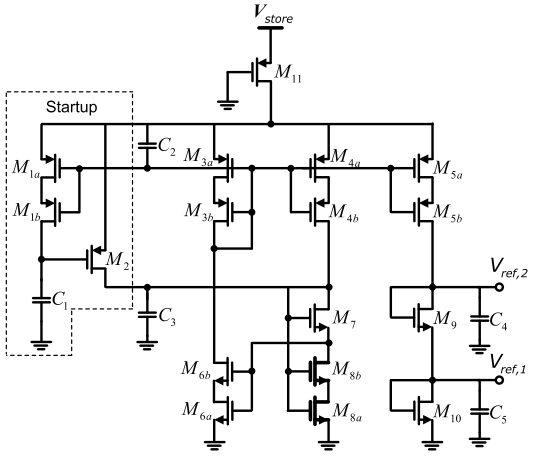


Fig. 4. Voltage reference circuit implementation.

The rectifier is optimized for a capacitive load and a high input impedance (12-j263 Ω at < -20 dBm), which enables a large passive voltage boost. A 50:50-Ω balun, a capacitor, and two high-Q off-chip inductors are utilized to provide an impedance transformation to the 50-Ω signal generator. Readers interested in the codesign principles of antenna-rectifier interfaces are referred to [12].

Only the voltage reference and the voltage detector are enabled in the harvesting mode and, therefore, sink a continuous current from the RF energy harvester. These two circuits together with the rectifier determine the overall system sensitivity and thus are designed for minimum power consumption. The CMOS voltage reference shown in Fig. 4 is utilized, since all its transistors can be biased in the subthreshold region to realize a low voltage and current design. Self-cascoded transistors (denoted by subscript a and b) are used to reduce sensitivity to supply voltage variations without requiring additional biasing or increased supply voltage. The reference voltage $V_{\text{ref},1}$ can be approximated to the threshold voltage difference between M_8 and M_6 [13]. This difference is increased by using a high threshold voltage transistor for M_8 and a low threshold transistor for M_6. This allows for a stable reference voltage, since both transistors experience the same variation over process corners. Device mismatch is minimized by using large transistor sizes and ensuring identical orientation and surrounding environment. Transistor M_9 is an exact copy of M_{10} and generates a second voltage $V_{\text{ref},2} = 2V_{\text{ref},1}$, which is used for various circuit blocks.

Transistor M_{11} is biased in the triode region and creates an LPF with the node capacitance at its drain, which improves the power supply rejection ratio (PSRR) at high frequencies. Simulations indicate an additional 30-dB improvement in PSRR

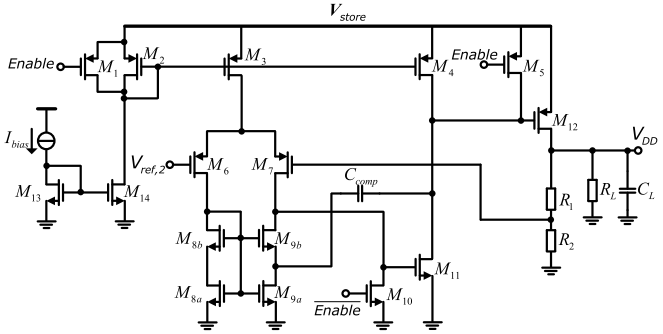


Fig. 5. Voltage regulator circuit implementation.

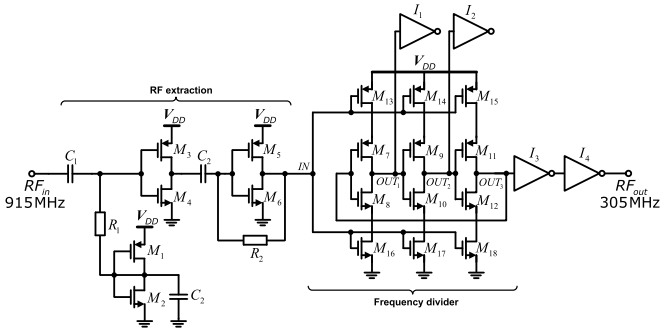


Fig. 6. RF extraction and frequency divider circuit implementation.

at 50 MHz. The voltage drop across M_{11} is negligible due to the low current flowing through it.

A start-up circuit consisting of M_1, M_2, and C_1 injects an initial current into the drain of M_7 when V_{store} increases from 0 V. Once C_1 is charged to V_{store}, transistor M_2 is turned OFF such that the start-up circuit consumes no static current. Postlayout Monte Carlo simulations show a mean voltage of $V_{\text{ref},1} = 316$ mV with a 3σ deviation of 30 mV over process corners and device mismatch. The current consumption at $V_{\text{store}} = 1.2$ V is around 55 nA.

The voltage detector indicated in Fig. 1 amplifies the voltage difference between $V_{\text{ref},2}$ and a scaled version of V_{store}, which is generated by a string of pMOS transistors. When Enable = "0," the capacitor is charged until the voltage detector senses that $(5/11)V_{\text{store}} > V_{\text{ref},2}$, which corresponds to the maximum storage voltage V_H. Enable is set to "1" at this condition, which automatically decreases the storage voltage divider ratio. The detector subsequently disables the system again when $(5/9)V_{\text{store}} < V_{\text{ref},2}$, which corresponds to the minimum storage voltage V_L. The simulated current consumption of the voltage detector equals 15 nA.

The bias currents for the various circuit blocks are generated with a self-biased negative feedback V–I converter (not shown). The V–I converter is disabled during harvesting mode and consumes 3 μA when enabled by the voltage detector.

B. Voltage Regulator

The circuit implementation of the voltage regulator is shown in Fig. 5. A two-stage opamp with pMOS input stage (M_6 and M_7) and pMOS pass transistor (M_{12}) is utilized to accommodate the input voltage and to provide a large dc gain. The system load impedance is represented by C_L and R_L. Note that C_L includes the decoupling capacitors of various circuit blocks and needs to be relatively small compared with C_{store} otherwise a significant amount of energy is lost by simply transferring charge from C_{store} to C_L.

Frequency compensation is done by connecting C_{comp} from the drain of M_{11} to the low impedance intermediate node of the self-cascode transistor consisting of $M_{9,a}$ and $M_{9,b}$. Besides providing pole splitting, an additional left-half plane zero is created that is used to stabilize the amplifier [14]. Transistors M_1, M_5, and M_{10} are used to minimize current leakage by defining critical floating nodes when Enable = "0" (I_{bias} is also switched OFF for Enable = "0.") The total current consumption of the voltage regulator equals 53 μA. For a compensation capacitance of $C_{\text{comp}} = 5.2$ pF, a dc gain, unity gain frequency, and phase margin are found to be 75.8 dB, 18.84 MHz, and 67°, respectively.

C. RF Extraction and Frequency Divider

The received RF signal is ac coupled and amplified by the first inverter-based amplifier consisting of M_3 and M_4, as shown in Fig. 6. Large transistors with high W/L ratios are used to obtain high gain and low noise. A small-scaled inverter replica (M_1 and M_2) is sized to provide a gate bias voltage for the first amplifier while consuming low static current. The input impedance is made high enough not to degrade the RF rectifier performance. The second amplifier (M_5 and M_6) is also ac coupled to avoid duty cycle distortion and provides additional driving capability with fast edge transitions that ensures a rail-to-rail input for the frequency divider. Simulations show that a minimum input power of approximately -26 dBm is required for RF extraction when including the passive voltage boosting obtained in the antenna-rectifier interface.

The frequency divide-by-three circuit converts the 915-MHz rail-to-rail signal into a 305-MHz signal and is based on a digital logic divider to obtain a large locking range [15]. The top and bottom transistors are controlled by the input signal and determine when M_7–M_{12} can go to the next transition. Inverter I_1 and I_2 are dummy cells to ensure equal capacitive loading. The frequency divider is followed by a single-to-differential converter (not shown) based on [16] combined with an edge aligner and pseudodifferential buffer for minimum skew and duty cycle distortion.

D. Delay Locked Loop and Frequency Multiplier

The DLL shown in Fig. 7 consists of an eight-stage VCDL with dummy delay cells at the input and output for equal loading. A phase detector [17] detects the phase difference between the delayed signal at the last stage to the signal at the first stage and subsequently drives a single-ended source-switching CP [18]. The CP output is filtered and controls the delay cells with V_{cntrl} such that eight evenly spaced signals are produced. Each delay cell is implemented with a current-starved pseudodifferential inverter and an additional

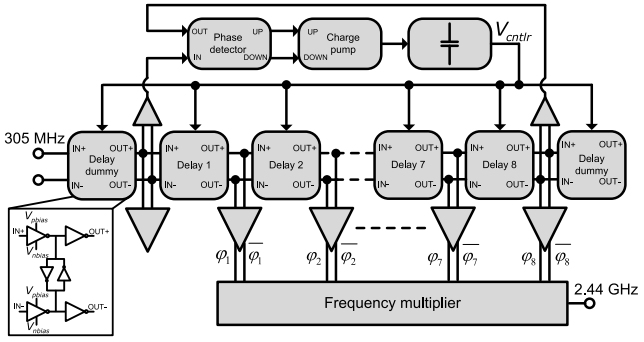


Fig. 7. DLL block diagram with frequency multiplier.

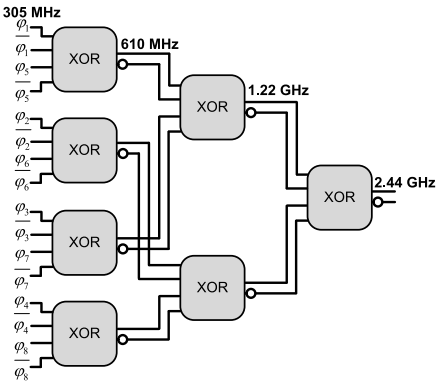


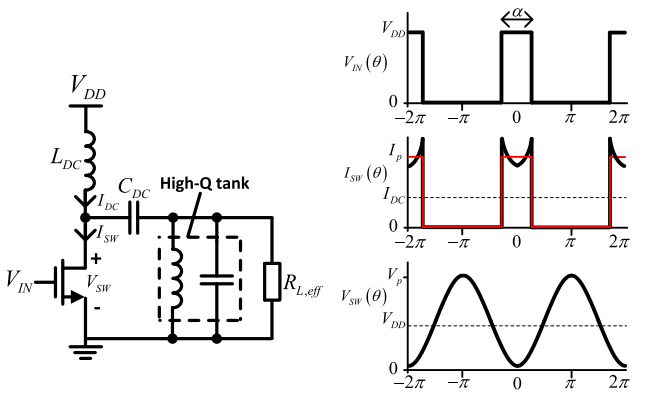
Fig. 8. Symmetrical XOR-based eight-time frequency multiplier.

buffer for low power consumption and good edge alignment for each delay cell. The simulated DLL locking time is approximately 150 ns.

The operating principle of the frequency multiplier is based on an XOR logic gate with two 90° out-of-phase signals applied to its input that generate an output signal at twice the frequency. By distributing the eight different phases available from the VCDL as shown in Fig. 8, an eight-time frequency multiplier can be realized. Monte Carlo simulations show that duty cycle distortion increases with each frequency multiplication. This distortion can be reduced by using duty cycle correction circuits after each frequency multiplication [19]. This, however, significantly increases the power consumption and is considered not to be a feasible solution for the limited power budget. Therefore, both the frequency multiplier and XOR implementation [20] are designed fully symmetrical to reduce mismatch between the different signal paths. Moreover, the 2.44-GHz output signal also does not require exactly 50% duty cycle, since the proposed PA uses a duty cycle calibration loop to obtain high drain efficiency, which will be discussed next.

E. Power Amplifier

The PA in this paper is based on the tuned switching PA, as shown in Fig. 9(a). The transistor acts as a switch with resistance $R_{\rm SW}$ that is controlled by the input signal with duty cycle $d = \alpha/2\pi$. The dc supply voltage is fed through a choke inductor $L_{\rm DC}$ and the load is dc-blocked with $C_{\rm DC}$.



(a) (b)

Fig. 9. (a) Tuned switching PA model. (b) Approximated waveforms of the tuned switching PA.

A high-Q harmonic tank filter at the output filters the fundamental RF signal. The load resistance $R_{L,\rm eff}$ represents the effective resistance seen from the PA.

For the following analysis, it is assumed that the voltage across the switch is a sinusoidal signal oscillating around V_{DD} due to the high-Q harmonic tank filter [21]. This is a fairly good approximation for high load resistances and duty cycles below 0.5. Furthermore, the current waveform through the switch is assumed to be a square wave with peak current I_p.

By inspecting Fig. 9(b), the dc current $I_{\rm DC}$ for a given duty cycle is simply given by $I_{\rm DC} = dI_p$. The fundamental current component for $R_{\rm SW} = 0$ is given by

$$I_1 = \frac{2}{\pi}\int_0^{\pi d} I_p \cos(\theta)d\theta = \frac{2\sin(\pi d)}{\pi} I_p. \tag{7}$$

Given that the fundamental voltage component is given by $V_1 = V_{DD}$ and that the fundamental RF power equals $P_{\rm RFout} = (1/2)V_1 I_1$, then the drain efficiency is given by

$$\eta_{\rm ideal} = \frac{P_{\rm RFout}}{V_{DD} I_{\rm DC}} = \frac{\sin(\pi d)}{\pi d}. \tag{8}$$

The reduction in drain efficiency due to the power loss in the switch resistance R_{SW} can be estimated, as described in [22]

$$\eta_{\rm drain} \approx \eta_{\rm ideal} \frac{P_{\rm RFout}}{P_{\rm RFout} + P_{\rm Switch}}. \tag{9}$$

The average dissipated power in the switch resistance is given by

$$P_{\rm Switch} = \frac{1}{\pi}\int_0^{\pi d} I_P^2 R_{\rm SW} d\theta \tag{10}$$

while the fundamental RF output power can be expressed as

$$P_{\rm RFout} = \frac{1}{2} I_1^2 R_{L,\rm eff}. \tag{11}$$

Substituting (7) into (11), rewriting for I_p^2 and substituting in (10) yields

$$P_{\rm Switch} = \frac{R_{\rm SW}}{R_{L,\rm eff}} \frac{\pi^2 d}{2\sin^2(\pi d)} P_{\rm RFout}. \tag{12}$$

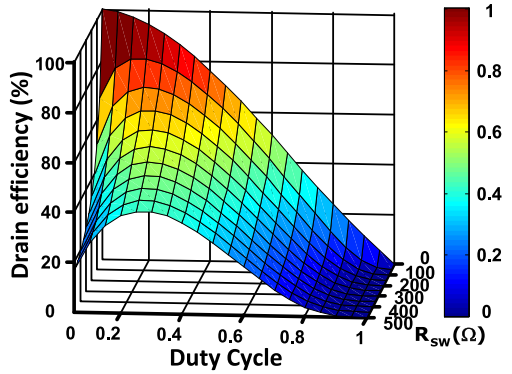


Fig. 10. Surface plot of the calculated drain efficiency when varying the duty cycle and switch resistance for $R_{L,\text{eff}} = 1$ kΩ.

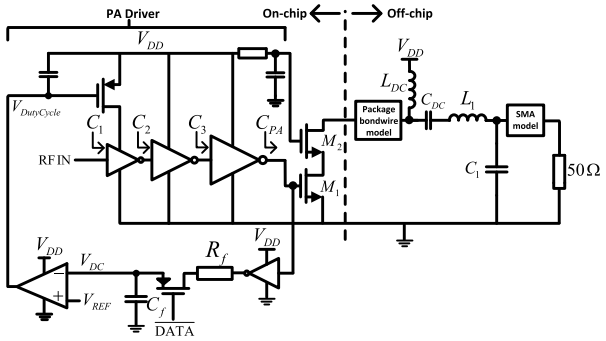


Fig. 11. Tuned switching PA and driver with on-chip duty cycle calibration loop [23].

Finally, the drain efficiency is found by substituting (12) and (8) into (9)

$$\eta_{\text{drain}} \approx \frac{\sin(\pi d)}{\pi d} \frac{1}{1 + \frac{R_{\text{SW}}}{R_{L,\text{eff}}} \frac{\pi^2 d}{2\sin^2(\pi d)}}. \tag{13}$$

Fig. 10 shows a surface plot of (13) for $R_{L,\text{eff}} = 1$ kΩ where the duty cycle is varied between 0 and 1 and the switch resistance varies between 0 and 500 Ω. For $R_{\text{SW}} = 0$, the drain efficiency always increases for lower duty cycles. However, this is no longer the case when $R_{\text{SW}} \neq 0$. When the duty cycle decreases, the power loss due to R_{SW} becomes relatively large, because the fundamental RF output power approaches zero. Therefore, for a non-ideal switch, an optimum duty cycle for maximum drain efficiency is found roughly between $0.2 \leq d \leq 0.3$, depending on R_{SW} and $R_{L,\text{eff}}$. Simulation results (not shown) indicate that this simplified model describes the drain efficiency with an inaccuracy of 12% or better for duty cycles below 0.5 and R_{SW} below 500 Ω.

Since no higher frequency signals are available to derive a reduced duty cycle from, the on-chip duty cycle calibration loop is used, as shown in Fig. 11. The PA driver consists of a cascade of tapered inverters, where the first inverter has an additional pMOS transistor that controls the inverter's rise time. The voltage at the PA input (M_1) is sensed with a small inverter that drives an LPF to obtain the dc voltage, which is an indication of the duty cycle. An opamp subsequently compares the dc voltage to a reference voltage and regulates the gate of the pMOS transistor. The reference voltage is set to $V_{\text{REF}} = (3/4)V_{DD}$ to obtain a 25% duty cycle. The PA

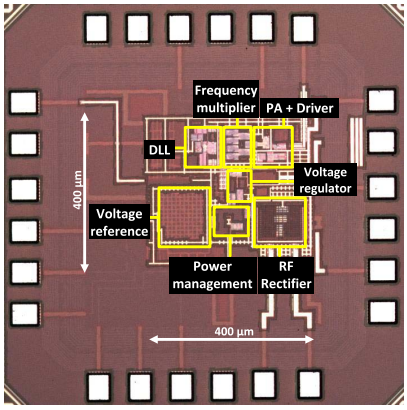


Fig. 12. Chip microphotograph with layout details.

transistors M_1 and M_2 are sized to obtain $R_{SW} \approx 220$ Ω and a total gate capacitance of approximately 36 fF. When using $R_{L,\text{eff}} = 1$ kΩ, it follows from (13) that $\eta_{\text{drain}} \approx 58\%$ for $P_{\text{RFout}} = -3$ dBm.

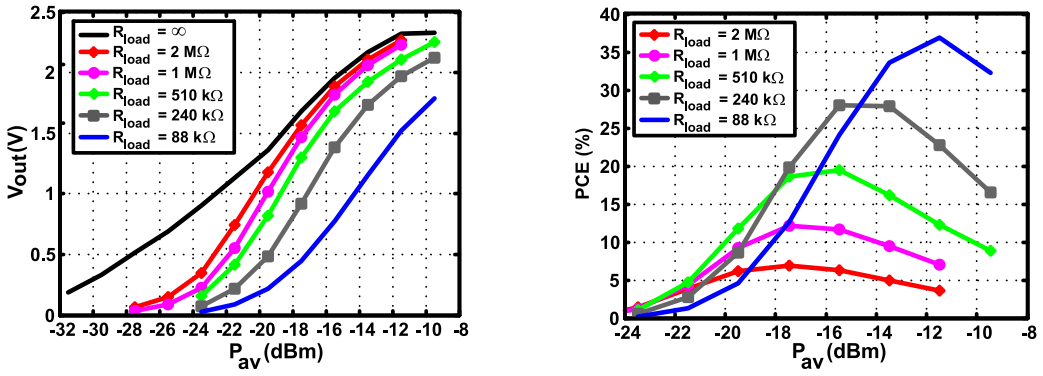
IV. Experimental Results

The TX is fabricated in TSMC 40-nm CMOS technology and is bond wired to a 24-lead QFN package, which is mounted on a PCB for testing. The active area occupies 0.16 mm^2, as shown in Fig. 12.

The RF rectifier performance is first evaluated by disconnecting the power management circuits and measuring the steady-state dc output voltage for different load conditions and available power. An off-chip picoampere input bias opamp is used to minimize the resistive loading effect of the measurement equipment. A 50-Ω signal generator is used to supply a 915-MHz RF continuous wave. The losses of the off-chip matching network (Fig. 3) are included while the insertion loss of the off-chip balun is excluded, since a balun is not required when replacing the 50-Ω source with a differential antenna.

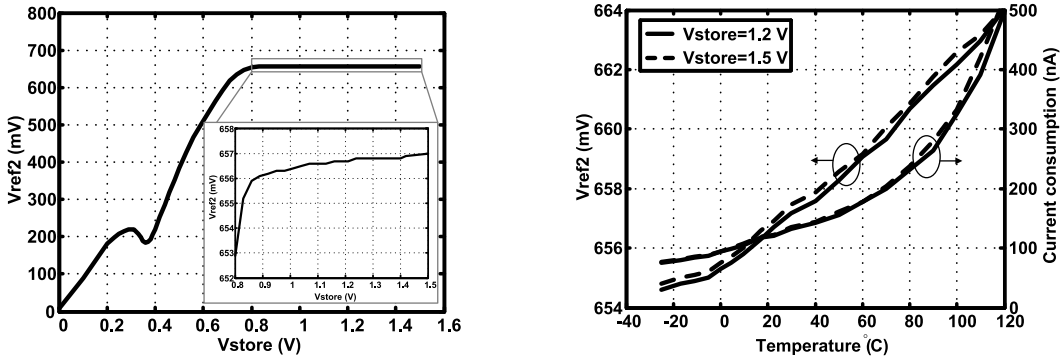
Fig. 13(a) shows the measured dc output voltage versus P_{av} for different load conditions. For the highest load resistance (a purely capacitive load, $R_{\text{load}} = \infty$ and $C_{\text{store}} = 1$ µF), the load current is the lowest and thus the rectifier requires only −22.6 and −18.6 dBm to generate 1 and 1.5 V, respectively. The power conversion efficiency (PCE) is determined by measuring the output voltage versus P_{av} for different load resistances and subsequently calculating $\text{PCE} = V_{\text{out}}^2/(R_{\text{load}} P_{\text{av}})$. The PCE presented in Fig. 13(b) peaks around −11.47 dBm with a maximum of 36.83% for a load resistance of $R_{\text{load}} = 88$ kΩ. The optimum load resistance is a function of the antenna Q-factor and the number of rectifying stages, but also varies with P_{av} due to the nonlinear input impedance of the rectifier [12]. The measured −3-dB bandwidth at $P_{\text{av}} = -18$ dBm equals approximately 60 MHz.

Fig. 14(a) shows that $V_{\text{ref},2}$ versus V_{store} characteristics at room temperature. For $V_{\text{store}} \leq 0.3$ V, the voltage reference output follows V_{store}, because a transistor in the voltage detector (not shown) connects $V_{\text{ref},2}$ to V_{store} to prevent a false positive "Enable." Once $V_{\text{store}} \geq 0.4$ V, this transistor is switched OFF and $V_{\text{ref},2}$ settles to approximately 656.5 mV. The voltage reference changes 0.9 mV when V_{store}



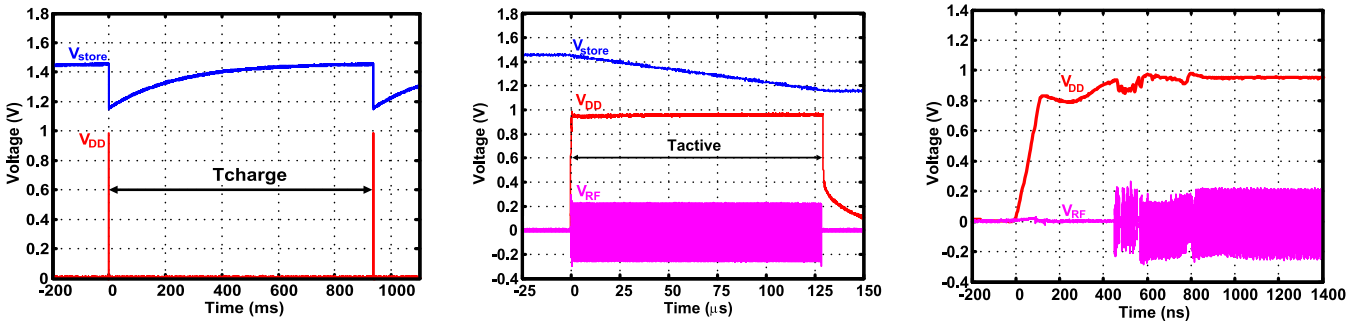
(a) (b)

Fig. 13. (a) Measured dc output voltage V_{out}. (b) PCE for different load conditions and available power P_{av}.



(a) (b)

Fig. 14. (a) Measured reference voltage V_{ref2} versus V_{store}. (b) Measured voltage reference V_{ref2} and its current consumption versus temperature.



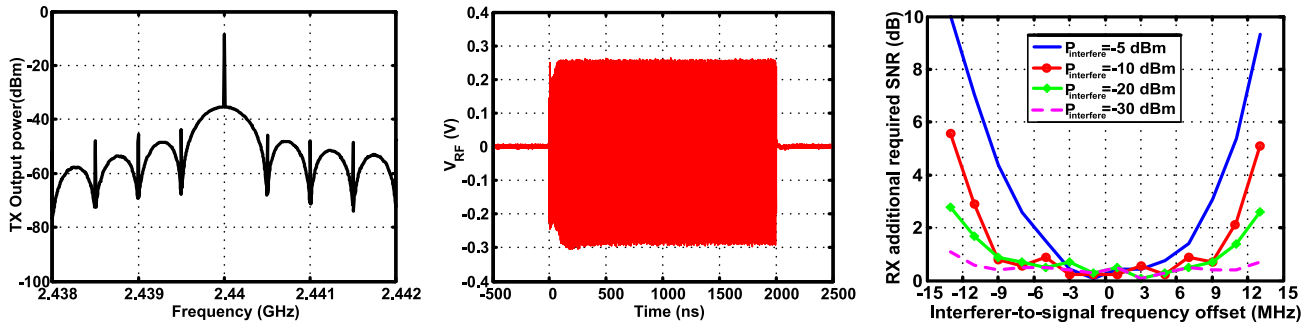
(a) (b) (c)

Fig. 15. Measured (a) waveforms of V_{store} and regulated V_{DD}, (b) active period, and (c) cold-start behavior of complete TX at minimum start-up power $P_{\text{av}} = -18.4$ dBm.

changes from 0.9 to 1.5 V, resulting in a line sensitivity $(\Delta V_{\text{ref},2}/\Delta V_{\text{store}})/V_{\text{ref},2}$ of 0.228%/V. The measured current consumption for $V_{\text{store}} > 0.8$ V (steady state) equals 124 nA.

The effect of temperature variations on the voltage reference is shown in Fig. 14(b). The voltage reference changes 9.6 mV between -20 °C to 120 °C, resulting in a temperature coefficient of 104.5 ppm/°C. Over the same temperature range, the total current drawn by the voltage reference and detector changes from 80 to 500 nA. Although the current consumption increases at high temperatures, the rectifier output current also increases, because the transistor threshold voltage decreases with increasing temperature and thus compensates for this effect. Note that there is a very small difference for both the voltage and the current characteristics when V_{store} is changed from 1.2 to 1.5 V (corresponding approximately to the voltage range V_L to V_H).

The measured charging waveform of V_{store} and V_{DD} shown in Fig. 15(a) is obtained with a minimum start-up power of $P_{\text{av}} = -18.4$ dBm. At this power level, the rectifier (when loaded with the voltage reference and detector) is able to generate $V_H = 1.44$ V and takes approximately 1.4 s from 0 V. The voltage detector subsequently enables the voltage regulator and all other circuit blocks. The current drawn by the TX discharges the storage capacitor until $V_L = 1.16$ V,



(a) (b) (c)

Fig. 16. Measured (a) TX output spectrum of a 0.5-Mb/s pseudorandom OOK modulation and (b) time-domain waveform of a logic "1" transmission. (c) Additional required SNR to maintain a 0.1% BER versus interferer-to-signal frequency offset with desired input signal at −18.4 dBm.

after which the detector again disables the circuit blocks. The charging time to reach V_H from V_L for $P_{\text{av}} = -18.4$ dBm and $C_{\text{store}} = 1\ \mu$F equals 936 ms. For higher power levels, T_{charge} decreases such that a higher sensor update rate can be realized.

Fig. 15(b) shows a zoomed-in-view of the active period where the TX is enabled continuously. While the storage capacitor is being discharged from V_H to V_L, the voltage regulator stabilizes V_{DD} and the TX outputs a continuous 2.44-GHz RF signal at −2.57 dBm for $T_{\text{active}} = 128\ \mu$s, which corresponds well with (6) for $m = 1$. During continuous transmission (no modulation), the voltage regulator consumes 54 μW, the frequency synthesizer 637 μW, and the PA driver consumes 105 μW. The PA drain current equals 1516 μA, resulting in a drain efficiency of 36.5% from a 1 V regulated supply. This is lower than the theoretical 58% predicted by (13). The main loss mechanisms not included in the analysis are the resistive and mismatch losses of the matching network and the nonideal square wave voltage at the PA input.

The total power consumed by the TX is 2.312 mW, resulting in a global efficiency $P_{\text{out}}/P_{\text{DC,total}}$ of 23.9%. The regulator efficiency is measured indirectly by calculating $\eta_{\text{regulator}}$ from the measured quantities in (3) and (4). It was found that the measured $\eta_{\text{regulator}}$ was 81.3%, which is 5.7% higher than predicted by (2). This discrepancy is caused by the fact that the analysis in Section II assumes a constant current sink as source, whereas the obtained measurement results include the complete radio with start-up and settling effects. Measurements at $P_{\text{av}} = -18.4$ dBm show a residual rms jitter of 0.9 ps at 2.44 GHz and a phase noise of −112.5 dBc/Hz at 1-MHz offset. The measured second and third harmonic tones are both 47 dB below the fundamental tone, while the closest spurious tone is −23 dBc and is located 305 MHz away from the carrier.

The start-up behavior of the complete TX at $P_{\text{av}} = -18.4$ dBm input is shown in Fig. 15(c). Note that this includes all cold-start settling effects like voltage and current biasing and internal and external capacitors charging effects. The DLL is activated after approximately 500 ns and after 800 ns, and the complete TX is settled with a regulated supply. The minimum measured power for RF extraction is −25.47 dBm across the entire 902–928-MHz unlicensed band.

The measured TX output spectrum for a 0.5-Mb/s pseudorandom OOK modulated signal is shown in Fig. 16(a). The measured power consumption of the complete TX during OOK modulation equals 1.46 mW. Measurement results showed, however, that the large PA start-up current causes a small voltage dip at the output of the voltage regulator. Since all circuit blocks share the same supply voltage, this voltage dip also detunes the DLL and causes a dip in the RF output during transmission of a logic "1," as shown in Fig. 16(b). As the duration of this voltage dip is approximately 75 ns, this limits the attainable bitrate. An external low dropout regulator was used to test this hypothesis, which indeed eliminated the dip in the RF signal and allowed for higher bitrates.

Fig. 16(c) gives an indication of the required receiver (RX) SNR when a continuous interference signal is present near the desired dedicated RF signal, which is utilized for frequency synthesis. This continuous interference signal can, for example, be considered to belong to a neighboring dedicated RF source that extends the area of wireless powering. The TX output signal is measured for a consecutive "0101" series at the RF input while a continuous wave interferer is added at a given frequency offset from the dedicated RF signal. The dedicated RF signal is set to the minimum start-up power of −18.4 dBm. Subsequently, the required SNR for a 0.1% bit error rate (BER) at the RX is determined using an optimum threshold noncoherent demodulator, which is implemented in MATLAB. When the interferer power level is below the dedicated RF power level, no significant performance reduction at the RX is observed. When the interferer power level is increased further, it shows that a higher SNR at the RX is required to maintain a 0.1% BER. A higher power interferer with small frequency offset does not degrade the required SNR, because the stronger continuous wave interferer simply determines the reference signal for the frequency synthesizer. Note that this does not hold in case of, for example, a frequency modulated interference signal. A high power interferer with larger frequency offset will more frequently generate a destructive signal at the input of the RF extraction circuit and hence results in more edge misalignments at the DLL and frequency multiplier and also impacts the fundamental signal frequency and amplitude. In order to demodulate the desired signal with a −10-dBm continuous wave interferer at 13-MHz offset, the RX requires an increase of 5 dB in SNR,

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ART

Parameters	This work	Shirane '15 [5]	Papotto '14 [8]	Xia '14 [9]	Ito '14 [24]
Technology	40 nm	65 nm	90 nm	65 nm	65 nm
Active die area$^{(a)}$	0.16 mm^2	0.13 mm^2	0.8 mm^2	1.7 mm^2	0.3 mm^2
Frequency	915 MHz / 2.44 GHz	5.8 GHz (backscattering)	915 MHz / 2.44 GHz	904.5 MHz / 402 MHz	800 MHz / 2.5 GHz UWB
Minimum startup RF power$^{(b)}$	-18.4 dBm	-5.9 dBm	-15 dBm	-20 dBm	-19.5 dBm
Rectifier max PCE	36.83% @ -11.47 dBm	-	16.1% @ -15.83 dBm	-	-
TX output power	-2.57 dBm	-28.6 dBm	-12.5 dBm	-16 dBm	-62.1 dBm
TX global efficiency	23.9% @ 1V supply	1.2% @ 0.6V supply	6.53% @ 1V supply	10.8% @ 0.6-1V supply	0.027% @ 0.6-1V supply
TX Data rate	0.5 Mbps (OOK)	2.5 Mbps (QAM)	5 Mbps (OOK)	0.25 Mbps (OOK)	1 Mbps (OOK)

(a): Extracted or estimated from available data.
(b): Available power P_{av} (including component and mismatch losses).

thereby limiting the maximum wireless range that can be achieved. More filtering at the antenna input in this case could be added to prevent this degradation.

Table I summarizes the measured experimental results and compares it with prior art. This paper shows a very small active area of only 0.16 mm^2 due to the compact DLL and frequency multiplier circuits. Only the work in [5] shows a smaller die area, but is based on backscattering and thus is much more limited in output power and also requires 12.5 dB more RF power for start-up. Also, a TX global efficiency of 23.9% shows favorable compared with its competitors. The minimum required start-up power shows excellent sensitivity to enable long wireless range operation.

V. CONCLUSION

A compact RF-powered DLL-based 2.4-GHz CMOS TX has been presented. The received dedicated RF signal is used for both RF energy harvesting as well as frequency synthesis by using a nanowatt power management circuit combined with a DLL and XOR-based frequency multiplier. A tuned switching RF PA with 25% duty cycle input is utilized in order to obtain high global efficiency for <0-dBm output power.

Experimental results of a 0.16 mm^2 40-nm CMOS prototype show a maximum rectifier efficiency of 36.83% and a power management circuit with 120-nA current consumption during harvesting mode. For a 1-μF storage capacitor and -18.4-dBm minimum available power at 915-MHz RF input, the TX outputs a continuous 2.44-GHz RF signal at -2.57 dBm for 128 μs with 36.5% PA drain efficiency and 23.9% global efficiency. The complete TX consumes 1.46 mW during OOK modulation at 0.5 Mb/s.

REFERENCES

[1] P. Kinget, "Designing analog and RF circuits in nanoscale CMOS technologies: Scale the supply, reduce the area and use digital gates," in *Proc. IEEE Int. Conf. Microw. Commun. Antennas Electron. Syst.*, Nov. 2009, pp. 9–11.

[2] H. J. Visser and R. J. M. Vullers, "RF energy harvesting and transport for wireless sensor network applications: Principles and requirements," *Proc. IEEE*, vol. 101, no. 6, pp. 1410–1423, Jun. 2013.

[3] M. Baghaei-Nejad *et al.*, "A remote-powered RFID tag with 10Mb/s UWB uplink and -18.5dBm sensitivity UHF downlink in 0.18 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2009, pp. 198–199.

[4] K. Sohrabi, J. Gao, V. Ailawadhi, and G. J. Pottie, "Protocols for self-organization of a wireless sensor network," *IEEE Pers. Commun.*, vol. 7, no. 5, pp. 16–27, Oct. 2000.

[5] A. Shirane *et al.*, "A 5.8GHz RF-powered transceiver with a 113 μW 32-QAM transmitter employing the IF-based quadrature backscattering technique," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[6] K. Finkenzeller, *RFID Handbook: Fundamentals and Applications in Contactless Smart Cards and Identification*, 2nd ed. West Sussex, U.K.: Wiley, 2003.

[7] S. Pellerano, J. Alvarado, and Y. Palaskas, "A mm-wave power-harvesting RFID tag in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1627–1637, Aug. 2010.

[8] G. Papotto, F. Carrara, A. Finocchiaro, and G. Palmisano, "A 90-nm CMOS 5-Mbps crystal-less RF-powered transceiver for wireless sensor network nodes," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 335–346, Feb. 2014.

[9] X. Lingli, C. Jiao, N. E. Glover, and P. Chiang, "0.56 V, –20 dBm RF-powered, multi-node wireless body area network system-on-a-chip with harvesting-efficiency tracking loop," *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1345–1355, Jun. 2014.

[10] S. Radiom, M. Baghaei-Nejad, G. Vandenbosch, L.-R. Zheng, and G. Gielen, "Far-field RF powering system for RFID and implantable devices with monolithically integrated on-chip antenna," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1746–1758, Sep. 2010.

[11] (May 2015). *Federal Communications Commission (FCC), Code of Federal Regulations, Title 47-Telecommunication, Chapter 1, Part 15*. [Online]. Available: http://www.ecfr.gov

[12] M. Stoopman, S. Keyrouz, H. J. Visser, K. Philips, and W. A. Serdijn, "Co-design of a CMOS rectifier and small loop antenna for highly sensitive RF energy harvesters," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 622–634, Mar. 2014.

[13] L. Magnelli, F. Crupi, P. Corsonello, C. Pace, and G. Iannaccone, "A 2.6 nW, 0.45 V temperature-compensated subthreshold CMOS voltage reference," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 465–474, Feb. 2011.

[14] V. Saxena and R. J. Baker, "Compensation of CMOS op-amps using split-length transistors," in *Proc. 51st Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2008, pp. 109–112.

[15] M. S. Jahan and J. Holleman, "A 4 μW dual-modulus frequency divider with 198% locking range for MICS band applications," *Analog Integr. Circuits Signal Process.*, vol. 77, no. 3, pp. 549–556, Dec. 2013.

[16] Y.-S. Park *et al.*, "PVT-invariant single-to-differential data converter with minimum skew and duty-ratio distortion," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2008, pp. 1902–1905.

[17] S. Sidiropoulos, D. Liu, J. Kim, G. Wei, and M. Horowitz, "Adaptive bandwidth DLLs and PLLs using regulated supply CMOS buffers," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2000, pp. 124–127.

[18] J. M. Ingino and V. R. von Kaenel, "A 4-GHz clock system for a high-performance system-on-a-chip design," *IEEE J. Solid-State Circuits*, vol. 36, no. 11, pp. 1693–1698, Nov. 2001.

[19] K.-H. Cheng, C.-M. Chang, S.-Y. Jiang, and W.-B. Yang, "A 2GHz fully differential DLL-based frequency multiplier for high speed serial link circuit," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2005, pp. 1174–1177.

[20] M. Mansuri *et al.*, "A scalable 0.128–1 Tb/s, 0.8–2.6 pJ/bit, 64-lane parallel I/O in 32-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3229–3242, Dec. 2013.

[21] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Norwood, MA, USA: Artech House, 2006.

[22] F. H. Raab and N. O. Sokal, "Transistor power losses in the class E tuned power amplifier," *IEEE J. Solid-State Circuits*, vol. SSC-13, no. 6, pp. 912–914, Dec. 1978.
[23] M. Stoopman, K. Philips, and W. A. Serdijn, "A 2.4 GHz power amplifier with 40% global efficiency at −5 dBm output for autonomous wireless sensor nodes," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 4, pp. 256–258, Apr. 2015.
[24] H. Ito *et al.*, "A 2.3 pJ/bit frequency-stable impulse OOK transmitter powered directly by an RF energy harvesting circuit with −19.5 dBm sensitivity," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2014, pp. 13–16.

Mark Stoopman (GS'10–M'11) was born in Rotterdam, The Netherlands, in 1983. He received the M.Sc. and Ph.D. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2010 and 2016, respectively.

In 2015, he joined Catena Microelectronics, Delft, as an Analog/RF Design Engineer. His current research interests include RF energy harvesting, low-power wireless communication, antennas and ultralow-power IC design for biomedical applications.

Kathleen Philips (A'02–M'03) holds the Ph.D. degree in electrical engineering.

She is a Program Director with imec, Eindhoven, The Netherlands, and the Holst Centre, in the area of perceptive systems for the IoT. She has 20 years of experience in the domain of low-power mixed-signal, RF, and integrated system design. She started her career at Philips Research, The Netherlands, working on analog and mixed-signal circuits. She joined the Holst Centre/imec in 2007, where she is currently leading a program on ultra-low power wireless, processing and sensing systems. This is part of an open innovation collaboration, together with local and international industry. The research targets applications in the area of infrastructure and personcentric IoT systems with a focus on ultralow power communication and sensing.

Wouter A. Serdijn (M'98–SM'08–F'11) was born in Zoetermeer, The Netherlands, in 1966. He received the M.Sc. (*cum laude*) and Ph.D. degrees from the Delft University of Technology, Delft, The Netherlands, in 1989 and 1994, respectively.

He is currently a Full Professor with the Delft University of Technology, where he heads the Section Bioelectronics. His current research interests include integrated biomedical circuits and systems for biosignal conditioning and detection, neuroprosthetics, transcutaneous wireless communication, power management, and energy harvesting as applied in such as hearing instruments, cardiac pacemakers, cochlear implants, neurostimulators, portable, wearable, implantable, and injectable medical devices, and electroceuticals. He is a co-editor and a co-author of *Design of Efficient and Safe Neural Stimulators-a Multidisciplinary Approach* (Springer, 2016), *EMI-Resilient Amplifier Circuits* (Springer 2013), *Ultra Low-Power Biomedical Signal Processing: An Analog Wavelet Filter Approach For Pacemakers* (Springer, 2009), *Circuits and Systems for Future Generations of Wireless Communications* (Springer, 2009), *Power Aware Architecting for Data Dominated Applications* (Springer, 2007), *Adaptive Low-Power Circuits for Wireless Communications* (Springer, 2006), *Research Perspectives on Dynamic Translinear and Log-Domain Circuits* (Kluwer, 2000), *Dynamic Translinear and Log-Domain Circuits* (Kluwer, 1998), and *Low-Voltage Low-Power Analog Integrated Circuits* (Kluwer, 1995). He authored or co-authored 8 book chapters, holds 2 patents, and over 300 scientific publications and presentations. He teaches circuit theory, analog integrated circuit design, analog CMOS filter design, active implantable biomedical microsystems, and bioelectronics.

Dr. Serdijn is an IEEE Distinguished Lecturer and a Mentor of the IEEE. He was the recipient of the Electrical Engineering Best Teacher Award in 2001, 2004, and 2015. In 2016, he was the recipient of the IEEE Circuits and Systems Meritorious Service Award. He has served as the General Co-Chair for IEEE ISCAS 2015 and IEEE BioCAS 2013, the Technical Program Chair for IEEE BioCAS 2010 and IEEE ISCAS 2010, 2012, and 2014, as a Member of the Board of Governors of the IEEE Circuits and Systems Society from 2006 to 2011, the Chair of the Analog Signal Processing Technical Committee of the IEEE Circuits and Systems Society, a member of the Steering Committee of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS and as Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I: REGULAR PAPERS (2010–2011).