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A Level Shifter With Almost Full Immunity to Positive dv/dt for Buck Converters

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***Abstract*— High-frequency buck converters need a fast transition of switching nodes (high *dv/dt*). Such high *dv/dt*, especially the positive one, can cause malfunction of a conventional pulse-triggered active-coupled (PTAC) level shifter that is used to control the high-side NMOS switch. In this work, we first discuss the *dv/dt* immunity of conventional PTAC level shifters. Subsequently, we propose a new scheme to block the noise current during the *dv/dt* sequence, allowing an almost full immunity to the positive *dv/dt*. With this scheme, the maximum *dv/dt* is determined by how well the circuitry is protected from the overvoltage during the *dv/dt* sequence. We design a 20-V buck converter with this level shifter, fabricated in 180-nm BCD process. Experimental results show it works correctly under a 67-V/ns *dv/dt*.**

***Index Terms*— DC-DC converter, level shifter, buck converter, dv/dt immunity.**

I. Introduction

BUCK converter (Fig. 1) has a wide utilization in high-efficiency applications. Due to the high mobility, NMOS power transistors have a lower turn-on resistance than PMOS under the same chip area. Therefore, it is favorable to use an NMOS as the high-side switch (M_H). The gate driver of M_H is working in a floating-voltage (FV) domain (from $V_{SSH} = V_X$ to $V_{DDH} = V_X + V_{DR}$, where V_{DR} is the gate-drive voltage, while V_X is the switching node from ground to supply voltage V_{IN}). Bootstrap circuit, consisting of a diode and a capacitor C_{BST} [1], is widely used to generate V_{DDH} that is V_{DR} higher than V_X. To turn M_H on and off, we need a level shifter (LS) to convert the control signal S_H from a low-voltage domain (LV, from ground to the control supply voltage V_{DD}) to the S_{FV} in FV domain. The level shifter design can be challenging in high-speed applications, where the short transient time of V_X leads to a high slew rate (*dv/dt*). The *dv/dt* can be even higher in high-voltage applications. A high *dv/dt* may lead to malfunction of the level shifter, as well as the converter.

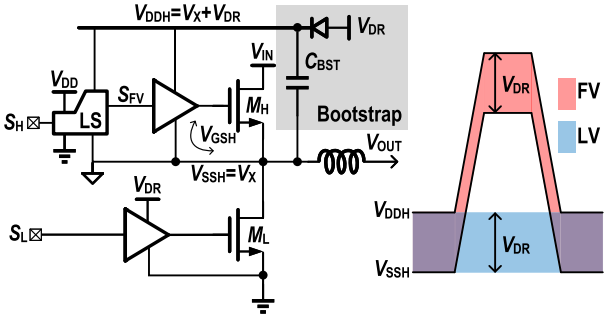

Fig. 1. Block diagram of a buck converter and voltage domains of its level shifter.

There are three main categories of level shifters: 1) capacitive-coupled [1], [2], [3], [4], 2) voltage-triggered active-coupled [5], [6], [7], [8], [9], [10], and 3) pulse-triggered active-coupled (PTAC) level shifters [11], [12], [13], [14], [15], [16], [17]. A capacitive-coupled level shifter exhibits small power consumption but needs high-voltage capacitors. A voltage-triggered active-coupled level shifter has a simple circuitry, while consumes a large power. By contrast, a PTAC level shifter has the advantages of both small power consumption and no high-voltage capacitor, which is more popular in high-voltage applications [15].

The PTAC level shifter always uses a differential topology, utilizing an output latch to obtain rail-to-rail output signals, achieving a small power consumption and propagation delay. However, the conventional PTAC level shifter has a high risk of output logic failure under a large common-mode noise current I_{NOISE} from a high positive *dv/dt* (V_X transitions from ground to V_{IN} in a short time), as explained in Section II. By contrast, a negative *dv/dt* (V_X transitions from V_{IN} to ground) has little harm on PTAC level shifter, as discussed in Section III-D. Therefore, most of the previous literatures investigated the topology of the PTAC level shifter that can resist a high positive *dv/dt*, a.k.a. to obtain a good

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TABLE I
THE *dv/dt* ISSUE OF CONVENTIONAL PTAC LEVEL SHIFTER

	Safety condition	Required transistor sizes
Signal phase	$I_{SIG} > I_{SIG,TH}$	Large M_{1A}, M_{1B}, and small M_{4A}, M_{4B}
Noise phase	$I_{NOISE} < I_{NOISE,TH}$	Small M_{1A}, M_{1B}, and large M_{4A}, M_{4B}

immunity to positive-*dv/dt*. For instance, [12] added shunt branches, and [14] added bypass transistors to reduce the I_{NOISE} within the *dv/dt* sequence. But their *dv/dt* immunity was improved with a higher circuit complexity, or an increased number of high-voltage MOSFETs. Reference [15] proposed a dual-interlock level shifter that desensitized the output stage, but increased the propagation delay. Furthermore, these designs may still malfunction under a very high *dv/dt*.

To address these issues and further improve the immunity to positive *dv/dt*, we propose a scheme that blocks the I_{NOISE} within the *dv/dt* sequence. This facilitates an almost full immunity, which means that in theory, the proposed level shifter functions correctly under an I_{NOISE} from infinitely large positive *dv/dt*. Its maximum allowable *dv/dt* is only determined by how well the protection diodes can protect the transistors from overstressing, as discussed in Section III-B. We organize this paper as follows: Section II reviews the previous PTAC level shifters and discusses their maximum *dv/dt* immunity. Section III presents the working principles and implementations of the proposed level shifter, and discusses its limitations. Section IV shows the simulation and measurement results, and a comparison with previous works. Section V draws the conclusions.

II. REVIEW OF PREVIOUS PTAC LEVEL SHIFTERS

A. Working Principles of the Conventional Level Shifter When Dv/Dt = 0

Fig. 2(a) shows the schematic of a conventional PTAC level shifter. The LV Pulse Generator outputs pulse V_{1A} and V_{1B} from the rising and falling edge of the input signal S_H, respectively. M_{1A} and M_{1B} are differential input high-voltage MOSFETs in LV domain, each with an output parasitic capacitance C_{P1} (to ground). Two inverters, M_{4A}, M_{5A} and M_{4B}, M_{5B} make up a latch. The outputs of the latch are V_{OA} and V_{OB}, with parasitic capacitance C_A and C_B (to $V_{SSH} = V_X$), respectively. Differential output buffers are used to ensure the same load capacitance of the two inverters. The output buffers generate a non-inverting output signal OUT_A and inverting signal OUT_B. Transistors M_{2A}, M_{3A}, M_{2B}, and M_{3B} (equal size) are current mirrors to copy the input currents from LV domain to FV domain.

We first review the working principles of this PTAC level shifter under a positive-edge input S_H, when $dv/dt = 0$. We define this period as signal phase. Fig. 2(a) includes the signal currents within the signal phase, and the transient waveforms are given in Fig. 2(c). It starts with V_{OA} = "0" and V_{OB} = "1". I_{CA} is the current charging C_A:

$$I_{CA} = I_{OA} - I_{4B} + I_{5B}, \tag{1}$$

where I_{OA}, I_{4B} and I_{5B} are current from M_{3A}, M_{4B} and M_{5B}, respectively. Note that we should ensure $I_{CA} > 0$ before the latch outputs flip completely in the signal phase, otherwise the latch will be locked in the state V_{OA} = "0" and V_{OB} = "1".

At S_H's rising edge t_1, V_{1A} turns on M_{1A}, outputting a current I_{SIG} which is mirrored to I_{OA} through the current mirror M_{2A}-M_{3A}. Most I_{OA} is injected to C_A at t_1, and V_{OA} increases. From t_1 to t_2, V_{DS} of M_{4B} increases due to the I_{CA} injection, and I_{4B} increases. V_{OB} almost has no change, and $I_{5B} = 0$. From t_2 to t_3, V_{OA} becomes sufficiently high to turn on M_{4A}, discharging C_B and decreasing V_{OB}. I_{OA} decreases because of an increasing V_{OA}, considering the channel length modulation effect of M_{3A}. Then I_{CA} is decreasing. I_{5B} is around 0. From t_3 to t_4, because of the V_{OB} decreasing, I_{5B} rises and I_{4B} falls, making I_{CA} raises again. This pulls V_{OA} up and V_{OB} down, and finally flips the outputs of the latch.

Clearly, I_{CA} achieves the minimum value at t_3, where M_{3A} works in saturation region due to the relatively low V_{OA}. Therefore, $I_{OA}(t_3)$ should well copy $I_{SIG}(t_3)$, $I_{OA}(t_3) = I_{SIG}(t_3)$. To make $I_{CA}(t_3) > 0$, we need to guarantee $I_{OA}(t_3) > I_{4B}(t_3)$ from equation (1), because $I_{5B}(t_3) \approx 0$. That is:

$$I_{SIG}(t_3) = I_{OA}(t_3) > I_{4B}(t_3) = I_{SIG,TH}, \tag{2}$$

where $I_{SIG,TH}$ is the threshold I_{SIG} to flip the latch, at t_3.

Clearly, to meet (2), we should choose large I_{SIG} (W_1) and small I_{4B} (W_4), where W_1 and W_4 are channel width of M_{1A} (and M_{1B}) and M_{4A} (and M_{4B}), respectively.

B. Dv/Dt Issue of the Conventional Level Shifter

Since the C_{BST} in Fig. 1 holds an almost constant voltage difference between V_{DDH} and V_X, $dV_{DDH}/dt = dv/dt$. As shown in Fig. 2(b), the parasitic capacitance C_{P1} on M_{1A} and M_{1B} generates common-mode I_{NOISE} within a *dv/dt* sequence:

$$I_{NOISE} = C_{P1} \cdot dv/dt. \tag{3}$$

Part of I_{NOISE} is mirrored to I_{OB} and I_{OA}, leading to possible false output of the latch. Hence we define the period of the *dv/dt* sequence as the noise phase.

Fig. 2(d) shows how different *dv/dt* magnitudes affect the output of the level shifter. Initial state is V_{OA} = "1" and V_{OB} = "0" at t_5, after the operation of the previous signal phase. When *dv/dt* is small, a small I_{OB} mirrored from I_{NOISE} pulls V_{OB} up to some extent, and the V_{OB} rise could pull V_{OA} down to a smaller value. But such a small change does not flip the output of the level shifter.

However, the I_{NOISE} from a large *dv/dt* can pull V_{OB} up greatly, and flip OUT_B at t_6. Subsequently, the OUT_B flipping can either maintain or flip back (as a glitch). Both glitch and flipping are harmful for buck converters.

To prevent the V_{OB} from crossing the threshold voltage at t_6, we should guarantee the C_B current $I_{CB}(t_6) < 0$. With M_{5A} turned off and M_{4A} turned on at t_6, we write:

$$I_{CB}(t_6) = I_{OB}(t_6) - I_{4A}(t_6) \approx I_{NOISE} - I_{4A}(t_6), \tag{4}$$

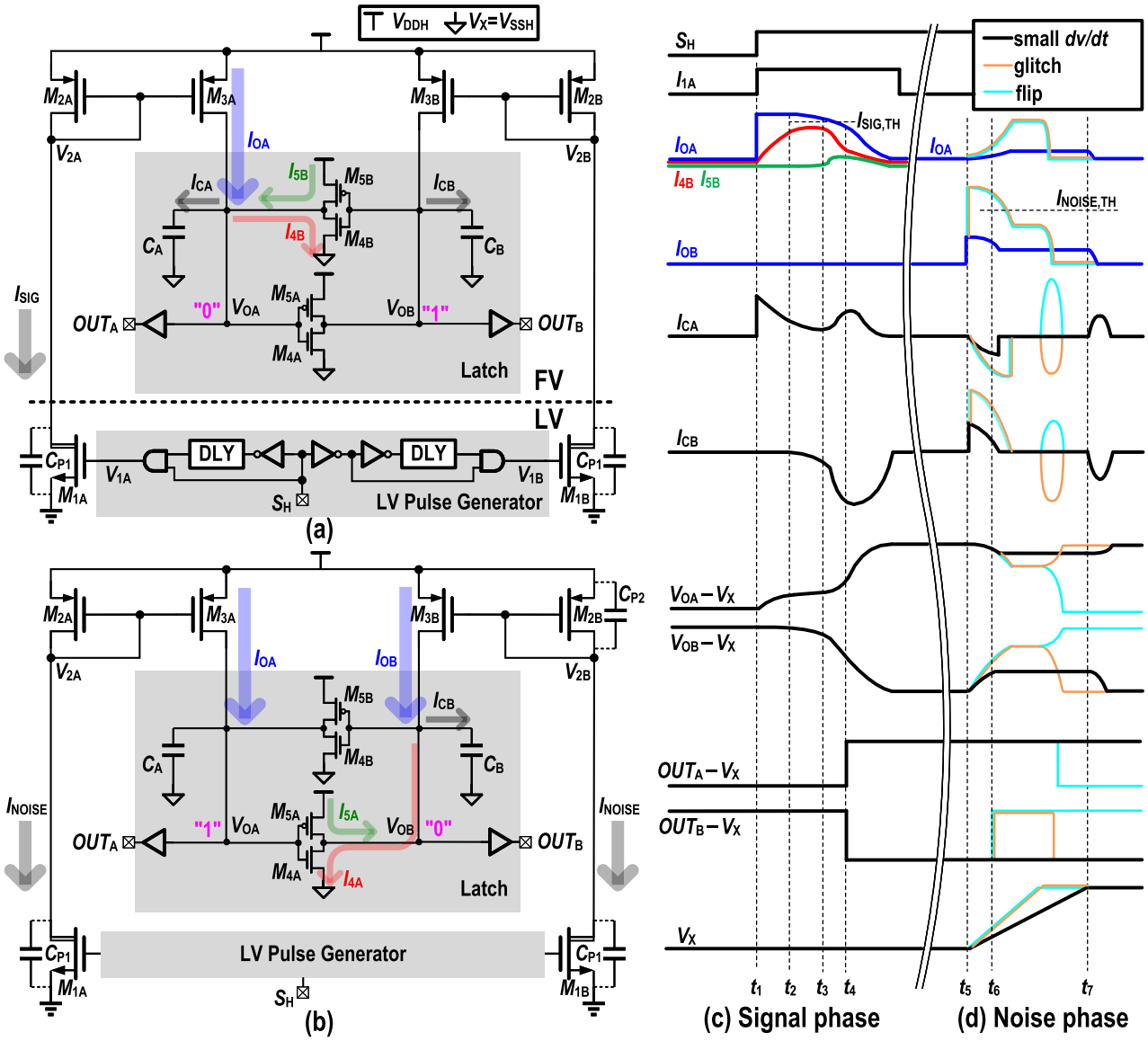

Fig. 2. (a) Schematic of a conventional PTAC level shifter and signal currents within the signal phase (from t_1 to t_4), (b) noise currents within noise phase (from t_5 to t_7), (c) transient waveforms with a positive-edge input signal, within the signal phase, and (d) transient waveforms within the noise phase.

where I_{4A} is the current of M_{4A}. Substitute I_{NOISE} with (3) and make (4) < 0, we have:

$$dv/dt < \frac{1}{C_{P1}} I_{4A}(t_6) = \frac{1}{C_{P1}} I_{NOISE,TH}, \tag{5}$$

where $I_{NOISE,TH}$ is the threshold value of I_{NOISE} to cause a false output of the level shifter.

Obviously, we could improve the *dv/dt* immunity by reducing C_{P1} or increasing I_{4A} (W_4), which means reducing the size of M_{1A} (and M_{1B}) and increasing the size of M_{4A} (and M_{4B}). However, both ways may contradict equation (2) for the signal phase. Thus, the *dv/dt* immunity of the conventional level shifter is limited.

Table I summarizes the *dv/dt* issue of the conventional PTAC level shifter. The safety condition in the signal phase requires large M_{1A}, M_{1B}, and small M_{4A}, M_{4B} sizes, while that in the noise phase needs small M_{1A}, M_{1B}, and large M_{4A}, M_{4B}. Clearly, the required transistor sizes of the two phases contradict each other.

Work from [12] improved the immunity to *dv/dt* with shunt branches, significantly reducing the currents I_{OA} and I_{OB} injected into the latch under a *dv/dt*. However, the improvement is limited, since the noise current is not completely removed. A possible malfunction could take place under a high *dv/dt*. Consequently, it is more attractive if a new topology can block I_{NOISE} completely and achieve a full immunity to *dv/dt*.

III. Working Principles and Implementations of the Proposed Design

A. Working Principles

Fig. 3 displays the high-side switch turning on waveforms of a buck converter in Fig. 1. Time interval t_1-t_2 is the rising delay of the level shifter. Interval t_2-t_3 is the delay between the rising edge of S_{FV} and V_{GSH} rising to its Miller Plateau

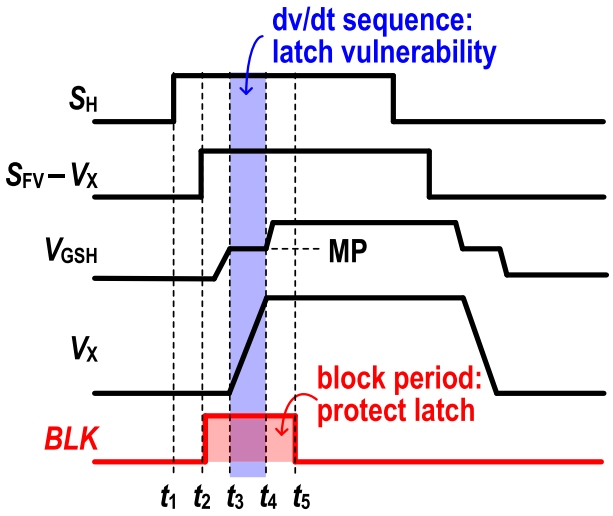

Fig. 3. Switching waveforms of a buck converter, and a possible way to obtain the full immunity to positive *dv/dt*.

(MP). After that, the *dv/dt* sequence occurs within t_3-t_4, where the triggered I_{NOISE} makes the level shifter vulnerable.

If we can completely block I_{NOISE} from t_3 to at least t_4 (with *BLK* signal), the level shifter output sees no common-mode noise current, and thus should resist an infinitely large *dv/dt*, (full immunity to positive *dv/dt*). Therefore, the rising edge of *BLK* should be generated after the rising edge of S_{FV} (t_2), and before the *dv/dt* sequence (t_3). This should be implementable, since interval t_2-t_3 usually lasts several nano-seconds, consisting of the delay between S_{FV} and V_{GSH}, and the time interval from V_{GSH} rising to its MP. Subsequently, *BLK* should be ended shortly after the *dv/dt* sequence (t_5), enabling I_{SIG} again.

Fig. 4 (a) presents the schematic of the proposed level shifter, based on the work from [12]. The shunt branches (M_{P2A}, M_{N2A}, M_{N3A}, M_{P2B}, M_{N2B}, and M_{N3B}) are used to equalize the delay of the rising and falling edges. Resistors R_{1A}, R_{1B}, R_{2A}, and R_{2B} prevent the current mirror misconducting during non-working periods. Furthermore, we add the BLK generator (consisting of a delay chain DLY_1, an inverter and an AND gate), blocking transistors (M_{P3A}, M_{P5A}, M_{P3B}, and M_{P5B}), and diode D_{1A} and D_{1B} for overvoltage protection [15]. We implement DLY_1 with an inverter chain.

Fig. 4 (b) explains the working principles of the proposed design. The BLK generator detects the positive edge of OUT_A, and generates a pulse signal *BLK*. The *BLK* turns off the M_{P3A}, M_{P5A}, M_{P3B}, and M_{P5B} synchronously, nulling the current I_{OA} and I_{OB}, or blocking the noise current from the parasitic capacitors of HV MOSFETs M_{N1A} and M_{N1B}. Therefore, the *dv/dt* sequence does not cause a malfunction. The waveforms without the block period are also given in Fig. 4 (b) for comparison.

We control the pulse width of *BLK* by carefully designing the delay of delay chain DLY_1. Its pulse width should be determined by the working frequency and load range of the buck converter. If the buck converter works in a higher frequency, we can design a narrower pulse width for *BLK*.

Note that a very large *dv/dt* still causes some V_{OA} and V_{OB} variations. This is because the capacitance between V_{OA}, V_{OB} and ground (C_{PA}, C_{PB} in Fig. 4 (a)) should be charged by C_A and C_B, within the positive *dv/dt* sequence. But due to the small value of C_{PA}, C_{PB}, the variations would be too small to flip the latch.

B. Maximum Dv/Dt Immunity of the Proposed Level Shifter

Although blocking I_{NOISE} can theoretically protect the latch from an infinitely large *dv/dt* sequence, such *dv/dt* may still be unsafe for the proposed level shifter. As shown in Fig. 5 (a), we use the R_{P1A} and R_{N1A} to represent the R_{DS} of M_{P1A} and M_{N1A}, respectively. The DC voltage of V_{2A} is V_{DDH} over the resistive divider of R_{P1A} and R_{N1A}. In the steady state, M_{N1A} is turned off, and hence R_{N1A} is large and V_{2A} is close to V_{DDH}. When a large *dv/dt* occurs, the large I_{NOISE} flows through the low-impedance capacitive divider path (C_{P2} and C_{P1}). Charging C_{P2} with the I_{NOISE} leads to an instantaneous increase in V_{SD} of M_{P1A} ($= V_{DDH} - V_{2A}$), as shown in Fig. 5 (a) and (c). The peak V_{SD} value at a large *dv/dt* is approximately equal to the V_{DDH} step ($= V_{IN}$) over the capacitive divider:

$$V_{SD,PEAK} \propto \frac{C_{P1}}{C_{P1} + C_{P2}} V_{IN}. \tag{6}$$

Once V_{IN} is not high and C_{P2} is large, the instantaneous V_{2A} (or V_{2B}) does not overstress M_{P1A}, M_{P2A} and M_{P4A} (nor M_{P1B}, M_{P2B}, and M_{P4B}). In this sense, the level shifter has "truly" full immunity to positive *dv/dt*. Nevertheless, if V_{IN} is high or C_{P2} is relatively small, a very large I_{NOISE} can instantly charge C_{P2} and then overstress the transistors (the "V_{2A} no D_{1A}" case as shown in Fig. 5 (c)).

To address this, diodes D_{1A} and D_{1B} are added to clamp V_{2A} and V_{2B} to V_X, and thus circumvent the overstress issue, as shown in Fig. 5 (b). In this scenario, the diode conducts part of I_{NOISE}, reducing the peak $V_{SD,PEAK}$ from equation (6). However, it is possible that the diode current I_D is instantaneously smaller than I_{NOISE}, making the diodes clamp V_{2A} to an instantaneously lower value that is still risky of overvoltage (the "V_{2A} small D_{1A}" case). Therefore, we should choose a large diode that can conduct sufficient I_{NOISE} during a *dv/dt* sequence (the "V_{2A} large D_{1A}" case).

In sum, the maximum *dv/dt* immunity of the proposed design is determined by protection diodes. With sufficiently large protection diodes, the proposed scheme can theoretically resist an infinitely large *dv/dt*, which is significantly improved from the previous works. We regard it as "almost" full immunity to positive *dv/dt*.

C. Possible Drawback and Solution

The possible drawback of this scheme is that the I_{SIG} may be blocked by the *BLK* signal as well. This prohibits the S_H signal transmission to the high-side switch through the level shifter during the block period (*BLK* enable in Fig. 3).

Fortunately, for most buck converters, the S_H transmission during the block period is not needed. To our best knowledge, the possible exception is the design that precisely controls

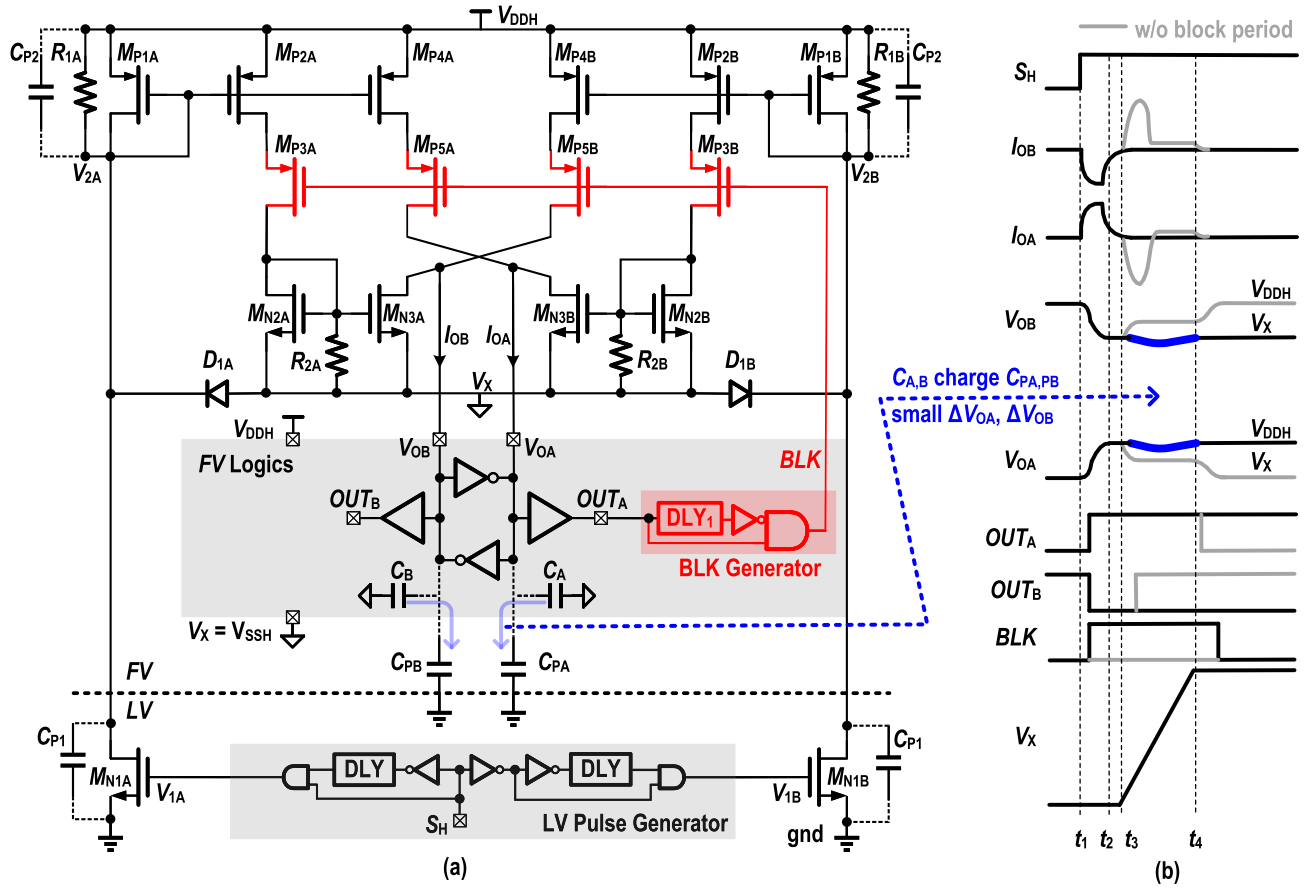

Fig. 4. (a) Schematic and (b) transient waveforms of the proposed level shifter.

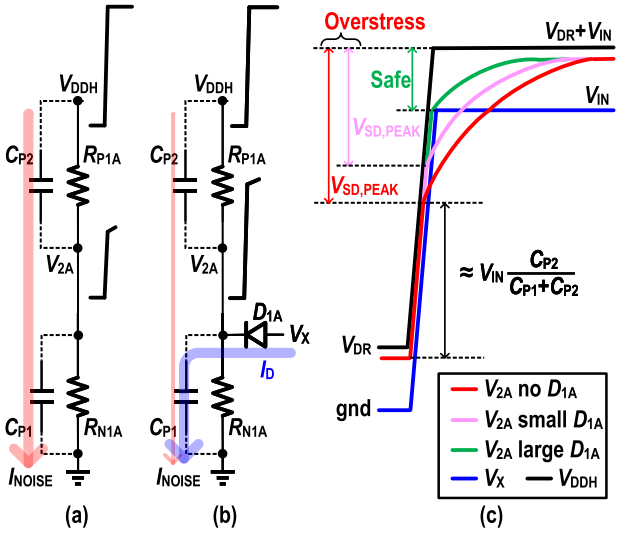

Fig. 5. I_{NOISE} conduction path (a) without and (b) with the protection diodes. Only show left-hand branch of the level shifter for simplicity. (c) V_{2A} waveforms within a *dv/dt* sequence.

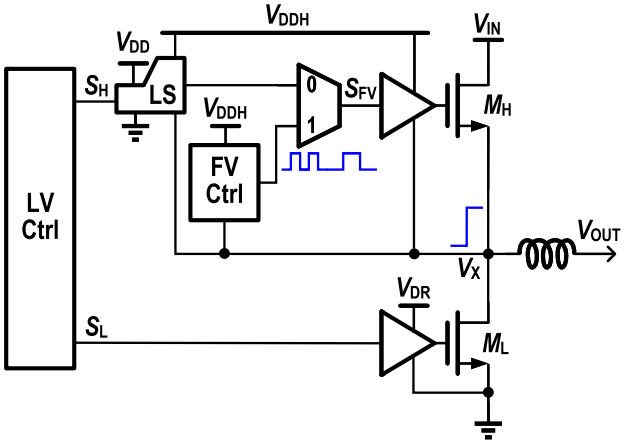

Fig. 6. A possible solution to control M_H during a *dv/dt* sequence, compatible to the proposed scheme.

the *dv/dt* value, such as in [18], where multiple S_H signals are transmitted during a *dv/dt* sequence. However, the precise *dv/dt* control schemes usually have stringent requirements on the delay of the transmission path. This makes the close-loop *dv/dt* control between the FV and LV domains not acceptable. Therefore, a possible and reasonable alternate is to implement the closed-loop control in FV, without using the level shifter, as shown in Fig. 6 [19], [20]. This removes the delay of the level shifter. Clearly, this scheme is fully compatible with the proposed level shifter.

D. Immunity to Negative Dv/Dt

A negative *dv/dt* triggers a negative I_{NOISE} that is conducted to V_{DDH} through the body diode of M_{P1A} and M_{P1B}. Therefore, the I_{NOISE} is not mirrored to the latch. That is why converters usually have a much higher tolerance to a negative *dv/dt*.

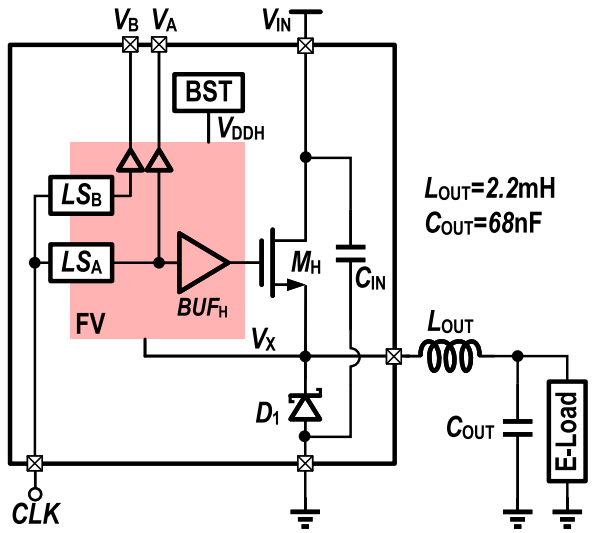

Fig. 7. Block diagram of the DUT.

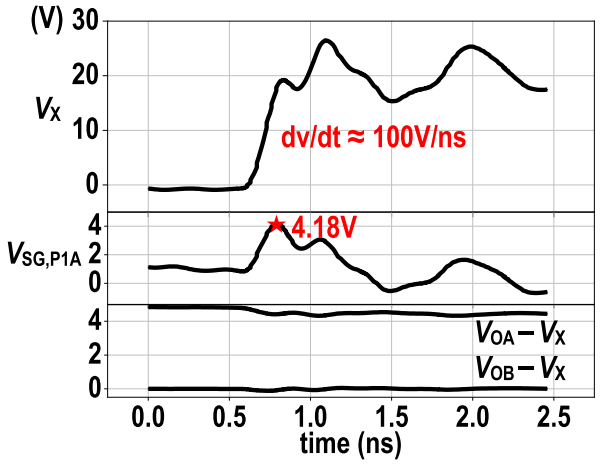

Fig. 8. Post-layout simulation results when $dv/dt \approx$ 100V/ns.

In fact, too large negative dv/dt could cause reliability issue as well. With a very large negative I_{NOISE}, V_{2A} and V_{2B} are pulled higher to conduct more I_{NOISE}. This may overstress D_{1A} and D_{1B}. Additional protection circuits should be added.

E. Implementations

Fig. 7 is the block diagram of the design under test (DUT). An asynchronous buck converter generates the dv/dt. The switching frequency is 500KHz. M_H is the power switch, D_1 is the asynchronous diode. The M_H, D_1, and bootstrap (BST) block are integrated. As widely used in buck converter, we integrate an on-chip input capacitor C_{IN} to provide a low-impedance AC path from V_{IN} to ground, filtering out the high-frequency glitches on V_{IN}. The value of C_{IN} implemented is 42pF, occupying a silicon area of 0.112mm^2. We integrate the proposed level shifter (LS_A), and also a level shifter (LS_B) using the topology in [12], as a baseline design for comparison. V_A and V_B are their outputs, respectively. We observe the V_A and V_B after on-chip buffers. Only the LS_A is used to control M_H, in case the malfunction of LS_B under a high dv/dt.

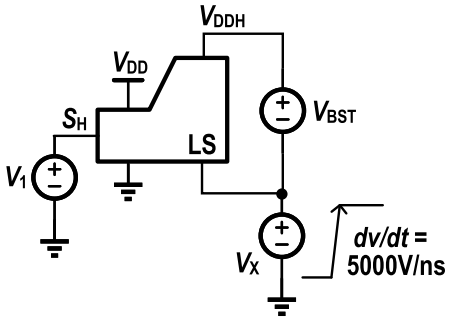

Fig. 9. Testbench of the proposed level shifter under dv/dt = 5000V/ns.

To measure the robustness of the level shifters under different dv/dt, we predesign two dv/dts.

To verify the dv/dt immunity of the proposed scheme, it is desirable to design the DUT buck converter with a high dv/dt. However, the high dv/dt design is challenging. From [21], the dv/dt of a buck converter is:

$$dv/dt = \frac{g_{FS}(V_{GS} - V_{MP})}{C_{OSS\_HS} + C_{OSS\_LS}}, \tag{7}$$

where g_{FS} is the transconductance of the M_H, V_{MP} is the beginning voltage of the MP, C_{OSS_HS} and C_{OSS_LS} are the output capacitances of M_H and D_1, and V_{GS} is the gate-source voltage of the M_H in the Miller Plateau calculated as:

$$\frac{dV_{GS}}{dt} = \frac{V_{DR} - V_{GS}}{R_G C_{ISS\_HS}} - \frac{g_{FS} C_{RSS\_HS}(V_{GS} - V_{MP})}{C_{ISS\_HS}(C_{OSS\_HS} + C_{OSS\_LS})}, \tag{8}$$

where R_G is the output resistance of the gate drive buffer BUF_H, and C_{RSS_HS} and C_{ISS_HS} are the reverse transfer and input capacitance of M_H.

Equation (7) and (8) indicate that $dv/dt = 0$ at the beginning of the MP, and increases to the maximum value after some time. Increasing the input voltage V_{IN} may allow a larger dv/dt, such as in [15], by extending the time duration of the MP.

However, the DUT is designed with devices only sustaining 20-V V_{IN} in this work. Therefore, we should increase dv/dt by reducing C_{OSS_HS} and C_{OSS_LS} as indicated in (7). Hence, we use a Schottky diode D_1 as the low-side switch, which has a smaller C_{OSS_LS} than that of a high-voltage MOSFET that conducts the same current. Meanwhile, we choose a small M_H size to minimize the C_{OSS_HS}.

Finally, we control the slew rate of V_{GS} for the maximum dv/dt, by using a strong BUF_H. However, even though we intentionally increase the dv/dt, the maximum value in post-layout simulation is only around 100V/ns, with parasitics included.

IV. Simulation and Measurement Results

Fig. 8 shows the post-layout simulation results under the implemented 100V/ns dv/dt, from DUT in Fig. 7. Under the protection of D_{1A} and D_{1B}, the peak $V_{SG,P1A}$ is 4.18V. Voltage $V_{OA} - V_X$ and $V_{OB} - V_X$ have small fluctuations. But the fluctuations do not cause a false output.

However, the dv/dt from an implemented buck converter is not high enough to verify the claimed "almost full immunity" to positive dv/dt. Therefore, we use another testbench as

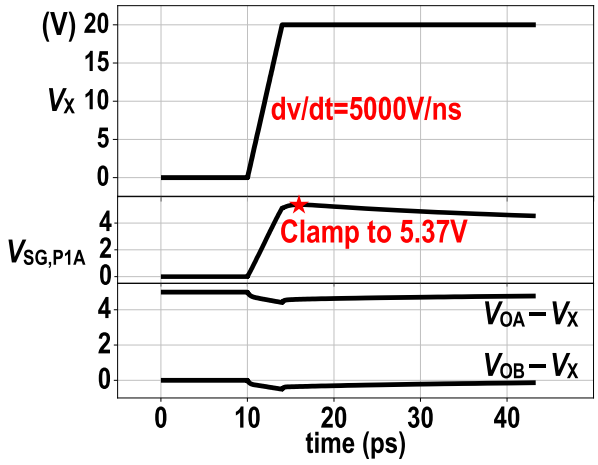

Fig. 10. Post-layout simulation results when dv/dt = 5000V/ns.

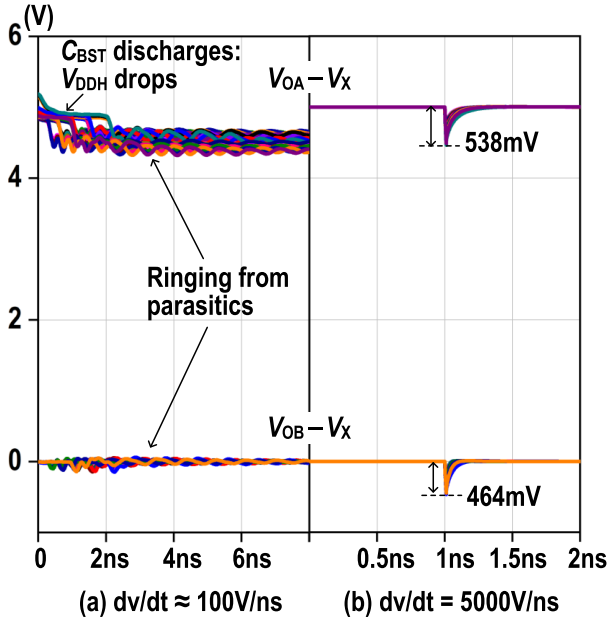

Fig. 11. Post-layout simulation results of $V_{OA}-V_X$ and $V_{OB}-V_X$ under different PVT conditions when (a) $dv/dt \approx$ 100V/ns (TB is Fig. 7), and (b) dv/dt = 5000V/ns (TB is Fig. 9).

shown in Fig. 9. The level shifter input S_H is connected to a DC voltage, while the bootstrap capacitor is replaced by a DC voltage source V_{BST}. We use an ideal voltage pulse signal V_X with 5000-V/ns slew rate (rise to 20V within 4ps). Fig. 10 shows the post-layout simulation results. Like in the 100V/ns-dv/dt scenario, the output logics are correct under the 5000-V/ns dv/dt, while the protection circuits clamp the peak $V_{SG,P1A}$ within the 5.5V maximum V_{SG} voltage.

Fig. 11 verifies the proposed design under different PVT conditions, where the TT, SS, FF corners, −40°C, 27°C and 105°C temperatures, 10V, 15V and 20V V_{IN} are included. Fig. 11 (a) uses the testbench (TB) in Fig. 7, while Fig. 11 (b) uses the TB in Fig. 9. As observed in Fig. 11 (a), under a 100-V/ns dv/dt, $V_{OA}-V_X$ decreases because of the V_{DDH} drop from the C_{BST} discharging. And $V_{OA}-V_X$ and $V_{OB}-V_X$ show ringings due to the parasitics included in DUT. Cleary, the dv/dt does not malfunction the level shifter. From Fig. 11 (b), the level shifter outputs have around 500-mV undershoot under

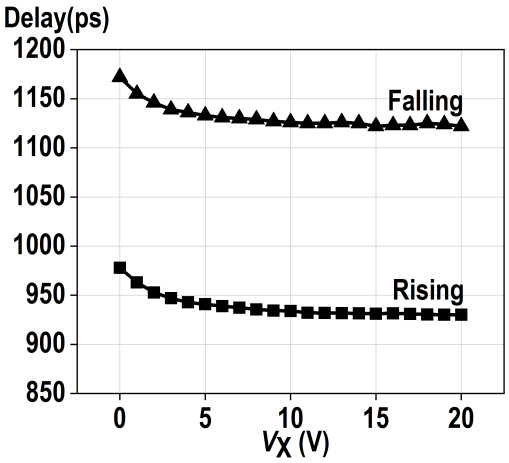

Fig. 12. Simulated delay of the proposed level shifter of rising edge input and falling edge input.

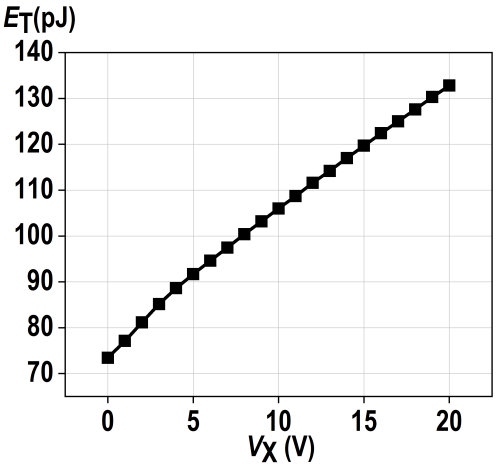

Fig. 13. Simulated energy consumption of the proposed level shifter.

the 5000-V/ns dv/dt, as discussed in Fig. 4. But the level shifter output is functionally correct.

Fig. 12 shows the post-layout simulation results of the delay of the level shifter. Delay of both rising and falling edges are around 1ns. The variation of the delay from 0 to 20V V_X is small. Although we insert couples of switches to the signal propagation paths to block the I_{NOISE} during the dv/dt sequence, the delay only increases slightly, and is comparable to the conventional level shifters.

Fig. 13 shows the post-layout simulation results of energy consumption in one transition (E_T). Compared to conventional level shifters, the additional power loss of the proposed design mainly comes from DLY_1. This power loss is around 16% as shown in the power loss breakdown in Fig. 14, when V_{IN} = 20V. Such power loss can be further reduced by using low-power delay chain design.

Fig. 15 (a) shows the post-layout simulation results of the delay between the start time of dv/dt (t_3 in Fig. 3), and the rising edges of BLK ($t_{BLK,RISE}$), under different corners. As seen, in all corners simulated, the BLK rising edge takes place at least 1ns before t_3. Fig. 15 (b) shows the simulated BLK pulse width, which covers the whole dv/dt sequence without blocking I_{SIG} too long. These verify the robustness of the BLK generator.

TABLE II
COMPARISON WITH PREVIOUS WORKS

	Year	Process(μm)	Area(mm^2)	V_{IN}(V)	Delay(ns)	E_T(pJ)	Sim. *dv/dt*(V/ns)	Meas. *dv/dt*(V/ns)
[1]	2015	0.5	N/A	40	2	160	40	N/A
[12]	2016	0.18	0.005	20	0.37	27.6	30	N/A
[2]	2018	0.18	0.00735	50	1.45	4.1	100	6
[22]	2018	0.5	N/A	80	1.618	N/A	50	N/A
[13]	2019	0.18	0.018	50	0.53	30.3	200	N/A
[3]	2021	0.18	0.0096	200	0.67	8.1	200	N/A
[4]	2023	0.5	0.051	50	1.26	27.3	200	56
This work (baseline)	2023	0.18	0.0045	20	1.02	105	8	<15
This work (proposed)			0.0094	20	1.17	133	>5000	67

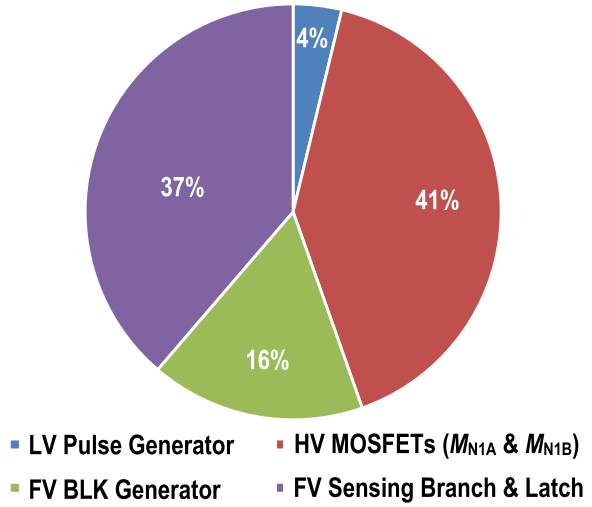

Fig. 14. Power loss breakdown of the proposed level shifter.

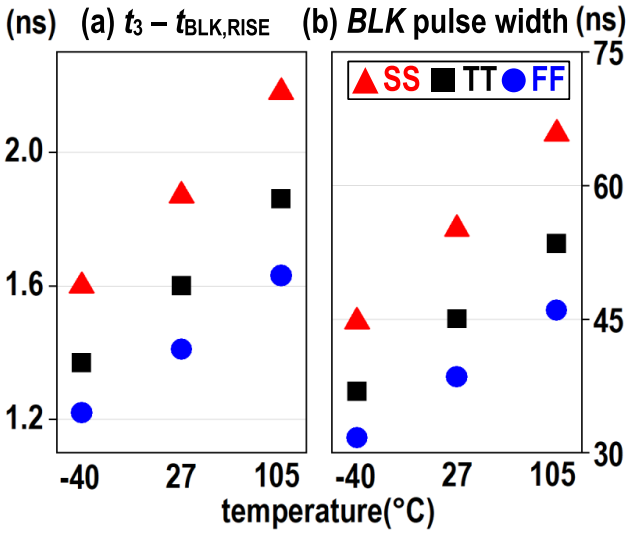

Fig. 15. Post-layout simulation of *BLK* signal timings under different corners: (a) delay between the *dv/dt* sequence and the rising edge of *BLK* ($t_{BLK,RISE}$), and (b) *BLK* pulse width.

We used a 0.18-μm Bipolar-CMOS-DMOS(BCD) process to fabricate the chip, and the maximum input voltage of the DUT buck converter is 20V. Fig. 16 shows the photo of the PCB, and the micrograph of the chip. We used chip-on-board (COB) packaging to connect the chip and PCB. The silicon area of LS_A and LS_B are around 9400μm^2 and 4500μm^2,

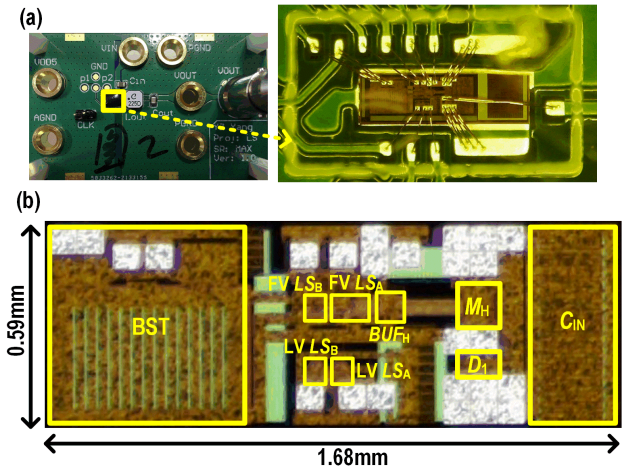

Fig. 16. (a) PCB photos, and (b) chip micrograph.

respectively. The additional area of LS_A comes from the BLK generator.

To capture the high frequency signals, we use an oscilloscope Keysight DSO-X 6004A (6GHz), an active differential probe Keysight 1134A (7GHz) and an attenuator Keysight 2880A (20dB). They can detect signal change in several hundreds of picoseconds.

Fig. 17 shows the measured waveforms of the buck converters with the proposed and baseline level shifter. We calculate the *dv/dt* value from the V_X waveform, using the calculator of the oscilloscope. The achieved maximum *dv/dt* is 67V/ns, lower than the simulated result. As observed, the proposed level shifter generates the correct output when the *dv/dt* is both 67V/ns and 15V/ns. By contrast, the baseline circuit outputs incorrectly even when $dv/dt = 15$V/ns. We observe ringing on V_A and V_B within the *dv/dt* sequence. This stems from the resonance of V_A (or V_B) output parasitic inductance and the C_{BST}. But we tell that the LS_A output is correct, otherwise the incorrect V_X flipping should be observed.

Table II compares the proposed design with previous works and the baseline design. With a comparable silicon area, power consumption, and propagation delay, the proposed design achieves both the highest simulated and measured immunity to positive *dv/dt*. The proposed I_{NOISE} blocking scheme should achieve an even higher measured *dv/dt* if we implement the converter with a high-voltage process.

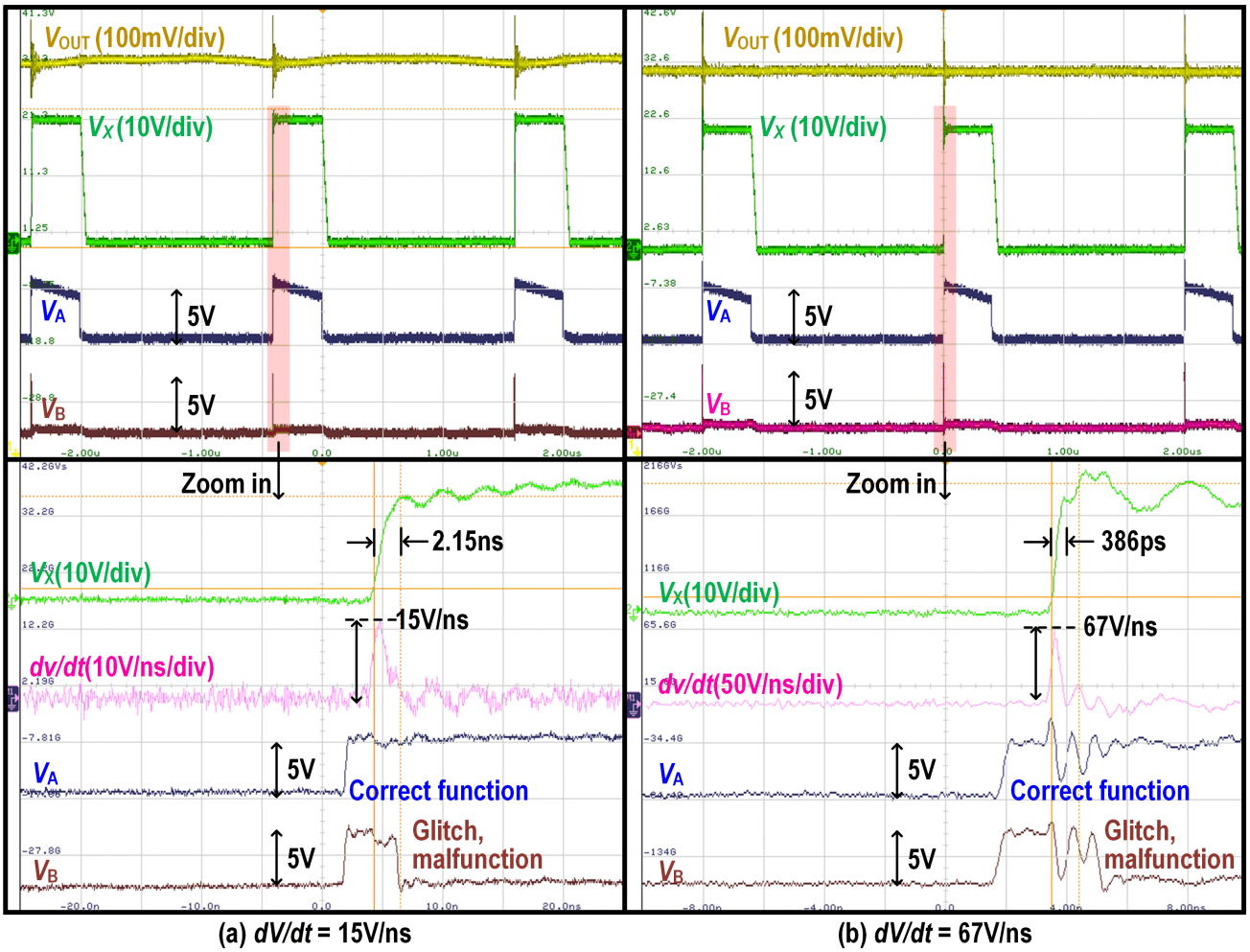

Fig. 17. Measured steady-state waveforms (a) with a 15V/ns, and (b) a 67V/ns *dv/dt*.

V. Conclusion

This article presented a PTAC-based level shifter that blocked the common-mode noise current during the positive *dv/dt* sequence. This achieved an almost full immunity to positive *dv/dt*, with the maximum *dv/dt* determined by how well the diodes can protect the transistors from overstressing. This scheme is compatible with a buck converter. The simulation results confirmed at least an immunity to 5000-V/ns *dv/dt*, while the silicon results exhibited 67V/ns.

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