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SCALING ASPECTS OF SILICON SPIN QUBITS

SCALING ASPECTS OF SILICON SPIN QUBITS

Proefschrift

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I Have a Dream

Martin Luther King Jr.

CONTENTS

SUMMARY

To harness the potential of quantum mechanics for quantum computation applications, one of the main challenges is to scale up the number of qubits. The work presented in this dissertation is concerned with several aspects that are relevant in the quest of scaling up quantum computing systems based on spin qubits in silicon. Few-qubit experiments are maturing quickly, but simultaneously the lacuna between them and large-scale quantum computers is filled with a combination of science and engineering challenges. The challenges that are addressed in this dissertation are reliable and reproducible sample fabrication, qubit resilience to temperature, spatial correlations in the noise affecting the qubits, and co-integration of qubits with classical control electronics.

I start with describing the development of an integration scheme for silicon spin qubits in an academic cleanroom environment, as several research groups have demonstrated over the last years. This has allowed them to successfully fabricate and operate silicon spin qubit devices. The development of such a scheme is crucial for the fabrication of proof-of-principle devices, and the testing of several design variations for more and more complex qubit devices, before transferring the optimal designs to industrial foundries that are generally less flexible. Moreover, it is essential for performing paramount few-qubit experiments in the near term. The developed scheme has been successfully implemented in the next chapter of this thesis.

In the first experiment, we investigate the effect of temperature on the spin lifetime, as a first step towards higher temperature operation of silicon spin qubits. Spin qubit operation at elevated temperatures will be required to allow for co-integration of qubits with classical control electronics on a single chip, since the heat load associated with this electronics will be too much to deal with at the current qubit operation temperature of ~10 mK. At a temperature of ~1–4 K, significantly more cooling power is available (see for example CERN's Large Hadron Collider). Such co-integration would alleviate the interconnect bottleneck and facilitate the implementation of local control in large-scale devices. We find only a modest temperature dependence and measure a spin relaxation time of 2.8 ms at 1.1 K (still much longer than the record spin dephasing time measured in such a system). In addition, we present a theoretical model and use it in combination with our experimentally obtained parameters to demonstrate that the spin relaxation time can be enhanced by low magnetic field operation and by employing high-valley-splitting devices. Together with more recent work, this experiment demonstrates no fundamental limitations to prevent high-temperature operation of silicon spin qubits. Simultaneously, bringing classical control electronics to lower temperatures also is an active research area.

The second experiment uses maximally entangled Bell states of two qubits to study spatial correlations in the noise acting on those two qubits. Spatial correlations in qubit errors hinder quantum error corrections schemes that will be required for fault-tolerant large-scale quantum computers, as these schemes are commonly derived under the as-

sumption of negligible correlations in qubit errors. Therefore, it is important to know to what extent the noise causing these errors is correlated. We find only modest spatial correlations in the noise and gain insight in their origin. The data is in accordance with decoherence being dominated by a combination of nuclear spins and multiple distant charge fluctuators coupling asymmetrically to the two qubits. We recommend to perform similar experiments in isotopically purified silicon to eliminate the effect of nuclear spins and in isolation study spatial correlations in charge noise. Furthermore, our insights show how correlations can be either maximized or minimized through qubit device design. For these reasons, the prospects for the development and implementation of quantum error correction schemes in fault-tolerant large-scale quantum computers are promising.

Finally, after having studied several aspects that are relevant to determine the suitability of silicon spin qubits for large-scale quantum computation in the preceding experiments, we propose a concrete physical implementation of co-integrated spin qubits with classical control electronics in a sparse spin qubit array. While the community usually claims compatibility of silicon spin qubits with conventional CMOS fabrication, existing proposals make assumptions that remain to be validated. Implementing quantum error correction protocols in a sparse array has been studied, but the description of a physical implementation was largely missing. The sparseness of the array allows for integration of local control electronics, as shown to be promising earlier in this thesis. Specifically, we propose to implement sample-and-hold circuits alongside the qubit circuitry that would allow to offset inhomogeneity in the qubit array. This enables individual local control and shared global control, resulting in an efficient line scaling. The scalable unit cell design fits 2^{20} ($\approx 10^6$) qubits in $\sim$150 mm^2. We assess the feasibility of the proposed scheme, as well as its physical implementation and the associated footprint, line scaling and interconnect density.

Jelmer Boter

SAMENVATTING

Eén van de voornaamste uitdagingen bij het benutten van het potentieel van quantummechanica voor quantumcomputertoepassingen is het vergroten van het aantal qubits. Het werk in dit proefschrift richt zich op verschillende aspecten die relevant zijn voor de zoektocht naar het opschalen van quantumcomputers gebaseerd op spinqubits in silicium. Experimenten met enkele qubits worden snel complexer, maar tegelijkertijd bevindt zich een combinatie van wetenschappelijke en technische uitdagingen in de leemte tussen deze experimenten en quantumcomputers op grote schaal. De uitdagingen die in dit proefschrift behandeld worden, zijn betrouwbare en reproduceerbare qubitfabricage, temperatuurbestendigheid van qubits, plaatsafhankelijke correlaties in de ruis die qubits beïnvloedt, en het samenbrengen van qubits met aansturingselektronica.

Ik begin met het beschrijven van de ontwikkeling van een fabricagemethode voor spinqubits in silicium in een academische cleanroomomgeving, zoals meerdere onderzoeksgroepen in de afgelopen jaren hebben laten zien. Dit heeft hen in staat gesteld om succesvol siliciumspinqubits te vervaardigen en aan te sturen. Het ontwikkelen van een dergelijke methode is cruciaal voor het vervaardigen en aansturen van *devices* waarmee de basisprincipes getest kunnen worden, en voor het testen van verschillende ontwerpvarianten voor complexere *devices*, voordat de optimale ontwerpen worden overgebracht naar de doorgaans minder flexibele industriële fabricagefaciliteiten. Tevens is dit noodzakelijk voor het uitvoeren van essentiële enkele-qubitexperimenten op de kortere termijn. De ontwikkelde fabricagemethode is succesvol toegepast in het volgende hoofdstuk van dit proefschrift.

In het eerste experiment bestuderen we het effect van temperatuur op de spinlevensduur, als een eerste stap in de richting van het opereren van spinqubits in silicium bij hogere temperaturen. Hogeretemperatuuroperatie van spinqubits zal noodzakelijk zijn om het samenbrengen van qubits met klassieke aansturingselektronica mogelijk te maken, aangezien de dissipatie veroorzaakt door deze elektronica te groot is om mee om te gaan op de huidige qubitoperatietemperatuur van zo'n ~10 mK. Bij een temperatuur van ~1–4 K is significant meer koelvermogen beschikbaar (zie bijvoorbeeld de Large Hadron Collinder van CERN). Dergelijke integratie zou de *interconnect bottleneck* verlichten en zou het implementeren van lokale controle in *devices* met vele qubits faciliteren. We vinden een beperkte temperatuurafhankelijkheid en meten een spinrelaxatietijd van 2.8 ms bij 1.1 K (nog steeds veel langer dan het record voor de spinfasecoherentietijd gemeten in dergelijke systemen). Tevens presenteren we een theoretisch model en gebruiken dit in combinatie met onze experimenteel verkregen parameters om te demonstreren dat de spinrelaxatietijd verlengd kan worden door te opereren bij lage magneetvelden en door gebruik te maken van *devices* met een grote valleisplitting. Dit experiment toont, samen met recenter werk, aan dat er geen fundamentele beperkingen zijn die hogeretemperatuuroperatie van siliciumspinqubits in de weg staan. Tegelijkertijd is het een actief onderzoeksgebied om klassieke elektronica naar lagere temperaturen te brengen.

Het tweede experiment maakt gebruik van maximaal verstrengelde Bell-toestanden van twee quantumbits voor het bestuderen van plaatsafhankelijke correlaties in de ruis werkend op deze quantumbits. Plaatsafhankelijke correlaties in qubitfouten belemmeren quantumfoutcorrectieprotocollen die noodzakelijk zullen zijn voor foutbestendige quantumcomputers op grote schaal, omdat deze protocollen in het algemeen zijn ontwikkeld onder de aanname van verwaarloosbare correlaties in qubitfouten. Het is daarom van belang om inzicht te krijgen in de mate waarin de ruis die deze fouten veroorzaakt gecorreleerd is. We meten slechts beperkte plaatsafhankelijke correlaties in de ruis en verkrijgen inzicht in de oorzaken daarvan. De data zijn in overeenstemming met decoherentie die met name wordt veroorzaakt door een combinatie van kernspins en meerdere ladingsfluctuatoren op enige afstand van de quantumbits die asymmetrisch koppelen met de twee quantumbits. We adviseren om vergelijkbare experimenten uit te voeren in isotopisch verrijkt silicium om het effect van kernspins uit te sluiten en zo plaatsafhankelijke correlaties in ladingsruis afzonderlijk te bestuderen. Tevens laten onze inzichten zien hoe correlaties gemaximaliseerd of geminimaliseerd kunnen worden door middel van het fysieke qubitontwerp. Vandaar dat de vooruitzichten voor de ontwikkeling en implementatie van quantumfoutcorrectieprotocollen in foutbestendige groteschaalquantumcomputers veelbelovend zijn.

Nadat we in de voorgaande experimenten verschillende aspecten hebben bestudeerd die van belang zijn bij het vaststellen van de geschiktheid van siliciumspinqubits voor de toepassing in groteschaalquantumcomputers, komen we ten slotte met een voorstel voor een concrete fysieke implementatie van spinqubits geïntegreerd met klassieke aansturingselektronica in een spinqubitraster met dunne qubitbezetting. Hoewel de gemeenschap doorgaans claimt dat siliciumspinqubits verenigbaar zijn met conventionele CMOS-fabricage, doen bestaande voorstellen aannames die nog gevalideerd moeten worden. Het implementeren van quantumfoutcorrectie in een dunbezet spinqubitraster is onderzocht, maar de beschrijving van een fysieke implementatie ontbrak grotendeels. Dat het raster dunbezet is, maakt het mogelijk om lokale aansturingselektronica te integreren, waarvan eerder in dit proefschrift is aangetoond dat dit veelbelovend is. Concreet stellen we voor om *sample-and-hold*-circuits, die het mogelijk maken om inhomogeniteit in het raster te compenseren, te implementeren naast de qubitcircuits. Dit maakt individuele lokale controle en gedeelde rasterbrede controle mogelijk, wat resulteert in een efficiënte schaling van het aantal controledraden. Met het schaalbare eenheidscelontwerp beslaan 2^{20} ($\approx 10^6$) qubits ~150 mm^2. We beoordelen de haalbaarheid van het voorstel, met inbegrip van de fysieke implementatie en het bijbehorende oppervlak, de bijbehorende schaling van het aantal draden en verbindingsdichtheid.

Jelmer Boter

1

INTRODUCTION

I think I can safely say that nobody understands quantum mechanics.

Richard P. Feynman

The world around us is governed by the theory of quantum mechanics instead of well-known classical physics. Everyday life does not usually reveal the intriguing properties of the theory that was developed more than a century ago, but at the fundamental level everything around us is quantum, and we really need quantum mechanics to explain some of the phenomena we observe. The ability to understand and control continuously growing quantum systems, such as atoms and molecules, has progressed significantly over the last decades, facilitating a better understanding of quantum mechanics and how it describes Nature. Researchers all over the world work hard to harness quantum properties such as superposition and entanglement in a new type of computer that is fundamentally different from classical computers. We are at the brink of building prototype quantum computers and experiencing a major breakthrough, but we can only guess what will be future applications of such systems. Without any doubt, interesting times lie ahead of us.

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1.1. QUANTUM MECHANICS

SEVERAL experiments around the dawn of the 20th century could not be explained by the known laws of classical physics. One of the famous examples is the photoelectric effect for which Albert Einstein earned his Noble Prize. In his 1905 paper [1], he advanced the theory of light being composed of discrete packets (quanta) of energy, which we now know as photons. Later experiments proved his hypothesis, and that light not only behaves as waves, but also has a particle-like nature. Conversely, the double-slit experiment showing interference effects for electrons means they are not just particles, but they do behave wave-like in certain situations [2]. These are key examples of how the laws of quantum mechanics govern what happens at the smallest scale.

Wave-particle duality, superposition and entanglement are (somewhat counterintuitive) main concepts in quantum mechanics. Superposition is the notion that a particle can be in multiple states simultaneously, for example at several places. Entanglement refers to particles sharing a joint state that can not be described as the combination of the states of the individual particles. The state of the individual particles in an entangled state is not well-defined, at least, until a measurement takes place, because then the wave function collapses and a definite state for each particle will be measured.

The counter-intuitive features of the quantum theory are sometimes hard to accept. Even Einstein was of the opinion the theory was incomplete, as he wrote down with Podolski and Rosen in their famous Gedankenexperiment [3]. Despite this, the theory has proven to be very successful in describing what happens in the world surrounding us. Quantum mechanics makes accurate predictions that can be experimentally verified, and already has significant contributions to society, for example the laser and magnetic resonance imaging (MRI).

1.2. QUANTUM SIMULATION AND COMPUTATION

TWO potential future applications of quantum mechanics are quantum simulation and quantum computation, as proposed already in the 1980s by Richard Feynman [4]. As Nature behaves quantum mechanically, the only way to properly simulate it is by using a quantum mechanical system. This is because superposition and entanglement make the number of states available to a quantum mechanical system grow exponentially with system size, while for a classical system the number of states grows linearly. Therefore, a quantum mechanical system quickly becomes intractable in a classical simulation as it grows. This exponential growth of complexity is also the origin of an enormous potential of computational power if quantum mechanics can be exploited to perform calculations. Opportunities of quantum computation lie, for example, in the field of material science (discovery of a high temperature superconductor) and drug design (more targeted selection of potential active substances).

Research groups all over the world, together with industry partners, are working on developing the quantum bit (qubit), the basic building block of a quantum computer. Analogous to how a classical bit, which is a two-level system that can be 0 or 1, can be used to store and process classical information, a quantum mechanical two-level system, that can be in a superposition of $|0\rangle$ and $|1\rangle$,[1] can be used as a qubit to store and

[1] The $|...\rangle$ notation indicates quantum states.

process quantum information. In addition, more and more attention is devoted to the other required parts of the quantum computing stack, such as control electronics and software. To harness the full potential offered by quantum computation, millions of qubits are required for fault-tolerant quantum computation, in order to fully describe the complex systems of interest, while being able to detect and correct errors in the calculation by means of quantum error correction (QEC).

However, before fault-tolerant quantum computers will become available, devices consisting of roughly 50 qubits or more, will already be capable of classically intractable, albeit useless, calculations.[2] John Preskill came up with the terms *quantum supremacy* [5] and *Noisy Intermediate Scale Quantum (NISQ)* technology [6] to describe this era ahead of us. Quantum supremacy refers to performing a task on a quantum device that cannot be performed by any existing classical computer. Google made demonstrating quantum supremacy one of their major milestones and recently announced to have achieved this [7]. However, IBM says they could simulate Google's experiment on a classical supercomputer in 2.5 days, albeit without actually performing the simulation [8]. In the near future, the number of qubits working together will maximally be a few hundred (intermediate scale) and their control will not be perfect (noisy). This will limit what can be done with such systems, but they still will open up possibilities to explore new physics and facilitate progress towards larger-scale quantum devices, and therefore the NISQ era already is a very interesting time for physicists.

QUBIT IMPLEMENTATIONS AND QUANTUM COMPUTER DEVELOPMENT

Several possible physical systems to implement a qubit exist. The main qubit candidates are trapped ions, cold atoms, superconducting qubits, spin qubits in quantum dots, spin qubits in nitrogen-vacancy centers in diamond and topological qubits based on Majorana fermions. They are at different stages of maturity, but for all of them the number of qubits in a single system is far from the millions required for large-scale quantum computation. All candidates have their advantages and disadvantages, and at this moment it is not yet clear which type or combination of qubit(s) is most suited. Industry puts most effort in superconducting qubits (Google, IBM, Rigetty and Intel), spin qubits in silicon quantum dots (Intel, CEA-Leti, STMicroelectronics, HRL and Imec) and topological qubits (Microsoft).

THE DIVINCENZO CRITERIA

Any type of qubit should fulfill a set of requirements, known as the DiVincenzo criteria [9], for it to be a viable candidate for large-scale quantum computation. These criteria are the following:

1. *Scalable physical system with well characterized qubits*
   For a physical system to act as a good qubit, its internal energy levels, including the coupling between them, should be known accurately, as well as interactions with other qubits and external fields. Furthermore, it should be, in principle, possible to increase the number of qubits to an arbitrary number.

[2] Computing the final state resulting from a random gate sequence on ~50 qubits is classically not possible on current hardware.

2. *Ability to initialize the state of the qubits to a simple fiducial state*
   Naturally, a set of qubits on which a computation is performed should be in a well-known state before a computation commences for it to give a meaningful outcome. In addition, to be able to detect and correct errors during computation by means of quantum error correction, a continuous supply of qubits in their ground state is required.

3. *Long relevant decoherence times*
   Quantum information has to be retained throughout the duration of the computation that is being performed. Qubits loose their quantum information due to decoherence. They can be protected from this by means of quantum error correction if the qubit coherence survives much longer than the time it takes to perform a single quantum operation.

4. *Universal set of quantum gates*
   To be able to perform universal quantum computation, qubits should offer the possibility to perform single- and two-qubit operations. It has to be possible to compose a complete set of quantum gates from the native interactions present.

5. *Qubit-specific measurement capability*
   To determine the outcome of a computation, it should be possible to measure the state of individual qubits. Ideally, such a measurement does not depend on the state of nearby qubits and leaves the state of the rest of the quantum computer unchanged.

Spin qubits in silicon quantum dots, the focus of this dissertation, can in principle satisfy all of these criteria and will be introduced in the next section.

THE DEVELOPMENT STAGES OF QUANTUM INFORMATION PROCESSING

Michel Devoret and Robert Schoelkopf later formulated seven stages (of increasing complexity) in developing quantum information processing [10]. These steps are depicted in Fig. 1.1. David DiVincenzo, who came up with the aforementioned criteria, referred to these steps as *complexity steps* and he expects that the upcoming future will be guided by these principles.[3] The DiVincenzo criteria are related to the first two stages that only involve physical qubits, while in the later stages quantum error correction and logical qubits play a role.

1.3. SILICON SPIN QUBITS

SILICON spin qubits store quantum information in the spin degree of freedom of electrons trapped in small conductive islands in silicon (see Sec. 2.2 for more details). For spin qubits in silicon quantum dots [11, 12] several few-qubit experiments, such as the demonstration of long coherence times [13], (high-fidelity) single- [13–16] and two-qubit gates [17–20], quantum algorithms [21], quantum non-demolition measurements [22, 23], strong spin-photon coupling [24–26] and long distance spin-spin coupling [27], have been demonstrated. Therefore, silicon spin qubits have already demonstrated most of the aforementioned DiVincenzo criteria and are promising candidates to

[3] David DiVincenzo, *Looking back at the DiVincenzo criteria*, QuTech Blog (2018)

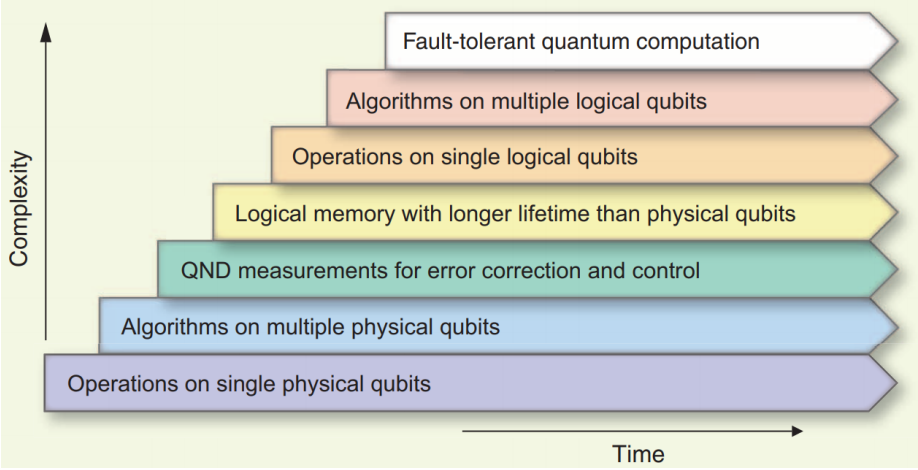

Figure 1.1: The development of quantum computation in seven stages of increasing complexity, where each step requires full proficiency over the preceding steps. Current research is still mostly focused on the lower stages, and silicon spin qubits are at the third stage with the recent demonstration of quantum non-demolition (QND) measurements [22, 23]. Adapted from Ref. [10].

be used in quantum computation, because their small footprint and compatibility with conventional CMOS fabrication make them attractive for scaling [28]. However, increasing the number of qubits (to the millions required for fault-tolerant quantum computation) still comes with challenges and for that reason the focus of this dissertation is on the scaling of silicon spin qubits.

Among other factors, qubit fabrication has to be reliable and reproducible, noise processes that cause qubit relaxation and decoherence (at elevated temperatures) have to be understood, and methods to control a large number of qubits have to be developed. These three aspects of scaling are the focus of the work presented in this dissertation, and will be discussed in the separate chapters. Therefore, the goal of this dissertation can be summarized as enabling next steps in the quest for larger quantum computation systems based on silicon spin qubits by solving some of the physics and engineering challenges involved in scaling.

1.4. THESIS OUTLINE

THE work presented in this dissertation is all motivated by the overarching goal of scaling up the system size and increasing the number of silicon spin qubits. The individual chapters discuss separate projects motivated by this goal, but do not directly build on each other. In what follows, the organization of this dissertation is sketched together with the connections between different chapters.

- **Chapter 2** provides the theoretical background for the work presented in the other chapters that follow. Quantum computation in general and spin qubits in silicon in particular are discussed.

- **Chapter 3** presents work on the development of a reliable and reproducible integration scheme for silicon quantum dot structures, that are meant for spin qubit experiments, in an academic cleanroom environment.
- A silicon spin qubit device fabricated following these fabrication recipes is used in **Chapter 4** for experiments on the dependence of spin relaxation on temperature and the external magnetic field, as well as the temperature dependence of charge noise. The purpose of this work is to assess the prospects of operating silicon spin qubits at elevated temperatures, which would allow for on-chip integration of classical control electronics.
- **Chapter 5** discusses a study of spatial noise correlations in a Si/SiGe two-qubit system based on Bell state coherences. We assess to what extent the assumption of negligible correlations in qubit errors in most quantum error correction schemes, on which large-scale quantum computers will have to rely, is justified.
- After having studied several aspects that are relevant to determine the suitability of silicon spin qubits for the use in large-scale quantum computers in the preceding chapters, **Chapter 6** presents a proposal for the design of a large-scale array of spin qubits that locally integrates classical control electronics. We assess the feasibility of such a design by considering the required electronic components, and the associated footprint, line scaling, interconnect density and heat load.
- Finally, in **Chapter 7** I summarize the key findings of this dissertation and draw some conclusions. Furthermore, I give an outlook for further research towards a large-scale quantum computer based on silicon spin qubits.

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2

THEORY

This chapter provides the theoretical background relevant for the work presented in this thesis. First, a brief introduction to relevant general quantum computation concepts is given, followed by an explanation of the basics of spin qubits in silicon quantum dots.

2.1. QUANTUM COMPUTATION

QUANTUM mechanics offers a fundamentally different way of computation, which makes it possible to solve certain problems that cannot be solved in a reasonable time by even the most powerful classical computers. This section introduces the basic concepts of quantum computation.

2.1.1. QUANTUM BITS

A quantum bit (qubit) is the quantum mechanical analog of a classical bit. A classical bit is formed by a classical two-level system and equivalently a qubit is formed by a quantum mechanical two-level system. While a classical bit can be either in 0 or 1, a qubit in general is in a quantum mechanical superposition of $|0\rangle$ and $|1\rangle$:

$$|\psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle\,, \tag{2.1}$$

with $|\alpha|^2 + |\beta|^2 = 1$ to ensure normalization. The probability for the qubit to collapse to the $|0\rangle$ or $|1\rangle$ state upon measurement, is given by $|\alpha|^2$ and $|\beta|^2$, respectively. Without loss of generality, it is possible to write $\alpha = \cos\left(\frac{\theta}{2}\right)$ and $\beta = e^{i\varphi}\sin\left(\frac{\theta}{2}\right)$. Here, θ determines the amplitude (and probability) of the two basis states, and φ sets the relative phase between these states. Following this definition, the state of a qubit can be represented on the Bloch sphere, see Fig. 2.1. All possible qubit states defined by Eq. 2.1 lie on the surface of this unity sphere.

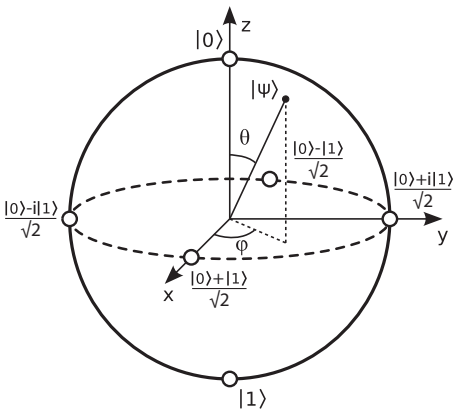

Figure 2.1: Bloch sphere representation of a qubit. The qubit basis states $|0\rangle$ and $|1\rangle$ lie at the poles of the sphere. The four other cardinal states on the $\hat{x}$ and $\hat{y}$ axis are also indicated. A general qubit state $|\psi\rangle$ is defined by θ and φ, as given by Eq. 2.1 and the definition of α and β in the main text. Adapted from en.wikipedia.org (courtesy of Smite-Meister).

Quantum information is fragile and will be lost over time as a result of several processes. Relaxation is the decay of the excited state ($|1\rangle$) to the ground state ($|0\rangle$), which is related to the projection of the qubit state on the $\hat{z}$ axis of the Bloch sphere, so to θ. The corresponding characteristic timescale is called T_1. Decoherence refers to the randomization of the phase φ of the qubit state, which corresponds to the direction in the $\hat{x}-\hat{y}$ plane of the Bloch sphere. Decoherence takes place at the timescale T_2^*.

A multi-qubit generalization of the Bloch sphere picture does not exist, but a general N-qubit state can be represented by a $2^N \times 2^N$ matrix, called a density matrix. The diagonal elements of a density matrix describe the population of the different N-qubit states, while the off-diagonal elements quantify the coherences between these states. For example, the density matrix corresponding to the two-qubit Bell state $|\Psi^+\rangle = \frac{|01\rangle+|10\rangle}{\sqrt{2}}$ is, in the $\{|00\rangle, |01\rangle, |10\rangle, |11\rangle\}$ basis, given by

$$\rho_{|\Psi^+\rangle} = \frac{1}{2}\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}. \tag{2.2}$$

SINGLE- AND TWO-QUBIT GATES

Creating a single-qubit state corresponding to any point on the Bloch sphere in general requires a combination of rotations (i.e. single-qubit gates) about two independent axis. For example, one has to be able to perform rotations about the $\hat{x}$ and $\hat{z}$ axis, but the two axis do not necessarily have to be orthogonal. This required controllability is referred to as two-axis single-qubit control. In general, single-qubit gates are described by 2×2 unitary matrices that are a linear combination of the identity matrix and the Pauli matrices.

To harness the full potential of quantum computation, it is required to create entanglement between qubits. The Bell state $|\Psi^+\rangle = \frac{|01\rangle+|10\rangle}{\sqrt{2}}$ is a maximally entangled state in which the two entangled qubits share a well-defined joint state, while the state of the individual particles is not defined. One of the qubits is in $|0\rangle$ and the other qubit is in $|1\rangle$, but which of them is in $|0\rangle$ and which is in $|1\rangle$ is undetermined.

To create entanglement between qubits, two-qubit gates (described by 4×4 unitary matrices) are required. The prototypical example of a two-qubit gate is the controlled-NOT (CNOT) gate. The CNOT gate flips the target qubit if the control qubit is in the $|1\rangle$ state, while the target qubit is unaffected if the control qubit is in the $|0\rangle$ state. In the $\{|00\rangle, |01\rangle, |10\rangle, |11\rangle\}$ basis the CNOT gate is described by the matrix:

$$U_{CNOT} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix}. \tag{2.3}$$

It can be proven that any logical multi-qubit gate can be composed from single-qubit gates and the CNOT gate, and for that reason this is called a universal gate set for quantum computation [1].

A common way to represent a quantum computation consisting of single- and multi-qubit gates, is a quantum circuit diagram. Figure 2.2 shows an example of a quantum circuit diagram. Each horizontal line represents a qubit, a block interrupting a line represents a gate and a block connecting lines is a multi-qubit gate.

2.1.2. QUANTUM ERROR CORRECTION

As already mentioned, quantum states are fragile and interaction with the environment causes decoherence, resulting in loss of quantum information. However, qubit control,

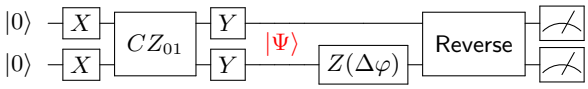

Figure 2.2: Quantum circuit diagram used in the experiments described in Ch. 5 to create the Bell state $|\Psi\rangle = \frac{|01\rangle - i|10\rangle}{\sqrt{2}}$ starting from the $|00\rangle$ state. The X and Y blocks represent 90 degree single-qubit rotations around the $\hat{x}$ and $\hat{y}$ axis, respectively, the Z block represents a rotation over $\Delta\varphi$ around the $\hat{z}$ axis, and the CZ_{01} block represents the two-qubit controlled-phase gate that phases the $|01\rangle$ state by -1, while leaving the other states unaffected. Here, the Reverse block implies execution of the preparation sequence in the reverse order and the blocks containing a dial represent single-shot measurements of the qubit.

and consequently quantum computation, relies on controlled interactions with the environment. Therefore, it is necessary to be able to deal with the inevitable errors occurring during any computation. For that purpose quantum error correction (QEC), analogous to classical error correction, has been developed. QEC makes it possible to detect and correct errors in a quantum computation by encoding a logical qubit in multiple physical qubits. Two types of (physical) qubits exist, based on their function: the data qubits store the qubit state, while the ancilla qubits are used to detect errors.

If the error probability is sufficiently low (below a constant threshold), i.e. if the fidelity of the individual operations is sufficiently high, the overall error can be reduced at the expense of more overhead by encoding the logical information in more and more physical qubits. In this situation, quantum computation is said to be fault-tolerant and can be performed with arbitrary precision [2].

Several QEC schemes exist, with the surface code as the most well-known example [3]. A concrete example is Surface-17, which encodes one logical qubit in 17 physical qubits [4]. The surface code has an error threshold of ~1% [5]. This threshold, as well as most other thresholds, is derived under the assumption of negligible correlations in individual qubit errors.

2.2. SPIN QUBITS IN SILICON QUANTUM DOTS

THE work in this thesis is focused on spin qubits in silicon quantum dots. This section first introduces gate-defined semiconductor quantum dots. Then, a brief overview of spin qubit implementations is given, followed by a discussion of several aspects that are relevant for (single-)spin qubits. Finally, the relevant properties of silicon for spin qubits are discussed.

2.2.1. SEMICONDUCTOR QUANTUM DOTS

Quantum dots (QDs) are tiny regions of conducting material in an environment of insulating material. Several types of QDs exist, but the work in this thesis only concerns lateral gate-defined QDs in semiconductors [6]. Due to the small size of these QDs (10-100 nm), it takes a finite energy to add an extra electron, because of Coulomb repulsion, as described by the constant-interaction model [7]. The additional energy required to add an extra electron to a QD is given by its charging energy $E_C = \frac{e^2}{2C}$,[1] and a sufficiently

[1] Here $e = 1.602 \cdot 10^{-19}$ C is the elementary charge and C is the total capacitance of the QD.

large charging energy allows to control the number of electrons confined in a QD accurately down to the single-electron regime. Furthermore, the small size also causes the orbital levels of electrons in such islands to be quantized. Adding electrons to a QD one by one shows shell filling and therefore quantum dots are often called artificial atoms [8].

To create lateral gate-defined QDs, first a two-dimensional electron gas (2DEG) is formed by confinement at an interface in a heterostructure. Band gap differences between the materials result in strong confinement in the vertical direction, which yields quantization of the electron motion perpendicular to the interface. The 2DEG is either supplied with electrons from a doping layer in the heterostructure (depletion-mode QDs) or induced by accumulation gates (accumulation-mode QDs). Examples of such material systems are gallium arsenide/aluminium gallium arsenide (GaAs/AlGaAs), silicon/silicon germanium (Si/SiGe) and silicon/silicon dioxide (Si/SiO_2). The latter is also referred to as Si-MOS, after the metal-oxide-semiconductor (MOS) stack. The work in this thesis concerns Si/SiGe and Si-MOS and these material systems are discussed in more detail later in this section. After forming the 2DEG, fine gate electrodes on top of the heterostructure allow to locally tune the potential landscape in the 2DEG by setting the gate voltages, thereby forming QDs that are isolated from other dots and the reservoirs by tunnel barriers. The same gate electrodes can be used to control the number of electrons in the QDs.

The number of electrons in a QD can be determined from transport measurements through the QD, but alternatively can also be measured non-invasively and very accurately by using a nearby charge sensor. A quantum point contact (QPC) [9] or QD [10] in the proximity of the QD to be sensed can be used as a charge sensor. As another possibility, one of the gate electrodes used to define the QD can be used for dispersive charge sensing [11]. The measurement of the occupation of a QD with a charge sensor does not depend on the tunnel barriers of the QD, which makes a charge sensor more suitable for the few-electron regime than transport measurements.

For the experiments in this thesis a sensing QD has been used. This method relies on the fact that transport through a QD is only possible if one (or more) of the discrete energy levels is (are) within the bias window between source and drain, while transport is not allowed otherwise due to Coulomb blockade. Transport through a QD that is tuned on the flank of one of its Coulomb peaks is very sensitive to its electrostatic environment, which makes it possible to discriminate single electrons in the environment of the sensing dot. A sensing QD can be used in transport, possibly in combination with lock-in techniques [12], or alternatively, the sensing dot can be embedded in a resonant circuit for RF sensing [10].

2.2.2. SPIN QUBITS

Having established the ability to trap a single electron in a quantum dot, this electron, being a spin-1/2 particle, offers the canonical example of a quantum mechanical two-level system formed by the electron spin-up and spin-down states. The spin of an electron is an intrinsic angular momentum giving rise to a magnetic dipole moment. The magnitude of this dipole moment is given by the Bohr magneton $\mu_B = 9.274 \cdot 10^{-24}$ J/T.

As a result, an external magnetic field B_{ext} splits the spin-up and -down states in energy due to the Zeeman effect by

$$E_Z = g\mu_B B_{ext}, \tag{2.4}$$

where g is the electron g-factor ($g \approx 2$ in silicon). The spin states of an electron in a magnetic field serve as the computational basis states of a qubit in what is referred to as a single-spin qubit or Loss-DiVincenzo (LD) qubit [13].

The single-spin qubit is the simplest form of a spin qubit, but several other implementations of spin qubits exist, which employ spin states of more than one electron in more than one quantum dot to define a qubit. In contrast with the single-spin qubit, all other types of spin qubits constitute an effective pseudo-spin two-level system. Examples of other spin qubit implementations are the singlet-triplet qubit (two electrons in two dots) [14], the hybrid qubit (three electrons in two dots) [15], the (always-on) exchange-only qubit (three electrons in three dots) [16, 17], as well as the quadrupolar exchange-only qubit (four electrons in three dots) [18]. All these spin qubit implementations attempt to mitigate certain decoherence mechanisms or to reduce the experimental requirements at the expense of complexity.

In general, using spin states as basis states for a qubit has the advantage of long coherence times, compared to for example a charge qubit [19], because spin does not interact directly with electric noise. However, spin-orbit coupling does provide an indirect coupling, which still causes decoherence, albeit less than for charge qubits. With a reduced effect of electrical noise sources, the hyperfine interaction also is a relevant decoherence mechanism for spin qubits. Spin-orbit coupling and the hyperfine interaction are discussed below.

SPIN-ORBIT COUPLING

An electron moving in an electric field $\vec{E}$, will experience a magnetic field in its own reference frame as a result of relativity. The effective magnetic field is proportional to $\vec{E} \times \vec{p}$, where $\vec{p}$ is the momentum of the electron, so it depends on the orbital motion of the electron, thereby coupling the spin of the electron to its orbital motion. In solids, such electric fields can originate from the absence of structural inversion symmetry or bulk inversion symmetry. Interfaces in general have structural inversion asymmetry, which causes Rashba spin-orbit interaction [20]. Bulk inversion asymmetry occurs for example in the zinc-blende structure of GaAs and gives rise to the Dresselhaus contribution to the spin-orbit interaction [21].

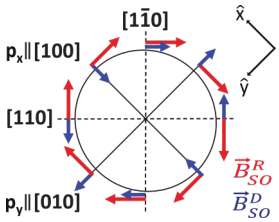

Figure 2.3: Rashba (red) and Dresselhaus (blue) contributions to the spin-orbit field $\vec{B}_{SO}$ for an electron moving in two dimensions with momentum $\vec{p}$. Here $|\alpha| \neq |\beta|$, $\alpha < 0$ and $\beta > 0$. Adapted from Scarlino *et al.* [22].

Spin-orbit interaction in two dimensions is described by the Hamiltonian

$$H_{SO}^{2D} = \alpha(-p_y\sigma_x + p_x\sigma_y) + \beta(-p_x\sigma_x + p_y\sigma_y), \tag{2.5}$$

where α and β describe the strength of the Rashba and Dresselhaus terms, respectively, p_i is the i component of the momentum of the electron and σ_i is the Pauli i spin matrix. α is determined by the material(s) and the confinement potential, and β depends on material properties and $\langle p_z^2 \rangle$ [23]. As depicted in Fig. 2.3, the Rashba and Dresselhaus contributions to spin-orbit interaction add up, cancel or are perpendicular for motion in certain directions. The total strength of the spin-orbit interaction is therefore anisotropic and is characterized by the distance an electron has to travel for a spin-orbit-induced π rotation, known as the spin-orbit length l_{SO}.

In the presence of spin-orbit coupling, the eigenstates are admixtures of spin and orbital states [24]. Electric noise does not couple directly to spin, but will couple to the orbital part leading to spin relaxation [24–26]. The most important source of electric field fluctuations in experimental setups with proper filtering is formed by phonons. Only acoustic phonons contribute, since optical phonons typically have energies much higher than the Zeeman energy [27]. Deformation potential phonons deform the crystal lattice inhomogeneously and are relevant in all semiconductors, while piezoelectric phonons cause homogeneous strain and only play a role in polar crystals [23]. Spin-orbit coupling does, to leading order, not give rise to pure dephasing of electron spins [28].

HYPERFINE INTERACTION

The spin of an electron in a quantum dot interacts with the spin of nuclei in the host material via the hyperfine interaction. The Fermi contact hyperfine interaction between the electron spin and nuclear spins is described by the Hamiltonian

$$H_{HF} = \sum_{i=1}^{N} A_i \vec{I}_i \cdot \vec{S} = g\mu_B \vec{B}_N \vec{S}, \tag{2.6}$$

where A_i is the interaction strength of the electron spin with the spin of nucleus i that depends on the overlap of the electron wave function with nucleus i, $\vec{I}_i$ and $\vec{S}$ are the spin operators for nucleus i and the electron, respectively, and $\vec{B}_N = \sum_{i=1}^{N} \frac{A_i \vec{I}_i}{g\mu_B}$ is an effective magnetic field (Overhauser field) describing the ensemble of nuclear spins acting on the electron spin, similar to an external magnetic field [23, 29].

The unknown and fluctuating nature of the Overhauser field results in a random evolution of the electron spin, causing decoherence [30–33]. The timescale of nuclear spin dynamics is typically longer than for the electron spin, so the Overhauser field assumes a quasi-static random value. For a Gaussian distributed Overhauser field with standard deviation σ_N, the electron spin coherence shows a Gaussian decay with timescale [23, 30]

$$T_2^* = \frac{\sqrt{2}\hbar}{g\mu_B\sigma_N}, \tag{2.7}$$

where $\hbar = \frac{h}{2\pi}$ is the reduced Planck constant.

In usual experimental settings, the energy scale of the hyperfine interaction is much smaller than the Zeeman energy, so hyperfine interaction does not lead to spin relaxation.

ELECTRON SPIN RESONANCE AND ELECTRIC DIPOLE SPIN RESONANCE

Single-qubit gates for single-spin qubits are based on the interaction of spin with magnetic fields. The Zeeman effect lifts the degeneracy of spin states in a magnetic field, as expressed in Eq. 2.4. Additionally, an oscillating magnetic field B_1 perpendicular to the static field that splits the spin-up and spin-down states, drives Rabi transitions between these states if its frequency f matches the energy difference ($hf = g\mu_B B_{ext}$). This is called electron spin resonance (ESR) and its most direct implementation is by applying an oscillating magnetic field by passing an alternating current with frequency f through an on-chip microwave stripline close to the electron spin. This has been demonstrated both in GaAs [34] and silicon devices [35]. Careful stripline design results in bulky structures, making it challenging to properly implement several striplines in one device and to achieve individual addressability of several electron spins. Furthermore, dissipation in the stripline causes sample heating, but this can be circumvented by using a superconducting material for the stripline.

Alternatively, an electron can also be made to experience an effective oscillating magnetic field by moving it back and forth in a spatially varying magnetic field, thereby driving spin transitions if the frequency of the oscillating motion matches the energy difference between the spin-up and spin-down states. In that case the coupling is indirect, via the charge of the electron, and the effect is referred to as electric dipole spin resonance (EDSR). A magnetic field varying on the length scale of quantum dots can be generated by micron sized magnets in the proximity of the dots, as proposed by Tokura *et al.* [36] and first demonstrated by Pioro-Ladrière *et al.* [37]. The magnitude of the effective oscillating magnetic field is given by

$$B_{MM}^{ac} = \frac{eE_{ac}l_{orb}^2 \left|\frac{\partial B_{x,y}}{\partial z}\right|}{E_{orb}}, \tag{2.8}$$

where e is the electron charge, E_{ac} is the amplitude of the varying electric field, l_{orb} is the spatial extend of the wave function, $\frac{\partial B_{x,y}}{\partial z}$ is the gradient of the transverse magnetic field component (x, y) in the direction of movement caused by the electric field (z) and E_{orb} is the confinement energy. Spin-orbit coupling (SOC) can also give rise to an effective magnetic field experienced by a moving electron, and for that reason the magnetic field gradient generated by micromagnets is sometimes called an artificial spin-orbit field. In GaAs, SOC can be used as an efficient driving mechanism [38], but SOC is weak in bulk silicon and spin-orbit driving therefore is inefficient. Nevertheless, interface effects allow for spin-orbit-like driving of silicon spin qubits [39, 40].

For single-spin qubits, the required two-axis control is achieved by microwave driven rotations based on E(D)SR around the $\hat{x}/\hat{y}$ axis, and rotations around the $\hat{z}$ axis by updating the rotating reference frame in software [41].

MICROMAGNET DESIGN FOR EDSR

A magnetic field in general has components in all three spatial directions as well as gradients of each component in all three directions, so in total there are twelve relevant quantities to consider in designing micromagnets for EDSR driving of spin qubits. Fortunately, Maxwell's equations and symmetry reduce this number. This section first makes

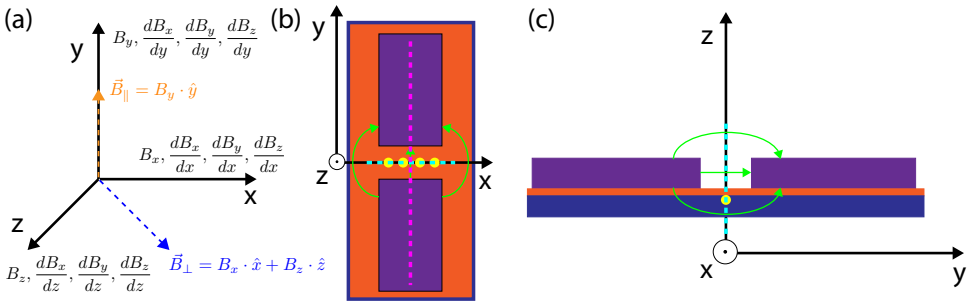

Figure 2.4: (a) The coordinate frame used for the discussion on micromagnets. All three directions have a magnetic field component and a gradient of all three components in that direction associated with it. An external magnetic field is applied in the $\hat{y}$ direction resulting in the indicated parallel and perpendicular field components. (b,c) A simple micromagnet design (purple rectangles) that is symmetric in the cyan and magenta lines. The qubits are indicated by yellow circles at the blue-orange interface in the heterostructure. Magnetic field lines are sketched in green. B_x and B_z vanish in the $\hat{x}$-$\hat{z}$ plane at $y = 0$ (indicated by the cyan lines).

some definitions and then gives an overview of what is relevant for micromagnet design to facilitate further discussions.

The coordinate frame used in this discussion is defined in Fig. 2.4. The 2DEG is formed in the $\hat{x}$-$\hat{y}$ plane, with the qubits along the $\hat{x}$ axis. An in-plane external magnetic field is applied along the $\hat{y}$ direction,[2] so the $\hat{y}$ component of the magnetic field generated by the micromagnet(s) is parallel to the external magnetic field: $\vec{B}_\parallel = B_y \cdot \hat{y}$. The $\hat{x}$ and $\hat{z}$ components of the micromagnet field add up to form the perpendicular magnetic field: $\vec{B}_\perp = B_x \cdot \hat{x} + B_z \cdot \hat{z}$.

The qubit frequency is defined by the absolute value of the total magnetic field via the Zeeman splitting as given by:

$$f = \frac{g\mu_B |\vec{B_{tot}}|}{h}, \tag{2.9}$$

where $|\vec{B_{tot}}| = \sqrt{B_x^2 + B_y^2 + B_z^2}$ is the vector sum of the field components of the total magnetic field in all three directions. For a magnet design symmetric in the $\hat{x}$-$\hat{z}$ plane indicated by the cyan lines in Figs. 2.4(b,c), B_x and B_z vanish in this plane. Since the qubits are in this plane, B_x and B_z vanish at the positions of the qubits, and B_y is the only relevant component; B_y is maximum in this plane. The qubit addressability is determined by the gradient of the parallel magnetic field component along the axis connecting the qubits, which is now given by $G_\parallel = \frac{\partial B_\parallel}{\partial x} = \frac{\partial B_y}{\partial x}$. This gradient, however, does also cause decoherence and therefore should be minimized given the required minimal addressability, so one has to find a balance between addressability and decoherence. The qubits are assumed to be driven in the $\hat{y}$ direction,[3] so the gradient responsible for driving of the

[2] Applying the external magnetic field along the long axis of the micromagnets is most logical, but for more complicated designs the long direction might not be obvious. Furthermore, in general the external magnetic field can be applied in another direction and this choice affects the following discussion. It is important to consider the effect on the magnetization of the micromagnet(s).

[3] Depending on the gate design, the qubits can be driven in both the $\hat{x}$ and $\hat{y}$ direction. This choice affects the

electron spin is given by: $G_\perp = \frac{\partial B_\perp}{\partial y} = \sqrt{\left(\frac{\partial B_x}{\partial y}\right)^2 + \left(\frac{\partial B_z}{\partial y}\right)^2}$ [42]. Here, the quantization axis is assumed to be fixed in the $\hat{y}$ direction, which to first-order is correct, since B_x and B_z vanish at the positions of the qubits. All other gradients $\left(\frac{\partial B_x}{\partial x}, \frac{\partial B_x}{\partial z}, \frac{\partial B_y}{\partial y}, \frac{\partial B_y}{\partial z}, \frac{\partial B_z}{\partial x}\right.$ and $\left.\frac{\partial B_z}{\partial z}\right)$ purely cause decoherence and should be minimized.

The stationary Maxwell equations in free space:

$$\nabla \times \vec{B} = \left(\frac{\partial B_z}{\partial y} - \frac{\partial B_y}{\partial z}\right)\hat{i} + \left(\frac{\partial B_x}{\partial z} - \frac{\partial B_z}{\partial x}\right)\hat{j} + \left(\frac{\partial B_y}{\partial x} - \frac{\partial B_x}{\partial y}\right)\hat{k} = 0, \tag{2.10}$$

$$\nabla \cdot \vec{B} = \frac{\partial B_x}{\partial x} + \frac{\partial B_y}{\partial y} + \frac{\partial B_z}{\partial z} = 0, \tag{2.11}$$

give relations between the nine magnetic field gradients:

$$\begin{aligned} \frac{\partial B_z}{\partial y} &= \frac{\partial B_y}{\partial z}, \\ \frac{\partial B_x}{\partial z} &= \frac{\partial B_z}{\partial x} = 0, \\ \frac{\partial B_y}{\partial x} &= \frac{\partial B_x}{\partial y}, \\ \frac{\partial B_x}{\partial x} &= \frac{\partial B_y}{\partial y} = \frac{\partial B_z}{\partial z} = 0, \end{aligned} \tag{2.12}$$

where the two equal-to-zero statements (that equate five of the gradients to zero) are true for a design that is symmetric in the $\hat{x}$-$\hat{z}$ plane indicated by the cyan lines shown in Figs. 2.4(b,c). This might not be true for a more complex design that is optimized for driving and addressability, but a careful design should minimize the effects of these five gradients that purely cause decoherence.

The four remaining gradients result in driving $\left(\frac{\partial B_x}{\partial y}\right.$ and $\left.\frac{\partial B_z}{\partial y}\right)$ and addressability $\left(\frac{\partial B_y}{\partial x}\right)$, or cannot be circumvented as a consequence of the Maxwell equations $\left(\frac{\partial B_y}{\partial z}\right)$. The main contribution to the driving gradient is $\frac{\partial B_z}{\partial y}$, which therefore should be maximized. Simultaneously also the decohering gradient $\frac{\partial B_y}{\partial z}$ will be maximized, but that cannot be prevented. $\frac{\partial B_x}{\partial y}$ forms a smaller contribution to the driving and has the same magnitude as the addressability gradient $\frac{\partial B_y}{\partial x}$. These gradients should be minimized, while yielding the required minimal addressability.

EXCHANGE INTERACTION

Two-qubit gates for single-spin qubits exploit the exchange interaction between two electron spins. The exchange interaction arises from the Pauli exclusion principle, which states that two identical fermions are required to have an anti-symmetric wave function under particle exchange. Therefore, a symmetric spin wave function (triplet) has to be

discussion that follows. However, as will become clear, driving in the $\hat{x}$ direction is ineffective for the design considered here.

associated with an excited, higher energy state, while an anti-symmetric spin wave function (singlet) can be combined with the ground state. The result is an effective interaction between the spins of two electrons, which is expressed by the Hamiltonian

$$H = -J\vec{S}_1 \cdot \vec{S}_2, \tag{2.13}$$

where J is the exchange interaction strength and $\vec{S}_i$ is the spin operator for electron i. In solids, the magnitude and sign of J depend on wave function overlap and material properties. Positive J favors parallel spin alignment giving rise to ferromagnetism, while negative J favors anti-parallel spins giving rise to antiferromagnetism.

In spin qubits in quantum dots, the strength of the exchange interaction can be controlled by gate voltages via the tunnel coupling, because of its dependence on wave function overlap allowing for a tunable two-qubit interaction. Exploiting the exchange interaction for two-qubit gates was first proposed by Loss and DiVincenzo [13, 16]. Under its influence $|\downarrow\uparrow\rangle$ evolves into $|\uparrow\downarrow\rangle$ and back, because the singlet and triplet spin states are the eigenstates of the exchange interaction. Starting from $|\uparrow\downarrow\rangle$, proper timing of the interaction creates the maximally entangled state $\frac{|\downarrow\uparrow\rangle+|\uparrow\downarrow\rangle}{\sqrt{2}}$. This operation is known as the $\sqrt{SWAP}$ gate [1]. In the presence of a difference in Zeeman energy between two single-spin qubits, the exchange interaction still mediates two-qubit interaction, but flip-flop terms are suppressed by the difference in qubit energy. The resulting Hamiltonian is of Ising type and the native two-qubit gate is the controlled-phase (CZ) gate [43], which (up to single-qubit rotations) adds a phase to a specific two-qubit state: $CZ_{ij}|m,n\rangle = (-1)^{\delta(i,m)\delta(j,n)}|m,n\rangle$ for $i,j,m,n \in \{0,1\}$ [44].

SPIN READOUT

Single-shot readout of individual spins relies on spin-to-charge conversion, because the magnetic moment of a single electron spin is very small and therefore hard to detect directly. As discussed before, the number of electrons in a QD can be determined accurately by a nearby charge sensor, which allows to discriminate between different spin states if these states have a different charge configuration associated with them. The two most common methods used for spin readout are *Elzerman* readout (based on energy-selective tunneling) [45] and Pauli spin blockade (PSB) readout [46]. These two methods are explained below and the corresponding energy diagrams are shown in Fig. 2.5.

Elzerman readout relies on the energy difference between spin-up and spin-down states in a magnetic field. By tuning the electrochemical potential of the reservoir in between the spin energy levels, only an electron in the excited spin state is allowed to tunnel out to the reservoir, while an electron in the spin ground state will stay on the QD. An electron tunneling out and in again can be detected by a nearby charge sensor and signals the electron was in the excited spin state. If no tunnel event is detected, the electron was in its spin ground state. For a high readout fidelity, the Zeeman energy has to be sufficiently large compared to the thermal energy: $E_Z \gg k_B T$.

PSB readout discriminates singlet and triplet spin states. Starting in the (1,1) charge state and pulsing to the (0,2) charge state, under the right conditions a singlet spin state will be able to tunnel to the (0,2) charge configuration, while a triplet state will remain in the (1,1) configuration, because the triplet (0,2) state is higher in energy than the singlet

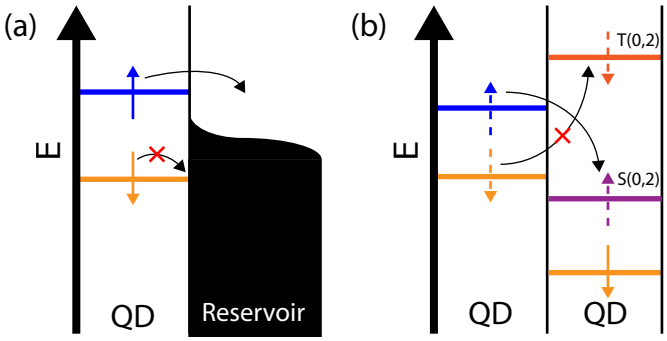

Figure 2.5: Energy diagrams for spin-to-charge conversion for spin readout in silicon. (a) For Elzerman readout the Fermi level of the reservoir is tuned in between the spin-up and spin-down energy levels. A spin-up electron can tunnel out, while a spin-down electron is trapped inside the QD. (b) For Pauli spin blockade (PSB) readout the right dot contains a spin-down reference electron. A spin-up electron in the left dot is able to tunnel to the singlet state in the right dot, while the triplet state is too high in energy for a spin-down electron to tunnel to the right dot.

state. Similar to Elzerman readout, the different charge configurations can be distinguished by a nearby charge sensor, signaling the combined spin state of the two electrons.

2.2.3. SILICON

Gallium arsenide (GaAs) for a long time has been the workhorse material for quantum dot experiments, because of its high material quality. Pioneering work on spin qubits has been performed in GaAs devices, having resulted in the demonstration of two-qubit gates for both singlet-triplet [47] and single-spin qubits [48]. However, all nuclei in GaAs carry spin, which gives rise to a strong hyperfine interaction between the electron spin and nuclear spins resulting in fast electron spin decoherence [47, 49]. Silicon based devices have the advantage of less spinful nuclei and therefore hold a strong promise as hosts for spin qubits. The advantage of fewer nuclear spins, as well as other relevant properties of silicon, will be discussed below. In addition, the fabrication of silicon quantum dots is largely compatible with conventional CMOS industry, which allows for large-scale manufacturing of silicon spin qubits and on-chip integration of classical control electronics [50].

HYPERFINE INTERACTION, SPIN-ORBIT COUPLING, SPIN RELAXATION AND G-FACTOR

In natural silicon, only 4.7% of the nuclei carry a spin, so the hyperfine interaction is small compared to GaAs, and isotopic purification allows to reduce the concentration of spinful nuclei even further [51]. In the context of the Avogadro project, silicon with a ^{29}Si concentration of 50 ppm has been produced [52], and several experiments in spin qubit devices with residual ^{29}Si concentration of 100–1000 ppm have been performed. As a result, spin coherence times are enhanced with a current record of $T_2^* = 120$ µs for quantum dot single-spin qubits [35], while for donors an even longer coherence time of $T_2^* = 270$ µs has been obtained [53].

Spin-orbit coupling in silicon is weak compared to GaAs, because of the lower atomic number and smaller band gap. Furthermore, bulk inversion asymmetry is absent in bulk silicon, so there is no Dresselhaus SOC, and the contribution is small otherwise. Finally, silicon does not have a polar crystal, so piezoelectric phonons do not exist. As a result, spin relaxation in silicon is slow compared to GaAs and a relaxation time $T_1 \approx 3$ s has been measured in a Si/SiGe quantum dot [54].

Electron spin relaxation in silicon quantum dots is expected to be dominated by Rashba SOC and phonon-induced modulation of the g-factor [25, 55–57]. Rashba SOC arises from the structural inversion asymmetry at the interface where the 2DEG is formed and at low temperature depends on magnetic field as $T_1^{-1} \propto B^7$. For quantum dots in Si(001) wafers,[4] relaxation caused by Rashba SOC is fastest for $B \parallel [100], [010]$ and slowest for $B \parallel [001]$, respectively. Phonon-induced modulation of the g-factor at low temperature yields $T_1^{-1} \propto B^5$ with fastest relaxation for $B \parallel [100], [010]$, while relaxation vanishes for $B \parallel [001], [110]$. Recently, another mechanism involving spin-valley mixing [58] has been experimentally demonstrated [59]. The dependence of spin relaxation on temperature and magnetic field in a Si-MOS quantum dot is studied in Ch. 4, and the results presented there are in agreement with the latter mechanism.

The electron g-factor in silicon is close to the free-electron value ($g \approx 2$), so spin-down is the ground state in silicon, in contrast to GaAs where a negative g-factor ($g \approx -0.44$) implies that spin-up is the ground state.

CONDUCTION BAND VALLEYS

For silicon, the bottom of the conduction band is not located at the center of the Brillouin zone (Γ point), but at non-zero wave vector along the Δ direction in between the Γ and X high symmetry points. As a result, there are six degenerate minima at $k_0 \approx \pm 0.85 \times \frac{2\pi}{a_0}$ in the $\hat{x}$, $\hat{y}$ and $\hat{z}$ directions, where a_0 is silicon's lattice constant. The band structure of silicon is shown in Fig. 2.6(a).

In two-dimensional structures, confinement lifts the four in-plane Δ valleys to much higher energies. In silicon/silicon-germanium (Si/SiGe) heterostructure in-plane strain also contributes to this effect. The remaining two-fold degeneracy of the Γ valleys is lifted by breaking of the inversion symmetry in the direction perpendicular to the 2DEG. This is the result of confinement at the interface where the 2DEG is formed and vertical electric fields. The energy difference between the two lowest valley states is referred to as the valley splitting, as depicted in Fig. 2.6(d).

Spin qubit experiments are potentially hindered by the presence of a low-lying excited valley state. If the valley splitting is not sufficiently large compared to the thermal energy $E = k_B T$, the excited valley state can be thermally populated, as was experimentally observed by Kawakami *et al.* [61]. First, this limits the initialization, manipulation as well as readout fidelity. Second, the exchange interaction often used for control of spin qubits (see Sec. 2.2.2) originates in the Pauli exclusion principle for fermions. Valleys offer an additional degree of freedom, which can render the exchange interaction ineffective [62]. Third, if the Zeeman energy and valley splitting are equal, states with both different spin and valley nature cross, and the combination of spin-orbit coupling and valley-orbit coupling gives rise to a second order spin-valley coupling, resulting in

[4] The growth direction for Si(001) wafers is [001].

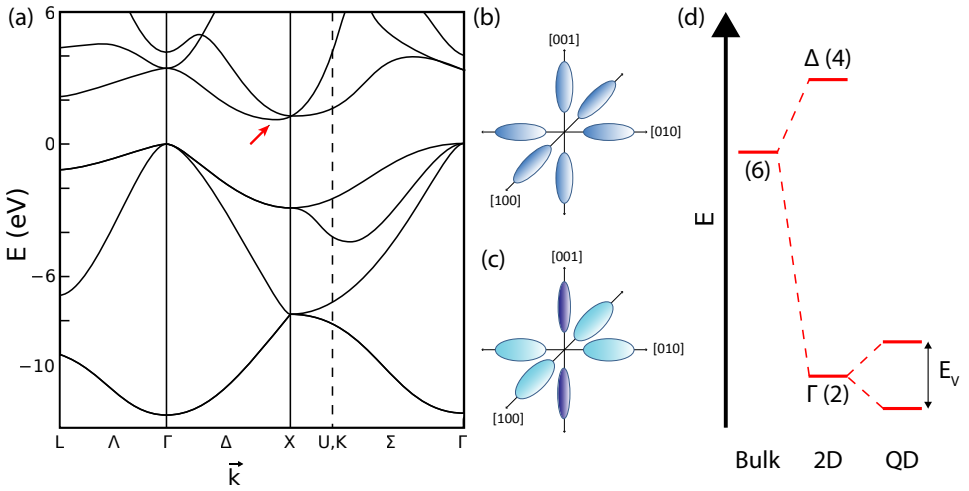

Figure 2.6: (a) Band structure of bulk silicon. The degenerate conduction band minimum is indicated by the red arrow. Adapted from de.wikipedia.org (courtesy of Cepheiden) [60]. (b,c) Constant energy surfaces (schematic, not to scale) near the conduction band minima for (b) bulk and (c) 2D silicon. The ellipsoids indicate a different curvature (and hence effective mass) in the longitudinal and transverse directions. In 2D structures (c) the parallel and perpendicular valleys split (courtesy of Pasquale Scarlino). (d) Valley splitting in silicon (schematic, not to scale). In bulk silicon, the conduction band minimum is six-fold degenerate (indicated between brackets), while in 2 dimensions the four Δ valleys are much higher in energy than the two Γ valleys. The Γ valleys are further split by the valley splitting E_V in QD structures.

fast spin relaxation in a hot spot. This was demonstrated by Yang *et al.* [59] and is used in the experiments presented in Ch. 4. Finally, switching between valleys in general results in a shift of the qubit frequency, causing the phase to be randomized, which result in decoherence on the timescale of the valley switching.

The experiments presented in Ch. 4 aim for increasing the operation temperature of silicon spin qubits, for which a large valley splitting is beneficial. Instead of being a nuisance, the valleys can also be used as an asset, for example in a valley qubit [63]. This has been experimentally demonstrated in Refs. [64, 65], but at present cannot compete with other semiconductor qubit implementations.

EFFECTIVE MASS

Transport and orbital properties at low temperature are affected by the effective mass m^*, which is inversely proportional to the curvature of the energy bands: $m^* \propto \left(\frac{\partial^2 E}{\partial k^2}\right)^{-1}$. The tunnel rate is, to first order, proportional to $\exp(-m^* E_B)$ for a tunnel barrier of height E_B, so a large effective mass gives a lower tunnel coupling. In addition, the orbital confinement energy is given by $E_{orb} \propto \left(m^* r_{dot}^2\right)^{-1}$, which implies tighter confinement in a smaller dot is required to achieve the same orbital energy in materials with a larger effective mass.

The effective mass for electrons in silicon is different for the transverse and longitudinal directions ($m_t^* = 0.19 m_e$ and $m_l^* = 0.92 m_e$, with m_e the free-electron mass), because the constant-energy surfaces near the conduction band minima are ellipsoids instead

of spheres (see Figs. 2.6(b,c)). In a silicon 2DEG grown in the $\hat{z}$ direction, the electrons occupy the lower-lying $\hat{z}$ valley(s) and are only allowed to move in the in-plane $\hat{x}$ and $\hat{y}$ directions, so the relevant effective mass is m_t^*. Furthermore, the effective mass in silicon is larger than in GaAs ($0.067 m_e$), so tunnel rates in silicon in general are lower than in GaAs, and more sensitive to gate voltages and charge noise. As a consequence, quantum dots in silicon have to be smaller, and to maintain a sufficient tunnel rate also closer together. Reducing the feature size poses challenging requirements on fabrication techniques. Integration techniques for the fabrication of silicon quantum dot devices are presented in Ch. 3.

SI-MOS AND SI/SIGE

Multiple variations of silicon-based quantum dot devices exist. The work in this thesis is concerned with two different planar options, silicon/silicon dioxide (Si-MOS) and silicon/silicon germanium (Si/SiGe), of which schematics are shown in Fig. 2.7. The 2DEG is formed at the interface of silicon and silicon dioxide (Si-MOS), and silicon and the silicon-germanium barrier layer (Si/SiGe), respectively, due to the band alignment at those interfaces. The SiGe buffer layer can be step- or linearly graded. For a step-graded buffer the Ge concentration is increased in steps and kept constant after each step to relax the stress, until in the last step a concentration of 30% is reached. In a linearly graded buffer the Ge concentration is increased gradually from 0% to 30%. In both cases the concentration is kept constant at 30% to fully relax the stress before the QW is grown. Most Si/SiGe hetrostructures use a Ge concentration of 30%, but other concentrations are used as well, which results in different properties.

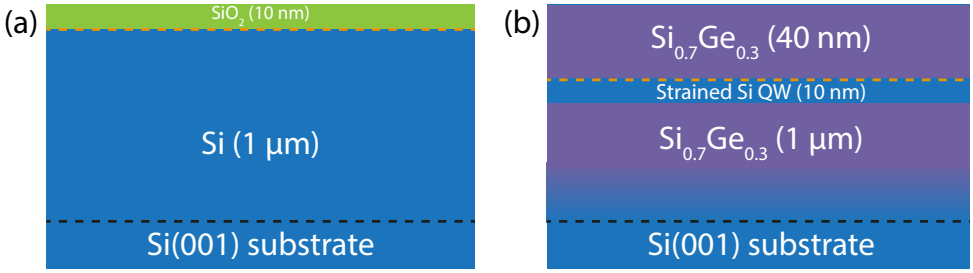

Figure 2.7: Schematic material stacks for (a) Si-MOS and (b) Si/SiGe. The orange dashed lines indicate the location of the 2DEG. (a) For Si-MOS, intrinsic silicon is grown on top of a Si(001) substrate, and a 10 nm-thick layer of SiO_2 is sacrificially grown. (b) For Si/SiGe, a buffer layer is grown on a Si(001) substrate. The schematic shows a linearly graded buffer layer (see main text) to reach the final Ge concentration of 30%. A strained Si quantum well (QW) followed by a $Si_{0.7}Ge_{0.3}$ barrier and a Si capping layer are grown on top of the buffer layer. All thicknesses are indications and the exact values can differ between substrates to obtain slightly different properties.

In Si-MOS devices, the quantum dots are only separated from the gates by a thin layer of silicon dioxide (SiO_2), with a typical thickness of 5-15 nm.[5] In Si/SiGe devices, the dots are formed in a buried Si quantum well (QW) at an epitaxial interface separated from the

[5] In a recent experiment on a sample with 30 nm SiO_2, Kim *et al.* [66] found very low critical and shallow trap densities around 9.0×10^{10} cm^{-2} and very high electron mobilities around 2.0×10^{4} cm^2/Vs.

heterostructure surface by a SiGe barrier layer with a typical thickness of 30-50 nm. The closer proximity of gates for Si-MOS offers the advantage of better control and it makes it easier to form the required small dots. However, the quantum dots in Si-MOS are formed at the interface with an amorphous oxide, most likely resulting in more disorder in the potential landscape and more charge noise. Consequently, quantum dots tend to form at unintended locations and direct control of the tunnel coupling via gate voltages in Si-MOS has only been shown very recently [67].

Another important difference between Si-MOS and SiGe is the valley splitting. In general, valley splitting is larger in Si-MOS than in SiGe devices, due to the sharper potential step at the Si/SiO_2 interface compared to the Si/SiGe interface, and the typically smaller quantum dots. Typical values for valley splitting are in the range 10–300 μeV and 200–1000 μeV for Si/SiGe and Si-MOS, respectively. In addition, valley splitting can be tuned by the vertical electric field via gate voltages, especially in Si-MOS [59].

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3

Device Fabrication and Experimental Setup

Nanofabrication is like cooking: you follow
the recipes and once in a while you burn something.

In this chapter, the development of an integration scheme for the reliable and reproducible fabrication of quantum dots in Si-MOS for spin qubit experiments, and the experimental setups are discussed.

3.1. FABRICATION OF SPIN QUBIT DEVICES IN SI-MOS

SPIN qubit devices can be fabricated from several different material systems that can differ in constituting materials as well as in dimensionality. A combination of silicon and germanium, for example, is used both in two-dimensional planer structures and one-dimensional nanowires. The work in this thesis focuses only on two-dimensional structures and is limited to group IV materials, but even then several possibilities remain.

This section presents the development of a fabrication scheme for silicon spin qubit devices, specifically in the planar silicon/silicon dioxide (Si-MOS) material system, with an overlapping gate structure that is inspired by work in other groups [1–4]. The overlapping gate structure makes it possible to achieve a smaller gate pitch compared to single-layer devices. This allows for the tight confinement potential that is required for quantum dots in silicon because of the larger effective mass of silicon compared to for example gallium arsenide.

First, the database used in fabrication, the wafers that form the starting point of the fabrication and the device design are briefly discussed. Next, the individual steps of the integration scheme are outlined, and finally some tips and tricks for fabrication are discussed.

3.1.1. DATABASE

To support reproducible fabrication, we make use of a fabrication database, QuTech SoloDB.[1] This database is a combined, centralized and digital version of different notebooks and logbooks, and makes it possible to keep track of all process steps (including all details) that have been applied to, or are planned for a specific sample. Differences between planned and actual parameters are also easily recorded. It makes it easier to log, look back at, search through and share with others what exactly has been done with a specific sample, especially the small details that tend to be easy to overlook and forget.

Furthermore, the SoloDB allows users to keep a record of their substrates and samples, offers a complete list of all available equipment in the Kavli and EKL cleanrooms, and aids in process development and monitoring for reliable and reproducible fabrication.

3.1.2. WAFERS

The Si-MOS material system, used for the fabrication in this section, was already introduced in Sec. 2.2.3. The wafers are provided by Intel Corporation and grown on industrial 300-mm substrates. A schematic of the specific material stack used here is shown in Fig. 3.1.

For the layer of purified silicon, silicon tetrafluoride (SiF_4) with natural isotope composition is purified to $^{28}SiF_4$ with a residual ^{29}Si concentration of 0.08%. Then, $^{28}SiF_4$ is reduced to isotopically enriched silane ($^{28}SiH_4$), which is used to deposit a ^{28}Si epilayer by chemical vapor deposition (CVD) in a state-of-the-art 300-mm fabrication line. Subsequently, 10 nm high-quality $^{28}SiO_2$ is formed by thermal processing at high temperature (as a result the ^{28}Si layer is slightly thinner than 100 nm). For these wafers, Sabbagh

[1] https://qtechserv.tnw.tudelft.nl/user/login A demo version is available at https://demo.solodb.net/user/login.

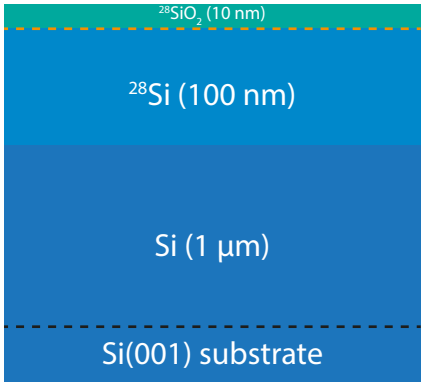

Figure 3.1: For the wafers used in this work, a layer of intrinsic silicon (1 µm) is grown on top of a high-resistivity Si(001) substrate, followed by 100 nm ^{28}Si (800 ppm residual ^{29}Si concentration). A 10-nm-thick layer of $^{28}SiO_2$ is sacrificially grown. The 2DEG is formed at the silicon/silicon dioxide interface as indicated by the orange dashed line.

et al. [5] measured a peak mobility and critical density of 9800 cm^2/Vs and 1.75×10^{11} cm^{-2}, respectively. More details and further characterization can be found in their work.

3.1.3. PREFAB

During the course of the last few years, steps have been taken to transfer the first steps of the fabrication process to the more automated cleanroom in the Else Kooi Lab (EKL) at the Delft University of Technology.[2] The equipment in this cleanroom allows for batch processing of full wafers. This easily allows for process splits and it speeds up the fabrication process, which both result in a faster feedback loop. The more automated fabrication is more reliable and reproducible. Furthermore, the EKL cleanroom is equipped with a dedicated silicon process line, which reduces contamination. This transfer process is out of the scope of this thesis, but some of the steps outlined below (tungsten markers, ohmic regions, ohmic contacts and platinum markers, and bond pad protection) are influenced by this transfer.

3.1.4. DEVICE DESIGN

We now briefly introduce the used gate design. The devices we fabricate consist of a one-dimensional array of four quantum dots with a pitch of ~100 nm (~50 nm gate pitch), and a sensor quantum dot opposite to this array. The device design consists of three overlapping gate layers that we refer to as the screening layer, accumulation and plunger layer, and barrier layer. In addition, the devices contain micromagnets on top of the gate layers. This design is schematically shown in Fig. 3.3(h).

The fabrication scheme presented here, naturally can be applied to other gate designs as well. As an example of its versatility, Fig. 3.7 shows a two-dimensional 3-by-3 array of quantum dots fabricated with the same integration scheme.

[2] https://www.tudelft.nl/en/eemcs/research/facilities/else-kooi-lab/

TEST STRUCTURES

In addition to the quantum dot devices, we include several structures on the chip that are dedicated for testing purposes, both in-line as well as end-of-line. In-line tests can be used to identify problems early on. In case an in-line test fails, one can decide to stop the fabrication for that chip, or solve the problem. This enables one to save valuable time by not working on a chip that is bound to fail. End-of-line tests serve to troubleshoot problems in the full fabrication process as well as to assess the (final) quality of the fabricated samples. Those test structures include:

- Dose tests for the fine gate structures to independently assess the correct dose.
- Overlapping fine gate structures (without the full fan-out, reducing the footprint) dedicated for TEM imaging.
- Transistors to test the quality and properties of the implants.
- Capacitors to test for leakage between all combinations of implants and gate layers, and to assess oxide quality.
- Transmission line (TLM) structures to determine contact resistance and resistivity for implants and metal layers.
- Hall bars for magnetotransport studies, as for example presented in Ref. [5].

DUMMIFICATION

To improve the quality of the lift-off of metal layers we include dummies in our designs. Dummies are isolated metal islands without any purpose in the device operation. Including them in the open areas of the lithography pattern for a metal layer to be lifted off, creates access holes in the metal layer for the lift-off solvent to reach the resist layer below more easily. Figure 3.2 shows the dummification in our devices.

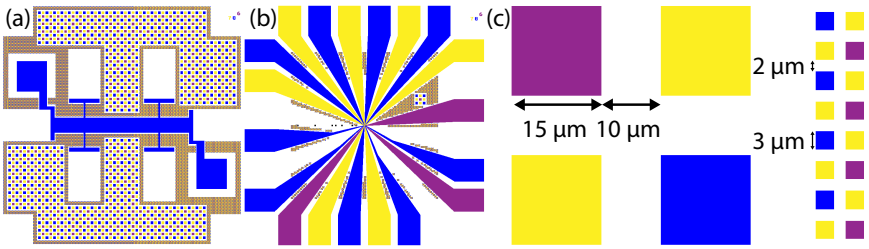

Figure 3.2: Dummification for (a) a Hall bar and (b) a quantum dot device with the design shown in Fig. 3.3(h). Only the screening (purple), accumulation and plunger (blue), and barrier (yellow) layers are shown. (c) Two levels of dummification are used: the first level consists of 15 µm squares with a distance of 10 µm between them, while the second level consists of 3 µm squares separated by 2 µm.

3.1.5. FABRICATION RECIPES

Starting from the wafers presented before, we fabricate planar, gate-defined Si-MOS quantum dot devices for spin qubit experiments in the Kavli Nanolab cleanroom of the Kavli Institute of Nanoscience in Delft.[3] The used integration scheme is outlined below and schematically shown in Fig. 3.3. Additionally, the detailed recipes of this integration scheme are presented in App. A.

Minor adjustments to account for differences in the material systems, allow this process to be applied to the other group IV material systems silicon/silicon germanium (Si/SiGe) and germanium/silicon germanium (Ge/SiGe) as well. In these material systems, a 2DEG is formed in a quantum well made from strained silicon and strained germanium, respectively. Applying this process to all three material systems has been done in Delft, demonstrating quantum dots that can be depleted to the last electron/hole in all of them [6]. This facilitates a fair comparison between spin qubit devices in different materials to come to a well-founded decision on the optimal material, which will be important for the future development of (silicon) spin qubits.

SURFACE TREATMENT

To achieve reproducible fabrication, we introduce surface treatment steps at several points in the process, just before performing a next step, in order to reset the surface and always start a new step from a similar state. The surface treatment consist of UV ozone exposure, a clean in acetone followed by a rinse in isopropanol, or a combination of these two.

TUNGSTEN MARKERS

Only the metals aluminum and tungsten are allowed in the implanter used for ion implantation. Therefore a simple and quick integration scheme with sputtering of tungsten (W) is used for a first set of markers. These markers are fabricated by means of electron beam lithography, but in principle photolithography can be used as well. However, the quality of markers made from sputtered tungsten is not optimal and degrades during the high-temperature activation anneal, so after this anneal step a new set of high-quality markers is fabricated.

OHMIC REGIONS

Ohmic (metallic) regions in the semiconductor material are created to serve as electron reservoirs, and to be able to perform electrical transport measurements on the devices. These ohmic regions are created by n-type ion implantation, followed by an activation anneal. Phosphorous ions are implanted in a TLC Varian E500 HP. We use simulations of the implant profile to determine the energy and dose of the implantation.[4] Subsequently, the wafer is annealed in forming gas in a SSI Solaris 100. The activation anneal at 1000°C is the highest-temperature step in the fabrication process.

[3] https://www.tudelft.nl/en/tnw/about-faculty/departments/quantum-nanoscience/kavli-nanolab-delft/ and http://www.kavli.tudelft.nl/

[4] https://cleanroom.byu.edu/implantcal

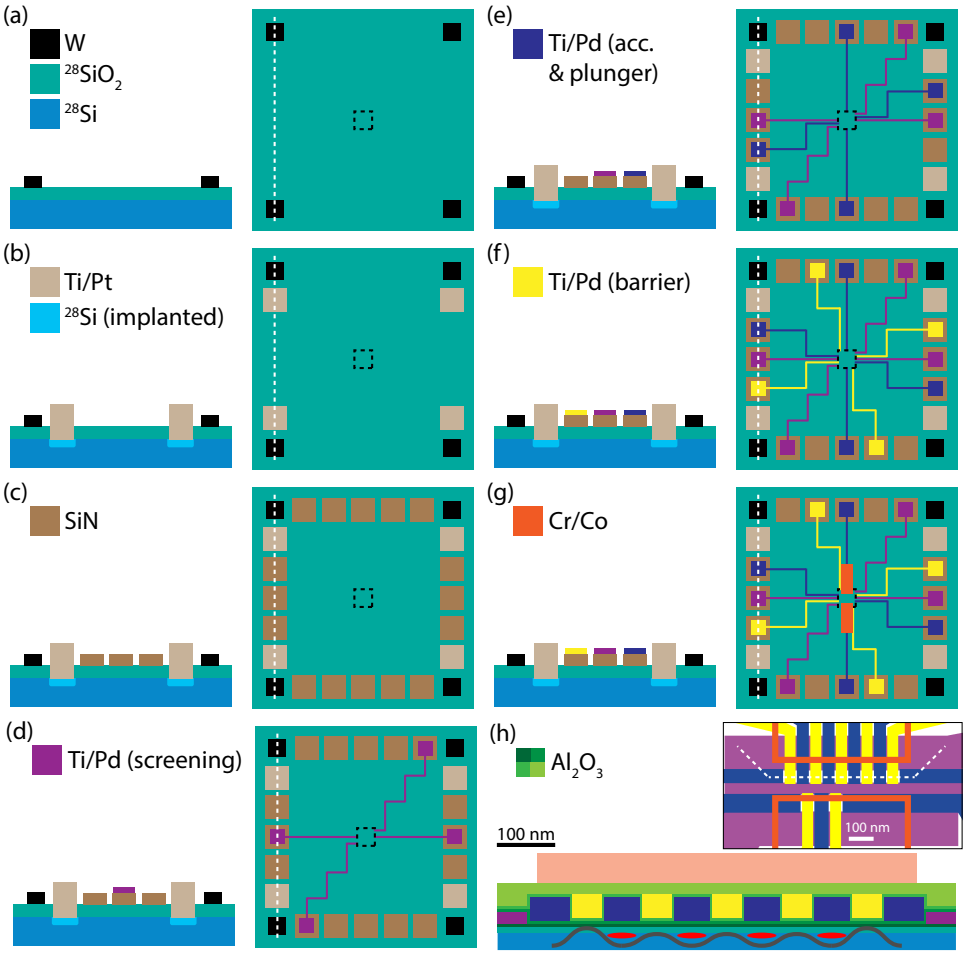

Figure 3.3: (a-g) Schematics (not to scale and not showing all gate electrodes) showing the different steps of the integration scheme in side (left) and top (right) view. The cross sectional view on the left is along the dashed line in the top view. Subfigures show the fabrication of (a) tungsten markers, (b) ohmic regions and contacts, and platinum markers, (c) bond pad protection, (d) the screening gate layer, (e) the accumulation and plunger gate layer, (f) the barrier gate layer, and (g) micromagnets. ALD layers that electrically isolate the gate layers from each other are omitted for clarity. The dashed box in the top view indicates the active region of the device and has been left empty for clarity, because the structures are to small. (h) Cross sectional view (roughly to scale) of the active region of the device along the dashed line in the top view shown in the inset. The outer two slightly wider blue gates are the accumulation gates that extend further to the implanted regions to connect the active region to the implanted electron reservoirs. Not in all devices the bottom Al_2O_3 layer (darkest green) is present. The quantum dots are intended to form at the positions indicated by red ellipses and separated from each other by tunnel barriers, as sketched by the grey line that indicates the potential landscape. Note that the micromagnets are actually not along the line cut.

OHMIC CONTACTS AND PLATINUM MARKERS

The be able to wire bond to the ohmic regions, platinum bond pads connecting the implanted areas are fabricated. First, a window in Allresist AR-P 6200 (CSAR62)[5] is created by means of electron beam lithography to expose part of the implanted area. Then, the silicon dioxide layer is etched in buffered hydrofluoric acid (BHF). After a rapid transfer to the deposition chamber to prevent natural oxidation of the exposed silicon, a 5-nm thick titanium (Ti) sticking layer and 55 nm of platinum (Pt) are deposited to serve as bond pads.

In the same step, high-quality $20\times20\ \mu m^2$ Ti/Pt markers for the alignment of the electron beam lithography patterns of all subsequent layers are fabricated. The combination of CSAR62 with Ti/Pt proved to result in high-quality markers with straight edges and clean lift-off.

BOND PAD PROTECTION

To prevent the wire bonds to punch through the thin silicon dioxide layer, causing shorts between the metallic gates and the substrate, thick dielectric pads (150 nm of silicon nitride, SiN) are fabricated in the bond pad regions by sputtering on top of a bilayer resist stack consisting of MMA/MAA Copolymer[6] and Allresist AR-P 6200 (CSAR62).[7] In subsequent fabrication steps, metal bond pads of $\sim100\times100\ \mu m^2$ connected to the gate electrodes in the active region of the device are deposited on top of the SiN pads. After fabrication, the wire bonds connecting the sample chip to the PCB are made to these metal bond pads.

ALUMINUM OXIDE BLANKET

In order to minimize the possibility of leakage between the substrate and the gate electrodes, a 10-nm thick layer of aluminum oxide (Al_2O_3) is grown over the entire substrate. However, recent work shows the presence of Al_2O_3 to result in more charge noise [7]. In addition, by removing the Al_2O_3 and exposing the silicon dioxide (SiO_2) in the active device area of $20\times20\ \mu m^2$, the gate electrodes are closer to the quantum dots and have a stronger effect. For this purpose we use a selective etch of Al_2O_3 vs. SiO_2. Both phosphoric acid (H_3PO_3) and Transene Aluminum Etchant Type D[8] can be used for this purpose. There is no clear advantage for one of the two, but currently Transene D is used due to availability. This etch is not performed for every device and thereby leaves an additional dielectric layer below all fine gates (darkest green in Fig. 3.3(h)) in some of the devices. This further reduces the possibility of gate leakage in those devices.

GATE ELECTRODES

To fabricate palladium gate electrodes on top of the sample, we pattern Allresist AR-P 6200 (CSAR62)[9] to achieve small gate structures by means of electron beam lithography in a Raith EBPG system (5000+ or 5200, 100 kV). After resist development, an ozone

[5] https://www.allresist.com/csar-62-ar-p-6200/
[6] http://microchem.com/pdf/PMMA_Data_Sheet.pdf
[7] See footnote 5.
[8] https://transene.com/aluminum/
[9] See footnote 5.

treatment is performed in a Bioforce ProCleaner 220 to clean resist residues at the bottom of the patterns that are defined in the resist to improve sticking of the metal to the oxide layer below. A thin titanium (Ti) sticking layer and palladium (Pd) are deposited by electron beam evaporation in a Temescal FC2000. After lift-off, the sample is treated in ozone to remove organic residues. Then, the sample is annealed to allow for reflow of the metal, thereby improving the quality of the gate structures [6].

Previous work used aluminum as gate metal [1], but palladium's smaller grains allow for finer and more uniform gate structures [4]. We have investigated several other metalizations (i.e. Al, Ti, Ti/Pt, Cr/Pd), but found Ti/Pd to give the best structures in terms of line edge roughness and clean lift-off, which both prevent shorts between gate electrodes, and overall yield. In addition, we experimented with low-temperature (77 K) as well as higher-rate deposition of aluminum. Both processes improve the structures, which we attribute to the reduced heating of the sample during deposition, but for convenience (low-temperature deposition is more complicated and takes more time, so has to be well-planned) we only implemented a higher deposition rate (2 Å/s instead of 0.5 Å/s).

Anisole is used as lift-off solvent, because it gives the smoothest structures with highest yield, but previously N-methyl-2-pyrrolidone (NMP) has been used as well. We also experimented with lift-off in NMP in combination with Triton X,[10] tetramethylammonium hydroxide (TMAH) and Triton X, and TMAH, potassium hydroxide (KOH) and Triton X, but all three combinations reduce the lift-off quality and add complexity to the process.

The previously used aluminum gate electrodes naturally oxidize, which creates an isolating dielectric layer between subsequent gate layers without the need for additional process steps [1]. This can be enhanced by thermal treatment, for example on a hotplate, or in a plasma. However, palladium does not oxidize, so to electrically isolate consecutive metal layers from each other, a 7-nm-thick aluminum oxide (Al_2O_3) layer is deposited after each gate layer by means of atomic layer deposition (ALD) in a Picosun R-200 Advanced. The dielectric strength of our Al_2O_3 has been determined to exceed 6 MV/cm [6].

The combination of metal and a dielectric isolation layer allows for several overlapping gate layers, which are fabricated by repeating the steps outlined above. We have fabricated devices containing up to three gate layers of which an example is shown in Fig. 3.4. If layers have to go over others layers, these later layers are made slightly thicker to ensure electric contact at the climbing edges.

MICROMAGNETS AND STRIPLINE

To perform spin manipulation in silicon devices, usually an additional structure is necessary, because there generally is no natural mechanism that is strong enough for spin driving. As discussed in Sec. 2.2.2, there are two possible methods for spin driving: ESR by a stripline and EDSR with micromagnets.

The design shown in Fig. 3.3(h) contains micromagnets, but we also fabricate devices with another gate design including a stripline to be able to explore the (dis)advantages of the two approaches in devices fabricated by a similar process. For devices containing

[10] https://www.labchem.com/tools/msds/msds/LC26280.pdf

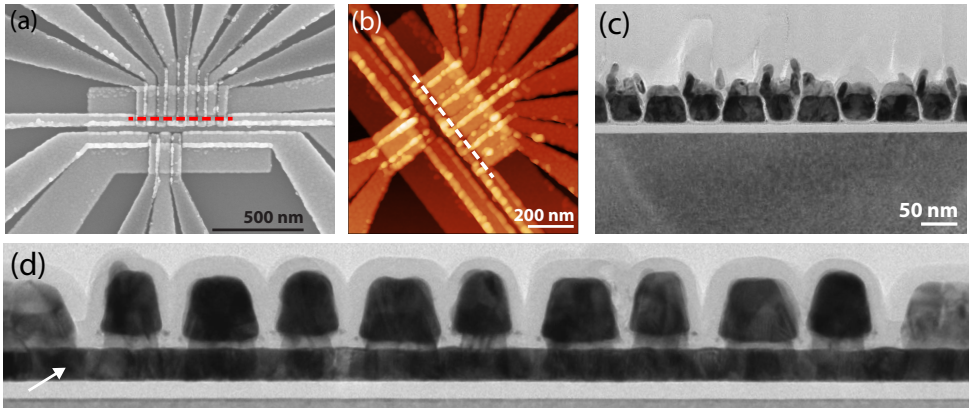

Figure 3.4: (a) Scanning electron micrograph, (b) atomic force micrograph and (c) transmission electron micrograph (image credit: Intel Corporation) of the active region of the same device after fabrication of the gate electrodes. The cross section shown in (c) is along the dashed lines in (a) and (b). (d) Transmission electron micrograph (image credit: Intel Corporation) of the active region of a device with an optimized design (reduced gate overlap) giving smoother structures. The cross section is slightly above the dashed line shown in (a) and therefore also shows the screening gate layer (indicated by the white arrow), which is not visible in (c).

micromagnets, an additional, slightly thicker layer of Al_2O_3 is deposited by means of ALD after the last metal gate layer.

Micron-sized magnets are fabricated from cobalt (Co) with a thin chromium (Cr) sticking layer, both deposited by electron beam evaporation. We develop a bilayer resist stack consisting of MMA/MAA Copolymer[11] and Allresist AR-P 6200 (CSAR62)[12] with orthogonal developers to be able to accurately control the undercut profile of the resist. Figure 3.5 shows the obtained resist profile and the resulting micromagnet structure. High-quality micromagnet structures are obtained as result of the combination of a bilayer resist with undercut profile and a sufficiently thick bottom layer resist compared to the micromagnet thickness (targeted at 335 nm and 205 nm, respectively).

Striplines are fabricated from aluminum or niobium titanium nitride (NbTiN), which both are superconducting at low temperatures, by electron beam evaporation and sputtering, respectively. A single-layer resist stack is used for stripline fabrication.

PACKAGING

To be able to wire bond to the metal layers that are covered by the Al_2O_3 gate isolation layers, the oxide has to be etched away on the Ti/Pt ohmic contacts, and in the contact areas for the Ti/Pd gate electrodes on top of the SiN pads. For this purpose, a selective etch of Al_2O_3 vs. both Pd and Pt by either phosphoric acid (H_3PO_3) or Transene Aluminum Etchant Type D[13] is performed. There is no clear advantage for one of the two, but currently Transene D is used due to availability.

The sample is then covered by a protective layer of photoresist and diced in a Disco DAD3220. The resist is removed and the sample is cleaned in ozone, before a final anneal

[11] See footnote 6.
[12] See footnote 5.
[13] See footnote 8.

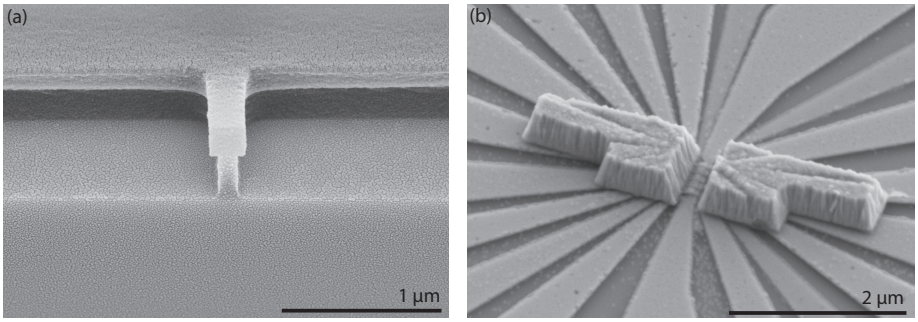

Figure 3.5: Scanning electron micrographs showing (a) the profile of the bilayer resist stack for micromagnet fabrication after resist development and (b) the micromagnet structure on top of the gate structure. The undercut profile shown in (a) can be accurately controlled, because we use resists with orthogonal developers.

in a hydrogen atmosphere is performed in an Ultratech Fiji to cure fabrication induced defects [1, 8].

Finally, we glue the sample to a printed circuit board (PCB) and attach bond wires to the metal bond pads with a Westbond wire bonder or a Bontec wire bonder. Figure 3.6 shows a sample bonded to a PCB for measurements.

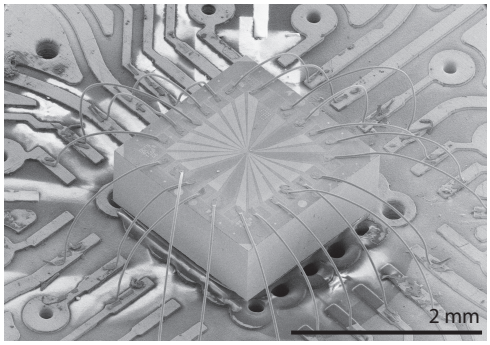

Figure 3.6: A 2 mm × 2 mm sample glued on a printed circuit board. Wire bonds connect the bond pads on the sample to the lines on the PCB.

3.1.6. TIPS AND TRICKS

AFM SCREENING

To prevent unnecessary wire bonding and low-temperature measurements, it is good practice to screen devices before mounting them on a PCB. In the past, we and others have refrained from scanning electron microscopy (SEM) for device screening, because of the known damage the electrons used for imaging cause to the devices, reducing their performance [8–10]. As an alternative, although the resolution is usually not as good as for SEM, we started using atomic force microscopy (AFM) for preliminary device screening, which allows to discriminate between structurally intact and damaged devices.

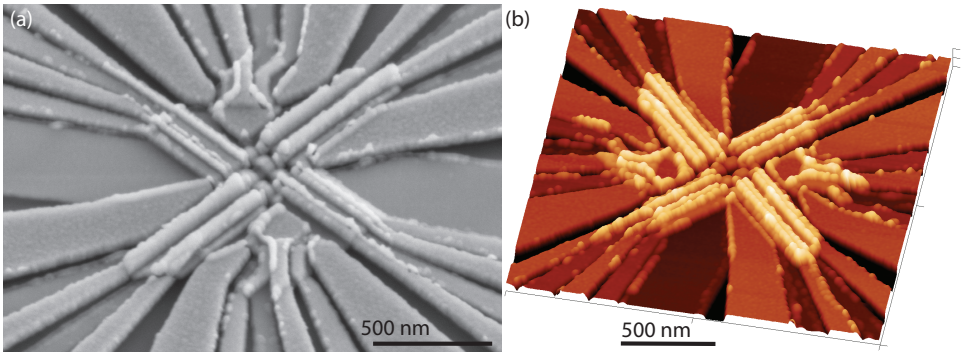

Figure 3.7: (a) Scanning electron micrograph and (b) atomic force micrograph showing an example of a two-dimensional array of 3-by-3 quantum dots fabricated with the same integration scheme, demonstrating its versatility.

ELECTROSTATIC DISCHARGE PROTECTION

We have implemented several measures to protect our sensitive devices against electrostatic discharge (ESD). In our devices, ESD is caused by a large potential difference between the gate electrodes that in the active area of the device are only separated from each other by a few nanometers of dielectric. A discharge of this potential difference through dielectric breakdown is accompanied by a large current flow through the narrow gates with relatively high resistance and therefore results in melting and/or exploding of the fine gate structures.

To prevent ESD to happen, build up of a potential difference should be circumvented as much as possible and any potential difference should be able to equilibrate safely. In this respect, the measures we have taken in our lab are:

- Samples are stored and carried in ESD-safe gel packs[14] and anti-static bags[15] as much as possible.
- While handling samples, users are grounded as much as possible through wrist straps[16] and heel straps,[17] via grounding cords[18] and earth plugs.[19] Straps should be tested regularly.[20]
- Surfaces and equipment used for sample handling should be grounded directly, or via grounding mats on tables[21] and floors.[22]

[14] AD-23C-00-ER4 from Gel-pak ordered through TELTEC.
[15] https://nl.farnell.com/multicomp/013-0003/static-shield-bag-zip-4x6-pk100/dp/1687798
[16] https://nl.farnell.com/multicomp/066-0055/set-esd-wristband-10mm-1meg/dp/1503191
[17] https://nl.farnell.com/scs/hgc1m-ec/heel-grounder/dp/1684259
[18] https://nl.farnell.com/multicomp/067-0016/earth-grounding-cord-coiled-10/dp/1503192
[19] https://nl.farnell.com/multicomp/mc0700016/bonding-plug-euro-2stud-1mohm/dp/2425510
[20] https://nl.farnell.com/vermason/222562/wrist-strap-tester-5-led/dp/2409568
[21] https://www.conrad.nl/p/bjz-c-184-105p-103-esd-matset-grijs-l-x-b-900-mm-x-600-mm-incl-aardingsarmband-incl-aardingsstekker-incl-aarding-189411
[22] https://nl.farnell.com/multicomp/082-0030f/esd-bench-mat-600x1200mm-beige/dp/1687905

- An ionizer[23] with collimator and auto emitter clean (options M and E) is used to neutralize charges in the air, especially during wire bonding.
- A charge detector[24] is used to check the environment for the presence of static charges.
- To safely discharge any static charge, the PCB is grounded through a large resistor (~1 MΩ) to prevent large current peaks.

There are possibilities to build in ESD protection (in the device design), but we did not (systematically) implement those:

- Shorting the gate electrodes in fabrication to keep them all at the same potential. The connection between the gates is only broken after wire bonding by scratching the metal.
- A low-density implant that is conductive at room temperature below the bond pads gives the same effect. At low temperature the dopants freeze out and the connection is broken. The disadvantage is that this prevents room temperature testing.
- Resistors that freeze out at low temperature at the PCB between the bond pads and ground also have the same effect. Room temperature testing is not possible in this case.

3.2. EXPERIMENTAL SETUP

THE experiments presented in Ch. 4 and Ch. 5 are performed in a dilution refrigerator, and controlled and measured via specialized electronics. Both will be briefly discussed in what follows.

3.2.1. DILUTION REFRIGERATOR

The energy scales associated with the quantum effects we want to study and exploit are small, so very low temperatures are required such that the thermal energy does not prevent the observation of these effects. Therefore, the experiments presented in this thesis are carried out in dilution refrigerators with a base temperature of 10–30 mK.

The experiments in Ch. 4 are performed in a Bluefors LD400 and the experiments in Ch. 5 are performed in an Oxford Kelvinox 300. The former is a dry cryostat based on pulse-tube cooling to reach 4 K, while the latter is a wet cryostat in which liquid helium is used for the first cooling step. Subsequently, the cooling mechanism for the two systems is the same, based on a dilution unit, and in several steps eventually the base temperature is reached at the mixing chamber plate where the PCB containing the sample is mounted.

The Bluefors LD400 is equipped with a single-axis 3 T superconducting magnet, while the Oxford Kelvinox 300 has a 3 T two-axis vector magnet, which can sustain a maximum field of 7 T along the main axis if the other axis is at 0 T.

[23] https://technology-ionization.simco-ion.com/products/ionizing-blowers/critical-environment/5802i-benchtop-ionizing-air-blower
[24] https://technology-ionization.simco-ion.com/products/instrumentation/775-electrostatic-fieldmeter

3.2.2. ELECTRONICS

The room temperature electronics used to control the experiments can be divided in a DC and an AC part.

DC ELECTRONICS

The gate voltages to set the potential landscape in our devices are supplied by home-built low-noise electronics.[25] The IVVI rack runs on batteries and is completely isolated from the mains to reduce (50 Hz) noise. For the same reason, the communication with the control-and-measurement computer is via an optical cable. Biasing of the gate electrodes is done via digital-to-analog converters (DACs) with a range of -4–0 V, -2–2 V, or 0–4 V, and with a resolution of ~60 μV. The DAC module is designed to have low noise and drift, measured to be 5 μVpp in a one hour time span. The DAC outputs are connected to the gate electrodes via a matrix module, a 24-pin Fischer cable and wire looms inside the dilution refrigerator, while being filtered at several stages along the way.

In addition to DC biasing, the IVVI rack offers a wide range of modules for tailored applications. For example, in Ch. 4 the IVVI rack is used in combination with lock-in techniques for spin readout and in Ch. 5 we perform spin readout via DC measurements with the IVVI rack.

RF CONTROL ELECTRONICS

Qubit operations are performed by applying pulses to the sample that are generated by commercial high-frequency electronics. Fast gate voltage pulses to change chemical potentials and tunnel coupling are applied by arbitrary waveform generators (AWGs). For the experiments in this thesis Tektronix 5014C AWGs are used.

Single-qubit operations are performed via microwave excitation with a typical frequency of 10–20 GHz. In the experiments in Ch. 5 we use Keysight E8267D vector microwave sources for this purpose.

Both fast voltage pulses and microwaves are applied via coaxial cables that are filtered and thermally anchored at several stages inside the dilution refrigerator to reduce noise.

[25] http://qtwork.tudelft.nl/~schouten/

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4

Spin Lifetime and Charge Noise in Hot Silicon Quantum Dot Qubits

We investigate the magnetic field and temperature dependence of the single-electron spin lifetime in silicon quantum dots and find a lifetime of 2.8 ms at a temperature of 1.1 K. We develop a model based on spin-valley mixing, and find that Johnson noise and two-phonon processes limit relaxation at low and high temperature, respectively. We also investigate the effect of temperature on charge noise and find a linear dependence up to 4 K. These results contribute to the understanding of relaxation in silicon quantum dots and are promising for qubit operation at elevated temperatures.

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4.1. INTRODUCTION

ELECTRON spins in semiconductor quantum dots [1] are considered to be one of the most promising platforms for large-scale quantum computation. Silicon can provide key assets for quantum information processing, including long coherence times [2, 3], high-fidelity single-qubit rotations [2, 3] and two-qubit gates [4–6], which have already enabled the demonstration of quantum algorithms [6]. Quantum dots based on silicon metal-oxide-semiconductor (Si-MOS) technology provide additional prospects for scalability due to their compatibility with conventional manufacturing technology [7, 8], which opens the possibility to co-integrate classical electronics and qubits on the same wafer to avoid an interconnect bottleneck [9, 10]. However, control electronics will introduce a power dissipation that seems incompatible with the available thermal budget at temperatures below 100 mK, where qubits currently operate. Understanding and improving the robustness of qubits against thermal noise is therefore crucial, while operating qubits beyond 1 K could entirely resolve this challenge.

Spin relaxation and charge noise are two essential metrics for quantum dot qubits. While the spin lifetime T_1 can be of the order of seconds in silicon quantum dots [11–13], exceeding by orders of magnitude the dephasing time T_2^* [2], it is presently unclear how T_1 will be affected by temperature and whether it will become the shortest timescale for quantum operations at elevated temperatures. Spin qubits are also sensitive to charge noise, and electrical fluctuations can reduce qubit readout and control fidelities. The temperature dependence of these two parameters is therefore vital in evaluating the prospects for hot spin qubits.

Here, we investigate in detail the temperature dependence of spin relaxation and charge noise of a Si-MOS quantum dot. We construct a model based on direct and two-phonon transitions including all spin and valley states of the lowest orbital. The model provides good agreement with the experiments and we conclude that while at low temperatures T_1 is limited by Johnson noise, probably originating from the two-dimensional electron gas (2DEG) channels present in the device, two-phonon processes determine the relaxation rate above 200 mK. Based on our results we predict how the spin lifetime can be improved by decreasing the magnetic field and increasing the valley-splitting energy. Furthermore, we investigate the charge noise and measure a rather weak temperature dependence.

4.2. DEVICE AND EXPERIMENTAL DETAILS

FIGURE 4.1(a) shows a scanning electron microscope (SEM) image of a quantum dot device, realized in isotopically enriched silicon (^{28}Si), identical in design to the one measured. Figure 4.1(b) presents the charge stability diagram of the device, showing charge transitions originating from three quantum dots, and we deplete one quantum dot to the last electron. From the temperature dependence of the transition width we extract a lever arm $\alpha_{P1} = 0.12$ eV/V (see Sec. 4.7.3). We tune the tunnel rate between the quantum dot and the reservoir by controlling the gate P2 (see Fig. 4.1(c)), which moves the position of the quantum dot thereby changing the distance to the reservoir. During the experiment, since the DC signal of the sensing dot is filtered with a 2-kHz low-pass filter, the dot-reservoir tunnel rate is set to approximately 700 Hz.

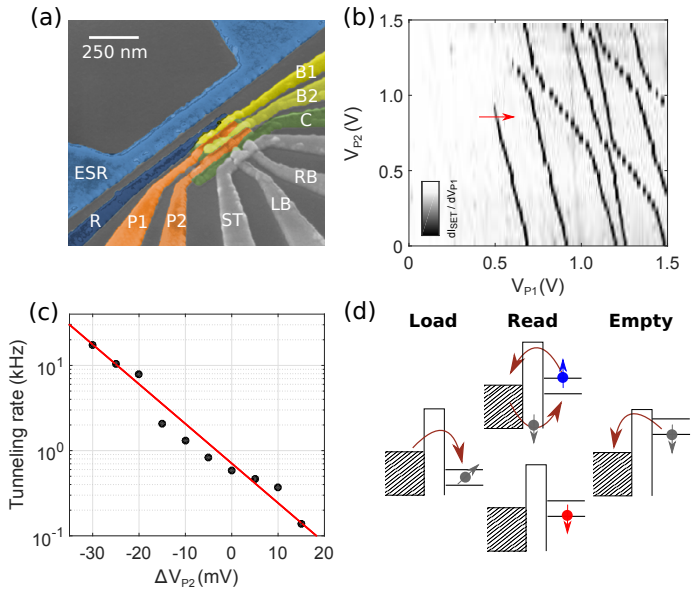

Figure 4.1: (a) Scanning electron microscope image of a device identical to the one measured. R is the reservoir gate, P1, P2, B1 and B2 are the plunger gates, and C confines the electrons in the dots. LB and RB are the left and right barrier of the quantum dot used for sensing, and ST is used both as top gate and reservoir. The ESR line can be used for spin manipulation. (b) Charge stability diagram of the device measured via a double lock-in technique [14] (see Sec. 4.7.3). The transition lines, due to the different slopes, can be attributed to three coupled quantum dots. The red arrow shows the (0→1) charge transition relevant for the experiment. (c) Tunneling rate between the dot and the reservoir as a function of V_{P2}. $\Delta V_{P2} = 0$ corresponds to the value set during the experiment. The red line is an exponential fit. (d) Pulsing sequence used to perform single-shot readout of the electron spin [15] in the case $E_z < E_{vs}$. Above the valley splitting there is also an intermediate level between the ground and excited spin state, corresponding to the spin-down state of the excited valley.

As shown in Fig. 4.1(d), we measure the spin lifetime by applying a three-level voltage pulse to the gate P1, while monitoring the DC current of the sensing dot. First, we inject an electron into the quantum dot, we read out the spin state, and we finally empty the quantum dot [15]. An additional level is added to the pulse after the empty phase in order to cancel out any DC offset. We measure the spin-up fraction as a function of load time and extract T_1 by fitting the data with an exponential decay.

4.3. EFFECT OF MAGNETIC FIELD ON SPIN RELAXATION

THE measured T_1 as a function of magnetic field (applied in the [010] direction) is plotted in Fig. 4.2(b) and the temperature dependence for three different magnetic fields is shown in Figs. 4.3(a-c). Thermal broadening of the reservoir limits the experimentally accessible regime. At base temperature (fridge temperature < 10 mK, electron temperature 108 mK, see Sec. 4.7.3) we measure a maximum T_1 of 145 ms at $B_0 = 1$ T. We find that even when increasing the temperature to 1.1 K, T_1 is 2.8 ms. This is more than an order of magnitude larger than the longest T_2^* reported in silicon quantum dots [2].

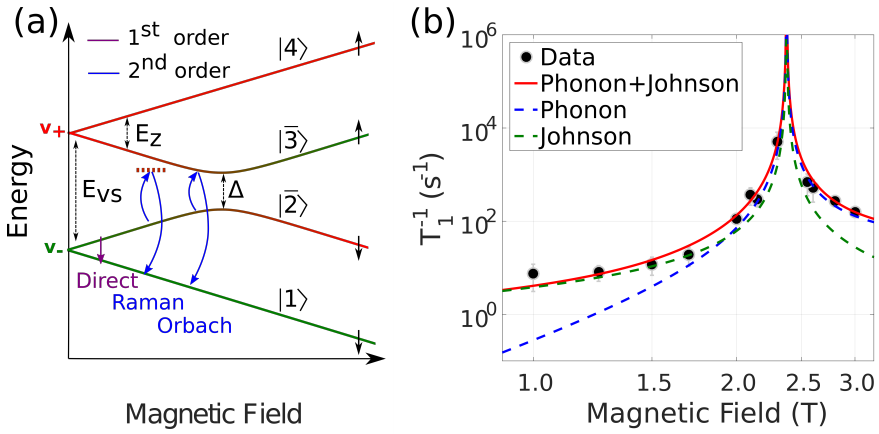

Figure 4.2: (a) Energy levels in a silicon quantum dot, showing both valley and spin degrees of freedom. As an example, the transition $\Gamma_{\bar{2}1}$ is sketched in first order, and in second order via virtual and resonant transitions. (b) Relaxation rate as a function of magnetic field. The fittings include contributions from Johnson and phonon mediated relaxation obtained through the model explained in the main text. From the fittings of the magnetic field and temperature dependence we extract $E_{vs} = 275$ μeV, $\Gamma_0^J(E_{vs}/\hbar) = 2\times10^{-12}$ s, $\Gamma_0^{ph}(E_{vs}/\hbar) = 6\times10^{-12}$ s and $\Delta = 0.4$ neV.

In order to understand the magnetic field and temperature dependence of the relaxation rate, we need to consider the mixing between spin and valley. In silicon the four lowest spin-valley states are [16]: $|1\rangle = |v_-,\downarrow\rangle$, $|2\rangle = |v_-,\uparrow\rangle$, $|3\rangle = |v_+,\downarrow\rangle$, $|4\rangle = |v_+,\uparrow\rangle$ (see Fig. 4.2(a)). In presence of interface disorder, spin-orbit interaction can couple states with different valleys and spins, introducing a channel for spin relaxation [13]. This leads to the eigenstates $|1\rangle, |\bar{2}\rangle, |\bar{3}\rangle, |4\rangle$, where:

$$|\bar{2}\rangle = \left(\frac{1-a}{2}\right)^{1/2}|2\rangle - \left(\frac{1+a}{2}\right)^{1/2}|3\rangle, \tag{4.1}$$

$$|\bar{3}\rangle = \left(\frac{1+a}{2}\right)^{1/2}|2\rangle + \left(\frac{1-a}{2}\right)^{1/2}|3\rangle. \tag{4.2}$$

Here we have $a = -(E_{vs}-\hbar\omega_z)/\sqrt{(E_{vs}-\hbar\omega_z)^2+\Delta^2}$, where Δ is the splitting at the anticrossing point of the states $|2\rangle$ and $|3\rangle$, E_{vs} is the valley splitting and $\hbar\omega_z$ the Zeeman energy. In the presence of electric fields, the electrons in the excited states $|\bar{2}\rangle$ and $|\bar{3}\rangle$ can relax to the ground state $|1\rangle$, because they are in an admixture of spin and valley states. We define a relaxation rate Γ_{sv}, corresponding to $\Gamma_{\bar{2}1}$ and $\Gamma_{\bar{3}1}$ before and after the anticrossing, respectively. The resulting expression is [17]:

$$\Gamma_{sv} = \Gamma_{v_+v_-}(\omega_z)F_{sv}(\omega_z), \tag{4.3}$$

where $\Gamma_{v_+v_-}$ is the pure valley relaxation rate and $F_{sv}(\omega_z) = (1-|a(\omega_z)|)$. When $E_{vs} = E_z$, the function F_{sv} peaks and the spin relaxation equals the fast pure valley relaxation [13]. From the location of this relaxation hot spot we determine a valley splitting E_{vs} of 275 μeV, comparable with values reported in other works [2].

Possible sources of electrical noise include $1/f$ charge noise, Johnson noise and phonon noise. We measure small values for charge noise (see Fig. 4.4) and thus neglect its contribution, further justified by the high frequencies of 20–100 GHz, associated with the Zeeman energies studied here ($1\,\mathrm{T} < B_0 < 3\,\mathrm{T}$). We also neglect the Johnson noise coming from the circuits outside the dilution refrigerator since all room temperature electronics are well filtered. The most relevant of these noise sources is the arbitrary waveform generator used to apply voltage pulses. However, the corresponding lines are attenuated by 12 dB and have an intrinsic cut-off frequency of 1 GHz, making the noise in the 20–100 GHz range negligible. Another possible source of Johnson noise is the resistive 2DEG, which generates electric field fluctuations that have a capacitive coupling to the quantum dot. In the present device, the main contribution is likely due to the 2DEG underneath the reservoir gate, which is in close proximity to the quantum dot.

Thus, the most relevant contributions are Johnson noise and phonons. The pure valley relaxation for these two cases is given by [13, 17]:

$$\Gamma^{J}_{v_+ v_-}(\omega) = \Gamma^{J}_{0} \cdot \left(\frac{\omega}{\omega_{vs}}\right)[1 + 2n_b(\hbar\omega, k_\mathrm{B}T)], \tag{4.4}$$

$$\Gamma^{ph}_{v_+ v_-}(\omega) = \Gamma^{ph}_{0} \cdot \left(\frac{\omega}{\omega_{vs}}\right)^5[1 + 2n_b(\hbar\omega, k_\mathrm{B}T)], \tag{4.5}$$

where $\hbar\omega$ is the energy difference between the two states, $\omega_{vs} = E_{vs}/\hbar$ and n_b is the Bose-Einstein distribution. The two contributions can be distinguished by the different magnetic field dependence that follows from $\omega_z F_{sv}(\omega_z)$ in the case of Johnson noise and from $\omega_z^5 F_{sv}(\omega_z)$ for phonons. As shown in Fig. 4.2(b) the magnetic field dependence of T_1 at base electron temperature can be explained in terms of Johnson mediated relaxation dominant at low fields, and a phonon contribution, mainly relevant for $\hbar\omega_z > E_{vs}$.

4.4. EFFECT OF TEMPERATURE ON SPIN RELAXATION

We now turn to the temperature dependence, shown in Figs. 4.3(a-c). As shown in Eqs. 4.4 and 4.5, the temperature dependence is the same to first order for phonon and Johnson noise and given by $1 + 2n_b(\hbar\omega_z, k_\mathrm{B}T)$. If $\hbar\omega_z \gg k_\mathrm{B}T$ spontaneous phonon emission dominates and the relaxation rate is temperature independent, while for $\hbar\omega_z \ll k_\mathrm{B}T$ it increases linearly with temperature. The relaxation rates caused by first-order processes are shown by the blue lines in Figs. 4.3(a-c), which fit the low temperature region of the plots. However, the same processes cannot justify the rapid decrease of T_1 measured at higher temperatures. In order to explain the full temperature dependence we also need to take into account two-phonon processes.

As depicted in Fig. 4.2(a), these transitions happen in a two-step process via intermediate states. These intermediate transitions can be energy-conserving and energy non-conserving (virtual) processes, since energy must be conserved only between the initial and the final state. We obtain a two-phonon process by expanding the spin-phonon interaction in second-order perturbation theory [18]:

$$\Gamma^{(2)}_{if} = \frac{2\pi}{\hbar}\left|\sum_k \frac{V_{fk}V_{ki}}{E_i - E_k + \frac{1}{2}i\hbar\Gamma_k}\right|^2 \delta(E_i - E_f), \tag{4.6}$$

where V_{fk}, V_{ki} are the matrix elements between the states and $1/\Gamma_k$ is the lifetime of the intermediate state, which depends on all first-order processes between k and the other states. The square of the matrix elements is proportional to the valley relaxation rate $\Gamma_{v_+ v_-}$. Relaxation through Johnson noise can also be expanded in second-order perturbation theory, however the temperature dependence is much weaker (see Sec. 4.7.2) and its contribution will therefore be neglected.

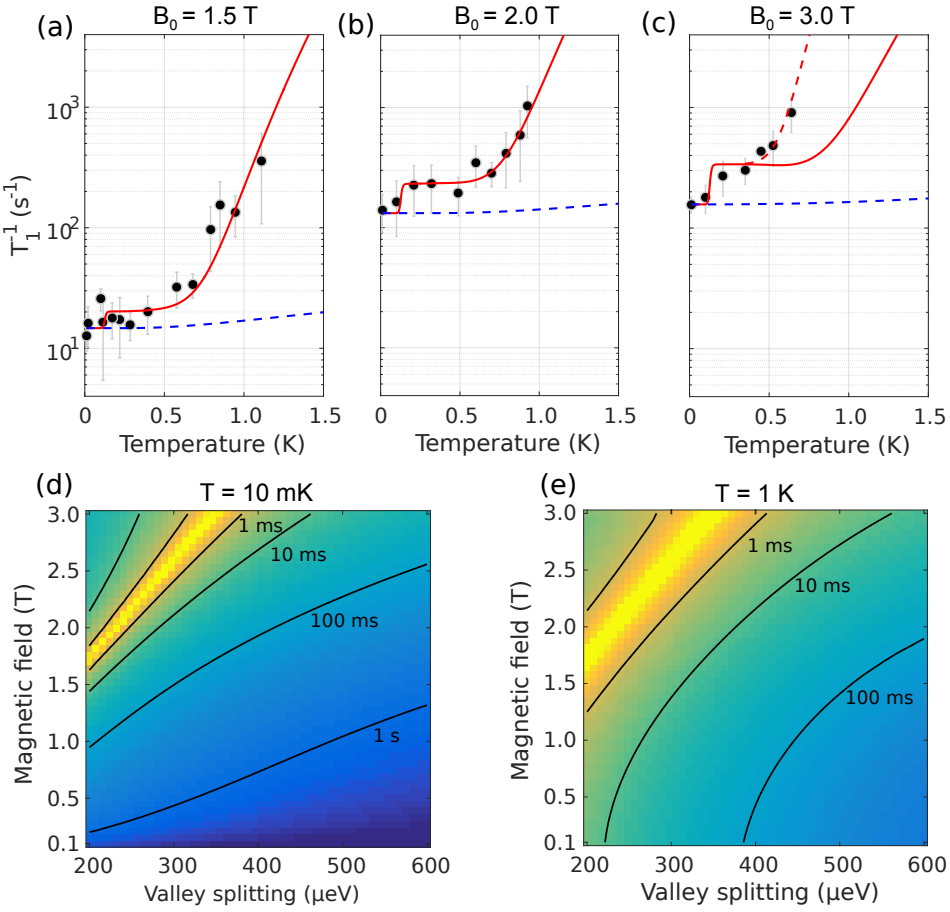

Figure 4.3: (a-c) Temperature dependence of the relaxation rate at (a) B_0 = 1.5 T, (b) 2 T and (c) 3 T. The red solid lines are fits taking into account Johnson and phonon noise in first and second order. The red dashed line includes possible contributions coming from the coupling with the excited orbital states. First-order processes are shown in the dashed blue lines. (d,e) Relaxation rate as a function of magnetic field and valley splitting for (d) T = 10 mK and for (e) T = 1 K as extracted from the model discussed in the main text.

Since the thermal energy is comparable to the level splitting in the temperature window 0.5–1 K, absorption processes cannot be neglected. In order to understand the relaxation dynamics, we have developed a model that includes all possible transitions between the four spin-valley states in first and second order. For completeness, we have

also included in the model the weak coupling between the states $|1\rangle$ and $|4\rangle$. We evaluate all the transition rates and we use them to solve a 4×4 system of coupled differential rate equations given by:

$$\frac{dN_i}{dt} = -N_i \sum_{j\neq i} \Gamma_{ij} + \sum_{j\neq i} \Gamma_{ji} N_j \quad \text{for} \quad i,j = 1,\bar{2},\bar{3},4, \tag{4.7}$$

N_i being the population of the state i. The red lines in Figs. 4.3(a-c), show the relaxation rates as obtained from Eqs. 4.3, 4.6 and 4.7 (see also Sec. 4.7.2). The good agreement between model and experiment provides an indication that, even at high temperatures, relaxation is dominated by spin-valley physics. The spin-flip transitions involving the three lowest states are found to be the relevant rates to the relaxation process. These are $\Gamma_{\bar{2},1}$ and $\Gamma_{\bar{2},\bar{3}}$ when E_z is below E_{vs}, and $\Gamma_{\bar{3},1}$ and $\Gamma_{\bar{3},\bar{2}}$ when E_z is above E_{vs}. The relaxation rate above 200 mK consists of a flat region followed by a rising part. We attribute this behavior to the second-order process described by Eq. 4.6. We consider separately the contributions of the resonant ($|E_i - E_k| \ll \hbar\Gamma_k$) and off-resonant transitions ($|E_i - E_k| \gg \hbar\Gamma_k$). In the first case, known as Orbach process [19], the second-order relaxation is proportional to $\left|V_{fk}V_{ki}\right|^2/\Gamma_k$ (see Sec. 4.7.2). At sufficiently low temperatures, the spin lifetime depends exponentially on the temperature since the numerator is proportional to n_b and the denominator is temperature independent. We therefore theoretically predict the brief steep rise around 150–200 mK. At high temperatures Γ_k also becomes proportional to n_b and the temperature dependence vanishes. This explains the main flat region that we observe in Figs. 4.3(a-c). For off-resonant transitions, known as Raman process, the relaxation rate scales polynomially with the temperature. As discussed in Sec. 4.7.2, in case of phonon-mediated transitions, a T^9 temperature dependence is obtained. The Raman process dominates over the Orbach process above 500 mK (see Figs. 4.3(a-c)).

As we can see from Fig. 4.3(c), the increase in the relaxation rate at $B_0 = 3$ T does not match the model predictions above 500 mK, suggesting contributions to the relaxation from a different source rather than the spin-valley mixing. We rule out second-order contributions from Johnson noise because of the much weaker temperature dependence. Possible contributions might come from a second-order process involving the excited orbital states, which is expected to give a T^{11} temperature dependence as discussed in Sec. 4.7.2. Coupling to orbital states can potentially give a magnetic field dependence that would make it not observable at lower fields. Coupling to orbital states mediated by direct processes give rise to a B_0^2 field dependence; this phenomenon is known as Van Vleck cancellation, a consequence of Kramer's theorem [20]. For two-phonon processes, Van Vleck cancellation together with the spin-valley mixing can potentially give an even stronger field dependence.

The spin lifetime can be increased by reducing the spin-valley coupling. As shown in Eqs. 4.1 and 4.2, it can be strongly increased by reducing the applied magnetic field or by increasing the valley splitting energy. In Si-MOS the valley splitting can be electrically controlled and increased to $E_{vs} \approx 1$ meV [2, 21]. Figures 4.3(d,e) show the magnetic field and the valley splitting energy dependence of the relaxation rate for $T = 10$ mK and $T = 1$ K, using the parameters extracted from our numerical fittings of the experimental data. These results predict a spin lifetime at 1 K of approximately 500 ms, when $B_0 = 0.1$ T

and $E_{vs} = 575$ μeV. The relaxation at low magnetic fields is predicted to be dominated by second-order processes even at low temperature, due to the stronger field dependence of the first-order processes.

4.5. EFFECT OF TEMPERATURE ON CHARGE NOISE

We now turn to charge noise measurements. In a minimal model, charge noise can be attributed to defects that can trap or release charges, giving rise to electrical noise with a characteristic $1/f$ spectrum [22]. We measure the charge noise in our device as current fluctuations of the sensing dot tuned to a regime with a high slope dI/dV, to maximize the sensitivity. The time trace of the current is converted to voltage noise by dividing by the slope; then the spectrum is obtained through a Fourier transform. The same process is repeated in Coulomb blockade in order to subtract the baseline noise coming from the electronics [23]. Finally, the voltage fluctuations are converted to energy fluctuations by using the lever arm $\alpha_{ST} = 0.18$ eV/V of the sensing dot. The spectra shown in Fig. 4.4(a), scale as $1/f$ for the probed frequency regime. Figure 4.4(b) shows the temperature dependence of the charge noise amplitude at a fixed frequency of 1 Hz. We observe a linear increase of the charge noise amplitude over more than one decade of temperature (0.1–4 K), changing from approximately 2 μeV/$\sqrt{\text{Hz}}$ to 12 μeV/$\sqrt{\text{Hz}}$. This is indicating a different relation than predicted by a simple model, which assumes an equal distribution of thermally activated fluctuators with relaxation rates distributed according to a Lorentzian. This model would give rise to a square-root temperature dependence of the charge noise amplitude [22]. The offset measured at low temperature can be attributed to electrical noise that couples to the sensing dot via the gates. This remarkably weak dependence suggests that qubit operation will only be moderately affected when increasing temperature.

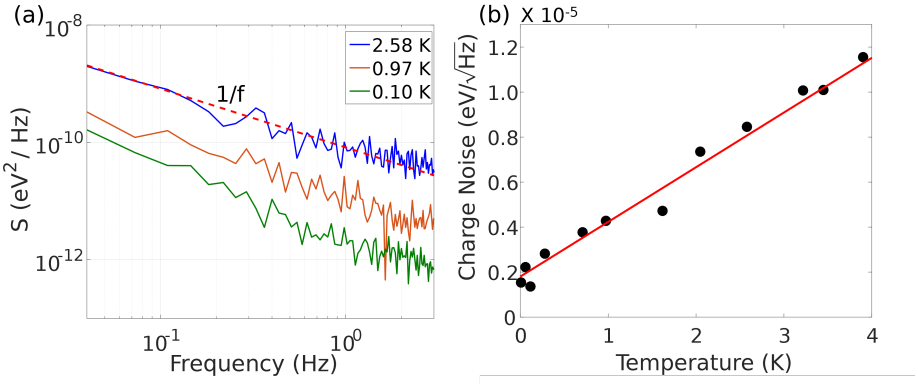

Figure 4.4: (a) Charge noise spectra obtained for three different temperatures. At higher frequencies the $1/f$ signal is masked by white noise. (b) Charge noise amplitude at a frequency of 1 Hz as a function of temperature fitted with a linear function.

4.6. SUMMARY AND CONCLUSION

IN summary, we have investigated the magnetic field and temperature dependence of the spin lifetime and measured $T_1 = 2.8$ ms at 1.1 K and $T_1 = 145$ ms at base temperature. Relaxation occurs through electric field fluctuations that cause spin transitions mediated by spin-valley coupling. At temperatures below 200 mK the dominant noise source is Johnson noise, while second-order phonon processes dominate at higher temperatures. We have also shown how the spin lifetime can be further improved by operating in low magnetic fields and tuning to high valley splitting energies. In particular Si-MOS devices have the advantage of a large and tunable valley splitting, whereas in Si/SiGe it is typically not larger than 100 μeV [24]. Future work aimed at improving lifetimes could focus on schemes that do not explicitly require a large magnetic field, such as readout via Pauli spin blockade. In addition, we have measured the temperature dependence of the charge noise amplitude and find consistency with a linear trend from 100 mK to 4 K.

Leading solid-state approaches for large-scale quantum computation focus on decreasing the operation temperature down to the millikelvin regime. Instead, the long spin lifetimes at elevated temperatures and the weak charge noise reported here indicate that such low temperatures are not a fundamental requirement for spins in Si-MOS quantum dots, providing an avenue for the demonstration of spin qubits with operation temperatures above one kelvin.

4.7. SUPPLEMENTAL MATERIAL

THIS section provides additional information on the device fabrication, the model and the corresponding rate equations, and the electron temperature and lever arm of the quantum dot used in these experiments.

4.7.1. DEVICE FABRICATION

Fabrication starts from a 300-mm silicon wafer, upon which a 100-nm layer of epitaxial ^{28}Si is grown, with a residual concentration of ^{29}Si of 900 ppm. The wafer is then thermally oxidized to form a 10-nm SiO_2 layer on top. We deposit 10 nm of Al_2O_3, fabricated by atomic layer deposition, and we pattern the nanostructures via electron beam lithography and deposit three layers of Ti (3 nm)/Pd (37 nm) that are electrically isolated by Al_2O_3 (7 nm). The smaller grain size of palladium films, compared to that of aluminum [25], enables a more uniform set of electric gates [26].

4.7.2. RATE EQUATIONS

Figures 4.5(a,b) shows the relevant contributions to the relaxation rate for $B_0 = 2$ T. The low-temperature regime is dominated by a first-order process between the states $|\bar{2}\rangle$ and $|1\rangle$. According to Eqs. 4.4 and 4.5, it is composed of a flat initial part followed by a linear increase. At higher temperatures, the second-order process mediated by phonons between the states $|\bar{2}\rangle$ and $|\bar{3}\rangle$ becomes dominant. We can better understand its functional

form by expanding the terms in Eq. 4.6:

$$\Gamma^{(2)}_{\bar{2}\bar{3}} \propto \int_0^{\omega_d}\int_0^{\omega_d}\left|\sum_{k\neq 2,3}\frac{c_{2k}\,c_{k3}}{\Delta E_{\bar{2}k}-\hbar\omega'+\frac{1}{2}i\hbar\Gamma_k}\right|^2 \cdot\omega'^5\omega''^5[1+n_b(\hbar\omega')]n_b(\hbar\omega'')\delta(\Delta E_{\bar{3}\bar{2}}+\hbar\omega'-\hbar\omega'')d\omega' d\omega'', \quad (4.8)$$

where ω_d is the Debye frequency and the coefficients c_{ij} come from the overlap between the states i, j due to mixing between spin and valley. In silicon, the electron-phonon interaction is mediated by deformation potential phonons. Therefore, the matrix elements have an additional factor ω^2 with respect to the standard interaction with piezoelectric phonons, because of the $\sqrt{q}$ dependence of the strain caused by deformation potential phonons, where q is the wave number.

As discussed earlier, $\frac{1}{2}\hbar\Gamma_k$ represents the energy width of the k state, determined by its lifetime. Since the ground state of the system $|1\rangle$ has, at least at low temperature, a long lifetime compared to the state $|4\rangle$, $\Gamma_4 \gg \Gamma_1$, we can neglect the transitions through the state $|4\rangle$ in the sum of Eq. 4.8. In the following, we will consider separately the contributions to the integral coming from off-resonant ($\hbar\omega' \neq \Delta E_{\bar{2}1}$) and resonant ($\hbar\omega' \approx \Delta E_{\bar{2}1}$) phonons.

In the off-resonant case and at sufficiently high temperatures, phonons with frequencies $\hbar\omega \gg \Delta E_{\bar{2}1}, \Delta E_{\bar{3}\bar{2}}$ are well populated and Eq. 4.8 can be rewritten as:

$$\Gamma^{(2)}_{\bar{2}\bar{3}} = C_R T^9 \int_0^{\hbar\omega_d/k_B T}\frac{e^x}{(e^x-1)^2}dx \quad (4.9)$$

and the relaxation rate scales to a good approximation as T^9. In the intermediate regime $\Delta E_{\bar{2}1} \gg \hbar\omega \gg \Delta E_{\bar{3}\bar{2}}$, the term $\hbar\omega'$ in the denominator of Eq. 4.8 can be neglected and the relaxation rate scales as T^{11}. In our experimental case, the energy differences between the levels are comparable with each other and thus this last regime is not visible in the experimental data. Instead, if we consider coupling with orbital states, these conditions apply and a T^{11} dependence is expected. The power laws we found are strictly related to the power of the ω terms in Eq. 4.8, which depends on the particular nature of the electron-phonon interaction. For example, in GaAs, where piezoelectric phonons dominate over deformation potential phonons, the power is reduced to three instead of five, which leads to a T^5 and T^7 temperature dependence. In case of Johnson mediated relaxation an even weaker temperature dependence is obtained.

In the resonant case, we have $\hbar\omega' \approx \Delta E_{\bar{2}1}$ and Eq. 4.8 can be approximated as:

$$\Gamma^{(2)}_{\bar{2}\bar{3}} = C_O\frac{[1+n_b(\Delta E_{\bar{2}1})]n_b(\Delta E_{\bar{2}1}+\Delta E_{\bar{2}\bar{3}})}{\Gamma_1}, \quad (4.10)$$

where the lifetime of the k state is in general evaluated as the inverse of the sum of all first-order processes between k and the other states and it is ultimately limited by the time scale of the experiment. At sufficiently low temperatures, Γ_k is temperature independent and the relaxation rate depends exponentially on the temperature according to $\Gamma^{(2)}_{\bar{2}\bar{3}} \propto n_b(\Delta E_{\bar{2}1}+\Delta E_{\bar{2}\bar{3}})$. At higher temperatures, Γ_k becomes also proportional to $n_b(\Delta E_{\bar{2}1}+\Delta E_{\bar{2}\bar{3}})$ and the relaxation rate is given approximately by $1+n_b(\Delta E_{\bar{2}1})$, which

is temperature independent for $k_B T \ll \Delta E_{\bar{2}1}$ and linear dependent for $k_B T \gg \Delta E_{\bar{2}1}$. In our experimental case, this linear dependence is masked by the the Raman process. The resonant and off-resonant transitions can thereby explain all the different regimes that we see in Fig. 4.5(a).

The rates in first and second order are used to solve the 4×4 system of coupled differential rate equations:

$$\begin{bmatrix} \dot{N}_1 \\ \dot{N}_2 \\ \dot{N}_3 \\ \dot{N}_4 \end{bmatrix} = \begin{bmatrix} -(\Gamma_{12}+\Gamma_{13}+\Gamma_{14}) & \Gamma_{21} & \Gamma_{31} & \Gamma_{41} \\ \Gamma_{12} & -(\Gamma_{21}+\Gamma_{23}+\Gamma_{24}) & \Gamma_{32} & \Gamma_{42} \\ \Gamma_{13} & \Gamma_{23} & -(\Gamma_{31}+\Gamma_{32}+\Gamma_{34}) & \Gamma_{43} \\ \Gamma_{14} & \Gamma_{24} & \Gamma_{34} & -(\Gamma_{41}+\Gamma_{42}+\Gamma_{43}) \end{bmatrix} \cdot \begin{bmatrix} N_1 \\ N_2 \\ N_3 \\ N_4 \end{bmatrix} \tag{4.11}$$

N_i being the population of the state i. For each temperature we extract the four eigenvalues of the matrix. Among the four, one equals zero and corresponds to the stationary population of the levels after the relaxation process is over. Two are much greater than the inverse time scale of the experiment and are therefore discarded, since they correspond to exponential decays not observable in the experiment. Finally, the remaining one represents the time constant that characterizes the single exponential decay of the spin-up fraction as a function of load time. This rate is shown in Figs. 4.3(a-c).

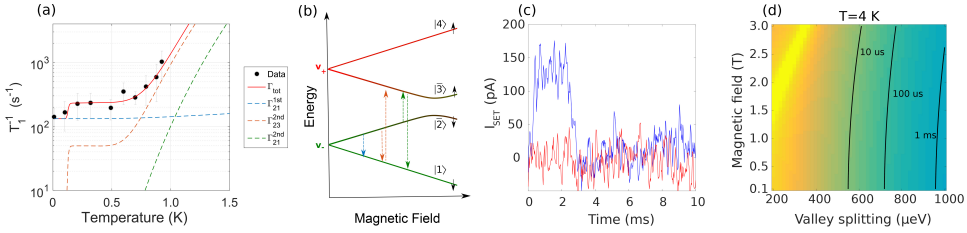

Figure 4.5: (a) Relaxation rate as a function of temperature for $B_0 = 2$ T. The dashed colored lines show the relevant transition rates, including the first-order process between the states $|\bar{2}\rangle$ and $|1\rangle$ and second-order transitions via the states $|1\rangle$ and $|\bar{3}\rangle$. (b) The relevant transitions shown in the plot in (a) are sketched in an energy diagram. (c) Example of a single-shot readout trace. The blue curve is the response of the SET when a spin-up electron is readout. The red line is the analogous case for a spin-down electron. (d) Magnetic field and valley splitting dependence of the relaxation rate at a temperature of 4 K. Lifetimes larger than 1 ms are accessible with a valley splitting close to 1 meV.

As discussed in Sec. 4.4, the spin lifetime can be further improved by working in a low magnetic field and high valley splitting regime. Figure 4.5(d) show this dependence at a temperature of 4 K, where second-order phonon processes dominate the relaxation process. Even at this relatively high temperature, we extract lifetimes larger than 1 ms for a valley splitting close to 1 meV, which is a very promising result for future scalability of these systems.

We did not discuss relaxation due to the residual ^{29}Si nuclei. However, the presence of nuclei mainly affects the dephasing of the electron spin rather than relaxation, due to the large Zeeman energy mismatch. The modulation of hyperfine coupling by phonons is also suppressed in natural silicon due the low concentration of ^{29}Si nuclei [27]. The effect can be expected to be even smaller in our case, where the substrate is made of ^{28}Si.

4.7.3. ELECTRON TEMPERATURE AND LEVER ARM OF THE QUANTUM DOT

Both the base electron temperature and the lever arm of the quantum dot have been extracted by a unique measurement, where the width of the charge transition (0→1) shown by the red arrow in Fig. 4.1(b) is measured as a function of the nominal fridge temperature [28]. The charge stability diagram shown in Fig. 4.1(b), is measured via a double-lock-in technique, where the transconductance dI_s/dP_1 of the sensing dot is measured by applying an AC excitation V_{AC} to the gate P1. During the map, the current I_s of the sensing dot is kept at the most sensitive point by using a digitally-controlled feedback. The width of the transition is determined by V_{AC} for large AC excitations and by the thermal broadening due to the finite electron temperature T_e when $V_{AC} \ll k_B T_e$. In these conditions the transconductance dI_s/dP_1 is proportional to the derivative of the Fermi-Dirac distribution:

$$\frac{dI_s}{dP_1} = a\cosh^{-2}\left(\frac{\alpha_{P1}(P_1 - b)}{2k_B T_e}\right) + c, \tag{4.12}$$

where a, b and c are fitting parameters and α_{P1} is the lever arm of the quantum dot. The electron temperature T_e depends on the nominal fridge temperature T_f and the base electron temperature T_0 according to:

$$T_e = \sqrt{T_0^2 + T_f^2}. \tag{4.13}$$

We fix the gate P2 such that the tunneling rate between dot and reservoir is maximized and therefore the signal-to-noise ratio in the charge stability diagram is also maximized. We sweep the gate P1 in the direction of the first charge transition. During the sweep we apply an AC excitation to the gate P1 of 15 μV at 133 Hz.

Figure 4.6 shows the width of the transition as a function of T_f. The width is for all points much higher than the excitation applied to the gate P1 meaning that we are in the conditions of a thermally limited transition. From the fit we extract a lever arm of $\alpha_{P1} = 0.122 \pm 0.005$ eV/V and a base electron temperature of $T_0 = 108 \pm 13$ mK.

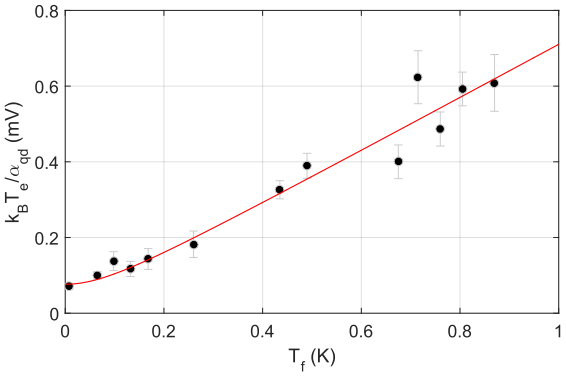

Figure 4.6: Width of the (0→1) charge-state transition as a function of the fridge temperature. The red line is a fit according to Eqs. 4.12 and 4.13. At sufficiently high temperatures, T_e equals T_f and the transition width increases linearly with a slope proportional to the inverse of the lever arm. At low temperature, T_f becomes smaller than T_0 and the transition width becomes independent of T_f.

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5

SPATIAL NOISE CORRELATIONS IN A SI/SIGE TWO-QUBIT DEVICE FROM BELL STATE COHERENCES

We study spatial noise correlations in a Si/SiGe two-qubit device with integrated micromagnets. Our method relies on the concept of decoherence-free subspaces, whereby we measure the coherence time for two different Bell states, designed to be sensitive only to either correlated or anti-correlated noise, respectively. From these measurements, we find weak correlations in low-frequency noise acting on the two qubits, while no correlations could be detected in high-frequency noise. We expect nuclear spin noise to have an uncorrelated nature. A theoretical model and numerical simulations give further insight into the additive effect of multiple independent (anti-)correlated noise sources with an asymmetric effect on the two qubits as can result from charge noise. Such a scenario in combination with nuclear spins is plausible given the data and the known decoherence mechanisms. This work is highly relevant for the design of optimized quantum error correction codes for spin qubits in quantum dot arrays, as well as for optimizing the design of future quantum dot arrays.

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5.1. INTRODUCTION

LARGE-SCALE quantum computers will need to rely on quantum error correction (QEC) to deal with the inevitable qubit errors caused by interaction with the environment and by imperfect control signals. The noise amplitude can vary from qubit to qubit and furthermore can exhibit correlations or anti-correlations between qubits. Most QEC error thresholds, such as the 1%-threshold for the surface code [1], are derived under the assumption of negligible correlations in qubit errors. Other approaches, such as decoherence-free subspaces (DFSs) [2], are designed under the assumption of correlated noise, taking advantage of symmetry considerations to reduce the qubit sensitivity to external noise. Examples for quantum dot based qubits include the singlet-triplet qubit [3, 4] and the quadrupole qubit [5]. In addition, QEC schemes exist that can deal with short-range correlations in the noise [6]. Spatial noise correlations have therefore been studied extensively, both theoretically [7–14] and experimentally [11, 15, 16].

Semiconductor quantum dots are promising hosts for spin qubits in quantum computation [17], because of their favorable scaling and excellent coherence properties. Silicon, in particular, has excellent properties for long-lived spin qubits: intrinsic spin-orbit coupling is weak and hyperfine interaction is small [18]. The hyperfine interaction can even be reduced further by isotopic purification. In addition, silicon quantum dot fabrication is largely compatible with conventional CMOS industry, which allows large-scale manufacturing of silicon spin qubits and on-chip integration of classical control electronics [19]. In recent years, significant progress has been made with silicon spin qubits, showing tens of milliseconds coherence times [20], high-fidelity single- [20–22] and two-qubit gates [23, 24], quantum algorithms [25], strong spin-photon coupling [26, 27] and long-distance spin-spin coupling [28].

The most important decoherence sources in natural silicon quantum dots are the hyperfine interaction with nuclear spins and charge noise. Nuclear spin noise is typically uncorrelated between adjacent dots [29]. Charge noise is usually caused by distant fluctuating charges [30–32], which is expected to lead to spatial correlations on the length scale of interdot distances of 100 nm or less. In the presence of a magnetic field gradient, which is commonly used for qubit selectivity and fast qubit control, qubits are sensitive to electric field fluctuations and charge noise will impact spin coherence [21, 33]. However, a quantitative measurement of spatial noise correlations in an actual two-qubit device is lacking.

Here, we study experimentally spatial noise correlations in a Si/SiGe two-qubit device, by preparing Bell states in either the parallel or the anti-parallel subspace, similarly to recent work with NV centers in diamond [34]. Via a Ramsey-style experiment, we find that Bell states in the anti-parallel subspace show a ~30% longer dephasing time than those in the parallel subspace. A Hahn-echo style measurement reveals no detectable difference in the decay time for the respective Bell states. We present a simple model to describe noise correlations on two qubits, including asymmetric noise amplitudes acting on the two qubits, and study numerically the combined effect of multiple (anti-) correlated, asymmetric noise sources. We use these simulations to assess which combinations of noise sources are compatible with the observed coherence times.

5.2. DEVICE AND EXPERIMENTAL DETAILS

FIGURE 5.1(a) shows a schematic of the device used in this work, which is the same as described earlier [23, 25]. It comprises an electrostatically defined double quantum dot (DQD) in a two-dimensional electron gas (2DEG). The 2DEG is confined in a 12-nm-thick silicon quantum well, 37 nm below the surface of an undoped Si/SiGe heterostructure with natural isotope composition. On top of the heterostructure, we fabricate two gate layers with cobalt micromagnets. The device is cooled down to $T \approx 30$ mK and subject to an external magnetic field of $B_{ext} = 617$ mT. Suitable voltages are applied to accumulation and fine gates (in the top and bottom layer, respectively) to form a DQD in the single-electron regime. Single-electron spin states are Zeeman split by the total magnetic field, and used to encode two single-spin qubits. The micromagnets ensure individual qubit addressability by a gradient in the longitudinal magnetic field, resulting in spin resonance frequencies of 18.35 GHz and 19.61 GHz for qubit 1 (Q1) and qubit 2 (Q2), respectively.

Figure 5.1(b) shows the resulting energy level diagram for the two qubits. For perfectly correlated noise, fluctuations in the Zeeman energy for both qubits are the same: $\delta E_{Z,1} = \delta E_{Z,2} = \delta E_Z$. Consequently, the sum of the two qubit energies fluctuates, $\Delta(E_{Z,1} + E_{Z,2}) = 2\delta E_Z$, while their difference is not affected, $\Delta(E_{Z,1} - E_{Z,2}) = 0$. On the other hand, for perfectly anti-correlated noise $\delta E_{Z,1} = -\delta E_{Z,2}$, and the opposite holds for the sum and difference energies. Bell states consist of superpositions of the two-spin eigenstates and allow to study dephasing between these eigenstates. An anti-parallel Bell state, which evolves in time at a rate proportional to the difference of the single-qubit energies, will be affected by anti-correlated noise, but not by correlated noise. A parallel Bell state, which evolves in time at a rate proportional to the sum of the single-qubit energies, is sensitive to correlated noise, but not to anti-correlated noise. Such properties are exploited in DFSs and are used here as a probe for spatial correlations in the noise acting on the qubits.

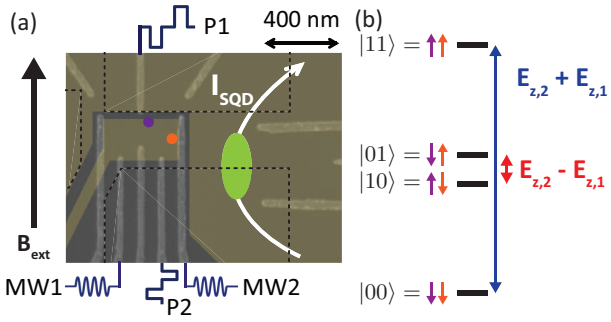

Figure 5.1: (a) Scanning electron micrograph of a similar Si/SiGe device as used in the measurements, showing the depletion gates used to define the potential landscape in the 2D electron gas accumulated by the yellow shaded gates (drawn digitally). Purple and orange circles indicate the estimated positions of the two dots, occupied by one electron each, and the ellipse indicates a sensing quantum dot. Two-qubit operations are controlled via gate voltage pulses applied to gates P1 and P2, and microwave signals for single-qubit control are applied to gates MW1 and MW2. The contours of cobalt micromagnets are indicated by the dashed black lines. (b) Energy level diagram for two qubits in an inhomogeneous magnetic field, giving rise to a difference in Zeeman energy between the two qubits.

We now summarize the experimental procedure; for more information on the measurement setup and individual qubit characteristics, see Secs. 5.8.2 and 5.8.3, and Ref. [25]. Q2 is initialized and read out via spin-selective tunneling to a reservoir [35]. Initialization of Q1 to its ground state is done by fast spin relaxation at a hotspot [36], and readout of Q1 is performed by mapping its spin state onto Q2 via a controlled-rotation (CROT) gate followed by spin readout of Q2 [25]. For single-qubit driving we exploit an artificial spin-orbit coupling, induced by cobalt micromagnets, for electric dipole spin resonance (EDSR) [37]. The two-qubit gate relies on the exchange interaction between the two qubits, controlled by gate voltage pulses. We operate in the regime where the Zeeman energy difference between the two qubits exceeds the two-qubit exchange interaction strength, hence the native two-qubit gate is the controlled-phase gate [25, 38, 39].

5.3. THEORETICAL ANALYSIS OF SPATIAL NOISE CORRELATIONS

REAL systems are often subject to both uncorrelated and (anti-)correlated noise. Furthermore, the noise amplitudes acting on different qubits are generally different, regardless of whether the noise is uncorrelated or (anti-)correlated. We wish to capture all these scenarios in one unified theoretical formalism. We include pure dephasing only, which is justified by the long T_1 times for spin qubits compared to the experiment and coherence timescales, and assume a quasistatic Gaussian joint probability distribution for the noise acting on the two qubits. We can then express the two-qubit coherence times for an anti-parallel ($|\Psi\rangle = (|\downarrow\uparrow\rangle - i\,|\uparrow\downarrow\rangle)/\sqrt{2}$) and a parallel ($|\Phi\rangle = (|\downarrow\downarrow\rangle - i\,|\uparrow\uparrow\rangle)/\sqrt{2}$) Bell state quantitatively as follows (see Sec. 5.8.1):

$$\begin{aligned}\left(\frac{1}{T^*_{2,|\Psi\rangle}}\right)^2 &= 2\pi^2\left(\sigma_1^2+\sigma_2^2-2\rho\sigma_1\sigma_2\right),\\ \left(\frac{1}{T^*_{2,|\Phi\rangle}}\right)^2 &= 2\pi^2\left(\sigma_1^2+\sigma_2^2+2\rho\sigma_1\sigma_2\right),\end{aligned} \tag{5.1}$$

where σ_i^2 is the variance of the noise in the resonance frequency of qubit i (the single-qubit coherence time is given by $\left(\frac{1}{T^*_{2,i}}\right)^2 = 2\pi^2\sigma_i^2$), and ρ is a correlation factor ($-1 \le \rho \le 1$). Positive ρ indicates correlations, while negative ρ indicates anti-correlations.

The effect of the noise amplitudes σ_i and the correlation factor ρ on the coherence time for the anti-parallel Bell state $T^*_{2,|\Psi\rangle}$ is visualized in Fig. 5.2(a). Here $\sigma_1 = \sigma_2$, so for $\rho = 1$, $|\Psi\rangle$ forms a true DFS and the noise has no effect regardless of its amplitude. With decreasing ρ, $T^*_{2,|\Psi\rangle}$ decreases, as the noise becomes initially less correlated ($\rho > 0$), then uncorrelated ($\rho = 0$) and eventually anti-correlated ($\rho < 0$). For $\rho = -1$, $T^*_{2,|\Psi\rangle}$ is only one fourth of the single-qubit coherence times. For $T^*_{2,|\Phi\rangle}$, the corresponding image is mirrored around $\rho = 0$, see the inset of Fig. 5.2(a), and the longest coherence time occurs for $\rho = -1$. Figure 5.2(b) shows the effect of asymmetric noise amplitudes on the two qubits for $\rho = 1$. We see that despite the maximal correlation factor, a true DFS only exists for symmetric noise ($\sigma_1 = \sigma_2$) and $|\Psi\rangle$ decoheres when $\sigma_1 \neq \sigma_2$. Clearly, both the asymmetry in the noise and the correlation factor impact the two-qubit coherence.

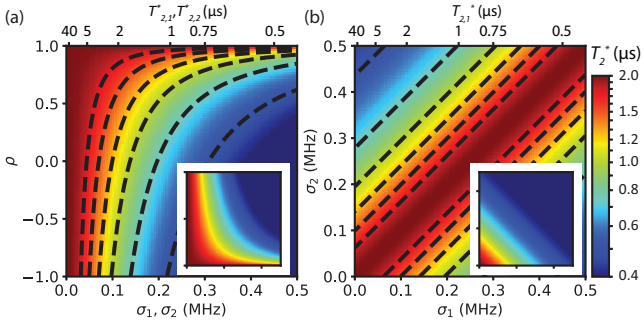

Figure 5.2: $T^*_{2,|\Psi\rangle}$ extracted from Eq. 5.1, (a) as a function of correlation factor ρ and noise amplitude $\sigma_1 = \sigma_2$, and (b) as a function of σ_1 and σ_2 for $\rho = 1$. Insets show the corresponding images for $T^*_{2,|\Phi\rangle}$. Contours correspond to (0.5, 0.75, 1.0, 1.25, 1.5, 1.75) μs. In all images an uncorrelated noise contribution corresponding to a Bell state coherence time of 2.0 μs is added to prevent singularities.

5.4. MEASUREMENT OF SPATIAL NOISE CORRELATIONS

FROM Eq. 5.1, we see that, as anticipated, experimental measurement of the decay times for the parallel and anti-parallel Bell states reveals whether (anti-)correlations in the noise acting on the two qubits are present. In order to quantify the correlation factor ρ, measurements of the single-qubit decay time are needed as well.

Concretely, we perform two-qubit measurements analogous to the measurement of Ramsey fringes to measure the decay of Bell state coherences over time [13]. As shown in the circuits in Figs. 5.3(a,c), we prepare $|\Psi\rangle$ or $|\Phi\rangle$ and after a varying free evolution time we reverse the sequence to ideally return to the $|00\rangle$ state. In every run of the experiment, we measure both spins in single-shot mode and determine the two-spin probabilities from repeated experiment runs. The two-spin probabilities are normalized and a Gaussian decay is fit to the $|00\rangle$ return probability. To improve the fit of the decay, we add an evolution-time dependent phase to the first microwave pulse applied to Q2 after the delay time (see Z($\Delta\varphi$) in Figs. 5.3(a,c)), so that the measured $|00\rangle$ probability oscillates. We first test the measurement procedure via artificially introduced dephasing from random rotations of each spin around its quantization axis, implemented in software via Pauli frame updates. The decay observed for the anti-parallel (parallel) Bell state is independent of the noise amplitude when the same (opposite) random rotations are applied to both spins, but increases when opposite (the same) random rotations are applied to the two spins, as expected. This validates the measurement protocol.

Figures 5.3(b,d) show typical decay curves for $|\Psi\rangle$ and $|\Phi\rangle$, respectively, when subject to natural noise only. A scatter plot of repeated measurements, Fig. 5.3(e), shows a systematically longer T_2^* for $|\Psi\rangle$ than for $|\Phi\rangle$, indicating correlations in the noise. Using Eq. 5.1, derived for quasistatic noise, we can extract from the decay of $|\Psi\rangle$ and $|\Phi\rangle$ a lower bound for the correlation factor, $\rho \geq 0.27 \pm 0.02$ (see Sec. 5.8.7). In order to go beyond a lower bound and determine an estimate of ρ from Eq. 5.1, we also need at least one of the single-qubit dephasing times, which we measured to be $T^*_{2,1} = 0.97 \pm 0.02$ μs and $T^*_{2,2} = 0.59 \pm 0.02$ μs. Using both single-qubit T_2^*s in Eq. 5.1 gives an overdetermined system of equations. We proceed by keeping $T^*_{2,1}/T^*_{2,2}$ equal to the measured ratio, and

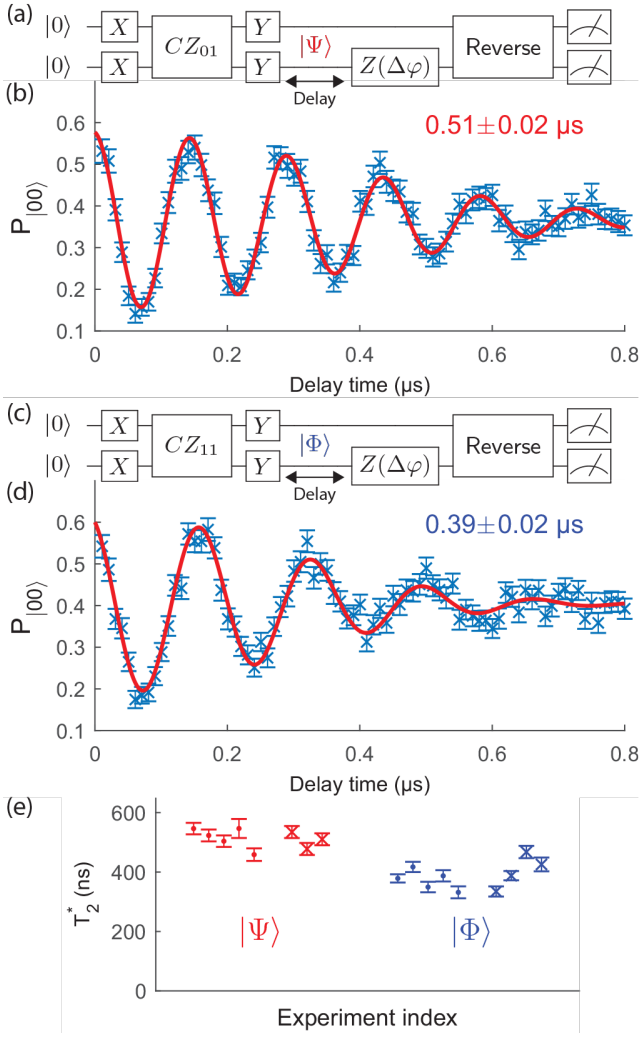

Figure 5.3: (a,c) Circuit diagrams for two-qubit experiments analogous to the measurement of Ramsey fringes. The gate sequences are designed such that single-qubit rotations are always applied simultaneously to both qubits, avoiding idle times that would lead to faster dephasing. Here $CZ_{ij}|m,n\rangle = (-1)^{\delta(i,m)\delta(j,n)}|m,n\rangle$ for $i,j,m,n \in \{0,1\}$ are the primitive two-qubit gates, constructed from a CZ gate with duration $t = \pi\hbar/J$ and single-qubit rotations [25]. (b,d) Typical $|00\rangle$ return probability as a function of delay time for (b) $|\Psi\rangle$ and (d) $|\Phi\rangle$. The data are fit with a sinusoidal function with Gaussian decay, $P_{|00\rangle} \propto e^{-\left(t/T_2^*\right)^2}$. Error bars are based on a Monte Carlo method by assuming a multinomial distribution for the measured two-spin probabilities and are $\pm 1\sigma$ from the mean [25]. We attribute the slight difference in oscillation frequency between (b) and (d) to crosstalk effects during frequency calibration, as for example observed in Refs. [23, 25, 40]. (e) Scatter plot of decay times for $|\Psi\rangle$ and $|\Phi\rangle$ for two measurement runs separated by ~50 hours (points and crosses). Every data point is averaged over ~100 minutes. The average coherence times are 513 ± 8 ns and 387 ± 6 ns for $|\Psi\rangle$ and $|\Phi\rangle$, respectively. Error bars are $\pm 1\sigma$ from the mean.

obtain a modest correlation factor, $\rho = 0.31 \pm 0.03$ (see Sec. 5.8.7). The data presented in Figs. 5.3 and 5.4 form a complete dataset with repeated measurements, all performed with very similar gate voltage settings.

We note that in keeping $T^*_{2,1}/T^*_{2,2}$ fixed, Eq. 5.1 returns a value for σ_1 and σ_2 that is ~15% larger than the measured value. The discrepancy may be in part due to the fact that the simple model that leads to Eq. 5.1 assumes quasistatic Gaussian noise. This is a commonly made assumption in simple models of silicon spin qubits, but various experiments showed higher-frequency noise to be relevant as well [20, 22, 25]. However, a more detailed model that accounts for non-quasistatic noise is beyond the scope of this work.

5.5. ECHO EXPERIMENTS

In order to gain insight into the frequency dependence of the spatial noise correlations, we perform measurements analogous to Hahn echo measurements. Here the delay times seen in the circuit diagrams of Figs. 5.3(a,c) contain 180 degree rotations around the $\hat{x}$ or $\hat{y}$ axis applied to the two qubits, which reverse the time evolution resulting from static noise contributions (see Sec. 5.8.9 for circuit diagrams and details). The results are presented in Fig. 5.4. The echo pulses prolong the two-qubit coherence times by a factor of ~4–5. We do not, however, observe a systematic difference in the echo decay times for the parallel versus anti-parallel Bell states, meaning there are no detectable spatial correlations in higher-frequency noise, and the correlations found in the Ramsey-style measurements of Fig. 5.3 are mostly present in the low-frequency part of the spectrum.

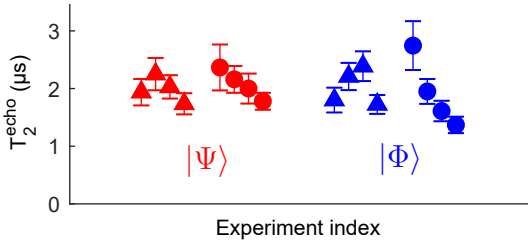

Figure 5.4: Scatter plot of the two-qubit coherence times obtained in Hahn-echo style measurements for $|\Psi\rangle$ and $|\Phi\rangle$, from a fit to the data with an exponentially decaying sinusoidal function ($P_{|00\rangle} \propto e^{-t/T_2^*}$). Triangles represent data points where the Hahn echo pulses applied to both qubits are rotations around the $\hat{x}$-axis. For the circles, the rotation of Q1 is around $\hat{x}$ and the rotation of Q2 is around $\hat{y}$. Data points are averaged over ~{47, 66, 100, 148} minutes. The average two-qubit Hahn echo coherence times are 2.03±0.09 μs and 1.98±0.09 μs for $|\Psi\rangle$ and $|\Phi\rangle$, respectively. Error bars are $\pm 1\sigma$ from the mean.

5.6. NUCLEAR SPINS AND MULTIPLE NOISE SOURCES

We observe only modest correlations in the noise. In this natural silicon substrate the hyperfine interaction with ^{29}Si nuclear spins, for which little or no spatial correlations are expected [29], is likely to contribute significantly. Estimates of the separate contributions to the noise are not reliable with the present data. In order to assess the spatial noise correlations arising from charge noise only, it would be helpful to repeat

the experiments presented here in an isotopically purified ^{28}Si sample.

In addition to noise that is uncorrelated by itself, multiple noise sources that produce correlated noise on the qubits can add up to give rise to noise that is mostly uncorrelated as well. This can be seen from the following observations. Multiple independently fluctuating noise sources each producing perfectly correlated noise ($\rho = 1$) with the same relative amplitude on the two qubits, are equivalent to a single (stronger) source of perfectly correlated noise with this same relative amplitude on the two qubits. However, randomly distributed relative amplitudes would rapidly render the combined noise indistinguishable from uncorrelated noise.

Different relative amplitudes can occur for charge noise from multiple charge fluctuators close to the dots, which couple to the spin states through the magnetic field gradient. Also remote charge fluctuators can give rise to different noise amplitudes on the two spins, for instance when either the tightness of the confining potential or the local magnetic field gradient differs between the dots (indeed Tab. 5.3 reveals that Q2 is much more sensitive to electric fields than Q1). In Secs. 5.8.10 and 5.8.11 we illustrate this effect with an example simulation and describe it mathematically.

Based on this discussion, a picture emerges where the combination of noise from multiple distant charge fluctuators that affect the qubits asymmetrically due to their different confining potentials and nuclear spin noise, is responsible for the (weak) spatial noise correlations at low frequency.

5.7. SUMMARY AND CONCLUSION

IN summary, we have demonstrated a method to quantitatively study spatial noise correlations based on the coherence of Bell states in a Si/SiGe two-qubit device. Experimentally we observe small spatial correlations in low-frequency noise, while for higher-frequency noise correlations appear to be absent. Applying this method to an isotopically purified silicon spin qubit device will yield more quantitative information on correlations present in charge noise only. Our findings on the importance of asymmetric coupling of noise sources to two (or more) qubits can be exploited for reducing or enhancing spatial correlations in the noise in any qubit platform. For the case of spin qubits in quantum dots, this can be done for instance through a device design with engineered differences in confining potential or magnetic field gradient. In this respect, qubits encoded in two-electron spin states in dot-donor systems offer an extreme difference in confining potential [41]. We anticipate that the optimization of future quantum error correction codes will go hand in hand with the design of qubits that either maximize or minimize spatial noise correlations, as has been done in for example Ref. [42].

Data supporting the findings of this study are available online [43].

5.8. SUPPLEMENTAL MATERIAL

THIS section provides additional information on the noise model, experimental details, quantification of the observed correlations, a note on the effect of the Bell state fidelity, echo experiments, simulation results and the effect of adding multiple noise sources.

5.8.1. NOISE MODEL

We model the two-qubit system by the Hamiltonian:

$$H = \frac{hf_1}{2}\sigma_1^Z + \frac{hf_2}{2}\sigma_2^Z, \tag{5.2}$$

where h is the Planck constant, $f_i = \frac{g\mu_B B_i}{h}$ is the Larmor frequency for qubit i, g is the electron g-factor, μ_B is the Bohr magneton, B_i is the total magnetic field at the position of qubit i and σ_i^Z is the Pauli Z operator for qubit i. The two qubits are subject to dephasing noise, which we model as a fluctuating qubit frequency f_i. We assume Gaussian distributed noise with zero mean and covariance matrix Σ:

$$\mathbf{f} = (f_1, f_2) \sim \mathcal{N}((0,0), \Sigma); \Sigma = \begin{bmatrix} \sigma_1^2 & \rho\sigma_1\sigma_2 \\ \rho\sigma_1\sigma_2 & \sigma_2^2 \end{bmatrix}, \tag{5.3}$$

where σ_i^2 is the variance of the noise in f_i, and ρ $(-1 \leq \rho \leq 1)$ is a correlation factor. Positive ρ indicates correlations, while negative ρ indicates anti-correlations. We obtain the unitary time evolution operator in the $\{|00\rangle, |01\rangle, |10\rangle, |11\rangle\}$ basis by exponentiating the Hamiltonian:

$$U = e^{-iHt/\hbar} = \begin{pmatrix} e^{-i\pi(f_1+f_2)t} & & & \\ & e^{-i\pi(f_1-f_2)t} & & \\ & & e^{i\pi(f_1-f_2)t} & \\ & & & e^{i\pi(f_1+f_2)t} \end{pmatrix}, \tag{5.4}$$

where $\hbar = \frac{h}{2\pi}$. Assuming quasistatic noise, we average over this unitary transformation by integrating over the joint probability distribution function:

$$\rho(t) = \overline{U\rho(0)U^\dagger} = \frac{1}{2\pi\sqrt{\det(\Sigma)}} \int U\rho(0)U^\dagger e^{-\mathbf{f}^T\Sigma^{-1}\mathbf{f}/2} d\mathbf{f}. \tag{5.5}$$

The relevant expressions for anti-parallel ($|\Psi\rangle$) and parallel ($|\Phi\rangle$) Bell states, reflecting dephasing between $|01\rangle$ and $|10\rangle$, and $|00\rangle$ and $|11\rangle$, respectively, are:

$$\begin{aligned} \langle 01|\overline{U\rho(0)U^\dagger}|10\rangle &= \frac{1}{2} \times \frac{1}{2\pi\sqrt{\det(\Sigma)}} \int e^{-i2\pi(f_1-f_2)t} e^{-\mathbf{f}^T\Sigma^{-1}\mathbf{f}/2} d\mathbf{f} \\ &= \frac{1}{2}\exp\left[-2\pi^2 t^2(\sigma_1^2+\sigma_2^2-2\rho\sigma_1\sigma_2)\right], \\ \langle 00|\overline{U\rho(0)U^\dagger}|11\rangle &= \frac{1}{2} \times \frac{1}{2\pi\sqrt{\det(\Sigma)}} \int e^{-i2\pi(f_1+f_2)t} e^{-\mathbf{f}^T\Sigma^{-1}\mathbf{f}/2} d\mathbf{f} \\ &= \frac{1}{2}\exp\left[-2\pi^2 t^2(\sigma_1^2+\sigma_2^2+2\rho\sigma_1\sigma_2)\right], \end{aligned} \tag{5.6}$$

so the decay for anti-parallel and parallel Bell states is Gaussian with associated time scales (Eq. 5.1):

$$\begin{aligned}\left(\frac{1}{T^*_{2,|\Psi\rangle}}\right)^2 &= 2\pi^2\left(\sigma_1^2+\sigma_2^2-2\rho\sigma_1\sigma_2\right),\\ \left(\frac{1}{T^*_{2,|\Phi\rangle}}\right)^2 &= 2\pi^2\left(\sigma_1^2+\sigma_2^2+2\rho\sigma_1\sigma_2\right).\end{aligned} \tag{5.7}$$

Noting that in the case of Gaussian quasistatic noise for single-qubit decay $\left(\frac{1}{T^*_{2,i}}\right)^2 = 2\pi^2\sigma_i^2$, these expressions can be rewritten in terms of single-qubit coherence times:

$$\left(\frac{1}{T^*_{2,|\Psi\rangle}}\right)^2 = \left(\frac{1}{T^*_{2,1}}\right)^2+\left(\frac{1}{T^*_{2,2}}\right)^2-2\rho\frac{1}{T^*_{2,1}T^*_{2,2}}, \tag{5.8}$$

$$\left(\frac{1}{T^*_{2,|\Phi\rangle}}\right)^2 = \left(\frac{1}{T^*_{2,1}}\right)^2+\left(\frac{1}{T^*_{2,2}}\right)^2+2\rho\frac{1}{T^*_{2,1}T^*_{2,2}}. \tag{5.9}$$

Subtracting Eq. 5.8 from Eq. 5.9, we express the correlation factor ρ in terms of the single- and two-qubit coherence times as:

$$\rho = \frac{T^*_{2,1}T^*_{2,2}}{4}\left[\left(\frac{1}{T^*_{2,|\Phi\rangle}}\right)^2-\left(\frac{1}{T^*_{2,|\Psi\rangle}}\right)^2\right]. \tag{5.10}$$

5.8.2. MEASUREMENT SETUP

The measurement setup used in this work is the same as the setup used by Watson *et al.* [25] and Xue *et al.* [23]. The measurements were done at a temperature of $T \approx 30$ mK in an external magnetic field of $B_{ext} = 617$ mT. DC voltages are set via filtered lines from room-temperature digital-to-analog converters. Tektronix 5014C arbitrary waveform generators (AWGs) are connected to gates P1 and P2 via coaxial cables for gate voltage pulses. Keysight E8267D vector microwave sources are connected to gates MW1 and MW2 for EDSR. I/Q input channels of the microwave sources are connected to a master AWG to control frequency, phase and duration of the microwave bursts via I/Q modulation. The phase of the microwave drive signal determines the rotation axis in the $\hat{x}-\hat{y}$ plane of the Bloch sphere, and we update the rotating reference frame in software to perform $\hat{z}$ rotations [44]. Pulse modulation is used to increase the on/off ratio of the microwave bursts. The master AWG also controls the clock of the entire system and triggers all the other instruments. Data acquisition is done by a Spectrum M4i.44 digitizer card that is installed in the measurement computer. This card records the sensing dot current traces at a sampling rate of ~60 kHz after passing through a 12-kHz Bessel low-pass filter (SIM965). Threshold detection is used to convert each trace to a single bit value (0 or 1) by the measurement computer. A schematic of the measurement setup is shown in Extended Data Figure 1 of Ref. [25].

5.8.3. QUBIT CHARACTERISTICS

For both qubits the microwave power is tuned to obtain a Rabi frequency of 2 MHz and a CPhase gate is performed in 90 ns. An upper bound on the residual exchange during single-qubit gates and free evolution of 100 kHz is determined from a decoupled CZ experiment with the detuning amplitude set to zero. Maximally a half exchange oscillation is observed in 5 µs.

	Q1	Q2
f	18.35 GHz	19.61 GHz
T_1	>50 ms [25]	3.7±0.5 ms [25]
T_2^*	0.97±0.02 µs	0.59±0.02 µs
T_2^{Hahn}	6.8±0.3 µs	2.8±0.2 µs
$F_{\|\Psi^+\rangle}$	0.88±0.02 [25]	
$F_{\|\Psi^-\rangle}$	0.88±0.02 [25]	
$F_{\|\Phi^+\rangle}$	0.85±0.02 [25]	
$F_{\|\Phi^-\rangle}$	0.89±0.02 [25]	

Table 5.1: Relevant single-qubit characteristics for simultaneous driving of both qubits, and Bell state fidelities F for the four Bell states. All errors are $\pm 1\sigma$ from the mean.

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5.8.4. REMOVING READOUT ERRORS

To remove errors in the measured two-spin probabilities $\mathbf{P}^M = (P^M_{|00\rangle}, P^M_{|01\rangle}, P^M_{|10\rangle}, P^M_{|11\rangle})^T$ caused by the limited readout fidelities $F_{|0\rangle}$ and $F_{|1\rangle}$ we use the relation $\mathbf{P}^M = (\hat{F}_1 \otimes \hat{F}_2)\mathbf{P}$, where

$$\hat{F}_i = \begin{pmatrix} F_{|0\rangle,i} & 1-F_{|1\rangle,i} \\ 1-F_{|0\rangle,i} & F_{|1\rangle,i} \end{pmatrix}, \tag{5.11}$$

to obtain the actual two-spin probabilities $\mathbf{P} = (P_{|00\rangle}, P_{|01\rangle}, P_{|10\rangle}, P_{|11\rangle})^T$. The readout fidelities are estimated from measurements of the spin-up probabilities P_1 and P_2 in experiments where we (1) initialize the qubit in $|0\rangle$ as described in Sec. 5.2, and (2) initialize the qubit in $|0\rangle$ and perform a π rotation:

$$\begin{aligned} P_{1,i} &= 1 - F_{|0\rangle,i} \\ \frac{P_{2,i}}{P_{\pi,i}} &= F_{|1\rangle,i} \end{aligned} \tag{5.12}$$

where i is the qubit number and $P_{\pi,i}$ is the expected spin-up probability after a π pulse on qubit i. The scripts used for this procedure are included in the Zenodo repository [43].

5.8.5. ERROR ANALYSIS

Error bars on the measured two-spin probabilities are estimated using a Monte Carlo method by assuming a multinomial distribution for the two-spin probabilities and binomial distributions for the readout fidelities, respectively. Random samples are taken from this distribution and readout errors are removed following the procedure above. This is repeated 1000 times and the final distributions are used to determine the mean

and standard deviations. The scripts used for this procedure are included in the Zenodo repository [43].

5.8.6. IMPROVE FITTING

To improve the fit of the decay, we add an evolution-time dependent phase to the first microwave pulse applied to Q2 after the delay time (see Z($\Delta\varphi$) in Fig. 5.3). The additional phase $\Delta\varphi$ is increased linearly with the delay time Δt. The added phase shift acting on Q2 affects the phase of the Bell state and consequently the $|00\rangle$ probability oscillates. The proportionality constant between $\Delta\varphi$ and Δt sets the frequency Δf of the oscillation of the $|00\rangle$ probability that results, $\Delta\varphi = \Delta f \cdot \Delta t$. Here we choose $\Delta f = 6$ MHz. The additional phase is applied by an update of the rotating reference frame in software in the same way as how we perform $\hat{z}$ rotations.

5.8.7. QUANTIFYING CORRELATIONS

In case the experimental data is not fully consistent with the simple quasistatic model, it is still possible to use this model to extract quantitative information on the correlations in the noise acting on the qubits based only on the two-qubit coherence times. From Eqs. 5.8 and 5.9, given the two-qubit coherence times, effective single-qubit coherence times can be calculated as:

$$\left(\frac{1}{T^*_{2,1(2)}}\right)^2 = \frac{\left(\frac{1}{T^*_{2,|\Phi\rangle}}\right)^2 + \left(\frac{1}{T^*_{2,|\Psi\rangle}}\right)^2}{4} \mp \frac{1}{2}\sqrt{\left(\frac{\left(\frac{1}{T^*_{2,|\Phi\rangle}}\right)^2 + \left(\frac{1}{T^*_{2,|\Psi\rangle}}\right)^2}{2}\right)^2 - 4\left(\frac{\left(\frac{1}{T^*_{2,|\Phi\rangle}}\right)^2 - \left(\frac{1}{T^*_{2,|\Psi\rangle}}\right)^2}{4\rho}\right)^2}, \tag{5.13}$$

where the minus (plus) sign corresponds to Q1 (Q2), assuming $T^*_{2,1} \geq T^*_{2,2}$. Solutions only exist if the argument of the square root is equal to or larger than zero, so for

$$|\rho| \geq \rho_{min} = \left| \frac{\left(\frac{1}{T^*_{2,|\Phi\rangle}}\right)^2 - \left(\frac{1}{T^*_{2,|\Psi\rangle}}\right)^2}{\left(\frac{1}{T^*_{2,|\Phi\rangle}}\right)^2 + \left(\frac{1}{T^*_{2,|\Psi\rangle}}\right)^2} \right|. \tag{5.14}$$

Using this simple model, we find a lower bound for the correlation factor $\rho_{min} = 0.27 \pm 0.02$.

Taking into account the experimental single-qubit coherence times and assuming their ratio ($\beta = \frac{T^*_{2,2}}{T^*_{2,1}}$) to be fixed, effective single-qubit coherence times can be obtained by adding Eqs. 5.8 and 5.9, and are given by:

$$\left(\frac{1}{T^*_{2,1}}\right)^2 = \left(\frac{\beta}{T^*_{2,2}}\right)^2 = \frac{\beta^2}{2(1+\beta^2)}\left[\left(\frac{1}{T^*_{2,|\Phi\rangle}}\right)^2 + \left(\frac{1}{T^*_{2,|\Psi\rangle}}\right)^2\right]. \tag{5.15}$$

The correlation factor ρ from Eq. 5.10 in that case is expressed as:

$$\rho = \frac{\beta\left(T_{2,1}^*\right)^2}{4}\left[\left(\frac{1}{T_{2,|\Phi\rangle}^*}\right)^2 - \left(\frac{1}{T_{2,|\Psi\rangle}^*}\right)^2\right]. \tag{5.16}$$

For the experimental value $\beta = 0.61 \pm 0.02$ ($T_{2,1}^* = 0.97 \pm 0.02$ µs and $T_{2,2}^* = 0.59 \pm 0.02$ µs), we find a correlation factor $\rho = 0.31 \pm 0.03$, and effective single-qubit coherence times $T_{2,1}^* = 0.84 \pm 0.03$ µs and $T_{2,2}^* = 0.51 \pm 0.02$ µs.

5.8.8. BELL STATE FIDELITIES

The Bell state preparation fidelities can in principle affect the noise correlations extracted from comparing the respective Bell state decays. Imperfect Bell state preparation can result in a finite overlap of the prepared state with Bell states of different symmetry. This will result in a combination of two decays and therefore affect the extracted coherence times and spatial noise correlations. In the present experiments, the Bell states have not been characterized, but for the Bell state density matrices presented in the Supplementary Information of Ref. [25], we determine the overlap of the prepared states with all four Bell states (see Tab. 5.2). The Bell state fidelities are on the diagonal of this table. The overlap of the prepared states with Bell states of different symmetry is 3–8%, so the contribution of the states with different symmetry is limited. In our experiments we indeed do not see deviations from a single decay and we expect the effect on the extracted spatial noise correlations to be limited.

	$\|\Phi^+\rangle$	$\|\Phi^-\rangle$	$\|\Psi^+\rangle$	$\|\Psi^-\rangle$
$\|\Phi^+\rangle_{\text{exp}}$	0.85	0.11	0.02	0.01
$\|\Phi^-\rangle_{\text{exp}}$	0.07	0.89	0.02	0.02
$\|\Psi^+\rangle_{\text{exp}}$	0.03	0.05	0.88	0.04
$\|\Psi^-\rangle_{\text{exp}}$	0.03	0.05	0.04	0.88

Table 5.2: Overlap of the four states experimentally prepared in Ref. [25] (rows) with the four orthogonal Bell states (columns), e.g. the overlap of the prepared $|\Phi^+\rangle_{\text{exp}}$ state with $|\Phi^-\rangle$ is 0.11. Only overlap with Bell states of different symmetry (indicated in red) results in a decay with a different timescale.

The main error sources that affect the Bell state preparation fidelities are dephasing due to nuclear spins and charge noise which impact the gate fidelities. Specifically, the two-qubit gate is performed by pulsing the detuning (instead of the tunnel barrier), which renders it first-order sensitive to charge noise.

5.8.9. ECHO EXPERIMENTS

Dynamical decoupling sequences can be used to investigate the frequency dependence of spatial noise correlations, similar to mapping out the frequency spectrum of noise acting on a single qubit [21, 22, 45]. In addition to the measurements analogous to Ramsey experiments, we performed measurements analogous to a Hahn echo experiment with a single decoupling pulse on each qubit halfway the waiting time. Results are presented in Fig. 5.4. We performed two versions of the echo experiment to which we refer

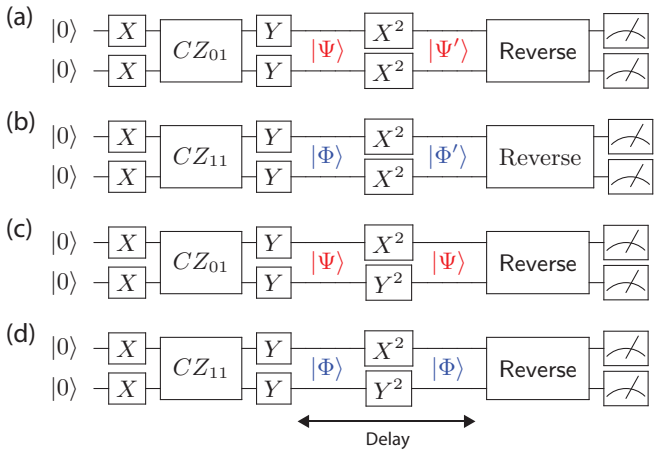

Figure 5.5: Circuit diagrams for two different versions ((a,b) XX and (c,d) XY) of an experiment analogous to the measurement of a Hahn echo for (a,c) $|\Psi\rangle$ and (b,d) $|\Phi\rangle$.

5

as XX and XY echo, respectively. In the XX echo experiment we apply a π_X pulse on both qubits, which transforms $|\Psi\rangle = (|\downarrow\uparrow\rangle - i\,|\uparrow\downarrow\rangle)/\sqrt{2}$ into $|\Psi'\rangle = (|\downarrow\uparrow\rangle + i\,|\uparrow\downarrow\rangle)/\sqrt{2}$, and $|\Phi\rangle = (|\downarrow\downarrow\rangle - i\,|\uparrow\uparrow\rangle)/\sqrt{2}$ into $|\Phi'\rangle = (|\downarrow\downarrow\rangle + i\,|\uparrow\uparrow\rangle)/\sqrt{2}$, as shown in the circuits in Figs. 5.5(a,b). The XY echo experiment consists of a π_X pulse on Q1 and a π_Y pulse on Q2, which transforms $|\Psi\rangle$ and $|\Phi\rangle$ to itself, as shown in the circuits in Figs. 5.5(c,d). The difference between the XX and XY sequences is analogous to that between single-qubit echo pulses around $\hat{x}$ versus $\hat{y}$. We do note that for both versions of the two-qubit decoupling used in this work, the two-qubit state is taken out of the logical qubit space during the pulses.

5.8.10. SIMULATION OF MULTIPLE ASYMMETRIC NOISE SOURCES

The result of a simulation of the combined effect of three asymmetric, correlated noise sources is shown in Fig. 5.6. The standard deviations of the distributions of fluctuations in difference and sum frequencies indicate that only modest correlations in the noise remain for their combined effect.

	Q1	Q2
P1	-1	-2
P2	0.175	0.8
MW1	-0.015	0.025
MW2	0.8	8.5
B	0.43	0.36
LD	-0.1	-1.44
accQD	0.9	-1.8
accRes	-0.8	-3.75

Table 5.3: Coupling factors (in MHz/mV) of eight of the surface gate electrodes on our sample to the two qubits.

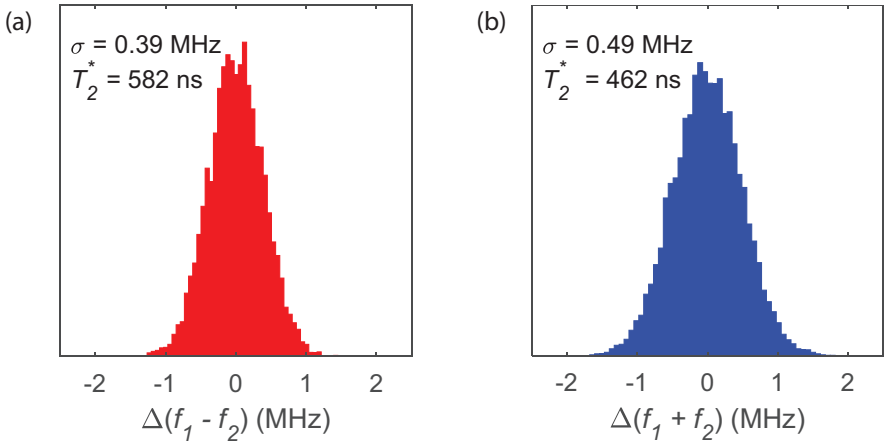

Figure 5.6: Simulation of three noise sources with coupling factors chosen to correspond to the experimentally measured coupling factors for three of the gate electrodes on the sample, namely P1, P2 and MW2 in Fig. 5.1(a). The coupling factors to the two qubits for these and five other gate electrodes are tabulated in Tab. 5.3. For all three gate electrodes, voltage fluctuations are sampled from a Gaussian distribution with 50 μV standard deviation. After sampling gate voltage fluctuations, the corresponding total frequency fluctuations for both qubits, and their difference and sum are calculated. The distributions of the fluctuations in (a) difference and (b) sum frequency are plotted.

5.8.11. ADDING MULTIPLE INDEPENDENT NOISE SOURCES

Consider a single noise source i with coupling strengths $\alpha_{i,1}$ and $\alpha_{i,2}$ (which can be expressed for instance in units of MHz/mV, if noise source i is expressed in units of mV) to qubit 1 and qubit 2, respectively. The noise source fluctuates with standard deviation σ. The standard deviations of the fluctuations in the difference $(f_1 - f_2)$ and sum $(f_1 + f_2)$ of the frequencies are then given by:

$$\begin{aligned} \sigma_{i,-} &= \sigma|\alpha_{i,1} - \alpha_{i,2}|, \\ \sigma_{i,+} &= \sigma|\alpha_{i,1} + \alpha_{i,2}|. \end{aligned} \tag{5.17}$$

For N independent noise sources the combined standard deviation is given by:

$$\sigma^2 = \Sigma_i^N \sigma_i^2. \tag{5.18}$$

Combining Eqs. 5.17 and 5.18 gives:

$$\begin{aligned} \sigma_- &= \sqrt{\Sigma_i^N \sigma_{i,-}^2} = \sigma\sqrt{\Sigma_i^N \left(\alpha_{i,1} - \alpha_{i,2}\right)^2}, \\ \sigma_+ &= \sqrt{\Sigma_i^N \sigma_{i,-}^2} = \sigma\sqrt{\Sigma_i^N \left(\alpha_{i,1} + \alpha_{i,2}\right)^2}, \end{aligned} \tag{5.19}$$

where we absorb differences in standard deviations between noise sources in the coupling strengths. Since $T_2^* \propto \frac{1}{\sigma}$, this yields:

$$\frac{T_{2,|\Phi\rangle}^*}{T_{2,|\Psi\rangle}^*} = \frac{\sigma_-}{\sigma_+} \propto \sqrt{\frac{\Sigma_i(\alpha_{i,1} - \alpha_{i,2})^2}{\Sigma_i(\alpha_{i,1} + \alpha_{i,2})^2}}. \tag{5.20}$$

This expression mathematically describes the possible effects of a combination of multiple noise sources on qubits that are described in Sec. 5.6. An extreme example described by this expression is that perfectly correlated and perfectly anti-correlated noise with equal amplitude combined are equivalent to uncorrelated noise.

Fluctuating background charges in the substrate, interfaces or dielectrics directly affect the qubit splitting because of the magnetic field gradient produced by the micromagnets. When these charges are located close to the dots, they will generally couple differently to the two qubits, introducing asymmetric noise. Specifically for charge fluctuators located in between the two dots, even anti-correlated noise may result. For distant charges, the coupling becomes more symmetric, but several factors can lead to asymmetric noise amplitudes even in this case, for instance a difference in the confining potential between the two dots or a difference in the strength of the local magnetic field gradient. We have clear evidence of a pronounced difference in the confining potential of the two dots in this sample, based on the sensitivity of the respective qubit splittings to changes in gate voltages (see Tab. 5.3). Similar considerations apply to the effect of gate voltage noise, which also couples to the qubit splitting through the magnetic field gradient.

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6

A Sparse Spin Qubit Array with Integrated Control Electronics

Current implementations of quantum computers suffer from large numbers of control lines per qubit, becoming unmanageable with system scale up. Here, we discuss a sparse spin-qubit architecture featuring integrated control electronics significantly reducing the off-chip wire count. This quantum-classical hardware integration closes the feasibility gap towards a CMOS quantum computer.

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6.1. INTRODUCTION

SEMICONDUCTOR spin qubits [1, 2] are an attractive platform for large-scale quantum computers, due to their potential compatibility with well-established semiconductor manufacturing processes. In the last decade, we have witnessed tremendous progress in the development of spin qubit hardware [3–8] and significant interest and contribution of the semiconductor industry into spin qubit research [9–11]. Therefore, the open questions surrounding the challenge of scaling up [12] have become timely and highly relevant. One of the main issues in common with all nanoelectronic qubits is that current implementations require at least one external control line for every qubit. The small pitch of quantum dots (Fig. 6.1) permits extremely dense qubit arrays but aggravates the interconnect challenges. Existing proposals for dense 2D spin qubit arrays [13, 14] assume either a device density or material homogeneity that remains to be achieved. Another approach involves a network architecture, where qubits are arranged in small-cluster nodes, interconnected by long-range entanglement distribution channels, with the goal of creating space for easing the density requirements of the interconnects [12]. The feasibility of implementing quantum error correction protocols using this approach has been thoroughly analyzed [15], but the description of the physical implementation is largely missing. Here, we present a design of a sparse two-dimensional array whereby classical electronics integrated locally with the quantum hardware is used to minimize the need for off-chip interconnects and hence with a scalable Rent's exponent [16]. We first describe the components of the array and the implementation of quantum gates and measurements, followed by a description of the control electronics required to operate the qubits in the array and correct errors via the surface code approach [17]. We then analyze how this implementation of locally integrated electronics reduces the number of connections at the quantum plane boundary, and the required footprint of such components. Finally we provide a discussion of some of the technological considerations, potential challenges and options for solving them.

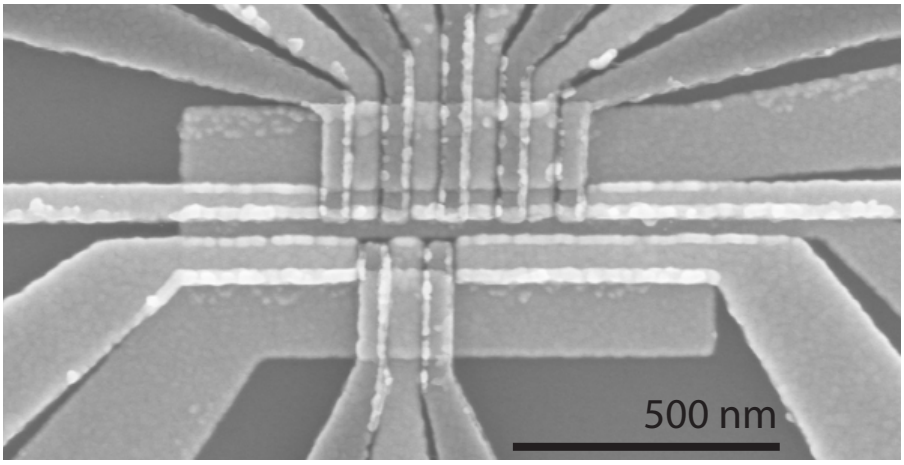

Figure 6.1: Image of a set of gate electrodes from a state-of-the-art device of electrostatically defined quantum dots.

6.2. ARRAY DESIGN

We propose a quantum computing architecture consisting of a two-dimensional array of electron-spin qubits using linear arrays of gate electrodes (Fig. 6.1) arranged to form a square lattice of electrostatically-defined quantum dots with nearest-neighbor connectivity. In conventional spin qubit designs, every quantum dot, with a typical pitch smaller than 100 nm, hosts a qubit. The proposed design uses a *sparse* qubit array with the qubits separated by ~12 µm, while the vertices are connected via electron shuttling channels to transport electrons to and from interaction regions. The array's sparseness enables the integration of sample-and-hold circuits alongside the quantum dot circuitry allowing to offset the inhomogeneities in the potential landscape across the array by independent DC biasing while sharing the majority of control signals for qubit operations across the array. The latter allows for a significant reduction in the number of connections at the quantum plane boundary. As detailed in Fig. 6.2, we start from a 22 mm × 33 mm (726 mm^2) die. The qubits are defined in the *quantum plane*, a section of the die consisting of M×M *modules*, each containing N×N *unit cells*. The unit cell is the smallest operational unit, containing four qubits along with all the elements required to operate them, as described in Fig. 6.3. Qubits remain at the vertices of the lattice while idle and are shuttled to the operation regions between the vertices in order to perform single- and two-qubit operations as well as readout and initialization.

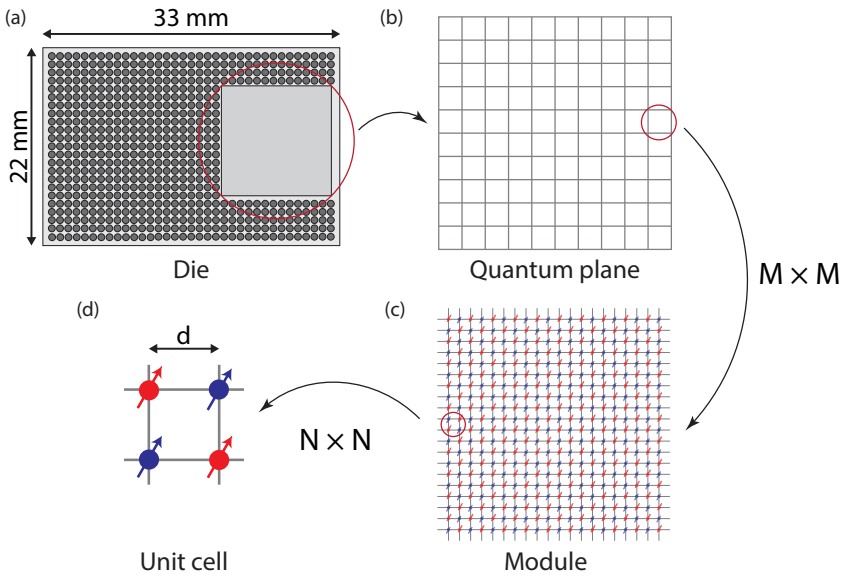

Figure 6.2: Overview of the qubit architecture with a schematic breakdown of its components as described in the main text, including (a) the die containing (b) the quantum plane area, highlighting a single (c) module which contains a set of (d) unit cells. Qubits are color coded to distinguish data qubits (blue) and ancilla qubits (red), as defined in the surface code.

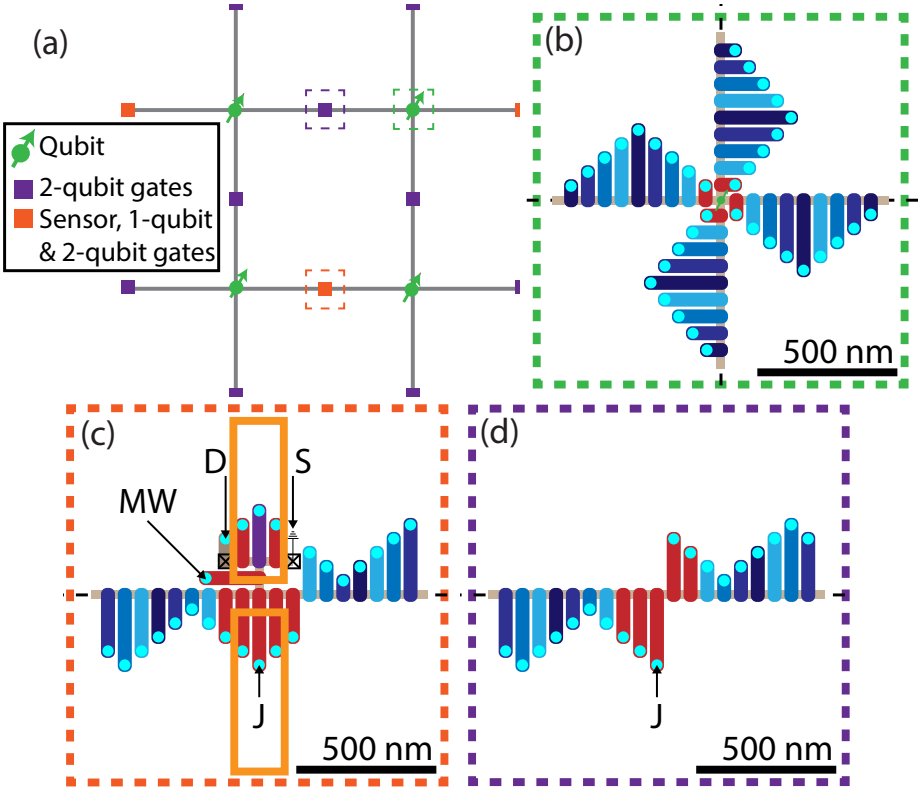

Figure 6.3: (a) Schematic (not to scale) of a unit cell containing four spin qubits (green), qubit operations regions (purple/orange), connected via shuttling channels (grey lines). (b) Qubit idling region. Four barrier gates (red) define the confinement potential and allow qubits into the shuttling channels (grey). Cyan circles represent vias. (c) Qubit operations region including control gates (red), sensing dot plunger (purple), source (S)/drain (D) ohmics (squares) and micromagnets (orange rectangles). (d) Two-qubit operation only regions.

6.3. DC BIASING

FIGURE 6.4 shows circuit schematics of locally integrated sample-and-hold circuits providing individual DC biasing of all the control gates, which total 64 gates per unit cell. Gate voltages within a unit cell are updated sequentially via four local demultiplexers that each distribute DC voltages generated remotely (i.e., outside the quantum plane) to 16 local capacitors connected to the gates. All demultiplexers within a module share the same input DC biasing signal, and all demultiplexers in the quantum plane share the same address bus (see Fig. 6.4(f)). The demultiplexers are enabled sequentially and in turn sequentially update each gate. In this way, all modules are updated in parallel and therefore one module refresh cycle is required to refresh the entire qubit array. We define two bias voltage resolutions, based on the gate functionalities. Gates acting as barriers to shuttling channels only require a resolution sufficient to maintain an electron in a quantum dot and therefore we can afford a coarse resolution of 1 mV. All other plunger and barrier gates require a resolution of 1 μV [12]. The minimum hold capacitance required

to achieve the coarse resolution is ~0.16 fF (limited by the electron charge $e/\Delta V$), while the fine resolution requires ~14 pF (limited by thermal noise $k_B T/C$, assuming power dissipation from the local electronics raises the operating temperature to 1 K). The gate voltage refresh rate will be set by the current leakage of the hold circuit and the time required to update each gate, which in turn will set the module size (i.e., the number of unit cells, and therefore total gates, which can be sequentially updated).

6.4. SIGNALS FOR QUBIT OPERATIONS

ALL the qubit operations are performed by shuttling the qubits to the operation regions and applying pulsed signals to the appropriate gates to perform the operations.

The shuttle channels are defined by a linear array of gates (blue gates in Fig. 6.3), along which a traveling wave potential can trap and shuttle an electron. The traveling wave potential is generated using four phase-shifted sinusoidal signals on four consecutive gates (different shades of blue in Fig. 6.3), with the signals being reused every fifth gate. The shuttling signals are always on and the phase shifts control the direction of shuttling. With the use of a barrier gate (Fig. 6.3(b)), an electron can be forced to tunnel into a shuttle channel. The amplitude of the traveling wave potential is made large enough to overcome the inhomogeneities in the potential landscape, eliminating the need to apply DC biasing on the shuttling gates.

Single-qubit gates are performed by applying a microwave pulse to the control gate labeled MW in Fig. 6.3(c). A pair of micromagnets in this operation region provide magnetic field gradients required to perform electric dipole spin resonance (EDSR) [18]. A two-qubit gate is performed by pulsing the control gate labeled J, to activate an exchange interaction between electrons underneath the adjacent gates. In order to apply the AC signals on gates that also require DC biasing, we make use of a complementary switching circuit (see φ_{AC} and $\overline{\varphi_{AC}}$ in Fig. 6.4(b)).

The surface code is sustained using a cyclic sequence of pulsed signals within a unit cell, with the same sequence performed in parallel across all unit cells in the entire array. A set of remote pulsed voltage sources is used to generate the required cyclic pulsed signals at each gate (i.e., one source per pulsed gate in a unit cell). Logic gates in the surface code with lattice surgery are achieved by creating defects in the lattice. We implement these defects by preventing shuttling of a subset of data qubits via locally integrated switches.

6.5. READOUT

QUBIT readout is performed at the operation region shown in Fig. 6.3(c). A readout quantum dot connected to source/drain ohmic contacts is used for charge sensing and spin readout is achieved via spin-to-charge conversion based on Pauli spin blockade [2]. Additionally, the ohmics in this region provide electrons that are shuttled to the unit cell vertices to initialize the array.

The drain contacts of all readout dots in a module are connected to a single line at the quantum plane boundary, and readout is performed sequentially across the unit cells of each module, while the modules are read out in parallel. This is achieved by sequentially

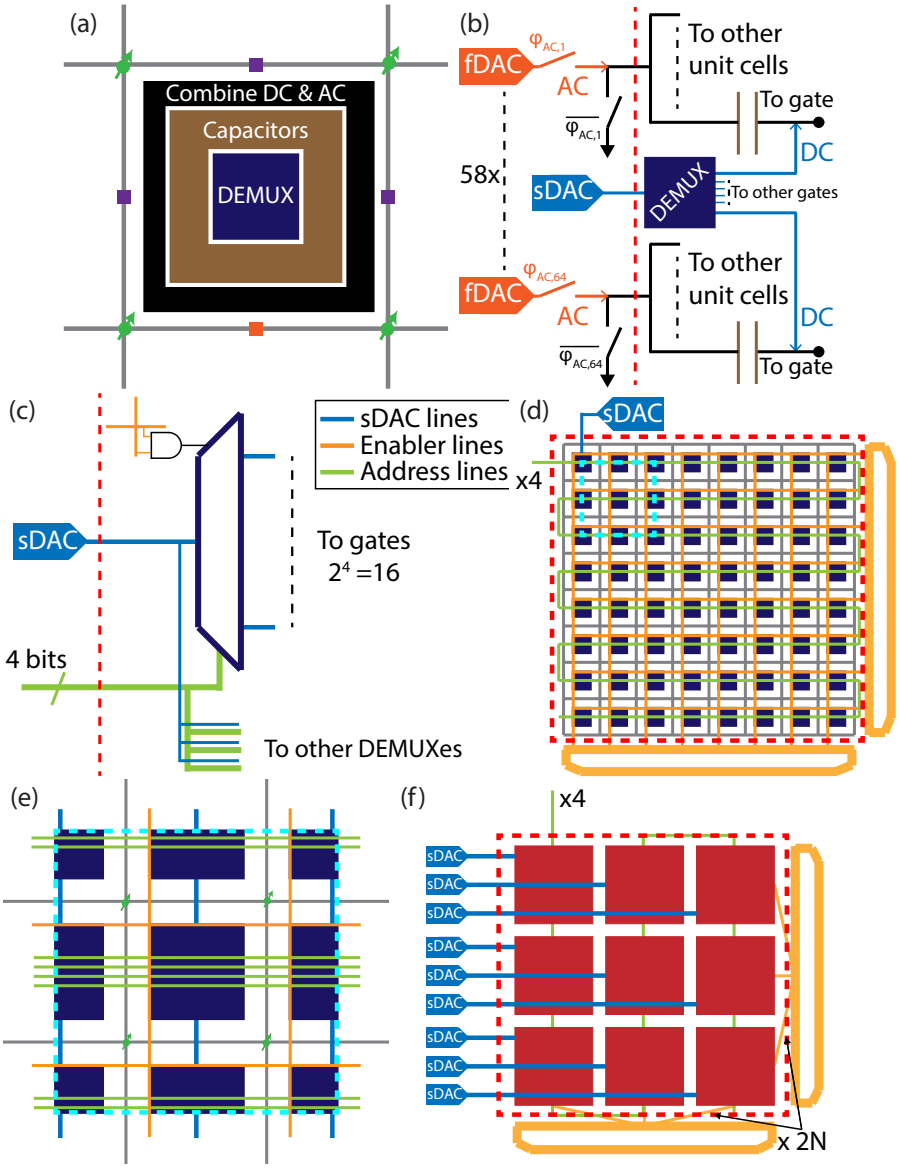

Figure 6.4: (a) Schematic of a unit cell with locally integrated classical electronics. The color coding represents the same components in all the panels. (b) Circuit schematic of the components in (a), with the functionality described in the main text. fDAC (sDAC) are voltage sources for pulsed signals (DC biasing). Dashed red lines denote the quantum plane boundary in this and following panels. (c) Input/output schematic of the demultiplexer. (d) Schematic of a module. Demultiplexers are sequentially enabled by crossbar addressing controlled by multiplexers (orange blocks). (e) Zoom into the area surrounding a single unit cell in (d). (f) Schematic of the array of modules completing the quantum plane.

pulsing every sensor plunger in a module to the low-impedance, electrostatically sensitive regime while all other sensors in the module are at high-impedance (i.e., Coulomb blockade). The sequential control of the plungers in a module is achieved using a global readout demultiplexer that can be shared between all modules across the entire array.

6.6. LINE SCALING

THE signal routing we have described (as summarized in Tab. 6.1), enabled by the described DC biasing scheme, allows for a very efficient scaling of the ratio of connections needed at the unit cell level to connection outputs at the quantum plane boundary. Considering that the total number of gates scales with the number of qubits ($4M^2N^2$), we now discuss how the operation schemes described above allow scaling down the number of connections at the quantum plane boundary.

The sparse array with sample-and-hold circuits provides independent DC biasing with $O(M^2+N)$ lines at the quantum plane boundary. All pulsed and microwave control signals needed to sustain the surface code, can be shared across every unit cell in the entire array. This amounts to a constant number of 58 lines at the quantum plane boundary irrespective of the number of qubits. The signal lines used to control the switches that deactivate data qubits for the logical qubit implementation scheme, are arranged in a crossbar fashion across the entire quantum plane, reducing the number of lines for this purpose to as few as $O(MN)$ at the quantum plane boundary. In practice, we propose to use x crossbars over the entire array, in order to allow for x defects to be simultaneously created and manipulated, bringing the line scaling to $O(xMN)$. By using decoding to address the readout plungers per module, the sequential readout scheme obtains a line scaling at the quantum plane boundary as $O(M^2+log(N))$. At the boundary of the quantum plane, Rent's exponent can thus be as low as p=0.5.

Shuttling gates (blue)	Source → gate
Pulsed gates (red)	DC: source → local demultiplexer → gate AC: source → gate
Sensing dot plunger (purple)	DC: source → local demultiplexer → gate AC: source → global demultiplexer → gate
Drain contacts	Measurement device ← ohmic

Table 6.1: Summary of signal routing for the four different type of control lines in the array design.

6.7. FOOTPRINT

WE now consider the footprint requirements of the control electronics that need to be locally integrated in the quantum plane, and the wire density at various levels.

The bulk of the footprint will be taken up by the capacitors required for the sample-and-hold scheme. Coarse resolution is required for 32 gates and another 32 gates require fine resolution, which comprise a total capacitance per unit cell of ~450 pF. Assuming ~1 pF/μm^2 (using state-of-the-art deep-trench capacitor technology [19]), we estimate a total capacitor footprint of ~450 μm^2. In addition, we modeled a demultiplexer circuit using 40-nm technology, extrapolated to 28-nm technology and obtained an estimate

of the total footprint of the DC biasing and readout demultiplexers of ~60 μm^2 per unit cell. This adds to a total footprint per unit cell of ~510 μm^2, which allows to set the qubit pitch to $d \geq 12$ μm. Assuming a 50 nm pitch between gate electrodes (Fig. 6.1), this would require linear arrays of 240 gate electrodes per lattice arm. A unit cell has an area $4d^2 \approx 576$ μm^2 and a perimeter $8d \approx 96$ μm. O(10^2-10^3) wires pass through the unit cell perimeter, using multiple interconnect layers. The area and perimeter for a module are $(2dN)^2$ and $8dN$, respectively, and the quantum plane has an area and a perimeter of $(2dNM)^2$ and $8dNM$, respectively.

For a total of 2^{20} ($\approx 10^6$) qubits, the total area covered by the quantum plane is ~151 mm^2, leaving ~575 mm^2 of space remaining in the die, which can be used to implement classical control circuits and to bring the wire count going off-chip, typically the real bottleneck for Rent's rule, to well below the wire count at the quantum plane boundary by means of additional levels of multiplexing.

6.8. DISCUSSION AND OUTLOOK

VERY large-scale spin qubit devices will ultimately be based on a trade-off of a large number of considerations. With this proposal, we explore the extreme sparse approach, with single qubits placed at the nodes of the shuttling channels. Different from some existing proposals, this approach does not make strong assumptions on the potential landscape homogeneity or the density with which transistors and qubits can be integrated, but it does assume that spins can be shuttled over 10-μm distances with very high fidelity. It should also be possible to design a similar integrated electronic scheme for architectures with larger qubit-cluster nodes, for which it has been shown that the fidelity requirements of the shuttling channels are more relaxed [15]. We also assume that magnetic field inhomogeneities and g-factor variations can be overcome by individual DC tuning.

In this work, we have focused on the reduction of the number of control lines at the quantum plane boundary, as well as on the footprint of the classical control electronics, a key first step to assess the feasibility of implementing sparse spin qubit architectures, which motivates future work into addressing the following open issues. Distributing all signals for qubit operations across the entire qubit array requires careful design for minimizing crosstalk, along with to estimate the total line capacitance, which will affect clock speeds and required source power. There will be a large number of switches, used to separate the cycles of DC biasing and qubit operation on the applied gate voltages, and to perform lattice surgery. The power dissipated by these switches can be significant and will be a factor in considering the clock rates of the system and the achievable operating temperature. It is most likely that both the surface code cycle rate and the size of the array will be limited by the number of sequential readouts required, since this is the most time consuming of all operations. Some degree of parallel readout can be implemented by amplitude modulation or frequency modulation. If that is not sufficient, smaller readout modules can be defined, each consisting of a subset of unit cells that are read sequentially. This comes at the expense of an increased number of readout connections. All things considered, this proposal provides an appealing outlook for the long-term implementation of larger scale quantum computing chips, and provides guidance for near-term research at the quantum, classical and integrated levels.

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7

CONCLUSION AND OUTLOOK

Harnessing the true power offered by quantum mechanics for quantum computing applications requires large-scale, error-corrected devices consisting of millions of qubits. My work over the last four years, as has been presented in this dissertation, had the overarching goal to study different aspects that are relevant in scaling up the number of qubits. In this final chapter, I will summarize my work and draw some conclusions. Moreover, I will outline some important next steps towards the development of fault-tolerant large-scale quantum computers based on silicon spin qubits.

7.1. CONCLUSION

IN order to realize large systems of qubits that can be efficiently controlled, all qubits need to be functional and they need to have predictable properties. For this, it is required to be able to reliably and reproducibly fabricate qubit devices. Although large-scale qubit systems will not be fabricated in academic cleanrooms, the crucial foundations are laid out in exactly those environments. Here, proof-of-principle devices will be fabricated and several design variations will be tested, before transferring a certain design to industrial cleanrooms. Industrial fabrication is generally less flexible, and the (re)design, production and validation of rather involved photolithography masks, as well as the subsequent process development, takes a considerable amount of time. Therefore, the development of an integration scheme as I presented in Ch. 3 is of fundamental importance in order to allow for relatively flexible fabrication of increasingly complex device designs in academic cleanrooms. Chapter 4 of this dissertation, as well as the work by Lawrie *et al.* [1], shows the successful application of this scheme.

A quantum computing chip containing millions of qubits will likely require on-chip co-integration of qubits with classical control electronics to allow for a reduction of the number of control wires going in to and out of the chip, and to facilitate some local control. The power dissipation associated with such classical control electronics cannot be dealt with by the limited cooling power of dilution refrigerators (~10 μW) at the current qubit operation temperature (~10 mK). Yet, the cooling power available at ~1–4 K

is likely to already be sufficient for this purpose (e.g. the eight cryocoolers that cool the magnets of CERN's Large Hadron Collider each provide a cooling power of ~2.5 kW at 1.8 K [2]). For that reason, both bringing classical control electronics to lower temperatures (see e.g. Ref. [3]) and simultaneously increasing the operation temperature of semiconductor spin qubits to 1–4 K are active areas of research, such that they meet at an intermediate temperature. We studied the feasibility of high-temperature operation of Si-MOS spin qubits, as presented in Ch. 4. We find a spin relaxation time $T_1 = 2.8$ ms at 1.1 K, more than an order of magnitude longer than the longest spin coherence time T_2^* in silicon spin qubits [4]. We show how this spin lifetime can be improved even further by operating at low magnetic field and by employing high-valley-splitting devices. Furthermore, charge noise is shown to depend only linearly on temperature. This work is a first step in demonstrating the suitability of Si-MOS spin qubits for high-temperature operation and consequently the integration with classical control electronics. More recently, other work has shown gate-based spin readout up to 0.5 K [5], coherent single-spin control at ~1.45 K [6] and universal quantum logic at 1.1 K [7]. Yang *et al.* [6] demonstrated the temperature dependence of the qubit coherence time T_2^* and Hahn echo time T_2^{Hahn} to be even weaker than the T_1 temperature dependence, and Petit *et al.* [7] showed readout via Pauli spin blockade, single-qubit fidelities around 99% and coherent two-qubit interaction. All these experiments together show that there are no fundamental limitations to operate silicon spin qubits at elevated temperature, which allows for the required on-chip integration with classical electronics.

Fault-tolerant large-scale quantum computers will have to rely on quantum error correction (QEC) and most of these schemes assume negligible correlations in errors on individual qubits. In Ch. 5, we find that the noise on the two qubits that causes these errors is uncorrelated to a large extent. In addition, we gain insight in the origin of the only modest spatial correlations. We interpret the data by multiple distant charge fluctuators with asymmetric coupling to the two qubits in our experiment in combination with nuclear spins. Performing similar experiments in isotopically purified silicon devices is interesting in order to assess the spatial correlations arising from charge noise only. Furthermore, our insights show that spatial correlations in the noise can be engineered through the design of qubit devices to either maximize or minimize these correlations. QEC schemes able to deal with certain types of correlations in the qubit errors do already exist [8]. Therefore, the prospects for the development and implementation of quantum error correction schemes in fault-tolerant large-scale quantum computers, in combination with qubit device designs that consider the effect on error correlations, are promising.

In the above, we have studied several aspects that are relevant to determine the suitability of silicon spin qubits for the use in large-scale quantum computers. Additionally, in this respect silicon spin qubits are usually claimed to be fully compatible with conventional CMOS fabrication, allowing for the co-integration of qubits and conventional electronics on a single chip [9]. However, while this is certainly true at the fundamental level, gaps have to be closed to fully justify this claim. For example, although there are proposals in this direction [10, 11], these make assumptions that remain to be validated. Quantum error correction in a sparse two-dimensional array has been studied [12, 13],

but a concrete, realistic proposal for a physical implementation that co-integrates qubits and classical electronics in a sparse array was still missing. The proposal in Ch. 6 does focus on exactly this lacuna and assesses what classical electronics is required locally, as well as the corresponding footprint, line scaling and interconnect density. Its unit cell design, with individual local control and shared global control, is scalable and allows 2^{20} ($\approx 10^6$) qubits to fit in ~150 mm^2. In this proposal, we have sketched an appealing outlook for the longer-term implementation of larger-scale quantum computing chips.

7.2. OUTLOOK

THE results presented in this dissertation, in combination with other recent developments, constitute relevant progress towards large-scale silicon spin qubit devices. The work in Ch. 6 starts with a high-level picture of a large-scale spin qubit array, as shown in Fig. 7.1. However, the progress does not mean we are there yet and work has to be done for such devices to be built. In this section, I will look ahead and describe crucial developments towards a large-scale spin qubit based quantum computer.

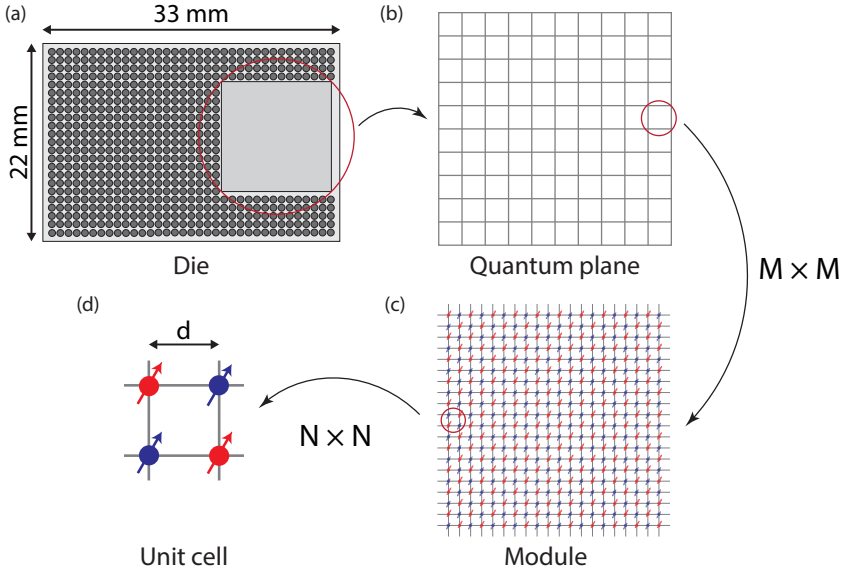

Figure 7.1: Overview of a possible spin qubit architecture showing (a) the die, (b) the quantum plane area, (c) a module and (d) the unit cell. Reprinted from Ch. 6.

7.2.1. QUBIT FABRICATION

Large-scale qubit device, as for example the one shown in Fig. 7.1, will not be built in academic cleanrooms. For this reason, the considerable attention that quantum computation has drawn from industry over the last few years is indispensable. Specifically silicon spin qubits are of interest for CMOS foundries, because of their assumed compatibility with conventional CMOS fabrication. Intel [14], CEA-Leti [15] and STMicroelec-

tronics [16] have employed their facilities for the fabrication of silicon spin qubit devices, and also Imec has a similar project.[1] The industrial devices fabricated by Intel by now show promising, reproducible results. It is only a matter of time before the first industrial electron-spin qubit will be demonstrated, and benchmarking its performance will be of significant interest and importance. Once at that stage, it is not unreasonable to expect an accelerated increase in qubit number and qubit performance, which will allow for an excellent test bed for (small-scale) quantum algorithms and quantum error corrections schemes. However, industrial two-dimensional qubit arrays will most likely still require significant process developments, but will be indispensable for the development of large-scale spin qubit devices. Additionally, co-integration of qubits with classical electronics has been shown on the small scale, but a large-scale implementation in industrial devices will presumably face new, currently unforeseen challenges. Specifically, for the sparse spin qubit array proposed in Ch. 6 floating gates based on sample-and-hold circuits [17] in industrial devices are a crucial ingredient.

On the other hand, fabrication in academic cleanrooms is more flexible and will remain important for exploring different approaches before transferring the most promising ones to industrial foundries. Integration schemes such as the one presented in Ch. 3 have led to the fabrication of more and more complex qubit devices; currently the longest linear one-dimensional array consists of nine quantum dots [18]. Other efforts have facilitated the integration of semiconductor spin qubits with resonators [19–21]. All these devices allow research groups all around the world to perform increasingly more intricate experiments with an increasing number of qubits, which are aided by predictable and reproducible qubit properties. Nevertheless, so far no experiments with more than two silicon spin qubits have been performed. Two-dimensional quantum dot arrays have been fabricated in GaAs, both 2×2 [22, 23] and 3×3 [24] geometries, but hitherto two-dimensional devices in silicon are scarce while the very few existing attempts follow an unconventional approach [25, 26]. Increasing the number of qubits in a one-dimensional array will remain relevant, but it is important to gain experience with two-dimensional arrays in silicon, since their increased connectivity has significant advantages for quantum error correction [27] and quantum algorithms. It is therefore recommended to devote efforts to two-dimensional qubit arrays and first endeavors in this direction are underway.

7.2.2. QUBIT OPERATION

In order to operate future large-scale spin qubit based quantum chips (e.g. Fig. 7.1), several advancements in qubit operation are vital, despite all the progress over the last years. Here, I will list a few. The first few are mostly relevant at the level of individual qubits (see Fig. 7.1(d)), and at the end I will briefly discuss some that are relevant at the higher levels of the qubit array.

A universal, high-fidelity gate set has been demonstrated both at base temperature and at elevated temperature, but not all gate fidelities are above the fault-tolerant threshold of ~99% yet. The two most pressing challenges are improving the two-qubit gate and readout fidelities. Possible approaches to improve all gate fidelities are the reduction

[1] Only Intel uses an all-optical lithography process, while the others employ a combination of optical and electron beam lithography.

of charge noise, potentially through cleaner fabrication techniques in industrial facilities, and reducing the ^{29}Si concentration even further. Furthermore, employing pulse shaping and optimization (e.g. through GRAPE [28]), instead of the now commonly used square pulses, can improve both single- and two-qubit gate fidelities. Specifically the fidelity of the exchange-based two-qubit gate can be improved by symmetric operation in which the tunneling coupling is pulsed instead of the detuning between the two qubits [29, 30], which renders the gate first-order insensitive to charge noise.

Currently, the most commonly used readout scheme relies on so-called *Elzerman* readout [31] in combination with a sensing quantum dot [32]. Both Elzerman readout and the use of a sensing dot have a disadvantage for space reasons. Elzerman readout requires the quantum dot to be read out to be connected to a reservoir for energy-selective tunneling; a sensing dot is an additional structure right next to the qubits. To circumvent the need for an electron reservoir, one could employ Pauli spin blockade (PSB) for readout [33], instead of energy-selective tunneling. An alternative to a sensing dot is to use gate-based dispersive readout [34], in which the gate electrodes that are used to define the quantum dot are employed as sensor. Several groups have recently achieved fast spin readout with this latter method [5, 35–37]. A disadvantage of this technique, as well as of an RF sensing dot [32], is the required resonant circuit, which might be incompatible with the omnipresent dielectrics in CMOS fabrication that reduce the resonator's quality factor through dielectric losses. However, readout based on transport through a sensing QD is slow, so finding the optimal readout scheme for industrial spin qubits is an outstanding challenge.

In order to tune qubit devices with an increasing number of qubits, (automated) tuning routines are required to perform this task efficiently, especially for the current devices where qubits have their own personality and therefore all require different settings. Several of such routines have already been demonstrated, such as virtual gates [38], the 'n+1 method' [39, 40], and the automated tuning of a double quantum dot in the single-electron regime [41], inter-dot tunnel coupling [42] and an S-T_0 qubit [43]. Furthermore, machine learning techniques are already being used to facilitate fast and reliable automated tune-up of spin qubit devices [44–47].

Apart from the necessary developments for the industrial fabrication of large-scale qubit devices with integrated classical electronics, operation schemes will have to be developed, tested and optimized. As first step, automated tuning routines, aided by machine learning, will also be of crucial importance to tune and calibrate such devices. Additionally, protocols and algorithms have to be developed to run the surface code (or any other QEC scheme) and perform actual quantum calculations. Specifically, the array design proposed in Ch. 6 relies on high-fidelity shuttling of electrons. Proof-of-principle experiments have been done [48–50], but long-distance shuttling remains to be shown and is an important milestone towards the proposed array.

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A

INTEGRATION SCHEME

This appendix details the integration scheme for Si-MOS spin qubits that has been developed as part of the work presented in Ch. 3. Even more (and more recent) details on the fabrication can be found in the QuTech SoloDB.[1] Fabrication recipes are always being adapted to the latest insights and experiences, and therefore subject to change. For that reason, it might be possible that this integration scheme does not reflect exactly how silicon spin qubit devices are currently fabricated in QuTech, but it does list the steps I would take if I would start a full fabrication run in the Kavli cleanroom today. It does not take into account prefab in the EKL cleanroom, which would replace steps (a-d).

Before listing the step-by-step recipes, there are some general remarks to make:

- It is recommended to limit variability and to control process variables as much as possible. However, some variability is inevitable in an academic cleanroom, so no unreasonable time and effort should be put into controlling variables that are likely to not have any effect and/or are smaller than other uncontrollable variations. Still, parameters that are relatively easy to keep constant should be kept constant, even though they are not expected to influence to process.
- The process below describes the fabrication of Si-MOS spin qubits, but minor adjustments to account for differences in the material systems, allow this process to be applied to the other group IV material systems silicon/silicon germanium (Si/SiGe) and germanium/silicon germanium (Ge/SiGe) as well.
- The spinners used for spin coating are programmed to initially revolve at 500 rpm for 5 s before spinning up to a variable speed for another 55 s. The spin speeds quoted below reflect this variable speed.
- Baking is done on a hotplate. To prevent contamination, a support wafer is used. The temperatures quoted reflect the temperature on top of the support wafer.
- During development and lift-off a magnet is used for stirring.

[1] https://qtechserv.tnw.tudelft.nl/user/login

A

(a) **Tungsten markers**

Surface treatment and spin coating

- Surface treatment - acetone - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry
- Prebaking - 180°C - 5:00 min.
- Spin coating - MMA(8.5)/MAA EL8 - 2000 rpm (target: 340 nm)
- Baking - 180°C - 5:00 min.
- Spin coating - PMMA A4 950 - 2000 rpm (target: 275 nm)
- Baking - 180°C - 5:00 min.

Lithography

- Electron beam exposure - 900 $\mu C/cm^2$
- Developing - MIBK:IPA 1:3 - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry

Metalization

- Sputtering - tungsten (W) - ~100 nm
- Lift-off - acetone - 50°C - 2:00 h
- Rinsing - isopropanol (IPA) - 5:00 min.
- N_2 dry
- O_2 plasma - 0.43 mbar - 120 W - 10:00 min.

(b) **Ohmic regions**

Surface treatment and spin coating

- Surface treatment - acetone - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry
- Prebaking - 180°C - 5:00 min.
- Spin coating - MMA(8.5)/MAA EL8 - 2000 rpm (target: 340 nm)
- Baking - 180°C - 5:00 min.
- Spin coating - PMMA A4 950 - 2000 rpm (target: 275 nm)
- Baking - 180°C - 5:00 min.

Lithography

- Electron beam exposure - 1000 $\mu C/cm^2$
- Developing - MIBK:IPA 1:3 - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry

Ion implantation

- Glue chips on 4" support wafer with tiny drop of PMMA A2
- Baking - 120°C - 5:00 min.
- Implantation - phosphorus (P^+) - 6 keV - 10^{16} cm^{-2} - 7° tilt

Resist strip

- O_2 plasma - 0.43 mbar - 120 W - 10:00 min.
- Cleaning - acetone - 50°C - 2:00 h
- Cleaning - acetone - 50°C - 1:39 h (ultrasound)
- Cleaning - acetone - 50°C - 2:00 h
- Cleaning - acetone - 20°C - overnight
- Cleaning - acetone - 50°C - 5:00 min.
- Rinsing - isopropanol (IPA) - 5:00 min.
- N_2 dry
- O_2 plasma - 0.43 mbar - 120 W - 10:00 min.

Activation anneal

- Rapid thermal anneal - forming gas (5% H_2, 95% N_2) - 1000°C - 30 s

(c) **Ohmic contacts and platinum markers**

Surface treatment and spin coating

- Surface treatment - acetone - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry
- Prebaking - 150°C - 3:00 min.
- Spin coating - CSAR 0.04 - 4000 rpm (target: 90 nm)
- Baking - 150°C - 3:00 min.

Lithography

- Electron beam exposure - 300 $\mu C/cm^2$
- Developing - pentyl acetate - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry

Etch

- Post-baking - 120°C - 10:00 min.
- Etching - buffered HF 7:1 - 15 s
- Rinsing - H_2O - 30 s
- Rinsing - H_2O - 1:00 min.
- N_2 dry

Metalization

- Evaporation - titanium (Ti) - 5 nm - 0.5 Å/s
- Evaporation - platinum (Pt) - 55 nm - 2 Å/s
- Lift-off - AR 600-71 - 40°C - 2:00 h (ultrasound)
- Rinsing - isopropanol (IPA) - 5:00 min.
- N_2 dry
- O_2 plasma - 0.43 mbar - 120 W - 10:00 min.

(d) **Bond pad protection**

Surface treatment and spin coating

- Surface treatment - acetone - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry
- Prebaking - 200°C - 3:00 min.
- Spin coating - MMA(8.5)/MAA EL8 - 4000 rpm (target: 250 nm)
- Baking - 200°C - 3:00 min.
- Spin coating - CSAR 0.13 - 4000 rpm (target: 400 nm)
- Baking - 170°C - 3:00 min.

Lithography

- Electron beam exposure - 500 µC/cm^2
- Developing - pentyl acetate - 3:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- Developing - H_2O:IPA 1:3 - 3:00 min.
- Spin dry

Deposition

- Sputtering - silicon nitride (SiN) - 150 nm
- Lift-off - AR 600-71 - 40°C - 30:00 min. (ultrasound)
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry
- O_2 plasma - 0.43 mbar - 120 W - 10:00 min.

(e) **Aluminum oxide blanket**

Isolation layer

- UV ozone - 2:00 min. (see [2])
- Atomic layer deposition - aluminum oxide (Al_2O_3) - 300°C - 10 nm

[2] UV ozone treatment is optional and only required if atomic layer deposition is not performed immediately after post-lift-off plasma cleaning.

Surface treatment and spin coating

- Surface treatment - acetone - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry
- Prebaking - 185°C - 5:00 min.
- Spin coating - PMMA A4 950 - 2000 rpm (target: 275 nm)
- Baking - 185°C - 5:00 min.

Lithography

- Electron beam exposure - 900 $\mu C/cm^2$
- Developing - MIBK:IPA 1:3 - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry

Window etch

- Post-baking - 120°C - 10:00 min.
- Etching - Transene D - 50°C - 3:30 min.
- Rinsing - H_2O - 15 s
- Rinsing - H_2O - 1:00 min.
- N_2 dry

Resist strip

- Cleaning - acetone - 50°C - 2:00 h
- Rinsing - isopropanol (IPA) - 5:00 min.
- N_2 dry
- UV ozone - 20:00 min.

(f) **Gate electrodes**[3]

Surface treatment and spin coating

- Surface treatment - acetone - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry
- Spin coating - CSAR 0.04 - 4000/2000 rpm (target: 90/130 nm) (see [4])
- Baking - 150°C - 3:00 min.

[3] This step is repeated for each gate layer.

[4] 4000 rpm is used for the screening and accumulation/plunger layers, while 2000 rpm is used for the barrier layer.

Lithography

- Electron beam exposure - 350 µC/cm^2 (see [5])
- Developing - pentyl acetate - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry
- UV ozone - 2:00 min.

Metalization

- Evaporation - titanium (Ti) - 3 nm - 0.5 Å/s
- Evaporation - palladium (Pd) - 17/37 nm - 2 Å/s (see [6])
- Lift-off - AR 600-71 - 40°C - 30:00 min. (ultrasound)
- Rinsing - isopropanol (IPA) - 5:00 min.
- N_2 dry
- UV ozone - 20:00 min.

Gate anneal

- UV ozone - 2:00 min. (see [7])
- Rapid thermal anneal - forming gas (5% H_2, 95% N_2) - 400°C - 15:00 min.

Gate isolation

- UV ozone - 2:00 min. (see [8])
- Atomic layer deposition - aluminum oxide (Al_2O_3) - 300°C - 7 nm (see [9])

(g) **Micromagnets**[10]

Surface treatment and spin coating

- Surface treatment - acetone - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry
- Spin coating - MMA(17.5)/MAA EL8 - 3000 rpm (target: 335 nm)
- Baking - 175°C - 10:00 min.
- Spin coating - CSAR 0.09 - 3000 rpm (target: 250 nm)
- Baking - 150°C - 3:00 min.

[5] The optimal dose depends on the pattern and can drift over time, so a dose test should be performed regularly to determine the optimal dose.
[6] For the first gate layer 17 nm of Pd is deposited, while 37 nm is used for all subsequent layers.
[7] UV ozone treatment is optional and only required if rapid thermal annealing is not performed immediately after post lift-off ozone treatment.
[8] UV ozone treatment is optional and only required if atomic layer deposition is not performed immediately after rapid thermal annealing.
[9] If micromagnets are deposited, the last ALD layer has a thickness of 20 nm.
[10] A sample only contains micromagnets or a stripline (not both), so only one of these two fabrication steps is performed on each sample.

Lithography

- Electron beam exposure - 300 µC/cm^2
- Developing - pentyl acetate - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- Developing - MIBK:IPA 1:3 - 2:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry

Metalization

- Evaporation - chromium (Cr) - 5 nm - 0.5 Å/s
- Evaporation - cobalt (Co) - 200 nm - 2 Å/s
- UV ozone - 20:00 min.
- Lift-off - acetone - 50°C - 1:00 h
- Lift-off - acetone - 50°C - 1:00 h (ultrasound)
- Lift-off - acetone - 50°C - 5:00 min.
- Rinsing - isopropanol (IPA) - 5:00 min.
- N_2 dry
- UV ozone - 20:00 min.

(h) **Stripline**[11]

Surface treatment and spin coating

- Surface treatment - acetone - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry
- Spin coating - CSAR 0.09 - 2000 rpm (target: 275 nm)
- Baking - 150°C - 3:00 min.

Lithography

- Electron beam exposure - 300 µC/cm^2
- Developing - pentyl acetate - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry
- UV ozone - 2:00 min.

Metalization

- Evaporation - aluminum (Al) - 100 nm - 2 Å/s
- Lift-off - AR 600-71 - 40°C - 1:00 h (ultrasound)
- Rinsing - isopropanol (IPA) - 5:00 min.
- N_2 dry
- UV ozone - 20:00 min.

[11] See footnote 10.

A

(i) **Contact etch**

Surface treatment and spin coating

- Surface treatment - acetone - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry
- Prebaking - 175°C - 5:00 min.
- Spin coating - PMMA A4 950 - 2000 rpm (target: 275 nm)
- Baking - 175°C - 5:00 min.

Lithography

- Electron beam exposure - 1200 µC/cm^2
- Developing - MIBK:IPA 1:3 - 1:00 min.
- Rinsing - isopropanol (IPA) - 1:00 min.
- N_2 dry

Etch

- Post-baking - 120°C - 10:00 min.
- Etching - Transene D - 50°C - 5:30 min.
- Rinsing - H_2O - 30 s
- Rinsing - H_2O - 1:00 min.

Resist strip

- Cleaning - acetone - 50°C - 2:00 h
- Rinsing - isopropanol (IPA) - 5:00 min.
- N_2 dry
- UV ozone - 20:00 min.

(j) **Dicing**[12]

Spin coating

- Spin coating - S1805 - 4000 rpm
- Baking - 110°C - 3:00 min.

Dicing

- ESD compliant tape (140 µm) - NBC blade - work thickness: 650 µm - 20,000 rpm

Resist strip

- Cleaning - acetone - 10:00 min.
- Rinsing - isopropanol (IPA) - 5:00 min.
- N_2 dry

(k) **End-of-line anneal**[13]

- Anneal - hydrogen (H_2) - 400°C - 45:00 min.

[12] Dicing and the end-of-line anneal can be interchanged.
[13] See footnote 12.

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List of Publications

10. *A Sparse Spin Qubit Array*
J. M. Boter, J. P. Dehollain, J. P. G. van Dijk, T. Hensgens, R. Versluis, J. S. Clarke, M. Veldhorst, F. Sebastiano, and L. M. K. Vandersypen, *in preparation.*

9. *A sparse spin qubit array with integrated control electronics*
J. M. Boter,* J. P. Dehollain,* J. P. G. van Dijk, T. Hensgens, R. Versluis, J. S. Clarke, M. Veldhorst, F. Sebastiano, and L. M. K. Vandersypen, *in print*, arXiv:1912.06461.

8. *Quantum Dot Arrays in Silicon and Germanium*
W. I. L. Lawrie, H. G. J. Eenink, N. W. Hendrickx, **J. M. Boter**, L. Petit, S. V. Amitonov, M. Lodari, B. Paquelet Wuetz, C. Volk, S. Phillips, G. Droulers, N. Kalhor, F. van Riggelen, D. Brousse, A. Sammak, L. M. K. Vandersypen, G. Scappucci, and M. Veldhorst, arXiv:1909.06575.

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