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Single-Shot Fabrication of Semiconducting–Superconducting Nanowire Devices

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Semiconducting–superconducting hybrids are vital components for
the realization of high-performance nanoscale devices. In particular,
semiconducting–superconducting nanowires attract widespread interest
owing to the possible presence of non-abelian Majorana zero modes, which
are quasiparticles that hold promise for topological quantum computing.
However, systematic search for Majoranas signatures is challenging because
it requires reproducible hybrid devices and reliable fabrication methods. This
work introduces a fabrication concept based on shadow walls that enables
the in situ, selective, and consecutive depositions of superconductors and
normal metals to form normal-superconducting junctions. Crucially, this
method allows to realize devices in a single shot, eliminating fabrication steps
after the synthesis of the fragile semiconductor/superconductor interface.
At the atomic level, all investigated devices reveal a sharp and defect-free
semiconducting–superconducting interface and, correspondingly, a hard
induced superconducting gap resilient up to 2 T is measured electrically.
While the cleanliness of the technique enables systematic studies of
topological superconductivity in nanowires, it also allows for the synthesis of
advanced nano-devices based on a wide range of material combinations and
geometries while maintaining an exceptionally high interface quality.

1. Introduction

Semiconductor–superconductor nanowires are prime candidates toward topological quantum computation based on the manipulation of Majorana zero modes.[1–5] However, to serve as basic units of complex qubit architectures,[6–9] hybrid nanowires require a homogeneous and pristine interface between the semi- and the superconductor. In state-of-the-art methods, a superconducting film is deposited in situ after the growth of the semiconductor nanowires,[10,11] which are then transferred onto insulating substrates for further fabrication. The superconductor is chemically etched away from certain sections of the wires to realize gate-tunable regions. This approach has a major drawback: the selectivity of the metal etching is often uncontrollable and results in damage to the semiconductor crystal, as well as in chemical contaminations.[12,13] An alternative method to obtain gate-tunable regions is the shadow evaporation of the superconductor. This can be obtained by engineering complex nanowire growth chips with trenches or horizontal bridges.[13–15] In this case, the nanowire growth needs to be accurately optimized, the variety of possible devices is minimal, and hybrid nanowires still need to be transferred onto a substrate and subsequently processed. Crucially, the semiconductor–superconductor interface is unstable and prone to degradation with time and temperature, a problem that is particularly severe for the case of InSb/Al where the degradation takes place even at room temperature.[16–20] The interface instability poses a limit to the development and systematic exploration of topological circuits.

Here, we establish a fabrication method based on our previously introduced shadow-wall lithography technique[21] that overcomes these problems and enables the synthesis of high-quality hybrid devices in a single shot. The complete elimination of processing after the formation of the delicate semiconductor–superconductor interface is the critical aspect of our approach. To achieve this, we employ chips with pre-patterned bonding pads, bottom gates and shadow walls, next to which we transfer the semiconducting nanowires. The shadow walls and their particular design facilitate the

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selective deposition of the superconductor as well as contact leads without breaking the vacuum, eliminating the need for extra lithography steps. We demonstrate the versatility of our approach by creating hybrid junctions, which are the primary devices utilized to verify the emergence of Majorana excitations. The high quality of the devices is probed by transmission electron microscopy and by quantum transport measurements. All the investigated devices reveal a sharp and defect-free semiconductor–superconductor interface and, consequently, a hard induced superconducting gap. Our technique is inherently versatile and can have vast applications, from sparking rapid exploration of different combinations of materials to enabling the fabrication of more complex devices.

2. Results and Discussion

2.1. Preparation of Single-Shot Nanowire Devices

Specifically, we exploit the properties of InSb nanowires and Al films, a combination of materials that is promising for the study of Majorana physics.[14,21,22] Nanowires are typically ≈10 μm long,[23] and the Al thin films can be grown homogeneously with thicknesses as low as 5 nm. The way the two materials are combined in situ is illustrated in **Figure 1**a. In brief, nanowires are transferred from the "growth" to the "device" substrate under an optical microscope. With accurate nanomanipulation, single nanowires (in red) are placed in the vicinity of dielectric shadow walls (in green) onto a gate oxide, which capacitively couples the wires to bottom gates (in yellow). Thanks to an atomic hydrogen cleaning step, the native oxide of the wires is removed without damaging the semiconductor crystal and introducing contaminations.[24,25] The superconductor is then deposited in situ via e-gun evaporation at a substrate temperature of ≈140 K.

Critically, the deposition is divided into two steps. First, we evaporate a thin Al layer at 50° with respect to the substrate (top panel of Figure 1b), and then a thick Al layer at 30° (bottom panel of Figure 1b). The two layers have a controlled thickness of 5–11 nm and 35–45 nm respectively (with ≈0.1 nm of accuracy). A longitudinal schematic cross-section of the device is illustrated in Figure 1c to emphasize that, due to the shallow angle of the second evaporation and the position of the middle wall, only the two source and drain nanowire sections (Figure 1a) are covered by the thick Al layer. This process enables the formation in a single shot of hybrid asymmetric Josephson junctions with Al leads of different thicknesses, and this controlled variation can be used as a knob to tune the superconducting properties of the junctions.[26] When a normal metal (e.g., Pt) is deposited in the second step onto the thin Al layer, the source and drain nanowire sections act as normal leads due to the inverse proximity effect forming a single-shot NS device (see Figure S1, Supporting Information).

Differently from ref. [21], the combination of such shadow-wall designs and double-angle deposition enables to engineer in situ multiple layer depositions providing a route to eliminate or minimize fabrication steps. In particular, our method
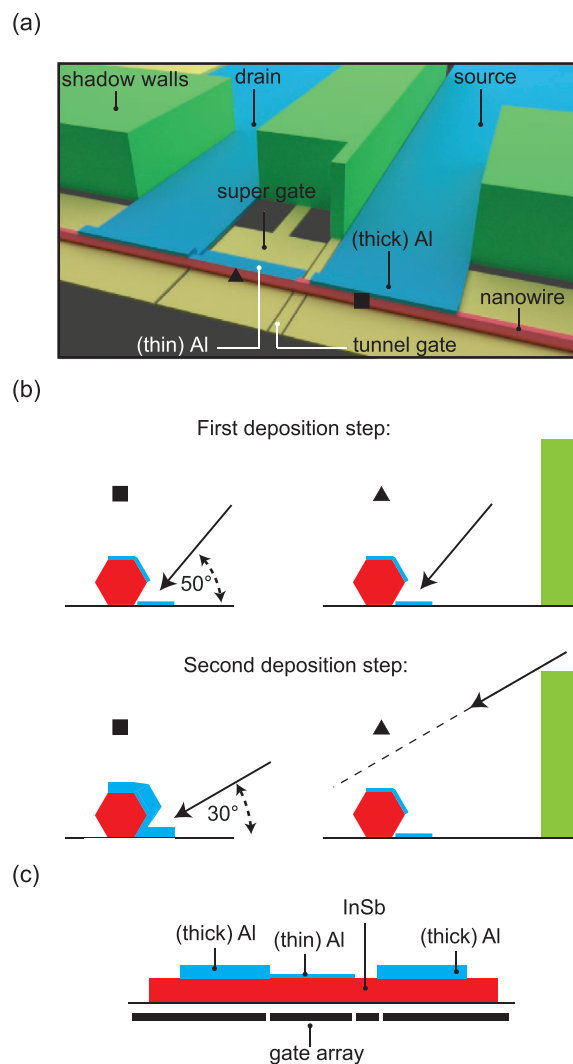
Figure 1. Fabrication of asymmetric Josephson junctions. a) An illustration of an asymmetric Josephson junction device: the nanowire (in red) is separated from the bottom gates (in yellow) by a dielectric layer and is adjacent to shadow walls (in green). The superconducting film (in blue) covers the wire selectively. The relevant gates are the "super gate" and the "tunnel gate" whose actions are discussed later. b) Cross-sections of the device taken at the two positions indicated by the square and triangle after the first (top panel) and the second evaporation step (bottom panel). c) Longitudinal cross-section of the hybrid nanowire after the two steps.

enables the direct formation of short tunneling junctions which are favorable to minimize the emergence of non-topological subgap states.[27] As a result, our chips can be mounted in a dilution refrigerator within a few hours after the evaporation, preventing the formation of chemical intermixing at the fragile InSb/Al interface. The total elimination of detrimental processes such as heating steps, metal etching, lithography and electron microscopy makes our flow advantageous with respect to other state-of-the-art methods, and similar principles have been applied successfully in the context of carbon nanotube devices.[28]

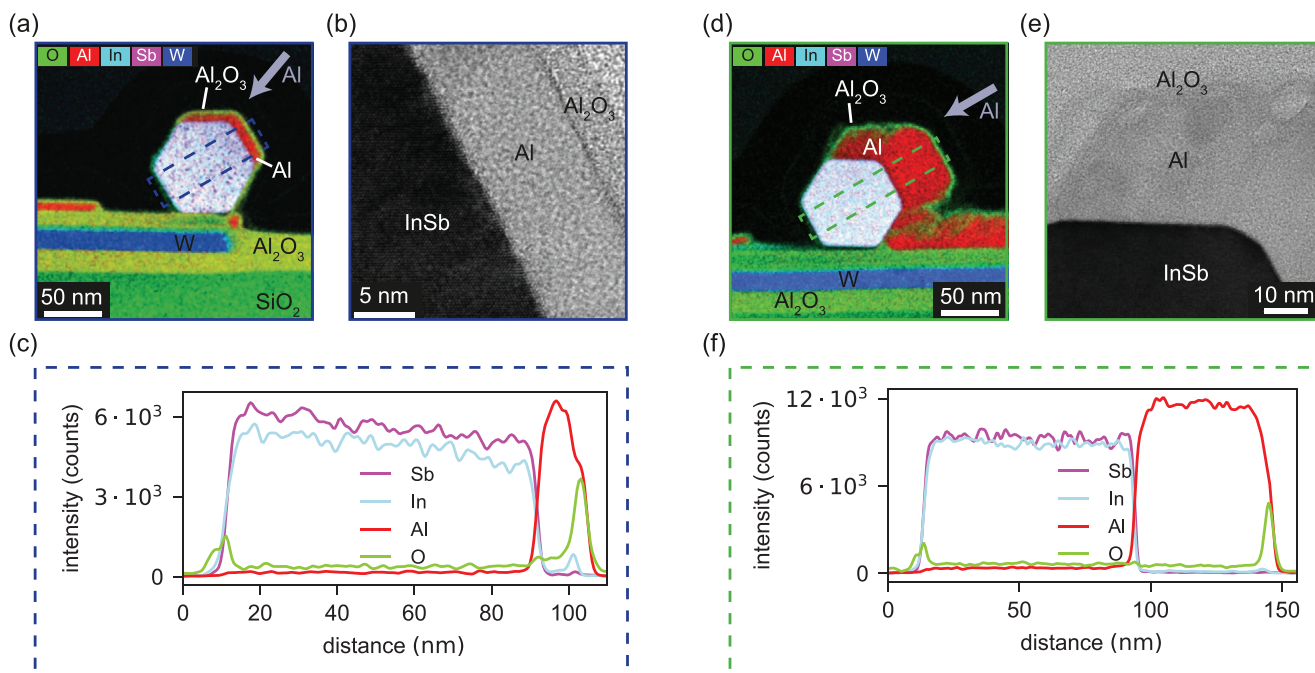**Figure 2.** Material analysis. a) Composite image of EDX elemental maps of the InSb nanowire covered with a thin layer of aluminum deposited at 50° (cf. grey arrow). b) Bright field (BF) STEM image of the InSb/Al interface. c) Elemental line scan extracted from (a) perpendicular to the top-side facet of the nanowire. d) Composite image of EDX elemental maps of the InSb nanowire covered with a thick layer of aluminum evaporated at 30° (cf. grey arrow). e) Annular dark-field (ADF) STEM image focusing on the aluminum layer on the top facet of the nanowire. f) Elemental line scan extracted from (d) perpendicular to the top-side facet of the nanowire.

2.2. Material Analysis

We evaluate the quality of the hybrid nanowires with transmission electron microscopy (TEM), and energy-dispersive X-ray analysis (EDX) performed on cross-sectional lamellas prepared via focused ion beam (FIB). The lamellas corresponding to **Figure 2**a,d have been taken from cross-sections of nanowires with thin and thick Al coverage, respectively. Figures 2b and e present typical bright-field scanning transmission electron microscopy images (BF STEM) of the thin- and thick-Al nanowire sections.

The EDX micrograph of Figure 2a shows that, with the first deposition, the Al coating forms a continuous polycrystalline layer on two of the wire facets and on the substrate with a thickness of 6.5 nm on the top and 8.5 nm on the top-side facet. There is no connection between the thin Al shell on the wire and the thin Al on the substrate. Similarly, Figure 2d illustrates that the thick-Al coverage is 26 and 49 nm depending on the facet. The wire exhibits three-facet coverage with a continuous metallic connection to the substrate, which allows for the creation of electrical contacts to the wire.

Importantly, the interface between Al and InSb is sharp and clean, demonstrating a good connection between the two materials and no damage from hydrogen cleaning on the semiconductor. The EDX elemental mapping manifests an oxygen peak at the InSb/Al interface that is much weaker compared to the native oxide on the surface of the nanowire visible in the EDX line scan, highlighting the successful hydrogen cleaning treatment (Figures 2c and f).

2.3. Multiple Andreev Reflections in Asymmetric Josephson Junctions

We validate our nanowire devices via low-temperature electrical transport. We consider first an asymmetric Josephson junction device (scanning electron micrograph in **Figure 3**a). A DC bias voltage with a small AC excitation, $V_{SD} + \delta V_{AC}$, is applied between source and drain, yielding a current $I + \delta I_{AC}$. Both the DC current and the differential conductance $G = \delta I_{AC}/\delta V_{AC}$ are measured. The gate voltage V_{TG} applied at the "tunnel gate" tunes the transmission of the junction, whereas the voltage V_{SG} at the "super gate" controls the chemical potential of the proximitized wire.

The conductance through the device displays prominent peaks due to multiple Andreev reflections and a zero-bias peak due to Josephson supercurrent (Figure 3b). Notably, these observations are found across all the measured devices, proving the strong and reproducible hybridization between the semi- and the superconductor (Figure S8, Supporting Information). The observation of different orders of multiple Andreev reflections demonstrates that transport is phase coherent across a length scale of multiple times the 100 nm-junction.

In widely studied symmetric junctions, multiple Andreev reflection peaks arise at subharmonic values of the superconducting gap.[29,30] In asymmetric junctions, transport mechanisms such as the ones presented in Figure 3c favor multiple Andreev processes at energies that relate to both gaps in a particular way. Odd orders manifest as conductance peaks at subharmonic values of the sum of the two gaps:[31,32]
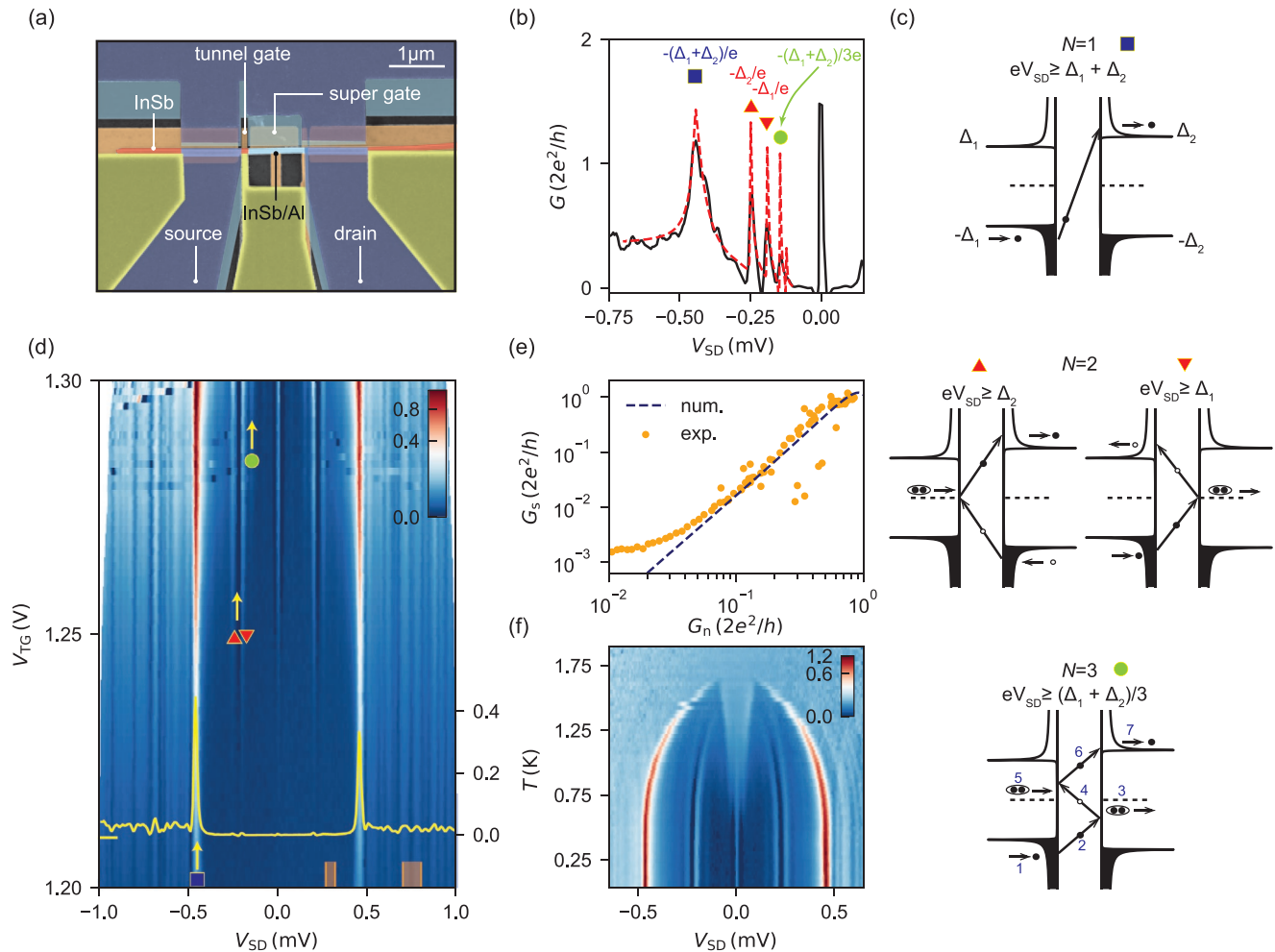
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Figure 3. Multiple Andreev reflections in asymmetric junctions. a) False-color scanning electron micrograph of the first device. b) G versus V_{SD} at $V_{TG} = 1.38\,V$ (black trace) and theoretical fit (dashed red trace). The blue square, red triangles and green circle indicate multiple Andreev reflection peaks of the first, second, and third order, respectively. c) Schematic of the multiple Andreev reflections processes. Top, middle and bottom panels describe first, second and third orders, respectively. Electrons (holes) are shown as black (white) circles, and pairs of two electrons identify Cooper pairs. d) Color map of G in units of $2e^2/h$ versus V_{TG} and V_{SD} displaying tunneling conductance peaks at constant bias voltages. The square, the triangles and the circle correlate these peaks to the processes depicted in (c). The yellow trace is a conductance line-cut at $V_{TG} = 1.21\,V$, as indicated by the yellow tick mark. Values on the right y-axis are in units of $2e^2/h$. e) In orange, G_s versus G_n (average conductances in the bias ranges indicated by the vertical tick marks in panel (d) of $[0.27, 0.32]\,mV$ and $[0.70, 0.80]\,mV$, respectively), and in dark blue, the result of the numerical calculations. In these measurements, the super-gate voltage has been set to the same value as the tunnel-gate voltage. f) Color map of G in units of $2e^2/h$ versus V_{SD} and temperature T of the second device. The measurement is taken in the tunneling regime with $V_{TG} = 1.145\,V$ and at a negative super-gate voltage of $V_{SG} = -1.75\,V$.

$$|V_{SD}| = \frac{\Delta_1 + \Delta_2}{Ne} \quad \text{with } N = 1, 3, 5, \ldots \quad (1)$$

where Δ_1 and Δ_2 are the small and the large gaps induced by the thick and the thin Al films, respectively, N is the order, and e is the electronic charge. Differently, even orders give rise to doublets of peaks at subharmonic energies of both gaps Δ_i with $i = 1, 2$:

$$|V_{SD}| = \frac{2\Delta_i}{Ne} \quad \text{with } N = 2, 4, 6, \ldots \quad (2)$$

While the positions of the peaks depend on the magnitude of the two induced gaps, their intensity is related to the number and the transmission of the confined nanowire modes. To

extract these parameters, we develop a theoretical model that accounts for different superconducting gaps in the two leads. A complete discussion of our model is presented in Section S3, Supporting Information. In Figure 3b we plot the result of the numerical calculation (red dashed trace) together with the experimental conductance (dark blue trace). Here, the junction is in the single-subband regime with transmission probability of 0.35 and the gap values are $\Delta_1 = 192\,\mu eV$, $\Delta_2 = 250\,\mu eV$. The peaks at $eV_{SD} = -(\Delta_1 + \Delta_2)$ (blue square), along with the doublet at $eV_{SD} = -\Delta_{1,2}$ (red triangles) and the one at $eV_{SD} = -(\Delta_1 + \Delta_2)/3$ (green circle), obey Equations (1) and (2) for $N = 1, 2, 3$ perfectly. Subharmonic structures where different gaps are involved were reported only in early investigations in planar Pb/InSb/Sn junctions.[31,32] In Figure 3d, we show the activation of these peaks upon varying V_{TG}. While orders above $N = 3$ are better resolved

at higher junction transparency (Figure S2, Supporting Information), the hard induced gap found in the tunneling regime (see yellow trace) corroborates the high quality of the InSb/Al interface presented above.

To demonstrate the hardness of the gap in hybrid devices, it is common to compare the subgap conductance of a normal-superconductor junction with what is predicted by the Beenakker formula that gives an analytical description of the Andreev processes.[14,21,33–35] Here, we provide an alternative approach for the case of Josephson junctions where there is no analytical description for the subgap conductance. Using Josephson junctions rather than normal-superconductor junctions to infer the hardness of the induced gap will be beneficial also for other hybrid nanostructures because it alleviates the need to fabricate a normal-metal contact.

In brief, we have calculated numerically the conductance of the system assuming hard gaps in both leads as a function of junction transmission probability (Section S3, Supporting Information). In Figure 3e, we illustrate the agreement between the simulation and the experimental data. Here, G_s is obtained by averaging theoretical and experimental conductance traces in the bias range [0.27, 0.32] mV. The theoretical normal-state conductance G_n equals to $T_p \cdot 2e^2/h$, with T_p the transmission probability, and the experimental one is the average in the bias window [0.70,0.80] mV. The experimental trace only deviates from the theoretical calculation for values of G_s approaching $\approx 10^{-3} \cdot 2e^2/h$, that is the noise floor of our electronics. The agreement between our experimental data and the numerical calculation further demonstrates the hardness of the induced gaps.

The difference in film thickness results also in two disparate superconducting critical temperatures: $T_{c1} \approx 1.66$ K and $T_{c2} \approx 1.76$ K (Section S7, Supporting Information), values that reflect the well-known enhancement in thin Al films with respect to the bulk value of 1.2 K.[26,36] We illustrate the difference of the two junction sides in Figure 3f with the conductance map versus bias voltage and temperature taken on a second asymmetric junction device. The sub-harmonic conductance peaks with $N = 2$, corresponding to $\pm\Delta_1$ and $\pm\Delta_2$, gradually shift to zero energy. The peak close to zero bias emerging at $T > 0.5$ K can be explained in term of thermally-activated quasiparticle current, which we discuss further in Section S7, Supporting Information.

We note that the second device is conceptually similar to the first one, and exhibits comparable induced superconducting properties ($\Delta_1 = 203 \mu eV$ and $\Delta_2 = 253 \mu eV$ at base temperature). However, in the second device, the nanowire section coupled to the thin Al film is longer than the first (1.5 μm versus 1.0 μm). We emphasize that the ability to tune this parameter with ease (i.e., by shadow-wall design) is an innovative result of our architecture, and it is relevant in topological circuits because it sets the maximum separation between emerging Majorana modes.

2.4. Tunneling Spectroscopy in Asymmetric Josephson Junctions

The well controllable thickness of each shell deposited in our method allows for the creation of devices that can be tuned to realize different superconducting or normal elements. In particular, we exploit the fact that, due to orbital effects, the critical parallel magnetic field of Al films increases upon reducing the film thickness.[26] We expect therefore that the gap induced by the thick Al film vanishes at a magnetic field significantly smaller than that of the thin Al side.

Such a transition is presented in **Figure 4**, where we display results obtained on the second device. Upon increasing the magnetic field along the wire ($B_{\parallel}$), the device transits from a Josephson junction (SS) into a normal-semiconductor–superconductor structure (NS), and eventually becomes a normal junction (NN) (Figure 4a). The first transition is accompanied by the coalescence of the $\pm(\Delta_1 + \Delta_2)/e$ peaks into the $\pm\Delta_2/e$ peaks at ≈ 0.40 T and by the suppression of the supercurrent peak, while the second occurs when Δ_2 vanishes at ≈ 2 T. These two field boundaries allow for tunneling-spectroscopy measurements in the NS configuration in a large magnetic field range relevant for topological superconductivity.[37] A similar result was demonstrated in planar junctions on 2D electron gases where the asymmetry of the critical fields was introduced by patterning one of the two leads much smaller than the superconducting coherence length.[38,39]

The versatility of our device preparation is also accompanied by the capability of tuning the device properties via the electric fields of the bottom gates. By varying the super-gate voltage, for instance, it is possible to both change the number of bands in the wire and shift the electron density close to or far from the Al interface, renormalizing properties such as the hardness of the induced gap, the effective g-factor and the spin-orbit coupling.[22,40,41] Although we did not observe an appreciable difference in the induced gap at zero magnetic field, we show that the magnetic field evolution of the gap is strongly affected by the voltage applied at the super gate.

At $V_{SG} = -1.75$ V, when the electron density is confined at the interface, bias spectroscopy reveals an Al-like hard-gap up to ≈ 1.8 T (Figure 4b). When increasing super-gate voltage to $V_{SG} = 0.2$ V, we observe the first state (with an effective g-factor of ≈ 5.5) coalescing with its own electron-hole symmetric partner in a zero-bias peak with conductance height of $\approx 2e^2/h$ (Figure 4c). Although a $2e^2/h$-high peak is a hallmark of a resonant Andreev reflection into a Majorana state, the energy and peak height are tunable by both the super and the tunnel gates (Figure S10, Supporting Information). This tunability suggests that this state might be a localized (i.e., non-topological) Andreev bound state located near the junction possibly originating from residual disorder in the semiconducting–superconducting device.[42–44]

At $V_{SG} = 0.5$ V and $V_{SG} = 0.7$ V, when the positive gate voltage allows the occupation of a greater number of nanowire bands, we observe that, upon increasing the magnetic field, a low-energy state oscillates around zero energy (Figure 4d,e). Additional subgap states shift down in energy (with an effective g-factor of $6 - 12$ in the first case, and 22 at maximum in the second) and are repelled via the spin-orbit interaction, which in finite-length systems can couple states with different orbitals and spins.[22,45] These states are tunable in energy by the super gate, but they are insensitive to variations in the tunnel gate (Figure S9, Supporting Information). While this robustness in barrier transparency has been used in the past to substantiate the presence of Majorana modes, we stress that the population of multiple nanowire subbands (see simulations in Figure S12, Supporting Information), together with orbital effects, result
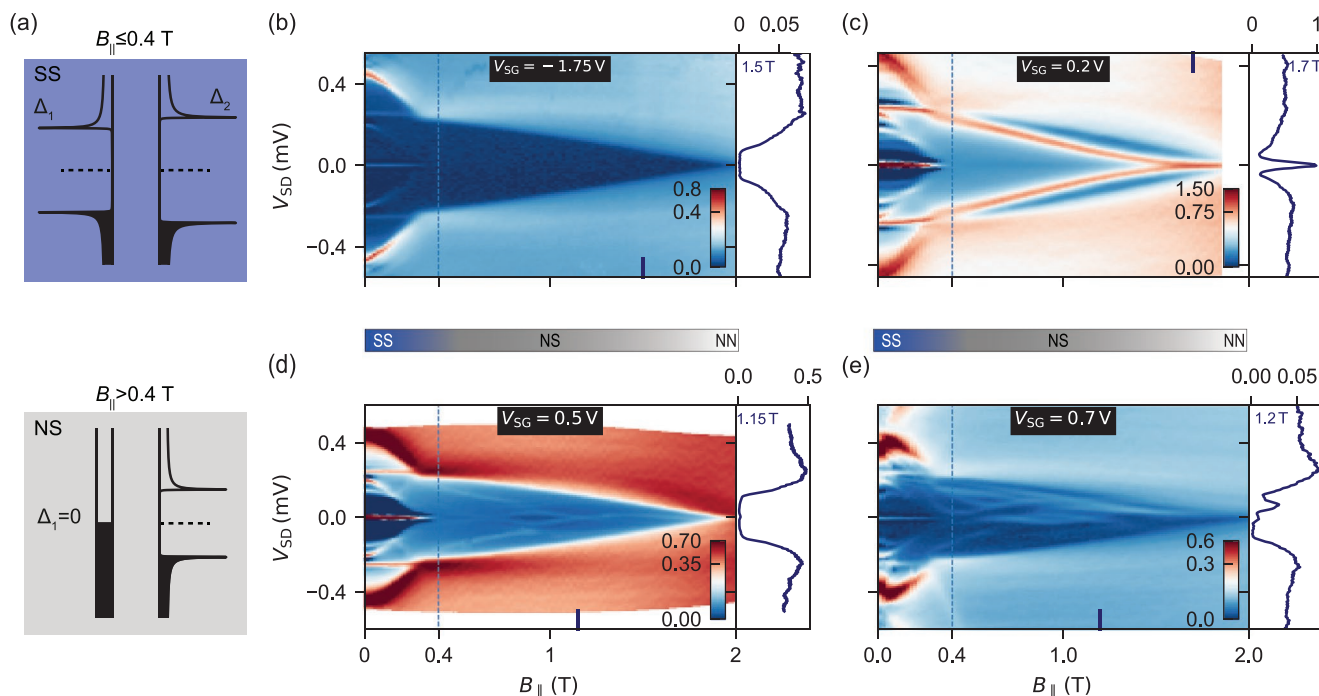
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Figure 4. Tunneling spectroscopy in asymmetric Josephson junctions. a) Top and bottom panels illustrate two schematics of the density of states at $B_\parallel \leqslant 0.4\,T$, and $B_\parallel > 0.4\,T$ in the asymmetric SS and NS junction regimes. The transition between the two regimes is marked with a vertical dashed line in the other panels. There, we display color maps of G in units of $2e^2/h$ versus V_{SD} and $B_\parallel$. b–e) The data sets differ in the value of V_{SG}, which increases from (b) to (e): in (b) V_{SG} equals $-1.75\,V$, in (c) $0.2\,V$, in (d) $0.5\,V$ and in (e) $0.7\,V$. Side panels show vertical line-cuts of the conductance in units of $2e^2/h$ at the positions indicated by the blue lines and labels. The two horizontal bars illustrate the junction regimes as a function of magnetic field.

in a complex topological phase diagram, making it arduous to assess the physical origin of the peaks in a normal-superconductor junction.[37,46]

Because of this difficulty and of the presence of Andreev states at normal-superconductor junctions,[47] future work will focus on three-terminal devices that enable probing both end-to-end subgap state correlations and, possibly, the presence of a topological gap.[48] It is noteworthy that the presented method will accelerate the progress in this direction by allowing an accurate design and realization of standardized Majorana devices.

3. Conclusions

One of the most significant challenges in the search for topological excitations in condensed matter is alleviating the complexity of the devices. This is a key aspect when it comes to reproducible measurements, high fabrication yield and eventually scalability. To this purpose, we introduce here an innovative technology to obtain hybrid nanowire junctions. By combining a double-angle evaporation with shadow walls, we demonstrate the possibility of completely eliminating the need for fabrication processing after the delicate semiconductor-superconductor interface is created. This method not only drastically reduces possible chemical contaminations and the deterioration of the interface but also results in reproducible and adjustable devices, with fast fabrication turnaround. Moreover, differently from previous shadowing methods without shadow walls,[14,15]

all the dimensions of the proximitized nanowire sections are accurately tunable.

While this study could not corroborate the presence of a topological state in hybrid nanowires, it lays the groundwork for future investigation of extremely long Majorana wires and the prompt fabrication of advanced devices such as hybrid two-path interferometers for the read-out of Majorana qubits.[49–51] Crucially, the versatility of the platform can stimulate rapid explorations of different material combinations toward a topological qubit without the need to develop material-dependent etching processes to define hybrid junctions. In addition, our method enables the fabrication of other quantum devices based on various kinds of nanostructures. For instance, the controlled and reproducible shadow evaporation of a superconductor onto a semiconductor can enable the direct synthesis of high-quality artificial Kitaev chains based on chains of hybrid quantum dots[52–54] and Cooper pair splitters in double nanowires,[55,56] which are becoming relevant devices for engineering parafermions in solid state systems.[57,58] Ultimately, we expect that our method will be beneficial for the advancement in the realization of Andreev qubits[59] and the engineering of quasiparticle traps in devices such as superconducting qubits and gatemons.[60–63]

4. Experimental Section

Substrates Fabrication: Bottom gates were fabricated by reactive-ion etching of a ≈17 nm thick W film with SF_6 gas, and were then covered by a ≈18 nm layer of Al_2O_3 deposited via atomic layer deposition. Shadow

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walls were created in the same top-down approach: a ≈700 nm thick layer of Si_xN_y deposited via plasma-enhanced chemical vapor deposition (PECVD) was reactive-ion etched by CHF_3. Shadow walls of the device presented in Figure S1, Supporting Information were made by patterning and developing a ≈1 µm-thick layer of HSQ that was subsequently baked at 300 °C. The substrates were then cleaned thoroughly for 1 h with oxygen plasma to remove resist residues.

Nanowire Growth and Transfer: Stemless InSb nanowires were grown with the method described in ref. [23]. They were then deterministically transferred from the growth substrate to the device substrate and pushed in the vicinity of shadow walls using an optical microscope and a micro-manipulator.

Semiconductor Surface Treatment and Metal Deposition: After the nanowire transfer, the chip was loaded into the load-lock of the metal evaporator. Here, the semiconductor oxide was gently removed with an atomic hydrogen cleaning treatment similar to ref. [21]. A tungsten filament at ≈1700 °C dissociates H_2 molecules into H* radicals which reacted with the oxygen at the nanowire surface and removed it. Typical parameters for this process were: a hydrogen flow of 2.2 mL min^{-1}, a process pressure of 6.3×10^{-5} mbar, and a process time of ≈1 h. The holder onto which the chip is clamped was kept at 277 °C for ≈3 h to ensure thermalization, and hydrogen cleaning is performed at this temperature.

The chip was then loaded from the load-lock into the main chamber of the evaporator. Here, it was cooled down and thermalized for an hour at ≈140 K. Thin Al was evaporated first at 50° with respect to the substrate plane (5–11 nm, measured by the evaporator crystal). Subsequently, Al (or Pt, depending on the device type) was deposited at 30° (35–45 nm, measured by the evaporator crystal). The deposition rate was maintained at ≈0.2 nm min^{-1}. The chip was brought back into the load-lock, where it was oxidized for 5 min in an oxygen pressure of 200 mTorr while still actively cooling the chip holder to maintain a temperature of ≈140 K. The load-lock was vented only when the chip had reached room temperature.

Transport Measurements: Electrical transport measurements were carried out with the samples in dilution refrigerators at a base temperature of approximately 15–20 mK and an electron temperature of ≈35 mK. Lock-in conductance measurements were conducted at low frequencies of 12–15 Hz, and the lock-in data was calibrated according to the measured DC conductance as demonstrated in ref. [21]. The data presented in the main text was taken from two representative devices. Additional data of these two devices is shown in Figures S2–S7, S9, and S10, Supporting Information. In total, three chips were fabricated and cooled down with respectively 3, 4, and 6 nanowire devices that all manifested similar induced superconducting properties. Exemplary transport characteristics of additional asymmetric junction devices are shown in Figure S8, Supporting Information, while data from a normal–superconducting junction are displayed in Figure S1, Supporting Information.

Determination of the Effective g-Factor: The effective g-factor of the subgap states are estimated in Figure 4 by considering their average slope versus the magnetic field as:

$$g = \frac{2\Delta E}{\mu_B \Delta B_\parallel} \tag{3}$$

where ΔE is the variation in energy in the magnetic field range ΔB, and μ_B is the Bohr magneton.

TEM Analysis: TEM investigation was carried out at 200 keV with a Thermo Fisher Talos transmission electron microscope equipped with a Super-X EDX detector. TEM samples were prepared via the focused-ion beam technique making use of a Thermo Fisher Helios dual beam scanning electron microscope. Additional TEM analysis is shown in Figure S8, Supporting Information.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Conflict of Interest

The authors declare no conflict of interest.

Data and Materials Availability

The data that support the findings of this study are openly available in 4TU.ResearchData TUD at https://data.4tu.nl/articles/dataset/Data_underlying_the_manuscript_Single-shot_synthesis_of_semiconducting-superconducting_nanowires/12764870, https://doi.org/10.4121/12764870.v3.

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