AN AMPLITUDE-TUNABLE BIPOLAR HIGH-VOLTAGE PULSER USING A UNIPOLAR SUPPLY FOR ULTRASOUND APPLICATIONS

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by

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ABSTRACT

This thesis discusses the architecture, circuit implementation and the simulation results of an amplitude-tunable bipolar high voltage (HV) pulser for ultrasound imaging. This design is capable of providing a relatively high-resolution amplitude modulation and allows bipolar pulsing under a unipolar supply with a small die size.

The pulser design starts from the driving circuit of the HV output stage. A driving circuit based on a current mirror structure is implemented to drive the ultrasound transducer element with different slewing currents. These currents levels are generated by 6-bit current DACs controlled by a calibration loop. This calibration loop senses the pulser output voltage through a capacitive divider. The resulting attenuated voltage is compared with a reference voltage by a low-voltage (LV) dynamic comparator. Based on the comparison result, the input code of the current DACs are adjusted by a successive approximation register (SAR).

Several techniques are proposed to flexibly change the pulse amplitude and reduce the die size. First, the pulser is driven in a current mode which allows the transistors at the output stage to operate in the saturation region, so that the currents through the transducer elements always follow the input codes. Second, a separate calibration phase is applied at the beginning of the transmitting and receiving cycles, which will generate flexible and accurate input currents for the corresponding transmission phase.

The pulser has been implemented in TSMC 180 nm HV BCD technology. The simulation results show that the prototype is able to transmit HV pulses with a 4-bit amplitude modulation with 0.5 V inaccuracy. The transmission power consumes less than 0.2 mW per channel when driving a transducer with a capacitance of 18.29 pF at a pulse repetition frequency (PRF) of 4 kHz. The estimated die size of the pulser is around 0.04 mm^2.

Keywords: ultrasound imaging, high-voltage pulser, current-mode driving, digital calibration

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Jianing Xing
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ACRONYMS

SAR successive approximation register

PRF Pulse repetition frequency

LV Low voltage

DAC Digital-to-Analog Converter

ADC Analog-to-Digital Converter

HV High Voltage

SNR Signal-to-noise ratio

TX Transmit Circuitry

RX Receive Circuitry

LNA Low noise amplifier

TGC Time gain control

T/R Transmit/Receive

CMUT Capacitive micro-machined ultrasonic transducers

3D Three-Dimensional

2D Two-Dimensional

RZ Return to zero

rms Root mean square

OTA Operational trans-conductance amplifier

MSB Most significant bit

LSB Least significant bit

INL Integral non-linearity

DNL Differential non-linearity

FMOM Finger metal oxide metal capacitor

ASICs Application-specific integrated circuits

IVUS Intravascular ultrasound

1 INTRODUCTION

With improvement of economy and advancement technology, physicians and patients increasingly need sophisticated medical imaging devices for diagnosis, treatment, and long-term health care [1].

Biomedical ultrasound imaging, which has been widely used since the early 19th century, provides a relatively fast, safe, power-efficient and radiation-free way to obtain medical images, in medical applications such as clinical diagnosis and image-guided interventions in heart and vascular diseases, prostate cancer, breast cancer, and obstetrics and gynecology diagnosis [2, 3, 4, 5].

At the beginning of the introductory chapter, the principle and application of ultrasound imaging will be introduced. Then, the challenges from pulse transmission will be discussed. In the next subsection, a review of the prior art is shown. Finally, the objectives of the thesis will be listed in the form of a set of design targets.

1.1 BACKGROUND

Three-Dimensional (3D) ultrasound imaging provides significant clinical benefits compared with those of traditional two-dimensional (2D) imaging. The imaging quality and utility of analyzing images increase as an expense of increasing size and design complexity. Large 2D transducer arrays are required for better signal-to-noise ratio (SNR) and improved image resolution [6, 7].

Pulse-echo measurement is an important method in each single array element of the ultrasound probe. During the pulse-echo measurement, the transducers in the array are operated in two different time phase. Its time diagram is shown in Figure 1.1.

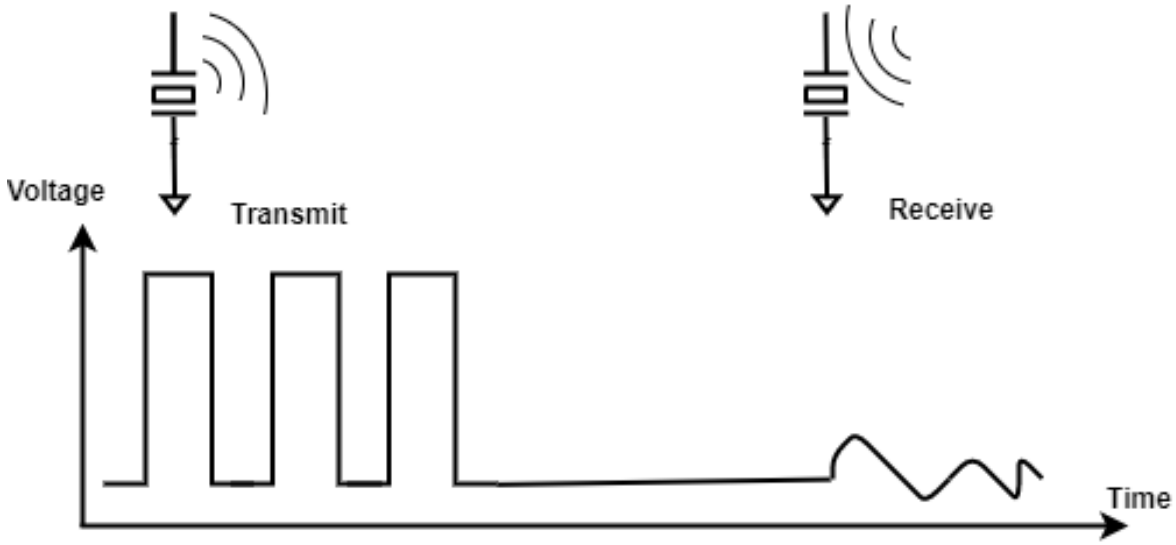


Figure 1.1: Voltage at the transducer during one transmit and receive cycle

Firstly, the transducer elements are excited by an electrical control signal, which they convert into acoustic pulses. These pulses are propagate to the targeting tissues, and then get reflected back to the transducer as echoes with different delay time and energy. The receive phase starts from the completion of the last pulse transmission and ends when all the echoes have been received. During the receive phase, the echoes are converted back to an electrical signal by the transducer elements and then amplified, digitized, and processed to render an image.

A block diagram of a typical ultrasound system is shown in Figure 1.2. A Digital-to-Analog Converter (DAC) converts digital control signals from a transmit beamformer into analog signals. These low voltage (LV) signals are converted into high voltage (HV) signals to drive the transducer elements by a (HV) driver (typically a pulser). Here, high voltage at the transducer is required to acquire sufficient signal-to-noise ratio (SNR) because of the attenuation during propagation of the acoustic

signal [8]. Generally speaking, the Transmit Circuitry (TX) works in the HV domain, while the Receive Circuitry (RX) including a low noise amplifier (LNA), time gain compensation (TGC) and following Analog-to-Digital Converter (ADC) works under low voltage. Therefore, a Transmit/Receive (T/R) switch is applied for the isolation. It connects TX to apply high voltage to the transducer during the transmit phase and connects RX to receive the relatively small electrical signals caused by echoes.

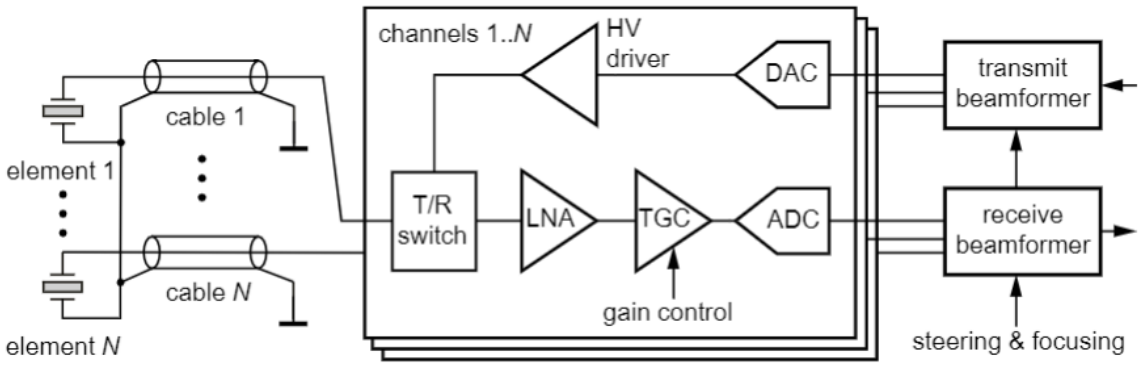


Figure 1.2: Block diagram of a typical ultrasound imaging system

In conventional ultrasound systems, the transducer array is connected to electronics of the imaging system by the cables. Commonly, these transducers are bulk piezo-electric transducers. Such transducers are based on the piezo-electric effect. In transmit mode, it converts electric signals to mechanical vibrations, which can be reflected as the variation of the axial depth of the crystal lattice of the piezoelectric materials. An alternative type of transducer that is becoming increasingly popular are capacitive micro-machined ultrasound transducers (CMUT). The working principle of a CMUT device is the deformation of an electrostatically actuated membrane. CMUT devices are fabricated using surface or bulk micro-machining techniques, and consequently have better integration than the piezo-electric transducers.

In Figure 1.2, lots of cables are used to connect each transducer to the imaging system, especially for 3-D imaging which requires thousands of transducer usage. These problems will be discussed in detail in the next subsection.

1.2 MAIN PROBLEMS

Even though commercially available HV pulsers have been applied to medical imaging systems, some requirements still cannot be fulfilled.

1.2.1 Requirement for local processing for cable count reduction

In conventional probe design, the elements are individually wired to an imaging system, which means many cables are required for the connection between probe and system. Especially in 3-D imaging, for which typically a 2D transducer array with thousands of elements is needed, the cable connections are too bulky and expensive [9, 10]. In this approach, electronic scanning is proposed instead of the physical movement of the transducer by the 2-D array to achieve the third dimension of the image, which brings out a significant number of elements used. As a result, in-probe application-specific integrated circuits (ASICs) are required to reduce the cable count, which will also contribute to higher image quality and initiate more applications [11]. And this also brings new challenges because of the limited chip area.

1.2.2 Requirement for reducing pulser die size

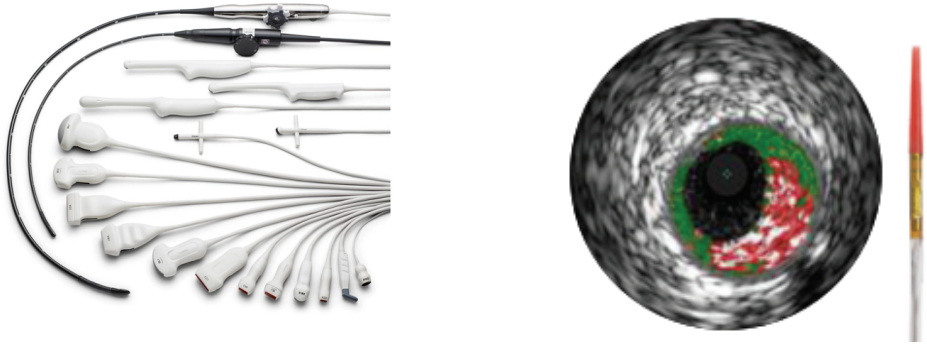
Sizing is an essential part of ultrasound probe design. Especially in the design of ASICs for 3D probes, pulser circuits are needed that can be integrated in a pitch-matched fashion directly underneath the transducer elements, which have dimensions in the order of only 100s of µm [12]. Because of the limited die size available for pulsers in ASICs for 3D imaging, simple unipolar designs have been adopted [13]. Compared to the (much larger) pulsers used in imaging systems, these unipolar pulsers have disadvantages of more out-of-band amplitude and higher power consumption. Also, the apodization technique could not be appropriately applied, since the structure of these simple pulsers limits the controllability of the pulses. However, realizing features like bipolar pulsing and apodization tend to require more high-voltage transistors, which are large and thus lead to a die size that exceeds what is available in 3D probes.

1.2.3 Requirement for apodization to decrease sidelobes

Typical integrated pulser implementations do not allow for amplitude control, while this is generally desirable to be able to control the beam shape by means of apodization. Apodization is a method to decrease the sidelobes on either side of the main beam. In transducer arrays, apodization can be achieved by exciting each elements in the array with different voltage amplitudes [14]. With the first requirement to be considered, an on-chip amplitude modulation is necessary f or each elements in the array.

1.3 STATE-OF-THE-ART

Some mature technology in ultrasound imaging has been commercialized, such as the imaging probes produced by Philips as shown in Figure 1.3. In some of these products, 3D-imaging has been achieved. However, these probes still suffer from sizing problems. For example for intravascular ultrasound (IVUS) application which is shown in the right, mostly 64 transducer elements can be integrated in one commercial prob, which means that they are still low in integration for ASIC size or cable counts reasons.



(a) (b)

Figure 1.3: Ultrasound imaging probes by *Philips*.

In [15] and [16], small and integrated three-level pulsers are proposed in ultrasound ASIC for higher imaging quality and power efficiency. However, there are still additional high-voltage switches used to tune the pulse in each channel, which occupy extra die size. Also, these design are not capable of apodization.

In the effort to achieve apodization, an amplitude-tunable pulser is proposed in [9]. In this design, both amplitude control and slew rate control are implemented. To limit the output swing, additional HV transistors are used in order to tune power supply as shown in Figure 1.4. Recently, in [17], a 7-level pulser is built instead of changing HV supplies based on the feedback loop, which the on-time of the pulser transistors is controlled as a response of the output amplitude.

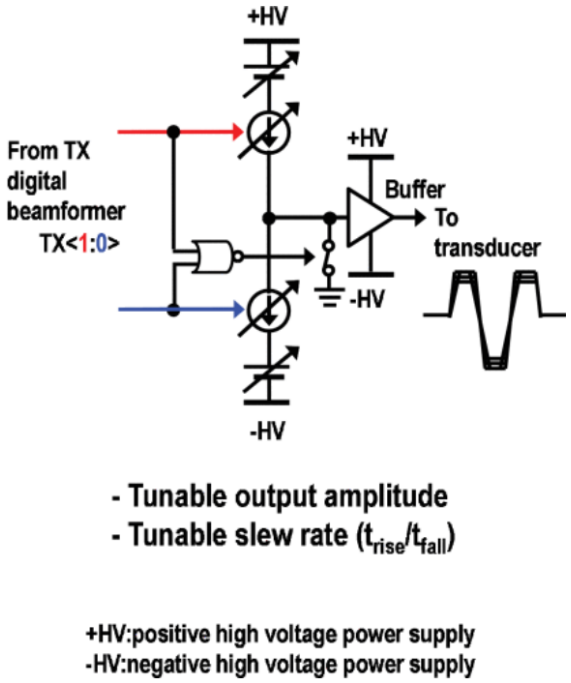


Figure 1.4: HV transistors implemented for supply tuning [9]

1.4 OBJECTIVES

To solve the problems mentioned above, a bipolar pulser with on-chip voltage amplitude modulation should be realized. In this pulser, high voltage transistors occupy most of the die area of the pulser, because the isolation region of HV transistors should be designed extremely large to avoid leakage current between adjacent devices in the fabrication process. As a result,the number of HV devices should minimized to minimize the die size. Compared with [9], instead of adding extra HV devices, the solution can be a simplified pulser driven by a current-mode driver with a calibration loop to generate controllable pulsing signals. Compared with previous multi-level pulsing and amplitude tuning works, this design aims to have more flexibility in targeted value of pulse amplitude.

In this work, a bipolar amplitude-tunable HV pulser is designed in TSMC 0.18 µm HV BCD technology and the pulser design is targeted at and simulated with a CMUT model with 18.29 pF//4 kΩ impedance.

Table 1.1 lists the target specification of the pulser.

Table 1.1: Design Target of the Pulser

	This work	[9]	[16]	[15]
Process	TSMC 180nm HV BCD	XFAB 180nm HV SOI	TSMC 180nm HV BCD	TSMC 180nm HV CMOS
Supply voltage	30 V	70 V	30 V	30 V
Amplitude modulation range	29 V	138 V	Not applicable	Not applicable
Bipolar pulse	Yes	Yes	Yes	No
Pulse frequency	7.89 MHz @ 18 pF	2 MHz	9 MHz @ 18 pF	2 MHz @ 40 pF
Power consumption per channel	<1 mW	0.74 mW	1 mW	66.7 mW
High voltage devices	Minimum	16	12	12
Estimated die size	$< 0.04\,mm^2$	$0.167\,mm^2$	$0.09\,mm^2$	$0.33\,mm^2$

1.5 OUTLINE

This thesis presents an integrated bipolar HV pulser with flexibly tunable output amplitude and extra small die size for ultrasound probes. The thesis is divided into five chapters besides this introductory chapter.

Chapter 2 introduces the basic architecture of the pulser design, including pulser type, driving mode, receive chain and the functionality of a calibration loop and the associated logic.

Chapter 3 discusses the circuit implementation in detail to realize the pulser. The driver of the pulser including current DAC and level shifter will be introduced first. Then, the choice of attenuator, dynamic comparator, and tunable reference will be discussed.

Chapter 4 presents simulation results of the entire design.

Finally, Chapter 5 summarizes the contributions of the thesis and highlights potential future directions.

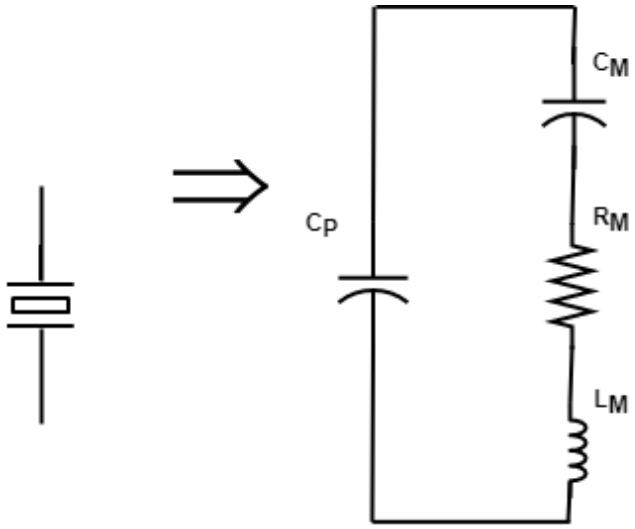
2 SYSTEM ARCHITECTURE

In this chapter, the architecture of the pulser design will be introduced from basic concepts to more complex. It will be discussed in five parts.

In the first part, basic HV pulsers for ultrasound applications will be presented, which are generally based on voltage-mode driving. Subsequently, in the second part, we will discuss current-mode driving, which is an alternative driving scheme that can potentially lead to more compact pulser implementations. The third part illustrates how the output pulse is sensed and controlled, including a calibration loop for the amplitude control and the operation of its different blocks. Next, the capability for RX mode in this system will be discussed. Finally, the overall structure and its timing diagram are shown.

2.1 BASIC HV PULSER

CMUT and PZT transducers can be described by the same RLC model with different parameters [18, 19], as shown in Figure 2.1. In this work, the impedance of the transducer is modeled as 18.29 pF//4 kΩ, similar to the impedance of the CMUT transducer used in [16].



Model Parameter	Value
C_P	18.29pF
C_M	9.24pF
R_M	4kΩ
L_M	44u

Figure 2.1: Butterworth-Van Dyke model for ultrasound transducers, and values of the model parameters used in this work

A typical pulser has a push-pull output structure to drive these transducers [7, 6], generating HV pulses from control signals, which can be simplified as shown in Figure 2.2. Compared with resistive pull-up structure [20], pulsers based on a push-pull topology are more complex but power-efficient.

There are at least two transistors needed in a push-pull structure, working as switches. These transistors should be HV transistors because they should be able to survive tens of volts at their drain. Consequently, a relatively high voltage signal (Around 5V) is needed to drive the gate of these HV MOSFETs. In a unipolar pulser, the HV transistors are controlled to switch from a positive HV supply to ground. In a bipolar pulser, the source of the NMOS transistor is connected to a negative HV supply instead of ground. Also, with a return-to-zero (RZ) switch, this kind of structure can achieve 3-level pulsing [16].

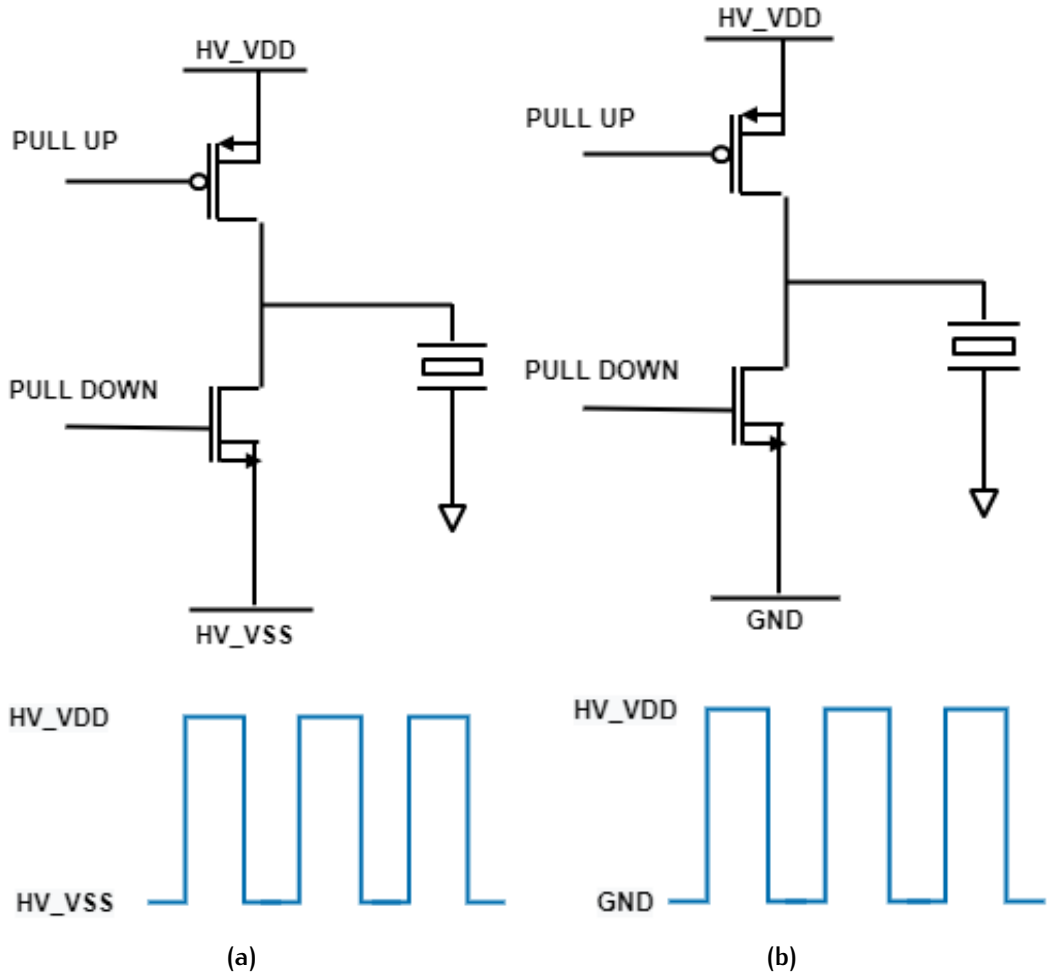


Figure 2.2: Simplified circuit diagram of traditional voltage-mode (a) unipolar and (b) bipolar pulser and their output signals

In [15], a mid-voltage is added in between to achieve 3-level pulsing under a unipolar supply. While this improves power efficiency, the additional HV devices needed to switch the transducer to this mid-voltage consume much more die size as an exchange.

2.2 CURRENT-MODE DRIVING

In this thesis, a mid-voltage is added as a 'natural state' of the transducer. The transducer is charged to the mid-voltage initially, and then it can be both charged to the high-voltage supply or discharged to the ground. This allows for bipolar pulsing using only a unipolar supply. Moreover, pulse inversion (**PI!**) for imaging enhancement [21] can be realized.

In order to realize amplitude modulation for apodization without increasing the required number of high voltage devices, a variable voltage will be applied at the gate of the high voltage transistors, operating them as tunable current sources rather than switches. In this way, the 'PULL UP' and' PULL DOWN' signals are no longer only control signals but also work as parameters to control the pulsing amplitude, as will be discussed in more detail below.

For the implementation of the pulser, a current-mode driving is applied for better control of ultrasound pulse to achieve bipolar pulser and amplitude modulation.

2.2.1 Pulse shape Analysis

In Figure 2.2, the pulse is described as a square wave with infinitely short rising and falling edges. In reality, the time needed for charging and discharging of the transducer cannot be neglected. With assumption that the transducer can be simplified as a capacitor, and the pulser transistors are in saturation during the rising and falling edges and provide a constant current to the transducer. The output pulse driven by the control signal can be seen as in Figure 2.3. The determined parameters of the shape of the pulse are also shown in the figure.

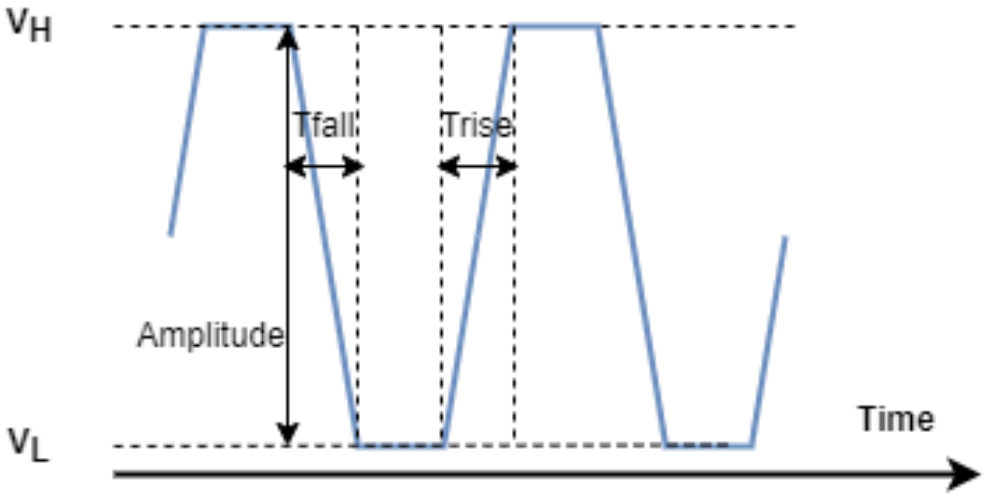


Figure 2.3: Pulses by a HV pulser with a capacitive load

There are several parameters to play with to achieve amplitude control of the pulse:

- **Limit V_H and V_L.** V_H and V_L can be seen as the voltage level at which the pulser output saturates when the transducer is fully charged or discharged. In the pulsers shown in Fig. 2.2, these voltage levels are set by the supply voltages. In [9], they are made programmable, using two HV transistors controlled by a variable current source out of the element area, to realize amplitude control.

- **Change Rise/Fall time.** Rise/Fall time is the time period in which the transducer is charged or discharged from one level to the other. In the traditional driving mode, when the on-time of the HV transistors is sufficient, it mainly depends on the slew rate and the supply voltage. On the other hand, when the on-time of the transistors is not sufficient to fully charge and discharge the output, adjusting the rise and fall time can be used to control the amplitude.

- **Change Slew Rate.** The slew rate can be seen as the charging speed of the transducer. It is determined by the charging current of the capacitor C_P as shown in Equation 2.1, and the current here is also the current through the HV transistors. When the on-time of the transistors is fixed, tuning the slew rate of the signal can efficiently adjust the pulsing amplitude, which means that the amplitude can be easily changed by adjusting the drain current of the HV transistors. In this way, we take current-mode driving into consideration.

$$I = \frac{dQ}{dt} = C\frac{dV}{dt} \propto SlewRate \tag{2.1}$$

2.2.2 Principle of Current-mode driving

In traditional pulsing method, the pulser gives a rail to rail output signal. Take unipolar pulsing as an example, the transducer is charging from ground to the supply voltage . The drain voltage of the HV transistors increases, which causes these transistors to work in the saturation region during slewing and in the triode region when the output voltage approaches the supply.

To realize amplitude control without extra HV transistors, we decide to use the current-mode driving. In pure current-mode driving, the voltage across the transducer is not charged to the supply voltage or ground. Instead, both the pull-up and the pull-down transistor are turned off before the output voltage reaches the supply, preventing the transistor from going into the triode region and letting the transducer float. In this way, the transistors are always in saturation, which can be seen as a current source with high resistance, effective driving the transducer as a current source.

In this driving mode, the gate-source voltage of the HV transistors is the dominant factor that determines the current through the transducer, as shown in Equation 2.2, which means that the amplitude of the pulse can be tuned by changing the gate-source voltage of the HV transistors.

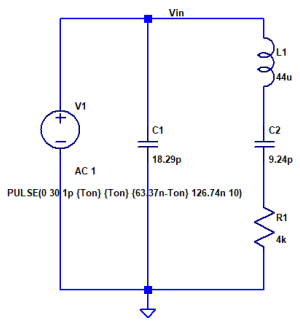
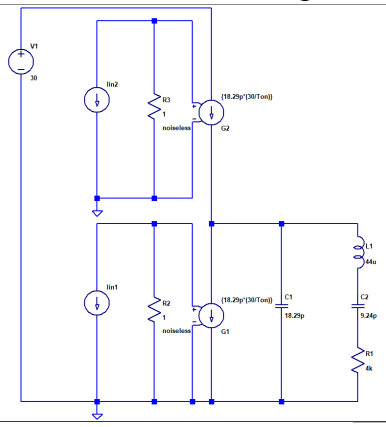
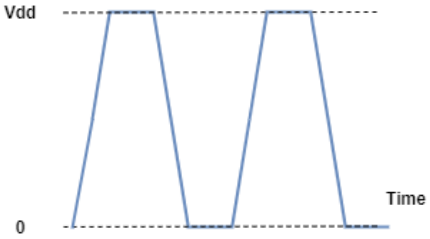
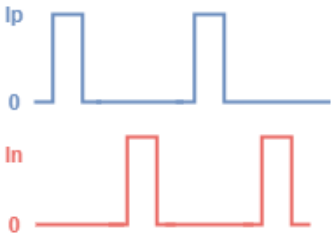
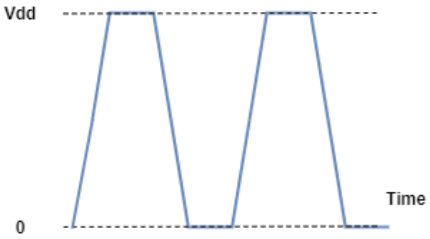
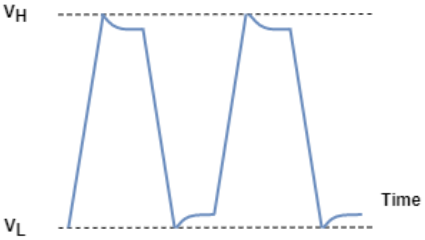
$$I_{d,sat} = \mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{2.2}$$

2.2.3 Current Mode VS Voltage Mode

The characteristics of the two driving modes with an input signal at the transducer's center frequency (7.89 MHz in our case) are listed in Table 2.1 below. The power efficiency is simulated with ideal components in two following ways:

- **Traditional voltage mode driving.** Transducer is driven by a ideal voltage source giving a trapezoidal wave.
- **Current mode driving.** Transducer is driven by two ideal current sources. These current source give square waves before hitting the settled peak value and making the transducer float.

Table 2.1: Differences in simulation results between two driving modes at 7.89 MHz

	Voltage-mode driving	Current-mode driving
Simulation circuit		
Input signals		
Output pulse*		
Power dissipation	169.55 m W	129.88 m W
Acoustic power	44.47 m W	37.07 m W
Power efficiency	26.23%	28.54%

To simulate the ideal current-mode behavior of the pulser, the saturated MOS transistors in the pulser are presented by two voltage-controlled current sources. And

the 30 V DC source is added as a presence of the supply voltage. The input currents are symbolically converted to voltage, then drive the transducer. To make the simulation result reasonable, V_H and V_H are set to over threshold voltage Vth and smaller than $V_{dd} - V_{th}$ to confirm the transistors are in the saturation region.

The values in the table are tested by *LTSPICE* under 7.89 MHz and $T_r/T_p = 25.348n/126.74n = 20\%$, in which T_r presents the rising time of the pulsing signal and charging time of the transducer and T_p is the time period of one duty cycle during transition time. With different frequencies and on-time, they have other power dissipation maps. When increasing the charging time, the power efficiency will be decreased. Still, similar efficiency is shown in both voltage-mode driving and current-mode driving.

The total power dissipation is generated from current delivered by the supply voltage by:

$$P_{tot} = \frac{1}{T_P} \int UIdt \tag{2.3}$$

And the acoustic power is simulated from the power dissipated in resistor R_M on the mechanical branch in Figure 2.1. It can be calculated as:

$$P_{acs} = \frac{1}{T_P} \int I_M^2 R_M dt \tag{2.4}$$

The main difference between the total power dissipation and the acoustic power comes from switching losses, i.e. the power consumed by the circuit during the process of charging and discharging the load capacitance at the output node. The driving loss can be calculated as:

$$P_{switch} = E/T_p = Q * V * f_p \tag{2.5}$$

Since $Q = CV$, in this design, the load capacitance is mainly the capacitance C_P in electrical branch:

$$P_{switch} = C_P * V_{dd}^2 * f_p \tag{2.6}$$

In this thesis, a 30 V voltage supply is applied to the pulser and the pulsing frequency is 7.89 MHz pulses. The switching loss is roughly 129.88 m W, which corresponds closely to the total loss.

In conclusion, with considering of the power dissipation under same supply voltage, the current-mode pulser provides less acoustic output compared with that in voltage-mode, since some peak-to-peak voltage swing is sacrificed to maintain

the pulser transistors saturated. This reduction is still acceptable in view of the advantages offered by current-mode driving. And the power efficiency won't be decreased a lot because there is no intrinsic power dissipation difference in two driving modes but a scaled-down in the voltage swing.

2.3 CALIBRATION LOOP

In the previous section, a current-mode method has been proposed to be able to control of the pulse amplitude. However, the pulsing current is hard to define because of non-ideal parameters in a realistic environment. In order to avoid problems such as the non-linearity from channel-length modulation and device mismatches , a closed-loop design is a better solution for amplitude modulation.

A most simplified feedback system for the pulser design is shown in Figure 2.4. There are three main parts to be determined for building this loop. The first is which kind of the input signal should be controlled. The second is which parameter of the output signal should be detected. And the last and the most crucial part is how to design an effective feedback path to close the loop.

In this section, different ways for closed-loop control will be discussed and analyzed in detail. The method for achieving amplitude control will be discussed first, and then, the analysis of the parameters to be detected and controlled is given in the next subsection. Finally, the total calibration loop will be presented.

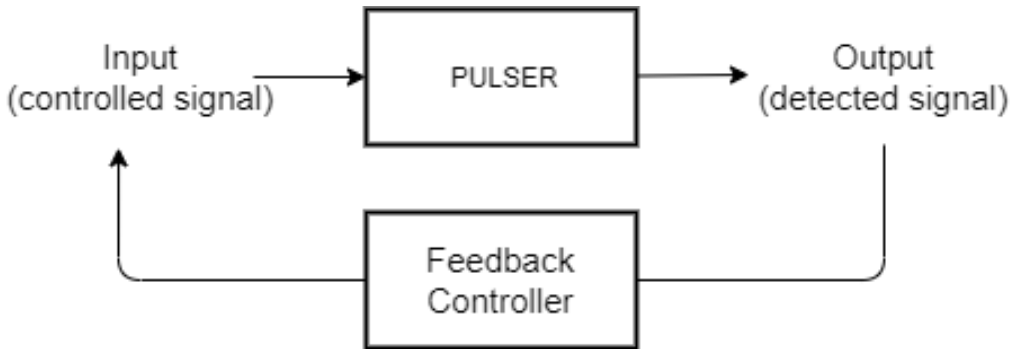


Figure 2.4: A simplified feedback loop for amplitude modulation

2.3.1 Strategy for feedback path

There are mainly two possible solutions for the feedback path:

Continuous-time feedback

The parameters of the output signal have a direct influence on the input by continuous time analog feedback circuits, and the signal fed back to the input is decided by the real-time output. In this approach, delay will be a significant parameter for feed- back path design.

In [17], a continuous time comparator is proposed to compare output signal with the reference voltage. And the comparison result will be fed into switches to charge/discharge the CMUT to achieve pulse-amplitude control. In this way, the delay of the comparator and switch will be the dominant inaccuracy source of the output.

Discrete-time digital control by calibration

For a feedback path in the digital domain, the input is controlled by a feedback signal derived from the output result in previous cycles. First, the input is given a default value to send pulses. Then, a feedback signal is generated from the detected output and fed to the input. As a result, the delay of the feedback path will not directly influence the input signals. Additionally, the calibration time can be separate from the transition time to avoid processing high-frequency digital signal under high voltage.

2.3.2 Choices for controlled and sensed parameters

As previously discussed in Section 2.2.1, several parameters can be chosen as controllable parameters to modify the pulse amplitude.

In [17], the pull/push charging time of the pulser front-end is set as a variable by changing the on-time of those switches. However, the delay time during the feedback signal transition will become a significant problem for maintaining the accuracy of the amplitude control in [17], which leads to a stricter design specification to the comparator in their design. And the delay will increase the asymmetry of the pulse wave intrinsically. As shown in Figure 2.5, the delay time will increase both the rise time and fall rime, which results in larger voltage steps during charging and discharging period.

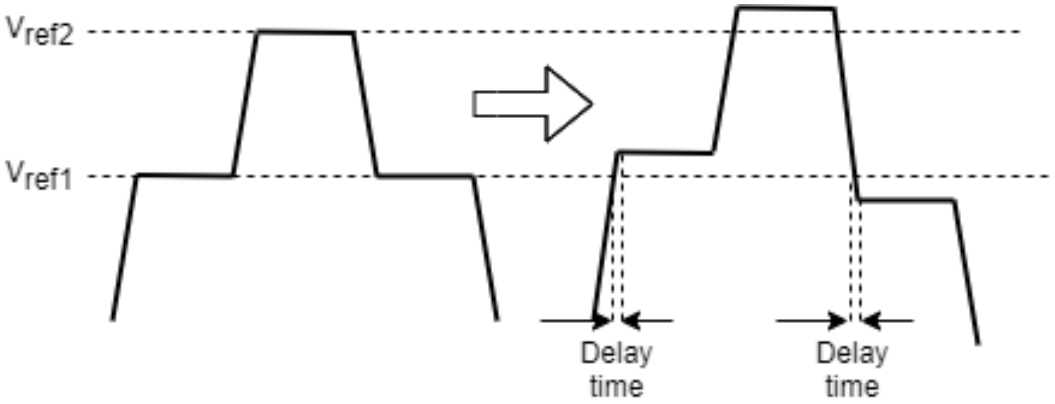


Figure 2.5: The asymmetry behavior of a pulse caused by the delay time

Also, it is hard for time-controlled circuit to achieve the same accuracy as the other ones by applying discrete-time calibration. For the reason that, the accuracy in digital calibration loop is achieved at the expense of more sampling points, which will generate higher frequency clock. This will be a problem especially in high frequency occasions. In this project, we are aiming at driving a CMUT device with a relatively high resonant frequency of 7.89 MHz, so continually increasing frequency is kind of risky. In this design, the current through the pulsing transistor is controlled to change the slew rate of the pulse, while keeping the same charging time fixed. This can be achieved by applying a programmable current DAC, which can be implemented in the low voltage domain which has very low area consumption compared with HV part.

Another thing to be concerned is the way and the moment to detect the transducer output. This will bring out different kinds of detection methods, such as peak detection, root mean square (rms) detection and ending-voltage detection. Peak detection circuits sense the largest peak present in the waveform. Mean-square detectors measure the average of the square of the wave, which is a reflection of energy in the wave [22].

In this thesis, we prefer to detect the ending-voltage, which we sense the output at certain sampling time when the oscillation of the waveform ends. Compared with other methods [23, 24], detecting the ending voltage has simpler structure and easier to match the sampling signals.

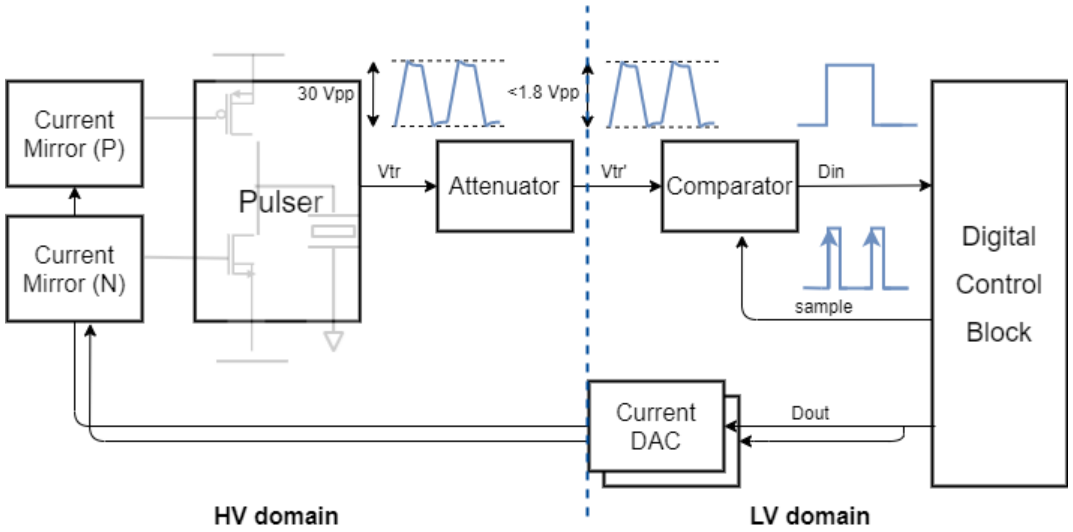


Figure 2.6: A simplified feedback loop for amplitude modulation

In this design, the output pulsing signal is a high voltage signal. As shown in Figure 2.6, to avoid HV devices in the detect circuitry, an attenuator should be implemented to convert this signal into low the voltage domain. The implementation of this attenuator will be discussed in the following sections. The following part of the detect circuitry will be a digital comparator, which compares the attenuated output with a reference voltage at the edge of a sampling signal. The comparison results will be sent to a digital feedback control block and change the level of the current DACs. These two current DACs are proposed to control the slew current of PMOS and NMOS transistors separately.

In this work, the low voltage part including the comparator, digital block and current DAC can be implemented under 1.8 V supply voltage. HV devices are used in the level shifter, pulser and attenuator, which occupy the most die area. With these in mind, the total calibration loop can be described in the following subsections.

2.3.3 Digital control block

The digital control block should be capable of converting the detection result into a control signal for the pulser. As mentioned earlier, this control signal will be used to operate the switches of the two current DACs.

Figure 2.7 is a block diagram of the digital block design. The comparison result of the comparator is processed in SAR logic and determines the digital output of the block [25]. Two SAR logic blocks are proposed to generate the code for PMOS driver and NMOS driver separately. The following signal generator with an internal clock provides sampling signals for the comparators and arranges the digital signals from SAR logic blocks to the DAC with proper timing.

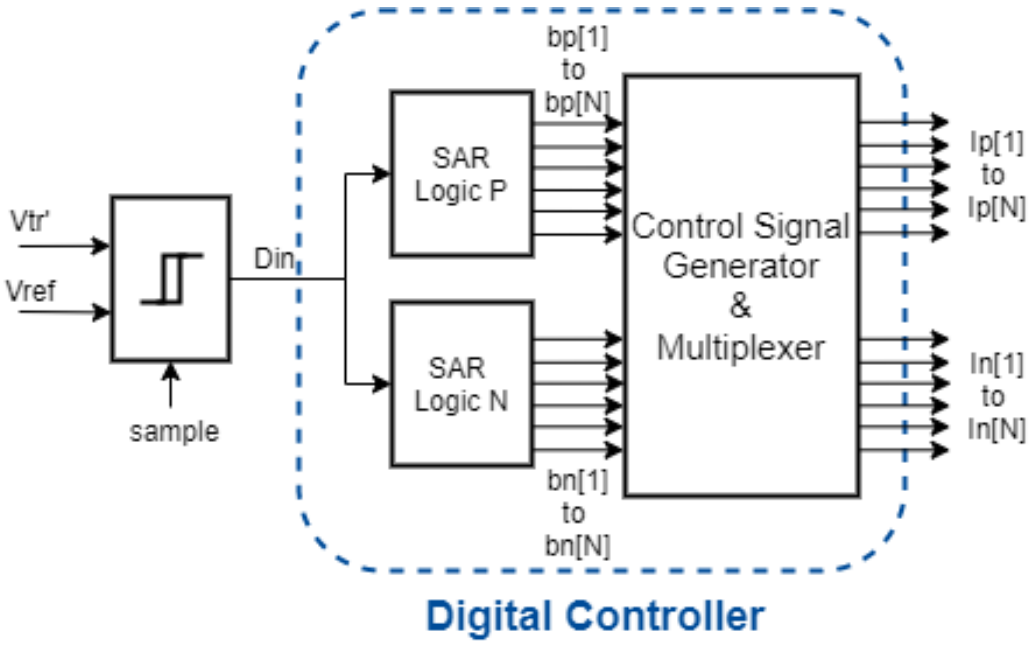


Figure 2.7: Design diagram of the digital control bloc

Figure 2.8 shows the timing diagram of the calibration process for charging from 0 to a reference voltage V_{ref}. The vertical purple line presents the sample time of the dynamic comparator, and the black dash line shows the time when changing the code of DAC and charging with different current levels. The changing of the code for current DAC follows the SAR logic starting from MSB b[N] to LSB b[1]. Din presents the comparison result between the attenuated pulse Vtr' and the reference Vref at sampling time. If the result is Low, the current bit operating by SAR will be changed to High, which increases the slew rate of the pulse and consequently increasing the amplitude. At the beginning of the calibration phase, a default code at the current DAC will generate a pulse during the first time cycle. The MSB b[N] will be changed after receiving the comparison result at the first cycle, and the this code will used as the input of the pulser at the second cycle. As a result, for a N-bit DAC, N+1 time cycles are needed for calibration.

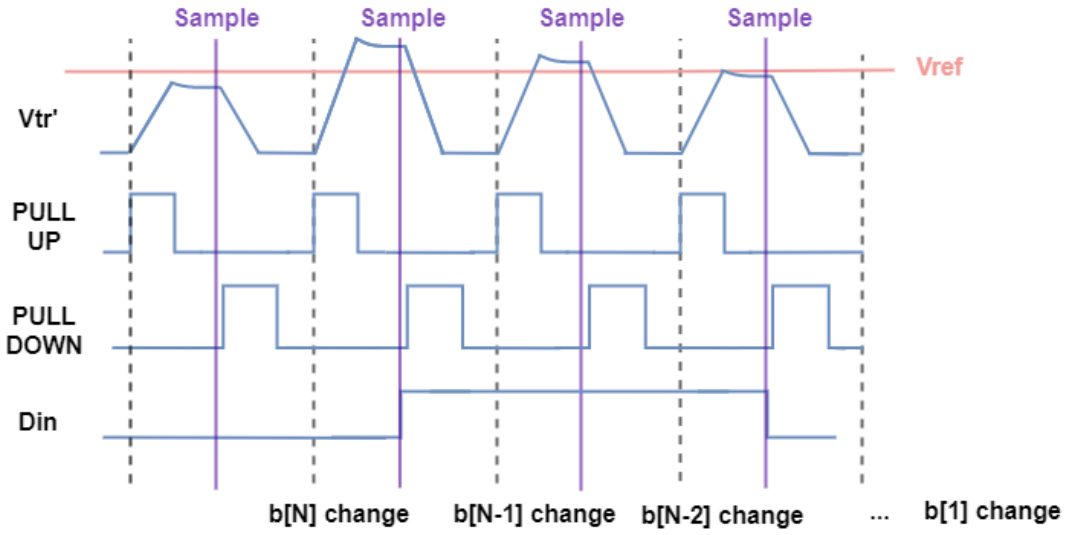


Figure 2.8: Time diagram of the calibration process

The 'PULL UP' and 'PULL DOWN' are not shown in Figure 2.6, since they are not working as ports but inner signals which control the outputs of the digital block. For example, the Multiplexer transfer the output of SAR logic block to the current DAC when 'PULL UP' is on. While 'PULL UP' signal is off, no current will go through the pulser. And same functions 'PULL DOWN' has. They work instead of HV switches on the pulser in other designs.

In this work, these blocks are simulated by VerilogA, and in the actual application, they can be integrated on chip and shared by some groups of element channel for apodization at different time.

2.3.4 Building a Calibrate—Transmit—Receive structure

To avoid high frequency switching during transmission, a separate calibration phase is proposed before the start of the TX and RX phases. The result of calibration can be applied in multiple following TX/RX phases.

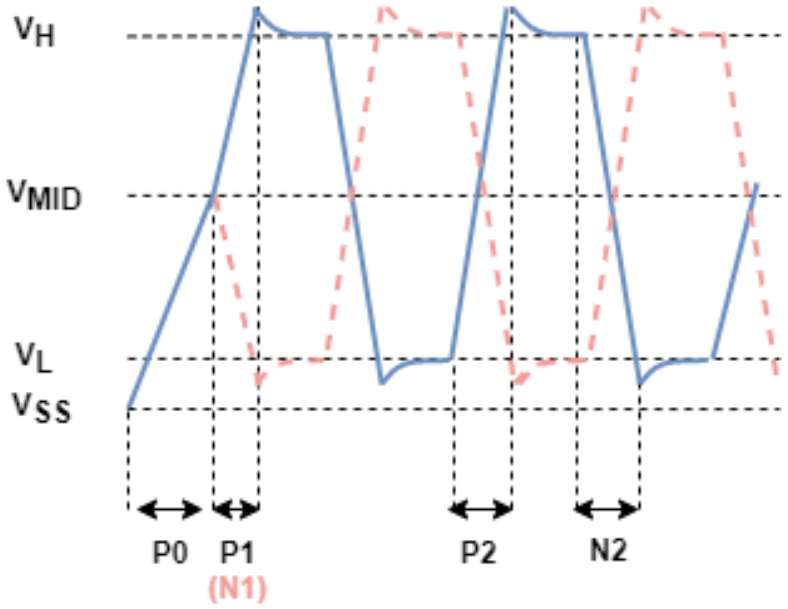


Figure 2.9: The steps to be detected during the transmission phase

There are five steps to be calibrated in the pulsing during transmit mode as shown in Figure 2.9:

- **P0:** Initial charging from ground to the middle voltage V_{MID} through PMOS transistor. The transducer is initially discharged to ground and hence needs to be brought to the V_{MID} level for bipolar pulsing.
- **P1:** Charging from the middle voltage V_{MID} to the high voltage V_H through PMOS transistor. This is the initial step of a pulse train.
- **P2:** Charging from the low voltage V_L to the high voltage V_H through PMOS transistor.
- **N2:** Discharging from the high voltage V_H to the low voltage V_L through NMOS transistor.
- **N1:** Discharging from the middle voltage V_{MID} to the low voltage V_L through NMOS transistor. This is the initial step of an inverted pulse train.

The current levels required for each step are detected and recorded as DAC-control codes by the digital control loop during calibration. When generating pulses during the TX phase, these codes are applied to the current DACs.

In potential application, the pulser works in calibration phase at the beginning, which generates current control codes for the following transmission and receive cycles. The procedure will repeat periodically as a reset to avoid the voltage drift of the pulse.

2.3.5 Comparison with the prior art

As shown in Figure 2.6, the block diagram introduces the working scheme of the calibration loop, The HV pulses Vtr generated from the pulser will be attenuated into the low voltage domain. The digital block triggers the dynamic comparator. Then the comparison result will be processed by successive-approximation logic in the digital control block. The output of the digital controller are the control signals of the current DACs, which change the charge and discharge current levels. Compared with previous works [refs], the level shifter here should be capable of transmitting different levels of signals, which means that traditional shifter is not enough. A current mirror is implemented as a current amplifier and level shifter here to drive the HV pulser with different signal levels.

A comparison of the proposed HV pulser with different amplitude-control methods is shown in Table 2.2. Compared with previous designs, this work aims at decreasing the number of HV devices, and consequently, decrease the die size.

Table 2.2: Control Method Comparison with Prior Art

	This work	[9]	[17]
Feedback strategy	Digital calibration	Not applicable	Continuous-time feedback
Detected parameter	Ending-voltage	Not applicable	Ending-voltage
Controlled parameter	Slew Rate	Slew rate, Rise/Fall time, Power supply	Rise/Fall time
#HV Transistors*	4	12	3
#HV Passives**	2	4	3

*Including HV MOS in level shifters
**HV-tolerant capacitors and resistors.

2.4 RECEIVE CHAIN

The receive chain of an ultrasound ASIC may consist of a low-noise amplifier, a time-gain compensation (TGC) stage and delay lines for sub-array beamforming for each transducer elements, as shown in Figure 2.10. In this thesis, we focus on the connection between the receive circuitry and the transducer as a proof of the feasibility of the design.

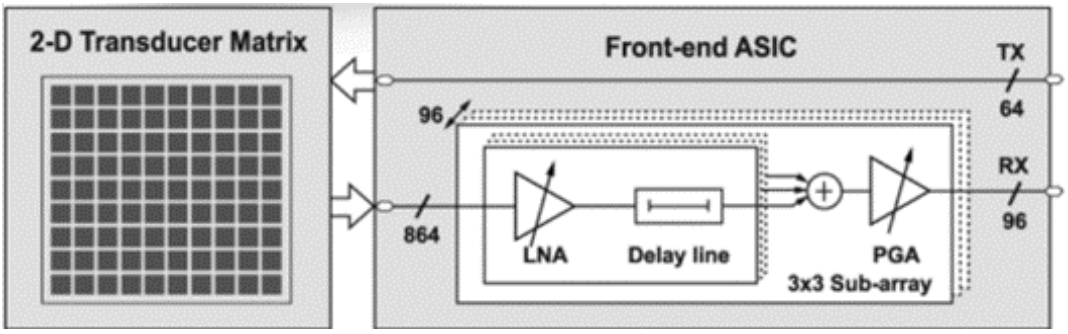


Figure 2.10: Receive circuitry for ultrasound transducer array [26]

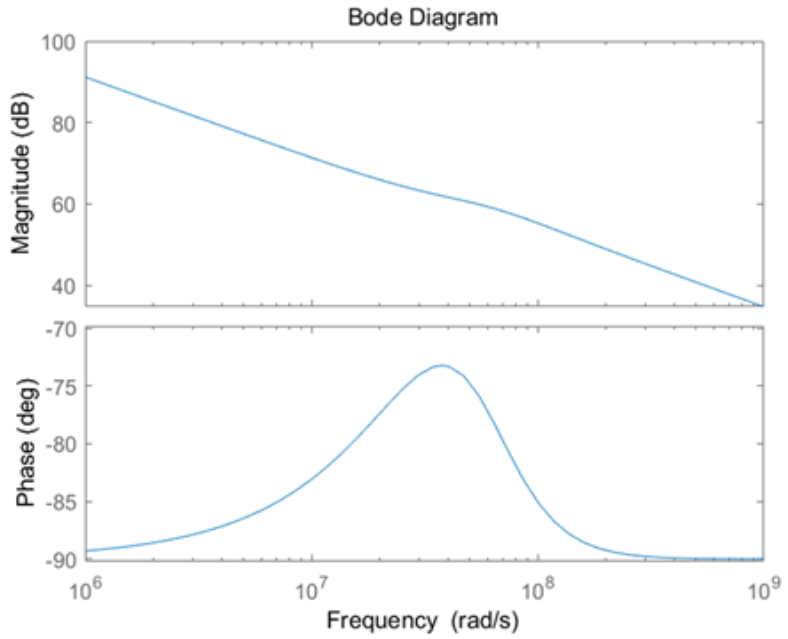


Figure 2.11: Impedance characteristic of the targeted CMUT model

The impedance of the targeting transducer determines the following design of low noise amplifier. Figure 2.11 shows the impedance characteristics of the extracted CMUT model simulated by MATLAB. The transducer has a impedance of 4 kΩ at its resonance frequency:

$$f_{res} = 1/(2\pi\sqrt{LC}) \tag{2.7}$$

The impedance of the transducer used in this design is relatively low, which means that a capacitive-feedback voltage amplifier is a good choice for LNA implementation. In [27], an LNA structure is proposed that is also adopted in this work and is shown in Figure 2.12.

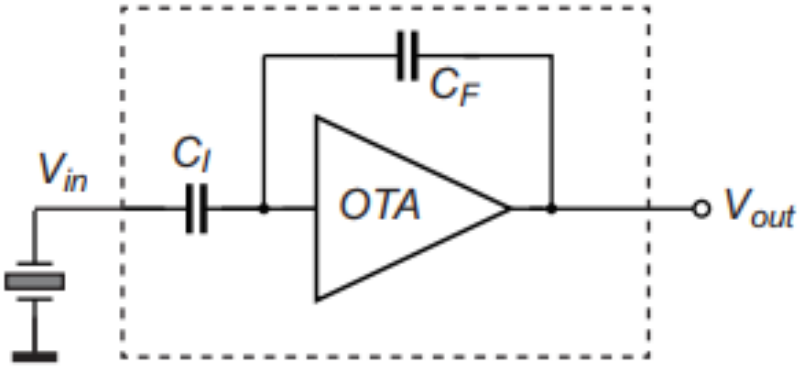


Figure 2.12: The proposed LNA structure [27]

The gain of this LNA can be expressed as:

$$A_M = C_I/C_F \tag{2.8}$$

The input impedance is dictated by the input capacitor C_I, which can be made small and thus provides a relatively large impedance compared with the transducer. And the mid-band frequency is still within the bandwidth determined by the operational trans-conductance amplifier (OTA) and the band of interest.

A T/R switch can be added between the input of OTA and ground. By closing this switch during the TX phase, the RX circuitry is protected, but also, the mid voltage is stored on the input cap of the LNA, so that the transducer can remain biased at V_{MID} during the RX phase, while the LNA operates in the low-voltage domain.

2.5 ARCHITECTURE OVERVIEW

The overall architecture of the design is shown in Figure 2.13. During the calibration phase, the codes for the current DACs are detected and recorded in the digital control block. Then, they are applied during the transmission phase. The switch in receive phase is on to protect the LNA from the HV during pulse transmission until the beginning of echo detection. After several T/R cycles, the circuit starts calibrating again to maintain the mid-voltage. A voltage DAC is added as a tunable reference voltage to achieve amplitude modulation. The V_{ref_high} and V_{ref_low} are set differently for send pulses with different amplitudes. The detail for each block will be introduce individually in Chapter 3.

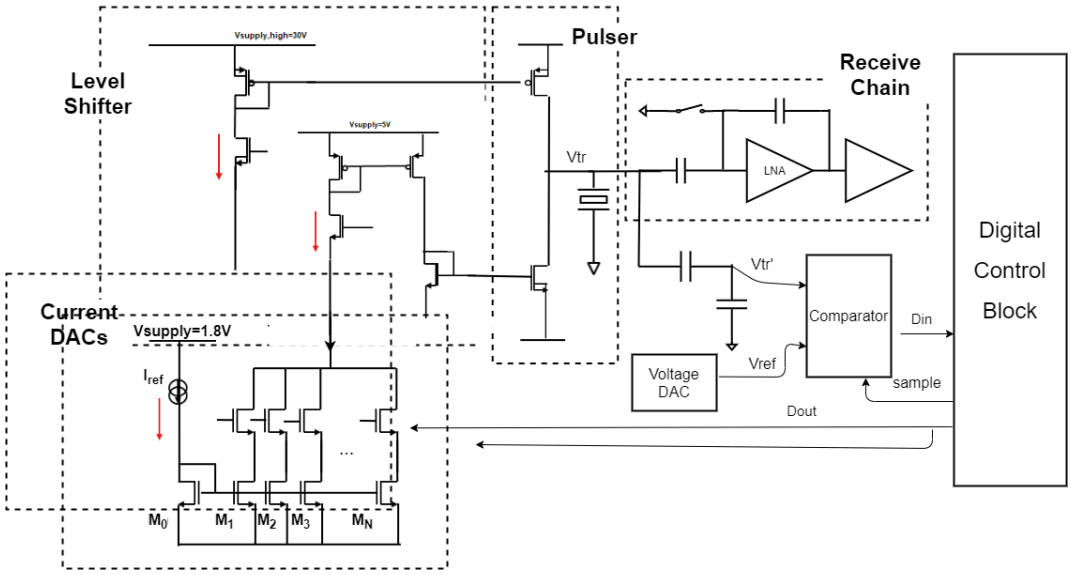


Figure 2.13: The architecture overview of the pulser design.

3 CIRCUIT IMPLEMENTATION

This chapter describes the circuit implementation of the different blocks of the pulser design, including the current switching DAC, the current-mirror-structured level shifter, the capacitive attenuator, and the dynamic comparator. For each block, the design requirements will be introduced, and the performance will be analyzed after the simulation of the circuit design.

3.1 CURRENT DAC AND LEVEL SHIFTER

As mentioned earlier, current DACs are implemented as programmable current sources to provide different levels of charging current. To minimize the chip area, the transistors used in the DACs are all low-voltage devices. As a result, the output of the DACs are also in the low-voltage domain. Therefore, a level shifting stage is needed to convert the low-voltage signal into HV (5V for gate driving) control signals. In this subsection, we will discuss the circuit and the performance of these blocks.

3.1.1 Current DAC

The current steering DACs in the design are used as variable current sources to provide different levels of input currents. Because of the implementation of the calibration loop, the errors associated with the current DAC can be corrected. The accuracy of the DAC is not the main factor to determine the proposed structure. Instead, we can choose a less accurate but simpler [28] structure to minimize the die size of the pulser. For this reason, a binary-weighted current-switching DAC is chosen.

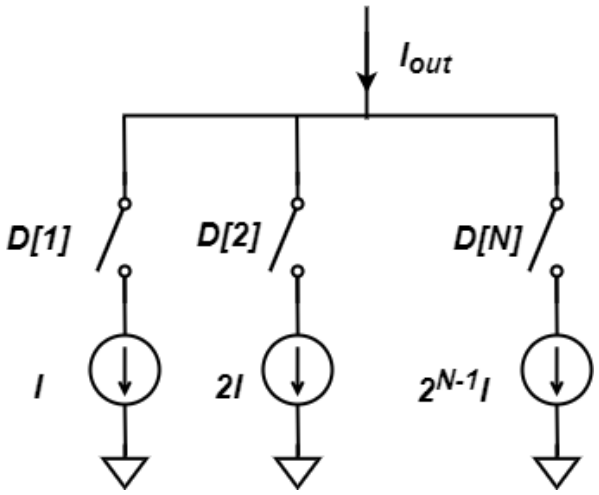


Figure 3.1: Circuit diagram of binary-weighted current-switching DAC

A typical binary-weighted current-switching DAC structure is shown in Figure 3.1. It converts N -bit digital signals D[1] to D[N] at its switches, to an analog current, I_{out}. D[N] is the most significant bit (MSB) and D[1] the least significant bit (LSB). The output current I_{out} can be expressed as:

$$I_{out} = D[N]\left(2^{N-1}I\right) + \ldots + D[2](2I) + D[1] \quad D[i] \in [0,1] \quad i \in [1,2\ldots N] \quad (3.1)$$

where I is the DAC's unit current.

Compared with other structures, the current-switching structure has a simpler output, but suffers from current transients when turning on the branches.

The schematic of the current DAC in the design is shown in Figure 3.2. The transistors M_1 to M_N work in the saturation region, copy and amplify the current I_{ref} from Mo by 2^N times. These transistors play the role of the current sources in Figure 3.1. The transistors at the drain of these current sources work as switches in the triode region. The output current is the sum of the currents through the on-switches.

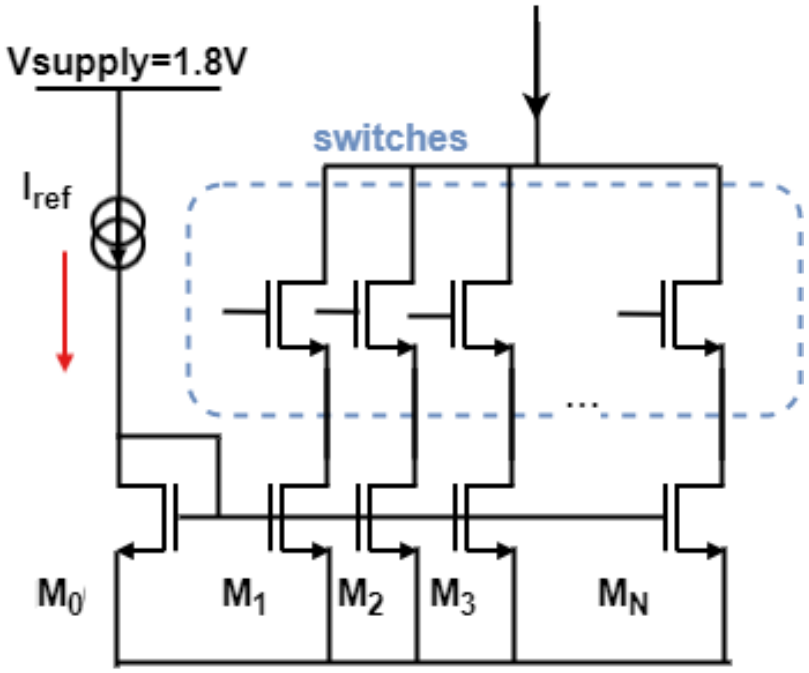


Figure 3.2: Circuit schematic of a binary-weighted current-switching DAC

3.1.2 Level shifter

The circuit schematic of the level shifters in the circuit are shown in Figure 3.3 :

A cascode NMOS transistor is added at the output of the DAC to protect it from the HV at the input of the high-side current mirror. In this figure, two HV transistors are applied for driving PMOS, and four 5 V transistors for driving NMOS. The sizing of the current amplifier will be discussed in the following subsection with simulation results.

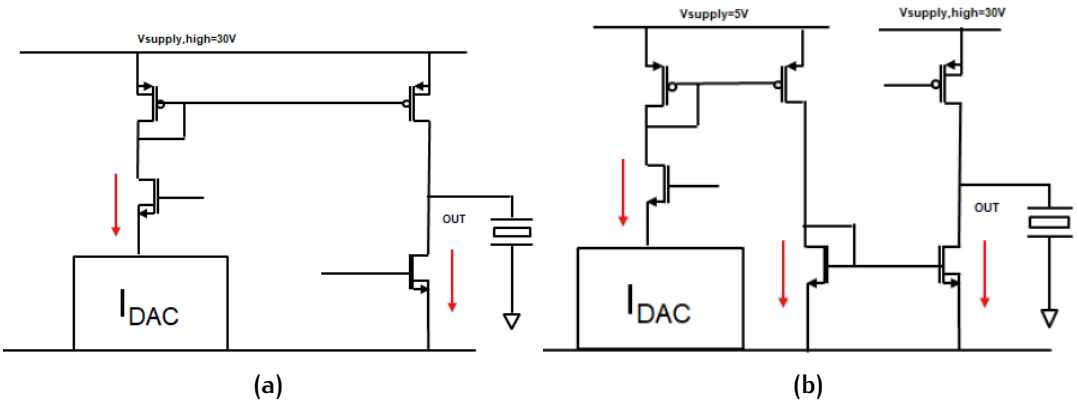


Figure 3.3: Level shifter for (a)PMOS and (b)NMOS driving

3.1.3 Simulation and analysis

The number of bits and the unit current of the DAC are determined by the modulation range of the pulse amplitude. The relationship between the acoustic power and the peak-to-peak amplitude Vpp of the pulse, simulated with an ideal current source, is shown in Figure 3.4.

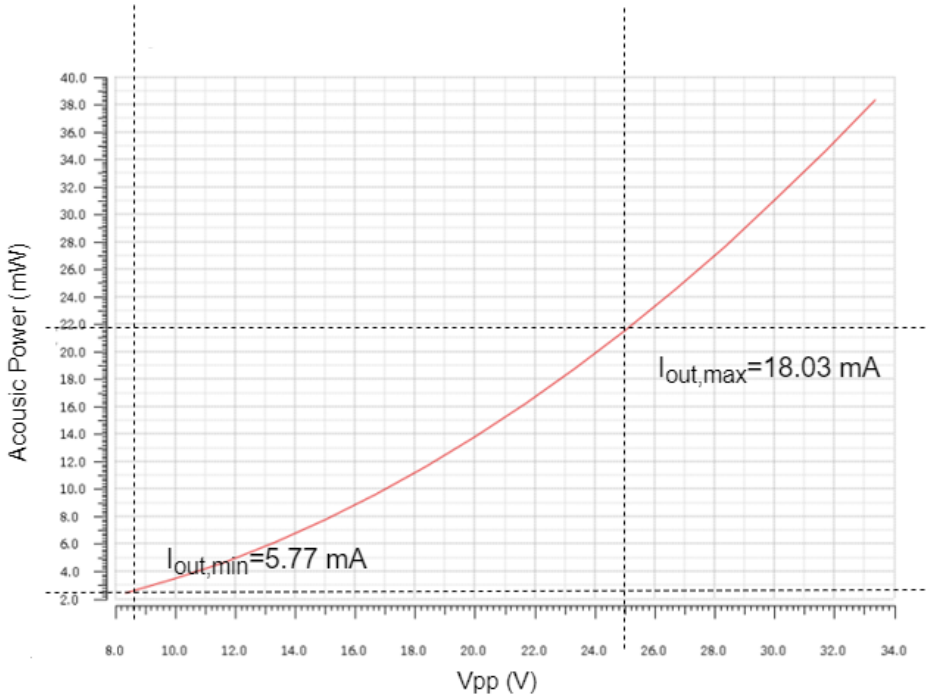


Figure 3.4: Acoustic power corresponding to different peak-to-peak values of the pulse

As in Section 2.2.3, the acoustic power is simulated as the average of power dissipated in the resistance R_M in the transducer model while it is pulsed at a frequency of 7.89 MHz . In order to reserve enough voltage headroom to keep the HV MOS transistors saturated at a 30 V supply, the maximum Vpp is temporarily chosen to

be 25 V. As shown in the figure, a 20 dB decrease of the acoustic power comes from 10 dB decrease of the Vpp, which is also 10 dB lower of the slewing current.

As a N-bit DAC, the quantization error caused at the output voltage δV_{tr} can be estimated by:

$$\delta V_{tr} = V_{pp} * 1/2^N * M \tag{3.2}$$

in which M is the number of cycles in one transmission phase.

In this design, the errors at output will be accumulated after sending several pulses in transmission phase, which cause a voltage drift at the output. It is better implemented in short-pulsing situation than long-time pulsing. A 6-bit DAC is proposed to achieve a quantization error less than 0.31 V at the output. Which means that, an unit current of the DAC should generate a output current around 2 mA, which is 64 times smaller than the maximum output current. This current can be generally calculated by multiplying the LSB current of the DAC and the amplification factor of the current mirror.

A transient simulation of the output current for increasing binary input codes is shown in Figure 3.5. The output current has a clear step behavior. However, a non-monotonicity can be seen in the characteristic between the transition from 011111 to 10000, in which all the switches in the DACs are turning on and off at the same time, and the brings in large charging current.

The integral non-linearity (INL) and differential non-linearity (DNL) are the main factors to evaluate a DAC. The INL plot shows the deviation of a practical output given from the ideal conversion function and the DNL plot shows the deviation of each step compared to the size of LSB [29]. Usually, they are expressed as:

$$\text{INL} = \max, \min \left(\frac{A(i) - i \times A_{LSB}}{A_{LSB}} \right), \forall i = 0.. \left(2^N - 1 \right) \tag{3.3}$$

$$\text{DNL} = \max \left| \frac{A(i+1) - A(i)}{A_{LSB}} - 1 \right|, \forall i = 0.. \left(2^N - 2 \right) \tag{3.4}$$

To obtain enough sample points for INL and DNL measurements, and a data storage of $10 * 2^N$ is necessary to achieve 0.1 LSB accuracy [29]. In this design, the least numbers of samples to be selected is 640.

The INL, DNL of the current DACs are shown in Figure 3.6 and Figure 3.7.

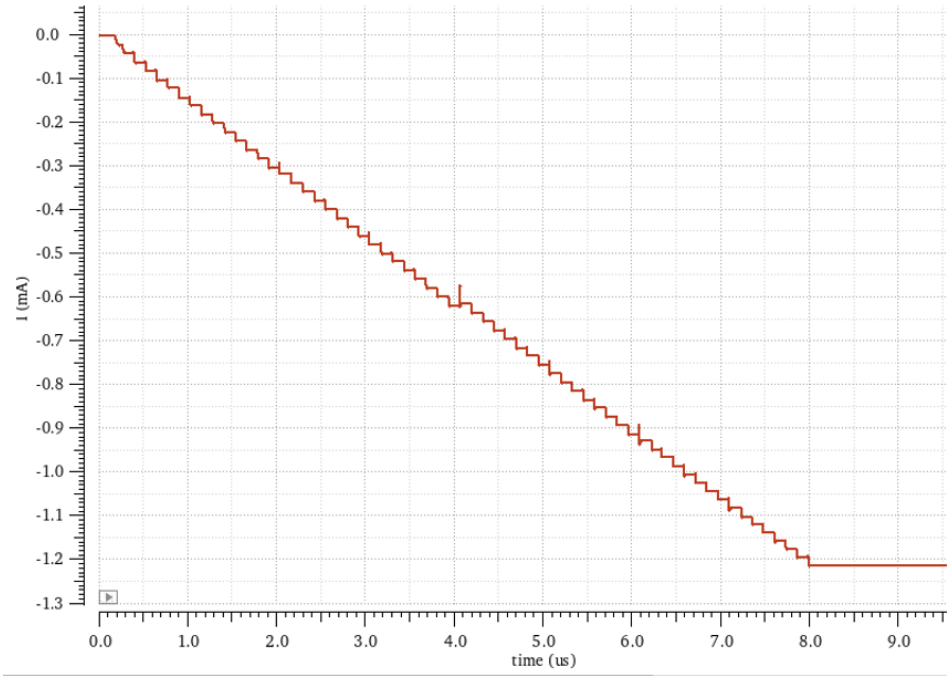
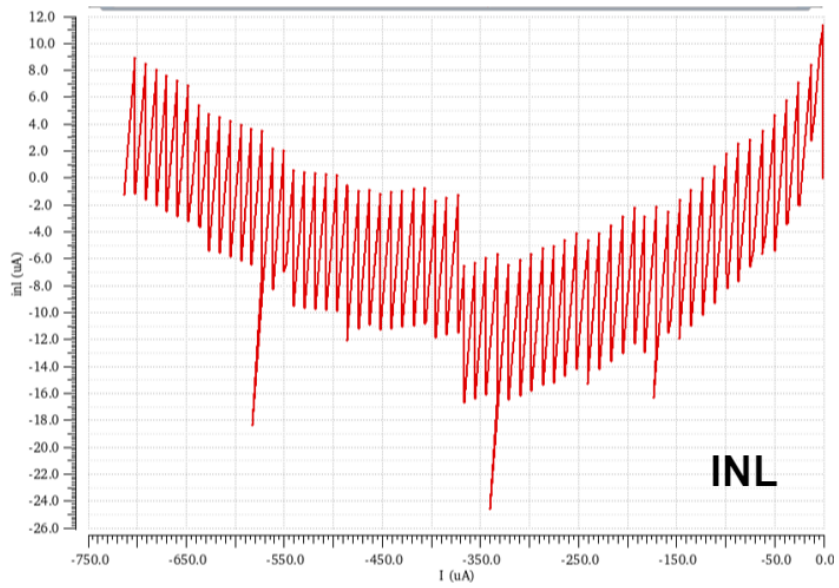


Figure 3.5: Transient simulation of the 6-bit DAC applying a binary weighted step-up input code

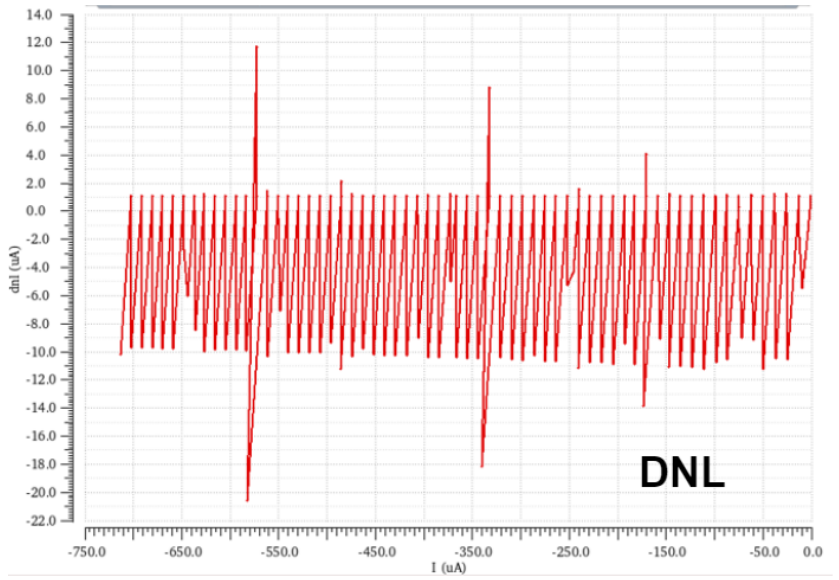
As shown also in the transient simulation plot, as a current-switching DAC, spikes mainly occur when switching on the MSB and cutting off others. In this situation Different from the transient plot, the spikes on the INL and DNL mainly come from the inaccuracy of code steps because of the binary structure. Because of the errors in transistor-level structure and the implementation of the load, the sum of the lower bits current is possibly different from $(2^N - 1) * I$. Thence, the inaccuracy and even nonmonotonicity may occur in the characteristics. Usually, this problem can be solved by applying a Binary-Thermometer Decoder and adding switches at every unit current source cell [28].

In this thesis, the functionality of the DACs is only offering applicable input current levels. And the inaccuracy of the DACs will not influence the accuracy of the output pulse as long as they can provide reproducible results, and even the nonmonotonicity can be seen as only a 1 LSB input range loss. Instead, the resolution of the DACs, the quantization error, is shown as the main cause of the output inaccuracy. To make it more compact, this kind of inaccuracy at the DAC can be accepted.

The difference between the current DAC for driving PMOS and NMOS transistors shown are caused by the different structure and sizing of the level shifters as loads. To reduce the power consumption of the driving circuit, the size ratio of the current mirror pair is set as a large value such as 1:10. The corresponding LSB current of the DAC can be 20 µA, which gives a 0.4 mA to 25.6 mA input range, in which the minimum current in Figure 3.4 can be generated at 1/5 FS, and the maximum

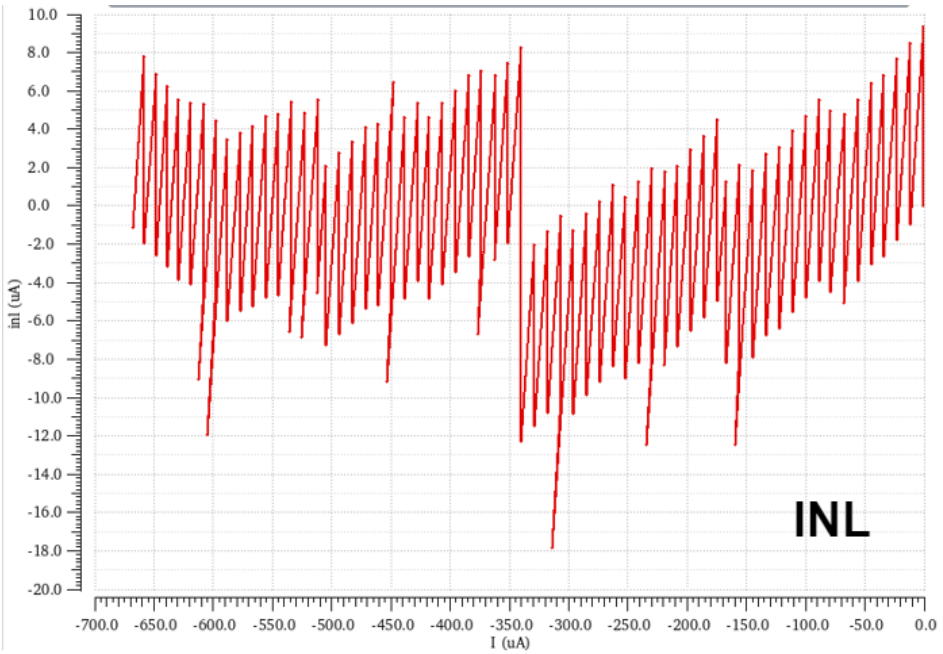


(a)

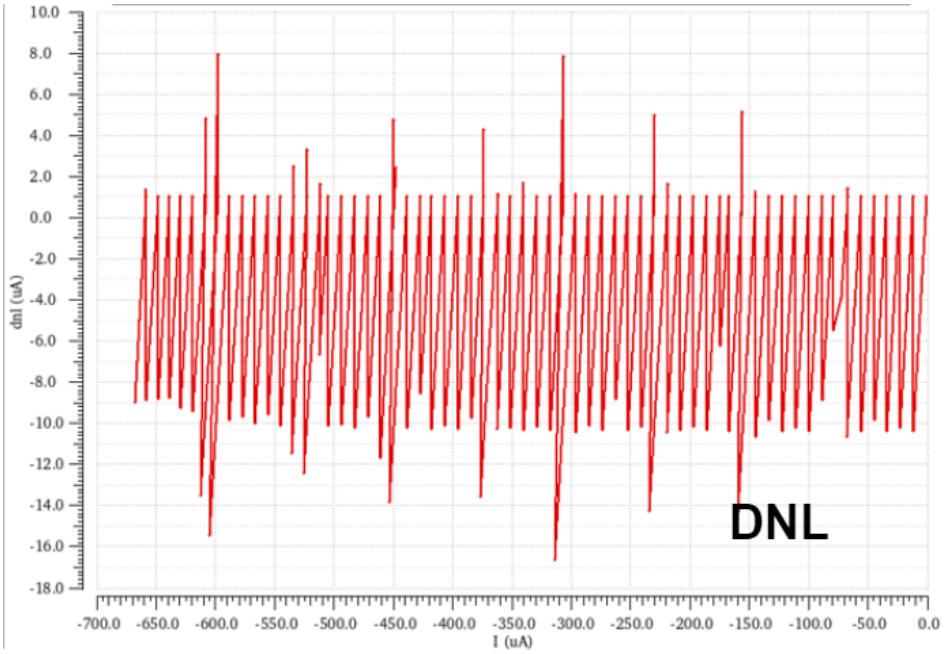


(b)

Figure 3.6: (a) INL and (b) DNL characteristic of the current DAC for HV PMOS driving



(a)



(b)

Figure 3.7: The (a) INL and (b) DNL characteristic of the current DAC for HV NMOS driving

current at 3/4 FS.

3.2 CAPACITIVE DIVIDER

The capacitive divider is proposed as an attenuator to obtain a detectable low voltage signal. A design target is to minimize the die area required.

A capacitive divider is implemented in parallel with the transducer as shown in Figure 3.8. The attenuation factor will be $C_{d1}/(C_{d1}+C_{d2})$.

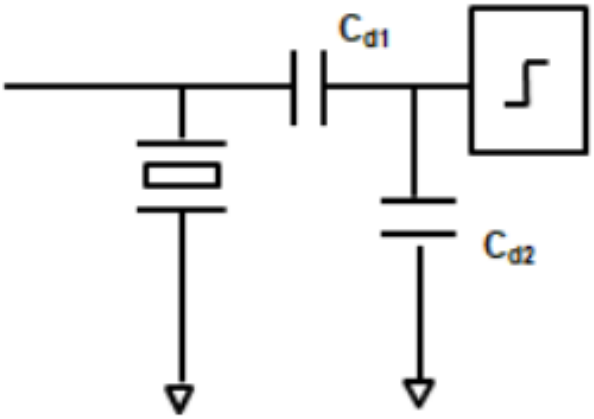


Figure 3.8: Capacitive divider in the calibration loop

C_{d1} should be small compared with C_p (18.29 pF) to avoid significantly increasing the load at the pulser output.C_{d2} should be big compared with the input capacitance of the comparator (100 fF) to maintain the attenuation ratio. To ensure the operation of a 1.8 V comparator at the output, the attenuated amplitude should at least smaller than 1.8 V. The value of $C_{d1}/(C_{d1}+C_{d2})$ should smaller than 0.06.

The main challenge in the design of the capacitive divider is the trade-off between mismatch and die size. The mismatch of the capacitive divider mainly comes from the spread, and the die size occupied by HV high-capacitance capacitor can be extremely large.

The C_{d1} should be a HV capacitor, because it faces the HV signal from the pulser during the whole process. In this work, it is simulated as a HV finger metal oxide metal capacitor (FMOM) in tsmc 180 nm BCD process. There are two options for implementing C_{d2}:

- Apply C_{d2} also as a HV capacitor. This is better for matching because the two capacitors are of the same type. However, it will lead to a much larger die

size, because C_{d2} is substantially larger than Cd1 and thus HV caps have a relatively large die size.

- Make C_{d2} a (denser) LV cap. This will lead to a smaller die size, but introduces mismatch, because the capacitor ratio will be sensitive to process spread.

As part of the calibration loop, the mismatch of attenuator and comparator themselves won't be calibrated, which means that a $X\%$ ratio mismatch at the input of the comparator will cause $1/(1 + X\%)$ amplitude error of the calibrated value.

Some solutions can be applied to avoid this mismatch such as: 1) Testing the real ratio during measurement and using the result, which means extra time and structure is needed for the detection. 2) Simulating possible mismatch. Then, the problem will be how much of the mismatch it can suffer.

If we assume FMOM is used in both capacitors in the attenuator, 0.1 pF HV capacitor occupies an $8.46\,\mu m \times 19.92\,\mu m$ die size. And even the die size of the 2.4 pF capacitor is still smaller than that of HV transistors. Also, it is possible to put the FMOM capacitors on the top of the transistors, since the layers of FMOM capacitors are mainly over the poly shielding as illustrated in the manual from *TSMC* So it is acceptable to apply HV process to both of the capacitors for better matching.

As a result, a 0.1 pF – 2.4 pF capacitive divider gives a 1.2 V attenuated output, which can be driven by a PMOS input dynamic comparator.

3.3 DYNAMIC COMPARATOR

The low voltage dynamic comparator in the circuit compares the attenuated pulse with a reference voltage at the sample time during the calibration phase. The digital output of the comparator will be used by the digital control block for the calibration process.

3.3.1 Design requirement

The input range that the comparator needs to be able to handle is dictated by the detection accuracy at the pulser output and the chosen attenuation factor. The accuracy with which the levels at the pulser output need to be detected translates into offset and noise requirements of the comparator. It can be reflected as the bits of the voltage DAC providing the reference voltage for the comparator. The attenuation factor depends on the ratio of the capacitive divider. By increasing the attenuation factor, the input range can be reduced but implies that the offset and noise requirements become stricter. With a 0.1 pF – 2.4 pF capacitive divider, a 1.2 V attenuated

pulse will be sent to the input of the comparator, which requires the comparator as least can operate under the full scale of the attenuated output.

The output of the attenuator just follows the rising and falling behavior of the input pulse but starting from some different DC voltages. These DC voltages can be unpredictable after several time cycles because of the resonance behavior of the transducer. To get rid of this kind of uncertainty, the pulsing signal is always discharging to the ground before the each start of the calibration process. As a result, the comparator should be able to detect the zero input. Finally, a 0 to 1.2 V input range is required, which means that the PMOS input is necessary to avoid biasing problem.

Besides, the speed and offset are also important factors for the comparator. With the consideration of the calibration loop, the input-referred offset is a significant parameter which can be large and directly influences the output.

The offset of the comparator mainly comes from the mismatch of devices during the process. Compared with inaccuracy caused by quantization error:

$$\Delta V_{out} = \Delta I * dT * 1/C_p = LSB * G * dT/C_p \approx 0.5V \tag{3.5}$$

In which G implies the current amplification factor of the level shifter. The result will be transferred into a 0.5*1.2/30 = 20 mV inaccuracy at the input of the comparator. As a result, the input-referred offset of the comparator should be at least smaller than this value.

The speed of the comparator is dictated by the calibration process. This provides less strict requirement to the comparator since the time for calibration is discrete from the transmission phase. As a result, only a small part of the delay time will have an influence on the decision of the comparator.

3.3.2 Circuit design

Since the input signal to be compared starts form 0, a comparator with PMOS input is required. A possible solution is a dynamic comparator as shown in Figure 3.9.

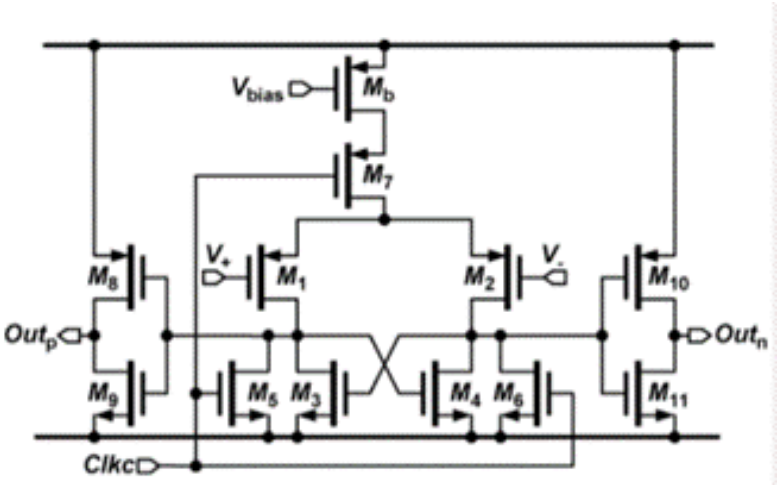


Figure 3.9: A typical dynamic comparator [30]

The input-referred offset of the design can be analyzed by [31]:

$$V_{os} = \Delta V_{TH1,2} + \frac{(V_{GS} - V_{TH})_{1,2}}{2}\left(\frac{\Delta S_{1,2}}{S_{1,2}} + \frac{\Delta R}{R}\right) \tag{3.6}$$

As shown in the equation, the larger the size of the input pair M_1 and $M2$, the smaller the offset of the comparator. With the trade-off between the allowed input swing, kick-back, and baseline delay, we choose the size of input pair at 20 u/0.18 u. Since the input swing is 1.2V, the $(V_{GS} - V_{TH})$ of the input pair won't be so small to maintain proper biasing, which might result in a relatively large offset.

For theoretical calculation, the offset of the transistors can be calculated as [32]:

$$\sigma_{\Delta_{GS}} \approx \sigma_{\Delta V_T} = \frac{A_{V_T}}{\sqrt{WL}} \tag{3.7}$$

In which the A_{V_T} of the TSMC 1.8V NMOS model *nch* is around 4 mVum. The $\sigma_{\Delta V_T}$ equals to 2.1 mV when setting the size of input W/L = 20 um/0.18 um, which is acceptable compared with 30 mV inaccuracy caused by quantization.

The delay time of the comparator can be divided into two parts: The first part is the delay time from the input reaching the reference voltage to the fully charging of the latch M_3, M_6, which determines the decision of the comparator. The second part is time when clips transfer from the the latch to the inverter as the output stage. In this work, two inverters are applied as buffers to maintain the voltage level and polarity for following digital process.

3.3.3 Simulation results

The transient behavior of the dynamic comparator with a 0 to 1.2 V sinusoid input signal is shown in Figure 3.10. The output of the waveform of the comparator are influenced by the size of the charging current and the input waveform. The biasing current generated by M10 should be large enough for sufficiently amplifying the difference of the input and charging the latch.

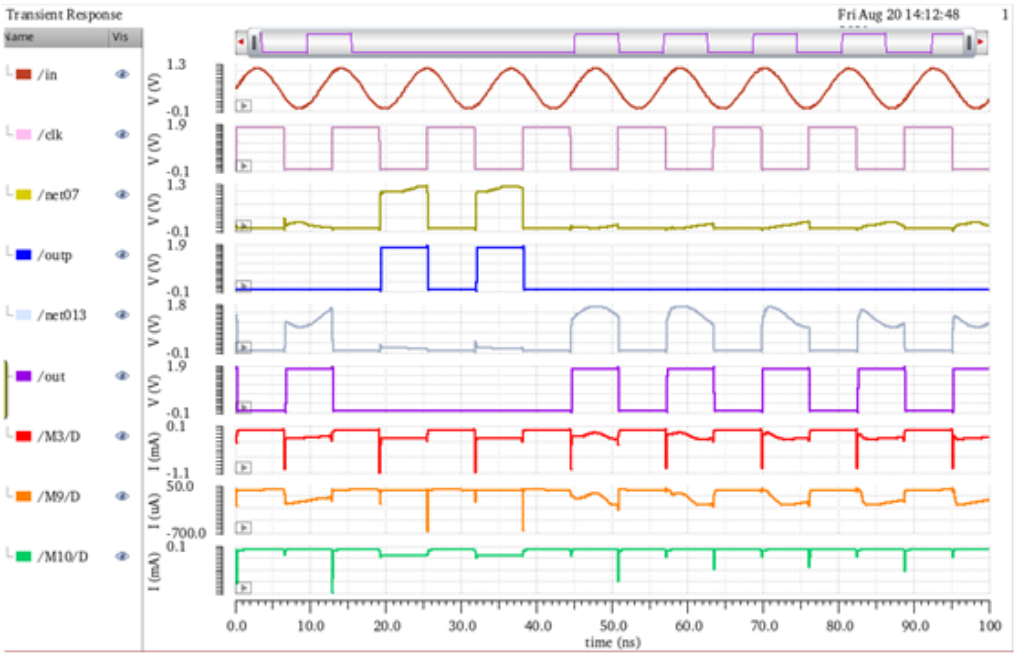


Figure 3.10: Transient behavior of the comparator

The baseline delay of the comparator is shown in Figure 3.11. Increasing the size of the input pair will obviously increase the delay, but the increased delay is mostly added to the time for charging the buffers T_{d2}, and the total baseline delay is still small compared with the stitching frequency, which will not influence the accuracy of the comparator.

Input referred offset mainly comes from the mismatch of devices during the process. Usually, the influence of these mismatch sources can be simulated in mismatch model by Monte-Carlo analysis [33].

To simulate the input-referred offset of the dynamic comparator, a very slow ramp signal is applied at the input so that the input-referred offset caused by the baseline delay is negligible. As shown in Figure 3.12, a delay time T_d is added to the sample signal to avoid the uncertainty around $V_{in} \approx V_{ref}$. Then, the differences between V_{in} and V_{ref} can be calculated as: $V_{in} - V_{ref} = T_d * k_{in}$, where the k_{in} indicates the slop

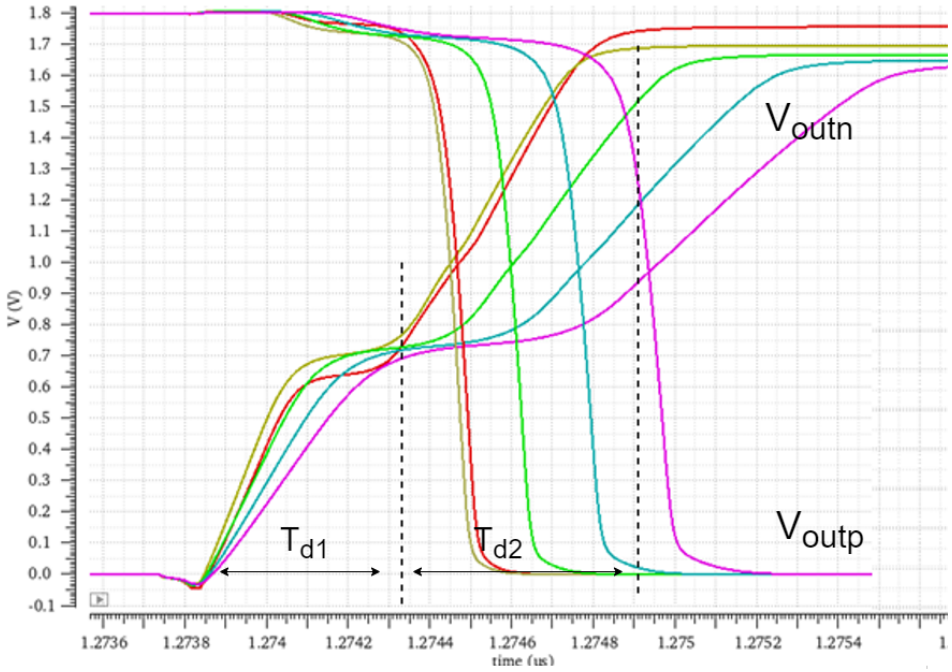


Figure 3.11: The delay behavior of the comparator output

of the input ramp signal. The input referred offset can be expressed as $\Delta(V_{in} - V_{ref})$.

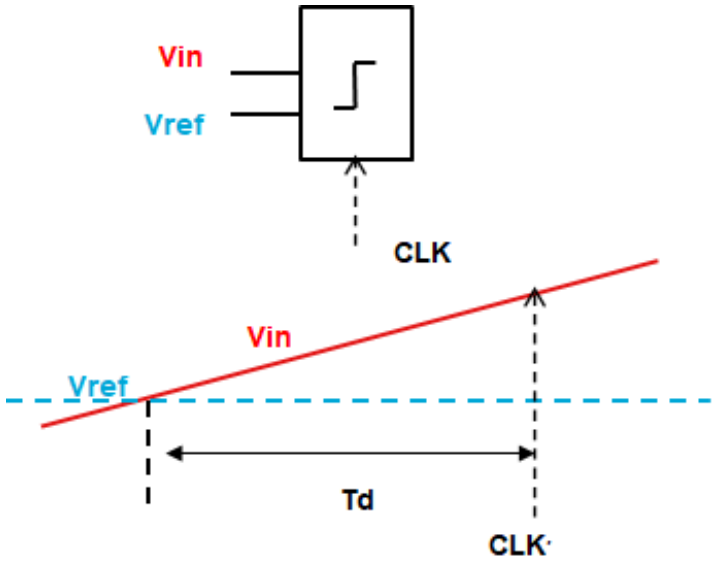


Figure 3.12: The input setting for offset measurement

The statistical result obtained by Monte-Carlo analysis is shown in Figure 3.13. With the considering of total size and delay, we choose the size of input pair 20 um/0.18 um. And get a 1σ offset of 3.3 mV. This value is similar with our calculation 1σ offset 2.1 mV.

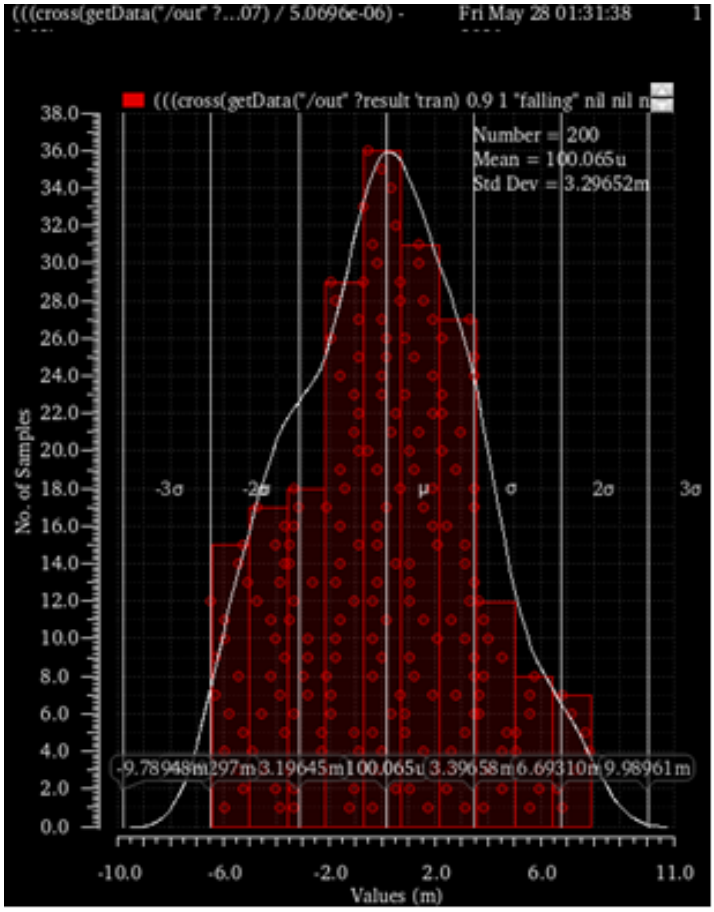


Figure 3.13: The histogram of the input-referred offset caused by mismatch

4 SIMULATION RESULTS

In this chapter, the simulation results of the pulser are presented. The output performance with overall pulser structure will be shown first. Then, the circuit's ability to tune the pulse amplitude will be demonstrated. Finally, the total power consumption will be shown.

4.1 SIMULATION OF POWER FUNCTIONALITY

With the proposed circuits shown in Chapter 3, the overall pulser design is settled. In this subsection, we present and analyze the output performance of the pulser with different input codes to realize amplitude modulation.

4.1.1 Calibration behavior

The output of the pulser during calibration and the first transmission phase is shown in Figure 4.1. In this plot, the reference input voltages of the comparator are set as $V_{ref,low} = 0.2\,\mathrm{V}$, $V_{ref,high} = 1\,\mathrm{V}$. With an attenuation factor of $1/25$, the amplitude of the pulse should be 5 V to 25 V. The output is firstly calibrated to the mid-voltage $V_{mid} = 15\,\mathrm{V}$ by 6-bit SAR approach in 7 counts. Then, similarly, the output is calibrated to the high voltage $V_H = 25\,\mathrm{V}$, and to the low voltage $V_L = 5\,\mathrm{V}$. The DAC current is calibrated and the corresponding DAC input code is recorded at each calibration step. During the transmission phase, these codes are applied to the circuit to generate the levels associated with the desired pulse waveform. At 47 µs, the transmission phase starts and the pulser sends stable output pulses.

4.1.2 Pulse amplitude tuning

When changing the codes of DAC providing reference voltage, the pulse signals after calibration are shown in Figure 4.2. The figure shows a 7-step amplitude modulation from $V_H - V_L = 4\,\mathrm{V}$ to $V_H - V_L = 20\,\mathrm{V}$. While pulses corresponding to 7 reference voltage levels are shown for clarity, more levels can in principle be generated. With the consideration of the maximum 0.5 V inaccuracy of the output signal, it is reasonable to have a maximum 20-step or 4-bit resolution for amplitude modulation. As mentioned in Chapter 2, the output voltage will have a drift because of the accumulation of the inaccuracy during the pulse cycles. The largest inaccuracy comes from the limit 6-bit resolution of the input current DAC.

The peak-to-peak voltage V_{pp} is higher than detected and calibrated value $V_H - V_L$ since it includes the peak voltage before the settling of the transducer. The relationship between the V_{pp}, settled voltage level $V_H - V_L$, and the input reference voltage is shown in Figure 4.3. In this and the following figures, the horizontal axis is the ideal reference voltage V_{ref_low} which is generated by the *VerilogA* with the same input codes applied to the circuit. In this way, the behavior of the design with different amplitude levels can be shown.

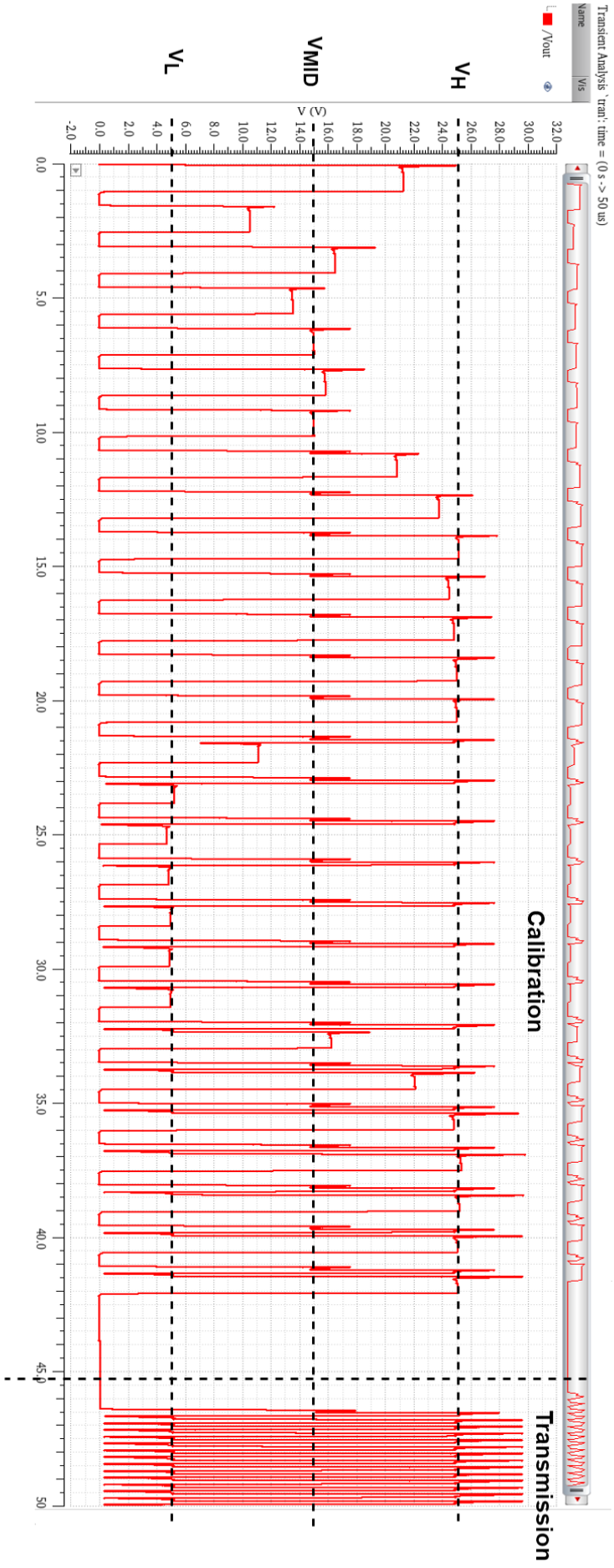


Figure 4.1: Transient simulation of the pulser output during the Calibration phase and the first Transmission phase

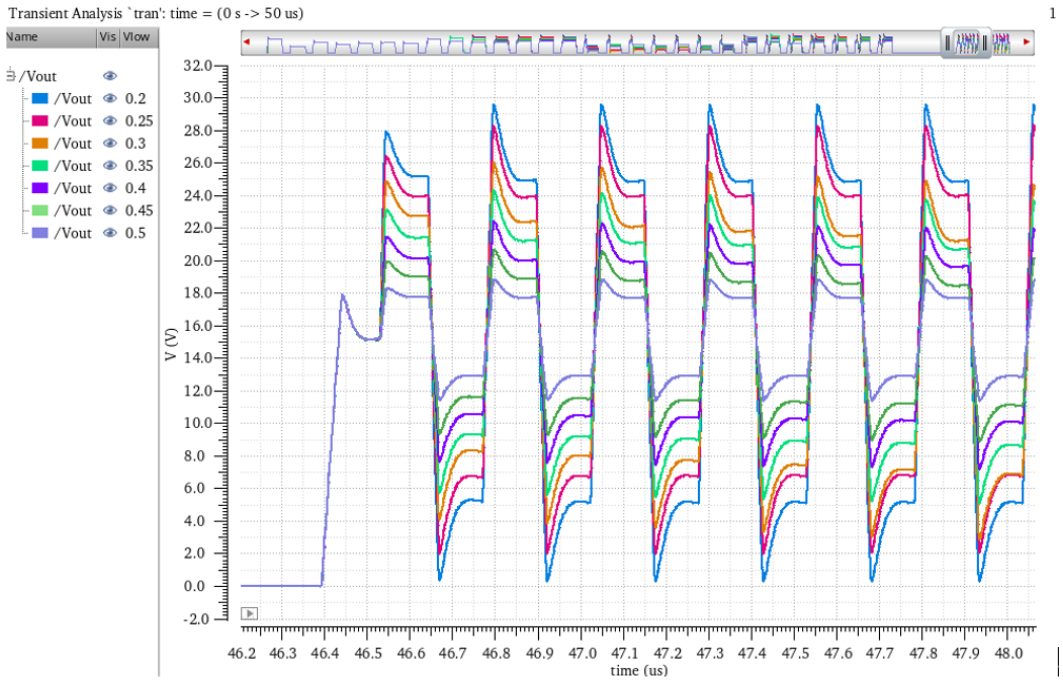


Figure 4.2: Transient simulation of the pulser output for different amplitude settings

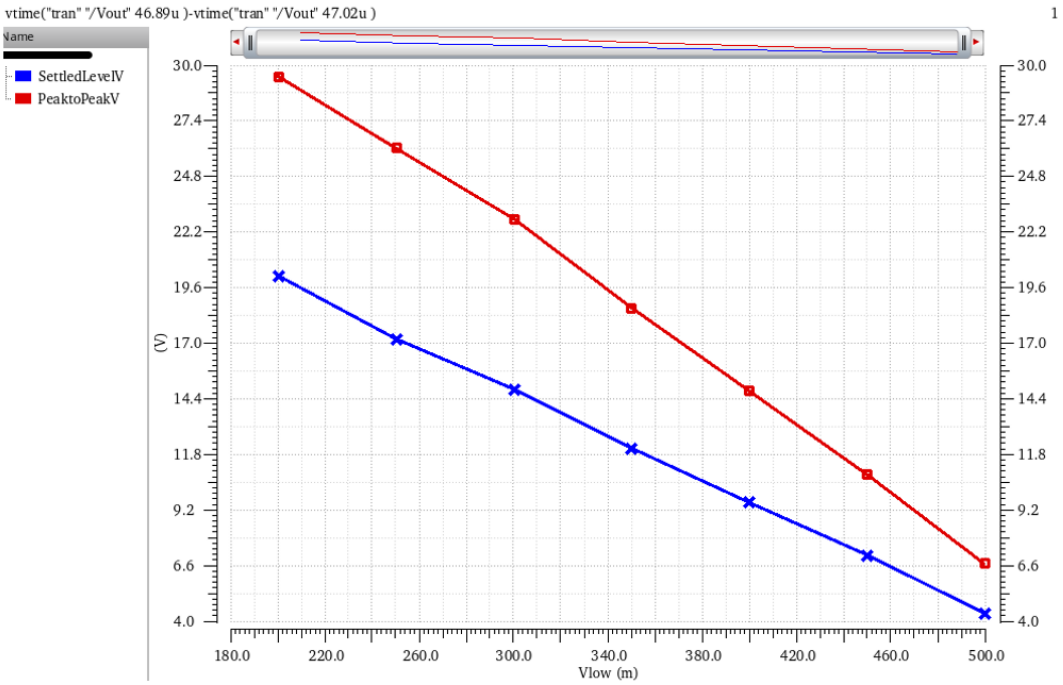


Figure 4.3: Peak-to-peak output voltage and the settled amplitude of the pulse for different levels of input

4.2 EVALUATION OF POWER CONSUMPTION

The total power dissipation consists of three parts: The power consumed by the HV output stage, that consumed by the gate-driving circuit, and that consumed by the calibration loop. It is obvious that the HV part consumes most of the power.

The power consumption of the output stage with different amplitude is shown in Figure 4.4. Ideally, this power consumption can be estimated by:

$$P_{supply30} = V_{supply} * I_{sr} * \frac{T_r}{T_p} \tag{4.1}$$

The calculation results are listed in Figure 4.4 as the theoretical value line at different amplitude levels from V_{low} = 0.2 mV to 0.5 mV. The difference between the calculation and simulation is that the slew current I_{sr} is not ideally amplified step current, and the waveform is not in an ideal square-shape and an accurately amplified value.

The power consumption of the PMOS and NMOS driving stages are shown in Figure 4.5. The value of the PMOS driving circuit should be decreased by 1/20 compared to output branch because of the amplification factor of the current mirror structure. The value of NMOS driving circuit is ideally about 1/12 of the output since the 5V supply of the NMOS driving circuit includes a 1x branch and also a 10x branch, which causes a 1/6 V_{supply} and 11/20 current. The results are similar with our assumption.

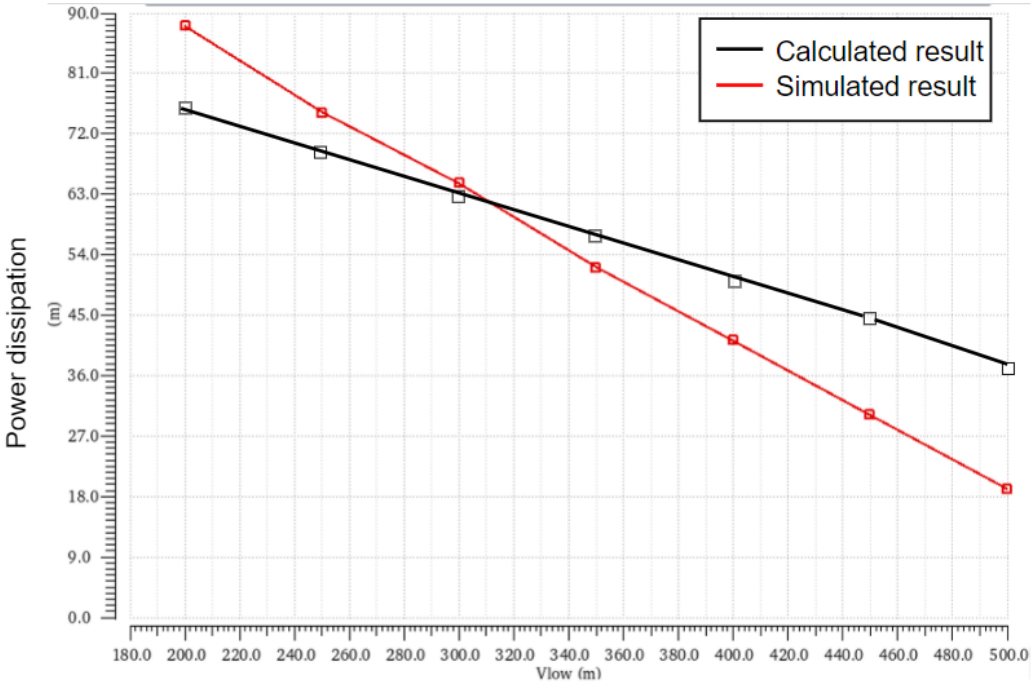


Figure 4.4: Power consumption of the output stage at different amplitude levels

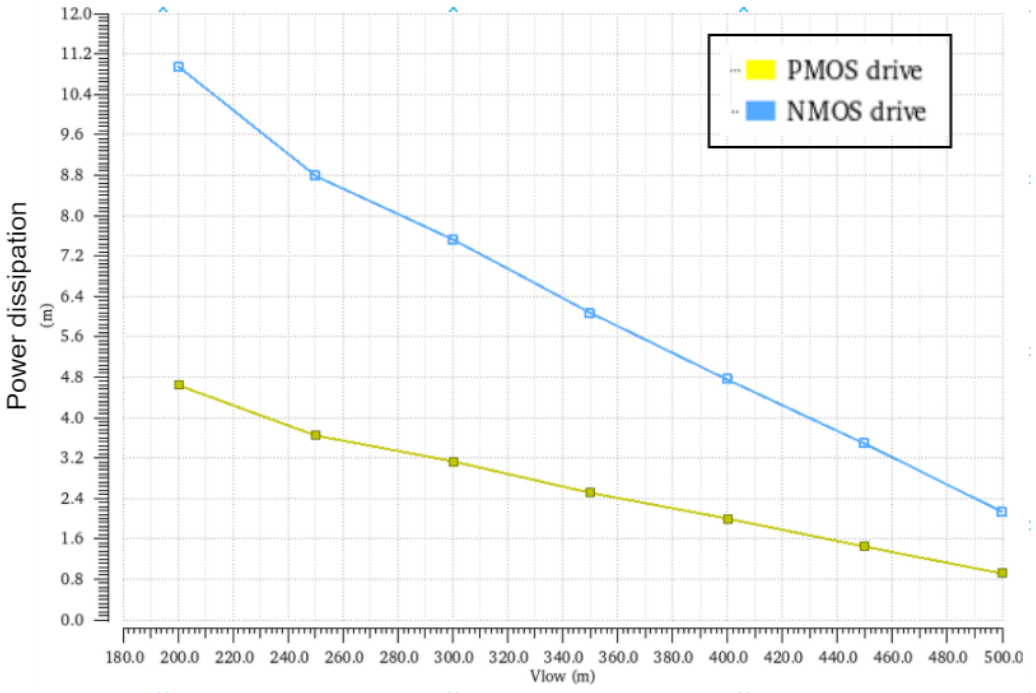


Figure 4.5: Power consumption of the PMOS and NMOS driving circuit at different amplitude levels

Take the third amplitude level $V_{low} = 0.3\,\mathrm{V}$ as an example, which gives a $22\,\mathrm{V}\,V_{pp}$ and a 15 V settled pulse amplitude. The HV transistors in the pulser are in the saturation region all of the time, which means a pure current-mode driving. The total power dissipation of the pulser is $64.77\,\mathrm{mW} + 3.15\,\mathrm{mW} + 8.54\,\mathrm{mW} = 76.46\,\mathrm{mW}$.

The value of the total power consumption of the design highly depends on the transducer parameters, the PRF and the number of the pulses in one T/R cycle. Assuming that the pulser is working at a pulse repetition frequency (PRF) of around 4 kHz, a 3-cycle pulse will consume 116.28 µW in transmission mode. This value seems to be low since this work is designed for short-time pulsing and the power consumption during receive mode is not included.

The relationship between the acoustic power and peak-to-peak voltage of the pulse is shown in Figure 4.6. Compared with Figure 3.1, the simulation result shows a lower but still reasonable power transition ratio. As shown in the figure, a 22 V V_{pp} will generate a 9 mW acoustic output power. The power efficiency of the third step will be $9/76.46 = 11.8\%$. Considering that power is lost on charging and discharging the transducer capacitance, the efficiency is reasonable. The power loss at C_p can be estimated by $C_p V_{pp}^2 f = 69.8\,\mathrm{mW}$. The acoustic power transition of the design at different amplitude levels can be seen in Figure 4.7.

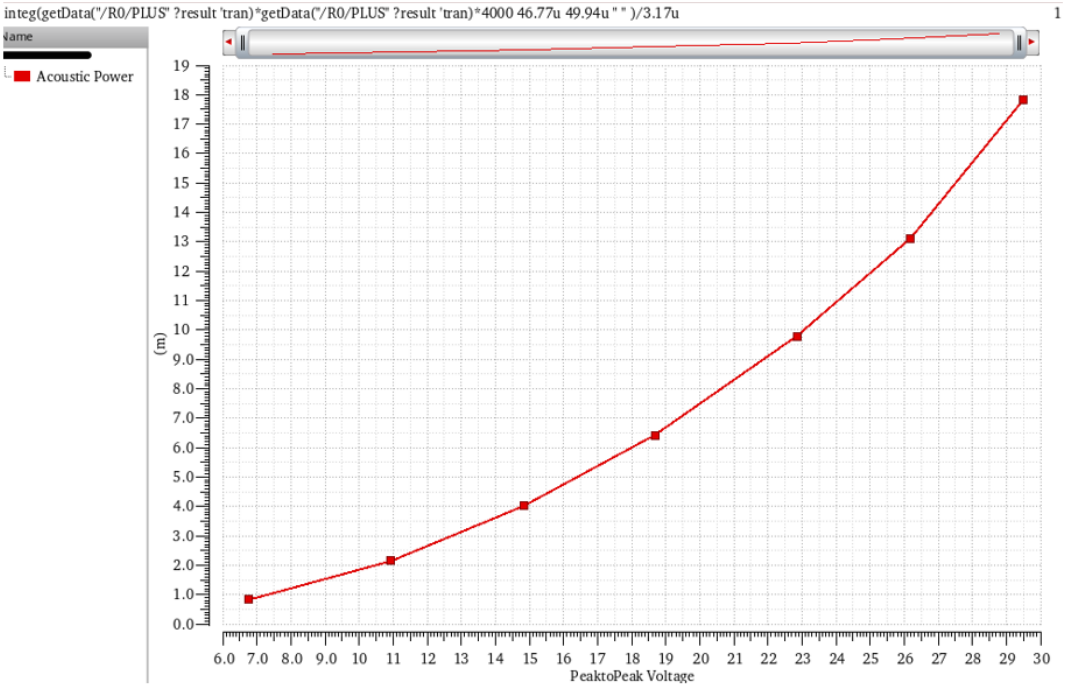


Figure 4.6: Acoustic output at different peak-to-peak output values

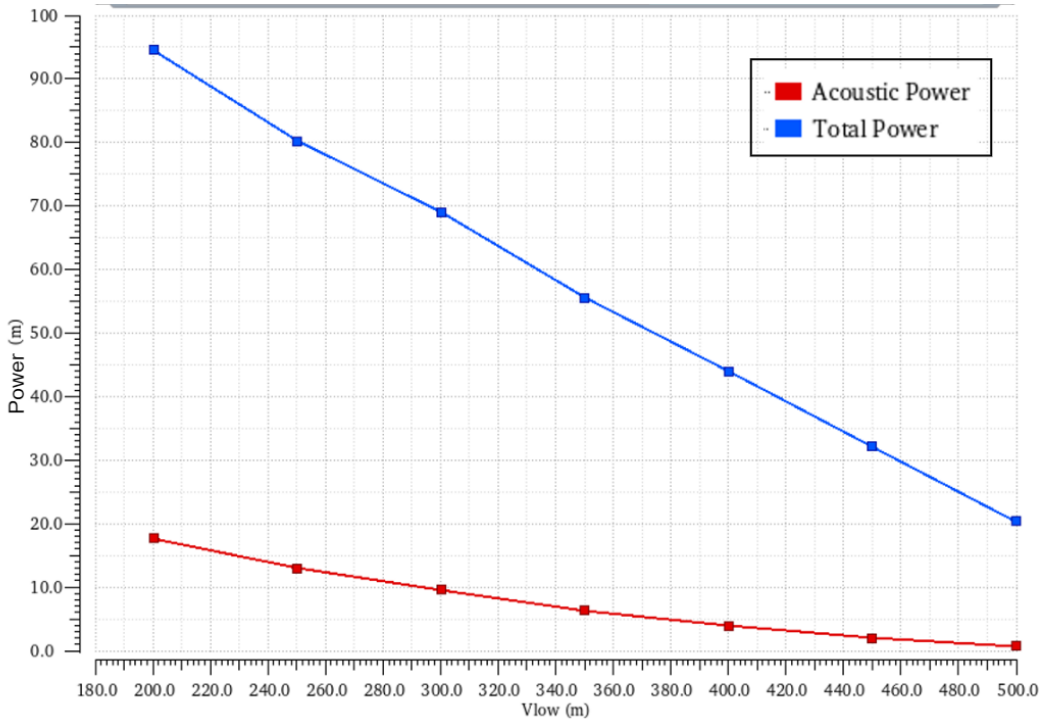


Figure 4.7: Overall power consumption and acoustic output power at different amplitude levels

5 CONCLUSION AND FUTURE WORK

5.1 CONCLUSION

The goal of the thesis has been to design a compact HV pulser with flexible amplitude modulation for apodization, to drive the elements of transducer arrays for 3-D ultrasound imaging.

In order to design this pulser, several contributions have been made:

- A current-mode pulser has been designed and compared with a conventional voltage-mode pulser. Current-mode pulsing provides the ability to change pulse amplitude more easily than voltage-mode pulsing. Moreover, it provides the possibility to generate bipolar pulses while using a single-ended HV supply. The driving circuit based on current-mirror structure drives the gate of the HV transistor at the output branch with controllable current levels.
- A digital calibration loop has been proposed to provide accurate amplitude control. In this loop, a current DAC is implemented to provide programmable input currents. These current signals are level-shifted to the HV pulser and converted into pulses with different amplitudes. A capacitive attenuator is designed and followed with a dynamic comparator to compare the attenuated output in the low-voltage domain with a desired reference level. The comparison result is sent to a digital control block and changes the corresponding codes of the current DACs.

Table 5.1 summaries the performance of the pulser design and compares it to the prior art.

Table 5.1: Performance summary and comparison with the prior art

	This work	[9]	[16]	[15]
Process	TSMC 180nm HV BCD	XFAB 180nm HV SOI	TSMC 180nm HV BCD	TSMC 180nm HV CMOS
Supply voltage	30 V	70 V	30 V	30 V
Amplitude modulation range*	29 V	138 V	Not applicable	Not applicable
Bipolar pulse	Yes	Yes	Yes	No
Pulse frequency	7.89 MHz @ 18 pF	2 MHz	9 MHz @ 18 pF	2 MHz @ 40 pF
Power consumption per channel**	<0.2 mW***	0.74 mW	1 mW	66.7 mW
# High voltage devices****	6	16	12	12
Estimated die size	< 0.04 mm^2*****	0.167 mm^2	0.09 mm^2	0.33 mm^2

*The peak-to-peak voltage at the maximum output amplitude.
**The value of the power consumption in different designs changes with the transducer used, the PRF and the number of the pulses in one T/R cycle rather than the pulser design.
***Excluding the power consumption during receive phase.

****Including HV MOS and HV-tolerant capacitors and resistors and excluding the devices in T/R switch.
*****Estimated by the layout of HV devices.

5.2 FUTURE WORK

Potential further improvements of this design can be summarized as follows:

- Applicability of the proposed current-mode driving for multi-level pulsing can be investigated. This may enable better control of the pulse shape, eventually contributing to better image quality.
- The on-time of the pulser transistors can be investigated as an alternative tunable parameter in the calibration loop, instead of the current level. This is similar to the approach presented in [Butterfly], and could help in the proposed current-mode pulser to further reduce size and power, as it may help to simplify the current-mirror-style driving of the output transistors.
- In the current design, errors in the output levels due to the finite accuracy of the calibration loop accumulate from cycle to cycle, as a result of which the design is only applicable for short-time pulsing. Additional calibration methods can be investigated to detect the drifting behavior resulting from this error accumulation.
- It is desirable to investigate ways to reduce the power consumption of the current-mirror based level shifters. They are still power hungry under high voltage.
- The receive chain should be implemented to make the pulse-echo measurement complete.
- The design has been implemented at the circuit-level. Currently, a die size estimate has been made based on the layout of the largest components in the design, but a full layout still needs to be made. Moreover, post-layout simulations should be done to verify the performance of the design including layout parasitics.
- The pulser design should be included in a prototype chip, which, in combination with a prototype transducer, can be used to demonstrate the pulser functionality in an acoustic experiment.

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